TU Delft

BAP Project

Solar Cell Balancing

Bachelor Thesis

Part 1

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Abstract

In this thesis an implementation is developed for a topology that solves the shading problems in solar panels. Shading even a single cell has a huge negative impact on the total performance of a solar panel and current solutions are either too expensive or wasteful. The implemented topology uses the differential diffusion charge redistribution method. This uses the capacitive properties of a solar cell to buffer charge for a short amount of time, then redistributes the charge to average out the performance over all cells. This breaks the weakest link dependency and greatly reduces the impact of shading. The net gain with this technology for one cell shaded in a 7 cell panel is about 86 % from the normal power against 2–4 % for a series stack. To distribute charge between cells, two series strings of PV cells have to be connected to a long stack of MOSFETs. Driving these MOSFETs poses a challenge because of the different voltage levels. This is solved using passives only in a clamping configuration. For the control system an algorithm is implemented that is capable of tracking the Maximum Power Point by controlling the duty cycle and the load current. The duty cycle is the switching ratio between the two series stacks and the load current is for this setup the current through a controllable dummy load.

Contents

1 | Introduction

1.1 Problem Definition

Our society and its increasing need for energy demands the development of new, or improved, sustainable technologies [17]. The growing number of PV installations in urban areas and therefore the amount of partially shaded solar modules (e.g. by chimneys, trees) is rising, making the shade induced power loss an increasingly large problem.

A solar panel is build up out of a set of solar cells connected in series. Shading a solar cell reduces its generated current, which means that it will deliver less current to the solar panel. When only a part of the solar panel is shaded, the shaded solar cells will limit the other cells in the panel. One consequence of the current limit implied by the worst performing cell is that all the other cells also operate at that current, causing them to work far off their maximum power point, greatly reducing string output. Therefore, the panel will roughly perform as bad as its worst performing solar cell, even if only one of the many cells is shaded. The same phenomenon in some degree occurs with production induced performance differences between the solar cells, called mismatch [24]. Without any safety measures, hot-spotting (cells dissipate energy as heat), or in extreme cases, reverse breakdown can occur because of this; both can permanently damage the solar cells.

Areas affected by partial shading such as periodic shade (chimneys and trees) [1] or soiling (bird droppings) [13] have a large impact on their system's power output and are nowadays therefore mostly nonviable for solar energy harvesting.

1.2 Thesis Synopsis

There are several workarounds for this problem, with bypass diodes being either very inefficient and individual DC/DC converters being very expensive due to the complexity and the number of components needed. More details on these technologies can be found in Section 2.2.

Diffusion Charge Redistribution[1] is proposed as a both affordable and efficient solution [6]. DCR is state of the art technology and a technical explanation of DCR can be found in Section 2.4. However, at its current state it is just an idea and a full hardware realization needs to be done in order to prove that the theory will work in practice. The goal for this thesis is to design hardware and software to show that (d)DCR is indeed a solution to the shading problem.

[1] Will be referred to as DCR from here on.

1.3 Thesis Composition

The four project members will all work on the SoCeBa[2] project. However, for the BAP course there has to be a well defined line between different subgroups. The thesis has been divided across two subgroups. One will deal with most of the hardware and the other will design and create all the supportive tools to investigate the properties of DCR and to enable the hardware to do what it is supposed to do.

For the BAP course, both subgroups will be evaluated separately. Part of the thesis also covers the system overview and integration and other general parts. To indicate which subgroup is responsible for which section a simple icon is shown in front of that section. For the most optimal reading experience, it is advised by the authors to read the full thesis in a (digital) colored format. Because it is obligatory to hand in two separated theses, each part of a subgroup can also be compiled to a standalone thesis.

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[2] **So**lar **Ce**ll **Ba**lancing

2 | State of the Art

2.1 Shading Solar Cells

Before talking about different solutions the problem that occurs while shading solar cells will be clarified. For now a photovoltaic cell will be modeled as shown below in Figure 2.2a.

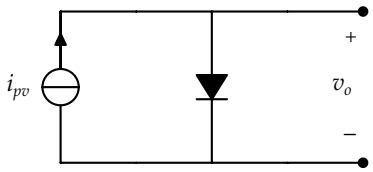
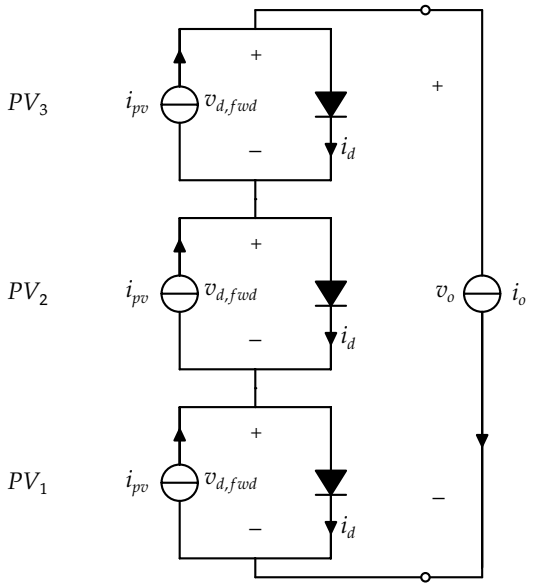
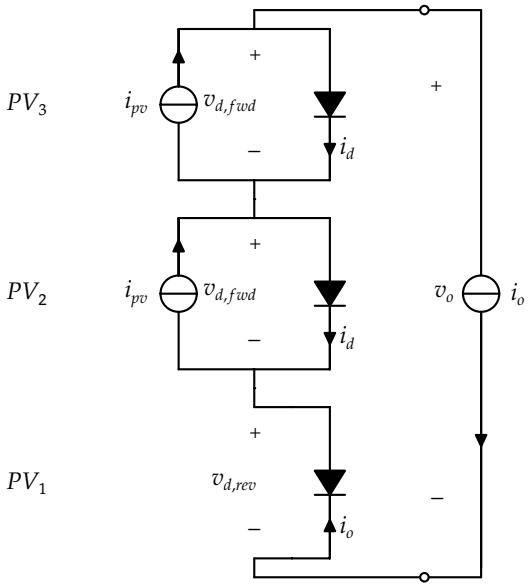


Figure 2.1: A simplified solar cell model

When light is cast on a cell, a photocurrent i_{pv} is generated. The size is dependent on the illumination level. So shading a cell causes this current to decrease. This generated current will put the diode in forward-bias causing some current to flow trough it. Assuming multiple cells are connected in series, the rest of the current will flow out of the output terminals trough the other cells of the stack. When one cell is fully shaded, its generated current i_{pv} will be zero. Since all the cells are connected in series and the other cells still generate a current, a voltage will be forced across the shaded cell. This will put the diode in reverse-bias causing it to dissipate a lot of power. Figure 2.2 show a stack of three solar cells. This general relation hold $i_o = i_{pv} - i_d$ and for the case in 2.2a $v_o = 3 \cdot v_d$. When PV_1 is shaded in 2.2b, the stack current i_o will reverse bias the diode. Putting a large reverse voltage across diodes causes them to dissipate a lot of energy.



(a) A stack of simplified solar cells



(b) A stack of simplified solar cells with a fully shaded cell

Figure 2.2: A series stack of three solar cells in two different illumination states.

2.2 Current Topologies

There are several methods to reduce the power loss when shading occurs with different levels of complexity and efficiency. These will be discussed in this section.

2.2.1 Diodes

One method to overcome the implied current limit is to bypass the limiting cell [28, 22]. The current can then flow through the diode, allowing for the stack current to be higher. By using this method some power is dissipated in the diode. This power can be dissipated away from the cell which reduces thermal stress, but power is lost none the less. This drawback can be overcome by using an active diode that also incorporates a MOSFET. This MOSFET has no fixed voltage drop and has only $I^2 \cdot R_{DS,on}$ losses, where $R_{DS,on}$ can be very low [23]. One other drawback of this method is that the maximum power point tracker[1] has to track a non convex function as switching off cells can, but might not, result in higher power output. The MPPT algorithm can easily get stuck in a local maximum. And last but not least the power of the bypassed cell is discarded. Each bypassed cell makes no contribution even if it operates at say 80 % of the average cell power.

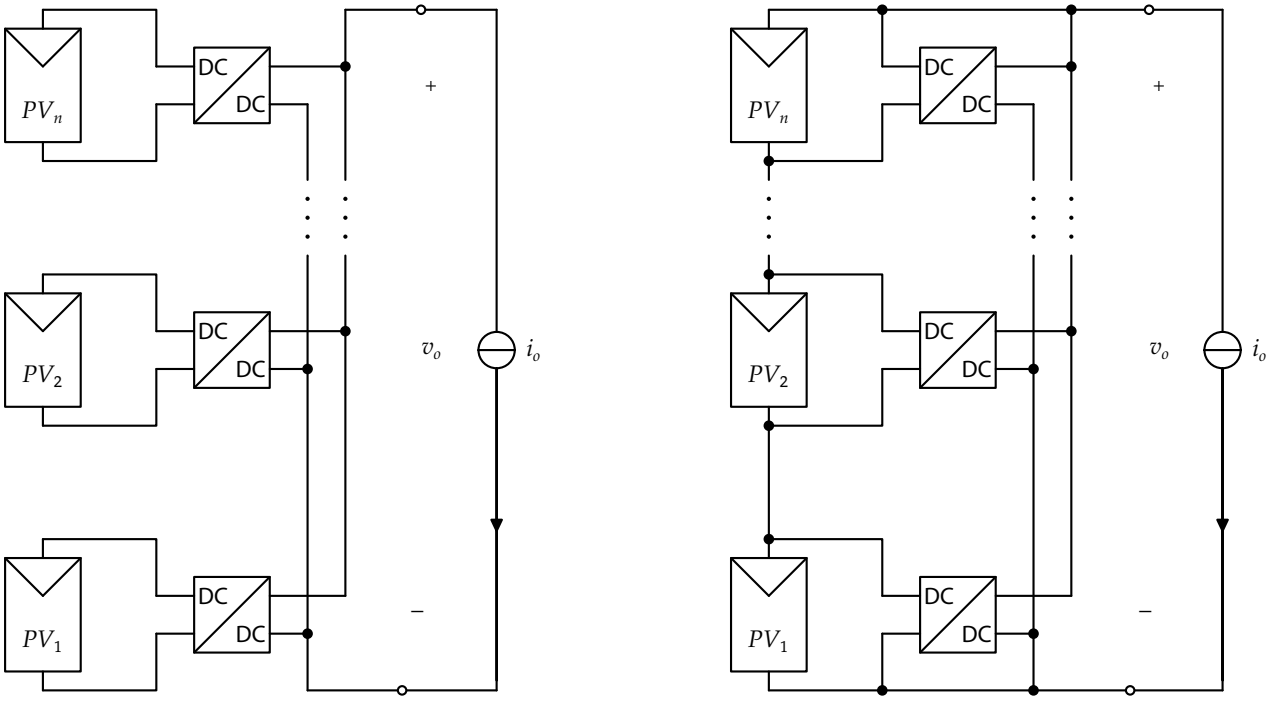
2.2.2 DC/DC Converters

A more complex approach to reduce the mismatch effects is using DC/DC converters, either per cell or per substring. Both configurations are shown in Figure 2.3a. This method allows to use the maximal amount of

[1] Will be referred to as MPPT from here on.

power available by every PV cell [14]. Each PV cell has a module that converts the output power to either a constant current or a constant voltage output, as can be seen in Figure 2.3a.

Although this approach removes the drawbacks of the diode approach and extracts the maximum amount of power from each individual cell, it is a complex and expensive solution. To reduce the processed power per DC/DC converter, a bidirectional DC/DC approach can be used. The DC/DC converters now only have to convert the power difference between cells, see Figure 2.3b. While the DC/DC converters become smaller, the complexity increases. Therefore this technique is more viable to only be used in conjunction with substrings. The substrings are generally optimized but the cells within each string still suffer from uncompensated mismatch.



(a) Parallel balancing

(b) Bidirectional balancing

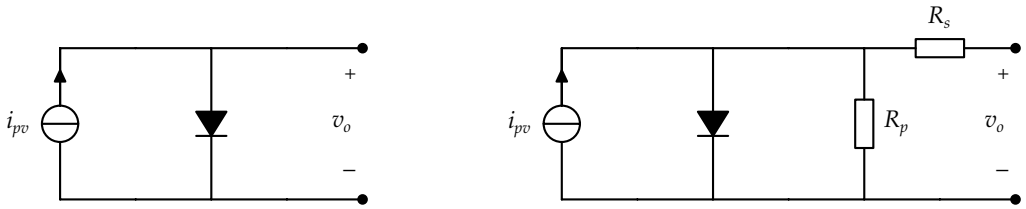
Figure 2.3: Two different Solar Cell Stack configurations.

2.3 Solar Cell Model

For simulating the effects of a balancing system, a model of a solar cell is needed. Of course there are multiple models to describe the behavior of a PV cell, all varying in accuracy and complexity. To simulate different irradiance levels of a solar cell the Ideal solar cell model model can be used. Sweeping the i_{pv} source emulates different irradiation intensities.

To be able to simulate I-V curves and operate the cell in its maximum power point, the losses have to be taken into account. This can be simulated by adding the shunt and series resistances to the model, the result is the Basic solar cell model of Figure 2.4b. The shunt resistor models the leakage in the junction, while the series resistor models the PV metal layer, termination and lead resistance. The parameters of this model can be estimated by the techniques proposed in [27, 8]. Due to the transport of charge carriers, a pn-junction has a diffusion capacitance. Since a PV cell has a lot of junctions in parallel, this adds up to quite a significant value. For doing transient simulations, this C_d has to be modeled as well (Figure 2.5) [6]. There are multiple ways to measure the

impedance of the PV cell [3, 21].



(a) Ideal solar cell model (b) Basic solar cell model

Figure 2.4: Two simple solar cell models

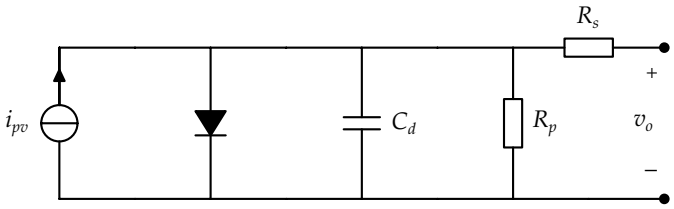


Figure 2.5: Transient solar cell model

Of course more complex models do exist, one example is the double diode model. This model is used to account for the recombination current at a wider temperature range. The differences between the power output of both models are relatively small ($\approx 1\,\%$) [20]. Since temperature effects have nothing to do with the research in the report the Transient solar cell model suffices.

2.3.1 Model Parameters

Now a suitable model has been chosen, its parameters have to be set. PV cell and module manufacturers often only specify a cell output specification in combination with an I-V curve. Using [18] an algorithm is built in Appendix A that can fit the parameters.

2.4 DCR development

2.4.1 Charge Redistribution

With the topology shown in Figure 2.6, charge is taken from cells with higher output and moved to the cells with lower output [6]. The average current through this lower performing cell can then increase, allowing for higher string currents. This topology is discussed in [25] and uses a separate charge storage string either with either capacitive or resonant storage elements to move charge.

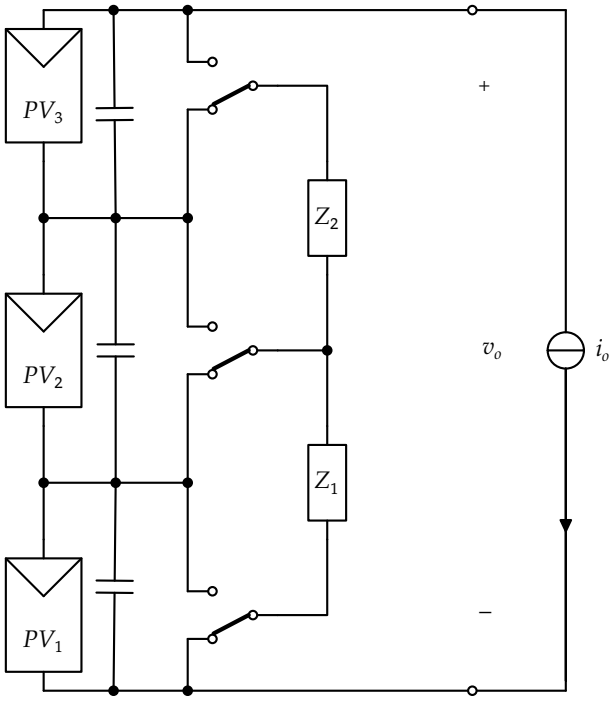


Figure 2.6: Charge Redistribution

2.4.2 Diffusion Charge Redistribution

The Diffusion Charge Redistribution[2] topology is an extension of charge redistribution using the junction capacitance, also called diffusion capacitance, of the PV cells (C_d in Section 2.3) instead of an external capacitor.

This diffusion capacitance was previously seen by the industry as parasitic but can be helpful for DCR. The DCR topology can be extended by also using PV cells for the flying impedances (Figure 2.7), allowing for a lower component count and using almost twice as many PV cells while maintaining the same amount of switches [6].

[2]Will be referred to as DCR from now on

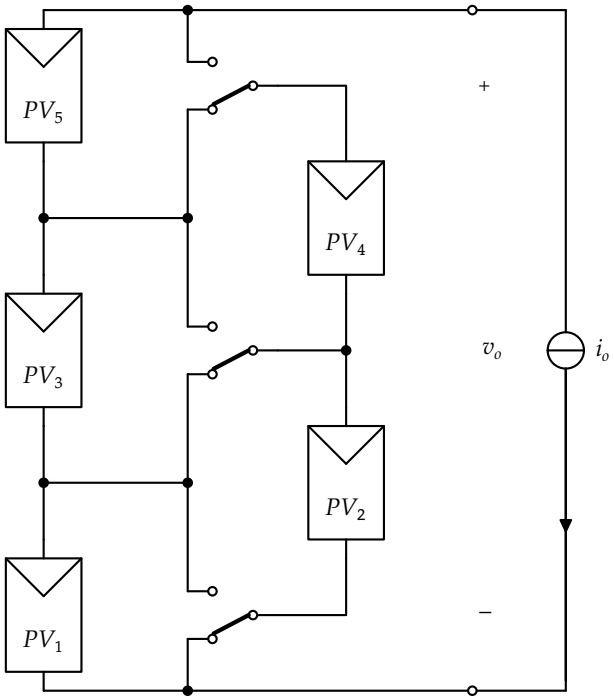


Figure 2.7: DCR topology

2.4.3 Differential Diffusion Charge Redistribution

Subsequent research by the same group led to the conclusion that the power delivered by the flying PV string is below optimum, as the whole power of this string needs to pass through the switching elements [7]. A solution for this is called Differential Diffusion Charge Redistribution(Figure 2.8). The switches in combination with the LC filter will cause two continuous currents to flow through both of the strings. This means that the switches, between the two strings, only have to carry the energy required to redistribute the energy of the string, but not the common flying string current. To maintain a single current output a current sharing bridge is added. By varying the duty cycle and output current the individual PV cell, string currents can be independently adjusted [7].

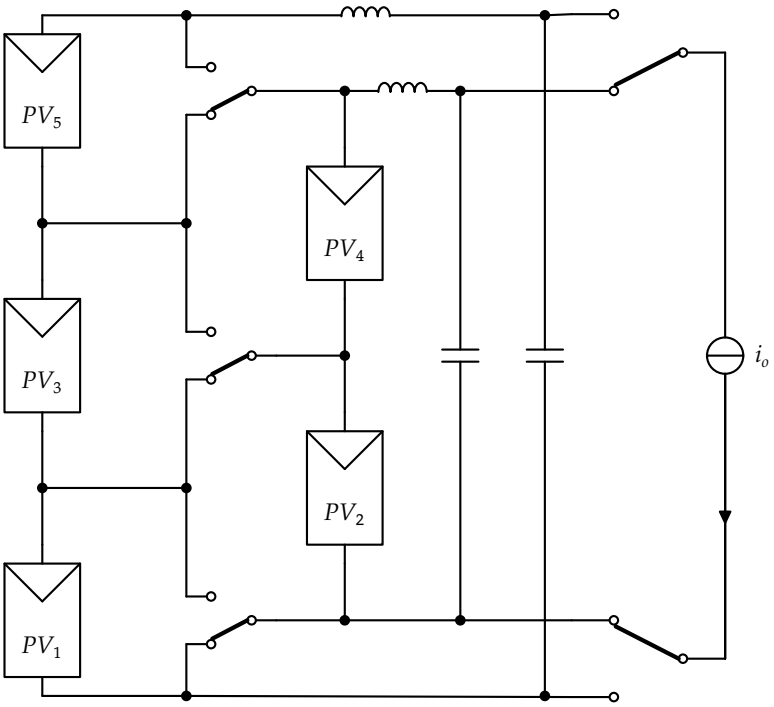


Figure 2.8: dDCR topology

2.5 Gate Driver Topologies

None of the switches required for the dDCR topology are configured like classical MOSFET situations. Classical cases would be:

- Low-side only switching, with sources referenced to ground.
- Full or half H-bridge switching where bootstrapping is allowed.
- High side switching at low frequencies where delay is not an issue.

But all the MOSFETs are configured in series, so the MOSFET gate voltages are at many different levels. The same situation arises with Charge Redistribution (see Section 2.4.1) and a same approach can be used. Clamping devices turn on in alternate phases to directly connect the gate of higher-voltage devices to the appropriate source node in the 'off' phase [25], this sets the DC level. A common gate driver can be coupled to all gates by capacitors as was implementend on the ASIC.

3 | Requirements

3.1 Introduction

As stated in Chapter 2: 'State of the Art' there are clearly some problems concerning shaded solar cells. It is common knowledge that even a little shade has major effects on the performance of the whole panel. There are already some solutions available on the market, but most of them do not qualify as the most optimal solution. Better solutions are under development but it will take some time before they become commercially available. The mindset behind this project is to make a bridge between those ends: a commercial solution that integrates new technologies. Since the limited time span of this project, only a part of this idea can be realized. The main goal is to make a first iteration prototype for a market viable solution to show what new technologies can accomplish. The detailed requirements for this will be discussed in the next sections.

3.2 Functional

To provide a new commercial solution for a problem some important requirements must be met. Most important is the price. A product might be more efficient, but if it is not worth the price, it will not be adopted by the market. In a similar way the product must be easy to use and to integrate in the photovoltaic system.

To show the viability of the new proposed solutions, a product and test setup have to be designed and build. So to design a working product, first its viability has to be proven by simulations and then the test cases for a real life product can be set. With these cases both a product and test setup can be made.

Since hardware development usually happens in multiple iterations, it will not be realistic to demand a neat, fully working product. The primary goal should be to make a first iteration. This means to build a prototype and determine all its major problems. Some of them can be solved, but on other compromises are needed for now. All these major problems and possible future pitfalls have to be researched now so there will be a plan ready for the start of a possible next iteration after the BAP project.

Since building a full scale test setup can be quite expensive, a small scale test setup is allowed. But for every compromise made for this setup a large scale alternative must be provided. It is very important to keep track of all the large scale alternatives, since the fact that down scaling might have an (seemingly) adverse effect on the viability.

Table 3.1: Result requirements

Number	Name	Description
1.1	Price	The price should be kept to a minimum, and below an additional 3$ per cell to allow for a larger customer segment.
1.2	Installing	The product should have a suitable connector to be easy to install or remove.
1.3	Life Expectancy	The product should at least match half the life expectancy of an average solar panel: 25 years.
1.4	Scalability	Solar panel manufacturers make panels up to 96 cells, the product should be able to scale to that size.
1.5	Efficiency	The product should be more efficient than bypass diodes over its life time.
1.6	Dimensions	The product may not take up too much space with respect to the panel.
1.7	Speed	The tracker should take at most 1 second to meet its MPP.
1.8	PCTestGround	Must be able to run same code as MCU.
1.9	SoCeBa.Director	Must be able to build a power space from individual points received in random order.
1.10	Load resolution	$\leq$ 10 mA

3.3 Ecological

The lifetime of SoCeBa must be matched to the lifetime of the solar modules it is mounted on. This way no extra maintenance will be induced by the addition of SoCeBa and the costs can be kept as low as possible by not over designing the components on lifetime. Given the current average lifetime of 25 years for solar modules being installed nowadays [11], one can conclude that SoCeBa should be dimensioned for an expected lifetime of more than 25 years.

It could also be argued that the lifetime of SoCeBa should be more than its payback time. However, the payback period of the device will likely be shorter than the lifetime of a solar module and therefore maintenance would be required if SoCeBa breaks before the solar module.

3.4 System

Table 3.2: System Requirements

#	Requirement	Values
2.1	Insertion loss	$\leq 1\,\%$
2.2	Redistribution loss	$\leq 15\,\%$
2.3	Tracking speed	≤ 2 s to MPP.
2.4	Tracking efficiency	Collect at least $\pm 95\,\%$ of the total energy.
2.5	Connector	Must be removable.
2.6	Frequency Filtering	Charge distribution switching frequencies should not be in the output.
2.7	Output Current	Output current should be near the sum of the two stack currents in value.
2.8	Output Power	The output power should be proportional to the shaded area with a deviation of $\leq 10\,\%$.
2.9	PWM Duty Cycle	Error should be $\leq 1\,\%$.
2.10	MPP deviation	Algorithm should track within $\pm 5\,\%$ of the MPP.

4 | Challenges & Proposed Solution

4.1 Introduction

As can be read in Section 2.4, (differential) diffusion charge redistribution seems like a good solution to the shading problem (Section 1.1). The main purpose of this research is to proof the concept developed by Chang [7] and to transform it into a working and market viable solution. None of the implementation details are state of the art and the focus of this report is to provide the reader with an implementable version of dDCR as shown in Figure 2.8. Below the challenges each group is facing, are listed.

4.2 Hardware

The hardware improvements required are mostly with respect to efficiency, as the circuit used by Chang [5] uses mostly DC/DC converters to supply the MOSFETs with gate driver power. This is a rather inefficient aproach. The main challenges are:

4.2.1 Current Sharing Signaling

The MOSFET configuration of the current sharing subcircuit is not a classical one. The signals need to be levelshifted, both fast and properly timed but this must not cost too much energy or distort the signal too much.

4.2.2 Balancing Driver

With many MOSFETs in series there is also no trivial solution to driving them. Besides the unusual configuration they also need to be driven very fast and with minimum rise time to avoid the lineair operation region. Due to the unusual configuration precautions must also be taken to enforce the proper DC level on the MOSFET gates.

4.2.3 MOSFET Optimisiation

For N solar cells, there are $N+1$ MOSFETs. That means that any avoidable losses when optimising the MOSFETs actually cause N+1 times as many losses compared to one MOSFET, making this optimisation much more critical.

4.2.4 Current Path

Because the MOSFETs are configured in series, the current path of the gate drive current could become unacceptably long. It is well known that the gate driver current paths must always be as short as possible [16] to avoid oscillations and delays.

5 | Power Space Simulation

5.1 DCR vs dDCR Verified

Simulation and verification whether the statements made by Chang [7] are valid is not within the scope of this thesis. The companion thesis [10] explores the MPPT operation and shape of the control space. For this thesis only component level simulations are done and dDCR is assumed to be a working topology, which is also proved in the companion thesis.

6 | Design

6.1 Charge Redistribution

The design will be for a configuration of 7 cells, or '4-3'. This number was chosen because it was assumed to be representable for both middle and endpoints of the stack. There are several options to consider for implementing the switches that allow for current sharing, see Figure 6.1, all of them will be explained below.

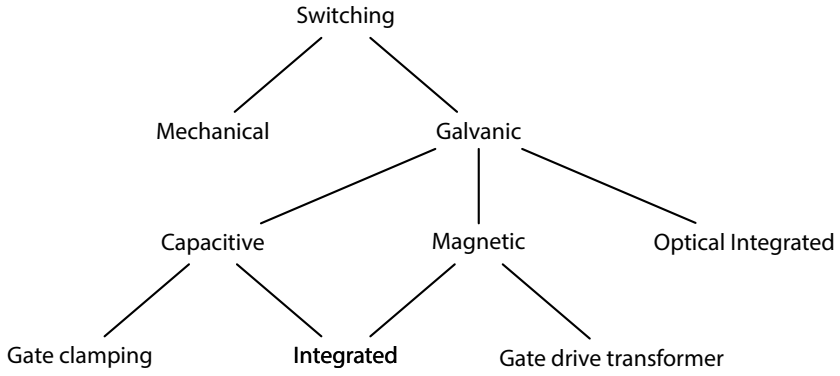


Figure 6.1: Overview of possible options for implementing the switches

Mechanical Rotor

A mechanical commutator with a rotor can switch this many contacts. It is however a very large and inefficient solution that is easily subject to wear. It may be clear that this is not a viable solution.

Gate Driver Transformers

Gate drive transformers use magnetic coupling for isolation and can be useful as each output is isolated from the other, allowing easy level shifting. Theoretically one could also add as many windings as needed to drive the whole stack. In practice the parasitic effects on this many windings is significant, and with the amount of taps needed for one solar module these effects become prevalent. Sinking current, sourcing current and ringing effects with large amount of taps are a too large obstacle.

MOSFET with Individual Integrated Drivers

From a switching point of view it would be optimal for each MOSFET to have its own gate driver. Two problems arise: the power needs to be transferred to each gate level and the signal needs to be level-shifted. The level shifting can be implemented with a central transformer as the design is much more relaxed for smaller signals but also with an integrated solution. The working principle of these small ICs are also either optical, magnetic or capacitive. However, getting power to each gate level requires a small DC/DC converter per cell, increasing the complexity beyond what is reasonable. In this case it would be easier to provide a DC/DC converter to process the full power for each PV cell instead, as stated in Section 2.2.2. This would be a less complex and more efficient solution.

MOSFET with Clamping Devices

As proposed before, the solution that is most likely to be optimal would be using gate clamping devices and transferring the driving energy capacitively. A very similar solution has already been implemented on an ASIC [25] and a discrete solution will be investigated in the next sections.

6.1.1 Clamping

To solve the clamping solution on a more detailed level, the schematic of Figure 6.2 was invented. During the off-period of a switch, another switching device can set the DC level of the capacitively shifted gate drive signal. Q2b performs this function for Q2a. The DC difference is blocked by C2. Logically small MOSFETs can be chosen to set the DC level. (like all the 'b' MOSFETs for all the 'a' MOSFETs.) When Q2a is closed, Q1a is driven open and the drain level of Q2b is approximately at the same level as the drain of Q1a. So Q2b is also driven open, setting the 'off' voltage level at the gate of Q2a. During the next phase this also happens for the MOSFETs of the other phase, as the structure is symmetrical. R2a and R2b are resistors required to dampen oscillations on the gates [16] and limit driver current. The gate current return path needs to pass through the PV modules. The cable length of the modules could drastically reduce performance, so initially extra bypass capacitors will be mounted close to the board to provide this current path. Another benefit would be increased cell capacitance.

Q0 and Q1 do not require a clamping structure as they are at the same level as the gate drivers.

6.1.2 Oscillator and Drivers

The signals driving each of the MOSFETs group in antiphase need to be referenced to the lowest level of the stack to which the drains of the MOSFETs are connected. If this were not the case and U2 would be at the same level as U1 the driving signal would be corrupted. Because when Q0a switches off, Q1a switches on some time later while the voltage across Q0a drops. This causes an extra positive going spike on the gate driving signal, which pushes Q1a in linear mode shortly before it is properly activated by its driver causing exessive dissipation.

Now that the level of the gate driver is specified, it is obvious that again some level shifting is needed. The oscillator will be at one of the two levels, and at least one signal requires shifting. When looking closer to Q0a and Q1a, it can be seen that they are arranged in half-bridge mode and a classical driving topology can be employed. Half-bridge drivers with integrated oscillators and dead time circuits are available on the market

which are perfect for this purpose.

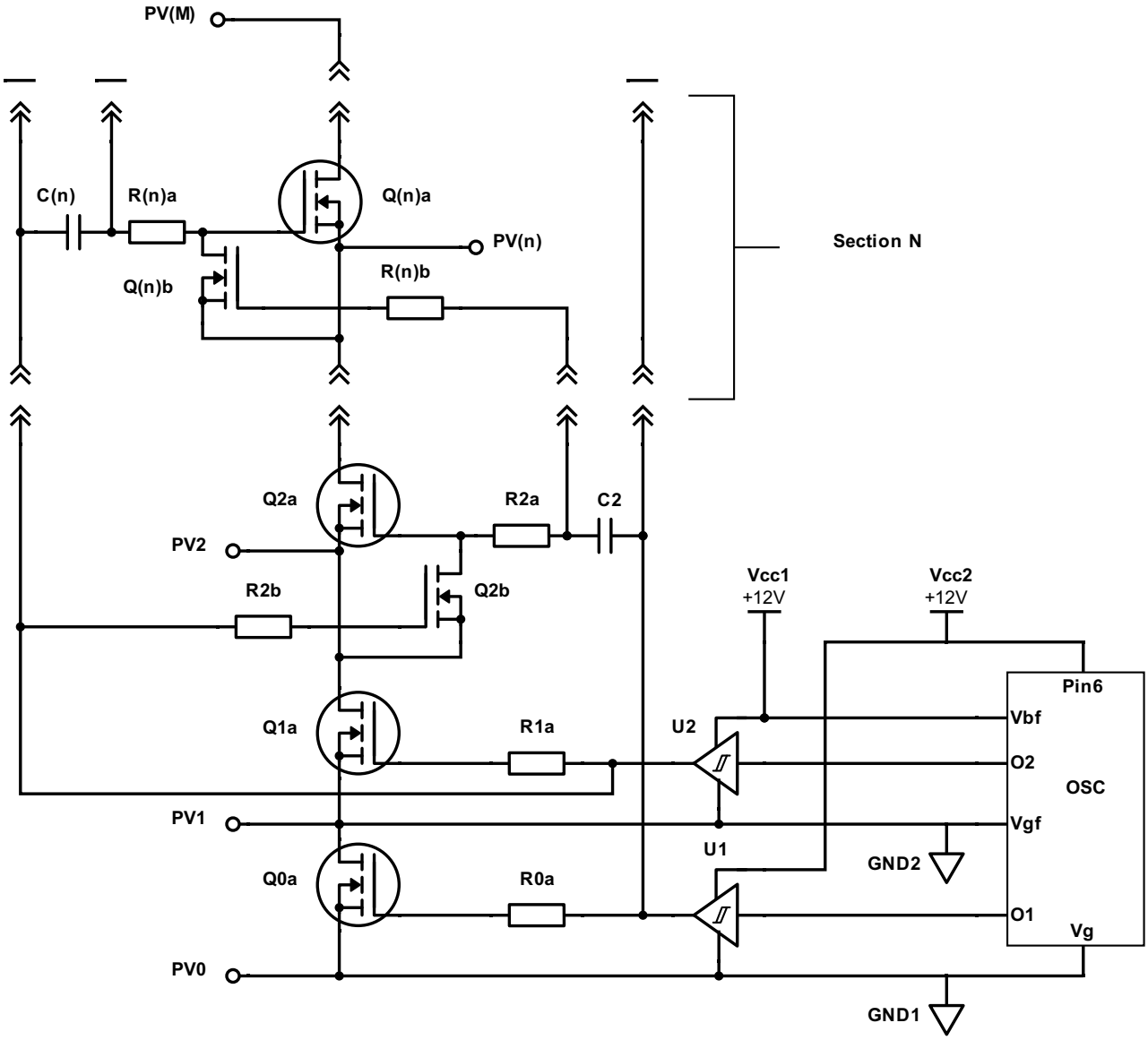


Figure 6.2: Switching string bottom part with one additional section shown. This section will be repeated N times. Power MOSFETs are encircled for contrast with the small clamping MOSFETs.

6.2 Current Sharing Switching

To draw current from both stacks with a single load, current sharing must be implemented as proposed for dDCR [7]. The proposed solution is closely related to Figure 6.3. By varying the duty cycle the current drawn from the supplies can be changed, see below.

$$I_{V_1,RMS} = \sqrt{D} \cdot I_{peak} = \sqrt{D} \cdot I_o \qquad I_{V_2,RMS} = \sqrt{(1-D)} \cdot I_{peak} = \sqrt{(1-D)} \cdot I_o$$

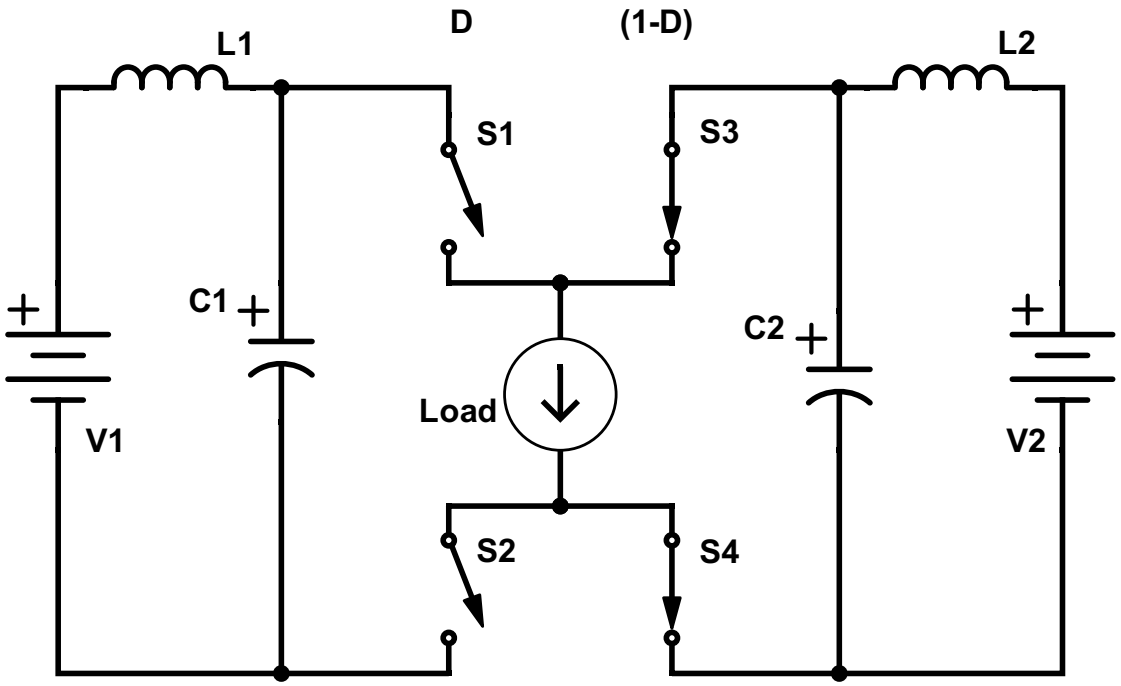


Figure 6.3: Current sharing simplified schematic

The filters ensure that the current drawn from the PV stack is continuous instead of a square wave. It should minimize the current ripple through the solar cells, while also keeping the output voltage relatively constant.

6.2.1 Switch Driving Options

The main design problem of this section is that the bridge configuration is not a classical one. One such classical topology is the full H-bridge and has the MOSFETs on the same positions. Unfortunately internal connections differ making the corresponding classical solution, bootstrap driving, impossible. A mechanical rotor would again be too heavy and unreliable, while a gate drive transformer does not work well with wide varying duty cycles due to its constant volt-seconds requirement. This requires a very high voltage output when the duty cycle is low, else the transformer saturates. The high voltage output can destroy the gates of the MOSFETs, so the remaining solution requires individual MOSFET drivers with level shifting. The options are as follows and follow from the same tree of Figure 6.1:

Optical

Optocouplers at the required speeds are reasonably priced, but require relatively large LED currents and are bulky. While they are not needed in large numbers it remains a disadvantage. However, it is a reasonable solution nonetheless.

Integrated Circuit

Digital isolators in integrated circuit form are based on magnetic, capacitive or optical coupling and less subject to aging but more expensive than the discrete solutions. Some digital isolators also have an integrated DC/DC converter in the package which could supply the required current for the driver. This converter has small coupling coils inside the package. Unfortunately the integrated converter is usually very inefficient ($< 25\,\%$). Devices incorporating such a DC/DC converter are even more expensive because special manufacturing techniques are required.

6.2.2 Discrete

During a brainstorm session a solution using a P-MOSFET in common gate configuration came to mind. This solution requires for the controller unit to be connected to the positive output terminal of the load, but this also eases the signal transportation to the upper two MOSFET drivers and allows the controller to use the same supply rail as these upper drivers. This solution will be used in the design. First, a few observations can be made.

- The bridge is symmetrical and the case can be considered for just one half. Figure 6.4 displays one such half.
- The lower MOSFET Q2 can be driven from the same supply as the driver for one phase of the balancing string (Figure 6.2, U1 or U2) since PV- (Figure 6.4) is connected to either PV0 or PV1 (Figure 6.2). This way two additional power supplies can be eliminated.
- A separate supply to drive the top switch Q1 is required for every case.
- Both top switches can be driven from the same power supply as their sources are connected; the lower switches require individual level shifters as their sources are not connected.
- The output voltage can not be used as power supply for the MCU or drivers as it may fall below the minimum operating threshold of the MCU or drivers, causing the system to shut down.
- It would be beneficial to reference the controller (MCU) to the drains of the upper switches as drawn in Figure 6.4 instead of to the negative terminal of the load. The latter would intuitively be the first choice as the controller has to send a current command and measure the output voltage. By using two low power inverting amplifiers, these signals can be level-shifted as well and will be discussed in Section 6.3. This removes the need for an extra power supply referenced to the negative load terminal.

With these constraints a simple solution is possible using two resistors and a MOSFET. The MOSFET is configured as a common gate amplifier, passing the signal to the lower level. If R1 and R2 are chosen to be the same value they will both have the same voltages across them. $V_{R_1} = V_{U3,High} - V_{th,Q3} = V_{R3}$ for their currents are equal. Even if the load voltage is zero, the level shifter still works. Assuming that Q3 conducts, $V_{U3,High}$ divides equally across R1 and R3 and is therefore $\frac{1}{2}V_{U3,High}$. If the $V_{th,Q3} < \frac{1}{2}V_{U3,High}$, $R_{DS,on}$ is significantly small to allow proper signal propagation. For this reason the input voltage of the level shifter is taken from the output of the gate driver, as the MCU output voltage is either 5 or 3.3V, while MOSFETs are usually driven with 8-12V.

If the output of U3 is low, V_{GS} is always zero and no current is conducted, transferring the low command regardless of the output load voltage.

Schmitt trigger input gate drivers are beneficial to remove any noise caused by $C_{GD,Q3}$ or $C_{GS,Q3}$. Another requirement is that the MOSFETs are never on at the same time. A lot of energy would be lost by equalizing the

voltages on C1 and C2 of Figure 6.3, as well as short-circuiting the lower PV cell. Dead time must be implemented to avert this issue.

R2 and R4 are standard gate stopper resistors.

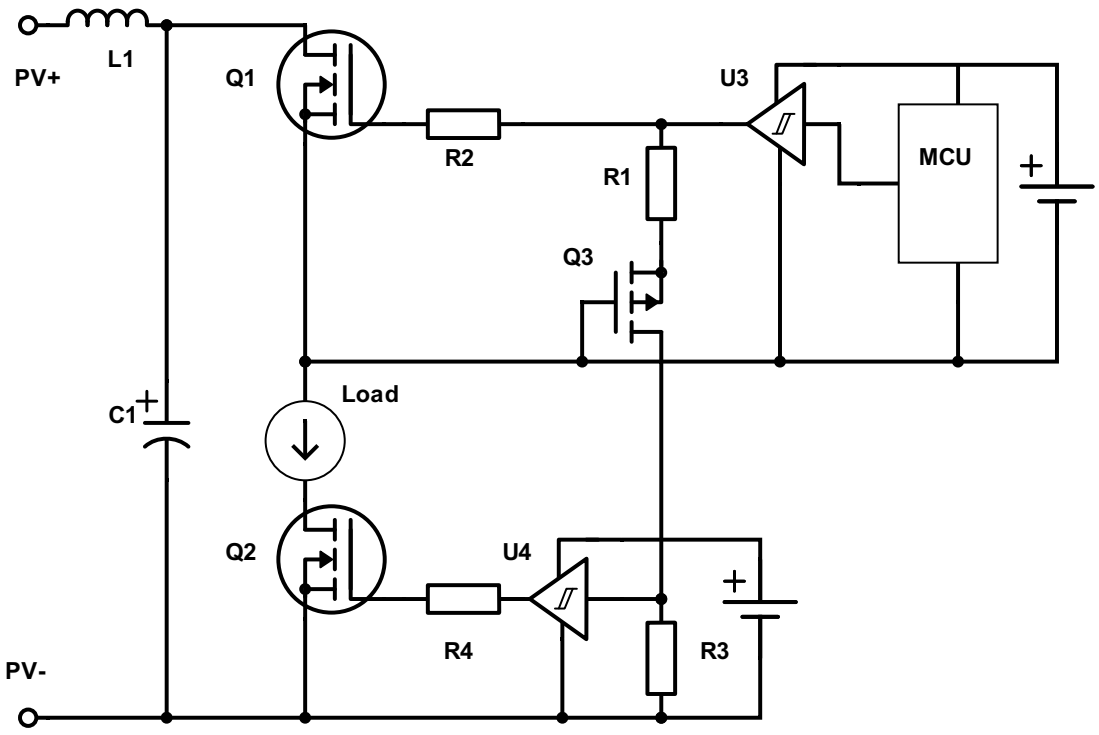


Figure 6.4: One half of the symmetric current sharing schematic

6.3 Current Sharing Analog Level Shifter

As explained in Section 6.2.2, the reference voltage of the MCU is connected to the drain of the upper switches. The control system needs to be able to control the I_{load}. The input signal for the load is referenced to the negative terminal of the load (and thus the drain of the lower switches). Therefore a circuit is needed that shifts the V_{i-cmd} signal down. The easiest solution for this is to use an analog isolator. These are chips that will just output an (amplified) isolated signal related to the input signal. The cheapest IC on Farnell with this function is the AMC1100, at a price of 2.30€. It has to be noted that these cheap ICs also need an external isolated power supply. Adding these costs makes this solution quite expensive. A better solution has to be found to comply with requirement 1.1 of Table 3.1.

Down Shifting

For down shifting a current signal, the same current buffer topology can be used as explained before. Using the common gate amplifier again, a current signal can be shifted down easily. The voltage signal from the microcontroller can be converted into a current signal by a simple resistor. However, V_{GS} across the MOSFET causes an offset. This offset can be eliminated by using a difference amplifier. The input signal V_{i-cmd} in Figure 6.5 will

appear also over $R3$ as shown in the following derivations.

The KCL at the non inverting input terminal gives:

$\frac{V_{in}-V_+}{R1} = \frac{V_+-V_{DG}}{R2}$ which can also be written as $V_{in} = V_+(1 + \frac{R1}{R2}) - V_{GS}\frac{R1}{R2}$

The voltage divider at the inverting input terminal gives:

$V_- = V_o\frac{R5}{R4+R5}$

Combining those using rough principles of the op-amp results in:

$V_{in} = V_o\frac{R5}{R4+R5}(1 + \frac{R1}{R2}) - V_{GS}\frac{R1}{R2}$

Now equalling all components (i.e. $R1 = R2$ and $R4 = R5$), this equation simplifies to:

$V_{in} = V_o\frac{1}{2}(1 + \frac{1}{1}) - V_{GS}\frac{1}{1} = V_o - V_{GS}$

Using $V_o = V_{R3} + V_{GS}$ the required expression $V_{in} = V_{R3}$ is obtained.

Up Shifting

The control system has to optimize the output power of the system. To calculate this, both the current and voltage at the load have to be known. Since the current is set by the control system itself this is covered, the voltage on the other hand is not. The voltage output voltage is of course the voltage difference between both drains of the switches. But for the MCU ADC the signal has to be mirrored and scaled and the easiest solution for this is an inverting op-amp. On power up, the op-amp clamps its inverting input to the negative supply rail. When the voltage across the load rises, a current will flow trough the feedback loop caused by the rising op-amp output. Caution has to be taken for the case when the current of the solar array is near its maximum, since its output voltage will be near zero in that case. To be able to still measure the voltage, the op-amp has to operate close to its negative supply rail.

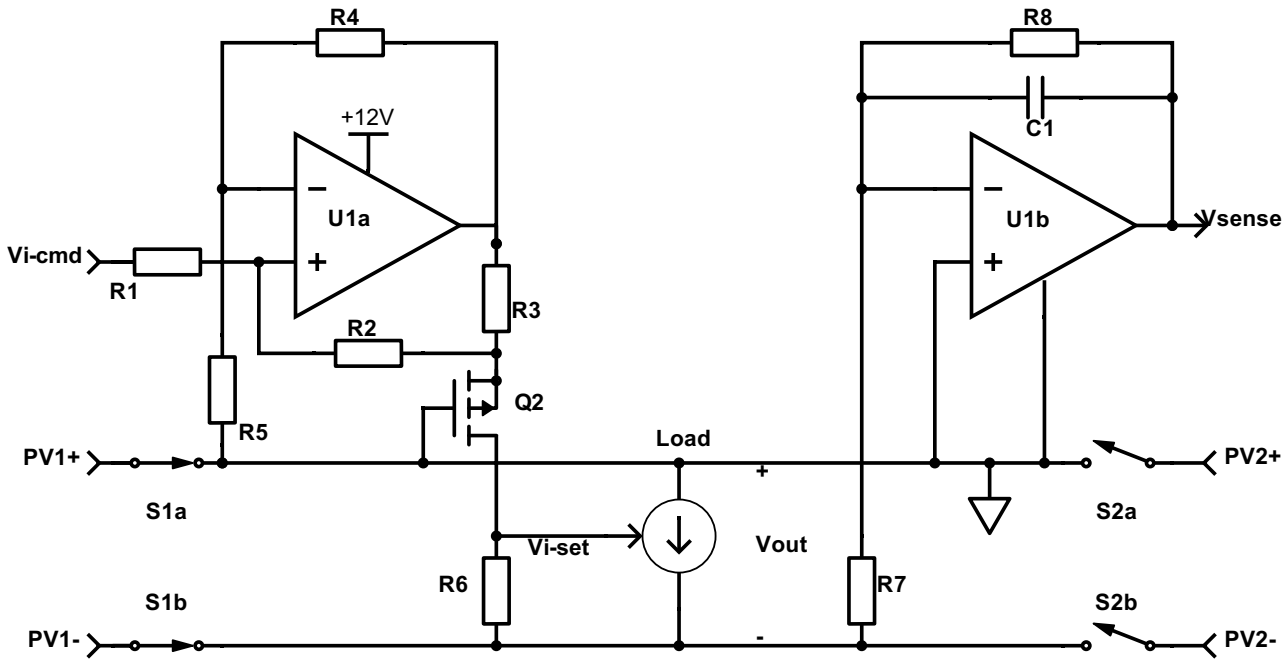


Figure 6.5: Schematic for level shifting the analog signals

7 | Implementation

7.1 Charge Redistribution

The first optimization is the switching MOSFET gate charge at the drive voltage, $Q_{g,on}$. Every extra MOSFET increases the current the driver needs to sink or source in order to archieve proper rise and fall times. The peak driver current and driving power required scales with $Q_{g,on}$ ($I_{peak} = Q_{g,on} \cdot (N_{PV} + 1) \cdot F_{sw} \cdot V_{GS}$). Since solar modules can contain as many as 96 PV cells it is important to minimize $Q_{g,on}$ in order to reduce the design constraints and power consumption of the gate driver. The second important optimization would be the MOSFET $R_{DS,on}$. A lower $R_{DS,on}$ would result result in lower switching losses, but the impact difference on the design makes it a lower priority than $Q_{g,on}$.

Switching FET

The first task was then to find a suitable MOSFET that also had a SPICE model available. As often the case when selecting components the outcome is mostly dependent on the technologies available. Every part has physical limitations, and parametric searching gives an indication of the best achievable selection. After parametric searching, IPD30N03S4L-14 [15] was found. Device parameters are ordered by their importance of optimization for the design, with Q_g by far the most important:

- $Q_g < 14\,\text{nC} \mid V_{GS} = 10\,\text{V}$
- $R_{DS,on} < 13.6\,\text{m}\Omega \mid V_{GS} = 10\,\text{V}$
- 10 k units price: 0.17 $/piece
- TO-252 Package
- $I_{D,max} = 30\,\text{A}$
- $V_{th} < 2.2\,\text{V}$, $V_{th} > 1\,\text{V}$
- $V_{(BR)DSS} = 30\,\text{V}$

Clamping FET

The requirements for the clamping MOSFET are easier. The bulk of the switching energy is sourced and sunk by the driver, and the clamping MOSFET only needs to set the DC level so a relatively high $R_{DS,on}$ is not a problem.

This means that the other parameters can be optimized to have the smallest impact on the circuit. With the criterion that a SPICE model needs to be available, the choice was made for BSS138 [4]. Device parameters are ordered by their importance of optimization for the design with Q_g and price being the most important:

- $Q_g < 2.4\,\text{nC} \mid V_{GS} = 10\,\text{V}$
- 10 k units price: 0.027 $/piece
- $R_{DS,on} < 3.5\,\Omega \mid V_{GS} = 10\,\text{V}$
- SOT-23 Package
- $I_{D,max} = 220\,\text{mA}$
- $V_{th} < 1.5\,\text{V}$, $V_{th} > 0.8\,\text{V}$
- $V_{(BR)DSS} = 50\,\text{V}$

Passive components

Detailed simulations are done using the models of the previously chosen active devices. These simulations are quite complex, since all parasitic effects (such as inductor/capacitor ESR and stray inductances, especially at the gate current path) are modeled. $C_{(n)}$ of Figure 6.2 was simulated first. It will not affect the rise and fall times if its value is too large, but it operates in series with the gate, meaning that the voltage will be shared across them inversely proportional to their values. The simulation results with various values can be see in Figure 7.1 and Figure 7.2. It can be seen that while the parameters are logarithmically spaced, they increase linearly. There could be a factor of diminishing returns, as with larger capacitors a higher ESL can be expected.

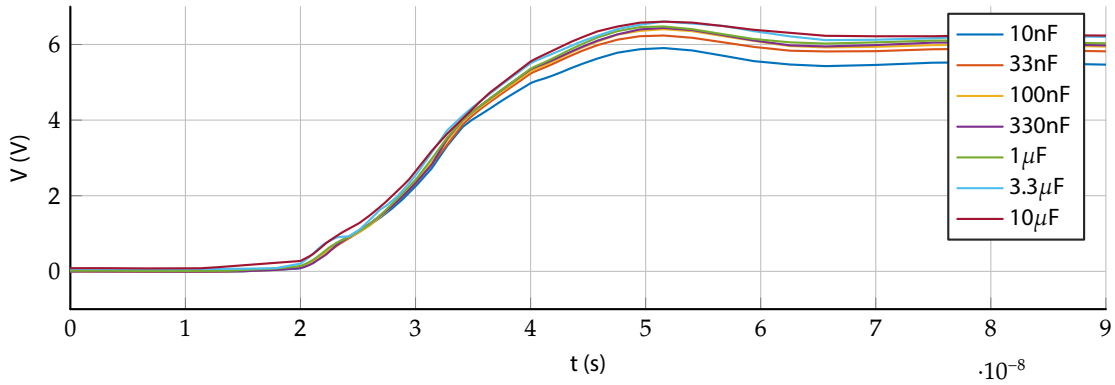


Figure 7.1: $V_{GS,a}$ rise times with the value of $C_{(n)}$ as parameter.

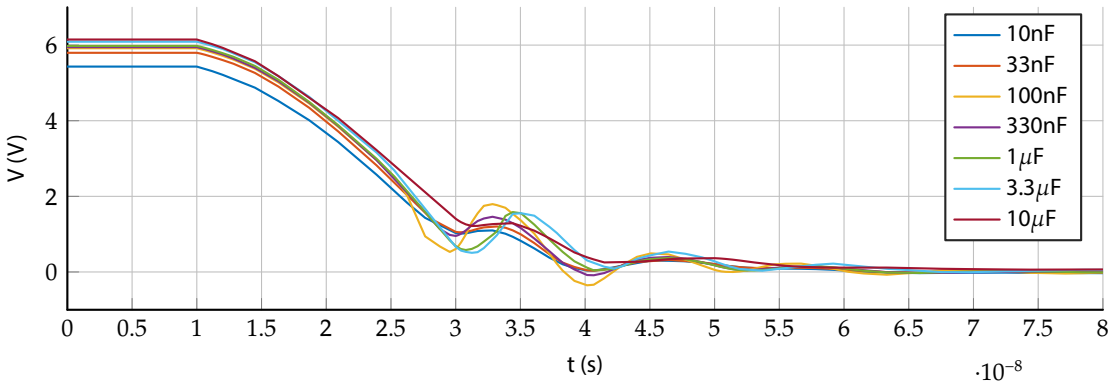


Figure 7.2: $V_{GS,a}$ fall times with the value of $C_{(n)}$ as parameter.

The minimal value appears to be larger than 33 nF and extra capacitance does not negatively influence the operation of the circuit. MLCC capacitors usually have wide tolerances and lose capacitance due to aging. They also exhibit capacitance loss due to DC bias effects. For example at 28 % of rated voltage, the capacitance is down almost 25 % for the X5R [19]. Taking a possible 90 % capacitance reduction into account, a initial value of 470 nF was chosen.

For gate resistors $R_{(n)a}$ and $R_{(n)b}$ the initial value was taken from the datasheet, 3.5 Ω and 6 Ω respectively [15, 4]. Figures 7.3 and 7.4 show the parametric analysis of the power MOSFET gate stopper resistor.

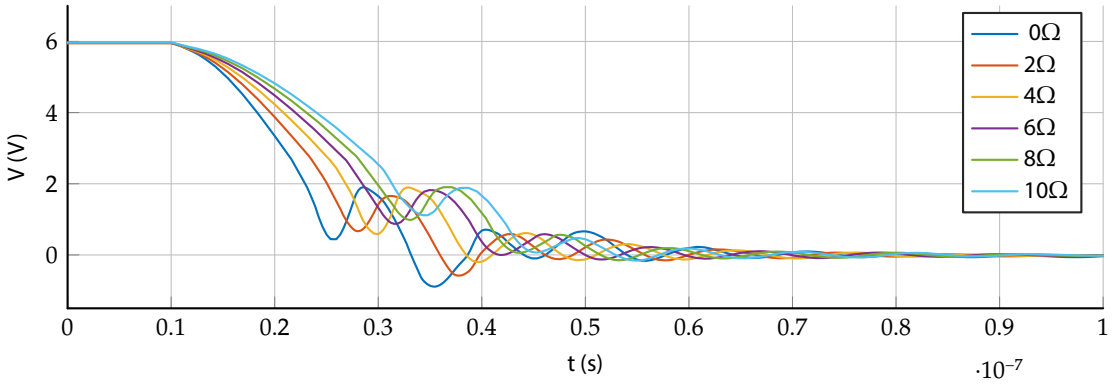


Figure 7.3: $V_{GS,a}$ rise times with the value of $R_{(n)a}$ as parameter.

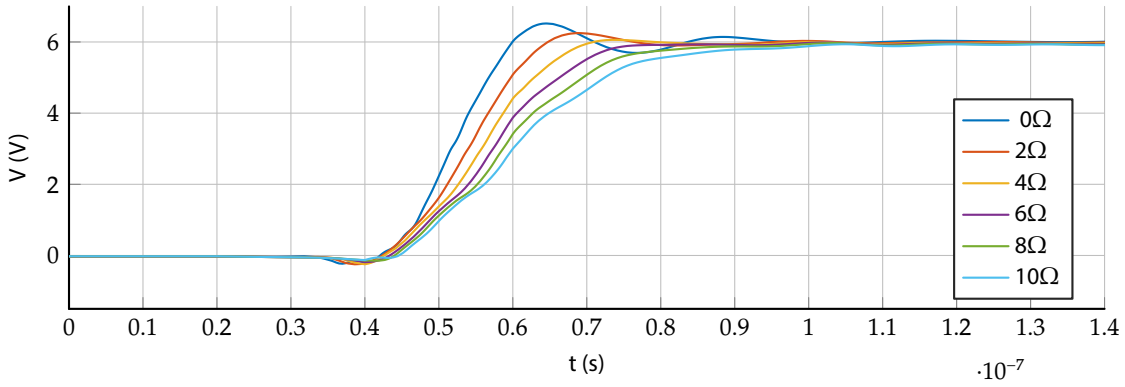


Figure 7.4: $V_{GS,a}$ fall times with the value of $R_{(n)a}$ as parameter.

It can be seen clearly that 0 Ω and 2 Ω show oscillating response in figures 7.3 and 7.4.

While it is not a very large oscillation, this can worsen when longer wires are needed with more MOSFETs due to a larger wire inductance. 4 Ω seems to be the value that dampens the oscillations best while maintaining the fastest rise rime, i.e. dampens critically. Larger values only cause longer rise times while not significantly reducing oscillations. The value is close to the datasheet value, which means that the $C_{(n)}$ simulation was done with a value close to the optimal solution. From this we might conclude that the chosen value for $C_{(n)}$ is very likely to be sound.

All curves show a slight nonlineairity at the middle. This is because of the miller plateau and only an indication that the model includes this effect.

The value of resistors $R_{(n)b}$ is less critical. The rise time is of no concern as clamping MOSFETs only needs to bias the switching MOSFETs. It is not a problem if the clamping MOSFETs open up when the switching MOSFET they clamp closes, as this relieves the driver of some of the current it has to sink. But the fall time of $V_{GS,b}$ is important because it should not interfere with driving the switching MOSFETs on, as it can form a short between the gate and source if it is not turned off on time. Figure 7.7 shows that with large values the turn-off delay of the clamping MOSFET is too large. When the driver attempts to drive the switching MOSFET on, the clamping MOSFET shunts away the delivered power. All this energy is lost without benefits and the driver is unnecessarily loaded. Figures 7.5 and 7.5 show the rise and fall times of $V_{GS,b}$ at different values of $R_{(n)b}$. It can be seen that the rise time correlates with the current sunk by the clamping MOSFETs. At small values of $R_{(n)a}$ the current converges and remains relatively stable while the oscillation at the gate increases. Accounting for tolerance, a value of 6.8 Ω is chosen.

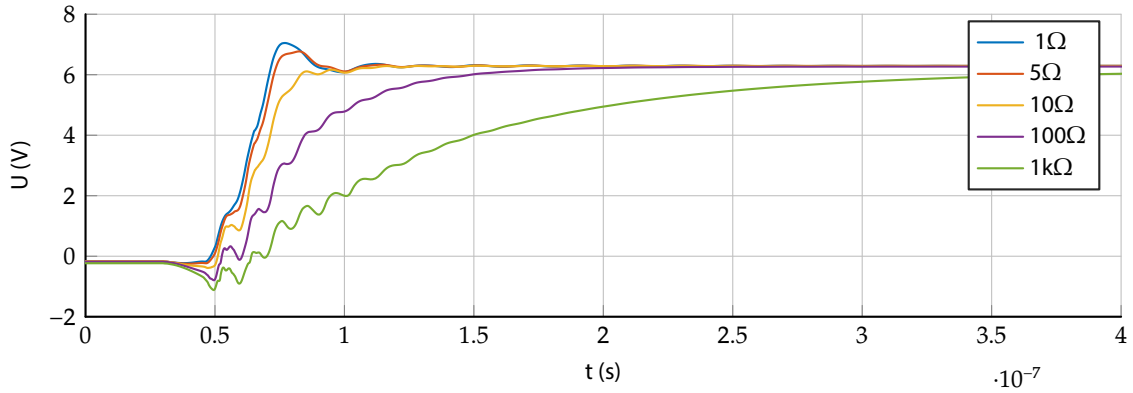


Figure 7.5: $V_{GS,b}$ rise times with the value of $R_{(n)b}$ as parameter.

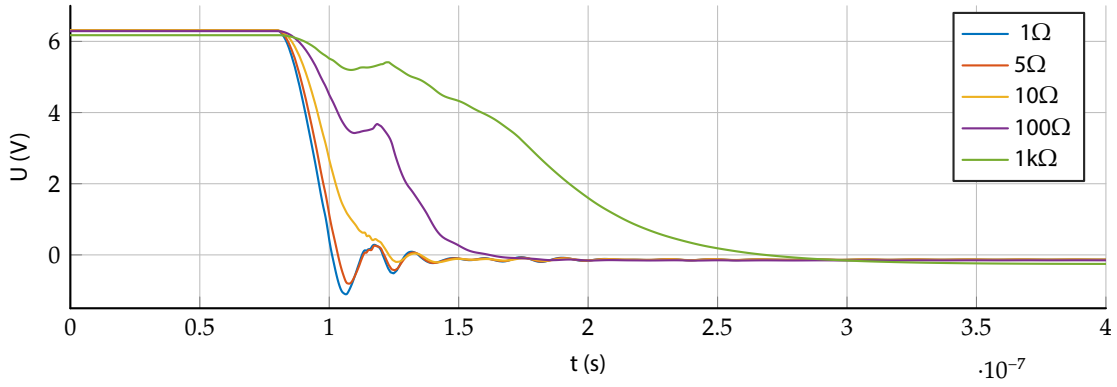


Figure 7.6: $V_{GS,b}$ fall times with the value of $R_{(n)b}$ as parameter.

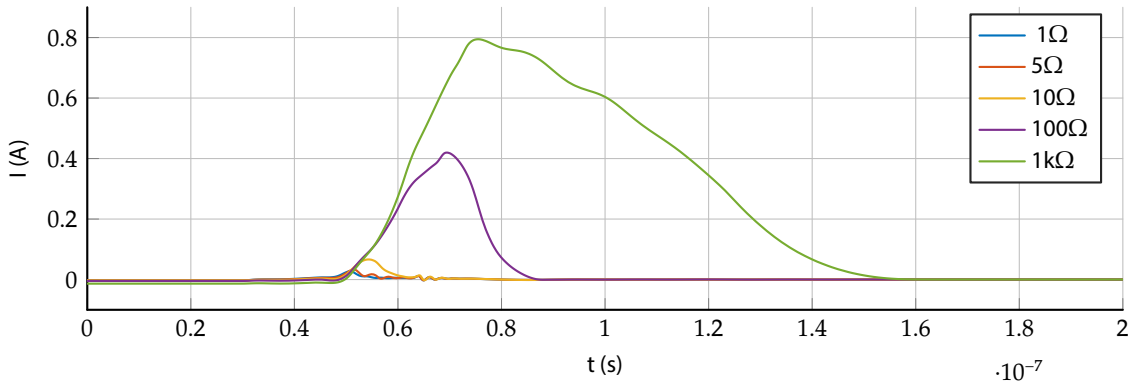


Figure 7.7: $I_{D,Q_{(N)b}}$ with the value of $R_{(n)b}$ as parameter.

It seems that most of the values that were chosen initially were very close to the found optimal value. After re-iterating this design procedure with the small changes it became clear that these values remained close to optimal and the following values were found:

- $R_a = 3.3\,\Omega$
- $R_b = 6.8\,\Omega$
- $C = 470\,\text{nA}$
- $Q_a =$ IPD30N03S4L-14 [15]
- $Q_b =$ BSS138 [4]

With these values, the question is if the peak driver current is still reasonable. Simulations proved that this was the case, as it remained well under 1 A for seven solar cells. The largest driver available on the market (price under 2 $/piece) with sufficient rise and fall times can source and sink 40 A, meaning that one such driver could theoretically drive 280 PV cells. The validity of this assumption can be questioned as the space needed to accommodate the required MOSFETs would probably cause wire inductances to become too large. But as an indicative amount it seems fair to say that the current values allow for expansion in the future.

Integrated Circuits

The self-oscillating half bridge driver could only marginally drive the required currents, and with the tolerances on the devices more headroom was required. The driver chip chosen for the design was UCC27511 [26], again using parametric searching. While a wealth of drivers is available, only a few have the required specifications:

- SPICE model available
- Source and sink current capability of 4 A and 8 A respectively
- Fast rise time, < 10 ns
- Schmitt trigger input to reject level translation noise
- Small SOT-23-6 package
- Relatively low price, 1 k units price of 0.49 $/piece

For the oscillator there was only one option. There was no other chip that had the closest combination of all factors. The minimum frequency specification, required to allow more energy to be transferred between cells, ruled out almost all of the self-oscillating half bridge bootstrapping drivers available. It was shown with simulation that, as frequency increased, the balancing action improved, but also logically the insertion losses would increase. Therefore it was beneficial to have a half-bridge driver with trimmable frequency to investigate this tradeoff. The maximum frequency of the chosen chip, AUIR2085 [2] is 500 kHz which should be sufficient and is trimmable by an RC stage. Another benefit of the chip is that it has an internal dead time mechanism, reducing the power loss due to MOSFET on-time overlap. This does not decrease balancing performance as the RC-time of the switching capacitor system is much smaller than $1/f_{switch}$ and the amount of rising edges remains the same.

7.2 Current Sharing Switching

Switching

The current sharing stages have a few switching components and a filter to implement. The first devices to be analyzed will be the power MOSFETs. All of the load current must pass through two MOSFETs in series, no matter what string it comes from. Therefore $R_{DS,on}$ losses are inevitable and should be minimized. A smaller $R_{DS,on}$ comes with a higher Q_g as this is limited by the state of technology. However, at the low frequencies that the current sharing section will operate at, the switching losses can be calculated and even with relatively large gate charge (100–200 nC) they still stay far beyond the losses due to $R_{DS,on}$.

The solar cells used to demonstrate have a short-circuit current slightly over 6 A, meaning that the load current will likely be around 12 A. The conduction losses from MOSFETs with an $R_{DS,on} < 1$ mΩ are per MOSFET three times as large as the total driving losses of all four MOSFETs. This makes the optimization a simple one: Pick the MOSFET with the lowest $R_{DS,on}$. Price is less important, as only four of these MOSFETs are needed for each solar panel.

- $R_{DS,on} < 1\,\text{m}\Omega \mid V_g = 10\,\text{V}$
- $Q_g < 1120\,\text{nC} \mid V_g = 10\,\text{V}$
- $I_{D,max} = 120\,\text{A}$
- 10 k units price: 1.13 $/piece
- TO-252 Package
- $V_{th} < 2.2\,\text{V}$, $V_{th} > 1.3\,\text{V}$
- $V_{(BR)DSS} = 30\,\text{V}$

For cells that have a higher I_{sc}, it is advise to use two cheaper MOSFETs in parallel as the combined features would be more attractive, both on price and performance.

It must be noted that it is adviseable to implement dead-time between each MOSFET half, to aoid short-circuits. For example the lower and upper PV cells are shorted when both current sharing sections are open at the same time.

For its gate resistor the datasheet value was taken, 5 Ω. A realistic value of 5.6 Ω was chosen. Simulations proved that this value was indeed optimal. Analysis of this problem is straight forward and closely related to Section 7.1.

Because of convenience, the same low side driver chip as for the balancing section was chosen. Bulk savings are larger, and less tool switching during production including ease of design make this a reasonable choice. For the upper two drivers, U3 in Figure 6.4, a dual driver in one package was chosen. It comes from the same family as the previously chosen driver, and its specifications are closely related making it again a reasonable choice. It is also twice as expensive, so it could be argued that again the same single driver IC can be used or even the other way around. This realization also came after the design and ordering of the PCB, but the difference is negligible for the large amount of effort needed to change this.

Level Translation

For the level translation circuit only two parts need to be optimized: the common gate P-MOSFET Q3 and both of the resistors, R1 and R3 in Figure 6.4. The resistors have the same value.

The common gate MOSFETs have the same criteria as the clamping MOSFETs, only of different polarity. Small parasitic capacitances, footprint size and cost should be kept to a minimum. Parametric searching returned BSS84 as a good candidate:

- $Q_g < 1.3\,\text{nC} \mid V_g = 10\,\text{V}$
- 10 k units price: 0.026 $/piece
- $R_{DS,on} < 10\,\Omega \mid V_g = 10\,\text{V}$
- SOT-23 Package
- $I_{D,max} = -130\,\text{mA}$
- $V_{th} < -0.8\,\text{V}$, $V_{th} > -2\,\text{V}$
- $V_{(BR)DSS} = -50\,\text{V}$

Subsequently a simulation was done with the models supplied by the manufacturer. Only two components are left to optimize, which are $R1$ and $R3$ in Figure 6.4. Intuitively one would choose the value as large as possible, because this reduces the power consumption of the ciruit. But the parasitic capacitances could add unwanted lowpass filters, adding delays and slow rising edges, favoring a lower resistance. The simulation results of Figures 7.8 and 7.9 prove otherwise, as the difference is marginal over a very wide range of resistance. A value of 100 kΩ was chosen, to anticipate some trace capacitance that could occur.

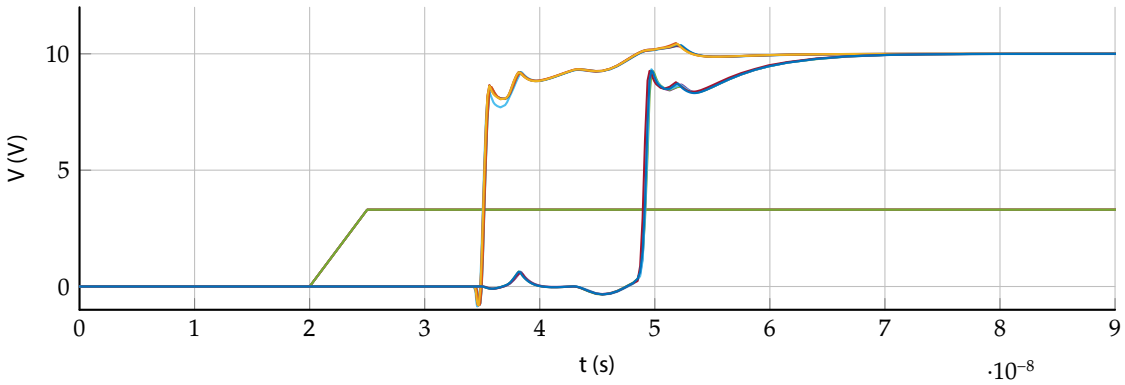


Figure 7.8: Level shifted signal on rising edge at the gates of the MOSFETs. Most left is the input signal, then $V_{GS,Q1}$ and last $V_{GS,Q2}$ both with the value of R_1 (= R_3) as parameter. (10Ω, 100Ω, 1kΩ, 10kΩ, 100kΩ)

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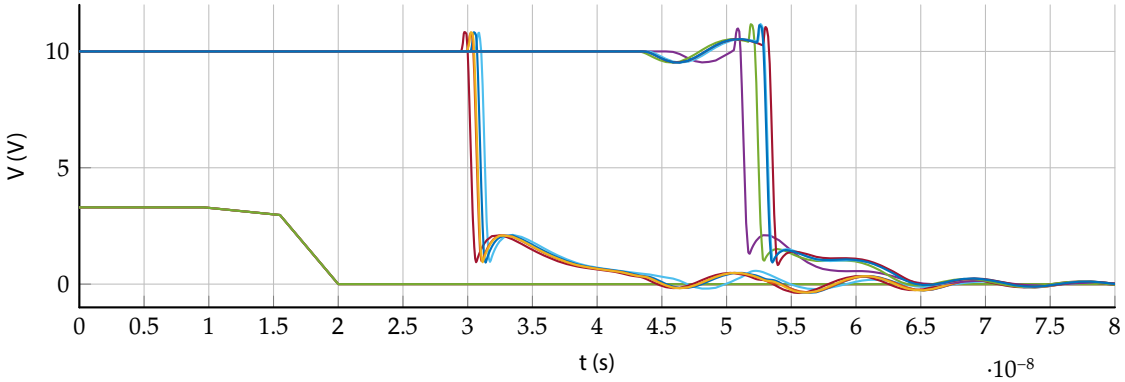

Figure 7.9: Level shifted signal on falling edge at the gates of the MOSFETs. Most left is the input signal, then $V_{GS,Q1}$ and last $V_{GS,Q2}$ both with the value of R_1 (= R_3) as parameter. (10Ω, 100Ω, 1kΩ, 10kΩ, 100kΩ)

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LC Filter

The LC section is only to keep the submodules of the design separated. If it was removed the solar cell would operate with a square wave current, of which both the low and high sections of the wave would be far off the maximum power point. One solution would be to increase the frequency enough so that the internal diffusion capacitance takes the bulk of the ripple, but simulated results showed that this requires very high frequencies (>800 kHz) and would very likely interfere with the also high frequency of the balancing system. The easiest solution would be the implemented filter. It would need to supply a high impedance to high frequencies at the input, and a low output impedance to frequencies up to and including the current sharing stage switching frequency. The LC filter could therefore have a cutoff frequency between or beneath these two frequencies, with the higher being the balancing frequency and the lower being the current sharing switching frequency between 10–50 kHz. Higher current sharing switching frequency causes lower output ripple on the capacitor, but more driving losses on the switching elements.

Simulations showed us that values of 300 µF and 1.1 µH gave sufficient damping of the lowest fundamental frequency of the current sharing module without getting overly cumbersome components. The cutoff frequency, $f_c = \frac{1}{2 \cdot \pi \sqrt{1.1\ \mu H \cdot 300\ \mu F}} = 8.8$ kHz is below both frequencies. That makes sense as it would lead to a larger inductance (more constant input current behavior) and a larger capacitor (less voltage drop during drain cycle). The values chosen could be judged sufficient but there would still be some current and mostly voltage ripple left.

Larger parts would however cost more space and money, but perform better filtering action. Especially a larger inductance would be difficult as larger inductors generally have larger ESR, are costly and are bulky to achieve a high saturation current. The choice of the parts is therefore mainly dependent on the opinion of the designer and could be optimized with a lot of research and simulating and clear design goals. This is left for further work.

7.3 Current Sharing Analog Level Shifter

Down Shifting

In the Design section of the Current Sharing Analog Level Shifter, the difference amplifier circuit is proposed. The required gain is achieved by setting $R1 = R2$ and $R4 = R5$. This results in 3 different values that have to be chosen. The voltage across $R3$ determines the size of the current signal that is shifted down trough the current buffer. However, the current in the non inverting feedback loop will also enter the drain of the common gate amplifier. So the current in the feedback loop has to be small enough to not cause major distortion. $R1$ and $R2$ have to be larger than $R3$ by a a couple of orders of magnitude.

I_S is the down shifted current proportional to I_D, this current induces a voltage across $R6$ to control the load input. The combination of $R3$ and $R6$ can therefore determine the gain of the common gate amplifier. The input voltage V_{i-cmd} (and thus V_{R3}, see Section 6.3) is set by the MCU and has a range of 0–3.3 V. This has to be mapped to a voltage specific to the used load. The load build according to Appendix B has an input range of 0–60 mV. The ratio between the resistors must be equal to $\frac{0.060}{3.3}$.

To save costs, a dual op-amp can be used for both the up and down shift circuit. As said before, the input and output range of the op-amp must include the negative supply rail. With this criteria the LM2904 [12] op-amp can be found as a cheap solution. Of course all the other requirements for the circuit have to compared with the specifications. All specification look fine, but the Input bias current, I_{IB}, has to be noted. At room temperature the typical $I_{IB} = -20$ nA up to a maximum of $I_{IB} = -250$ nA. While picking the exact values of the feedback resistors, it has to be noted that this will cause a bias in the feedback current.

For the common gate amplifier the same MOSFET, BSS84, is picked as in Section 7.2. The same optimization parameters apply as before, so it would be logical to use the same part.

With all this in mind, all the resistors can be determined. $R3$ and $R6$ have to be relatively small, according to their gain desired gain ratio a value of 3.3 kΩ and 60 Ω will suffice. The current $I_{R3} = 1$ mA maximum, which is well within the MOSFET range. Now $R1$ and $R2$ have to be chosen in such a manner that their current does not effect I_{R3} but is also not distorted by I_{IB}. Setting $I_{R1} = I_{R3}/100$ as a rough goal will cause no distortion on the current buffer input. The distortion caused by I_{IB} still lies a couple of order of magnitudes lower, which therefore will be neglectable. Thus a value for both $R1$ and $R2$ of 180 kΩ will be used. $R4$ and $R5$ can be chosen as desired, some where around 50 kΩ is fine.

Up Shifting

The proposed design for this part is to use an inverting op-amp. For this the same LM2904 dual op-amp can be used, with its main feature being that the output range includes the negative supply rail. For now the gain can be set to unity, since the stack voltage will not exceed the ADC input limit of 3.3 V. However, for a full array or module version, the gain can be set lower. To filter the noise of the measured signal a first order RC filter is

added in the feedback loop. The f_c of this filter has to be lower than the lowest system operating frequency (the current sharing frequency of 1 kHz). The lower limit is determined by the maximum frequency of the MCU control loop. The chosen resistor values are both 220 kΩ.

7.4 PCB design

To test the implementation in real life, a PCB needs to be manufactured. There are a few considerations to be made when designing a PCB. Most of the important considerations are well-known, but crucial to keep in mind during design [9]. A reduced size reduces both PCB cost and shipment, therefore most of the components will be of the SMD type. Another benefit of using SMD is that components can be placed closer together which reduces parasitic inductances and is beneficial to fast switching. But it should be kept in mind that some traces need to remain wide to accommodate for larger currents, and certain traces benefit from low inter-trace capacitances. The first only puts a restrain on the minimum PCB size while the latter implies that a ground plane should be kept away from these signals. Optimization on routing should be done with the following priorities:

- Trace length between driver and gate should be kept to a minimum to reduce parasitic inductance of the transmission line. Larger inductances lead to stronger oscillations, which need to be dampened more by larger gate resistors, which in turn reduce the maximum gate voltage rise time.
- Decoupling capacitors should be placed as close and with the smallest possible trace resistance to the drivers and lesser extent other ICs. This decreases the influence of the power supply on switching performance of the circuit because larger currents can be sourced faster.
- There should be no ground plane close to the gate current paths. This reduces the capacitive load of the transmission line between the gate and the driver, increasing the current that needs to be sourced and sunk.
- Sensitive signals should be kept away from switched power signals to reduce coupling.
- Trace width for power carrying signals should be made as wide as reasonably possible to reduce copper losses.
- Mounting holes should be placed so that the PCB can be mounted on standoffs, to avoid making contact with stray pieces of metal or other conductors during testing.

For the PV cell connector two options were made available; a board-edge connector with pads wide enough to solder but also with holes so that a 5.08 mm pitch connector can be used. The resulting PCB can be seen in Figures 7.10 and 7.11.

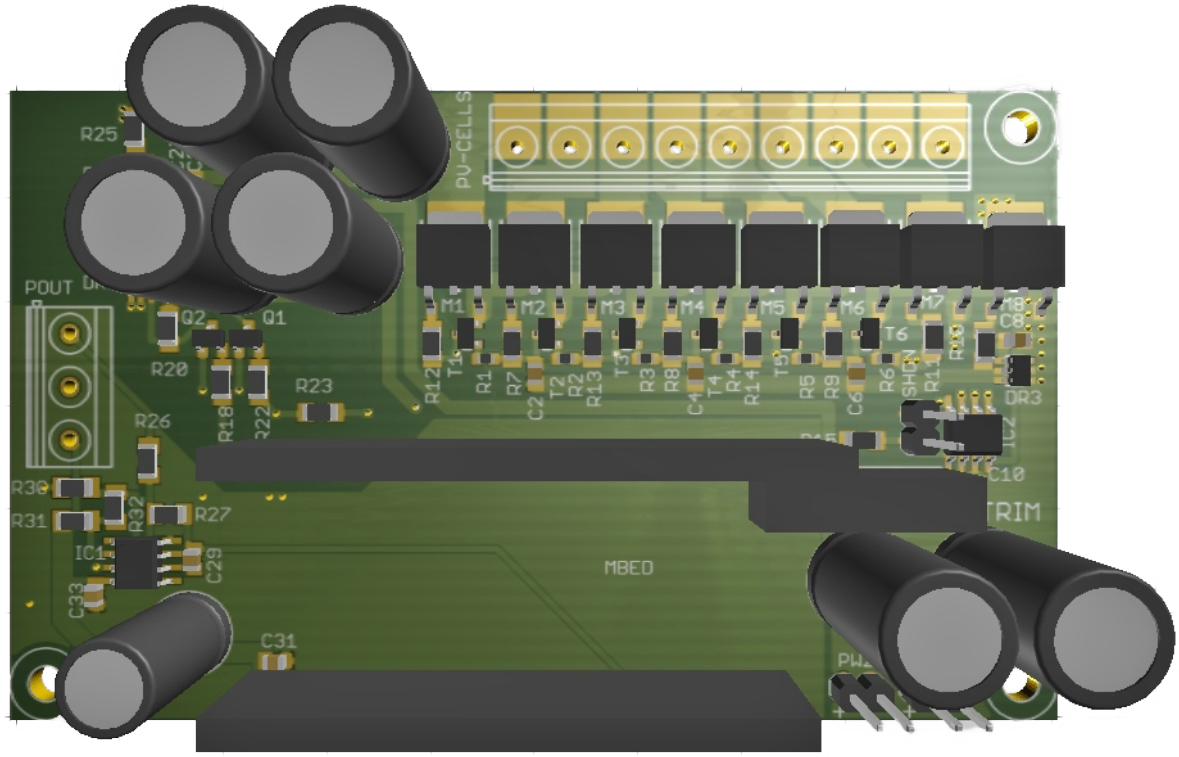

Figure 7.10: The PCB top side.

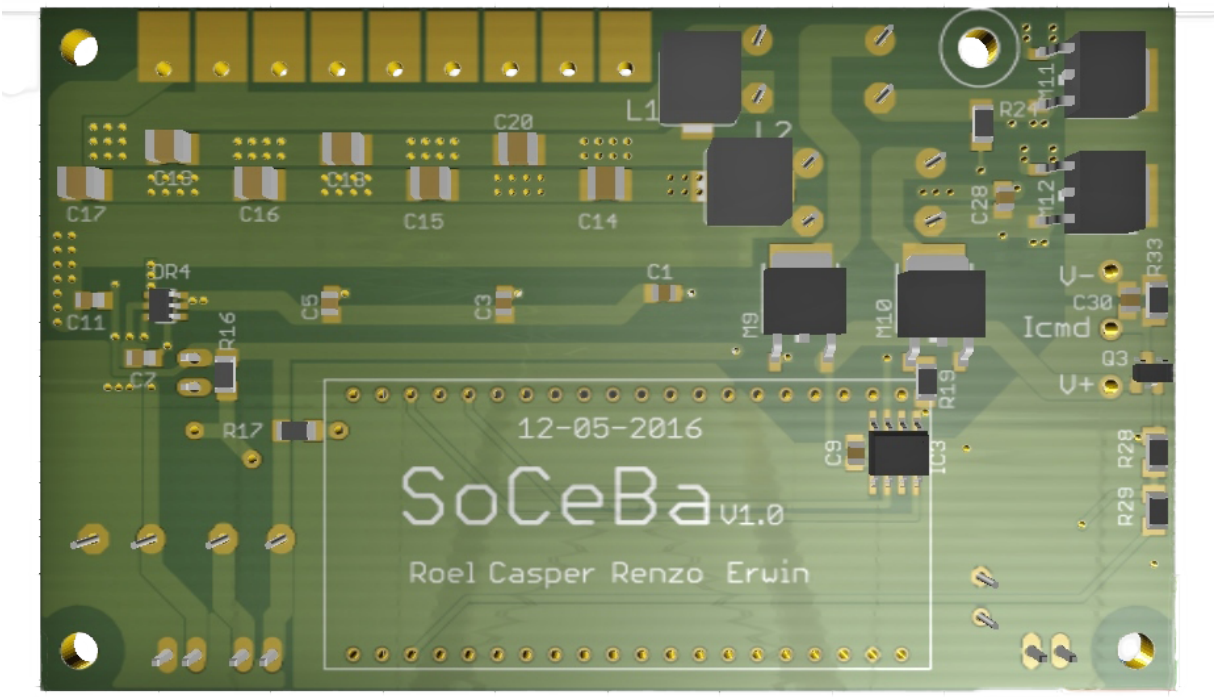

Figure 7.11: The PCB bottom side.

8 | Test Plan

8.1 Testing Setup

In Table 8.1 all the used equipment in listed and in Figure 8.1 the test panel is shown with the cell numbers next to each cell.

Table 8.1: Testing equipment

Function	Device	Specifications
MPPT load	Chroma 63600-2 (2 * 63630-80-60)	Integrated MPPT, $V < 80$ V, $P_M = 60$ W, $I_M = 0 - -6$ A(±0.1 mA)
Electronic DC load	Elektro-Automatik EL 3400-25A	400 V, 25 A, analog interface 0–10 V
Oscilloscope	Tektronix TDS2022C	250 MHz, dual-channel
Oscilloscope	Fluke ScopeMeter 190	500 MHz, quad-channel
Artificial Light source	Eternal Sun	800–1000 W m^{-2}, halogen and gas-discharge lamps
Power supplies	Multiple different lab power supplies	

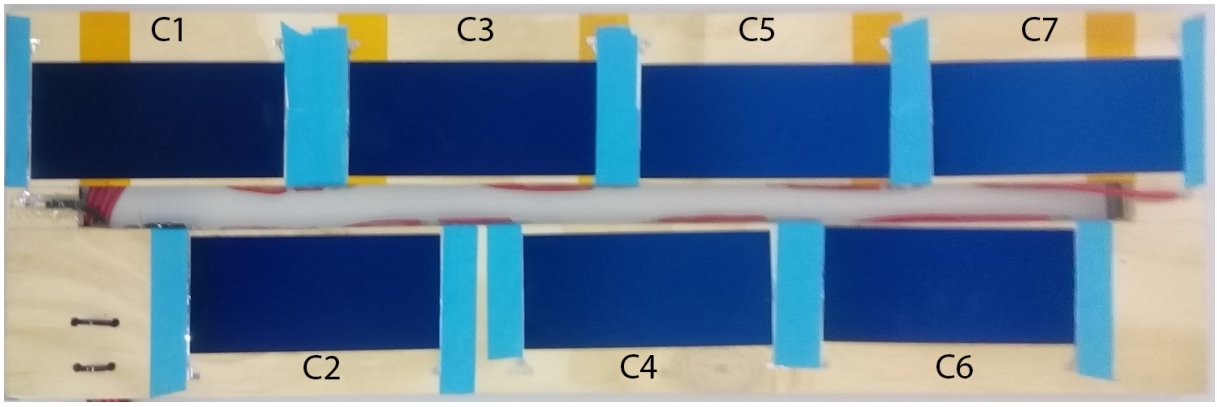

Figure 8.1: The cell layout on the test setup

8.2 Charge Redistribution

8.2.1 Features to be Tested

As the circuit is a discrete system designed to perform one function, the features to be tested are rather straightforward. The signals should propagate through the system as intended without too much pulse width and shape distortion.

8.2.2 Approach

To simulate the environment without increasing complexity the PV strings will be replaced by forward-biased diode strings, simulating the voltages present on the stack. Loading will be provided by an electronic load as described in 8.1. This setup does not simulate switching with actual PV cells, and this feature will be tested in Section 8.5. Because the diodes only simulate voltage levels the loading and filters will be left out. To provide a driver return path the bypass capacitors need to be mounted during the test.

Figure 8.2 shows the signal points that will be monitored with an oscilloscope during the test to follow propagation of the gate drive signals.

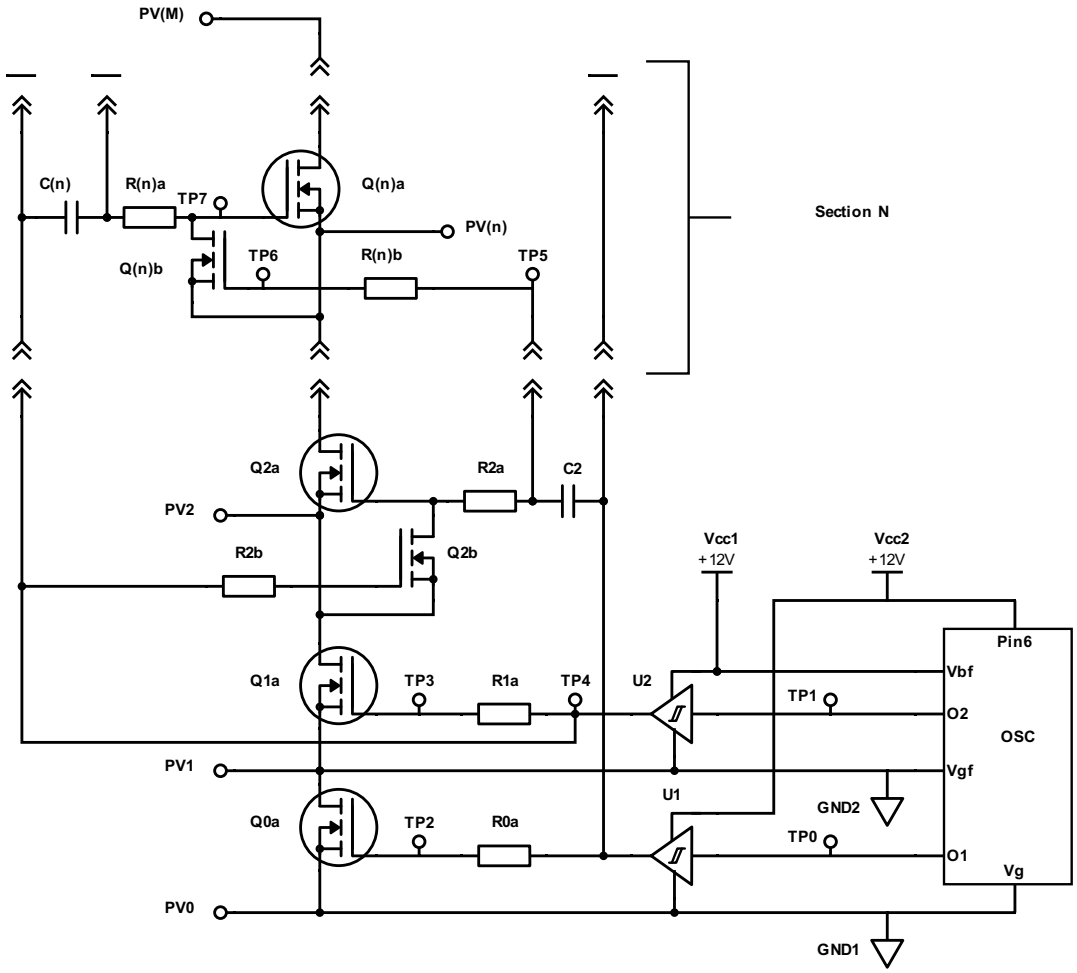

Figure 8.2: dDCR schematic with test points.

8.2.3 Criteria

The requirements of the subsystem are as follows:

- The gate drive signals needs to be levelshifted.
- The gate drive signals should not give excessive DC offset with respect to the gate and source. They are associated with, i.e. the gate clamping should work.
- Gate clamping may not interfere with gate driving.
- The level shifting propagation delay difference between MOSFETs should be in the same order of magnitude as the rise time of the gate driver.
- There should be no oscillating response that may cause the MOSFETs to switch at frequencies higher than the switching frequency.
- The gate drivers should drive sufficiently fast rise time with respect to the dead time and frequency without oscillating response on the gate.

8.3 Current Sharing Switching

8.3.1 Features to be Tested

As with Section 8.2 the circuit is a discrete system designed to perform one function, the features to be tested are rather straightforward. The signals should propagate through the system as intended without too much pulse width and shape distortion.

8.3.2 Approach

To simulate the environment without increasing complexity the PV strings and balancing systems will be replaced by two independent power supplies. The filters will be left in place to remove any artifacts caused by the power supply and maintain a realistic filter output response with respect to loading. The load would have been the op-amp-transistor current sink of Appendix B, so that the load will not force the current when the MOSFETs are closed.

Figure 8.3 shows the signal points that will be monitored with an oscilloscope during the test to follow propagation of the gate drive signals.

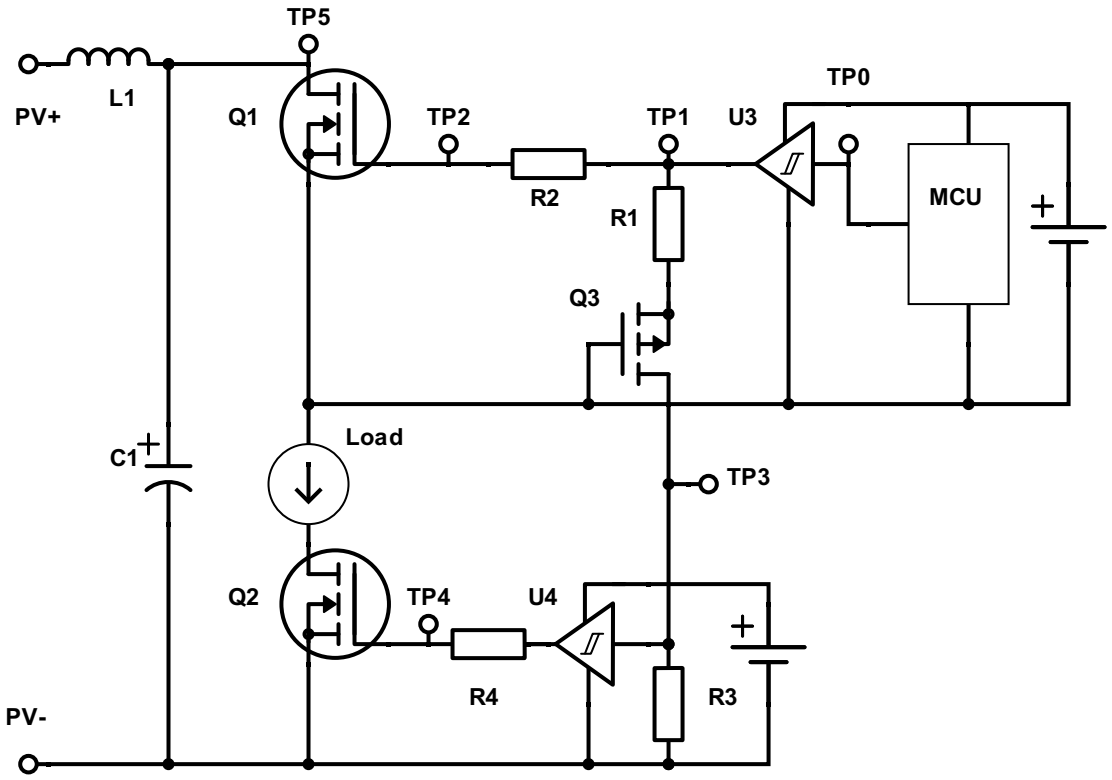

Figure 8.3: Half bridge schematic with test points.

8.3.3 Criteria

The requirements of the subsystem are as follows:

- The gate signal needs to be level-shifted.
- The level shifting propagation delay should be in the same order of magnitude as the rise time of the gate driver.
- The level shifting propagation delay difference between MOSFETs should be in the same order of magnitude as the rise time of the gate driver.
- There should be no oscillating response that may cause the gate driver to drive the MOSFETs at frequencies higher than the switching frequency.
- The gate level translators should operate down to zero voltage difference between signal levels without loss of performance.
- The gate drivers should drive sufficiently fast rise time with respect to the dead time and frequency without oscillating response on the gate.

8.4 Current Sharing Analog Level Shifter

8.4.1 Features to be Tested

The circuitry responsible for shifting the analog signals to the correct levels can be seen in Figure 6.5. It can be split up into two parts which can be tested separately: down shifting the command signal for the load and up-shifting the measured voltage across the load. Again it performs a single function and assessment will be done how well it performs.

8.4.2 Approach

To test if the levels are correctly shifted, a test setup can be created by simulating the shifting load by adding an external power supply. When a control signal is applied to V_{i-cmd}, the down shifted signal should be visible across $R6$. To measure the distortion the voltage of the external power supply can be sweeped.

With a similar but opposite test setup the up shifting of the voltage measurement can be tested. The applied voltage by the external power supply can be retreived at the output if all works well. Sweeping the voltage range from 0 V to V_{oc} (where V_{oc} is the maximal output voltage of the PV module) should output a signal 0 V to V_{AREF} (where $V_{AREF} = 3.3$ V, the maximal reference voltage of the microcontroller ADC).

8.4.3 Criteria

- The voltage signals needs to be levelshifted.

- The level shifterst should perform filtering to keep switching noise away from the microcontroller and load.
- The level shifting should remain lineair within the required bounds.
- The level shifting should not exhibit significant offsets.

8.5 Balanced Solar Module

8.5.1 Features to be Tested

- Power output
  - The ability of the MCU algorithm to climb the power space.
  - The power output should be almost proportional to the shaded area.

8.5.2 Approach

- Power output
  Connect SoCeBa to the solar module and log the output power with Section 7.3.3. Perform a series of shading tests and see if SoCeBa stays working at its maximum power point.

8.5.3 Criteria

- Power output
  - Is the algorithm on the MCU able to climb the power space?
    The algorithm should be able to find the maximum power point within a threshold of 5 % *(Table 3.2 number 2.4).*
  - The power output should be almost proportional to the shaded area.
    The maximum power point power value should be proportional to the area shaded with a maximum deviation of 10 % *(Table 3.2 number 2.4).*

9 | Testing & Results

9.1 Charge Redistribution

The test results were very encouraging. The oscillator provided excellent square waves at TP0 and TP1, referenced to GND1 and GND2 respectively and can be seen in Figure 9.1. The oscillator was excellently trimmable and proved usable far beyond the frequency range specified in the datasheet without pulse distortion.

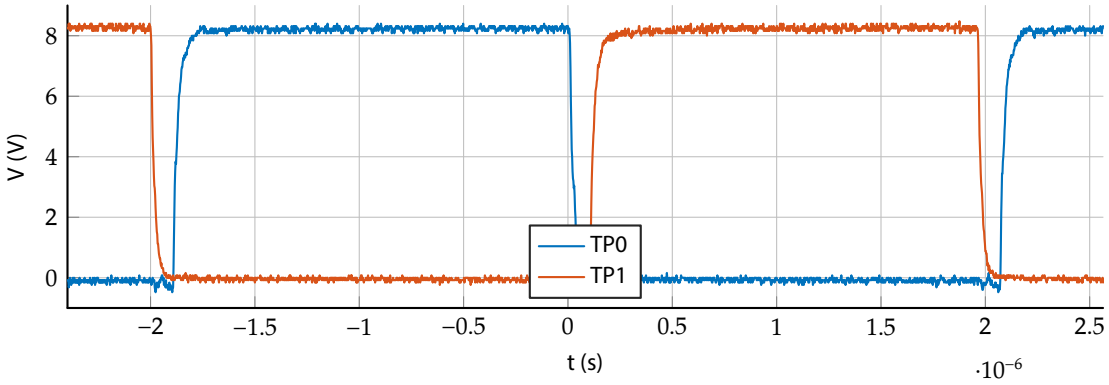

Figure 9.1: Low side balancing oscillator output.

These signals also propagated well through the gate drivers, and resulted in no abnormal rise times at the gates of Q0a and Q1a and only very small ringing, verifying the component choice. These signals were equal to the gate levels at the highest MOSFET on the string.

Testing of these signals at different levels is more difficult, as it would be preferred to measure this with a differential probe. Unfortunately these were unavailable and the oscilloscope with multiple isolated inputs had no capturing capabilities. Inspection proved that the propagation delay was more than sufficiently small, smaller than the propagation time through the gate driver. This leaves only the shape of the pulse to be discussed. The best case waveform would be a perfect square wave at TP7 and TP6, both with respect to $PV_{(n)}$. This can also be measured with an oscilloscope, as can be seen in Figures 9.2 and 9.3. Both images are strongly zoomed in on the edges, and the dead time shown is about 100 ns. The small bump that can be seen shortly after $Q_{(n)b}$ turning off on TP7 and is caused by the clamping MOSFET turning on and off, and the small drop on TP7 after the turning on of $Q_{(n)b}$ shows the clamping in action.

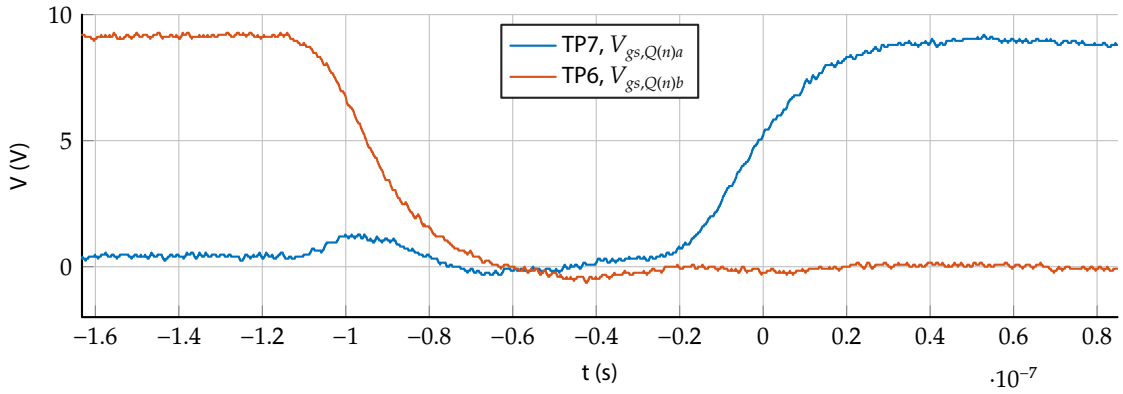

Figure 9.2: Switching and clamping MOSFET gate signals at rising edges.

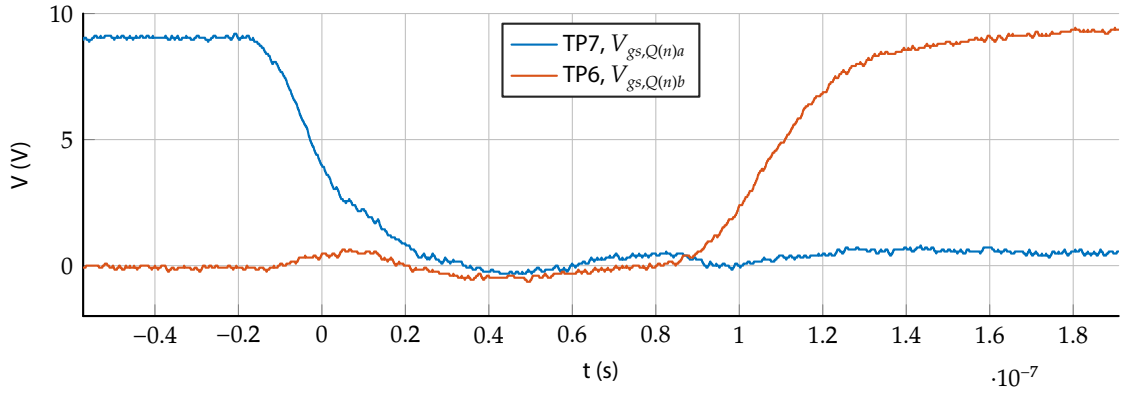

Figure 9.3: Switching and clamping MOSFET gate signals at falling edges.

While these images are taken at the worst case position (the furthest from the driver and highest of the string) this does not necessarily mean that the intermediate signals are equally sufficient. To avoid an overload of plots, many potential test points of interest in Figure 8.2 were omitted. They were all in line with the performance shown and provided no additional information needed to asses the performance of the system. This leads to the conclusion that the gate driving system performs as expected.

One other aspect must be discussed, and that would be power consumption. The static power consumption of the gate driver ICs and oscillator proved to be very small: well below 5 mA at 9 V for both sections together. When oscillating at a relatively high frequency (600 kHz) the power consumption was still surprisingly small but increased with approximately 7 mA per channel. From this can be concluded that for each additional solar cell the required driving power would be 14 mW. This would decrease linearly with frequency, and thus depends on the amount of balancing needed. This means that for 185 cells, one cell is used to provide the power to drive the balancing system.

The last test concerning balancing requires the full system to be operational, and will be discussed in Section 8.5.

9.2 Current Sharing Switching

It became clear early on that while the system performed well on low-frequency switching, the bandwidth of the level shifting system was far below the required bandwidth to function. This could be observed from the

fact that the two upper MOSFETs, Q1 and its counterpart[1] have proper behaviour as can be seen in Figure 9.4. It can be argued that the rise time could be improved as no oscillating behaviour can be seen while the RC decay still limits the rise time significantly. The MOSFETs did not heat up and the resistors were left in place for initial testing. The PCB layouting was apparently good enough to omit the gate stopper resistor entirely, as the system showed no oscillation when they were removed. These new plots were not very spectacular as they show the same shape as Figure 9.4.

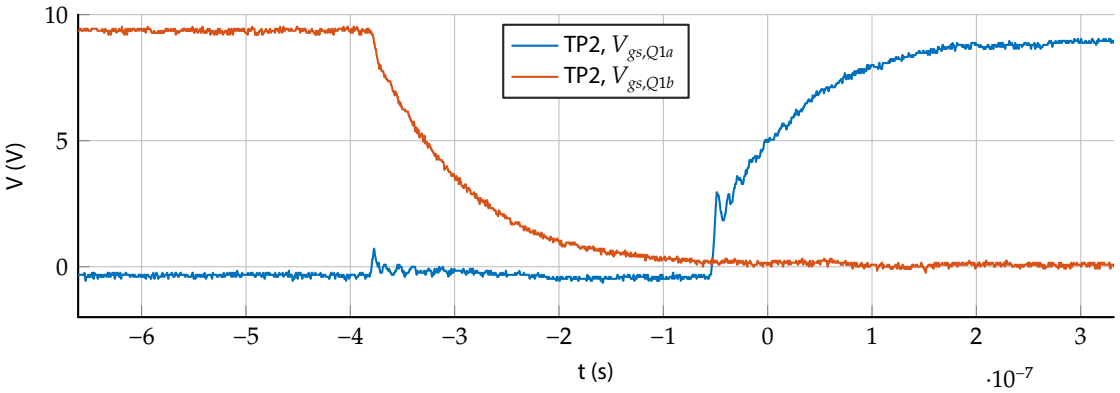

Figure 9.4: High side MOSFET driving signals.

With a square wave input and output of the gate driver U3 of Figure 8.3 the signal at TP3 would distort to a triangle wave at frequencies above 5 kHz. The triangle wave exhibited RC charge and discharge behaviour, leading to the conclusion that a capacitance was not modeled properly during the simulation. When adding the specified 25 pF Q_{gs} of the level shifting MOSFET Q3, the simulated system showed the same behaviour as the real life implementation. The RC time constant of R1 and this added capacitor was in the same order of magnitude and slightly lower as the intended frequency, leading us to believe that this was the cause. R1 and R3 were decreased from 100 kΩ to 1 kΩ, which theoretically should place the cutoff frequency of the parasitic filter two decades higher. This quick analysis and solution had the intended result, giving waveforms as can be seen in Figures 9.5 and 9.6. RC decay is still present but is now of the same order of magnitude as the rise time at the output of the gate drivers with schmitt trigger inputs. The main difference is the delay between TP3 and TP4, which has been reduced significantly. Arguments for lower gate stopper resistors can still be made, however.

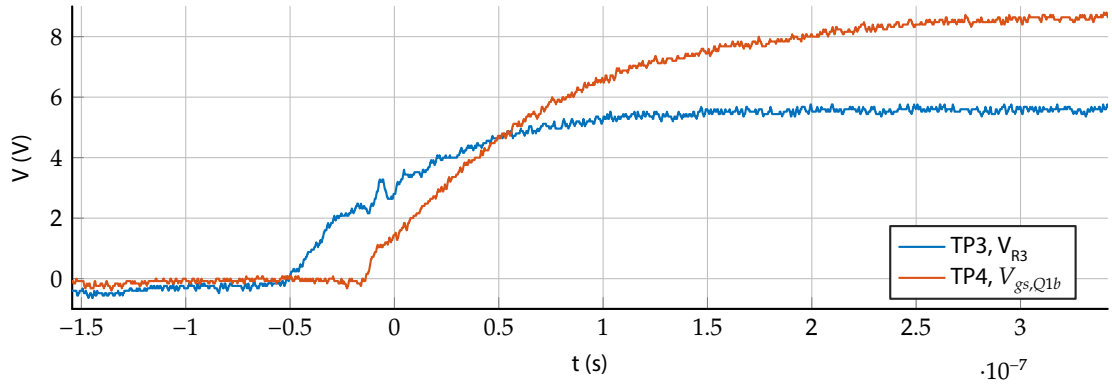

Figure 9.5: Low side MOSFET drive signal and gate driver input on rising edge.

[1] Figure 8.3 shows only one MOSFET. The complementary MOSFET will be referenced to as Q1b, while the other will be referenced as Q1a.

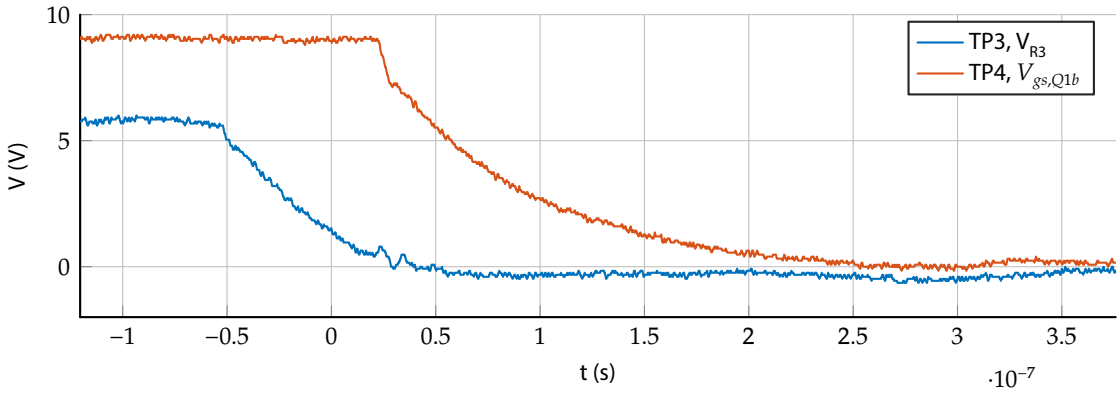

Figure 9.6: Low side MOSFET drive signal and gate driver input on falling edge.

LC filter

With the initial testing at 1 kHz the ripple was obviously much too large. During one cycle the capacitor buffer could be completely discharged and the resonant frequency was clearly present in the waveforms. All the spare capacitors we had were mounted on the board, totaling the buffer capacitor to 750 µF, but that still was not enough. When the bandwidth issue was solved, the capacitors were left on, because more capacitance can only increase filter performance and at 20 kHz the current ripple through the solar cells was still almost too large, in the order of 20 % of the nominal string current. Decreased capacitance would only worsen this as the RMS difference between the string voltage and capacitor voltage would increase. Increased frequency, to the initial target of 50 kHz did reduce both voltage and current ripple. It may be clear that a lot of optimization can still be done on the filter. However, since the load would need to be implemented quite differently on a real life product (i.e. CCM converter, flyback, etc) the operating characteristics would change drastically so no further research was done.

9.3 Track Balanced Solar Module

Given the troubles that occurred with the dummy load (Appendix B), little time was available to perform tests on the algorithm running on the MCU. In order to test the performance of the algorithm in conjunction with the balancing hardware the following test is carried out:

- Full illumination (Figure B.17)
- Shade cell C4 (Figure B.21)
- Full illumination (Figure B.17)
- Little illumination, solar panel was removed from the solar simulator
- Full Illumination (Figure B.17)
- Shade cell C1 (Figure B.19)

It is difficult to draw any conclusions on the exact behavior of the current and duty cycle settings as shown in Figure 9.8 and Figure 9.9, as the logging tool (Section 7.3.3) only logged every 10^{th} data point. Therefore, only

conclusions can be drawn on the rough value of both i_o and D. Table 9.1 lists the i_o and D ranges for each of the maximum power points and also lists the average values derived from the graphs for i_o and D.

Table 9.1: Full system maximum power point related values

Shading case	i_o (A) **MPP range**	D (%) **MPP range**	i_o (A) **Avg.**	D (%) **Avg.**
Full-Illum	3.4 - 4.3	45 - 60	4.3	54
C4-No-Illum	2.7 - 3.2	44 - 55	2.7	64
C1-No-Illum	2.5 - 3.5	90 - 100	2.9	65

According to Table 3.2, the algorithm should be able to get in range of the maximum power point (MPP range) with a power deviation from the maximum power point of maximum 5 %. Table 9.1 lists the belonging i_o and D values that mark the boundaries of the *MPP range* for the different shading cases.

For the full illumination case, the maximum power point is tracked according to the requirements. The full illumination case is one of the simpler to track since it had one very profound maximum, with smaller local maximums.

With the cell C4 fully shaded the algorithm is able to stay barely in bounds for i_o, however the duty cycle D is far off. It is hard to draw a conclusion why, but it seems that noise kept the algorithm in place, after which STAY got triggered. Because of STAY the algorithm stopped looking for a higher power value, but probably it needed BUMP mode (subsection 6.2.8) to find its way to the maximum power point.

The case in which cell C1 gets fully shaded is similar to the one of cell C4. However, the difference here is that the maximum power point in the case of C1 completely shifts to a duty cycle of 90–100 %, leaving a small maximum at the 50–65 % duty cycle range. This is also where the algorithm gets stuck, again a solution would be to search the power space with for example BUMP mode.

From the same figure it is also apparent that the requirement for Tracking Speed (2.3) is easily satisfied. For example it can be seen that the algorithm takes from about iteration 350 to 450 to get to the new maximum power point. This run was done at 100 Hz, so this took about one second.

From iteration 200 to 300 the algorithm goes twice in STAY mode, Figure 9.8 and Figure 9.9 are stable, indicating that both i_o and D are not set anymore. In Figure 9.7, one can clearly see that during the interval from iteration 200 to 300, the power is more stable as compared to the rest of the run. This could be beneficial in the future when other systems are going to be connected to the tracker.

In Table 9.2 the power values of just the 7 cells in series connected to the chroma load (Table 8.1) in MPPT mode. It is clear that as soon as one cell is shaded the power output completely collapses to about 3 % of the maximum possible power. This while in a ideal scenario it should drop to exactly $\frac{6}{7}$.

Table 9.2: Series stack power figures

Shading case	**Power**
Full-Illum	7.2 W
C1-No-Illum	0.22 W

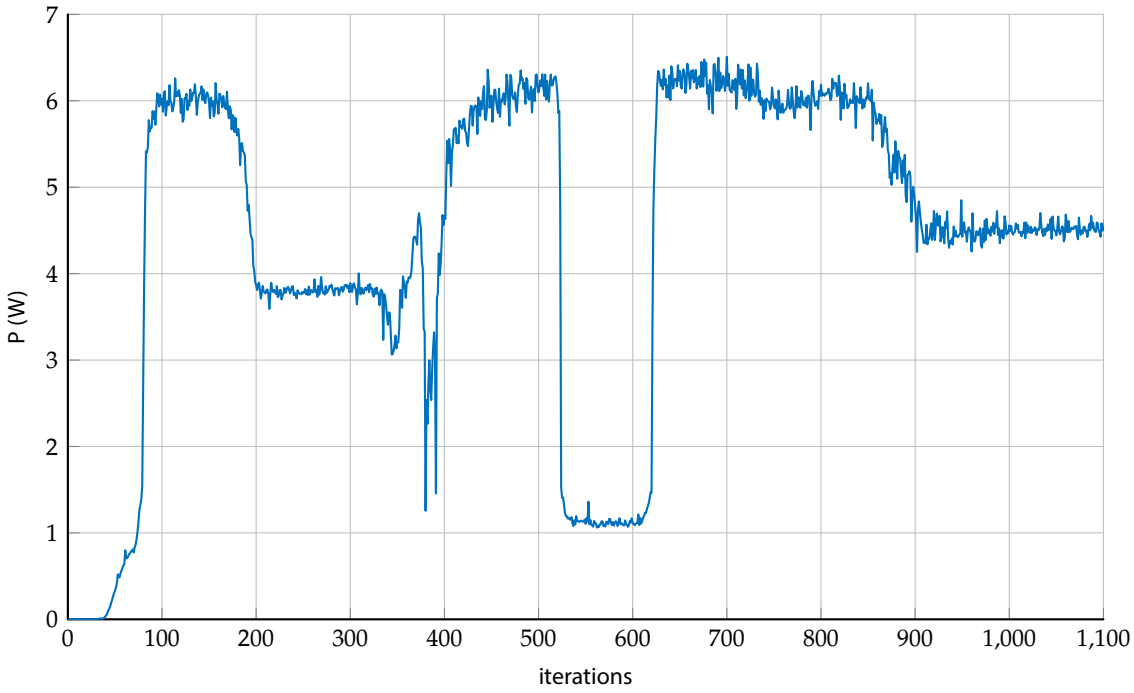

Figure 9.7: Power output with algorithm running on MCU @ 100 Hz

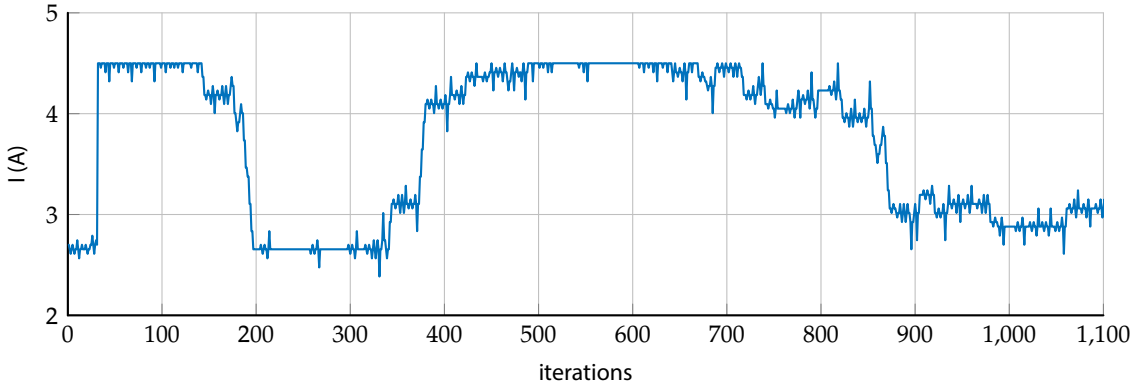

Figure 9.8: Current setting with algorithm running on MCU @ 100 Hz

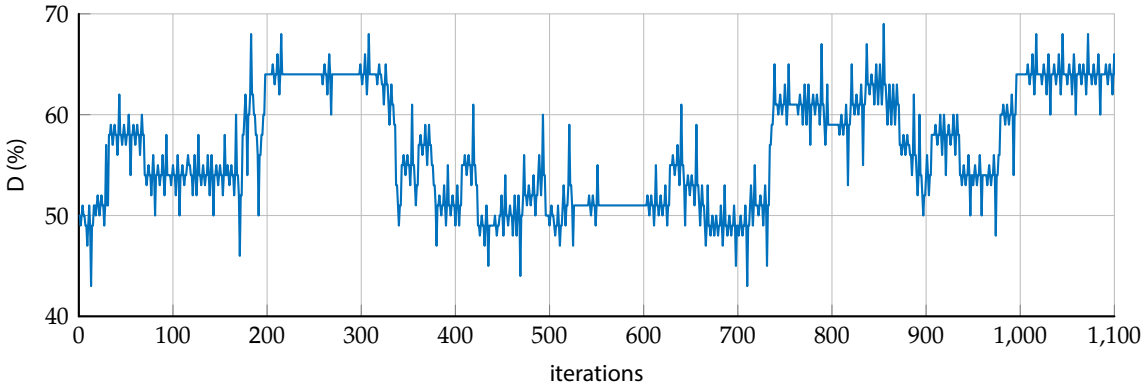

Figure 9.9: Duty setting with algorithm running on MCU @ 100 Hz

10 | Conclusions

10.1 Charge Redistribution

The papers of Chang and Leeb [7] have already proven that dDCR works. While we have also shown that power output increases significantly when charge redistribution is activated, the main goal of the thesis was to provide an improved driving circuit and MPPT. From the test results it is clear that especially the dDCR switching design works as intended and leaves room for deterioration when more MOSFETs are added. The rise times at the gate of each MOSFET is short, and the clamping circuit maintains level shifting without disturbing the driving signal.

With more careful routing, smaller packages and MOSFET development it seems very likely that dDCR will be a solution for the future.

10.2 Current Sharing Switching

The current sharing section proved itself during testing, but the main issue of current sharing remains bandwidth of the level shifter for the driver. While it was solved, the current bandwidth is only sufficient if enough power is dissipated in the current buffer at the cost of higher insertion losses. This issue can of course be easily be resolved with smaller transistors which are optimized further for low capacitance and high frequency as they do not need to carry large currents.

As far as efficiency is concerned, the current solution is not sufficient but the operating principle clearly works and as a proof of concept the possibilities have been explored. The main problem is that the optimal configuration for the LC filter and switching MOSFETs is dependent on the cell parameters.Since a temporary test setup was used, not all component parameters were not optimized for this configuration.

The main costs involved are for the MOSFETs. Other component prices are very low and only few are needed, much lower than for the other suggested solutions. It can be concluded that price wise a proper solution has been found that can be optimized for lower insertion loss as well.

10.3 Full system

To create a truly viable product an ASIC may be required to achieve maximum control speed and minimal insertion losses. Limited by parasitic elements, bandwidth and noise the full system gets to the MPP eventually but the time it takes is not constant. Sometimes it is a bit slow or gets stuck on local maximums. It does however meet requirement 2.4 of Table 3.1. With more work on the algorithm, or maybe different approaches, this should be able to be corrected.

dDCR works, but is only able to recover roughly $\frac{2}{3}$ of the power. This is more than the bypass diode and thus meets requirement 1.5 from Table 3.1. However, the measurement setup was not perfectly equal, so drawing a one to one comparison is not possible without a few assumptions. The amount of cabling needed to connect the balancing module is much more than for a simple series string. As the current to the load doubles when using SoCeBa doubles, losses would quadruple. Different loads also had to be used due to the operation limits of the loads available. However, the requirement is met and through optimization more can be gained, which is exactly what usually happens when making a first design iteration.

11 | Recommendations

11.1 Hardware

Concerning the hardware there are a few possible areas of improvement. Most of these concern efficiency and cost while some are of the more structural kind. Currently the oscillator is a separate IC running at at fixed frequency, but as the need for balancing decreases the frequency can be reduced to minimize driving losses. This requires that the oscillator can be controlled by the MPPT but ICs on the market which have such capabilities are usually more compex than necessary. Since the driver does contains only simple low voltage analog circuits this may be implemented directly on the same chip as the MPPT. The same principle goes for many parts of the discrete level shifting and driving solutions. Most of these are already implemented on an ASIC individually but the combining circuits required induce significant power loss.

The the question remains if the current sharing section is necessary. When the output stage changes its operating principle the filters can also be reconsidered and optimized. For example a dual primary flyback or two CCM inverting DC/DC converters could be used to provide current sharing with galvanic isolation between input channels. The development of such a system was never within the scope of this thesis, but needs to be considered for product development.

No tests were performed without the additional capacitors parallel to the PV cells. Whether this is necessary depends on the layout of the solar panels and should be investigated along with the development of the routing.

11.2 General

In the future, the developed technology has to be incorporated in a working product that should be placed as a daughter board at the back of a solar module. This to facilitate both separation upon disposal and customer choice. This also enables “half-way” upgrades as it were. For example if the technology makes a big leap, or other smart features are integrated, such as advanced cell health or soiling monitoring. This can be done by changing the current board to cable connector with a board to board connector. With a larger (near full scale) setup, all the system parameters can also be determined to be more efficient. If one adds a DC/DC converter to each SoCeBa module, one can create one high voltage bus to connect all panels. That bus can then go into the main inverter, delivering the energy to the grid using a DC/AC converter.

List of Figures

List of Tables

Bibliography

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Appendix A | Solar Cell Model Parameter Fitting

Manufacturers of PV products only specify the maximum output specifications and its I-V curve. For a decent model(Figure 2.5) R_s, R_p and the diode constant have to be fitted. Of course I_{pv} also has to be set to a maximum, the real value scales with the cells' irradiance. In Piazza and Vitale [18] a method is proposed to approach the model parameters for cells. The approaching algorithm is implemented in MATLAB. Using a couple of equations the I-V curve of the model can be calculated. Iteratively a better and better fit can be estimated. For calculating the curve with a reasonable resolution a lot (≈ 50) of equations have to be solved. Using a computing node these are solved in parallel. Each iteration increases R_s with 1 mΩ, so a couple hundred iterations are done. As a reference, the P-maxx 2500 mA cells used in [6] are modeled first. The curve fitted by the algorithm is shown in Figure A.2, its parameters are given in Table A.1.

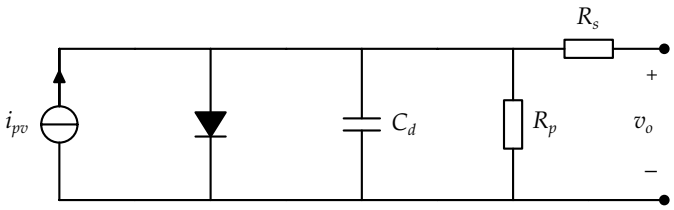

Figure A.1: Transient solar cell model, duplicate of Figure 2.5

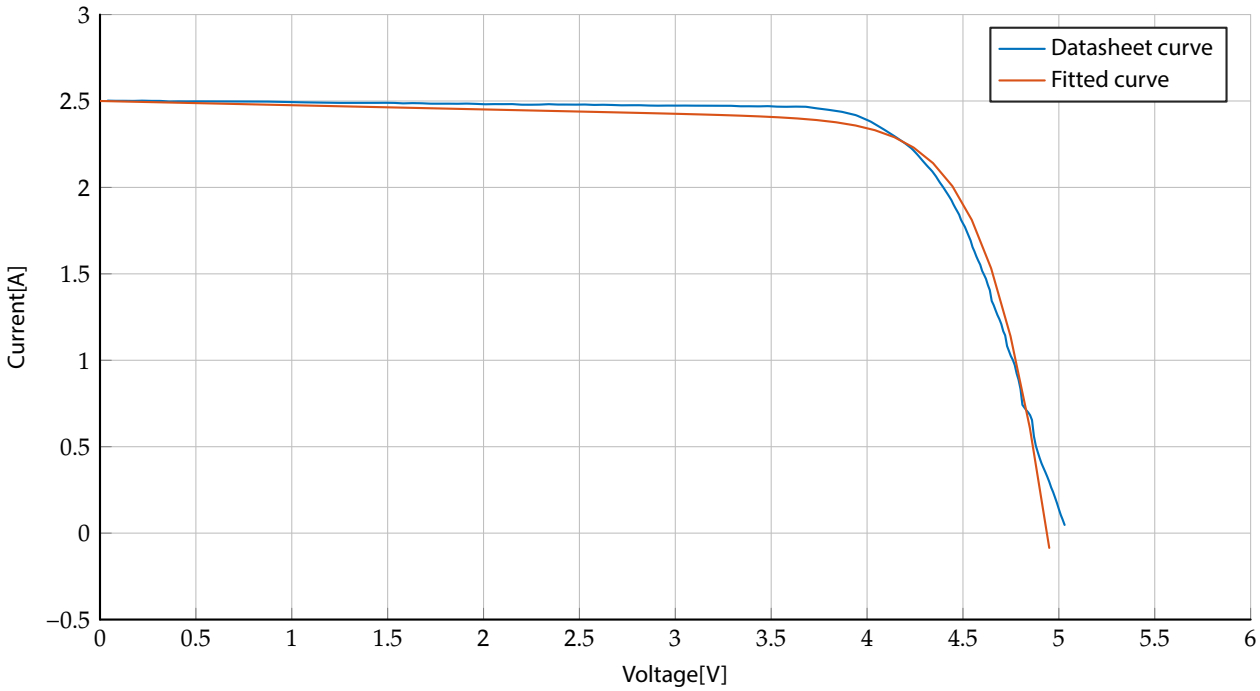

Figure A.2: The I-V curve fitted by the parameter estimating algorithm.

Table A.1: Model parameters of a P-maxx 2500mA used in [6].

name	**Value**
R_s	0.036 Ω
R_p	40.934 Ω
I_{pv}	2.5236 A
a	1.3

Appendix B | Controllable Dummy Load

To test the system a controllable load is needed. This load needs to be controllable by the MCU, accept low input voltages while maintaining high currents. The initial implementation can be seen in Figure B.1. The MOSFET $R_{DS,on}$ needs to be sufficiently small, but has nothing to do with losses as the MOSFET will operate in linear mode. It needs to be small because the PV string output voltage can drop significantly during testing when the current is near I_{sc}.

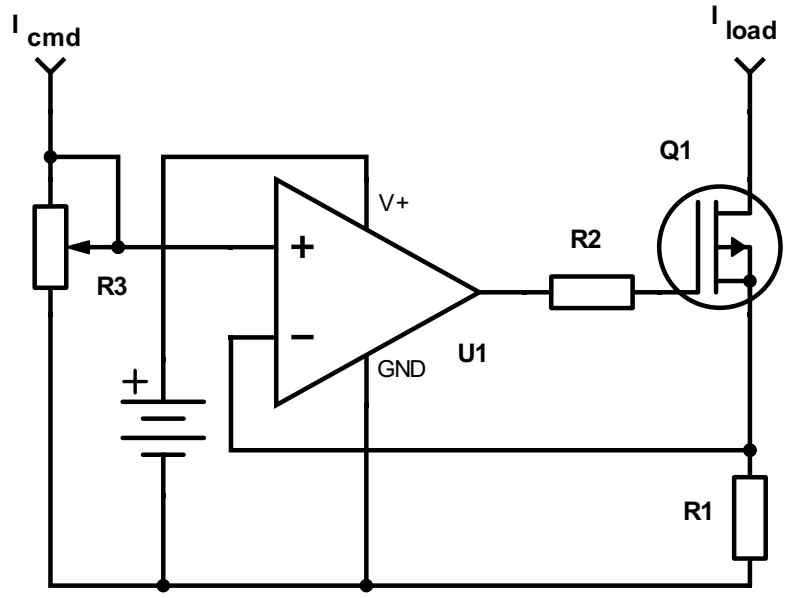

Figure B.1: Initial schematic of the controllable constant current sink (CCCS), or load.

A problem arose early on in testing. When the load was disconnected for example when only one section of the PV string was used at 50 % duty cycle, the feedback loop is broken. The op-amp would still see a current command, but no voltage across the shunt resistor and therefore it clips to its upper rail. At relatively high PWM frequencies the load effectively behaved as a short. When implementing RC filters to reduce the slew rate of the system to filter out the short absences of current, the system became too slow to operate together with the MCU. The command signal needs to be followed sufficiently fast, as the MCU also has a feedback loop. However, the design of this load is not within the scope of this thesis, and will not be discussed further as for a commercial design the load will most likely be a CCM converter or flyback step-up system. For the system test a separate off-the-shelf load was used, which required additional signal isolation. This interface is not a part of the thesis.