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INTEGRATED SILICON CARBIDE SUN POSITION SENSOR SYSTEM-ON-CHIP FOR SPACE APPLICATIONS

INTEGRATED SILICON CARBIDE SUN POSITION SENSOR SYSTEM-ON-CHIP FOR SPACE APPLICATIONS

Proefschrift

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aan de Technische Universiteit Delft,
op gezag van de Rector Magnificus prof. dr. ir. T.H.J.J. van der Hagen,
voorzitter van het College voor Promoties,
in het openbaar te verdedigen op maandag 19 december 2022 om 17:30 uur

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SUMMARY

This dissertation describes the development of the sun position sensor based on silicon carbide and integrated optics. The sun position sensor device is a navigation instrument that is commonly used on satellites for movement control. The operation of the device is to provide information of the location of the Sun, from which its name is derived. To do so, it relies on the incident sun light on light sensitive detectors that are functionalized to be angle sensitive. The sun position sensor device is commonly used on modern satellites and is based on conventional silicon semiconductor technology.

This research work aims to address the two major challenges that sun position sensor devices have, as is described in Chapter 1. The first challenge is the sensitivity towards visible light, which distorts the signal in sunrise or sunset conditions. In these situations, the visible light reflected by the Earth occupies a dominant portion of the sensor field-of-view, which cannot be distinguished from light directly from the Sun. To tackle this challenge, the sun position sensor is implemented in a wide bandgap semiconductor material, which limits the device selectivity to UV light. This drastically improves the sensor operation in the described conditions, as no UV light is reflected by the Earth. The second challenge is the satellite miniaturization trend, which demands smaller and cheaper instrumentation. This is tackled by advanced wafer-level packaging techniques, to integrate the sensor optics in a scalable microfabrication process.

The architecture and design of a sun position sensor can vary greatly, as there are different approaches towards angular sensitivity. As one of the goals is to develop a scalable microfabrication process, an architecture is chosen that is build from planar layers. This architecture is the collimating sun sensor, which includes the detectors, light mask and optical window. The design parameters and readout considerations are discussed and simulated in Chapter 2 for two implementations of the collimating sun sensor device, which are the quadrant sensor and the pixel array sensor. To circumvent the need for integration of the bulky optical window, an additional new architecture based on diffraction gratings is introduced and simulated.

This research adopts the wide bandgap material silicon carbide to tackle the first research challenge. The fabrication and characterization of integrated devices and circuits in silicon carbide is summarized in Chapter 3. The in-house silicon CMOS technology BICMOS7 is used for rapid prototyping and comparison of process parameters. It has seven design layers that includes a single well front-end-of-line and two-layer metal interconnect back-end-of-line. Similarly, the silicon carbide CMOS technology SICCMOS9 at Fraunhofer IISB has nine design layers, including a double well front-end-of-line and single-layer metal interconnect back-end-of-line. Furthermore, the SICCMOS9 technology employs polysilicon gates, which are used for local interconnections, while BICMOS7 has metal gates. Finally, the ohmic contacts are necessarily more complicated in SICCMOS9 by means of RTA of dedicated silicides in the respective n-type and p-type regions, in order to form proper ohmic contacts.

There are some major differences in extracted technology parameters, considering BICMOS7 and SICCMOS9. The SICCMOS9 doped layer sheet resistance is increased by a factor of 100, thus contributing more significantly to the source/drain series resistance on the device channel. Furthermore, the threshold voltages are about double in absolute magnitude in SICCMOS9, accompanied by increased subthreshold slopes and slope factors. Additionally, the device mobility and process transconductance are vastly lower in SICCMOS9. Overall this amounts to slower devices in the silicon carbide counterpart, and lower source/drain currents due to the larger channel resistance in the on-state. In both technologies, circuit blocks are implemented and validated for correct operation. These circuit blocks include inverters, NAND gates, NOR gates, 1-bit digital multiplexer, 1-bit analog multiplexer, d-flipflop, push-pull transconductance amplifier, comparator, unity-gain buffer, 2-bit ADC and SRAM cell. The effects of temperature are investigated on the same devices and circuit blocks, clearly indicating the severe influence on silicon device leakage current, which is negligible in the silicon carbide implementation. The temperature effects are furthermore exploited to perform temperature sensing in silicon carbide, using resistors in the implanted layers and a CTAT based on CMOS transistors.

Silicon carbide photodetectors for UV selective detection are designed and implemented in Chapter 4, using three variants of PN photodiodes. The peak responsivity is achieved at a wavelength of 290 nm, which could be further optimized by changing the doping profile or ARC coating. Comparing with the silicon counterparts, the silicon carbide photodetectors exhibit superior UV selectivity that can be used for albedo rejection in sun position sensors. These photodetectors are integrated in the commonly employed 3-transistor active pixel architecture, which allows for the implementation of addressable pixel arrays. In these opto-electronic circuits, the silicon carbide implementations did not show any response to ambient light. These active pixels are complemented by connection to a comparator or voltage buffer for further signal processing. The comparator variant effectively digitizes the pixel output, while the voltage buffer copies the signal level. These circuit blocks have limited switching speed, thus limiting the response times of these opto-electronic circuits. Furthermore, the silicon carbide photodiodes did not show degradation at a temperature of 200 °C, while the silicon photodiodes are rendered inoperable at this temperature.

The active pixels are configured in an 8×8 array with addressable rows and columns. Each column has its own analog processor, which includes the aforementioned comparator and analog buffer circuit blocks. This allows for two system readout modes; analog or digital. The system is further expanded by a 2-bit ADC, which adds a third system readout mode. This system amounts to 1263 transistors on a $10 \times 10\,\mathrm{mm}^2$ chip and is implemented both in the silicon and silicon carbide technologies. The functional blocks in the system are verified by electrical measurement and their response times are profiled. As the silicon carbide devices generate orders of magnitude lower photocurrent, the pixel response is proportionally slower. Nevertheless, the full silicon carbide array of 64 pixels is readout at a 0.39 Hz refresh rate. The timing of the silicon counterpart is not optimized, but runs at >2.0 Hz. The achieved preliminary yield is promising, with 78 % of the silicon carbide devices operating as intended.

The second research challenge that develops a scalable microfabrication process is investigated in Chapter 5. There are several options that are considered, including the

patterning of transparent substrates and the 3D printing of transparent polymer. However, it was found that the standard thermocompressive bonding matches well with the application, and was therefore optimized for the sun position sensor device. This technique employs a patterned adhesive on the device wafer, followed by bonding sapphire optical windows under mechanical pressure and elevated temperature. The adhesive pattern is an outline around the sensor detectors, directly on top of the CMOS readout circuitry. The width and spacing of this outline is varied to find the best pattern in terms of predicted bond strength and preliminary yield on test wafers. The used adhesive material is epoxy-based SU-8 photoresist, which is deposited by spin coating and patterned by standard lithography, yielding an SU-8 layer thickness of (9.27 ± 0.23) µm. The bond strength of the selected pattern is investigated by die shear testing and resulted in (78 ± 65) N, or (6.9 ± 5.8) MPa. The detachment failure mode is found to always be between the SU-8 and the sapphire optical window, which is in accordance with the predicted bond strengths of its datasheet.

Finally, the opaque light mask layer is deposited on top of the bonded stack and patterned by spray coating, which is followed by alignment and exposure in the mask aligner. Where this worked well for the silicon platform that was used for prototyping, the yield dropped to zero on the silicon carbide wafers. The critical steps were in the wet chemical processing at the very end of the fabrication, including the development, wet etching and cleaning of the wafer. As silicon carbide device wafers are a scarce resource, the issue is combated by adding glue droplets right after deposition of the light mask layer. This glue deposition is done on wafer-level on the optical window corners. With this modification, the process yield was restored. The light mask overlay alignment is verified by optical inspection through the pattern on the optical window, indicating a typical shift of 30 µm. This alignment is deemed adequate for the much larger aperture and photodetectors, but should be improved in future work by adopting different alignment strategies, such as backside alignment or the use of a wafer stepper.

The resulting devices are verified for operation and characterized for angular response. The best performing quadrant sensor device reaches a mean angular accuracy (MAA) of 1.9° in a ±33° field-of-view and the readout is done by analog measurement of the generated photodetector currents. The pixel array sensor reaches a MAA of 5.7° in a ±37° field-of-view, using its analog output mode. The lower MAA would be improved by optimizing its design parameters, such as the optical window thickness and aperture dimension. The current implementation suffers from blind spots and only utilizes part of the active area. Lastly, the alternative to the bulky optics integration is investigated, relying on diffraction gratings. This investigation is limited to monochromatic light, as the structures are specifically designed for a single wavelength. Both the amplitude and phase grating architectures are measured, resulting in a MAA of 0.6° in a ±26° field-of-view and a MAA of 2.8° in a ±45.5° field-of-view, respectively. The higher EQE of the phase gratings allows for the larger field-of-view. The demonstrated silicon carbide device and system operation at elevated temperature is superior over the silicon implementation. This is an added benefit for the application in space technology and indicates great potential for application in other harsh environments as well. The sun position sensor device with integrated optics was also subjected to this elevated temperature, without noticeable degradation of the device.

SAMENVATTING

Dit proefschrift beschrijft de ontwikkeling van de zon positie sensor gebaseerd op silicium carbide en geïntegreerde optica. Het zon positie sensor apparaat is een navigatie instrument dat vaak word gebruikt op satellieten voor bewegingscontrole. De werking van het apparaat is om informatie te verstrekken over de locatie van de zon, waarvan de naam is afgeleid. Om dit te doen, vertrouwt het op het invallende zonlicht op lichtgevoelige detectoren die zijn gefunctionaliseerd om hoekgevoelig te zijn. De zon positie sensor wordt vaak gebruikt op moderne satellieten en is gebaseerd op conventionele silicium halfgeleider technologie.

Dit onderzoekswerk richt zich op de twee grootste uitdagingen die zon positie sensor apparaten hebben, zoals beschreven in Hoofdstuk 1. De eerste uitdaging is de gevoeligheid voor zichtbaar licht, dat het signaal vervormt bij zonsopgang of zonsondergang condities. In deze situaties neemt het zichtbare licht dat door de aarde wordt gereflecteerd een dominant deel van het gezichtsveld van de sensor in, wat niet kan worden onderscheiden van licht dat rechtsreeks van de zon komt. Om deze uitdaging aan te gaan, is de zon positie sensor geïmplementeerd in een halfgeleidermateriaal met een brede bandgap, waardoor de selectiviteit van het apparaat tot UV licht wordt beperkt. Dit verbetert de werking van de sensor in de beschreven omstandigheden drastisch, omdat er geen UV licht door de aarde wordt gereflecteerd. De tweede uitdaging is de miniaturisatie trend van satellieten, die kleinere en goedkopere instrumentatie vereist. Deze uitdaging word aangegaan door geavanceerde verpakkingstechnieken op wafer niveau, om de sensor optica te integreren in een schaalbaar microfabricage proces.

De architectuur en het ontwerp van een zon positie sensor kan sterk variëren, omdat er verschillende benaderingen zijn voor hoekgevoeligheid. Omdat een van de doelen is om een schaalbaar microfabricage proces te ontwikkelen, is gekozen voor een architectuur die is opgebouwd uit vlakke lagen. Deze architectuur is de collimerende zon sensor, die de detectoren, het lichtmasker en het optische venster omvat. De ontwerpparameters en uitleesoverwegingen worden besproken en gesimuleerd in Hoofdstuk 2 voor twee implementaties van de collimerende zon sensor, namelijk de kwadrant sensor en de gerangschikte pixel sensor. Om de noodzaak voor integratie van het omvangrijke optische venster te omzeilen, wordt een aanvullende nieuwe architectuur op basis van diffractieroosters geïntroduceerd en gesimuleerd.

Dit onderzoek gebruikt het brede bandgap materiaal silicium carbide om de eerste onderzoeksuitdaging aan te gaan. De fabricage en karakterisering van geïntegreerde apparaten en schakelingen in silicium carbide is samengevat in Hoofdstuk 3. De interne silicium CMOS technologie BICMOS7 wordt gebruikt voor snelle prototyping en vergelijking van procesparameters. Het heeft zeven ontwerplagen, waaronder een enkele put voorkant-van-de-lijn en tweelaags metalen verbinding achterkant-van-de-lijn. Evenzo heeft de silicium carbide CMOS technologie SICCMOS9 bij Fraunhofer IISB negen ontwerplagen, waaronder een voorkant-van-de-lijn met dubbele put en achterkant-van-

de-lijn met een enkele metalen verbinding. Bovendien maakt de SICCMOS9 technologie gebruik van polysilicium poorten, die worden gebruikt voor lokale verbindingen, terwijl BICMOS7 metalen poorten heeft. Ten slotte zijn de ohmse contacten in SICCMOS9 noodzakelijkerwijs gecompliceerder door middel van RTA van speciale siliciden in de respectievelijke n-type en p-type gebieden, om goede ohmse contacten te vormen.

Er zijn enkele grote verschillen in de afgeleide technologieparameters, rekening houdend met BICMOS7 en SICCMOS9. De weerstand van de SICCMOS9 gedoteerde lagen is verhoogd met een factor 100, en levert daardoor een grotere bijdrage aan de source/drain serieweerstand op het apparaat kanaal. Bovendien zijn de drempelspanningen ongeveer het dubbele in absolute waarde in SICCMOS9, gepaard met verhoogde subdrempelhellingen en hellingsfactoren. Verder zijn de mobiliteit van het apparaat en de procestransconductantie veel lager in SICCMOS9. Over het algemeen komt dit neer op langzamere apparaten in de silicium carbide uitvoering, met lagere source/drain stromen vanwege de hogere kanaalweerstand in de aan-status. In beide technologiën zijn schakelingen geïmplementeerd en gevalideerd voor een correcte werking. Deze schakelingen zijn inverters, NAND poorten, NOR poorten, 1-bit digitale multiplexer, 1-bit analoge multiplexer, d-flipflip, push-pull transconductantieversterker, comparator, unity-gain buffer, 2-bit ADC en SRAM cel. The effecten van temperatuur zijn onderzocht op dezelfde apparaten en schakelingen, wat duidelijk de ernstige invloed op de lekstroom van de silicium apparaten aangeeft, welke verwaarloosbaar is in de implementatie in silicium carbide. De temperatuureffecten zijn bovendien benut door temperatuurmetingen uit te voeren in silicium carbide, met behulp van weerstanden in de gedoteerde lagen en een CTAT op basis van CMOS transistoren.

Silicium carbide fotodetectoren voor UV selectieve detectie zijn ontworpen en geïmplementeerd in Hoofdstuk 4, met behulp van drie varianten PN fotodiodes. De piekresponsiviteit wordt bereikt bij een golflengte van 290 nm, welke verder kan worden geoptimaliseerd door het dopingprofiel of de ARC coating te wijzigen. In vergelijking met de silicium tegenhangers, vertonen de silicium carbide fotodetectoren een superieure UV selectiviteit die kan worden gebruikt voor albedo afwijzing in zon positie sensoren. Deze fotodetectoren zijn geïntegreerd in de veelgebruikte actieve 3-transistor pixelarchitectuur, die de implementatie van adresseerbare pixel rangschikking mogelijk maakt. In deze opto-elektronische schakelingen, vertoonden de silicium carbide implementaties geen enkele reactie op omgevingslicht. Deze actieve pixels worden aangevuld met een aansluiting op een comparator of spanningsbuffer voor verdere signaalverwerking. De comparator variant digitaliseert effectief de pixeluitvoer, terwijl de spanningsbuffer het signaalniveau kopieert. Deze schakelingen hebben een beperkte schakelsnelheid, waardoor de reactietijden van deze opto-elektronische schakelingen worden beperkt. Verder vertoonden de silicium carbide fotodiodes geen degradatie bij een temperatuur van 200 °C, terwijl de silicium fotodiodes onbruikbaar worden bij deze temperatuur.

De actieve pixels zijn geconfigureerd in een 8×8 rangschikking met adresseerbare rijen en kolommen. Elke kolom heeft zijn eigen analoge processor, die de bovengenoemde comparator en spanningsbuffer schakelingen bevat. Dit stelt twee systeem uitleeswijzen ter beschikking; analoog of digitaal. Het systeem wordt verder uitgebreid met een 2-bit ADC, die een derde uitleeswijze toevoegt. Dit systeem telt 1263 transistors op een $10 \times 10\,\mathrm{mm}^2$ chip en is zowel in silicium als silicium carbide technologie geïm-

plementeerd. De functionele blokken in het systeem zijn geverifieerd door elektrische metingen en hun reactietijden zijn geprofileerd. Omdat de silicium carbide apparaten een orde van grootte lagere fotostroom genereren, is de pixelreactie proportioneel langzamer. Desalniettemin wordt de volledige silicium carbide rangschikking van 64 pixels uitgelezen met een ververs snelheid van 0.39 Hz. De timing van de silicium tegenhanger is niet geoptimaliseerd, maar loopt op >2.0 Hz. De voorlopige behaalde opbrengst is veelbelovend, waarbij 78 % van de silicium carbide apparaten werkt zoals bedoeld.

De tweede onderzoeksuitdaging is een schaalbaar microfabricage proces ontwikkelen, en is onderzocht in Hoofdstuk 5. Er zijn verschillende opties overwogen, waaronder het modelleren van transparante substraten en het 3D printen van transparant polymeer. Het werd echter bevonden dat standaard thermocompressieve verbinden goed past bij de toepassing en is daarom geoptimaliseerd voor de zon positie sensor. Deze techniek maakt gebruik van een lijm patroon op de apparaat wafer, gevolgd door het hechten van optische vensters van saffier onder mechanische druk en verhoogde temperatuur. Het lijm patroon is een omtrek rond de sensordetectoren, direct bovenop de CMOS schakelingen. De breedte en tussenruimte van de omtrek worden gevarieerd om het beste patroon te vinden in termen van voorspelde hechtsterkte en voorlopige opbrengst op testwafers. De gebruikte lijm is SU-8 fotolak op epoxybasis, die wordt gevormd door spincoating en patroonvorming door standaard lithografie, wat een SU-8 laagdikte van (9.27 ± 0.23) µm oplevert. De hechtsterkte van het geselecteerde patroon is onderzocht door middel van afschuiftesten en resulteerde in (78 ± 65) N, of (6.9 ± 5.8) MPa. Het falen van de hechting is altijd tussen de SU-8 en het optische venster, wat in overeenstemming is met de voorspelde hechtsterktes van de datasheet.

Ten slotte wordt de ondoorzichtige lichtmaskerlaag aangebracht bovenop de gebonden stapel en van patroon voorzien door sproeicoating, gevolgd door uitlijning en belichting in de maskeruitlijner. Waar dit goed werkte op het silicium platform dat werd gebruikt voor prototyping, zakte de opbrengst op de silicium carbide wafers naar nul. De kritieke stappen waren in de natte chemie verwerking aan het einde van de fabricage, welke de ontwikkeling, nat etsen en reinigen van de wafer omvatten. Omdat silicium carbide apparaat wafers een schaars goed zijn, wordt dit probleem bestreden door lijmdruppels toe te voegen direct na het aanbrengen van de lichtmaskerlaag. Het aanbrengen van deze lijm gebeurt op waferniveau op de hoeken van de optische vensters. Met deze modificatie werd de procesopbrengst hersteld. De uitlijning van de lichtmaskerlaag is geverifieerd door optische inspectie door de opening op het optische venster, wat wijst op een typische verschuiving van 30 µm. Deze uitlijning wordt voldoende geacht voor de veel grotere opening en fotodetectoren, maar zou in toekomstig werk moeten worden verbeterd door andere uitlijnstrategieën toe te passen, zoals uitlijning op de achterkant of het gebruik van een waferstepper.

De resulterende apparaten worden gecontroleerd op werking en gekarakteriseerd voor hoekrespons. De best presterende kwadrant sensor bereikt een gemiddelde hoeknauwkeurigheid (MAA) van 1.9° in een ±33° gezichtsveld en de uitlezing wordt gedaan door analoge meting van de gegenereerde fotodetectorstromen. De gerangschikte pixel sensor bereikt een MAA van 5.7° in een ±37° gezichtsveld, met behulp van de analoge uitvoermodus. De lagere MAA kan worden verbeterd door de ontwerpparameters te optimaliseren, zoals de dikte van het optische venster en de afmetingen van de opening

in de lichtmaskerlaag. De huidige uitvoering heeft last van blinde gebieden en benut slechts een deel van het actieve gebied. Ten slotte wordt het alternatief voor de omvangrijke optica integratie onderzocht, waarbij gebruik wordt gemaakt van diffractieroosters. Dit onderzoek beperkt zich tot monochromatisch licht, omdat de structuren specifiek zijn ontworpen voor een enkele golflengte. Zowel de amplitude- als de faserooster architecturen zijn gemeten, wat resulteert in een MAA van 0.6° in een ±26° gezichtsveld en een MAA van 2.8° in een ±45.5° gezichtsveld, respectievelijk. De hogere EQE van de faseroosters zorgt voor een groter gezichtsveld. De gedemonstreerde silicium carbide apparaat en systeem werking bij verhoogde temperatuur is superieur ten opzichte van de implementatie in silicium. Dit is een bijkomend voordeel voor de toepassing in de ruimte technologie en wijst op een groot potentieel voor toepassing in andere ruwe omgevingen. Ook het zon sensor apparaat met geïntegreerde optica werd aan deze verhoogde temperatuur blootgesteld, zonder merkbare degradatie van het apparaat.

1

INTRODUCTION

The art and science of asking questions
is the source of all knowledge.

Thomas Berger

For over half a century, humankind has send off spacecraft into outer space for exploration, communication, observation and more. Modern society depends heavily on satellites and will demand ever more from the next generation. For the majority of spacecraft, movement control is vital for successful operation and therefore the acquisition of the spacecraft attitude is an important aspect. The devices used for this are called attitude sensors, of which the sun position sensor is most commonly adopted. The two main scientific challenges for the next generation of sun position sensors, namely the signal distortion by reflection from the Earth and the scalable integration of sensor optics, will be specifically addressed in this thesis research. This is relevant for the increasing need to deploy satellites, as it yields better performing devices and a scalable fabrication technology.

1

SATELLITES are employed for many tasks that become ever more demanding. To keep up with our changing society's needs, more satellites are expected with greater diversification. As a result, space instrumentation is continuously subjected to application specific requirements, that generally call for cheaper, smaller and better performing devices. The success for most space missions starts with the ability to control the movement of the satellite. The movement control of spacecraft is called attitude control, which encompasses information on the spacecraft location and direction. Common examples of attitude sensors are magnetometers, sun sensors, earth horizon sensors and star sensors. Detailed descriptions on the operation of all the mentioned attitude sensors exist [1], but in this work the focus is only on the sun sensor.

The history of the sun position sensor predates any satellite launched into space by many centuries. Rudimentary structures where already used in ancient times to track the seasons according to the location of the sun. Later centuries brought instrumentation that could be used for daytime navigation. In the early 1950s, the first sun sensors were employed for the guidance of solar telescopes, in automatic sextants[1] and for the guidance of heliostats[2]. Early implementation of the sun sensor was by phototubes, which are basically gas-filled or vacuum tubes that are sensitive to light. These phototubes are still widely today used as photomuliplier tubes, which amplify the electrical current produced by incident light by a large amount, in the fields of Raman spectroscopy, fluorescence spectroscopy and confocal microscopy. With the emerging of space flight however, miniaturization and ruggedness became important factors for the sun position sensor. This resulted in the adaptation of devices in solid-state semiconductor material, first the photoresistor and later the photodiode in favor of sensitivity.

At the conclusion of the space milestones in the 1960s, the importance of improved space instrumentation was recognized and reported. For example, NASA formulated the need for sun sensing devices by capturing all aspects of such devices in great detail [2].

[1] A sextant is a navigation instrument that measures the angular distance between two objects.
[2] A heliostat is a device with a turning mirror to keep reflecting sunlight towards a predetermined target.

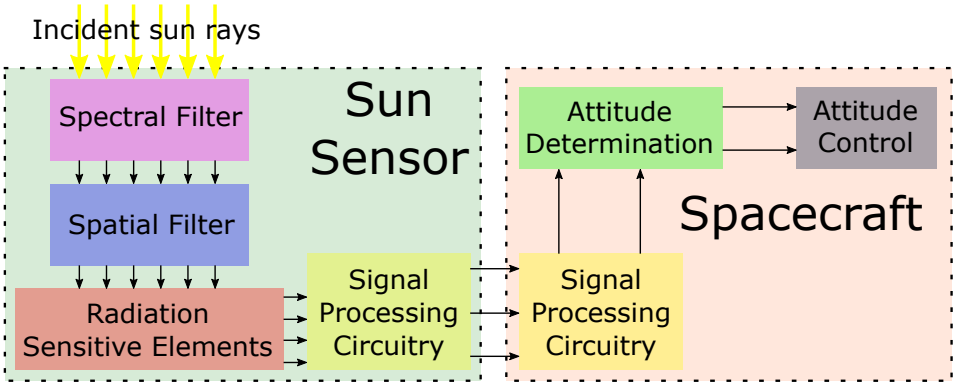


Figure 1.1: Functional elements of the sun position sensor and related spacecraft elements. The defined functional blocks are not bound to discrete hardware blocks, which means that a single hardware block can implement several or partial functional blocks. Modified representation from design criteria by NASA [2].

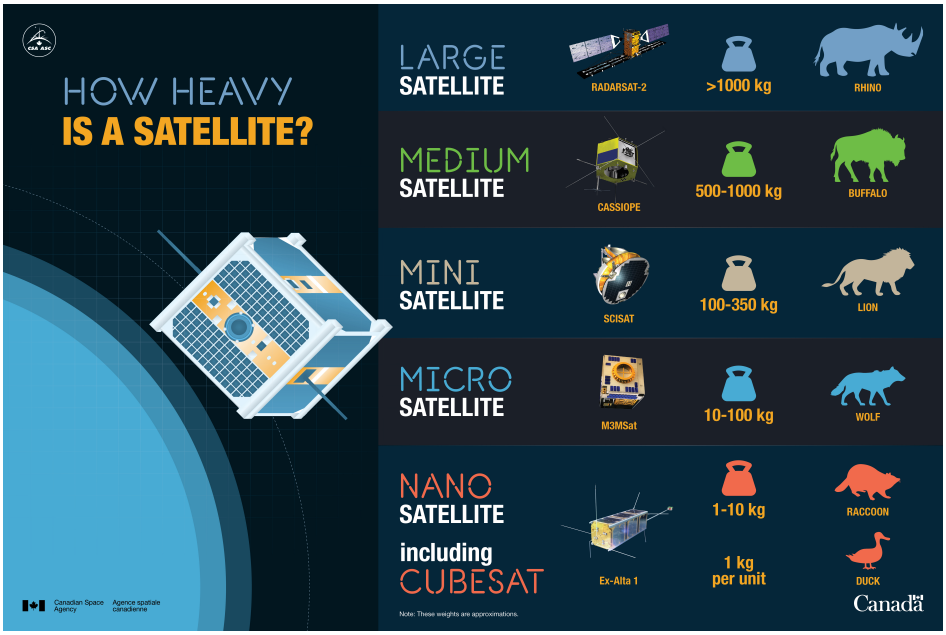


Figure 1.2: Overview of different satellite classes and their weight compared to animals for reference which includes the large, medium, mini, micro and nano satellites. Note that the smaller pico, femto an atto satellites are not included in this set. © Canadian Space Agency [3].

The sun position sensor system also became more complete, with readout circuits and communication capability integration in-package or on-chip. The functional block diagram of the sun position sensor for attitude control is given in Figure 1.1, dividing the sun position sensor in the spectral filter, spatial filter, radiation sensitive elements and signal processing circuitry blocks. It should be noted that the implementation of these blocks may overlap in real-world devices. For example, using photodetection in semiconductor material implies sensitivity for a specific spectral range, therefore capturing parts of both the spectral filter and radiation sensitive elements.

The well known miniaturization trend in the semiconductor industry, an its challenges [4], has set the stage for other industries to follow. A similar trend is also seen for space satellites [5], which makes access to space cheaper. An overview of different satellite weight classes is given in Figure 1.2, where the large, medium, mini and micro formats are the classical satellites in use today. The CubeSat format enabled the emerging field of drastic satellite miniaturization and, as shown in the illustration, it is shaped and sized like a carton of milk with the capability of housing multiple stacked printed circuit boards [6]. More recently, pico satellites (0.1–1 kg), femto satellites (10–100 g) and atto satellites (1–10 g) emerged. The pico satellite is still of the CubeSat format, but the femto and atto satellites are build around the much smaller ChipSat format [7–9]. These small satellites are cheaper and can work in networks, allowing higher system reliability and increased coverage of the region of interest. However, shrinking the satellite means that its instrumentation, such as the sun position sensor, must be miniaturized as well.

1

This introduction chapter provides overviews of the sun position sensor device, including presently available devices and the challenges for the future generations. To address the challenges, the migration to wide bandgap material is proposed and an overview of such materials is given. To complete the device fabrication, wafer-level packaging is suggested and the technology is discussed. Finally, the chapter concludes with the proposed research solution and lists the research questions.

1.1. SUN POSITION SENSORS

The working principle of the sun position sensor is the determination of the direction vector towards the sun. In order to do this the sensor needs the functional elements in Figure 1.1, of which the spatial filter is found in diverse implementations. This section provides an overview of the different sensor types and a list of state-of-the-art devices. This is accompanied with the challenges for the next generation and the functional specification of the device development in this work.

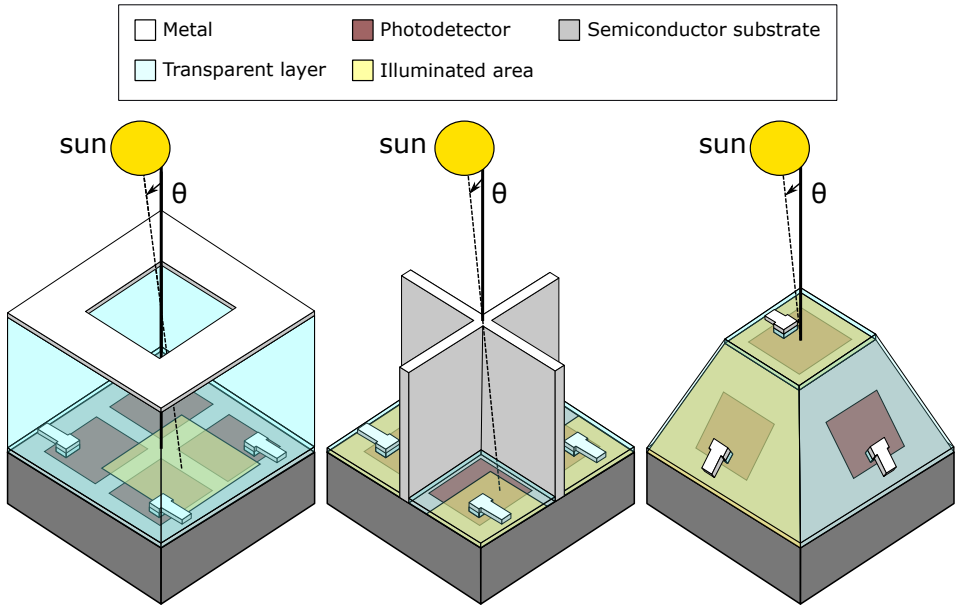
1.1.1. DIFFERENT APPROACHES TO SUN SENSING

A thorough review on sun position sensors was made by Salgado-Conrado in 2017, highlighting different types as well as sensor outputs and transmission classifications [10]. The four defined types are the collimating sensors, sun-pointing sensors, tilted mount sensors and hybrid sensors. These classifications are used as guidelines in this research work, but it should be noted that the diverse and creative implementations in existence do not always allow for straightforward classification. In the classification of the different types, the spatial filter (see Figure 1.1) implementation is a leading characteristic.

Firstly, the collimating sensor type (Figure 1.3a) implements the spacial filter by a light masking layer on top of a collimator. The collimator is typically a transparent spacer with possible additions like lenses and mirrors to ensure parallel incident light rays. The light masking layer is typically implemented by a pinhole in a light blocking thin film. Omitting the lenses and mirrors (as illustrated), results in a device that has planar detector and spacial filter designs, which matches well with microfabrication technologies.

Secondly, the sun-pointing sensor type (Figure 1.3b) implements the spacial filter by shadows typically cast by an opaque pillar or wall on top of the sensor. These pillars or walls have large step heights of orders of magnitude larger than the photodetectors, rendering the fabrication not compatible with standard microfabrication. The pillars or walls could be integrated by advanced wafer-level packaging techniques, though mechanical stability is a concern. Furthermore, suppressing reflections and stray light is challenging with respect to the collimating sensor type.

Thirdly, the tilted mount sensor type (Figure 1.3c) implements the spacial filter by the placement of the photodetectors on two or more tilted planes. This is typically fabricated on system level with separate photodetectors on a tilted mount. In standard microfabrication, these tilted planes must be created through etching or deposition techniques, with the definition of the photodetectors on sloped planes. Alternatively, advanced wafer-level packaging techniques can be employed to implement this structure. Furthermore, suppressing reflections and stray light is again challenging with respect to



(a) (b) (c)

Figure 1.3: Different sun position sensor types [10], including a) the collimating sensor [11, 12] with a light masking layer above four photodetectors, b) the sun-pointing sensor [13, 14] that relies on shading of four photodetectors and c) the tilted mount sensor [15, 16] that has five differently angled photodetectors.

the collimating sensor type.

Finally, the hybrid sensor type implements the spacial filter by combining the working principles of multiple already mentioned sensor types. It is not illustrated in Figure 1.3, as implementations can be very diverse. From these four sun position sensor types, the collimating sensor is selected as the best match for a implementation by microfabrication, and is therefore the research interest in this work. This type is also dominantly found in commercially available devices.

1.1.2. STATE-OF-THE-ART SUN SENSOR DEVICES

An overview of commercially available sun position sensors from different vendors and academic reports is listed in Table 1.1. The device resolution is sometimes reported but not included to the list, as the spatial resolution is typically not constant over the entire field-of-view. It is therefore a less sensible measure for comparison in this set of devices. Some observations from this list are the limited temperature range, the significant jump in accuracy reported in academic implementations, and the absence of albedo sensitivity information. The temperature range is dictated by the conventional silicon technologies used for the photodetectors and/or readout circuitry. The much higher accuracy in academic literature is likely to be for optimal scenarios, while the commercial devices are officially rated after a variety of stress tests. The information on albedo sensitivity is never reported, though often mentioned to be a limiting factor. This is likely due to the

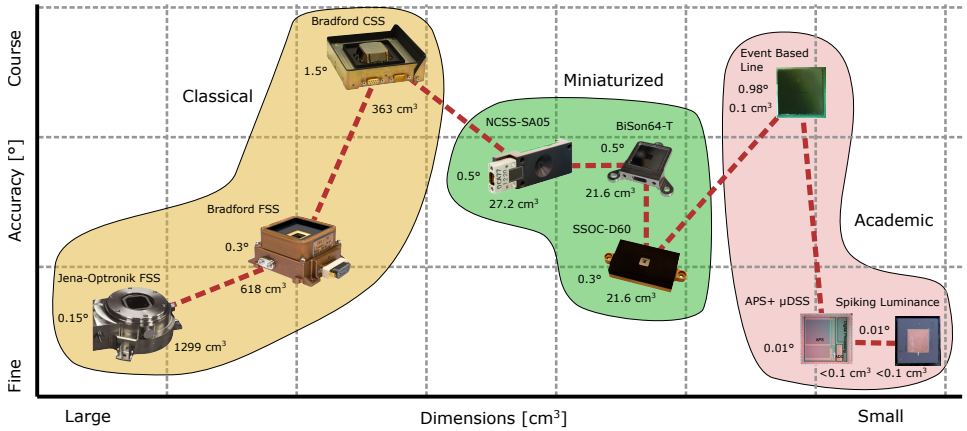


Figure 1.4: Comparison of the listed sun position sensor devices [17–21] in Table 1.1, by considering their size and accuracy. The scales are relative and the values of each device are given in the plot for reference. Three group classifications for device implementations are identified.

lack of an official rating method and generally severe performance degradation.

The best comparison method in order to rank these devices in light of this research project, is to look at their dimensions and albedo rejection. However, as albedo rejection information is lacking, the accuracy is chosen instead. The devices are plotted for these two parameters in Figure 1.4, where a small/fine device is best and a large/course device is worst. Three groups of devices are identified in this way, which are the classical bulky sun sensors, the miniaturized sun sensors and the academic reports. The classical devices tend to decrease in accuracy for shrinking dimensions, which is not the case in the miniaturized devices. The academic reports are on the far end of the miniaturization, but it should be noted that these implementations are not fitted in space grade housing.

With the different rating of academic and commercial devices in mind, the trend towards higher accuracy is achieved by implementation of pixel arrays. A specific deriva-

Table 1.1: Overview of selected device parameters of both commercially available sun sensor devices and academic reports. In some cases the parameter is not determined (ND), or has been derived from graphic figures.

	Field-of-view	Accuracy	Power	Temp. range	Dimensions	Device type	Ref.
Commercially available devices							
BiSon64-ET	116°	0.5° (3σ)	ND	−120–120 °C	49 × 49 × 9 mm	quadrant	[17]
Bradford CSS	180°	1.5° (3σ)	ND	−80–120 °C	110 × 110 × 30 mm	pyramid	[18]
Bradford FSS	128°	0.3° (3σ)	0.25 W	−80–120 °C	108 × 108 × 53 mm	quadrant	[18]
Jena-Optronik FSS	128°	0.15° (3σ)	0.25 W	−80–120 °C	160 × 145 × 56 mm	pixel array	[19]
NCSS-SA05	114°	0.5° (RMS)	0.15 W	−25–70 °C	34 × 40 × 20 mm	PSD	[20]
SSOC-D60	120°	0.3° (3σ)	70 mW	−45–85 °C	60 × 30 × 12 mm	MEMS	[21]
Academic reports							
APS+ µDSS	100°	0.01° (3σ)	21 mW	−40–80 °C	5 × 5 mm[a]	pixel array	[22]
Spiking Luminance	146°	0.01° (3σ)	52 mW	ND	4.1 × 3.3 mm[a]	pixel array	[23]
Event Based Line	144°	0.98° (3σ)	6.3 µW	ND	9.5 × 9.5 × 1 mm	pixel lines	[24]

[a] Chip dimensions.

tive from the sun position sensor is the star tracker device, which typically can also be used as a sun position sensor. A successful example is FAINTSTAR [25], which consists of a large array of photodetectors and integrated readout circuitry.

1.1.3. CHALLENGES FOR THE NEXT GENERATION

The next generation of sun position sensors must follow the requirements set by the changing ecosystem of spacecraft. As was stated in the abstract of this chapter, the two main challenges to face for the future are 1) signal distortion by reflection from the Earth and 2) a scalable integration of the sensor optics. Ideally, next generation devices are albedo insensitive and monolithically integrated, both these terms are addressed in the following paragraphs.

The term albedo is referred to as the light reflected by planetary bodies, particularly the albedo of the Earth as most satellites are in orbit of the Earth. All state-of-the-art sun position sensors suffer from albedo sensitivity to some degree, because of the widespread adaptation of silicon based photodetectors. As a result, the outstanding performance that many of these devices report, comes with the footnote that this concerns situations without albedo influence. The degradation of the accuracy performance can be tens of degrees in sunset or sunrise conditions, severely limiting the use of these instruments in those situations. Other applications of albedo insensitive photodetectors, also known as visible blind photodetectors, can be found in industrial environments for flame detection [26].

Ranking the ability for albedo rejection, we find the quadrant and PSD types at the

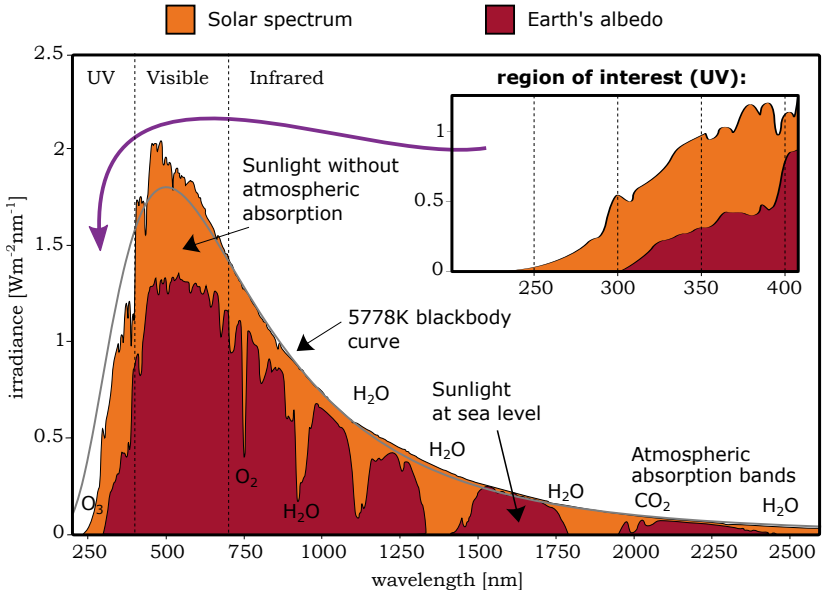
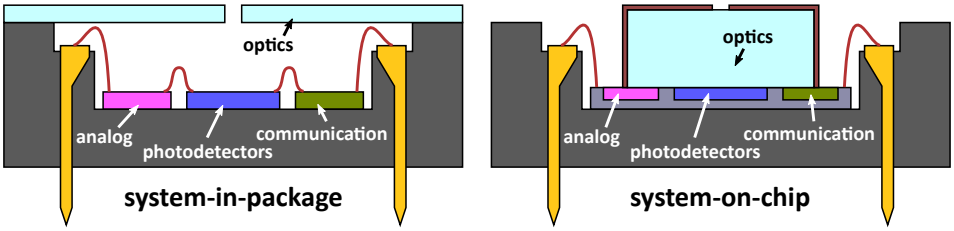


Figure 1.5: Solar spectrum above (orange) and below (red) the Earth's atmosphere [27–29]. The absorption bands are denoted with the responsible molecules in the atmosphere (adapted from Wikimedia [30]). The inset shows the spectral range of interest in UV for this research project.



(a) (b)

Figure 1.6: Schematic illustrations of the two main integration trends in microfabrication, with cross-sections of the a) system-in-package and b) system-on-chip applied for the sun position sensor. The highlighted modules are an indication of required blocks.

bottom, as these architectures have no possibility towards albedo rejection. The use of pixel arrays, also known as digital sun sensors[3], allows for albedo rejection algorithms by identification of the sun and Earth horizon separately. Such implementations still deal with a sun sensor that is highly affected by the albedo, but attempt to filter out the albedo by assuming its shape. Going beyond the conventional devices, wide bandgap material is inherently insensitive to visible light, which means great ability of albedo rejection without any additional algorithm efforts. Another advantage of migration to wide bandgap electronics is the general increase of radiation tolerance, which brings reduction of shielding requirements and thus device mass reduction. The solar and albedo spectra in Figure 1.5 show the broad overlap between the two, but with some openings where the albedo is absent. Employment of spectral filters is proposed for the infrared band [31] and wide bandgap materials are proposed for the ultraviolet band [32].

Monolithic integration is the ultimate form of integration in modern technology in terms of miniaturization and overlay accuracy of each functional layer. It has been the preferred route in microfabrication for decades, until the concept of heterogeneous integration stepped in to enable cost reduction and integration of various functions into a single microsystem. The system engineer needs to identify which of the two approaches fits the application best, as typically both concepts could be applied to a successful end. The sun position sensor is schematically illustrated for the heterogeneous, or system-in-package (SiP), and monolithic, or system-on-chip (SoC), approaches in Figure 1.6. It should be noted that a general form is illustrated, with very diverse alternatives possible for each approach.

At present, the SiP approach is mostly applied for the sun position sensor and comes with the challenge of aligning the optics in the package with respect to the photodetectors. It furthermore requires careful radiometry considerations to avoid unwanted optical interference such as internal reflections. When instead using the SoC approach, the alignment of the optics can be performed by standard microfabrication tools to reach excellent overlay. As such, no cumbersome device verification or calibration is required. Furthermore, the optics internals are greatly simplified and completely microfabricated,

[3] Digital sun position sensors typically encompass a pixel array topology, though a clear definition for the term is lacking in both industry and academia. One can also consider the device outputs (analog versus digital) or availability (time continuous versus discrete).

containing the radiometry considerations to just the on-chip optics. Moreover, the complete wafer-level fabrication allows further miniaturization of the device, which comes with further cost reduction. Though one might want to move all the control and readout circuitry to an efficient silicon technology with small feature size, this does demand proper shielding against cosmic radiation. Instead, full monolithic integration of the electronics in a wide bandgap material would be on a larger chip area, but in a material that is inherently less prone to cosmic radiation and thus needs less shielding.

1.1.4. SUN SENSOR FUNCTIONAL SPECIFICATION

From the reported sun position sensor devices in Table 1.1, a list of specifications for this project is derived. The main targets for this research are the albedo sensitivity and miniaturization, so the other parameters should be similar in order to develop a superior device. The target field-of-view of 120°, is considered an industry standard to aim for. For a proof-of-principle implementation, half of this target is considered adequate. Moving to larger field-of-views is of interest, as this is a challenge faced in industry, though it should be noted that many aspects play a role for successfully expanding the field-of-view [33]. The accuracy of the commercially available devices should be matched at 0.5°. This will be challenging, given the still immature technology level of silicon carbide technologies in comparison to conventional silicon technologies, and is therefore considered the maximum. The sensor architecture should be scalable, so that future implementations in silicon carbide can reach higher accuracy without redesign of the topology.

The power and temperature ranges are not the main goals of this research work, but wide bandgap material is often praised for its ability of higher temperature operation. As such, the aim is to extend the operation temperature to higher levels, which is not covered by any available device on the market today. The power consumption should be comparable or better than the devices on the market, but will highly depend on the used technology. The focus of the sun position sensor will be on chip level, excluding specialized packaging for space application. As such, the dimensions are to be considered for the single system-on-chip. As the feature size of wide bandgap material technology is at present larger than conventional silicon capabilities, the target chip area is similar to those of the devices reported in literature.

The application in the harsh environment of outer space brings more challenges, such as radiation and vibrations during launch. Two major problems in electronics

Table 1.2: Listing of functional specifications for the sun sensor implementation in silicon carbide with integrated optics in this research work. A target, minimum and maximum value is given for each parameter.

	Minimum	Target	Maximum
Field-of-view	60°	120°	130°
Accuracy	3.0°	1.5°	0.5°
Power	0.1 W	10 mW	1 mW
Temperature range	20–100 °C	0–150 °C	0–300 °C
Dimensions	50 × 50 × 50 mm	30 × 30 × 10 mm	10 × 10 × 2 mm

caused by the high-energy radiation are single event upsets (SEUs) and CMOS latch-up. SEUs cause bit-flips in the memory, which changes commands that can have disastrous effects. CMOS latch-up causes high currents through devices, which usually destroys the devices permanently. Both problems can be addressed by addition of protection circuits [34, 35]. Vibration during launch and the journey into space [36] demand high mechanical reliability and stability. However, both these aspects are considered out of scope for this research work.

1.2. WIDE BANDGAP MATERIALS

To tackle the challenge of albedo sensitivity that modern sun position sensors face, it is proposed to develop technology based on wide bandgap semiconductors. The higher bandgap energy translates to a selective spectral sensitivity in the UV range, which allows for inherent albedo rejection of the device. Other benefits to application in space that wide bandgap electronics offer, are operation at higher temperature and higher radiation tolerance. For that reason, their use for harsh environment microsystems has been proposed in literature [37, 38], though this brings new challenges such as reliable packaging in these environments [39]. A selection of wide-bandgap materials and their properties is listed in Table 1.3, taken from the complete overview listed by Monroy *et al.* [40]. This section illustrates the wide bandgap landscape and their use for UV photodetection, before diving into specifics on silicon carbide.

1.2.1. THE RACE BETWEEN GALIUM NITRIDE AND SILICON CARBIDE

Gallium nitride and silicon carbide are often mentioned in the same sentence when introductions to wide bandgap materials are given [44, 45]. It is these two materials that are extensively researched in both academia and industry, with the most mature technologies available, that already introduced discrete components in both materials. Large companies have entered the scene the past years, such as chip manufacturers Infineon and STMicroelectronics. The main economic driving force is the rapidly increasing electric vehicle (EV) market, focusing on the automotive chips for power electronics, with companies like Tesla, Hyundai, BYD, Nio and General Motors. The benefits of silicon carbide and gallium nitride here, is that they offer a high breakdown voltage, high

Table 1.3: Overview of wide-bandgap materials silicon (Si), 4H polytype of silicon carbide (4H-SiC), 6H polytype of silicon carbide (4H-SiC), zinc oxide (ZnO), galium nitride (GaN), aluminum nitride (AlN) and diamond [40–43]. The 4H-SiC and 6H-SiC polytypes are discussed further in Section 1.2.3.

	Si	4H-SiC	6H-SiC	ZnO	GaN	AlN	Diamond
Bandgap [eV]	1.12	3.2	2.86	3.35	3.39	6.2	5.5
Excitation wavelength [nm]	1170	387	434	370	366	200	225
Melting point [°C]	1410	2557	2557	1969	2518	2752	3500
Electron mobility [$cm^2 V^{-1} s^{-1}$]	1400	950	400	200[a]	1000	135	2200
Hole mobility [$cm^2 V^{-1} s^{-1}$]	600	120	75	-[a]	30	14	1600
Electron/hole mobility ratio [-]	2.33	7.92	5.33	-[a]	33.3	9.64	1.38
Thermal conductivity [$W cm^{-1} K^{-1}$]	1.5	4.9	4.9	0.54	1.3	3.19	20

[a] Synthesis of single-crystal samples remains challenging.

switching speed and small form factor. This allows for reduction of the required components on a system level, thus saving on volume and weight, that reduces the system costs even though the discrete components are more expensive. To reduce costs further, foundries are migrating their technologies to 200 mm substrates and beyond. With both materials tackling challenges in a similar domain, it seems to be a development race where the prize is a multi-billion dollar market. At present, galium nitride is ahead in this race, where it is seen in increasingly more products.

However, the integration requirements are currently not demanding with most of the focus on single power devices. The galium nitride technology is based on the high electron mobility transistor (HEMT), which is a lateral device that is normally on. The lateral nature translates to large area requirements and the normally-on operation requires an additional (silicon) gate driver to be integrated in the package. This is a cost-effective and reliable approach for discrete power components, but is not a feasible route for integrated sensor and readout systems as this would translate to large area and power consumption using the HEMT. Still, research performed by Miller at the Stanford University [32, 41] also recognized the potential of wide-bandgap materials for sun sensing applications and implemented a course collimating sun position sensor in galium nitride. The work focused on the incorporation of graphene[4], due to its excellent optical properties, as well as reliability testing in high-temperature and radiation environments. No attempts were made to integrate on-chip circuitry or develop a scalable fabrication of the optics.

1.2.2. UV PHOTODETECTION

The field of ultraviolet (UV) photodetection has gained increased attention for industrial, biological and environmental applications [46]. Conventional silicon photodetectors rely on the broad spectral sensitivity range of the material, but there are approaches for selective UV sensing. For example, implementations based on silicon-on-insulator [47] or ultrashallow junctions [48] exist, which exploit the thin film that transmits light with longer wavelengths. Alternatively, UV selectivity can be achieved by elegant readout approaches, such as the use of a differential method [49, 50], though this comes at the cost of area increase. By instead using wide-bandgap materials as the substrate, the sensitive spectral bandwidth of the semiconductor is reduced to shorter wavelengths. This furthermore comes with the potential of applications in deeper UV or in higher temperature environments. The excitation wavelength relates to the bandgap energy through

$$E = \frac{hc}{\lambda,} \tag{1.1}$$

where h is Planck's constant, c the speed of light and λ the photon wavelength. Considering the albedo insensitivity requirement, complete albedo absence is at <300 nm and would correspond to a bandgap energy of >4.13 eV. This can only be fulfilled by AlN or diamond, but these are sensitive only at even smaller wavelengths. The technologies in these materials are at a immature level and would need to deal with very low light

[4] Graphene is a single layer sheet of sp^2 bonded carbon atoms, first isolated in 2004 by Geim and Novoselov using scotch-tape exfoliation from a graphite crystal [51, 52].

intensities. So instead the spectral range is made larger, by including GaN, ZnO and 4H-SiC, which means that part of the albedo is captured at the upper limit of the spectral responsivity of photodetectors in these materials. The many photodetector device types [46] are listed and discussed in the implementation stage in Chapter 4.

1.2.3. SILICON CARBIDE STATE-OF-THE-ART

For integrated circuit technology, it is beneficial to have a high electron and hole mobility for fast devices and a mobility ratio close to 1 for matching of complementary devices. There are significant differences in the mobility values in Table 1.3, where the best candidate by far regarding mobility is diamond, followed by silicon carbide. Silicon carbide (SiC) is a wide bandgap material that has been extensively researched over the past decades, especially for the application in power electronics [53, 54]. Together with galium nitride (GaN), the future market of wide bandgap materials in power electronics is expected to be booming [55]. This foresight paves the way for application in other fields as well [56–59], as the substrate and technology costs are expected to decrease, the technology to mature and become more accessible. Several silicon carbide sensors were previously reported in our research group, such as pressure sensors based on deposited poly-SiC [60, 61] and a transparent heater [62]. However, a key aspect that is missing is the on-chip integrated readout to make the sensors fully compatible with harsh environment sensing.

Silicon carbide is a compound semiconductor with silicon dioxide (SiO_2) as its native oxide. It is composed by 50 % silicon and 50 % carbon atoms in its crystal structure [63]. The fabrication process of SiC wafers is very similar to that of Si wafers, as a cylindrically shaped ingot is formed and then wire sliced to form wafers. One immediate visual difference between Si and SiC wafers is that the latter is transparent. Silicon carbide is the best known example of polytypism. This is a phenomenon in which a material can take different crystal structures that vary in one dimension, without changes in the chemical composition. This variation in crystal structure occurs in the stacking sequence of identical layers. Since both Si and C atoms are tetravalent elements, each Si must have four C atom neighbors and vice versa [63]. Figure 1.7a illustrates the hexagonal close-packed SiC system that has three possible sites, marked as 'A', 'B' and 'C'. Two stacked layers

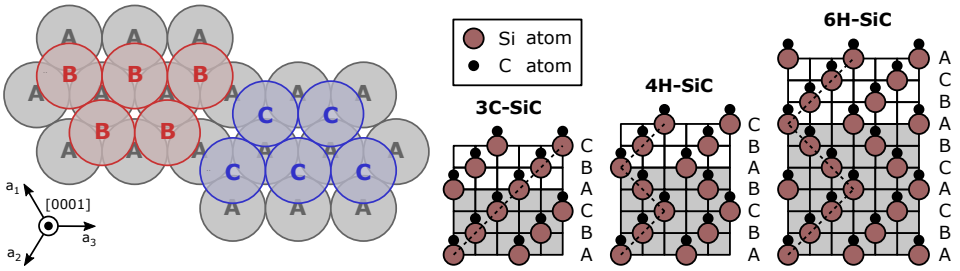


Figure 1.7: Schematic illustration of SiC bilayer stacking (adapted from Kimoto and Cooper [63]). The top view a) of the system that has three possible sites, marked by 'A', 'B' and 'C'. The stacking sequence b) of polytpes 3C-SiC, 4H-SiC and 6H-SiC is indicated.

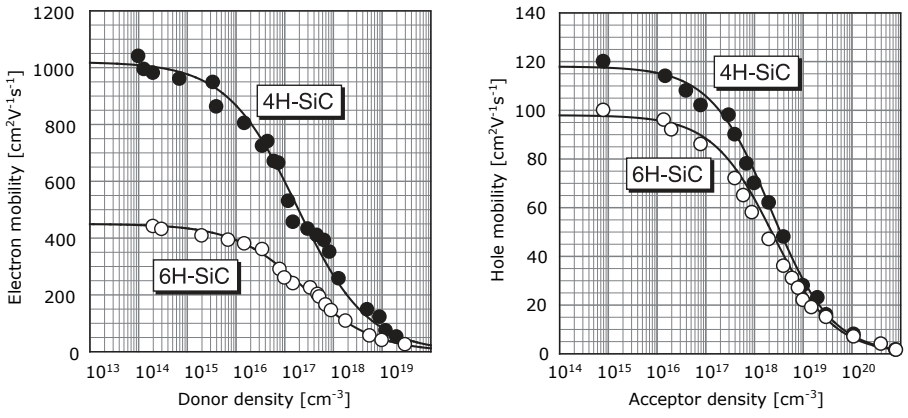


Figure 1.8: Carrier mobilities in 4H-SiC and 6H-SiC for different dopant densities. The a) electron and b) hole mobility are both higher in 4H-SiC. Courtesy of Kimoto and Cooper [63].

must occupy different sites, so the stacked layer on top of 'A' must be either 'B' or 'C'. In principle, a tremendous amount of stacking variations exist, but for most materials only a single stacking sequence is stable. This is where SiC is different, as it has over 200 polytypes. However, most of them are not stable at elevated temperature, which is typically required in the ingot growth process. To represent these polytypes, different notations exist such as Ramsdell's, Zhdanov's, and Jagodzinski's notations. At present, Ramsdell's notation is most widely used and is therefore considered in this work. In Ramsdell's notation, the polytypes are identified by the number of SiC bilayers in the unit cell and the crystal structure (C for cubic, H for hexagonal, and R for rhombohedral). The three most popular SiC polytypes are 3C-SiC, 4H-SiC and 6H-SiC and the stacked bilayer is illustrated in Figure 1.7b. Yet another classification is that 3C-SiC is often referred to as β-SiC and the other polytypes as α-SiC.

The electron and hole mobilities of the 4H-SiC and 6H-SiC polytypes are provided in Figure 1.8a and Figure 1.8b respectively. It is evident that the carrier mobilities are higher in 4H-SiC, although the ratio is closer to 1 for 6H-SiC (see also Table 1.3). In terms of low-voltage device performance, a higher mobility is typically considered beneficial as it increases device output current and speed. In terms of complementary device technology, a carrier mobility ratio closer to 1 allows more symmetrical behavior, which is beneficial for circuit design.

1.2.4. CHALLENGES IN SILICON CARBIDE FABRICATION TECHNOLOGY

The primary challenge faced in the fabrication of silicon carbide devices is the ability to form ohmic contacts, which is a challenging task for wide bandgap devices in general. An ohmic contact is a metal-semiconductor junction that obeys Ohm's Law and is a part of the more general group of Schottky contacts [64–67]. Its resistance is normalized over the contact area, typically defined as $\Omega\,\mathrm{cm}^2$. The energy band diagrams before and after physical contact between a metal and semiconductor are illustrated in Figure 1.9.

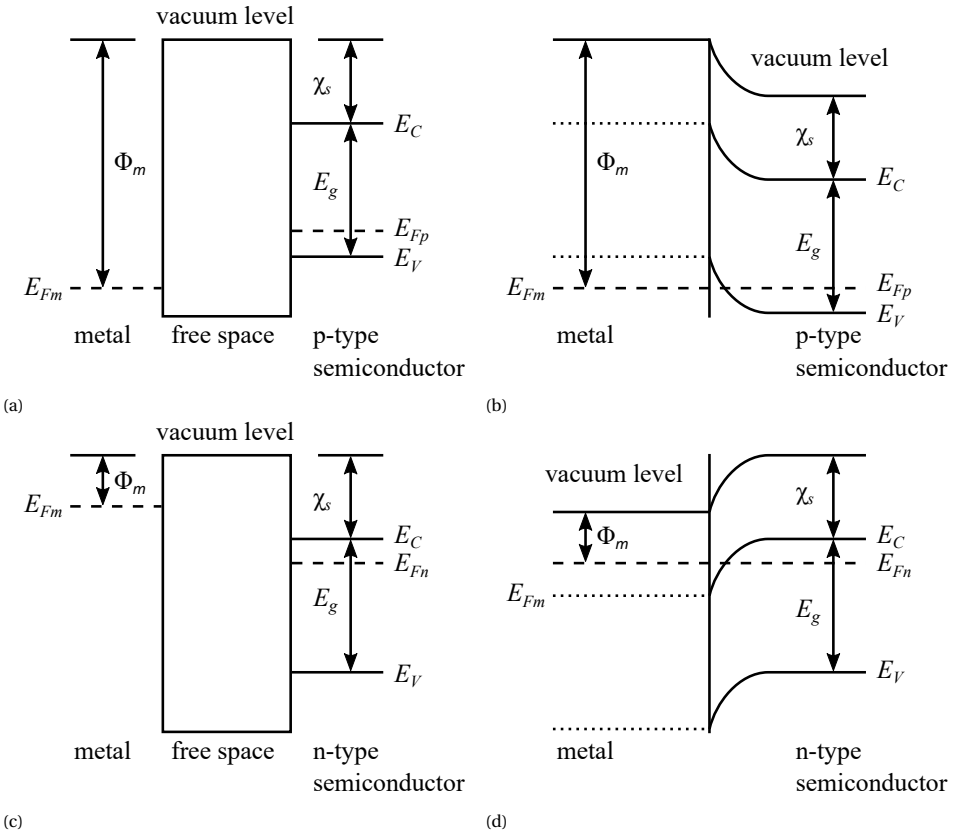


Figure 1.9: Energy band diagrams of a p-type semiconductor a) before and b) after physcial contact with a metal and an n-type semiconductor c) before and d) after physical contact with a metal. The metal work function Φ_m, Fermi levels E_F, semiconductor bandgap E_g, conduction band E_C, valence band E_V and electron affinity χ_s are marked [64–67].

The metal work function Φ_m is the energy difference between the vacuum level and the Fermi level E_{Fm}. The semiconductor on the other hand, has a bandgap E_g that is the difference between the conduction band E_C and valence band E_V. The electron affinity χ_s is the energy difference between the conduction band and vacuum level. Finally, the Fermi level is closer to the conduction band for an n-type and closer to the valence band for a p-type semiconductor, marked by E_{Fn} and E_{Fp} respectively.

In simplified systems, the Fermi levels of the metal and semiconductor are pinned to the same level and the Schottky-Mott rule[5] can be applied, which predicts the Schottky barrier height Φ_B. To form an ohmic contact to a p-type or n-type semiconductor, the E_V level must be higher than E_{Fp} or the E_C level must be lower than E_{Fn} at the interface, respectively. Therefore, metals with a high and low work function generally

[5]The Schottky–Mott rule predicts the Schottky barrier height based on the difference between the vacuum work function of the metal and the vacuum electron affinity of the semiconductor.

Table 1.4: Selection of metallization techniques for ohmic contacting to n-type or p-type α-SiC from the review by Crofton *et al.* [68]. The annealing temperature is simplified, by not reporting the time schemes.

Metallization	Deposition method	Annealing temperature [°C]	Contact resistance [$\Omega\,cm^2$]
Ohmic contacts to n-type α-SiC			
Mo	sputtering	none	1×10^{-4}
Ni	e-beam evaporation	1000	5×10^{-6}
Ta	sputtering	none	1×10^{-4}
Ti	thermal evaporation	none	1×10^{-2}
TiW	sputtering	750	8×10^{-4}
Ti-Al	thermal evaporation	1000	1×10^{-3}
W	thermal evaporation	1200	5×10^{-3}
Ohmic contacts to p-type α-SiC			
Mo	sputtering	none	2×10^{-4}
Ta	sputtering	none	7×10^{-4}
Ti	thermal evaporation	none	3×10^{-2}
Ti-Al	sputtering	1000	5×10^{-4}
Al-Ti-Al	thermal evaporation	800	2×10^{-4}

make good ohmic contacts to a p-type and n-type semiconductor respectively. It boils down to achieving a current flow through the barrier with as low energy as possible, for which there are two approaches. Firstly, lowering of the barrier height itself to enable carriers to overcome it due to the thermal energy of the system. This can be done by implementing an intermediate semiconductor layer, that is typically a complicated metallization stack with thermal processing. Secondly, thinning down the barrier distance, allowing quantum mechanical tunneling through the barrier. This is achieved by highly doping the semiconductor contact, which thins the depletion region in the metal-semiconductor junction. Note that the barrier height remains the same for low or highly doped contact regions [67, 68]. A selection of metallization techniques for ohmic contacting is provided in Table 1.4. Often a high temperature anneal is necessary to form silicides in order to obtain a low contact resistance.

A secondary challenge for silicon carbide is the limited capability to etch the material. The only feasible option is by lengthy dry etching procedures, where an electroplated nickel layer is generally used as a hard mask. Still, high quality cavities are demonstrated [69–71] with limited micromasking and aspect ratios of 19-25, reaching etch rates of 0.3–2.0 $\mu m\,min^{-1}$ for 4H-SiC. This renders bulk micromachining technology for microelectromechanical systems (MEMS) unfeasible, but does allow for some surface micromachining and shallow trenches isolation (STI), or mesa etching, for integrated devices. More secondary challenges are the implantation and activation of dopants, which requires higher temperature than is used in conventional silicon fabrication, and inferior thermal oxide dielectric quality with trapped charge caused by inevitable defects at the SiO_2-SiC interface.

1

1.3. WAFER-LEVEL PACKAGING TECHNOLOGY

The implementation of a sun position sensor that is harsh environment compatible, means that its optics, sensors and readout circuitry are integrated in a single device. This mitigates the need for a controlled environment and a long shielded cable (as illustrated in Figure 1.10). To enable complete wafer-scale fabrication, the 3D optics of the device must be implemented on wafer level as well. The main challenge to take into account is the typical milimeter scale for the optical window thickness. This optical window furthermore needs to be transparent in the targeted UV range, and its light mask pattern must be aligned to the photodetectors.

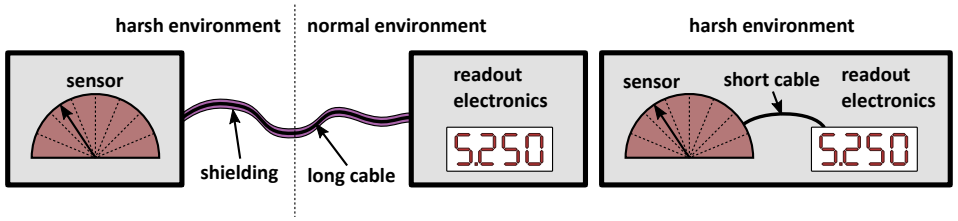
1.3.1. WAFER-TO-WAFER VERSUS DIE-TO-WAFER

Wafer scale deposition of uniform layers is common place in the world of microfabrication. However, transparent compositions like silicon oxide (SiO_2), silicon nitride (Si_3N_4) or aluminum oxide (Al_2O_3) can not be used to implement the required thick milimeter scale layer for the optics. It is therefore required to resort to the joining of a transparent substrate to the device substrate. One can propose various different processes for joining the device chip and the optics chip, which are more generally classified in the three options discussed below.

Firstly, the integrated circuit device wafer is joined with the optics wafer, e.g. wafer-to-wafer bonding (see Figure 1.11a), and the final result is schematically depicted in Figure 1.11d. The advantage of this technique is that there is only two substrates to join, requiring only a single alignment procedure. The disadvantages of this technique is the fact that a dicing blade would cut through both substrates at the same time, which may cause damage or detachment due to the mechanical force, and that the complete front side of the device chip is inaccessible.

Secondly, the optics wafer is first diced before joining the substrates, e.g. die-to-wafer bonding (see Figure 1.11b), and the final result is schematically depicted in Figure 1.11e. The advantages are that the final dicing of the wafer is only in the device wafer and that a portion of the device front side is accessible. The disadvantage is the alignment and placement of each individual optics chip.

Lastly, the device wafer is first diced before joining the substrates, a second die-to-wafer bonding option (see Figure 1.11c), and the final result is schematically depicted in Figure 1.11f. The advantage is again that the final dicing is only through one substrate,



(a) (b)

Figure 1.10: Schematic overview of sensing in a harsh environment with a) the sensor and readout in separate environments and b) the complete device in harsh environment.

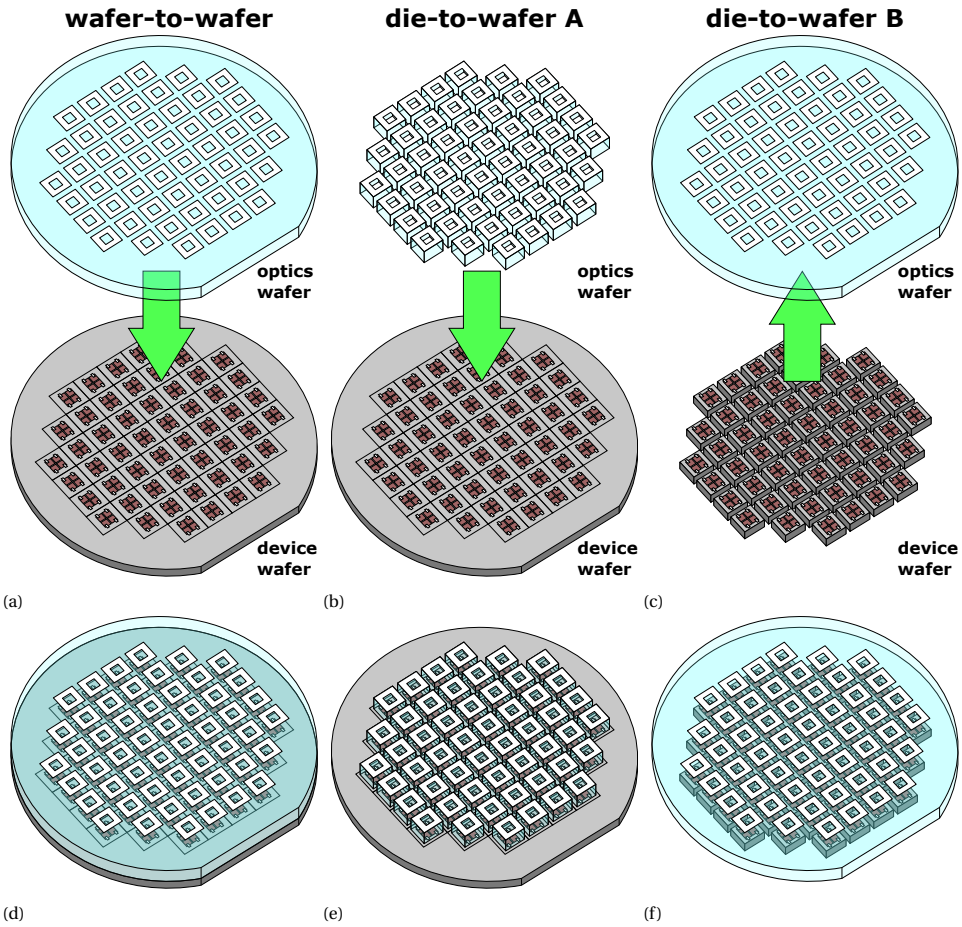


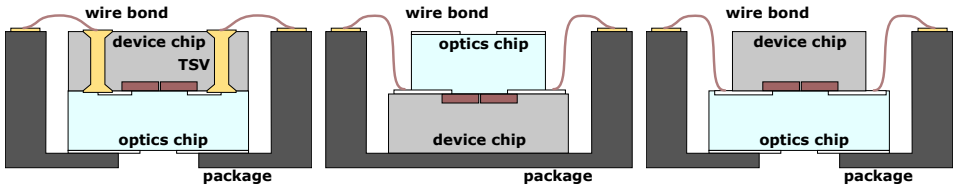
Figure 1.11: Overview of three different options for joining the device and optics substrates, including a) wafer-to-wafer, b) die-to-wafer method A, c) die-to-wafer method B and d-f) the final joined substrates.

in this case the optics wafer. The disadvantages are that the device chip front side is not accessible and that each device chip must be aligned and placed individually.

1.3.2. INTERCONNECT OPTIONS

Joining the device chip and the optics together is one thing, but to package the device with electrical interfacing is another. Each of the three options for joining the substrates comes with its own packaging challenges. The variety of packages and electrical contacting technologies is huge, so the examples below consider generic packages and wire bonding technology.

From the wafer-to-wafer option, the final device consists of a wafer stack of identical chip area. This means that wire bonding must be done on the device chip backside or the optics chip. To provide access to the electrical signals, through-substrate-vias (TSVs)



(a) (b) (c)

Figure 1.12: Three interconnect examples for interfacing with the package, corresponding to the options a) wafer-to-wafer, b) die-to-wafer A and c) die-to-wafer B from Figure 1.11.

could be employed. This is however a another technical challenge, especially considering the non-conventional wide bandgap substrates. An example of a possible implementation is illustrated in Figure 1.12a.

The die-to-wafer option A in turn does allow for direct access to the device chip front-side for wire bonding, as depicted in Figure 1.12b. This requires the chip to be placed with its optics up, which demands for a suitable lid or encapsulation (not illustrated). Finally, the die-to-wafer option B would omit the need for TSVs and place the device with its optics down, as depicted in Figure 1.12c. However, this then calls for an interconnect technology between the device and optics chip.

1.3.3. SELECTIVE ADDITIVE PROCESSING

Instead of relying on the joining of a transparent substrate, novel additive technologies can be considered. A basic approach is to spin coat a polymer on top of the wafer, potentially by implementing multiple layers. This polymer layer is ideally patterned directly by lithography, or otherwise through DRIE etching. Unfortunately, the polymers that are typically used in this way (SU-8, polyimide, PDMS) do not have great optical transmission in the UV range. To this end, other polymers with better optical transmission can be considered, such as acrylates, but it remains challenging to obtain layers of acrylate that are thick enough by spin coating. Alternatively, the polymer can be selectively deposited by using advanced stereolithography apparatus (SLA) 3D printing manufacturing techniques or hot embossing.

The space environment poses more challenges for polymers related to outgassing[6] and UV degradation effects. Not to mention the limited temperature range in which polymers can typically be applied reliably. Therefore a technology based on polymer optics poses many challenges related to the reliability of the device.

1.4. MOTIVATION AND OUTLINE OF THIS THESIS

A sun position sensor is a device commonly used in spaceflight to determine the attitude of the spacecraft with respect to the sun as a reference. This work aims to create a proof-of-principle device to verify the feasibility of a microfabricated sun position sensor in silicon carbide that solves the challenges faced by the state-of-the-art. Taking the mentioned parameters in mind and considering technology readiness, silicon carbide

[6] Outgassing is the release of a gas that was dissolved, trapped, frozen, or absorbed in some material.

is the most suited material for the next generation of albedo insensitive sun position sensor devices. It is a material that attracted extensive research in the power electronics industry. As a result, the substrate and device technologies have improved massively, enabling reliable and wafer-scale fabrication of integrated circuits. Advanced back-end-of-line and packaging techniques are employed for integration of the 3D optics. The envisioned end result is schematically illustrated in Figure 1.13.

The relevance of this research is that it will greatly reduce albedo sensitivity as well as increase the miniaturization of sun position sensors. This enables the high performance of state-of-the-art in cases where light reflected from the Earth is in the sensor field-of-view, as well as cost reduction by a scalable fabrication technology. Relying on the great potential of wide bandgap semiconductors, the envisioned sensor allows for reduced mission costs, longer missions, further missions and missions into harsher environments. Moreover, the work contributes to the fields of electronics for harsh environments and novel packaging techniques for imaging sensors. In order to pursuit and assess the new sun position sensor technology, several research questions and challenges are formulated below.

1. **Question**: *"What sun position sensor architecture is best suited for the envisioned proof-of-principle and how can this be determined?"*
   Challenges: "Research different existing and non-existing sun position sensor architectures and evaluate them for use in this project. Build predictive models to qualitatively compare the different architectures and/or fabricate different architecture designs to compare their performance."

2. **Question**: *"How can the sun position sensor devices be fabricated in silicon carbide and where can this be performed?"*
   Challenges: "Evaluate the possibilities for the sun position sensor fabrication and take this into account in the design. Establish suitable collaborations to perform parts of the fabrication that cannot be done at EKL. Identify missing modules or tools and find access to them or investigate workarounds."

3. **Question**: *"How to implement the wafer-level integration of the aligned sensor 3D optics with the on-chip photodetectors?"*
   Challenges: "Investigate possibilities for monolithic integration of the UV photodetectors with readout circuitry in silicon carbide. Develop methods to attach and pattern the 3D optics by wafer-level packaging."

4. **Question**: *"How reliable is the proof-of-principle in the current technology and what is the impact of the albedo and temperature?"*
   Challenges: "Extensive measurements are required to estimate the impact of the albedo and the reliability with respect to temperature."

To start, Chapter 2 dives into sun position sensor architecture and design in order to answer the first question and give direction for the second question. This is continued in Chapter 3, which describes a scalable technology for integrated circuitry in silicon carbide, and compares it to the comparable in-house silicon technology. This is basis for the development of an opto-electronic platform in Chapter 4, which is again

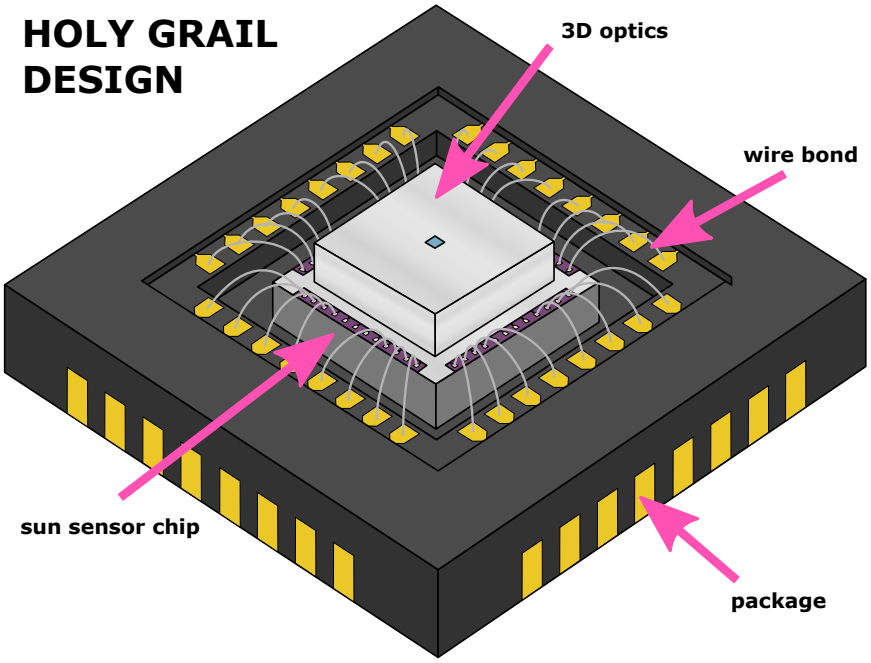


Figure 1.13: Schematic illustration of the envisioned maximum outcome of the project (holy grail design). It is a SoC that has monolithic integration of photodetectors with readout electronics in a silicon carbide chip, and the 3D optics aligned on top.

also implemented in silicon for comparison, and ultimately answers question two. The 3D optics integration is tackled in Chapter 5 to answer question three, and finalizes the sun position sensor device for characterization. All chapters contain measurements and characterization to investigate the reliability of the device, answering the final research question. Finally, this thesis is concluded in Chapter 6 with a summary of the achievements and remarks for the future. Flowcharts, lists of acronyms and abbreviations, materials and more can be found in the appendices.

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2

Sun Position Sensor Architecture and Design

You've got to be very careful if you don't know where you are going, because you might not get there.

Yogi Berra

The sun position sensor is an angle sensitive optical light source, that is ideally only sensitive to the direction towards the sun. Though the concept of an optical sensor that is angle sensitive is seemingly simple, it demands thorough analysis to predict performance and ease the geometry design process. As such this chapter aims to qualitatively describe the leading parameters, sources for errors and any calibration efforts for three different architectures. This includes the widely employed quadrant sun position sensor, pixel array based sun position sensor and a novel approach.

Parts of this chapter have been published in 2021 IEEE 34th International Conference on Micro Electro Mechanical Systems (MEMS) (2021) [1], 2022 IEEE 35th International Conference on Micro Electro Mechanical Systems (MEMS) (2022) [2] and IEEE Sensors Letters (2022) [3].

FROM the different types available, the collimating sun position sensor type is considered for implementation in this work due to its widespread adaptation in the state-of-the-art and its compatibility with microfabrication technology (see also Section 1.1.1). To classify devices of the collimating sun position sensor type, there are two more independent classifications that are typically considered and mentioned in state-of-the-art, but are unfortunately not consistently defined in industry or academic publications. These classifications are between course/fine and analog/digital devices.

Firstly, consider the difference between course and fine devices. This classification directly follows from the sensor accuracy, with course devices being less accurate than fine devices in resolving the angular information. However, there seems to be no clearly documented accuracy that divides these two. Therefore, this work considers devices with an accuracy of <0.5° fine sun sensors and the rest course sun sensors, which is based on typical state-of-the-art classifications.

Secondly, the different analog and digital modes one could use to distinguish implementations. One way is to look at the device output signals, if these are analog values then the device classifies as analog and vice versa for digital. Another way is to look at the availability of the device output signals, if these are time-continuous the device classifies as analog and if these are made available on clock pulses the devices classifies as digital. A third way is to look at the device readout scheme, if the readout algorithm directly compares individual photodector magnitudes it classifies as analog and if it incorporates other parameters of the device (such as photodetector coordinates) it classifies as digital. Examples of digital sun position sensors can be found both in hardware and software, with approaches such as physical analyzer masks [4] or centroid algorithms [5]. This third definition is adopted in this work as it is deemed more relevant to classify devices on their readout algorithm rather than purely on their output signals.

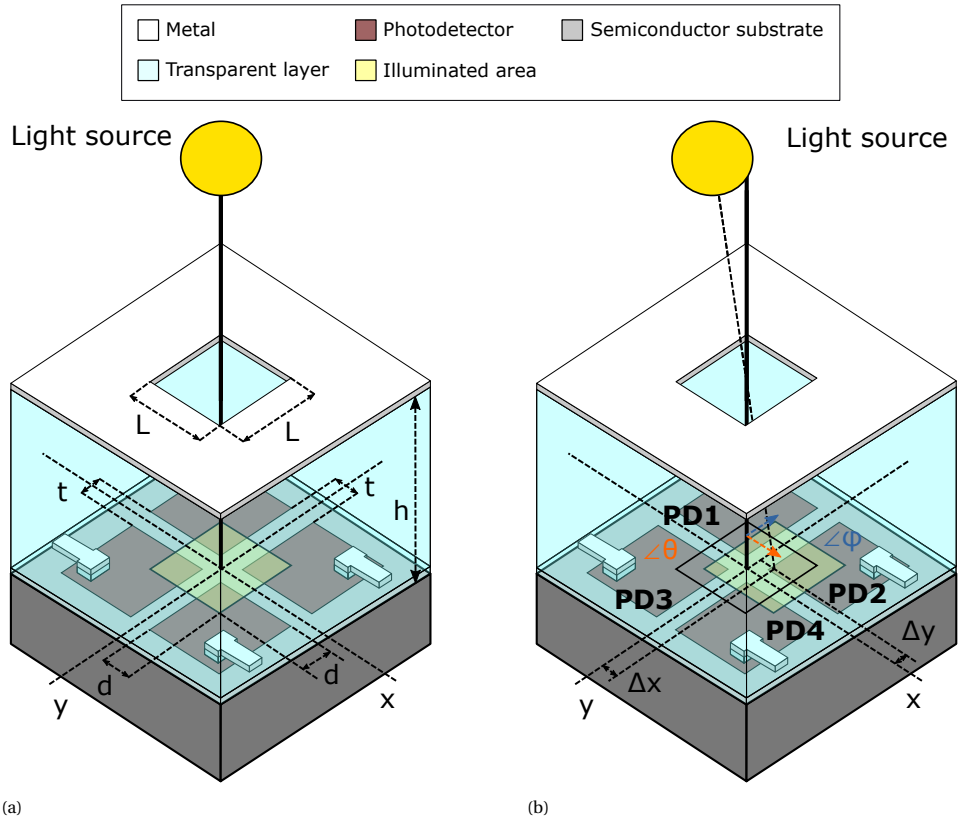
In this chapter, two collimating sun position sensor architectures are considered. The first is the four quadrant sun position sensor, which is a widely applied architecture in commercial devices. The second is the pixel array sun position sensor, which relies on a centroid algorithm to find the angular information. As a novelty, a completely new sun sensing type is then explored using stacked diffraction gratings. The chapter is concluded by considering the radiometry, which is leading for later electrical design.

2.1. QUADRANT SUN POSITION SENSOR

An often employed architecture of the collimating sun position sensor type is the quadrant sun position sensor. The schematic overview of this architecture is given in Figure 2.1 and consists of four photodetectors on the substrate and a light mask that casts a light spot on the detectors. The distance between the detectors and light mask is implemented by a highly transparent optical window added during device packaging.

2.1.1. LEADING DESIGN PARAMETERS

The angles $\angle\theta$ and $\angle\varphi$ in the schematic overview given in Figure 2.1b provide the cartesian direction vector to the light source (see Figure A.1 for the polar counterpart), which are extracted from the detectors response. In the plane of the four photodetectors, these angles correspond to a lateral displacement of the light spot in x and y direction through



(a) (b)

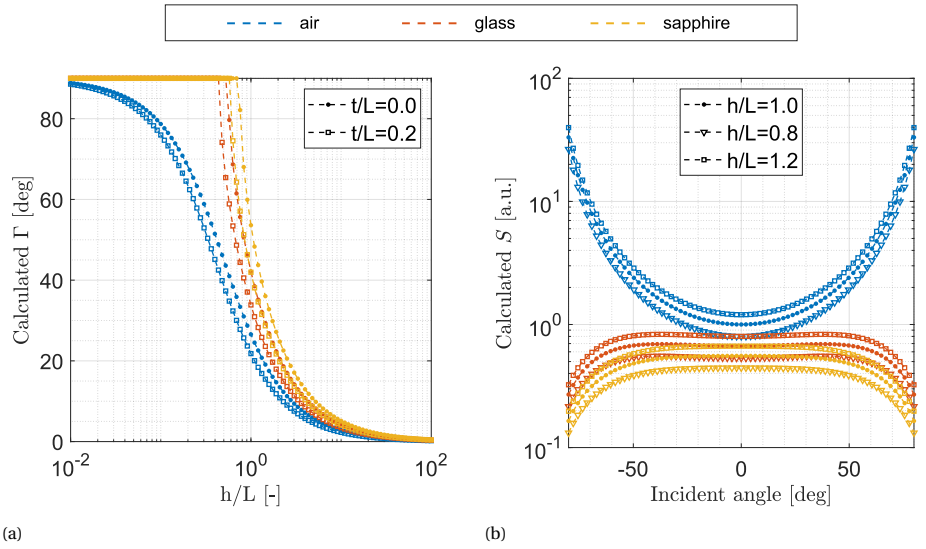
Figure 2.1: Schematic overview of the quadrant sun position sensor for a) perpendicular illumination and b) arbitrary direction. The direction towards the light source is defined by $\angle\theta$ (orange) and $\angle\varphi$ (blue) and the corresponding lateral displacement of the light spot is described by Δx and Δy. Including t as the distance between photodetectors, L as the aperture dimension, h as the distance between metal mask and photodetectors and the light spot overlap is d at perpendicular illumination.

$$\angle\theta = \tan^{-1}\left(\frac{\Delta x}{h}\right) \quad \text{and} \quad \angle\varphi = \tan^{-1}\left(\frac{\Delta y}{h}\right), \tag{2.1}$$

where h is the optical window thickness. The determination of Δx and Δy is done through a readout scheme that compares the illuminated areas of the photodetectors. Snell's Law is added to account for refraction into the optical window, which results in

$$\angle\theta = \sin^{-1}\left(\frac{n_2}{n_1}\sin\left(\tan^{-1}\left(\frac{\Delta x}{h}\right)\right)\right) \quad \text{and} \quad \angle\varphi = \sin^{-1}\left(\frac{n_2}{n_1}\sin\left(\tan^{-1}\left(\frac{\Delta y}{h}\right)\right)\right), \tag{2.2}$$

where n_2 is the refractive index of the optical window and n_1 the refractive index of air ($n_1 = 1$). There are two leading parameters that characterize the geometry of the device, which are the field-of-view (FoV) and sensitivity. Unfortunately, it is not possible to define a single sensible figure-of-merit (FoM) to rank each implementation, as



(a) (b)

Figure 2.2: Simulation results of the quadrant sun position sensor leading parameters, considering optical windows with refractive indices of air ($n_2 = 1$), glass ($n_2 = 1.5$) and sapphire ($n_2 = 1.8$). The device a) field-of-view Γ (Equation 2.4) over a range of optical window thickness h and aperture dimension L ratios. The influence of the trench width t is depicted by two t/L ratios. The device b) sensitivity S (Equation 2.5) over a range of incident angles. The effect of varying h/L ratio is depicted for three ratios.

the two parameters to be optimized are orthogonal in nature. The device FoV is determined by the maximum detectable lateral translation, which is dictated by d as long as the photodetectors dimensions are large enough[1]. The determination of d through direct measurement is challenging, but can be related to the aperture dimension if one assumes the incident light rays completely parallel. From Figure 2.1a it is deduced that

$$d \approx \frac{L-t}{2}, \tag{2.3}$$

with t the spacing between photodetectors. Note that the collimating sun sensor FoV is asymmetric for a square aperture (see Figure A.2) and the above definition holds for angles in the direction of the x- or y-axis. Finally, the four quadrant sun sensor FoV is calculated by substituting Equation 2.3 in Equation 2.2, which results in

$$\Gamma < \sin^{-1}\left(\frac{n_2}{n_1}\sin\left(\tan^{-1}\left(\frac{L-t}{2h}\right)\right)\right). \tag{2.4}$$

The sensitivity is determined by the change of the lateral displacement, which implies solving Equation 2.2 for Δx and Δy and taking the derivative towards $\angle\theta$ and $\angle\varphi$ respectively. This derivation (listed in Equations A.1 to A.7) results in

[1] The device FoV is maximized by photodetectors of dimensions $> 2d$ and should be ensured in the device design. The alternative is a reduced FoV that is dictated by the photodetector dimensions.

$$S_{\angle\theta} = \frac{h n_1 n_2^2 \cos(\angle\theta)}{\left(n_2^2 - n_1^2 \sin^2(\angle\theta)\right)\sqrt{n_2^2 - n_1^2 \sin^2(\angle\theta)}} \quad \text{and}$$
$$S_{\angle\varphi} = \frac{h n_1 n_2^2 \cos(\angle\varphi)}{\left(n_2^2 - n_1^2 \sin^2(\angle\varphi)\right)\sqrt{n_2^2 - n_1^2 \sin^2(\angle\varphi)}}. \tag{2.5}$$

Although one can intuitively think about the relation between the device geometry and the leading parameters Γ and S, the interplay is plotted using the presented relations in Figure 2.2. This leads to several conclusions on the design parameters. Firstly, the increased refractive index of different materials for the optical window positively affects the FoV, while it negatively impacts the sensitivity. A perfect FoV can be reached, which would never be possible without refraction, and a relatively constant sensitivity is expected over a large range because of the effect of refraction. Secondly, another contradiction is the effect of varying the h/L ratio. A lower ratio allows for a larger (or even ideal) FoV, while it reduces the sensitivity. Finally, it is concluded that the addition of trenches between the photodetectors has a negligible effect on the leading parameters.

The defined sensitivity is useful in the consideration of designing the device geometry, but it is not a conventional parameter given in state-of-the-art. The reason for this is of course that this parameter is challenging to extract from an actual device. Therefore, the sensitivity is replaced by the sensor accuracy when characterizing the device. The most commonly used definitions of the accuracy are the mean angular accuracy (MAA) and the 3σ error[2], which are calculated over N sets of angular information by

$$\varepsilon_{\text{MAA}} = \frac{1}{2N}\sum_{n=1}^{N} \left|\angle\theta_{\text{n}} - \angle\theta_{\text{n,ideal}}\right| + \left|\angle\varphi_{\text{n}} - \angle\varphi_{\text{n,ideal}}\right| \quad \text{and} \quad \varepsilon_{3\sigma} = \varepsilon_{\text{MAA}} + 3\sigma_{\text{MAA}}. \tag{2.6}$$

2.1.2. READOUT METHODOLOGY USING CURRENT RATIO

There are three different illumination cases to consider for the quadrant sun position sensor. Firstly, the light spot partially illuminates all photodetectors within the sensor area, as illustrated in Figure 2.3a, which is the desired situation inside the device FoV. Secondly, the light spot does not illuminate several photodetectors, as illustrated in Figure 2.3b, which is outside the device FoV. It can be easily identified that this situation lies outside the device FoV, as two or more photodetectors will not generate photocurrent. Finally, the light spot partially illuminates all photodetectors and is partially outside the sensor area, as illustrated in Figure 2.3c, which is outside the device FoV. This situation is much harder to recognize, as all photodetectors are generating photocurrent. To completely omit this illumination case, the design is constrained by setting the maximum aperture dimension L to equal the photodetector dimension.

Since the photodetectors are only partially illuminated through the aperture, the generated photo current is calculated using the ratio of the illuminated area to the total area of the photodetector using

[2] Known as the empirical rule in statistics, 99.73 % of the error values lie within a band around the mean in a normal distribution with three standard deviations.

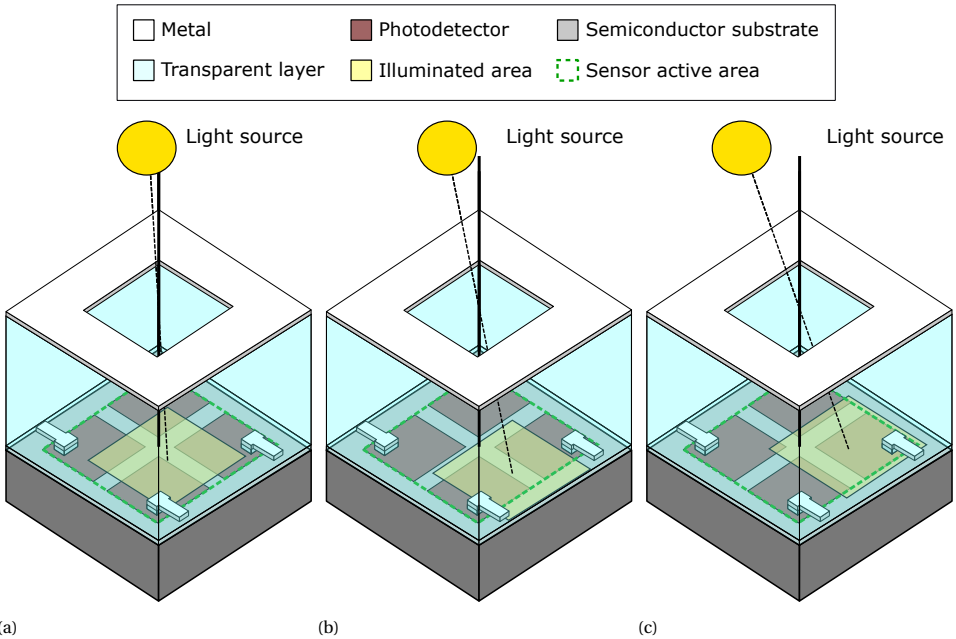


Figure 2.3: Three different light spot illumination situations in the quadrant sun position sensor illustrating a) partial illumination of all four photodetectors inside the sensor active area, b) no illumination of some photodetectors and c) partial illumination outside the sensor active area.

$$I_{\mathrm{PD}}\left(\theta,\varphi\right)=\frac{A\left(\theta,\varphi\right)}{A_{\mathrm{tot}}}I_0\cos\left(\theta\right)\cos\left(\varphi\right), \tag{2.7}$$

where $A\left(\theta,\varphi\right)$ is the illuminated area of a single photodetector, A_{tot} the total area of a single photodetector and I_0 the current generated at perpendicular illumination of the full photodetector area. Note that A_{tot} is therefore also incorporated in I_0. An approach for estimating I_0 is given in Section 2.4.1. As $A\left(\theta,\varphi\right)$ will be used in the readout scheme, it should be considered that it is trivial to calculate the overlap of a square light spot over a square photodetector, but not for a circular light spot over a square photodetector. For this reason, only a square aperture is consider for the evaluation of the quadrant sun position sensor, though it would work comparatively to one with a circular aperture. The resulting generated photocurrent of each photodetector in the quadrant sun position sensor for a fixed geometry over the full angular range is given in Figure 2.4.

The first step in the determination of the angular information, is to identify the function of each photodetector. This function for each photodetector is unique and directly related to the quadrant of the direction vector, which is illustrated in Figure 2.5. There are three marked roles, which are the reference photodetector $\mathrm{PD_r}$, the photodetector used for Δx determination $\mathrm{PD_x}$ and the photodetector used for Δy determination $\mathrm{PD_y}$. The fourth photodetector is not needed and therefore not considered. The reference is

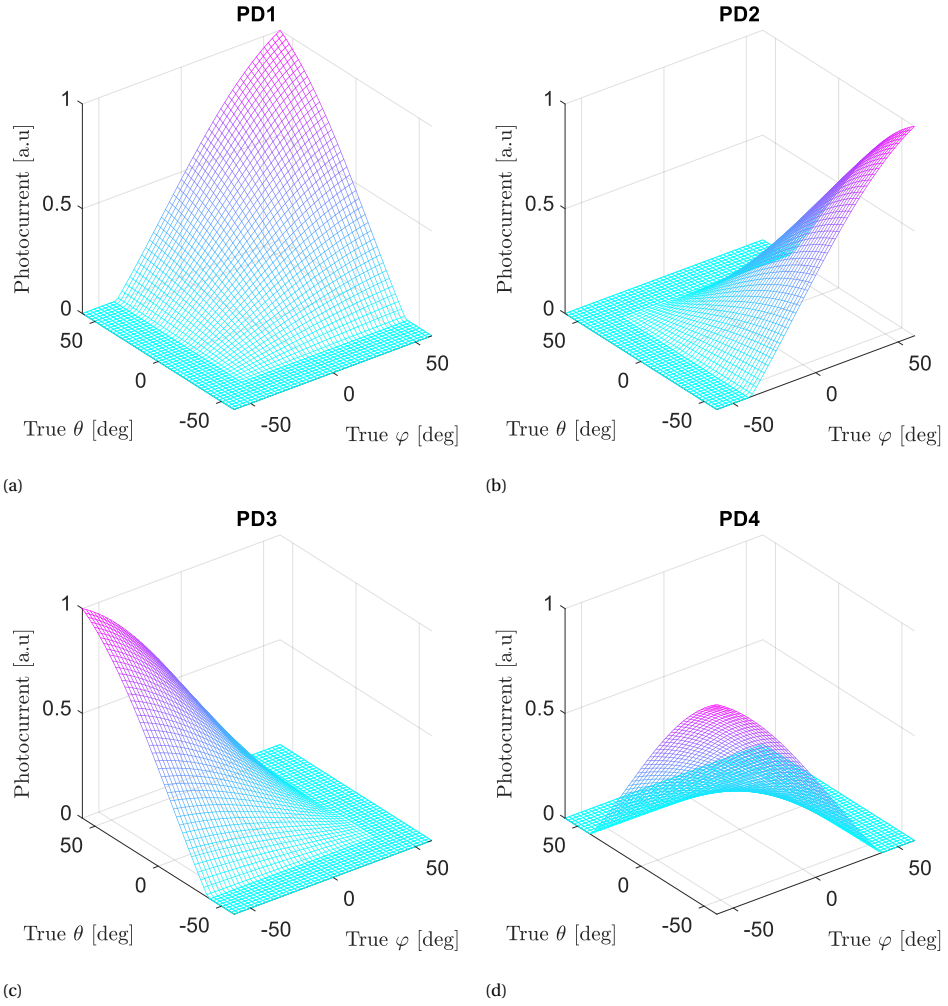


Figure 2.4: Normalized generated photocurrent of each quadrant photodetector (PD1, PD2, PD3 and PD4) for each direction vector ($\angle\theta$,$\angle\varphi$). Each angle vector is discritized in 51 steps, which results in a total of 2601 points in the depicted mesh.

identified by the photodetector with the largest photocurrent[3] and results in the function definitions listed in Table 2.1. When each photodetector is assigned to its function using this simple look-up table (LUT), ratios can be calculated from the measured photocurrents that are dependent on a single rotation angle by

$$R_{\mathrm{x}}(\theta) = \frac{I_{\mathrm{PD,x}}(\theta,\varphi)}{I_{\mathrm{PD,r}}(\theta,\varphi)} \quad \text{and} \quad R_{\mathrm{y}}(\varphi) = \frac{I_{\mathrm{PD,y}}(\theta,\varphi)}{I_{\mathrm{PD,r}}(\theta,\varphi)}. \tag{2.8}$$

[3] In the case where two or more photodetectors would produce identical photocurrent, taking any one of these as the reference would also result in identical direction vectors.

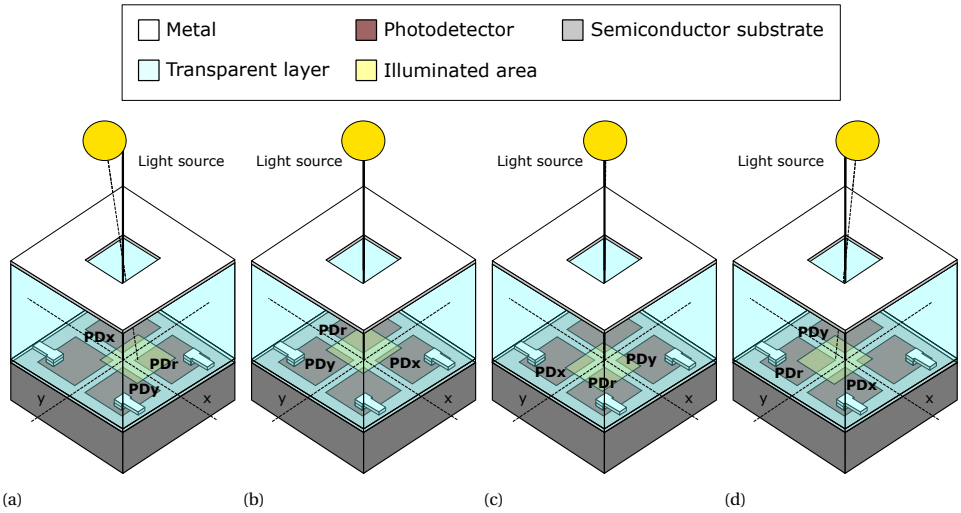


Figure 2.5: The four photodetector role divisions PD_r, PD_x and PD_y of the quadrant sun position sensor for quadrants a) $\angle\theta > 0°$ and $\angle\varphi > 0°$, b) $\angle\theta < 0°$ and $\angle\varphi > 0°$, c) $\angle\theta > 0°$ and $\angle\varphi < 0°$ and d) $\angle\theta < 0°$ and $\angle\varphi < 0°$.

At this point, it cannot yet be concluded that these ratios are indeed solely dependent on a single rotation angle. To reveal this, the areas A of the specific photodetector functions are first reduced to the multiplications

$$\begin{aligned} A_r(\theta,\varphi) &= (d+\Delta x(\theta))\left(d+\Delta y(\varphi)\right) \quad \text{and} \\ A_x(\theta,\varphi) &= (d-\Delta x(\theta))\left(d+\Delta y(\varphi)\right) \quad \text{and} \\ A_y(\theta,\varphi) &= (d+\Delta x(\theta))\left(d-\Delta y(\varphi)\right). \end{aligned} \tag{2.9}$$

Note that the lateral displacements Δx and Δy are defined to only depend on the corresponding rotation axis. These area definitions are substituted in Equations 2.7 and 2.8 for each photodetector function, which yields

$$R_x(\theta) = \frac{I_{0,x}}{I_{0,r}}\frac{d-\Delta x(\theta)}{d+\Delta x(\theta)} \quad \text{and} \quad R_y(\varphi) = \frac{I_{0,y}}{I_{0,r}}\frac{d-\Delta y(\varphi)}{d+\Delta y(\varphi)}. \tag{2.10}$$

Note that in the ideal situation $I_{0,x} = I_{0,y} = I_{0,r}$, which simplifies the relation as the

Table 2.1: Function definition of the photodetectors as marked in Figure 2.1b, identifying the reference by the photodetector that generates the largest photocurrent. In each definition, a single photodetector is not used.

PD_r	PD_x	PD_y
PD_1	PD_2	PD_3
PD_2	PD_1	PD_3
PD_3	PD_4	PD_1
PD_4	PD_3	PD_2

first term is removed. In the non-ideal case where there is mismatch, calibration constants can be derived as described in Section 2.1.3. Solving for the lateral displacements in the ideal case results in

$$\Delta x(\theta) = d\frac{1-R_x(\theta)}{1+R_x(\theta)} \quad \text{and} \quad \Delta y(\varphi) = d\frac{1-R_y(\varphi)}{1+R_y(\varphi)}. \tag{2.11}$$

Finally, the lateral displacements are calculated considering some geometry parameters and the ratios between photodetector outputs, which allows for determination of the angular information by returning to Equation 2.2. The resulting readout scheme is described by Algorithm 1.

Algorithm 1 Readout algorithm for the quadrant sun position sensor, translating the raw photodetector outputs to the angular information.

1: Measure the photodetector output currents PD1, PD2, PD3 and PD4.
2: Determine the function of each photodetector as given in Table 2.1.
3: Calculate the ratios between photodetector outputs by Equation 2.8.
4: Calculate the lateral displacements using the ratios by Equation 2.11.
5: Calculate the angular information using the lateral displacements by Equation 2.2.

2.1.3. INCREASING PERFORMANCE BY CALIBRATION

The ideal quadrant sun position sensor, without mismatching between the photodetectors and overlay misalignment, is optimally readout with the previous presented model. However, to account for situations that do suffer from these non-ideal effects, the model needs to be complemented with calibration constants. These two non-idealities are different mechanisms with similar effects on the generated photocurrent of each photodetector. Firstly, the mismatching effect between the four photodetectors is described by

$$m_1 I_0 = m_2 I_0 = m_3 I_0 = m_4 I_0, \tag{2.12}$$

where m_i is the mismatch factor for the respective photodetector with $m_i = 1$ in the ideal case. Similarly, the overlay misalignment affects the illuminated area of each photodetector, which can be described by

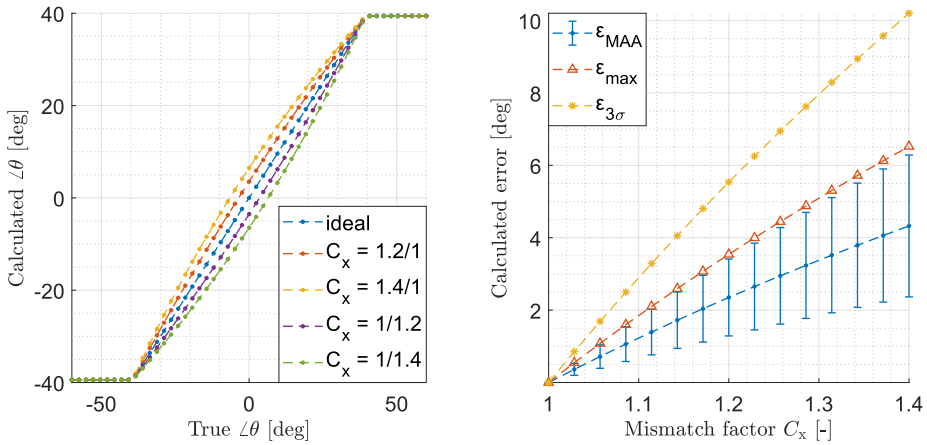
$$p_1 A_1(\theta,\varphi) = p_2 A_2(\theta,\varphi) = p_3 A_3(\theta,\varphi) = p_4 A_4(\theta,\varphi), \tag{2.13}$$

where p_i is the overlay misalignment factor for the respective photodetector with $p_i = 1$ in the ideal case. Substituting Equations 2.12 and 2.13 in the derived model in Equation 2.10 for the ratios in the ideal case, now yields

$$R_x(\theta) = \frac{m_x p_x}{m_r p_r}\frac{I_{0,x}}{I_{0,r}}\frac{d-\Delta x(\theta)}{d+\Delta x(\theta)} \quad \text{and} \quad R_y(\varphi) = \frac{m_y p_y}{m_r p_r}\frac{I_{0,y}}{I_{0,r}}\frac{d-\Delta y(\varphi)}{d+\Delta y(\varphi)}. \tag{2.14}$$

Thus the effects of mismatch and overlay misalignment are simplified into a pair of calibration constants, that are unique for each quadrant[4], resulting in

[4] A unique pair of C_x and C_y is appended to the function definition in Table 2.1 for calibration.



(a) (b)

Figure 2.6: Simulation results considering the combined effect of photodetector mismatch and overlay misalignment using a fixed device geometry. The single axis angular response a) lists four different cases, which are chosen to be large mismatch in favour of visualizing the effect. The mismatch is varied b) over a similar range to investigate the relation.

$$R_x(\theta) = C_x \frac{d - \Delta x(\theta)}{d + \Delta x(\theta)} \quad \text{and} \quad R_y(\varphi) = C_y \frac{d - \Delta y(\varphi)}{d + \Delta y(\varphi)}. \tag{2.15}$$

Concurrently, this relation is rewritten to derive the relation for the lateral displacements, which yields

$$\Delta x(\theta) = d \frac{C_x - R_x(\theta)}{C_x + R_x(\theta)} \quad \text{and} \quad \Delta y(\varphi) = d \frac{C_y - R_y(\varphi)}{C_y + R_y(\varphi)}. \tag{2.16}$$

The effect of neglecting the calibration on the angular response is depicted in Figure 2.6a, indicating that the largest error occurs around perpendicular illumination. Typical values for the mismatch factor are in the order of a few percent. The mismatch factor is varied to visualize the effect on the different accuracy definitions in Figure 2.6b, which is a proportional relation. The first observation is that one can get away with neglecting the calibration of course sun position sensors ($\varepsilon_{MAA} > 0.5°$) as even a mismatch of 10 % yields a ε_{MAA} of 1.5°. The second observation is the large difference between the ε_{max} and $\varepsilon_{3\sigma}$. As per definition, the expectation is $\varepsilon_{max} > \varepsilon_{3\sigma}$, which is opposite in this situation. In this case it may be evident to state that the $\varepsilon_{3\sigma}$ is not relevant, as we investigate a predictable offset in this example. However, it is much harder to assess this if one does not obtain the full angular range when characterizing devices.

There are multiple approaches to find the calibration constants C_x and C_y, but the most accurate procedure is to numerically calculate the calibration sets for each quadrant with the lowest ε_{MAA} using sets of measured and true angle compositions. This is of course a one time calibration that is demanding in measurement efforts for each indi-

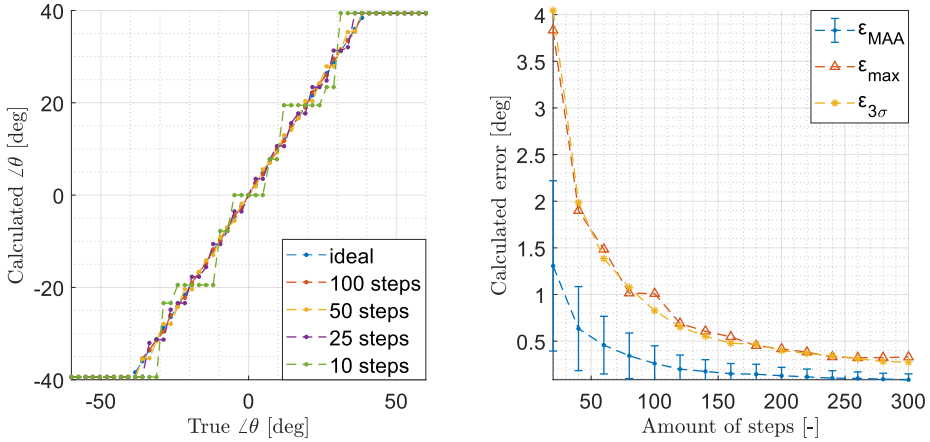
vidual device and remains prone to drift over time (such as photodetector degradation). When aiming for a fine sun position sensor ($\varepsilon_{\text{MAA}} < 0.5°$), the cumbersome calibration could be skipped if the mismatch factor is <4 %, which in turn demands more from the device fabrication.

2.1.4. EFFECT OF FINITE RESOLUTION

Up to this point, the quadrant sun position sensor response could be transformed with infinite resolution and accuracy, given that one takes constant non-idealities such as geometry offsets into account. However, each photodetector output needs to be measured or compared in the first step in Algorithm 1, which introduces a resolution through analog-to-digital conversion or comparator offset. Therefore, the quadrant sun position sensor is fundamentally subjected to a finite resolution, and thus accuracy, even without considering system non-idealities such as the signal-to-noise ratio (SNR). To investigate this, the true photodetector outputs are now discretized with a fixed resolution before calculating the angular information, through

$$I_{\text{PD,s}}(\theta,\varphi) = \left\lfloor \frac{I_{\text{PD}}}{q_{\text{step}}} \right\rceil q_{\text{step}}, \tag{2.17}$$

where q_{step} is the quantization step or resolution. The effect on the angular response is given in Figure 2.7a, which intuitively seems to have random offsets even though each step is completely deterministic. The amount of discrete steps is varied in Figure 2.7b, which shows an exponential decay relation. In stark contrast with Figure 2.6b, the expectation $\varepsilon_{\text{max}} > \varepsilon_{3\sigma}$ is met, especially considering that these should be close in magni-



(a) (b)

Figure 2.7: Simulation results considering the effect of finite resolution of the photodetector readout using a fixed device geometry. The single axis angular response a) lists four different cases, which are chosen to be large mismatch in favour of visualizing the effect. The resolution is varied b) over an extended range to investigate the relation.

tude. This verifies the intuitive observation of a pseudorandom offset. Furthermore the crossing point from theoretical course and fine sun position sensors is around 50 steps, which corresponds to $\lceil log_2(50) \rceil = 6$ bits.

Additional negative effects on the device accuracy are caused by the non-idealities in the system, which are not further investigated here. Parameters to consider are the SNR, internal reflections, charging and readout circuit performance

2.2. PIXEL ARRAY SUN POSITION SENSOR

Using the miniaturization and reproducibility benefits that microfabrication technology brings, the amount of photodetectors in the sensor area can be scaled up. The schematic overview of this architecture is given in Figure 2.8 and indicates the relevancy of on-chip control and readout electronics. By use of the photodetector array, or pixel array, one can employ different strategies to find the angular information.

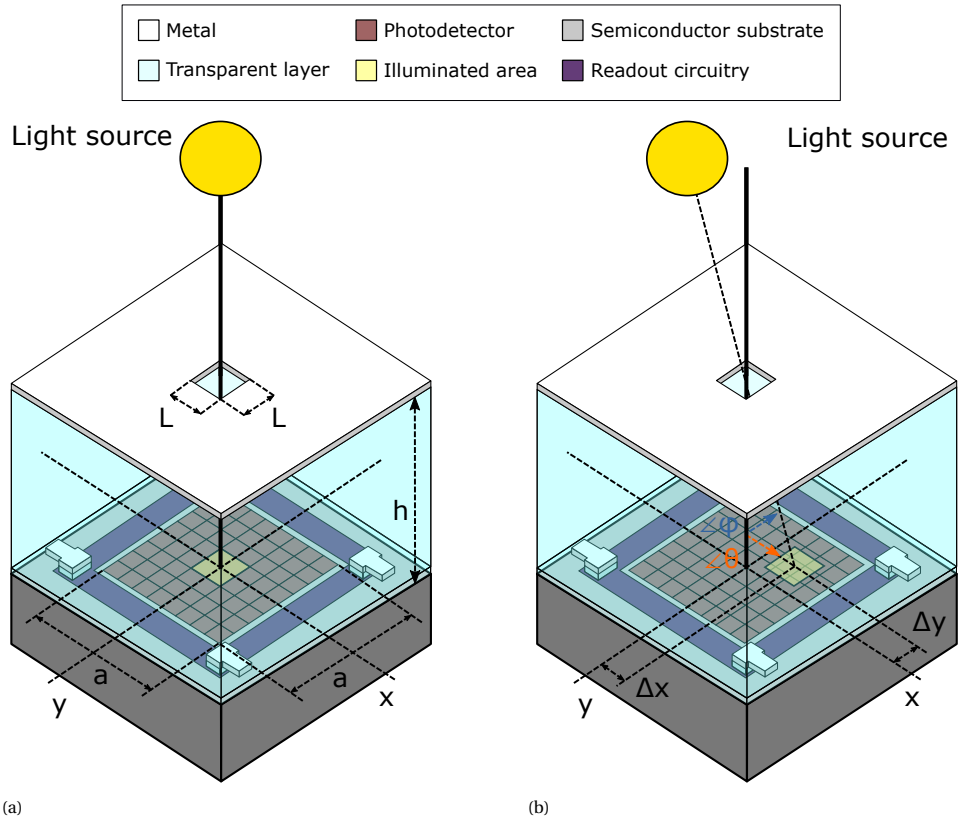


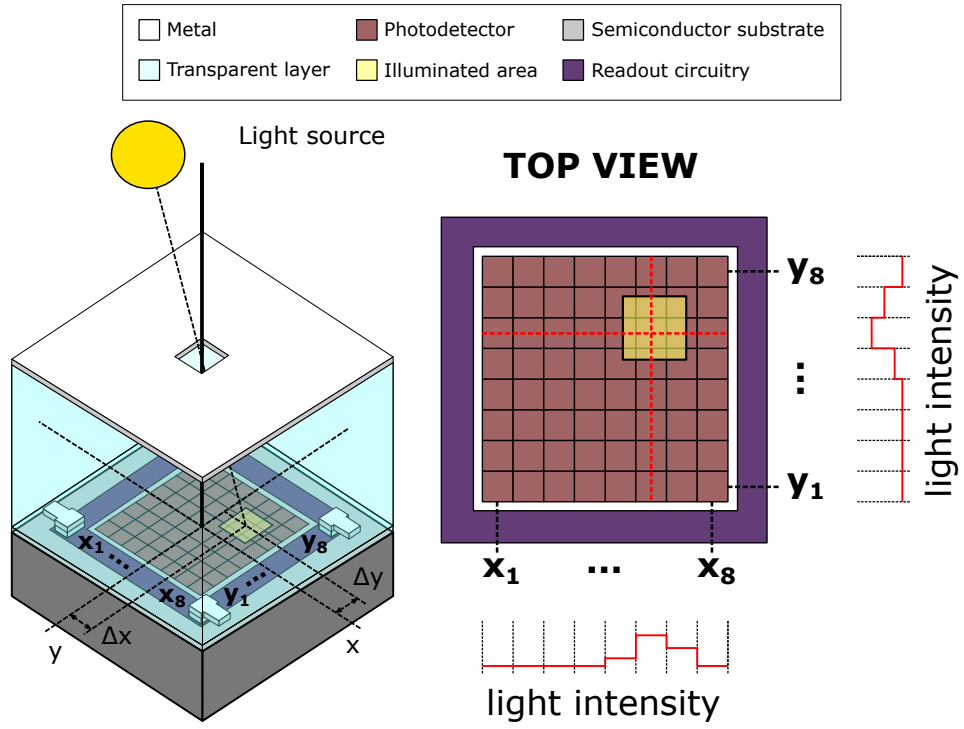
Figure 2.8: Schematic overview of the pixel array sun position sensor for a) perpendicular illumination and b) arbitrary direction. The direction towards the light source is defined by $\angle\theta$ (orange) and $\angle\varphi$ (blue) and the corresponding lateral displacement of the light spot is described by Δx and Δy. Including a as the sensor active area, L as the aperture dimension and h as the distance between metal mask and photodetectors.

2.2.1. ADDITIONAL DESIGN PARAMETERS

The previously discussed leading design parameters of the quadrant sun position sensor (see Section 2.1.1), are still relevant in this architecture. Firstly, the given definitions for different errors in the device characterization, remain identical for the current case. Secondly, the sensitivity is dependent on shared geometry parameters and the same conclusions therefore hold. However, for the FoV definition, the situation is slightly changed as there no longer is a parameter d. The maximum detectable lateral translation is now simply equal to the point where the light spot moves out of the sensor active area, resulting in the very similar relation

$$\Gamma < \sin^{-1}\left(\frac{n_2}{n_1}\sin\left(\tan^{-1}\left(\frac{a-L}{2h}\right)\right)\right). \tag{2.18}$$

Note that compared to the quadrant sun position sensor Γ in Equation 2.4, the only differences are $L \rightarrow a$ and $t \rightarrow L$. This implies that the FoV is now dominated by the choice of a and that the size of L only has a marginal effect. Another crucial design parameter in this architecture is the amount of pixels used. But to investigate this, the readout methodology must be considered first, which is discussed next.



(a) (b)

Figure 2.9: Schematic illustration of the centroid principle of a) the overview of the pixel array and b) the top view with indicated readout value for highlighted row and column.

2.2.2. READOUT METHODOLOGY USING CENTROID

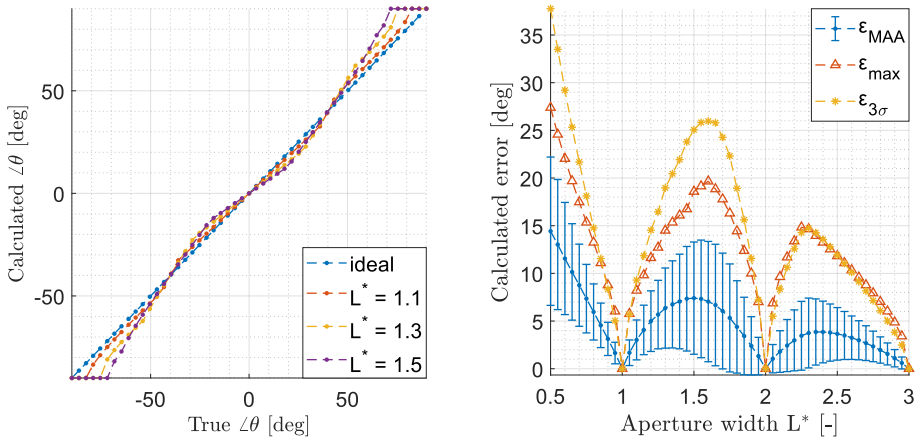
The translation of the light spot is directly dependent on the location of the illuminated photodetectors. As a result, one can use the photodetector output and location to determine the light spot translation in a centroid algorithm [5, 6]. In this case, a weighted average approximation is performed to find the centroid, though an analytic calculation is also an option. However, in the case of an analytic calculation, one would focus on a region of interest and assign photodetector roles, while misidentification of these roles is a risk to the device accuracy, especially with low pixel counts. Here, we sum the contribution of each photodetector through

$$\Delta x(\theta) = \frac{1}{S}\sum_{i=1}^{M} I_{\mathrm{PD,i}}(\theta,\varphi)\, x_{\mathrm{i}} \quad \text{and} \quad \Delta y(\varphi) = \frac{1}{S}\sum_{i=1}^{M} I_{\mathrm{PD,i}}(\theta,\varphi)\, y_{\mathrm{i}}, \tag{2.19}$$

where $I_{\mathrm{PD,i}}(\theta,\varphi)$ is the generated photocurrent of each photodetector (calculated by Equation 2.7), S the sum of generated photocurrent, M the total amount of photodetectors and x_i or y_i the coordinate of the corresponding photodetector center in the array. Note that $I_{A,i}(\theta,\varphi)$ is sensitive to both angles $\angle\theta$ and $\angle\varphi$, but only the contribution of x_i

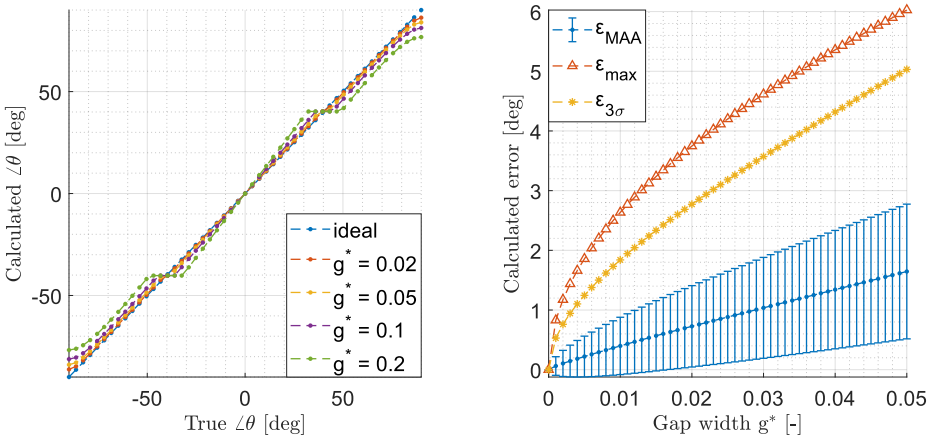
Algorithm 2 Readout algorithm for the pixel array sun position sensor, translating the raw photodetector outputs to the angular information.

1: List the coordinates of each respective photodetector in the array.
2: Measure all photodetector output currents in the array.
3: Sum the weighted individual contributions, using the coordinates, by Equation 2.19.
4: Calculate the angular information using the lateral displacements by Equation 2.2.



(a) (b)

Figure 2.10: Simulation results considering the effect of different ratios of aperture and pixel size L^* using a fixed device geometry (8 × 8 pixels). The single axis angular response a) lists three different cases visualizing the effect. The resolution is varied b) over an extended range to investigate the relation.



(a) (b)

Figure 2.11: Simulation results considering the effect of different ratios of gap width and pixel size g^* using a fixed device geometry. The single axis angular response a) lists four different cases visualizing the effect. The resolution is varied b) over an extended range to investigate the relation.

or y_i is considered for determination of $\Delta x(\theta)$ or $\Delta y(\varphi)$ respectively. The generated photocurrent $I_{\mathrm{PD,i}}(\theta,\varphi)$ is still calculated by Equation 2.7, though no general relation for the illuminated area can be given. This concept is illustrated in Figure 2.9 for an 8×8 pixel array. Using the found light spot lateral displacements, the angular information is obtained using Equation 2.2. This readout scheme is described in Algorithm 2.

The effect of the amount of pixels is best visualized by considering the ratio of the aperture width and the width of a single pixel. As such, the normalized aperture width L^* is varied, which shows a noticeable distortion on the angular response in Figure 2.10a. The ideal case is for $L^* = 1$, thus requiring the aperture width and pixel width to be equal. The aperture width is varied over an extended range in Figure 2.10b, indicating that the aperture width must be an integer multiple of the pixel width to yield an ideal angular response. It can furthermore be deduced that the distortion effect is reduced around higher integer multiples of the pixel size. The consequence for the amount of pixels is that neglecting the matching of aperture and pixel size may result in large distortion. However, increasing the amount of pixels while keeping the aperture size constant, greatly reduces the caused distortion if mismatches in sizing remain.

In contrast to the quadrant sun position sensor, the addition of gaps between pixels significantly distorts the sensor angular response, as depicted in Figure 2.11a. Varying the gap width in Figure 2.11b indicates that the maximum allowable gap width is 1.3 % of the pixel width for the device to qualify as fine sun sensor (in this fixed geometry). A closer look at Figures 2.10a and 2.11a suggests that the caused distortions are opposite in nature. Indeed, adding the gap width to the aperture width yields the ideal curve without distortion, of course ensuring that the aperture width is a multiple of the pixel width before adding the gap width. As such, this allows for the design of ideal sensor geometries that include gaps for photodetector separation.

2.2.3. CALIBRATION OF THE PIXEL ARRAY

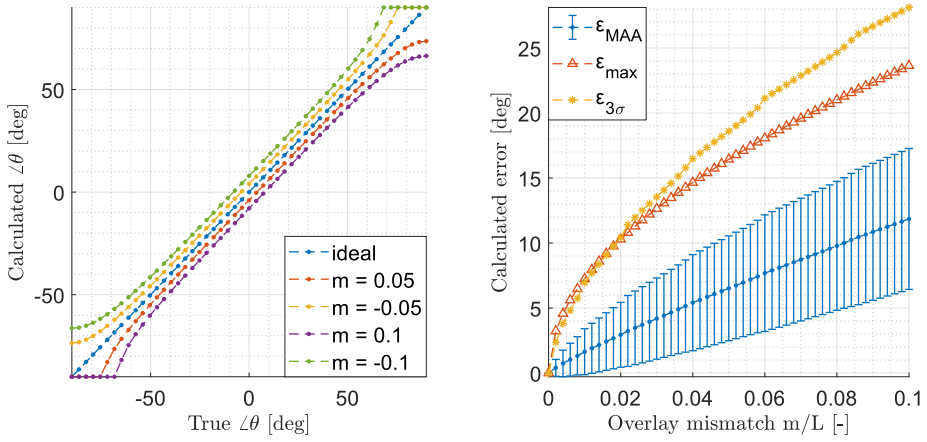
The pixel array sun position sensor readout scheme is tolerant towards photodetector mismatch, as it no longer directly compares photodetectors and averages over multiple photodetectors. Small array sizes approaching the 2×2 size of the quadrant sun position sensor may however be influenced significantly, as one can no longer average over a large amount of pixels that way. Since taking into account individual mismatch coefficients for each individual pixel in the array requires a huge LUT which is a practically infeasible approach, the effect of mismatch is not taken into account for the calibration of the pixel array sun position sensor.

This leaves only the overlay misalignment as source for the sensor offset. As the individual pixel coordinates are already used to find the lateral translations, calibration can be done by adding the misalignment by

$$\Delta x(\theta) = \frac{1}{M}\sum_{i=1}^{M} I_{\mathrm{PD,i}}(\theta,\varphi)\,(x_\mathrm{i} - C_\mathrm{x}) \quad \text{and} \quad \Delta y(\varphi) = \frac{1}{M}\sum_{i=1}^{M} I_{\mathrm{PD,i}}(\theta,\varphi)\,(y_\mathrm{i} - C_\mathrm{y}). \tag{2.20}$$

The effect of the misalignment on the angular response is depicted in Figure 2.12a and corresponds to a fixed shift for most of the FoV. The effect of misalignment is high, depicted in Figure 2.12b, as the misalignment must be less then 0.3 % of the aperture width to qualify as a fine sun sensor (in this fixed geometry). Implementations that can rely on microfabrication tools used for high overlay accuracy can help to ensure that this architecture does not require calibration.

The calibration efforts are greatly reduced for the pixel array sun position sensor with respect to the quadrant sun position sensor, as it is not longer required to find the



(a) (b)

Figure 2.12: Simulation results considering the combined effect of overlay misalignment using a fixed device geometry. The single axis angular response a) lists four different cases, which are chosen to be large mismatch in favor of visualizing the effect (5 % and 10 % of the aperture size). The mismatch is varied b) over a similar range to investigate the relation.

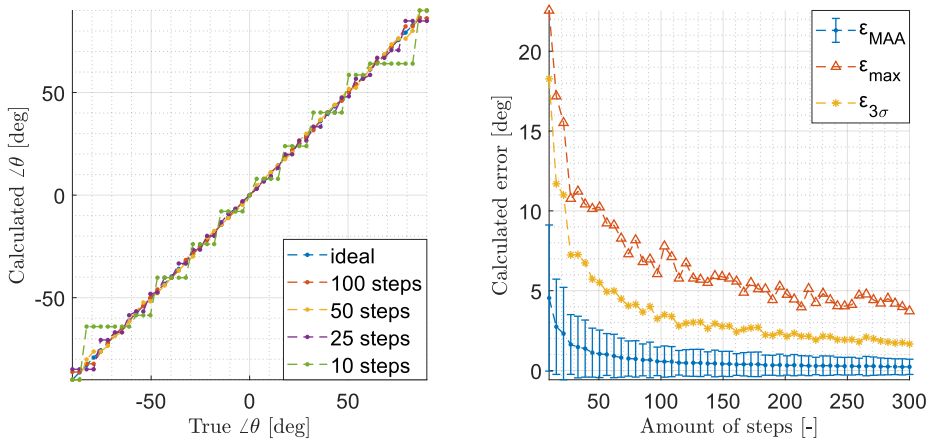
calibration constants by numerical calculation on measured calibration sets for each device. Instead, one can measure the overlay misalignment of each device using alignment structures and an optical microscope. Alternatively, several measurement points would allow for finding the shift in angular response, assuming the measurement points are not close to the FoV limits.

2.2.4. PIXEL ARRAY RESOLUTION REQUIREMENTS

Similarly to the quadrant sun position sensor, the effect of finite readout resolution is investigated. The effect on the angular response is given in Figure 2.13a, which is comparable in behaviour to the quadrant sun position sensor. Investigating over a similar range in Figure 2.13b, the accuracy improves for higher resolution, but the device qualifies as fine sun sensor only at 110 steps, corresponding to $\lceil log_2(110) \rceil = 7$ bits. This is 1 bit worse than the quadrant sun position sensor.

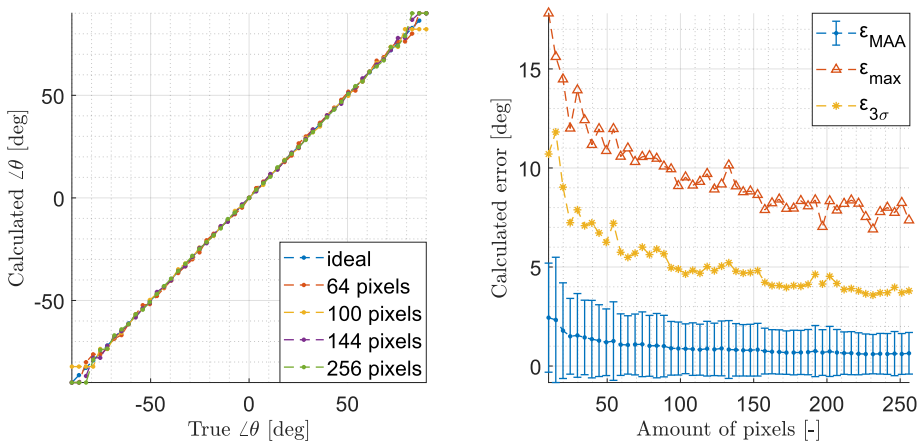
Next, the amount of pixels in the array is varied while keeping the sensor active area constant, to investigate its effect. Since it was previously deduced that the aperture width should be a multiple of the pixel width, the aperture width follows the pixel width in this simulation. The resolution is fixed at 50 steps to introduce enough non-ideality for visualization purposes, resulting in the angular responses in Figure 2.14a that show comparable behaviour to the quadrant sun position sensor. In a similar range, the accuracy in Figure 2.14b remains larger than 0.6° as is expected from the fixed resolution, thus the device is not qualifying as a fine sun sensor.

Finally, it is concluded that all the considered effects in the pixel array sun position sensor still reached the maximum FoV for the selected geometry parameters. In



(a) (b)

Figure 2.13: Simulation results considering the effect of finite resolution of the photodetector readout using a fixed device geometry. The single axis angular response a) lists four different cases, which are chosen to be large mismatch in favor of visualizing the effect. The resolution is varied b) over an extended range to investigate the relation.



(a) (b)

Figure 2.14: Simulation results considering the effect of the amount of pixels in the sensor array. The single axis angular response a) lists four different cases, visualizing the effect. The amount of pixels is varied b) within a similar range to investigate the relation.

contrast, these geometry parameters are similar to those of the quadrant sun position sensor which only reached less then half of the ideal FoV. Furthermore, the caused distortion from all effects on the angular response is largest when approaching the FoV limits, thus implying that the calculated accuracy figures will improve if the FoV is constrained to a lower range. This means that there is a direct trade-off for the pixel array sun position sensor between a larger FoV or a higher accuracy. For example, if the investigated FoV is lowered to ±50° in the last simulation on the effect of amount of pixels, the device would already qualify as fine sun sensor at the previously considered 8×8 pixel array.

2.3. DIFFRACTION GRATING SUN POSITION SENSOR

The work on angle sensitive pixels was performed by S. Şanseven as part of her thesis work in collaboration with and under supervision of the author. Parts of this section have been included in her dissertation [7].

Considering the previously discussed two collimating sun position sensor architectures, there is one shared functional part to be integrated in the sensor, which is the optical window. The integration of the optical window during by wafer-level packaging techniques is one of the main research efforts in this research work. However, using a novel sensor architecture that does not require this optical window in the first place, would drastically reduce fabrication requirements. That is what this section explores, by use of unique angle-sensitive pixels compatible to standard microfabrication technology. The pioneering work by Gill *et al.* at the Cornell University in the United States is taken as the foundation for the explored concept.

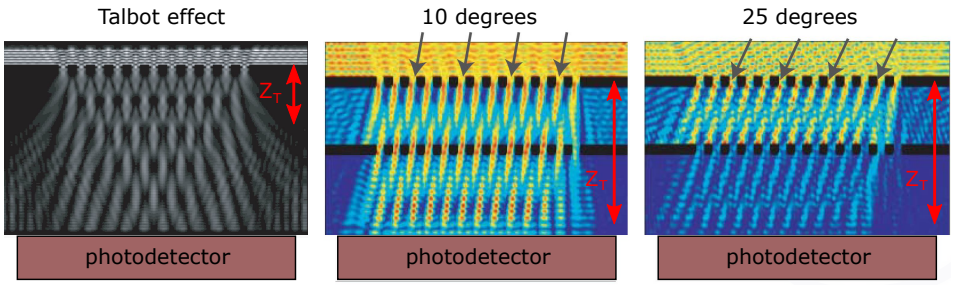


Figure 2.15: Wave simulation images of a) the Talbot effect through a single diffraction grating, b) angle sensitive pixel by means of two identical diffraction gratings with the light field at a low incident angle and c) the same angle sensitive pixel with the light field at a higher incident angle. Each case has the annotated Talbot depth Z_T. Courtesy of Gill *et al.* [9], with minor adaptations.

2.3.1. ANGLE SENSITIVE PIXELS

The previous work on angle sensitive pixels (ASPs) by Gill *et al.* focused on the miniaturization of focusing cameras, by implementation of planar Fourier capture arrays (PFCAs) through use of unique diffraction gratings on each ASP. These gratings are spaced much closer to the photodetector then conventional optics, thus allowing direct implementation during the wafer-level microfabrication. Such lensless devices fill the size gap between single photodetectors and the smallest cameras [8], while retaining full compatibility with conventional fabrication technologies. Each individual ASP in a PFCA is a single point in the so-called planar Fourier space, which needs to be captured completely to transform the array output to an actual image [9, 10]. As such, careful considerations are to be made when tiling the Fourier space through design variation of each ASP [11]. Of course, these considerations are made for conversion of an actual image, while the interest for this work is solely the incident angle of a point light source. Therefore, the tiling considerations and linear algebra used for image generation is completely omitted and reduced to its simplest form in equations, that are discussed below.

The diffraction grating ASP exploits the Talbot effect, which is the forming of strong intensity patterns at specific distances of illuminated periodic masking layers (see Figure 2.15a). These patterns are referred to as self-images and occur at integer multiples of the Talbot depth, as calculated by

$$Z_T = 2\frac{g^2}{\lambda}, \tag{2.21}$$

where g is the grating pitch and λ the wavelength of the incident light. Note that this relation is not dependent on the incident angle of the light. To make the sensor angle sensitive, a second identical grating is placed at half the Talbot depth (see Figures 2.15b and 2.15c). To compare different ASPs, the unitless angular sensitivity is defined by

$$\beta = 2\pi\frac{Z_T}{ng}, \tag{2.22}$$

where n is the refractive index of the dielectric. Two main types of ASPs that make

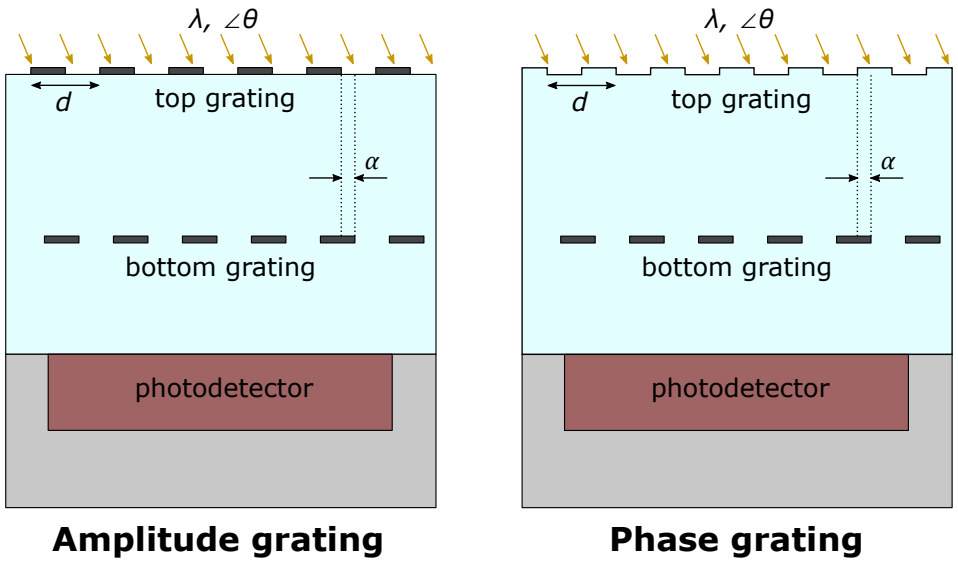


Figure 2.16: Schematic cross-section illustration of a) amplitude grating and b) phase grating architectures that include two opaque grating layers in a transparent dielectric and a photodetector. The top and bottom gratings are also referred to as diffraction and analyser gratings.

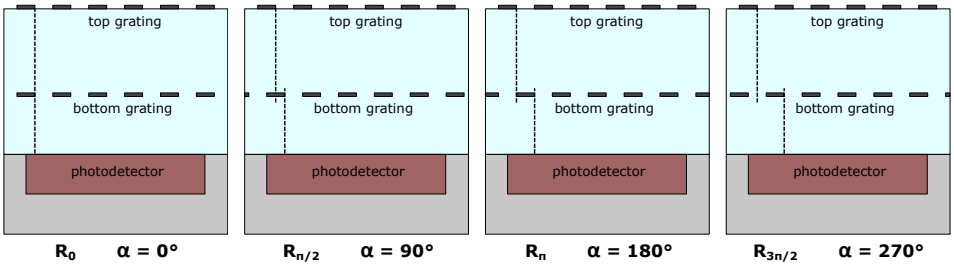
use of the Talbot effect are based on amplitude gratings or phase gratings. Amplitude gratings (fig. 2.16a) consist of two identical opaque layers of periodic gratings that are separated by a certain multiple of Talbot depths. Phase gratings (fig. 2.16b) implement the top grating layer directly in the transparent layer, which results in similar behavior but with higher quantum efficiency [12]. Placing a photodetector below the grating stack, effectively integrates the generated pattern and its output is calculated by

$$R(\theta,\varphi) = I_{\mathrm{PD,tot}}(\theta,\varphi)\left(1 - m\cos\left(\beta\angle\theta + \alpha\right)\right)F(\angle\theta), \tag{2.23}$$

where m is the modulation depth, α the phase offset and $F(\angle\theta)$ the non-idealities and noise in the system. Note that the pixel depends on both angles, because the generated photocurrent of the photodetector without diffraction gratings is also dependent on both angles. The design parameters are annotated in Figure 2.16 and include the grating pitch g and vertical distance h, but also the light source wavelength λ.

2.3.2. READOUT USING UNIQUE PIXELS

The response of a single ASP in Equation 2.23 contains both angle and intensity information on the incident light, similar to the discussed quadrant sun position sensor. To obtain the angle information of the incident light, it is necessary to either know the intensity or employ a differential measurement that eliminates the need for this information. Here, only amplitude gratings are investigated and employs ASPs with different phase offsets between the two stacked diffraction gratings, which allows for extraction



(a) (b) (c) (d)

Figure 2.17: Schematic cross-section illustration of the four amplitude grating ASPs used for determination of the angular information in Equation 2.24, including a) in-phase, b) $\pi/2$ phase shift, c) π phase shift and d) $3\pi/2$ phase shift grating layers.

of the angle information through

$$\angle\theta^* = \frac{1}{\beta}\tan^{-1}\left(\frac{R_{\pi/2}(\theta,\varphi) - R_{3\pi/2}(\theta,\varphi)}{R_0(\theta,\varphi) - R_\pi(\theta,\varphi)}\right), \tag{2.24}$$

where R_0, $R_{\pi/2}$, R_π and $R_{3\pi/2}$ correspond to pixels with phase shifts of 0, $\pi/2$, π and $3\pi/2$ respectively[5], which are illustrated in Figure 2.17. The dependency of R on both angles is reduced to only a single direction, as the gratings are all orientated in the same direction. Note that the found $\angle\theta^*$ is periodic in nature, so one has to identify the period as well to come to the actual angle. This is done through

$$\angle\theta = \angle\theta^* + kN_i, \tag{2.25}$$

where k is the period of $\angle\theta^*$ and N_i the amount of periods from the origin. To identify the period for fine angle detection, a course non-periodic ASP must be included. For example, a previous hybrid implementation demonstrated this concept using polarization and Talbot ASPs [13]. Typically, one needs two course ASPs per axis for the course angle detection (similar to the quadrant sun position sensor). As a result, this implementation requires the four phase shifted diffraction grating ASPs per rotation angle and an additional four course ASPs to counteract the periodic nature of the sensor output, bringing the minimum amount of pixels to twelve (illustrated in Figure 2.18). The resulting readout scheme is given in Algorithm 3.

Algorithm 3 Readout algorithm for the diffraction grating sun position sensor, translating the raw photodetector outputs to the angular information.

1: Measure all photodetector output currents in the array.
2: Extract the angular information using four phase shifted pixels and Equation 2.24.
3: Determine the rough angle by using the course detector.
4: Identify the period and transform the angular information through Equation 2.25.

[5]The differential measurement requires at least four pixels with $\pi/2$ phase shift.

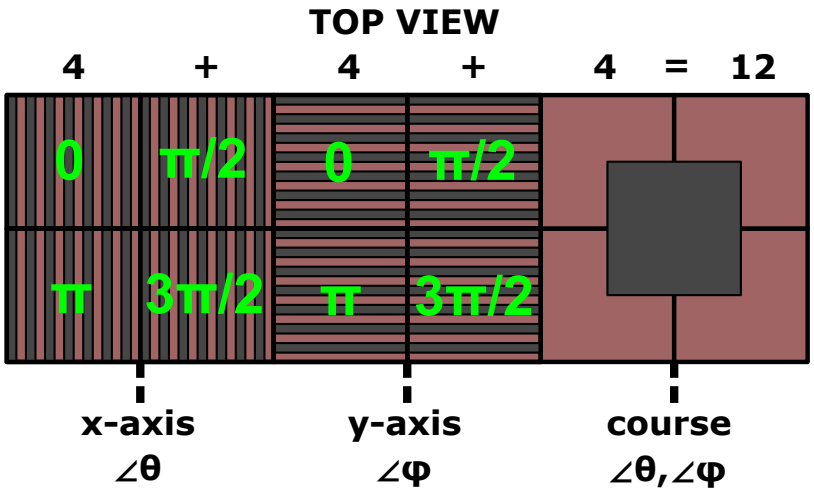


Figure 2.18: Schematic overview of the diffraction grating ASP based sensor pixels. From left to right the sensor includes four phase shifted ASPs for detection over the x-axis, another four phase shifted ASPs for detection over the y-asis and finally a course quadrant sensor. The course quadrant sensor is similar to the one discussed in Section 2.1, but it has an inverted design (metal shading instead of aperture) and has the light mask spaced much closer to the sensor which reduces its sensitivity.

To evaluate some of the design parameters of the diffraction grating ASP, the adition of COMSOL Multiphysics software is employed to allow for better control of the geometry in this architecture. Hence, the ASP response of each of the four variants (see Fig-

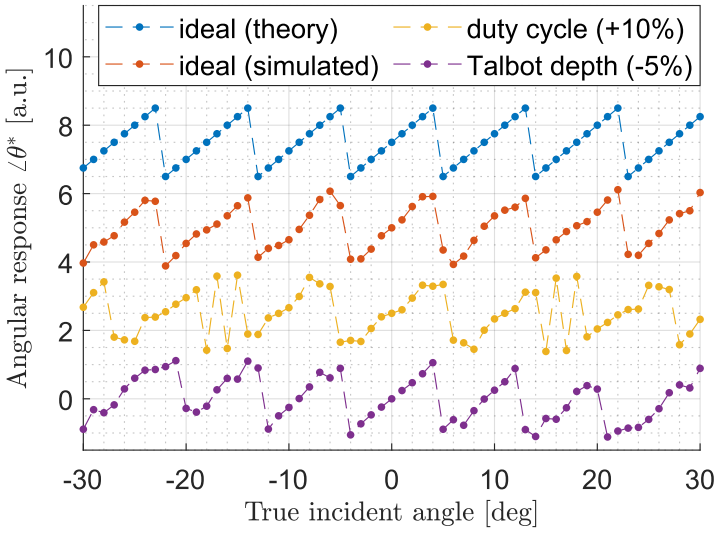


Figure 2.19: Angular response $\angle\theta^*$ as result of simulation of the ASPs considering different effects. The individual ASP simulation results are combined through Equation 2.24. The curves are shifted for readability.

ure 2.17) for different incident angles over a single rotation axis is both calculated and simulated for the ideal case. Some non-ideal cases of the design parameters are then investigated only in simulation. The outputs of the four ASPs are combined to extract the angular information using Equation 2.24 and the results are listed in Figure 2.19.

From the simulated sensor responses and listed equations, several observations are made. Firstly, the simulation result of the ideal simulated ASPs shows some distortion, which is caused by inescapable effects like reflection inside the grating stack. Upon defining the diffraction grating material, it was found that more distortion is added for materials with higher reflectivity. As such, the depicted results are using TiN, which is commonly used in microfabrication as a light masking layer with low reflectivity in the UV range. Secondly, the grating pitch inversely affects the period of the sensor response, where a larger grating pitch results in a smaller sensor response period. Consequently, the angular sensitivity goes up for a larger grating pitch (see Equations 2.21 and 2.22). The effect of a non-ideal grating pitch duty cycle is shown in Figure 2.19 and indicates severe distortion in the 15–20° range. This demonstrates that it is crucial to optimize the fabrication of the gratings to obtain an ideal duty cycle. Lastly, the vertical distance affects the period and angular sensitivity of the sensor in a similar way (see Equation 2.22) and Figure 2.19 shows that small deviations expected from the fabrication process have a minor effect.

As the sensor investigation at this stage only considered a 625 nm monochromatic light source. Future research should be directed towards broadband light sources to investigate the necessity of optical filters or odd-symmetry spiral phase gratings [14, 15].

2.3.3. ANGULAR PERIOD LIMITATIONS

The ideal periodic saw tooth response of Figure 2.19 allows for perfect construction of the angle information through Equation 2.25, but it must be identified that it has a large impact when non-idealities are put in the mix. This error occurs at the sharp transition points of the saw tooth curve, resulting in large jumps that can be caused by either photodetector readout errors or misidentification of the angular period, as illustrated in Figure 2.20a. The corresponding transformed angle in Figure 2.20b shows these errors as large spikes, that are offsets upto 10° from the ideal value.

There are multiple approaches to mitigate this effect, of which four are given here. Firstly, one can measure each device for the full angular space and build a LUT as a means of calibration of the error. This is not a scalable approach, as it demands cumbersome measurements for each individual device. A more elegant way is to ensure that one always uses the linear region of the sawtooth for the readout and not the sharp transition region. This can be accomplished using the existing pixels and rearrangement of Equation 2.24 by using $R_{i+\pi/2}(\theta,\varphi)$ (moving each R up by $\pi/2$), which effectively gives the same periodic angular response with a π phase shift. The original curve (ideal 1) and the rearranged curve (ideal 2) are given in Figure 2.20c, as well as the corresponding curves with similar errors as in Figure 2.20a. Using the course detector, one of the highlighted periods is identified and matched to either curve 1 or 2 for use in the readout, ensuring that only the linear regions are used. This holds even for the curves with the artificial readout errors, thus transforming to the ideal angle information. This approach allows for the mentioned readout errors to occur around the transition points

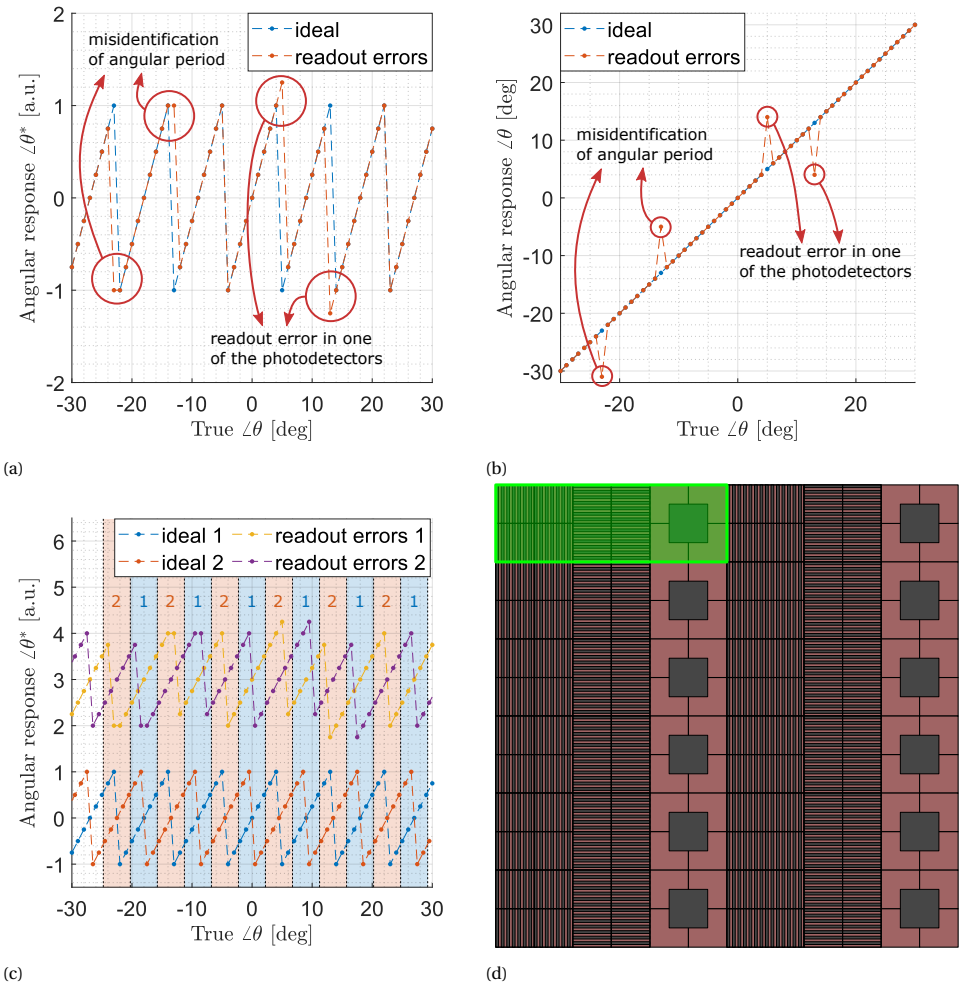


Figure 2.20: Simulation results considering the effect readout errors a) around the sharp transition points in the periodic sensor response and b) the effect on the extracted incident angle. The proposed solution c) runs a rearranged Equation 2.24 to effectively obtain a π phase shift in the angular response, allowing to ensure readout in the linear region instead of the sharp transition region. Further redundancy is achieved by d) including the same sensor configuration (highlighted in green, see Figure 2.18) multiple times to average out any errors.

with maximum offset of half of the designated periods, which in this example is 2.25°. A third approach could make a slight alteration to this, by adding new pixels with different grating pitches and/or phase differences to obtain more of these saw tooth curves that allow avoiding the use of the sharp transition point. Finally, it is straightforward to add the same pixels many times in a larger array and use the average of the collective readout to mitigate errors that individual sensors may have.

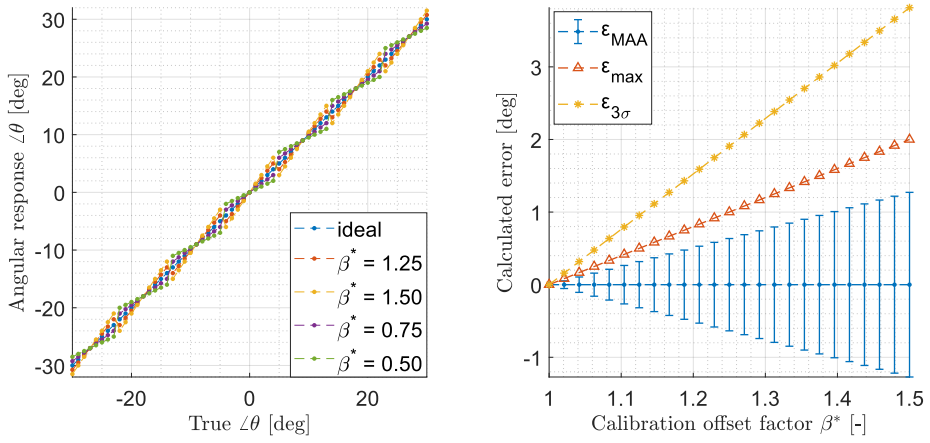
The preferred approach is to use the second and last options together. This means that the principle of using two phase shifted angular responses is combined with many copies of the same pixels, to achieve robustness for the unlikely events were there occur readout errors that span too far from the sawtooth transition point to be caught. This tackles the described angular period limitations, while keeping the added device and readout complexity to a minimum.

2.3.4. CALIBRATION AND FINITE RESOLUTION

The diffraction grating sensor still needs calibration to be operated at high accuracy. The parameter to calibrate is the angular sensitivity β, which can deviate from the calculated value in Equation 2.22 by fabrication process deviations such as the actual vertical distances between gratings. This β is the slope of the linear part of the periodic saw tooth curve and directly translates to the transformed angle response and the mismatch between the used and ideal β is here defined as

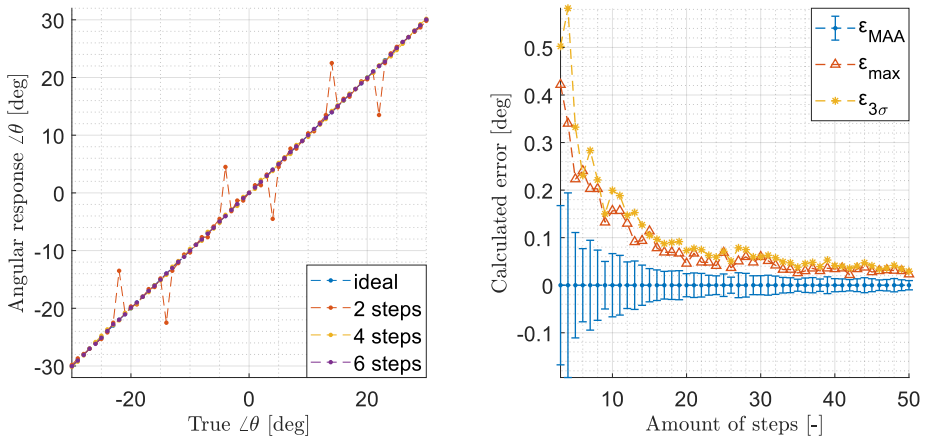
$$\beta^* = \frac{\beta_{\text{ideal}}}{\beta_{\text{used}}}, \tag{2.26}$$

with β_{ideal} the actual angular sensitivity of the device and β_{used} the angular sensitivity used for extracting angle information. The effect for different mismatch factors is illustrated in Figure 2.21a and shows periodic deviations of the ideal value that correspond with the different slopes caused by the mismatched angular sensitivity. Investigating the resulting errors in a similar range of β^* in Figure 2.21b shows that the ε_{MAA} equals to zero, which is expected due to linear deviations of the ideal value in both positive and negative direction. Additionally, the maximum and 3σ errors increase in a



(a) (b)

Figure 2.21: Simulation results considering the effect of different offset to the ideal angular sensitivity of the diffraction grating device. The single axis angular response a) lists four different cases visualizing the effect. The offset is varied b) over a similar range to investigate the relation.



(a) (b)

Figure 2.22: Simulation results considering the effect of different offset to the ideal angular sensitivity of the diffraction grating device. The single axis angular response a) lists four different cases visualizing the effect. The offset is varied b) over a similar range to investigate the relation.

linear way. The sensor is quite tolerant to neglecting the calibration, as it still qualifies as a fine sun position sensor at 6.5 % offset from the ideal angular sensitivity value.

Besides the calibration of the angular sensitivity, the effect of finite readout resolution is again investigated and the results are given for a selection in Figure 2.22a. In contrast to the previously investigated architectures, the effect of finite readout resolution is minimal, with the exception for the case of only 2 steps which shows similar spikes to errors in photodetector readout as discussed previously. This becomes even clearer in Figure 2.22b, which indicates that already at 5 discrete steps the sensor classifies as a fine sun sensor device. This makes this approach based on diffraction gratings an elegant alternative to established technologies, as it allows for standard planar microfabrication and seriously reduces the photodetector readout and calibration requirements. However, it should be noted that the complexity is moved to the overall sensor readout, combining unique pixels to transform the signal and extract the angular information. Moreover, the effects of broadband light sources must be investigated further to allow for application as sun position sensors.

2.4. RADIOMETRY CONSIDERATIONS

The optical elements in the discussed sun position architecture are further investigated in this section. As such, the generated signal from a photodetector is quantified by an estimation strategy. The quantum efficiency and the material options to implement the added optics in are considered. Finally, the effect of the albedo is illustrated and compared for the different architectures.

2.4.1. ESTIMATING THE GENERATED PHOTODETECTOR SIGNAL

Since photodetectors are typically photodiode based, they operate through the photoelectric effect and their output is a photo current. Incident photons on the photodetector result in a photo current according to the responsivity for that specific wavelength. The generated photo current by a photodetector for a single wavelength is calculated by

$$I_0(\lambda) = A_{\text{tot}} P_{\text{opt}}(\lambda) R(\lambda), \tag{2.27}$$

where $P_{\text{opt}}(\lambda)$ is the wavelength dependent incident optical power and $R(\lambda)$ the wavelength dependent responsivity. To determine the generated photo current for all wavelengths, the function is integrated over the wavelength [16] through

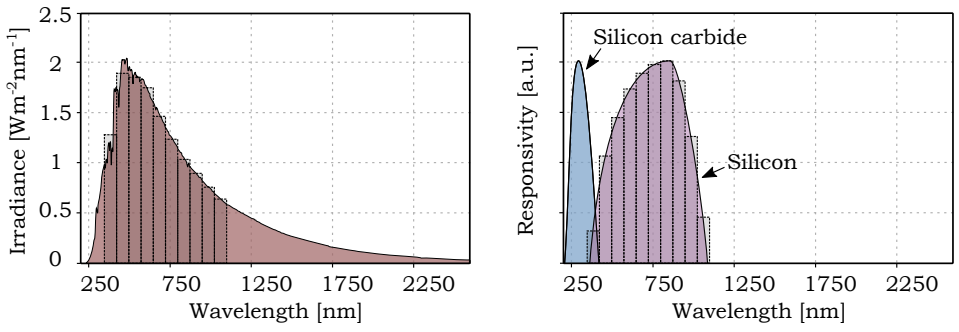
$$I_0 = A_{\text{tot}} \int P_{\text{opt}}(\lambda) R(\lambda) \, d\lambda. \tag{2.28}$$

However, this relation requires a continuous $P_{\text{opt}}(\lambda)$ and $R(\lambda)$, while these are typically based on measured data points. The integral is therefore rewritten using a uniform Riemann sum[6], which yields

$$I_0 \approx A_{\text{tot}} \sum_{i=1}^{N} P_{\text{opt}}\left(\lambda_i^*\right) R\left(\lambda_i^*\right) \Delta\lambda, \tag{2.29}$$

where i iterates through the discrete wavelengths and N is the total amount of wavelengths. The wavelength step size $\Delta\lambda$ is obtained by $\Delta\lambda = \lambda_i - \lambda_{i-1}$ and $\lambda_i^* \in [\lambda_{i-1}, \lambda_i]$. Often used values for λ_i^* are either the left, middle or right side of the range, which all give the same result in the limit where N goes to infinity. However, in the estimations in this work, N will be relatively low. Therefore, the midpoint Riemann sum is considered, since it is intuitively more accurate for low N. For this type of Riemann

[6] Uniform Riemann sums are approximations of the area below a curve by the summation of rectangles of equal width below the curve.



(a) (b)

Figure 2.23: The photo current is estimated by the multiplication of a) the solar spectrum [17] (see Figure 1.5 for more detail) and b) the typical silicon and silicon carbide photodetector responsivities. A uniform midpoint Riemann sum ($N = 10$) is illustrated for the silicon range and the responsivities are normalized for readability.

sums $\lambda_i^* = \lambda_{i-1} + \frac{\Delta\lambda}{2}$ and is used in further mentions in this work. The typical spectra of $P_{\text{opt}}(\lambda)$ and $R(\lambda)$ for silicon and silicon carbide photodetectors are illustrated in Figure 2.23, including the illustration of a low N uniform midpoint Riemann sum for the silicon photodetector case. The photodetector responsivity values are typically measured and reported in literature, but is physically defined by

$$R(\lambda) = \eta(\lambda)\frac{q\lambda}{hc}, \tag{2.30}$$

where $\eta(\lambda)$ is the quantum efficiency, q the elementary electric charge, h Planck's constant and c the speed of light [18, 19].

2.4.2. ABSORPTION, REFLECTION AND TRANSMISSION IN THE OPTICS

Now that a strategy for photo current estimation is given, it is necessary to investigate what losses exist for light that travels through the optics and into a photodetector to generate the photo current. This is dictated by the quantum efficiency, which is generally defined by taking the external quantum efficiency (EQE) as

$$\eta_{\text{EQE}}(\lambda) = \frac{\text{generated electrons/sec}}{\text{incident photons/sec}} = \frac{I_{\text{gen}}(\lambda)}{P_{\text{inc}}(\lambda)}\frac{hc}{q\lambda}, \tag{2.31}$$

where I_{gen} is the generated photo current and P_{inc} the incident optical power. Note that $\eta_{\text{EQE}}(\lambda)$ is dimensionless and typically lives in the range of $[0,1]$. The key parameter in the EQE to further look at in order to identify signal losses is P_{inc}, which is divided in the three parts as a result of interaction with the optics by

$$P_{\text{inc}}(\lambda) = P_{\text{ref}}(\lambda) + P_{\text{tran}}(\lambda) + P_{\text{abs}}(\lambda), \tag{2.32}$$

where $P_{\text{ref}}(\lambda)$ is the reflected optical power by the optics, $P_{\text{tran}}(\lambda)$ the transmitted optical power and $P_{\text{abs}}(\lambda)$ the absorbed optical power in the optics. Of course, to maximize the generated photo current (and as a result maximize $\eta_{\text{EQE}}(\lambda)$ and $R(\lambda)$) it is necessary to maximize $P_{\text{tran}}(\lambda)$ within the spectral range of interest. As such, it makes sense to define an internal quantum efficiency (IQE) as

$$\eta_{\text{IQE}}(\lambda) = \frac{\text{generated electrons/sec}}{\text{transmitted photons/sec}} = \frac{I_{\text{gen}}(\lambda)}{P_{\text{tran}}(\lambda)}\frac{hc}{q\lambda}. \tag{2.33}$$

Here, the quantum efficiency is only dependent on light that actual reaches the photodetector and it holds that $\eta_{\text{IQE}}(\lambda) \geq \eta_{\text{EQE}}(\lambda)$ within the same range. With the reflection and absorption of the optics no longer considered, it must be noted that reflection from the photodetector surface itself is still factored in. To reduce the lost signal from reflection from the photodetector, an anti-reflection coating (ARC) is a commonly applied additional layer on the device surface. Though UV light tends to be absorbed by many ARC for other spectral bands, some candidates are identified such as SiO_2 and Al_2O_3 [20, 21]. Other means of improving the EQE and IQE are by using avalanche photodetectors, which multiply the electron generation, or by addition of microlenses [22], which capture and focus more incident photons.

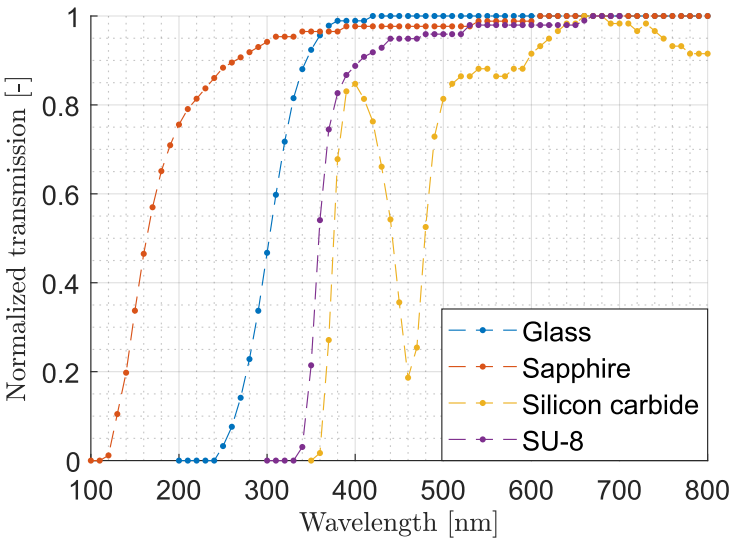
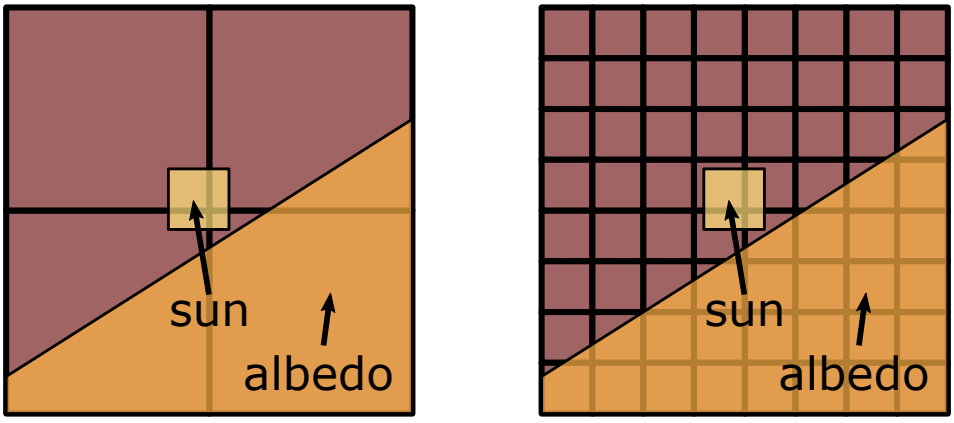


Figure 2.24: Normalized transmission spectra of different transparent materials, including glass [23], sapphire [24], silicon carbide [25] and SU-8 [26]. The data was extracted for plotting and normalizing in the same range, note that in the limits for no transmission and high transmission data is missing and considered to have reached a constant value. Drop-off behavior in the far infrared is not included, as it is outside the region of interest for this work.

Focusing on the optical windows in the discussed architectures for the UV range <300 nm of interest, several different candidates are identified and the spectral transmission is given in Figure 2.24. One would typically consider a glass type for the optical window, but for the Corning glass used here it is clear that the UV transmission is severely limited. However, a well-known material for optics in the UV range is sapphire, which indeed is shown to transmit light much deeper into the UV range. Alternatively, spin coated transparent polymers like SU-8 would work for the visible range, but have UV transmission worse than glass. Finally, one could consider the transparent substrate itself as the optical window to effectively use backside illumination of the photodetectors. Unfortunately, the silicon carbide substrate does not provide optical transmission in the UV range. Alternatively, advanced technologies that allow for thin epitaxial silicon carbide layers directly on top of sapphire substrates would still allow for the backside illumination approach. However, such technologies are not available at present, though it is a proven concept for silicon directly on sapphire substrates [27].

2.4.3. EFFECT OF THE ALBEDO

Visible blindness is often defined as the ratio between generated signal at two fixed wavelengths, which gives an indication of the visible blindness but is not a complete representation when considering broadband sources like the albedo. As such, in this work an albedo rejection ratio (ARR) is defined by



(a) (b)

Figure 2.25: Schematic illustration of worst case distortion situation by the albedo for a) the quadrant sun position sensor and b) the pixel array sun position sensor. These situations occur at sunrise or sunset conditions and capture the full image of the sun, but only a fraction of the image of the Earth.

$$\Psi_{\text{ARR}} = \frac{I_{\text{solar}}}{I_{\text{albedo}}}, \tag{2.34}$$

where I_{solar} and I_{albedo} are the photo currents generated considering the solar or albedo spectral irradiance respectively. As the I_{albedo} is by definition a fraction of I_{solar}, it follows that $\Psi_{\text{ARR}} > 1$. Furthermore, the factor $\Psi_{\text{ARR}} > 1$ is a worst case lower limit when considering the completed device, as it will never capture both the complete image of the sun and the Earth in the same field-of-view. A typical worst case situation for the sun position sensors is depicted in Figure 2.25, which occurs only at sunset or sunrise conditions. It is clear that only a fraction of the albedo is contributing to distortions and this fraction is highly dependent on the device geometry, but also satellite location in terms of distance from the Earth. These application specific effects are challenging to estimate and thus are not included in Equation 2.34.

Finally, reflections from structures on the satellite can be captured by the sun position sensor, which are similar to the albedo distortion. As such they are not further considered in this work.

2.5. CONCLUSION

This chapter provided design and modelling of three sun position sensor architectures. This included the quadrant, pixel array and diffraction grating sun position sensor architectures. In each device, aspects such as the effects of scaling geometry parameters, fabrication non-idealities or signal discretization effects are discussed, but also the readout procedure is given.

The quadrant sun position sensor leading design parameters are FoV, sensitivity and accuracy, for which respective relations are derived. The sensor readout methodology is based directly on the magnitude of the currents generated by each quadrant photode-

tector, which first need to be compared to identify the dominant quadrant and assign the corresponding function of each photodetector. In each case three of the four photodetectors are used to derive ratios, which are used to calculate the position of the light spot that is then used to calculate the angle information. This readout scheme is complemented by calibration constants, that account for photodetector current generation mismatch and overlay misalignment of the aperture. The calibration is demanding, as it requires angular response data in each quadrant and must be performed for each individual device. However, the calibration can be skipped if the design requires only a course sun position sensor, or if the fabrication of the device ensures a maximum mismatch factor of 4 %. Finally, it is identified that this sensor architecture is fundamentally subjected to a finite resolution by measurement or comparison of each photodetector output. As such, this resolution is explored and indicates that a fine position sensor requires at least 50 quantization levels in the measured range. Further effects from system non-idealities are not explored.

The pixel array sun position sensor relies on the same design parameters as the quadrant architecture counterpart, with minor difference for the FoV and the addition of the amount of pixels. Its readout relies on a centroid algorithm, which operates on the weighted average of the pixel coordinates by means of the signal generated in each pixel. Using similar geometry as the quadrant sun position sensor, the pixel array sun position sensor reached an ideal FoV. This is however at the cost of some accuracy, which is degraded most at the FoV limits. By limiting the FoV just larger than the quadrant sun position sensor achieves and using the same pixel readout resolution, the accuracy of a fine sun position sensor is achieved at an 8×8 array size. Finally, the effect of aperture misalignment is high and demands calibration, which can also be done through optical measurement of the absolute overlay shift.

A completely different approach is implemented by means of diffraction gratings that are spaced much closer to the photodetector, effectively omitting the need for an optical window to be added during the device fabrication. The explored topology is the amplitude grating approach, where each pixel is combined with a unique stack of diffraction gratings and is directly angle sensitive. A monochromatic light source is considered in this evaluation, while it must be noted that the pixel response will change for different wavelengths. Further research into broadband light sources is therefore required to truly enable application as a sun position sensor. The device readout demands differential outputs to obtain the angle information and remove the intensity information, similar to the quadrant sun position sensor readout. This is implemented by using four pixels with incremented phase difference in the grating stack. The implementation suffers from large offsets at the limits, caused by sharp transition points in its periodic response. To counteract this problem, one can run a second algorithm on the same hardware that yields a phase shifted response.

Finally, radiometry considerations are provided in order to estimate the generated photodetector signal. This is accompanied by the distinction between external and internal quantum efficiency, and the comparison of the optical transmission of several material options. The best suited material for optical windows in the targeted UV application is sapphire. A figure-of-merit for the albedo rejection ratio is defined, with indication of the nature of the signal distortion caused by the albedo.

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3

Integrated Devices and Circuits in Silicon Carbide

If I have seen further than others,
it is by standing upon the shoulders of giants.

Isaac Newton

The famous words in the quote above by Sir Isaac Newton, who can be considered a giant himself, beautifully capture the starting point of this chapter. As no established silicon carbide technology was available in-house at the start of this research work, one option would have been to develop a new technology for use in the implementation of the sun position sensor. Alternatively, extensive research opened up collaboration with Fraunhofer IISB in Germany, who successfully developed an open silicon carbide CMOS technology. As such, their technology is used for integrated devices and circuits in this chapter, in order to explore the capabilities and to use it for the sun position sensor implementation. As comparison and for risk management, most devices and circuits are first implemented in the comparable in-house silicon CMOS technology.

Parts of this chapter have been published in 2021 IEEE 34th International Conference on Micro Electro Mechanical Systems (MEMS) (2021) [1], IEEE Sensors conference (2021) [2] and IEEE Transactions on Electron Devices (2022) [3].

INTEGRATED circuits in silicon carbide have attracted research interest over a variety of transistor types since the early 90s. The preferred transistor technology in modern silicon technologies is complementary metal-oxide-semiconductor (CMOS), so it makes sense that the majority was focused on implementing this in silicon carbide. A decade ago, Raytheon Systems Limited developed a proprietary 1.2 µm SiC CMOS technology, called HiTSiC, and demonstrated SiC integrated circuits [4–6]. In this technology, the group of Mantooth at the University of Arkansas demonstrated a comparator [7], gate driver [8], 8-bit digital-to-analog converter (DAC) [9], voltage and current references [10], complex digital circuits [11], protection circuits [12], digitally controlled PWM generator [13], gate driver [14] and data converters [15]. However, the HiTSiC technology was discontinued in 2018, which hinders researchers to reproduce these results and explore the capabilities further. Other in-house SiC CMOS technologies are reported by General Electric Global Research Center in the United States of America for example [16–18], but in strong contrast with silicon services like Europractice, accessible SiC CMOS fabrication technologies are scarce to non-existent.

Alternatively, other transistor technologies are being researched. By far the best example of this, is the promising SiC bipolar junction transistor (BJT) technology for high temperature and harsh environments, called HOTSiC, developed by the group of Zetterling at the KTH in Sweden [19, 20]. It is implemented by mesa etching in a complex epitaxial layer stack on top of a monocrystalline 4H-SiC wafer. In this technology, an OR/NOR gate [21], ECL-based logic circuits [22, 23], operational amplifier [24], differential amplifier [25], high current linear voltage regulator [26] and 8-bit DAC [27] were implemented and characterized up to 500 °C. Other examples are results in junction field-effect transistor (JFET) [28, 29] and metal-semiconductor field-effect-transistor (MESFET) [30, 31] technologies. These technologies are researched in favor of stable operation at high temperatures. Although the CMOS gate dielectric reliability has been a concern [32, 33], more recent work contradicts the poor reliability prediction and suggests much longer lifetimes [34, 35]. Moreover, CMOS technologies are typically preferred in mixed-signal circuit designs and have lower power consumption.

More recently, a promising new and open SiC CMOS technology candidate arose. This state-of-the-art 4H-SiC CMOS process [36, 37] was developed by the Fraunhofer Institute for Integrated Systems and Devices Technology (IISB), based in Erlangen, Germany. Using this technology, the group of Mantooth at the University of Arkansas already reported high temperature memory SRAM cells [38]. This technology is adopted in this research work, as a strong foundation towards the implementation of integrated circuits for the sun position sensor. As the present lead time for the Fraunhofer IISB CMOS fabrication process is close to one year and the fabrication is costly, the in-house silicon CMOS technology is used as a test vehicle. This allows for risk management, by identification and correction of layout errors that may arise due to the lack of full design kits. At the same time, some comparisons can be made between the two platforms.

This chapter starts by providing the employed measurement setup design and used methodology. Concurrently, fabrication overviews and comparisons are given of the in-house BICMOS7 and Fraunhofer IISB SICCMOS9 technologies. Then, a section is dedicated to circuit block design and characterization. Finally, the effects of elevated temperature are investigated and discussed, before concluding the chapter.

3.1. MEASUREMENT SETUP DESIGN AND METHODOLOGY

The designed structures are electrically characterized in-house using DC analysis and transient analysis on either wafer-level or chip-level. Depending on the configuration used, the measurements are automatic, semi-automatic or completely manual. The different approaches are described in this section as well a the data visualization and analysis software tool that was developed in this project.

3.1.1. APPROACHES FOR DIFFERENT ANALYSIS TYPES

The wafer is probed using a MicroTech Cascade probe station, which is fitted with 7 probe needles and has a temperature controlled chuck in the range of 0–200 °C. For DC analysis, this is paired to an Agilant 4156C Precision Semiconductor Parameter Analyzer, which offers 4 high-resolution source-measurement units (HRSMU), 2 voltage source units (VSU) and 2 voltage measurement units (VMU). The system is controlled through a PC running IC-CAP measurement software. An overview picture is provided in Figure 3.1. The system allows for fully automatic operation, if the user provides the measurement locations and specific measurements to run beforehand.

The parameter analyzer is not capable of transient response measurement, which requires a fitting different tool to be paired with the probe station setup. Making use of what is commercially available, a data acquisition tool (DAQ) from National Instruments is a commonly used solution. However, these cards are limiting in terms of the voltage range and amount of addressable pins, as the technology signal range is 10 V or 20 V for the silicon or silicon carbide platforms respectively. For this reason, a simple custom DAQ is developed for the transient response analysis, of which a schematic overview is provided in Figure 3.2. The measurements are controlled and visualized in a MATLAB GUI on a laptop, which communicates with the microcontroller in the separate interface box through USB. Analog 5-to-10 V and 10-to-5 V level-shifters are implemented by the

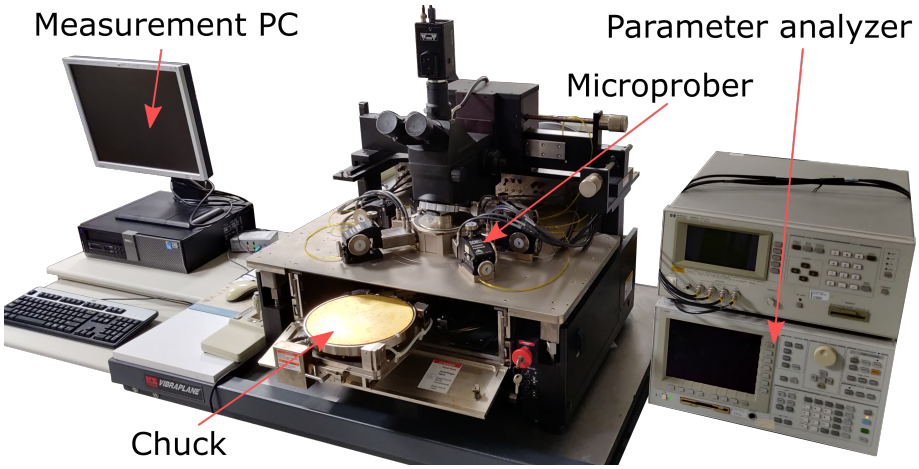


Figure 3.1: Picture of the probe station setup for wafer-level measurements, with annotations of the relevant components. The probe station is used for automatic DC and semi-automatic transient analysis.

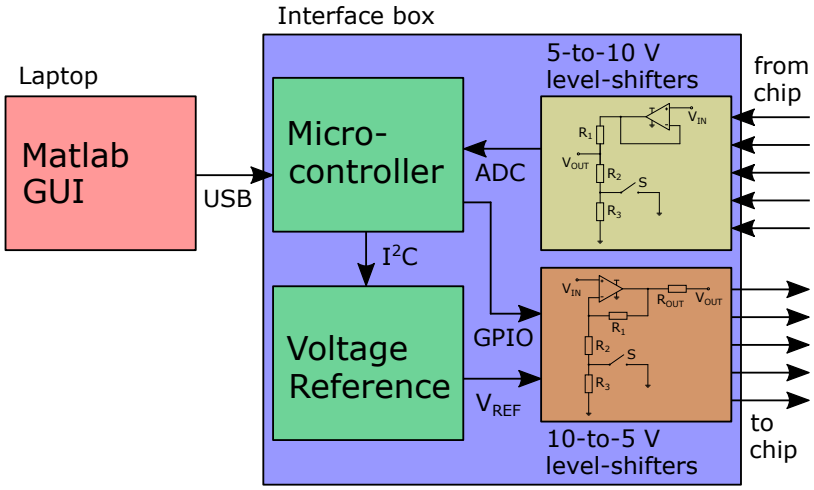


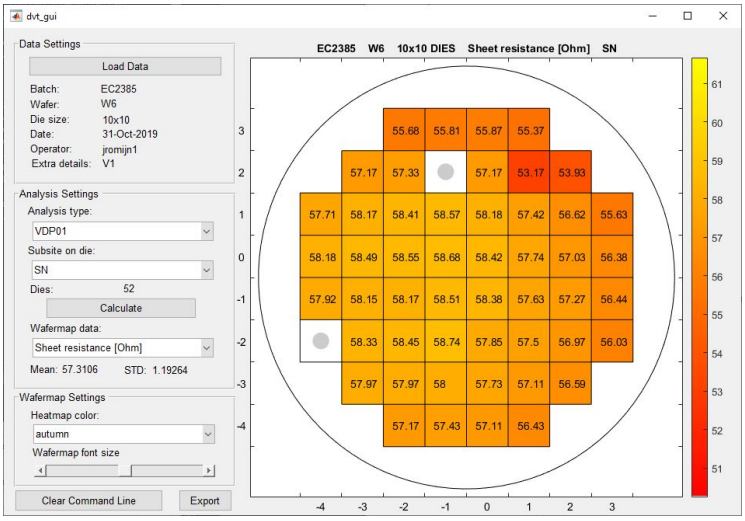
Figure 3.2: Schematic overview of the custom DAQ tool functional blocks for transient analysis. Inside the interface box is an ATMEGA2560 microcontroller, which holds the measurement code and stores measurement results locally in its flash storage. Each level-shifter is present twelve times in the interface box and uses LM358 industry standard dual operational amplifiers [39] and resistor values $R_1 = 30\,\text{k}\Omega$, $R_2 = 10\,\text{k}\Omega$, $R_3 = 20\,\text{k}\Omega$ and $R_{\text{OUT}} = 100\,\text{k}\Omega$. The R_{OUT} resistor is in place as over-current protection. The voltage reference is implemented by a MCP4725 board, that houses a 12-bit DAC.

illustrated circuits on printed circuit boards and can alternatively be configured as 5-to-20 V and 20-to-5 V using jumpers (Figure B.2). A separate voltage reference provides a stable output for bias pins. The custom DAQ is not compatible with the automatic measurements and reduces it to semi-automatic measurements, where the system can automatically cycle through all wafer locations, but requires an operator to start and stop each measurement.

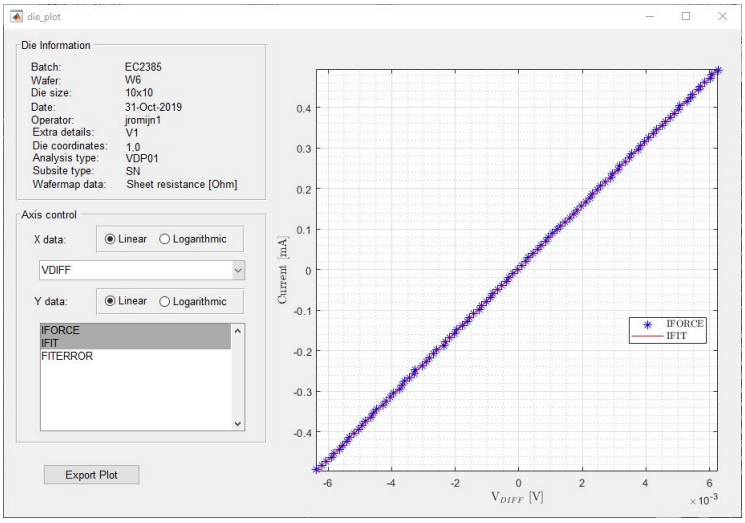
After dicing the wafer, the individual chips are to be packaged for further characterization. The system-on-chip (SoC) design is anticipated to include a large amount of connections, especially considering intermediate signals for verification of the system operation. A suitable package for chip-level measurements should allow ease of mounting in specific setups in this research work, such as optical or thermal characterization. Therefore, a ceramic pin-grid array (CPGA) package [40] is employed that includes 64 pins and allows chip sizes up to $10 \times 10\,\text{cm}$. This ensures a small footprint, plenty of connections and wide temperature range of operation. To interface with this specific package, an interface PCB including an 11×11 zero insertion force (ZIF) socket [41] was implemented (Figure B.3) that allows for fast re-configuration of the measured pins. For effective chip-level measurements, it is vital to perform thorough bookkeeping of all the signals in play.

3.1.2. DATA VISUALIZATION AND ANALYSIS TOOL

To interpret the many data files a custom data visualization and analysis tool (DVT) is used, which is implemented by a graphical user interface (GUI) in MATLAB. A key aspect of the developed tool is the high level of modularity, allowing the analysis of many



(a)



(b)

Figure 3.3: Overview of the DVT MATLAB GUI (version 0.4.3), showing example data. The GUI consistst of two parts, which are a) the main window to select the data and view key parameters on wafer-level and b) the individual die plot for in depth analysis. Insight in the structure of the tool is listed in Figure B.1. The grey dots mark broken chips.

different devices as well as measurement types. An example is visualized in Figure 3.3 using sheet resistance data. The wafermap displays a heatmap of the derived resistance with mean and standard deviation, allowing identification of potential gradients due to fabrication process steps. It also indicates if any of the measured chips was broken and clicking on a chip gives the measured data curve for closer inspection.

3.2. TECHNOLOGY OVERVIEW AND PARAMETERS

The silicon carbide CMOS process at Fraunhofer IISB is comparable to the in-house silicon CMOS process, considering aspects such as feature size, design layers, design approach and higher supply voltage level than conventional. This in-house silicon technology is therefore used for rapid prototyping, which is not possible in the silicon carbide process due to higher cost and longer lead time. The two processes are named by the technology type and amount of design layers. The in-house silicon technology includes BJT and CMOS in seven design layers (BICMOS7) and the Fraunhofer IISB silicon carbide technology includes CMOS in nine design layers (SICCMOS9).

3.2.1. THE SILICON BICMOS7 PROCESS

The BICMOS7 technology [1, 42–44] is a robust and simple 1 µm technology, used for educational purposes and basic circuit design. It implements both BJT and CMOS devices, operates at a power supply voltage of 10 V and requires only seven masks for lithography. All circuit design in this research work used only CMOS topologies, thus the fabrication steps for BJT specific devices are left out. Due to its robustness, the BICMOS7 technology lends itself for integration of new fabrication processes, such as the integration of graphene [45]. The seven core fabrication steps of the BICMOS7 technology are schematically illustrated in Figure 3.4, which are the n-well (NW), shallow n-type (SN), shallow p-type (SP), contact openings (CO), first metal interconnect layer (M1), contact via openings (VI) and second metal interconnect layer (M2). The detailed fabrication steps are listed in the flowchart in Appendix E.1. The process starts with bare p-type 100 mm silicon wafers with a highly uniform background dopant concentration, provided by an epi-layer.

The single-well front-end-of-line (FEOL) fabrication entails the implementation of the doped regions and consists of the NW, SN and SP steps. The n-well, shallow n-type and shallow p-type regions are implemented by phosphorus ion (P^+), arsenic ion (As^+) and boron ion (B^+) implantation respectively. The P^+ ions are implanted and diffused deep in the silicon substrate to form a well. The concurrent As^+ and B^+ ion implantations form highly doped shallow regions. The FEOL ends with the thermal growth of SiO_2 as a dielectric material that is used both as the gate dielectric and the field oxide.

The two-level metal back-end-of-line (BEOL) starts with the formation of the contact openings to the doped regions. The first metal interconnect layer is then implemented using aluminum with 1 % silicon (AlSi(1 %)). The silicon ensures no diffusion into the substrate so no spiking[1] can occur. This is followed by the tetraethylorthosilicate (TEOS) plasma-enhanced chemical vapor deposition (PECVD) to form another SiO_2 dielectric layer. The TEOS plasma reacts at the exposed wafer surface and forms SiO_2 directly. Vias are implemented in this dielectric to contact the first metal layer. Finally, another AlSi(1 %) layer is used to implement the second metal interconnect layer. Each of the seven core fabrication steps in BICMOS7 requires a separate lithography mask to pattern the structures. The mask set of the full design in this technology is given in Figures B.4 and B.5.

[1] Spiking is the effect of Al atoms diffusion into the silicon substrate, which can cause short circuits to other doped regions.

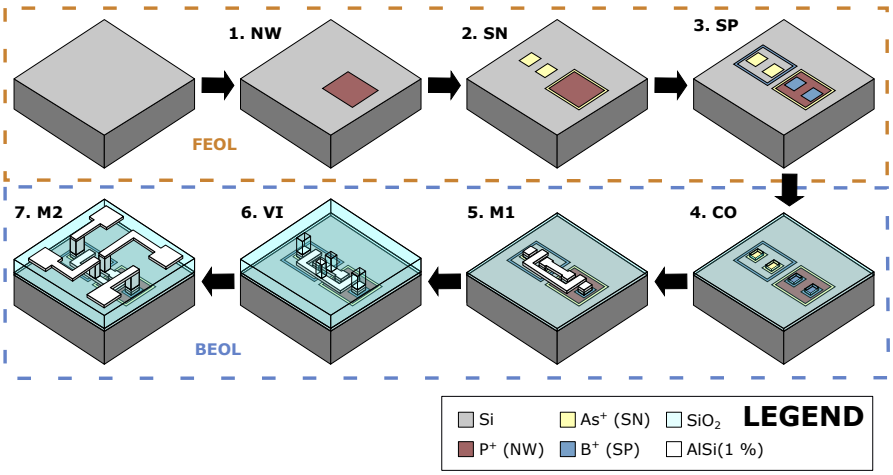


Figure 3.4: Schematic illustration of the fabrication steps of the BICMOS7 technology. The FEOL includes the definition of the doped NW, SN and SP regions. The BEOL includes the definition of the two metal interconnect layers, with corresponding contact openings and vias. Note that each of the depicted steps requires a mask for lithography (adapted from earlier work [1, 44]).

3.2.2. THE SILICON CARBIDE SICCMOS9 PROCESS

The SICCMOS9 technology [3, 36, 37] is a state-of-the-art SiC CMOS technology, operating at a power supply voltage of 20 V and used for research on integrated circuits and sensors in silicon carbide. To accommodate the fabrication costs, multi-project designs are run. It includes nine design layers that are very similar to the BICMOS7 technology. The major differences are the addition of the p-well, an active area to define the thinner gate oxide, the polysilicon gate material and the use of silicides in the contact openings. The nine core fabrication steps of the SICCMOS9 technology are schematically illustrated in Figure 3.5, which are the n-well (NW), p-well (PW), shallow n-type (SN), shallow p-type (SP), active area (AC), polysilicon layer (PO), contact openings to the substrate (CO), contact openings to the polysilicon (PC) and first metal interconnect layer (M1). The process starts with bare n-type 350 µm thick four inch 4H-SiC wafers with a highly uniform 1–2 µm epitaxial n-type $> 1 \times 10^{18}$ cm^{-3} buffer layer and an 8 µm epitaxial n-type 5×10^{14} cm^{-3} top layer.

The double-well FEOL implements the doped regions by ion implantation, forming the n-well, p-well, shallow n-type and shallow p-type regions, which are activated by a 1700 °C anneal for 30 min. The NW and SN are formed by N^+ implantation and the PW and SP by Al^+ implantation. The active area region is implemented by wet etching the field oxide at ohmic contact and MOSFET channel locations, followed by thermal gate oxidation. The resulting gate oxide thickness is 50 nm and the field oxide is 400 nm. Note that this implies there is no form of shallow trench isolation to prevent latch-up of MOSFET devices.

The single-level BEOL starts with the implementation of a 500 nm polysilicon layer, for the gate and short interconnects. An oxide passivation layer of 400 nm is deposited followed by the definition of ohmic contacts to the SN and SP regions in two steps. First,

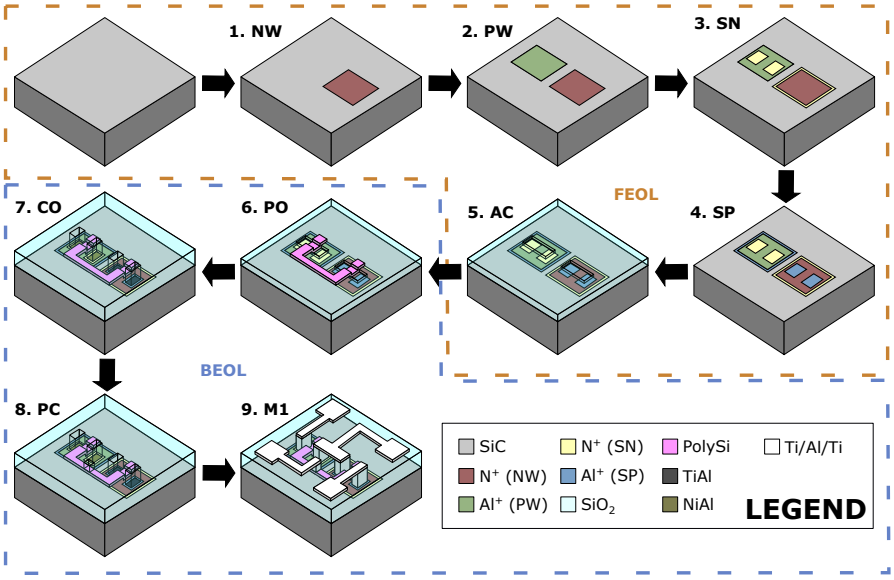


Figure 3.5: Schematic illustration of the fabrication steps of the SICCMOS9 technology [3]. The FEOL includes the definition of the doped NW, PW, SN and SP regions, as well as the definition of the active area. The BEOL includes the definition of the polysilicon and metal interconnect layer, with corresponding silicide contacts and vias. Note that each of the depicted steps requires one or more masks for lithography.

the openings to the SP layer are opened using a lithography mask, which is followed by the deposition and patterning of 80/300 nm Ti/Al inside the openings. The procedure is repeated to form the openings to the SN layer and implements 50 nm NiAl patterns inside these openings. Rapid thermal annealing (RTA) at 980 °C is employed to form silicides in the contact openings, which ensures ohmic contacts from the metallization stack to the doped regions in the substrate. This is possible due to the high thermal stability of the present layers other than the contact metals. The final result is shown in Figure 3.6. It should be noted that the patterned area of the metals in the contact openings is smaller then the etched openings, to avoid diffusion of these metals between the SiC-SiO_2 interface, and generally into the SiO_2 during the RTA. As a result, the CO design layer actually requires three separate lithography masks. Other metal stacks are investigated by Fraunhofer IISB [46] and ideally a single stack could be used to contact to both the SN and SP regions simultaneously. The process continues by opening the contacts to the polysilicon and is completed by deposition and patterning of a 50/700/20 nm Ti/Al/Ti interconnect layer. This reduces the thermal budget to 400 °C and should be adhered to in future implementations of multiple metal interconnect layers.

The fabrication process can be taken over from Fraunhofer IISB in EKL only after the RTA is done, as this is one of the processes that the EKL facilities are lacking. However, this does open up the possibility to add high temperature fabrication steps at EKL before the metallization. Moreover, a second metal layer can be added at EKL using the VI and M2 design layers from the BICMOS7 technology (upgrading to SICCMOS11), to implement denser interconnect and metal-insulator-metal (MIM) capacitors. The mask

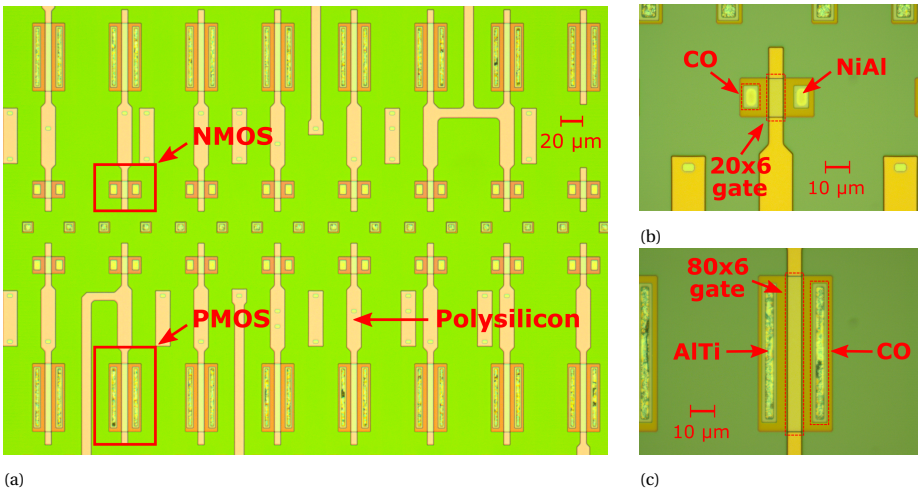


Figure 3.6: Fabrication result in silicon carbide after step 8 (PC), as illustrated in Figure 3.5, of a) multiple devices, b) a single 20x6 NMOS and c) 80x6 PMOS device [3]. The formed silicides inside the contact openings are clearly visible. Note that none of the implanted regions can be observed.

set of the M1 layer at EKL facilities is given in Figure B.6, which uses ASML markers inside the multi-project design space for alignment and separately exposes parts of the multi-project design space using a custom stepper job.

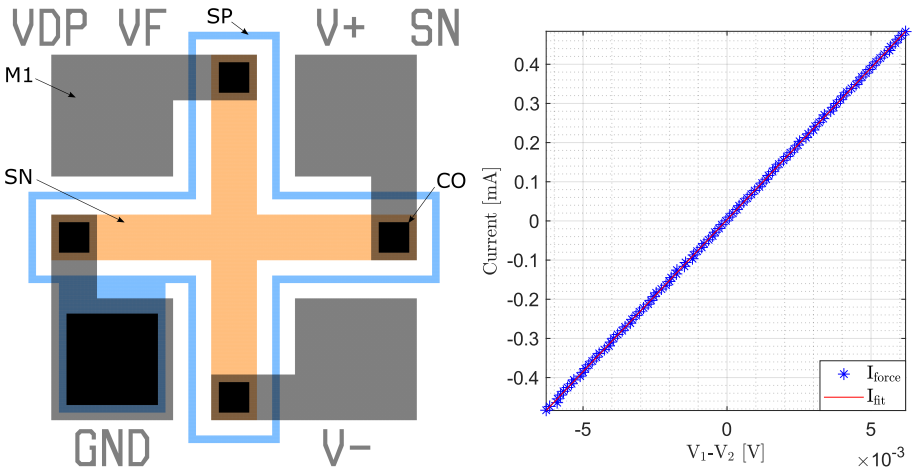
3.2.3. COMPARISON OF TECHNOLOGY PARAMETERS

To investigate key technology parameters, test structures are included on process control modules (PCMs). The BICMOS7 PCM (Figure B.7) is part of the designed chip area and thus included on each silicon chip in this work. On the other hand, the SICCMOS9 PCM is divided in two parts, PCM A (Figure B.8) and PCM B (Figure B.9), and on separate chips on multi-project wafers. To start, the resistance of the doped layers and interconnect layers is investigated. A key parameter for this is the sheet resistance[2], which is measured here using Van der Pauw Greek cross structures (Figure 3.7a) and extracting the IV curves (Figure 3.7b). The resistance that is extracted from the IV curve is multiplied by a correction factor to find the sheet resistance through

$$R_{\square} = \frac{\pi}{\ln(2)} R_x, \tag{3.1}$$

where R_x is the resistance extracted from the IV curve. The sheet resistances are extracted on wafer level (Figures F.1 to F.10) and the values are listed in Table 3.1. All doped layers have much higher sheet resistances in SICCMOS9, which negatively impacts the CMOS devices by increased resistance in the source and drain area. Reasons for this higher resistance are the much lower intrinsic carrier concentration in SiC and the higher ionization energies of the doped regions [47]. This amounts to factors of 18 and 345 source/drain resistance increase for the NMOS and PMOS device respectively.

[2]Sheet resistance is the electrical resistance of a design layer with fixed thickness per square area in $\Omega\square^{-1}$.



(a) (b)

Figure 3.7: Example of the a) 4-probe Van der Pauw Greek cross structure of the SN layer in BICMOS7, with annotated layers. The SP guard ring ensures electrical insulation from other structures. Note that the probe pads are both in M1 and M2 layer to allow measurement at different stages in the fabrication (VI and M2 not shown in favor of readability). The corresponding measured IV curve in b), where the voltage is forced at VF and swept within the linear region of the structure and grounded at GND. The corresponding input current is measured at VF and the voltage drop at V+ and V-.

To verify the ohmic contacts to the SN and SP area, a 4-probe measurement is done on lines in these layers with fixed geometry. The total resistance is composed of the line resistance and two contacts, which gives a contact resistance of $(0.22 \pm 0.06)\,\mathrm{m\Omega\,cm^2}$ and $(16 \pm 11)\,\mathrm{m\Omega\,cm^2}$ for the SN-M1 and SP-M1 contacts respectively in BICMOS7 (Figures F.11 and F.12). The inferior contacts to the SP layer, are caused by over etching in this region due to asymmetry in the field oxide thickness for SN and SP regions. This could be improved by altering the process, by either changing the plasma etching step or by etching the SN and SP regions in separate steps. Similarly, a contact resistance

Table 3.1: Sheet resistance $R_{\square}$ of the relevant design layers in the BICMOS7 and SICCMOS9 technologies. Values are obtained from wafer-scale measurements on 52 and 35 dies on a BICMOS7 and SICCMOS9 reference wafer respectively. Note that the NW layer value in the SICCMOS9 technology could not be obtained, as it is implemented directly in the n-type epi-layer.

	BICMOS7	SICCMOS9
NW	$(1.69 \pm 0.02)\,\mathrm{k\Omega\,\square^{-1}}$	-
PW	-	$(431 \pm 19)\,\mathrm{k\Omega\,\square^{-1}}$
SN	$(57 \pm 1)\,\mathrm{\Omega\,\square^{-1}}$	$(1.03 \pm 0.01)\,\mathrm{k\Omega\,\square^{-1}}$
SP	$(117 \pm 33)\,\mathrm{\Omega\,\square^{-1}}$	$(40.4 \pm 1.3)\,\mathrm{k\Omega\,\square^{-1}}$
PO	-	$(14.0 \pm 0.1)\,\mathrm{\Omega\,\square^{-1}}$
M1	$(138 \pm 2)\,\mathrm{m\Omega\,\square^{-1}}$	$(47 \pm 3)\,\mathrm{m\Omega\,\square^{-1}}$
M2	$(22 \pm 4)\,\mathrm{m\Omega\,\square^{-1}}$	-

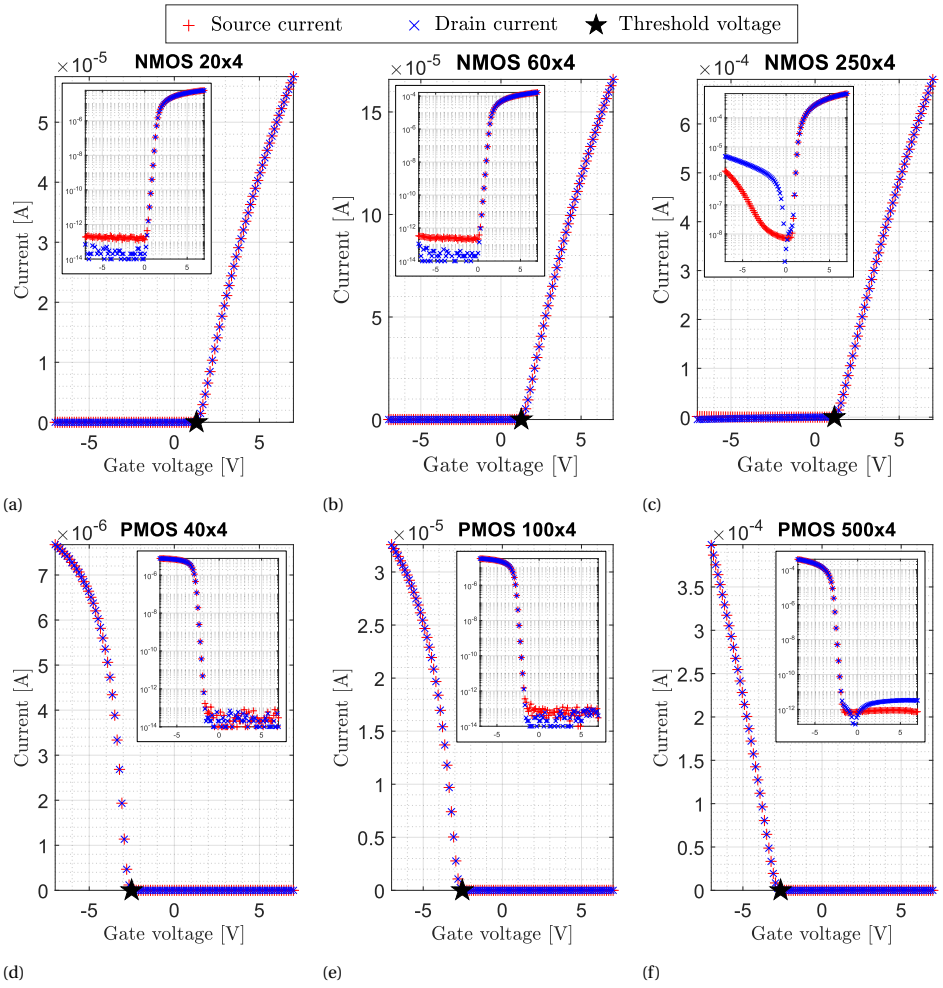


Figure 3.8: The measured I_{ds}/V_{gs} curves at room temperature with marked threshold voltage on die (0,0) of the a) 20 × 4 µm NMOS, b) 60 × 4 µm NMOS, c) 250 × 4 µm NMOS, d) 40 × 4 µm PMOS, e) 100 × 4 µm PMOS and f) 500 × 4 µm PMOS Si devices. The insets show the same data with logarithmic y-axis and the devices are biased in the linear region at 0.1 V and −0.1 V for NMOS and PMOS respectively.

of $(0.23 \pm 0.13)\,\mathrm{m\Omega\,cm^2}$ and $(0.75 \pm 1.22)\,\mathrm{k\Omega\,cm^2}$ for the SN-M1 and SP-M1 contacts respectively are found in SICCMOS9 (Figures F.13 and F.14). The SN-M1 contact resistance is similar, while the SP-M1 contact resistance is much worse in SICCMOS9 than the already bad contacts in BICMOS7. This is attributed to the inferior silicides in these regions, which can be improved by optimizing the RTA process or by choosing a different silicide material.

To evaluate the performance of the technology further, the NMOS and PMOS devices are investigated. The I_{ds}/V_{gs} curves of a selection of BICMOS7 NMOS and PMOS geometries are measured and depicted in Figure 3.8. The NMOS drain current scales

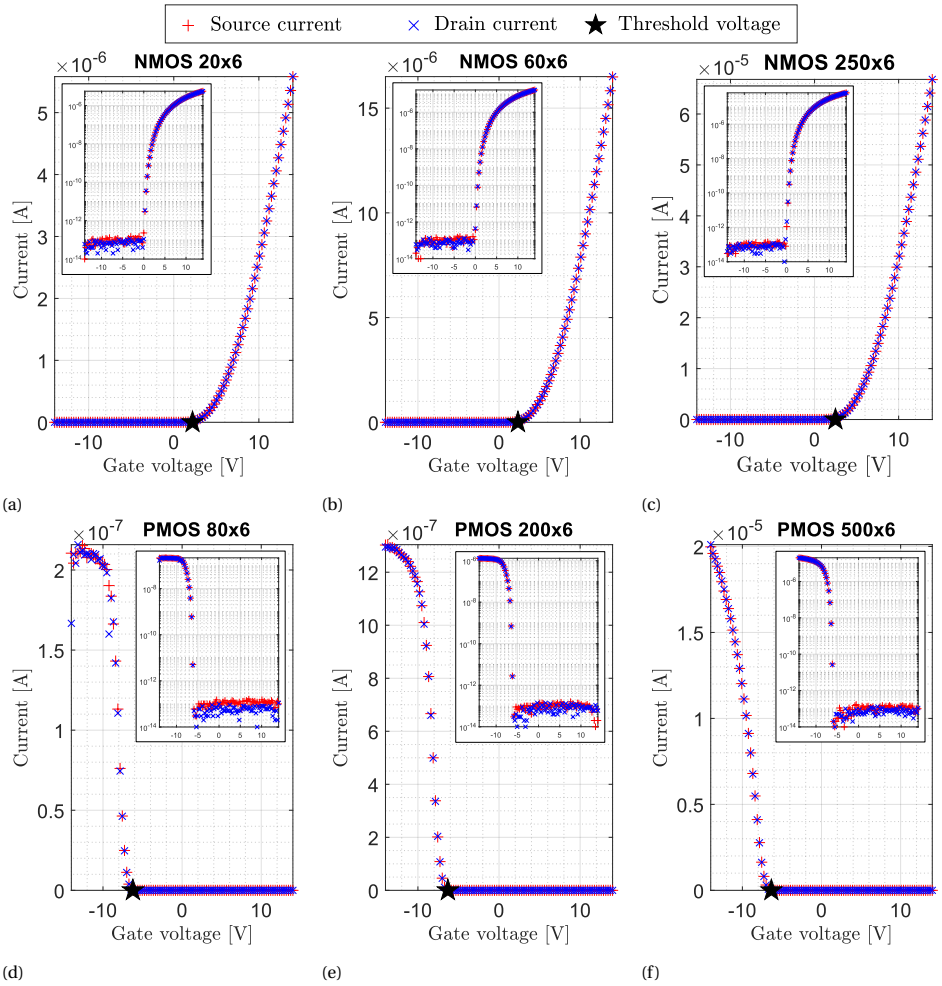


Figure 3.9: The measured I_{ds}/V_{gs} curves at room temperature with marked threshold voltage on die (0,0) of the a) 20 × 6 µm NMOS, b) 60 × 6 µm NMOS, c) 250 × 6 µm NMOS, d) 80 × 6 µm PMOS, e) 200 × 6 µm PMOS and f) 500 × 6 µm PMOS SiC devices. The insets show the same data with logarithmic y-axis and the devices are biased in the linear region at 0.2 V and −2 V for NMOS and PMOS respectively.

as expected with the W/L ratio, which is less evident for the PMOS as it shows saturation effects. This is attributed to the inferior contacts to the SP regions used for the source and drain of the PMOS device. The curves do show that this saturation effect is greatly reduced for increased W/L ratios, so that interfacing with off-chip loads is feasible (though recommended to ensure these loads have a high input impedance). Finally, the NMOS devices show leakage currents of 0.2 fA when the devices are off. This leakage is much larger for the 250 × 4 µm device, which is likely to be caused by the different layout used. This area optimized layout has parallel 'fingers' that implement the wide channel, which may suffer from depletion regions to partially punch through. The

PMOS does not show leakage, except for the largest geometry which again has parallel 'fingers' to optimize area, but even then it is nothing severe.

Similarly, the I_{ds}/V_{gs} curves of a selection of SICCMOS9 NMOS and PMOS geometries are measured and depicted in Figure 3.9. Again, the NMOS drain current scales as expected with the W/L ratio, while the PMOS shows saturation effects. These saturation effects are worse and are caused by the bad SP-M1 contact resistance. Fortunately, the effect is greatly reduced for larger W/L ratios, allowing off-chip interfacing. Related to this limited current driving capability is the increased V_{ds} bias of the PMOS, which reduces the saturation effect and allows extraction of some technology parameters. However, this increased bias will shift the threshold voltage towards more negative values and reduce the subthreshold swing. No leakage current is identified in the SiC devices, not even the ones with parallel 'fingers'. The reported asymmetry of the threshold voltages could be addressed in future work by means of a blanket p-type ion implantation to shift both NMOS and PMOS threshold voltages towards more positive levels, which is already used in the BICMOS7 fabrication (Appendix E.1).

To investigate further, the I_{ds}/V_{ds} curves for a selection of V_{gs} values and minimum size NMOS and PMOS devices are measured for both technologies and depicted in Figure 3.10. For BICMOS7, the NMOS and PMOS drain current shows both quadratic and linear increase in magnitude for lower and higher V_{gs} values respectively, illustrating that both saturation and velocity saturation are relevant. Similarly for SICCMOS9, the NMOS drain current shows both quadratic and linear increase, while the PMOS device behavior is close to a linear increasing drain current, indicating mostly velocity saturation. The unified model for manual analysis [48] is fitted to the curves by empirical determination of the fitting parameters. To achieve a good fit, the transition point from linear to saturation of the NMOS devices of both technologies and the BICMOS7 PMOS devices is moved to lower V_{ds} levels and the starting point of the SICCMOS9 PMOS fit is shifted to higher V_{ds} levels. This starting point shift for the SICCMOS9 PMOS also validates the higher V_{ds} used for the V_{th} extraction. Finally, the BICMOS7 NMOS devices indicate that drain current leaks away at higher drain-source bias, which is presumably due to the expanding depletion region at the drain contact.

For both technologies, the CMOS threshold voltages, subthreshold slopes, slope factors, process transconductances and mobilities are extracted from device measurements and reported in Table 3.2. The threshold voltages V_{th} are extracted (Figures F.15 to F.26) using the second-derivative method [49]. The absolute threshold voltages in SICCMOS9 are significantly higher, as well as the asymmetry between NMOS and PMOS. Concurrently, the subthreshold slopes S are extracted (Figures F.27 to F.38) by considering the maximum of the inverse slope of the drain current[3]. Another often used derivative of this parameter is the slope factor n, which is defined by

$$S = n\frac{kT}{q}\ln(10), \tag{3.2}$$

which for an ideal transistor ($n = 1$) evaluates to $60\,\mathrm{mV\,dec^{-1}}$ when at room temperature [48] and real transistors must have $n > 1$ at room temperature. The BICMOS7

[3]The subthreshold slope measures by how much V_{gs} has to be reduced for the drain current to drop by a factor of 10 and thus has the $\mathrm{V\,dec^{-1}}$ units.

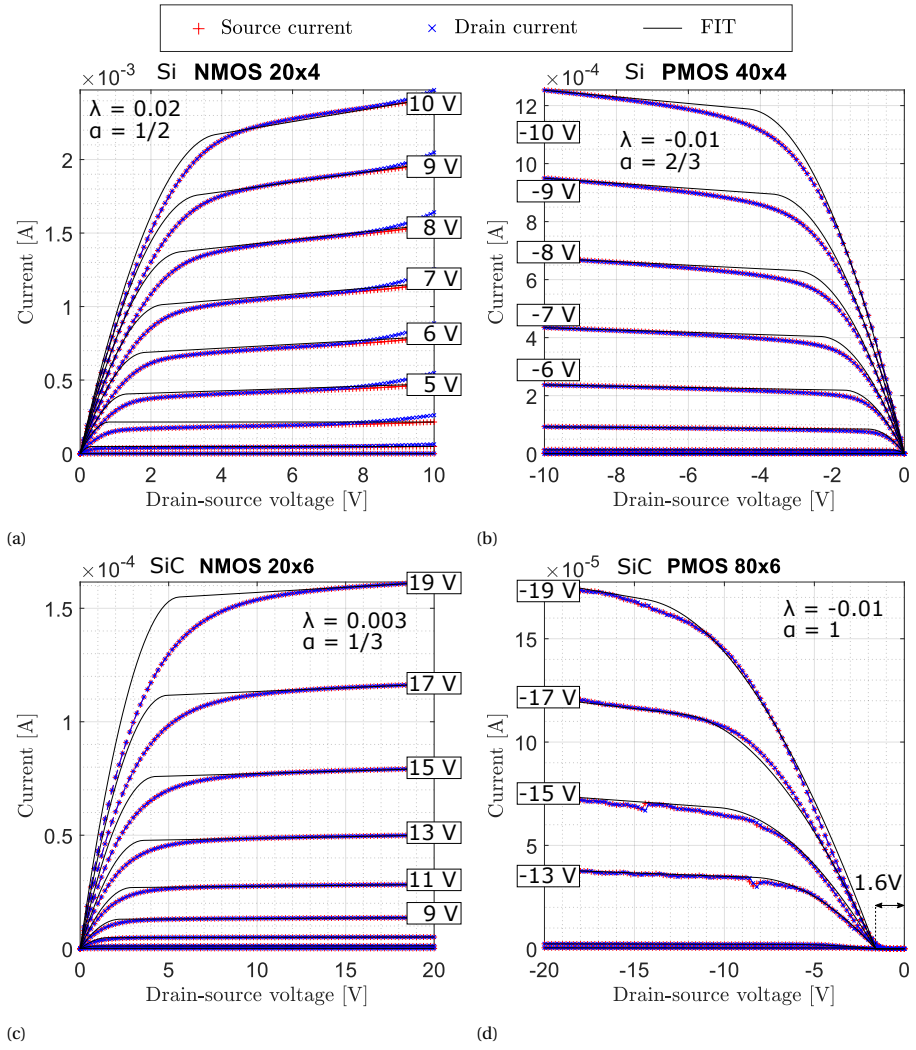


Figure 3.10: I_{ds}/V_{ds} curves on die (0,0) for a selection of V_{gs} values and a) 20 × 4 µm Si NMOS and b) 40 × 4 µm Si PMOS c) 20 × 6 µm SiC NMOS and d) 80 × 6 µm SiC PMOS devices. The curves are fitted to the unified model for manual analysis [48] and are achieved by assuming a $V_{dsat,n} = 2\,\text{V}$, $V_{dsat,p} = -1\,\text{V}$ and the λ annotated in the plots. To account for deviation in the linear region, the transition point in the NMOS curves is moved to lower V_{ds} by a factor α and the PMOS curves are shifted to higher V_{ds} by −1.6 V.

devices have values of n that are closer to the ideal value than the SICCMOS9 devices. However, both technologies are still far from established silicon based technologies [50, 51] that typically have $n < 2$. Next, the carrier mobilities μ are extracted (Figures F.39 to F.50) in the linear region using the relation

$$I_{ds} = \frac{W}{L}\mu C_0 \left(V_{gs} - V_{th}\right) V_{ds}, \tag{3.3}$$

Table 3.2: Mean values of the threshold voltage V_{th}, subthreshold slope S, slope factor n, mobility μ and process transconductance parameter k' at room temperature, derived from wafer-level I_{ds}/V_{gs} or I_{ds}/V_{ds} results of 52 and 35 dies from BICMOS7 and SICCMOS9 reference wafers respectively. The overall single device yield is high (> 96 %), for both technologies.

BICMOS7 NMOS devices			
size	$20 \times 4\,\mu m$	$60 \times 4\,\mu m$	$250 \times 4\,\mu m$
V_{th}	$(1.34 \pm 0.06)\,V$	$(1.30 \pm 0.06)\,V$	$(1.21 \pm 0.06)\,V$
S	$(0.15 \pm 0.02)\,V\,dec^{-1}$	$(0.15 \pm 0.02)\,V\,dec^{-1}$	$(0.11 \pm 0.03)\,V\,dec^{-1}$
n	2.5 ± 0.3	2.5 ± 0.4	1.9 ± 0.4
μ	$(637 \pm 49)\,cm^2\,V^{-1}\,s^{-1}$	$(612 \pm 34)\,cm^2\,V^{-1}\,s^{-1}$	$(632 \pm 8)\,cm^2\,V^{-1}\,s^{-1}$
k'	$(22.6 \pm 4.2)\,\mu A\,V^{-2}$	$(20.2 \pm 3.8)\,\mu A\,V^{-2}$	$(18.8 \pm 3.6)\,\mu A\,V^{-2}$
BICMOS7 PMOS devices			
size	$40 \times 4\,\mu m$	$100 \times 4\,\mu m$	$500 \times 4\,\mu m$
V_{th}	$(-2.50 \pm 0.04)\,V$	$(-2.50 \pm 0.03)\,V$	$(-2.58 \pm 0.02)\,V$
S	$(0.16 \pm 0.04)\,V\,dec^{-1}$	$(0.16 \pm 0.04)\,V\,dec^{-1}$	$(0.17 \pm 0.02)\,V\,dec^{-1}$
n	2.6 ± 0.7	2.7 ± 0.6	2.9 ± 0.4
μ	$(101 \pm 42)\,cm^2\,V^{-1}\,s^{-1}$	$(104 \pm 34)\,cm^2\,V^{-1}\,s^{-1}$	$(233 \pm 6)\,cm^2\,V^{-1}\,s^{-1}$
k'	$(16.9 \pm 8.5)\,\mu A\,V^{-2}$	$(16.1 \pm 8.1)\,\mu A\,V^{-2}$	$(15.6 \pm 7.8)\,\mu A\,V^{-2}$
SICCMOS9 NMOS devices			
size	$20 \times 6\,\mu m$	$60 \times 6\,\mu m$	$250 \times 6\,\mu m$
V_{th}	$(2.23 \pm 0.12)\,V$	$(2.39 \pm 0.12)\,V$	$(2.48 \pm 0.07)\,V$
S	$(0.20 \pm 0.03)\,V\,dec^{-1}$	$(0.20 \pm 0.01)\,V\,dec^{-1}$	$(0.18 \pm 0.02)\,V\,dec^{-1}$
n	3.4 ± 0.5	3.3 ± 0.2	3.1 ± 0.4
μ	$(14.2 \pm 2.6)\,cm^2\,V^{-1}\,s^{-1}$	$(14.5 \pm 0.4)\,cm^2\,V^{-1}\,s^{-1}$	$(14.5 \pm 0.3)\,cm^2\,V^{-1}\,s^{-1}$
k'	$(0.45 \pm 0.37)\,\mu A\,V^{-2}$	$(0.46 \pm 0.37)\,\mu A\,V^{-2}$	$(0.48 \pm 0.37)\,\mu A\,V^{-2}$
SICCMOS9 PMOS devices			
size	$80 \times 6\,\mu m$	$200 \times 6\,\mu m$	$500 \times 6\,\mu m$
V_{th}	$(-6.25 \pm 0.07)\,V$	$(-6.28 \pm 0.07)\,V$	$(-6.26 \pm 0.05)\,V$
S	$(0.25 \pm 0.07)\,V\,dec^{-1}$	$(0.26 \pm 0.09)\,V\,dec^{-1}$	$(0.26 \pm 0.08)\,V\,dec^{-1}$
n	4.2 ± 1.1	4.4 ± 1.5	4.3 ± 1.3
μ	$(0.1 \pm 0.1)\,cm^2\,V^{-1}\,s^{-1}$ [a]	$(0.2 \pm 0.2)\,cm^2\,V^{-1}\,s^{-1}$ [a]	$(0.1 \pm 0.1)\,cm^2\,V^{-1}\,s^{-1}$ [a]
k'	$(0.33 \pm 0.26)\,\mu A\,V^{-2}$	$(0.39 \pm 0.30)\,\mu A\,V^{-2}$	$(0.38 \pm 0.29)\,\mu A\,V^{-2}$

[a] The μ_p standard deviation in SICCMOS9 is high due to significant non-linearity in the I_{ds}/V_{gs} curves.

where W is the channel width, L the channel length and C_0 the unit capacitance in the channel area in $F\,cm^{-2}$ [49]. Linear fitting of the drain current (Figure B.10) allows for extraction of the reported mobility. The ideal mobilities in silicon are $1350\,cm^2\,V^{-1}\,s^{-1}$ and $480\,cm^2\,V^{-1}\,s^{-1}$ for the NMOS and PMOS channels respectively [52]. The BICMOS7 NMOS devices reach 45–47 % of the ideal mobility, which complies with internal reports as the technology is not optimized for phenomena such as surface scattering, nor is any correction attempted for the effective channel dimensions. The largest size BICMOS7

PMOS device reaches 49 % of the ideal mobility, which again complies with the expectation. However, the smaller sizes BICMOS7 PMOS devices reach only 21–22 %. Since the slope of the drain current is inversely proportional to the channel resistance, any series resistance will reduce this slope and thus the extracted carrier mobility. This is a limitation of the used extraction method and is noticeable for the PMOS, which has high contact resistance at the source and drain. As the largest geometry PMOS also has the largest contact areas, the effect is greatly reduced.

The ideal mobilities in silicon carbide are $1020\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ and $120\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ for the NMOS and PMOS channels respectively [47]. The SICCMOS9 NMOS devices only reach 1.4 % of the ideal mobility and the PMOS devices are even lower at 0.2 % of the ideal mobility. Here, the limitation of the used extraction method is even more prominent as the source/drain areas have much higher sheet resistance, thus introducing more series resistance. Further investigation of the device mobility would require additional measurements that are independent of any series resistance at the source/drain.

Finally, the process transconductance parameter k' is extracted as a fitting parameter in the unified model used on the I_{ds}/V_{ds} curves for all geometries and are in line with the expected values [48].

3.3. CIRCUIT BLOCK DESIGN AND CHARACTERIZATION

The characterized CMOS devices are used in the design of digital and analog circuit blocks to build a library of functional blocks that are used to design the on-chip readout circuitry in Chapter 4. Each circuit block is implemented separately in the layout design to investigate its operation independently.

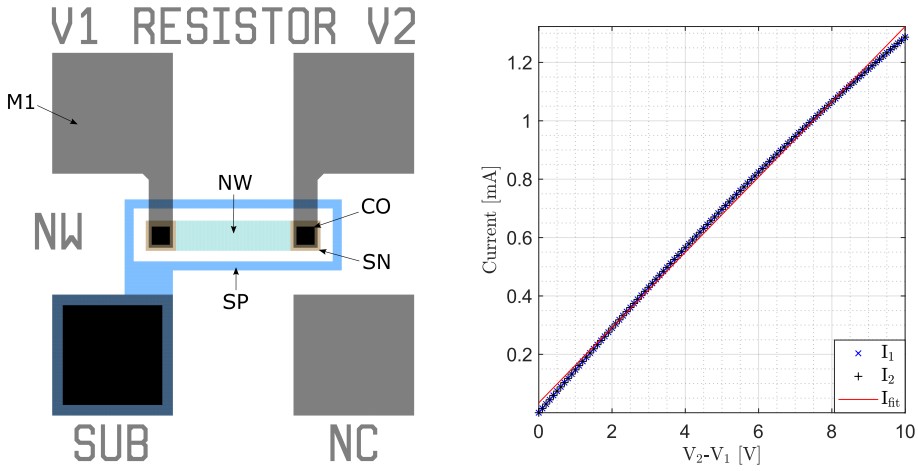
3.3.1. CIRCUIT MODELING STRATEGY AND DESIGN CONSIDERATIONS

At present, no mature design models are available for both BICMOS7 and SICCMOS9 that predict device performance well over a broad range of geometries and temperatures. Furthermore, the models only include DC signal performance with little to no AC performance taken into account. This means that it is crucial to keep circuit designs in these technologies simple with focus on function, rather than performance. This ensures successful system integration in this stage of the technology development. Hence, the characterized circuits in this chapter are not compared to simulation.

The BICMOS7 design kit is based in Cadence Virtuoso for circuit design and simulation. Hardware layout design is possible, but since there is no design rule check (DRC) or layout-versus-schematic (LVS) tool available, it is common practice in this technology to perform the layout design separately in L-Edit software. The lack of these automatic checks means that it is vital to work in a well defined hierarchy and manually check if the layout matches the designed circuit. Separate lab documents are available which provide design guidelines on each specific layer or tool used in the process. The recommended supply voltage is 10 V, which is therefore fixed for all circuit simulation. Since this concerns a single-well technology using the n-well, the p-type channel is directly implemented in the p-type epi-layer. As a consequence, all the NMOS body contacts are inherently connected through the substrate. The NMOS body bias is typically at the lowest potential, so here it always connects to ground.

The SICCMOS9 design kit is based in LTspice for circuit design and simulation. The hardware layout design is again performed separately in L-Edit. Extensive efforts by the Fraunhofer IISB research team has led to a DRC tool in K-layout (compatible with L-Edit), which is not yet bullet-proof but helps to catch most design errors. At present, there is no LVS yet, but this is on the roadmap for the coming years. The recommended supply voltage is 20 V and is fixed for all circuit design. This technology is a double-well process, with both the n-well and p-well available. However, since the n-well is directly implemented in the n-type epi-layer, all PMOS body contacts are inherently connected through the substrate. The PMOS body bias is typically at the highest potential, so here it always connects to the supply voltage.

As the contact resistances to PMOS devices in both technologies are quite high, it is decided to only include on-chip resistors that have higher values to ensure any resistance of the CMOS is negligible. To implement resistors in the order of several kΩ, the NW layer is used in BICMOS7 as it has a sheet resistance in this order of magnitude. A resistor of four squares is implemented (Figure 3.11a) and the IV curve is extracted over the complete range of operation (Figure 3.11b). The response reveals that this is not a completely linear resistance over this range, but can still be applied in many cases when resistance in this order of magnitude is required. The average resistance (Figure F.51) is $(7.85 \pm 0.14)\,\mathrm{k\Omega}$, which amounts to 4.6 squares. From this, it is concluded that the designed contact areas (metal-to-SN-to-NW) actually account for and additional 0.3 square each. Similarly, a 23 squares SN resistor in SICCMOS9 is investigated, which is designed in a serpentine manner. Contrary to the BICMOS7 NW resistor, the SICCMOS9 SN resistor IV curve is highly linear and an average resistance (Figure F.52) of $(23.2 \pm 0.4)\,\mathrm{k\Omega}$ is found, which amounts to 22.5 squares. The smaller effective amount



(a) (b)

Figure 3.11: NW resistor in BICMOS7 including a) 4-probe layout structure and b) measured IV curve. Note that the probe pads are both in M1 and M2 layer to allow measurement at different stages in the fabrication (VI and M2 not shown in favor of readability). The voltage is forced at V2 and swept within the BICMOS7 supply voltage range and grounded at V1 and SUB. The corresponding input current is measured at V2.

of squares is due to the fact that squares in the corners of a serpentine structure do not count as full squares (0.56 per corner square as a rule of thumb).

In addition to resistors, metal-insulator-metal (MIM) capacitors are implemented using two metal layers in the BEOL, which are present in BICMOS7 and the expanded SICCMOS11. The value of the MIM capacitance is calculated by

$$C = \frac{\epsilon_r \epsilon_0 A}{d_{ox}}, \tag{3.4}$$

where ϵ_r is the relative permittivity of SiO_2 and equals to 3.9, ϵ_0 the free space permittivity and equals to 8.854×10^{-12}, A the overlapping plate area and d_{ox} the distance between the two plates. Fringe fields at the capacitor plate edges are ignored.

The dimensions of a NAND logic gate in both technologies are included in Figure 3.12 to illustrate some design constants and compare the two technologies. As example, the NAND layout design footprint in BICMOS7 is only 76 % of the same design in SICCMOS9. This area increase is dominated by an increased sizing ratio between the NMOS and PMOS channel areas, which is caused by relative reduction of the anticipated PMOS driving strength in SICCMOS9 [37]. Furthermore, the SICCMOS9 BEOL is currently run on a mask aligner with reduced overlay accuracy which as a result increases the footprint, the technology would improve greatly if a wafer stepper is used. In both technologies gate lengths down to 1 µm are technically possible, but the device performance deviates much more from the simulation models due to short channel effects and in BICMOS7 can even cause short circuited devices due to dopant diffusion in the source and drain regions. Following recommendations from previous implementations in both technologies, as well as a way of reducing risks of failure at these short channel lengths, it is decided to adhere to minimum gate lengths of 4 µm in BICMOS7 and 6 µm in SICCMOS9. It was furthermore experienced that it is more convenient to fix the channel

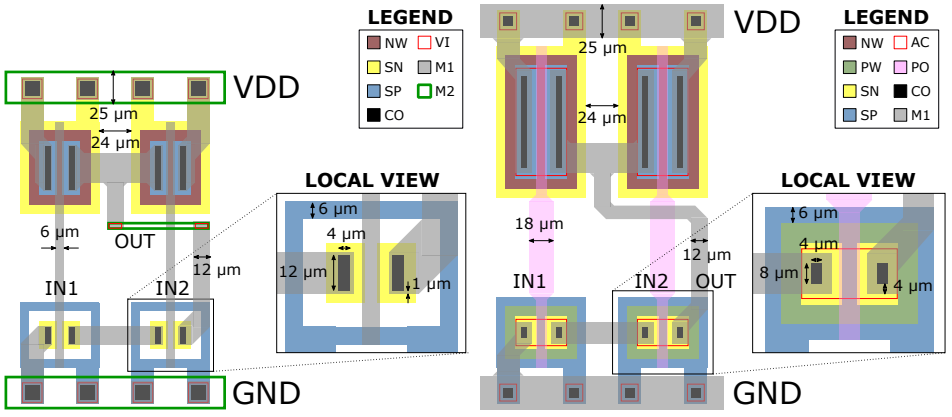


Figure 3.12: Layout design example of a NAND logic gate in a) the EKL BICMOS7 and b) Fraunhofer IISB SICCMOS9 technologies, highlighting several feature sizes. The insets show the local feature sizes of and NMOS device, which is identical for the PMOS or scaled for the channel width. Note that the SICCMOS9 PC design layer is not used in this logic block.

lengths and only vary the channel widths for large scale manual layout design, which is therefore the case in most of the designs in these technologies discussed in this work. The minimum channel geometries used are a 20 × 4 µm NMOS and 40 × 4 µm PMOS in BICMOS7 and 20 × 6 µm NMOS and 80 × 6 µm PMOS in SICCMOS9.

3.3.2. DIGITAL CIRCUIT BLOCKS

The input/output responses of inverters in both technologies are given in Figure 3.13 and the switching voltage V_m is extracted (Figures F.53 to F.56) at the point of maximum I_{dd}. Ideally, the V_m is at half of the supply voltage, which amounts to 5 V and 10 V for BICMOS7 and SICCMOS9 respectively. The BICMOS7 inverters have a V_m of (3.5 ± 0.2) V and (4.0 ± 0.1) V for the minimum size and the larger output inverters respectively. The SICCMOS9 inverters have a V_m of (9.2 ± 0.7) V and (9.2 ± 0.5) V for the minimum size and the larger output inverters respectively. The switching voltage V_m is calculated through

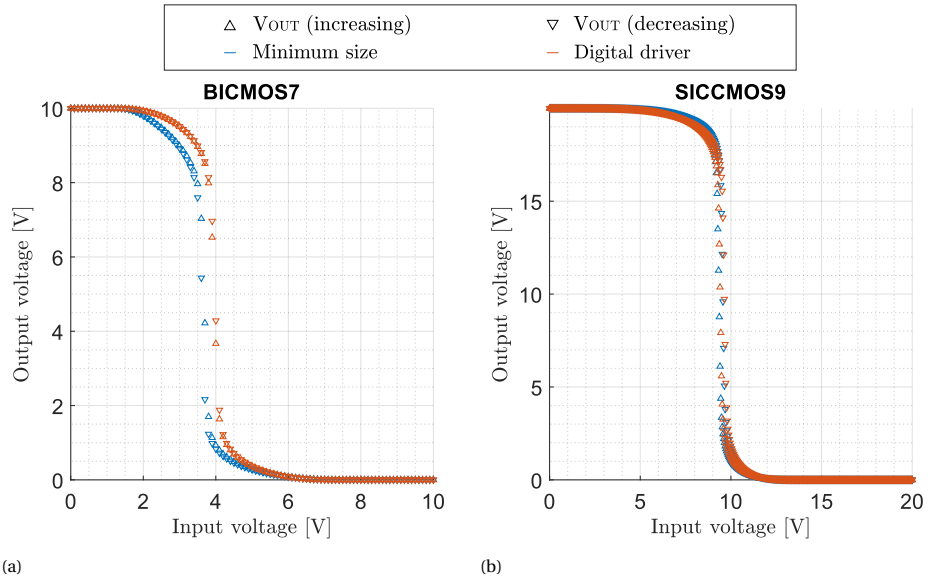
$$V_m = \frac{\alpha\left(V_{th,n} + \frac{V_{dsat,n}}{2}\right) + \beta\left(V_{dd} + V_{th,p} + \frac{V_{dsat,p}}{2}\right)}{\alpha + \beta}, \tag{3.5}$$

where $\alpha = k_n V_{dsat,n}$ and $\beta = k_p V_{dsat,p}$ [53] and V_{dsat} is the saturation drain voltage. In BICMOS7 this results in a switching voltage of 4.3 V, which is significantly higher than the measured value and could indicate that V_{dsat} is over or under estimated. This is however difficult to verify, for which more inverter sizes would be helpful in future work to better estimate this parameter. In SICCMOS9 this results in a switching voltage of 9.2 V, which matches the measured value and therefore validates the V_{dsat} derived from the fit in Figure 3.10 as the inverter matches the assumption of high V_{ds} and V_{gs} for each device. Furthermore, a suggestion can be made for the geometry ratio of future implementations by calculating the ratio [53] for $V_m = 1/2 \cdot V_{dd}$ through

$$\frac{W_p/L_p}{W_n/L_n} = \frac{k'_n V_{dsat,n}\left(V_m - V_{th,n} - \frac{V_{dsat,n}}{2}\right)}{k'_p V_{dsat,p}\left(V_{dd} - V_m + V_{th,p} + \frac{V_{dsat,p}}{2}\right)}, \tag{3.6}$$

which evaluates to 3.6 and 5.7 for BICMOS7 and SICCMOS9 respectively at room temperature, indicating that the current design ratio of both technologies should be increased to optimize V_m. This will however severely negatively impact the footprint of the digital circuits. Certainly, future improvements to the SICCMOS9 PMOS device should re-evaluate this ratio.

The minimum size inverter is used to implement a SICCMOS9 static random-access memory (SRAM) cell, with a footprint of 0.30 × 0.39 mm. The characterization curves are extracted in different modes of operation, commonly known as the butterfly curves, and analysis is performed to find the respective static noise margins (SNM) that give an indication of the data state stability (wafer-level results in Figures F.57 to F.59). The reported SNM values are taken from the minimum between the data 0 and 1 cases. The wafer-level results over 28 dies have a yield of > 85 %. The hold mode, or standby mode, characteristics are depicted in Figure 3.14a and represents two inverters connected in parallel in opposite direction as WL, BL and $\overline{\text{BL}}$ are connected to ground. The corresponding hSNM equals to (7.1 ± 1.0) V, which is close to the ideal value of 10 V consid-



(a) (b)

Figure 3.13: DC response of different sized inverters in a) BICMOS7 and b) SICCMOS9 technology. The two sizes include minimum size inverter and a digital driver which is two minimum size inverters in parallel.

ering the technology supply voltage. The read mode characteristics are depicted in Figure 3.14b, which shows the effect of read stress on the ability of the device to pull the measured terminals to 0 V as WL, BL and $\bar{\text{BL}}$ are connected to V_{dd}. As a consequence, the SNM is inevitably reduced and the corresponding rSNM equals to (4.4 ± 0.7) V.

The write mode characteristics for the data 1 case are depicted in Figure 3.14c, of which the SNM derivation is slightly different as the largest square is drawn between corresponding read and write mode curves. In this mode, WL and BL are connected to V_{dd} and $\bar{\text{BL}}$ to ground when sweeping Q, while BL and $\bar{\text{BL}}$ are swapped when sweeping $\bar{\text{Q}}$. The wSNM equals to (7.5 ± 0.9) V, which is even closer to the ideal value than the hSNM. In comparison, the aforementioned results in the same technology of the group of Mantooth at the University of Arkansas found an hSNM and rSNM of 4.65 V and 1.90 V respectively and did not report the wSNM [38]. The devices in this work have improved SNM values with a factor of 1.5 and 2.3 for the hSNM and rSNM respectively.

In addition to the inverters, several NAND and NOR logic gates are investigated with minimum size NMOS and PMOS devices. Several alterations in the layout design of the interconnect are made, which offers versatility when incorporating these logic gates in larger designs. The operation of the logic gates is verified by confirmation of their inputs/output truth table. In BICMOS7 the logic gates have a yield of > 98 % over 52 dies and in SICCMOS9 a yield of > 88 % was found over 26 dies.

Logic gates are combined to implement a digital 1-bit multiplexer in both technologies, of which the circuit diagram is illustrated in Figure 3.15a. The corresponding footprints in BICMOS7 and SICCMOS9 are 0.41 × 0.45 mm and 0.44 × 0.58 mm respectively, with a yield of > 96 % on 52 devices and > 93 % on 26 dies respectively. As expected, the

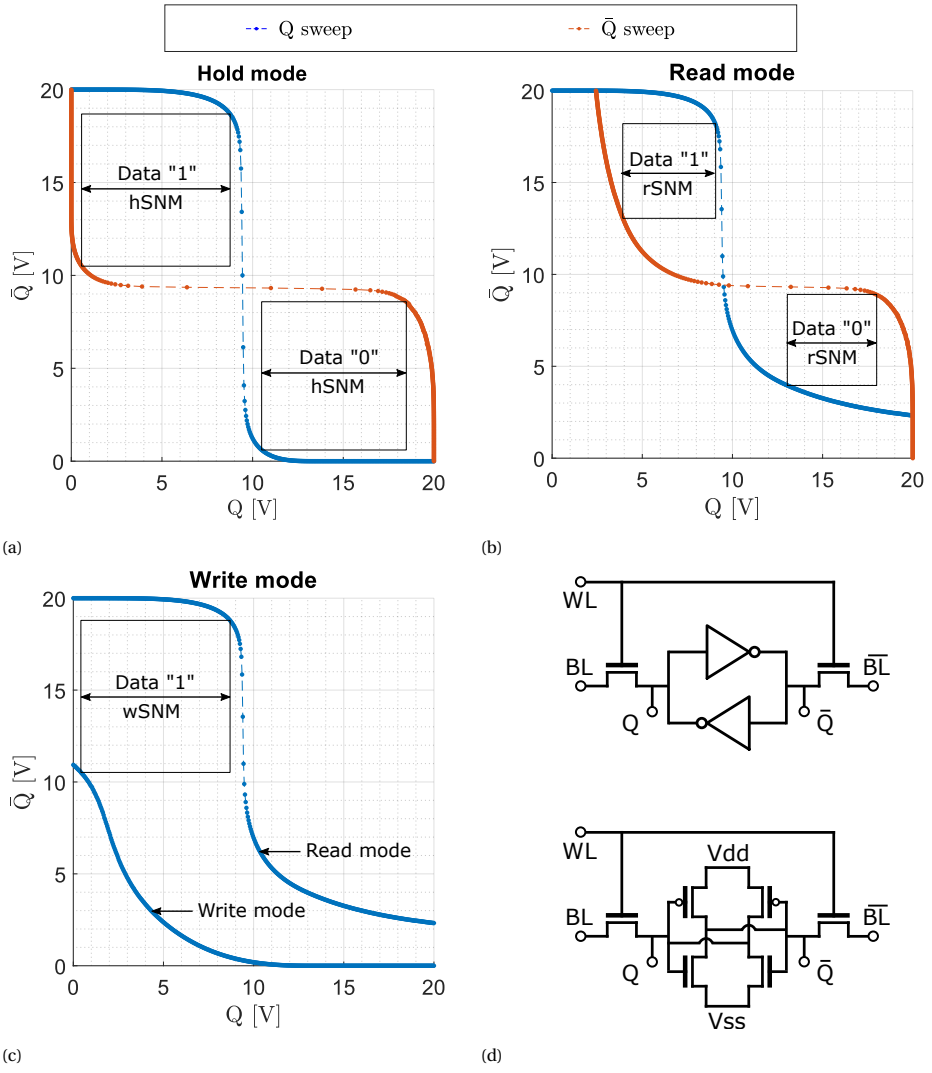


Figure 3.14: The measured $Q/\bar{Q}$ SICCMOS9 SRAM cell butterfly curves of the a) hold, b) read and c) write modes on die (0,-2), including d) the circuit representations. A sweep of Q or $\bar{Q}$ and the maximum size squares are drawn for SNM derivation and a single sweep is depicted for the write mode in favor of readability.

DC digital response is identical in both technologies, hence only the SICCMOS9 result is given in Figure 3.15c. From this response, it is deduced that OUT=IN2 for SEL=LOW and OUT=IN1 for SEL=HIGH. Increasing the device count further, a d-flipflop is implemented using the diagram in Figure 3.15b with a footprint of 1.39×0.45 mm in BICMOS7 and 1.54×0.58 mm in SICCMOS9 and yields of > 96 % on 52 devices and > 93 % on 26 dies respectively. Again, the DC response is identical in both technologies, so only the SICCMOS9 response is given in Figure 3.15d. From the response it is verified that

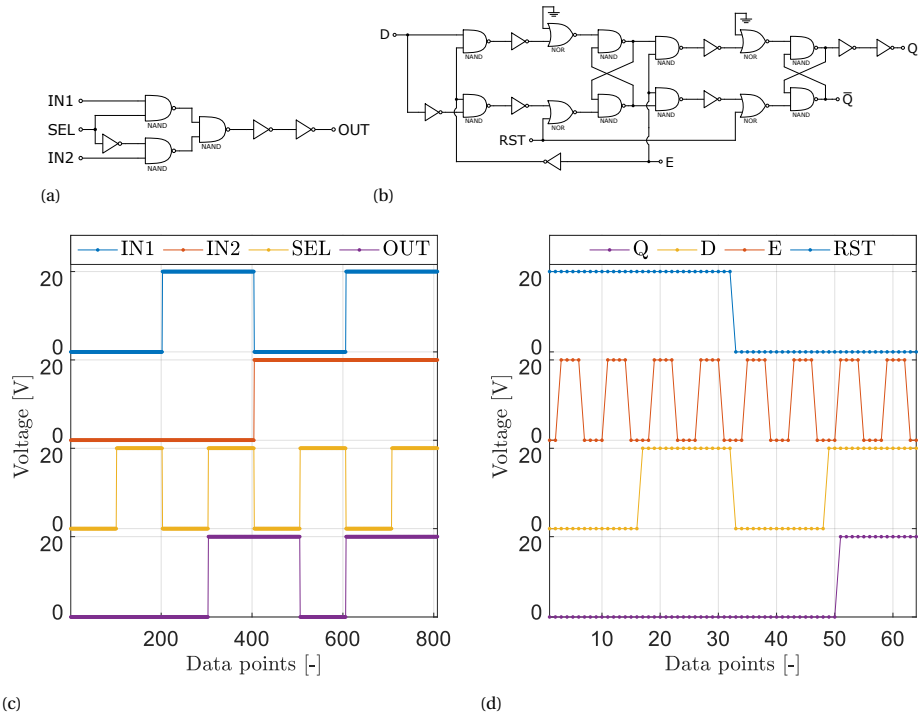


Figure 3.15: Circuit diagrams of the a) digital 1-bit multiplexer (20 devices) and b) d-flipflop (66 devices) which includes only minimum size devices. The DC response is identical in both technologies, so only the SICCMOS9 result is given of the c) digital 1-bit multiplexer and d) d-flipflop. The respective legends are included at the top of each figure.

the output is updated to Q=D on a rising edge of E, while RST=LOW.

3.3.3. ANALOG CIRCUIT BLOCKS

Inverters, pass-gates and resistors are combined to implement an analog 1-bit multiplexer, as illustrated in Figure 3.16a. The footprint is 0.57 × 0.46 mm in BICMOS7 and 0.48 × 0.58 mm in SICCMOS9. The inverters are implemented using minimum size devices in both technologies and the pass-gates include 500 µm or 250 µm wide NMOS and PMOS devices in BICMOS7 and SICCMOS9 respectively. Resistors are in place at the input and output of the pass-gates, to mitigate any current spikes during switching which may impact the devices connected to the input. In BICMOS7, these resistors are implemented by the resistor from Figure 3.11, while in SICCMOS9 the trace resistance of the polysilicon used for interconnect is deemed enough. The response in SICCMOS9 is given in Figure 3.16b. From the response it is deduced that V_{OUT}=V_{IN1} for E=HIGH and V_{OUT}=V_{IN2} for E=LOW. The analog 1-bit multiplexer is measured on wafer-level (Figures F.60 and F.61) with a yield of > 96 % in BICMOS7 (52 dies) and > 84 % in SICCMOS9 (26 dies) for a maximum offset of 2.5 % of the total range.

A two-stage amplifier, implemented using an NMOS differential pair and a com-

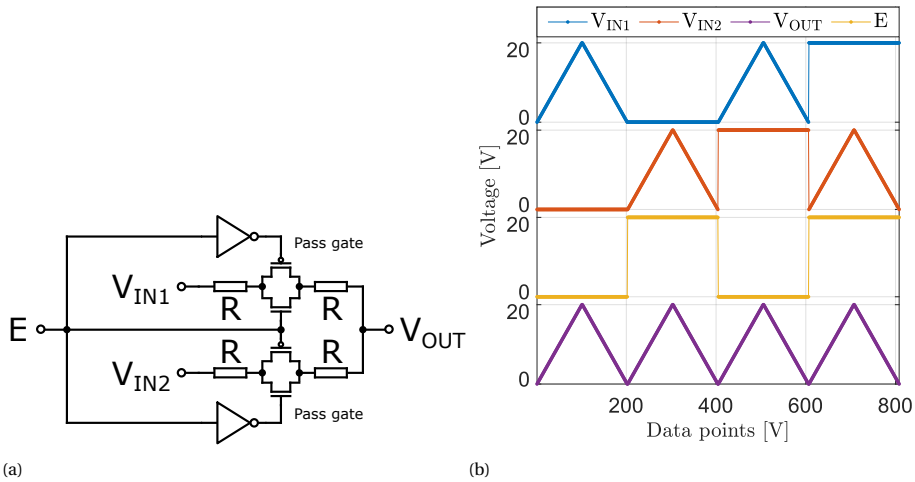


Figure 3.16: Analog 1-bit multiplexer a) circuit diagram (8 devices) and b) DC response for different input combinations of the SICCMOS9 implementation. The resistance *R* is explicitly added in BICMOS7 using NW resistors, while in SICCMOS9 only the polysilicon interconnect is considered.

mon drain stage, with an output inverter is considered as a comparator of which the circuit diagram is given in Figure 3.17a. The footprint is 0.38×0.47 mm in BICMOS7 and 0.46×0.58 mm in SICCMOS9. The typical response of the BICMOS7 comparator is given in Figure 3.17c, which includes different levels for the threshold voltage V_t and shows the expected behavior. Different bias levels are investigated to ensure optimal operation of the comparator and the averaged wafer-level (Figure F.62) offset voltages are reported for BICMOS7 in Table 3.3 with a yield of > 94 %, from which is concluded that the investigated range has negligible effect on the BICMOS7 comparator operation and the found offset voltages are low (< 0.3 % of total range). Similarly, the typical response for the SICCMOS9 comparator is given in Figure 3.17e, which also shows the expected behavior. However, the wafer-level (Figure F.63) offset voltages are significantly higher at (254 ± 242) V with a yield of > 88 % and the lowest threshold voltage deviating the most. Similarly to the BICMOS7 comparator, the offset is stable for a wide bias range.

The same two-stage amplifier is used as a unity-gain buffer, of which the circuit diagram is illustrated in Figure 3.17b. The footprint is 0.38×0.64 mm in BICMOS7 and 0.53×0.78 mm in SICCMOS9. The typical responses of the BICMOS7 and SICCMOS9 unity-gain buffer are given in Figure 3.17d and Figure 3.17f respectively. The wafer-level (Figures F.64 and F.65) offsets are (0.18 ± 0.01) V and (0.21 ± 0.13) V with yields of > 96 % and > 80 % for BICMOS7 and SICCMOS9 respectively. Since AC information is missing in the design models, no accurate simulation can be done to investigate the stability of the unity-gain amplifier. For this reason, the feedback compensation capacitor *C* is implemented with a large enough value to ensure stability. Four circular unit MIM capacitor with a radius of 55 µm are combined to efficiently fit between the CMOS power supply traces, which amounts to 2.2 pF for *C* considering the 0.6 µm M1-M2 dielectric.

The unity-gain buffer is more prone to changes in the bias voltages, as is indicated in

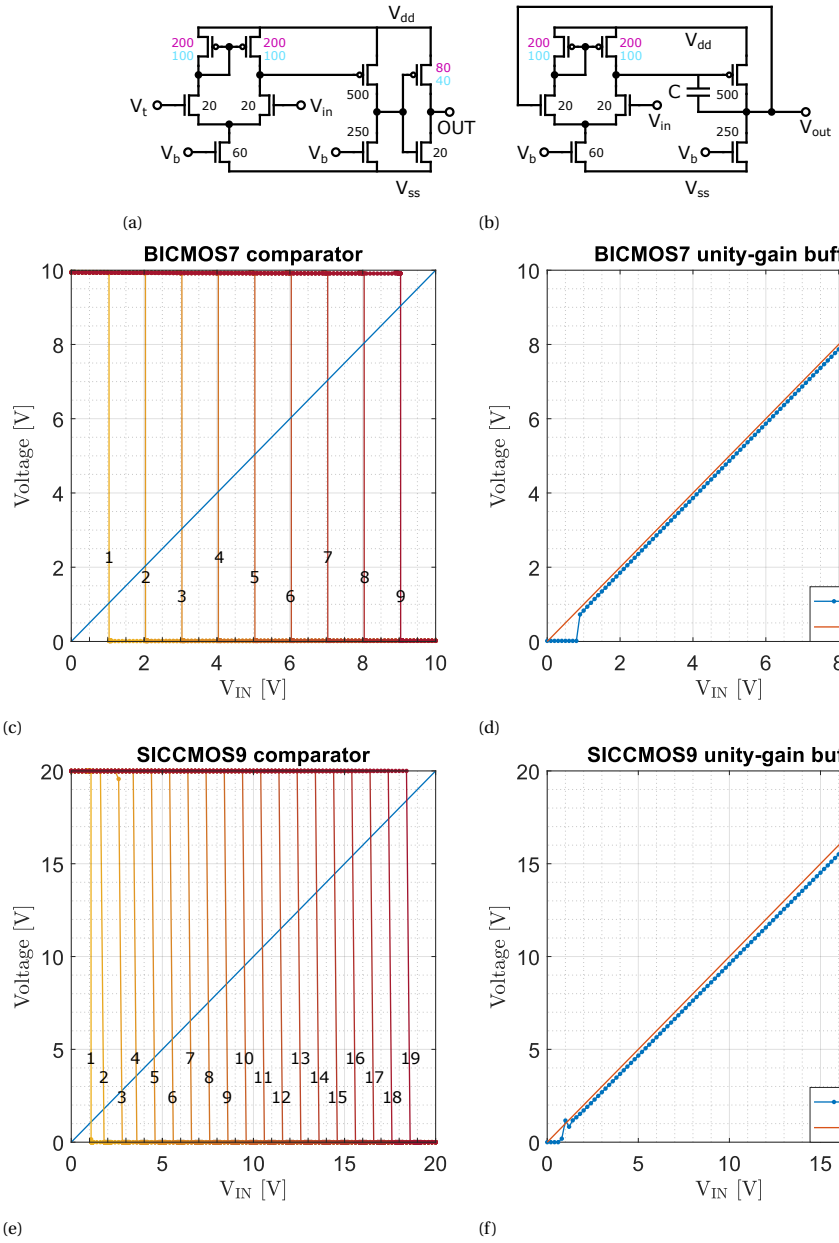


Figure 3.17: Circuit diagram of a) the comparator and b) the unity-gain buffer. The device channel width is annotated and the length is kept constant at 4 µm in BICMOS7 and 6 µm in SICCMOS9. Different device widths are indicated for BICMOS7 in cyan and SICCMOS9 in purple. The two stages are biased at pins V_b using a single off-chip voltage source at 1.2 V and 1.5 V for BICMOS7 and SICCMOS9 respectively. The typical response of c,e) the comparator and d,f) the unity-gain buffer is given on die (0,0) in both technologies.

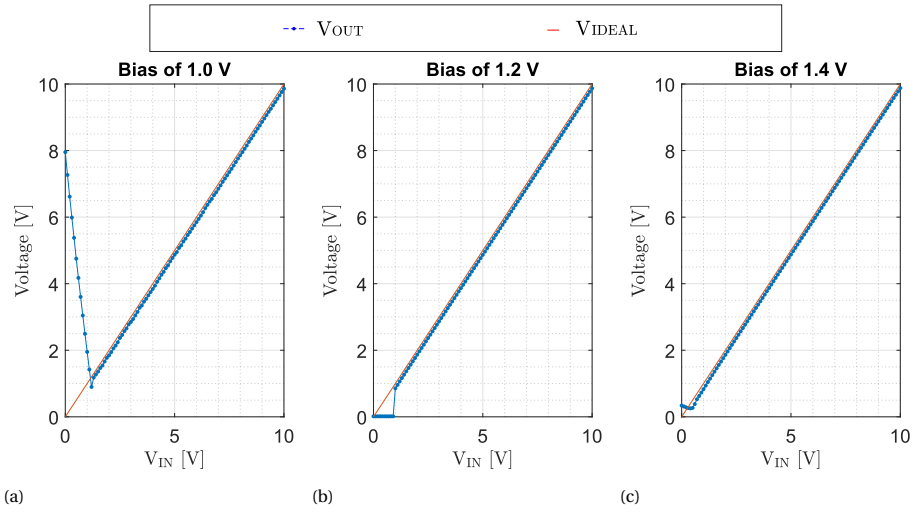


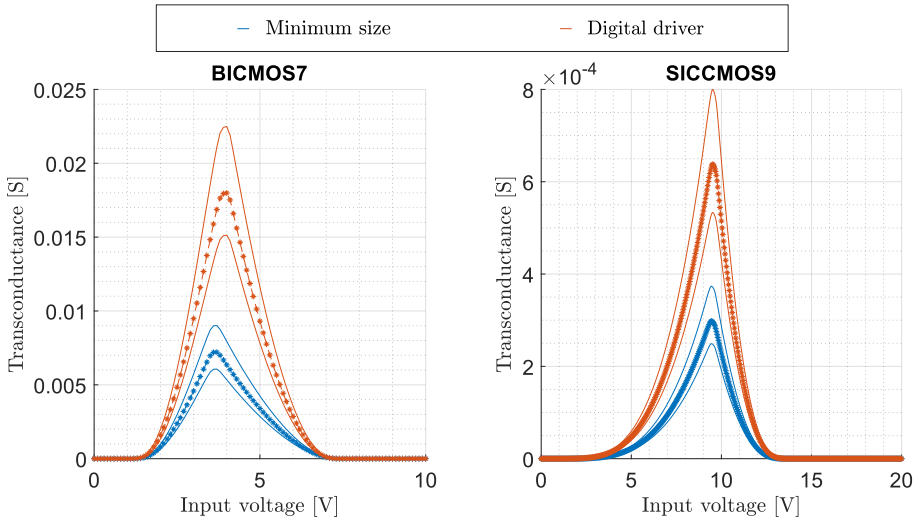
Figure 3.18: Different behavior of the BICMOS7 unity-gain buffer in the investigated biasing range, deviating in the low voltage input range. Three different cases are identified, including a) large deviations for bias of 1.0 V on die (-4,0), b) flattened output at 0 V for a bias of 1.2 V on die (-4,0) and c) higher flattened potential for a bias of 1.4 V on die (0,0).

Table 3.3. The typical response of the BICMOS7 unity-gain buffer at a bias level of 1.0 V is given in Figure 3.18a. Low input voltages result in highly undesired behavior with offsets upto 8 V, which is unacceptable for the sensor readout implementation. However, it should be noted that the upper limit is maximum which provides a wide range of operation. The unwanted behavior for small input signals is explained by the low bias voltage, which is 0.3 V below the NMOS threshold voltages reported in Table 3.2. The biased NMOS device will therefore remain in cut-off for low V_{ds} levels in both stages. The bias voltage is increased to 1.2 V and the typical response is depicted in Figure 3.18b. The highly undesired behavior for low input voltages is now reduced to a flattened output level at 0 V. Though still undesired, this is deemed acceptable for the readout implementation. Increasing the bias voltage to 1.4 V gives similar results to the 1.2 V biasing, though on several dies the flattened output is not on 0 V but a slightly higher potential, as shown in Figure 3.18c.

The previously mentioned inverter logic gate can also be considered as a push-pull

Table 3.3: Wafer-level offset voltage information of the BICMOS7 comparator and unity-gain buffer for three different bias levels.

	Comparator		**Unity-gain buffer**	
Bias	Mean offset	Maximum offset	Mean offset	Maximum offset
1.0 V	(18 ± 11) mV	(22 ± 11) mV	(0.28 ± 0.13) V	(3.40 ± 2.75) V
1.2 V	(17 ± 11) mV	(22 ± 11) mV	(0.18 ± 0.01) V	(0.79 ± 0.05) V
1.4 V	(17 ± 12) mV	(24 ± 11) mV	(0.16 ± 0.02) V	(0.59 ± 0.24) V



(a) (b)

Figure 3.19: Extracted inverter transconductance of the DC responses in Figure 3.13 of different sized inverters in a) BICMOS7 and b) SICCMOS9 technology. The two sizes include minimum size inverter and a digital driver which is two minimum size inverters in parallel. The solid lines mark the lower and upper limit considering the standard deviations reported in Table 3.2 for n.

based transconductance amplifier, with the amplifier transconductance G_m given by adding the gate-drain small signal transconductance of the NMOS and PMOS devices through

$$G_m = g_{m,n} + g_{m,p} = \frac{I_{dd}}{\phi_t}\left(\frac{1}{n_n} + \frac{1}{n_p}\right), \tag{3.7}$$

where $g_{m,n}$ and $g_{m,p}$ are the gate-drain small signal transconductance of the NMOS and PMOS devices respectively and ϕ_t the thermal voltage [50]. The resulting G_m/V_{in} curves are given in Figure 3.19 and the maximum G_m is found at the switching voltage and equals to approximately 4.8–7.1 mS and 15–23 mS for the small and large inverter respectively for BICMOS7 and 0.22–0.33 mS and 0.44–0.66 mS for the small and large inverter respectively for SICCMOS9.

3.3.4. ANALOG-TO-DIGITAL CONVERSION

A vital functional block for sensor signal readout is the analog-to-digital converter (ADC), which at present has not been reported to be integrated with sensors on-chip in silicon carbide. In the domain of ADC design, there are various different approaches, such as flash, successive approximation or sigma-delta, that each have their advantages and disadvantages. As a first attempt to find an intermediate between pure analog or digital output, digital and analog blocks are combined in a 2-bit flash ADC that is implemented using a resistive ladder, comparator bank and thermometer encoder (68 MOS devices) with a footprint of 1.5 × 2.3 mm. This architecture allows for direct and continuous con-

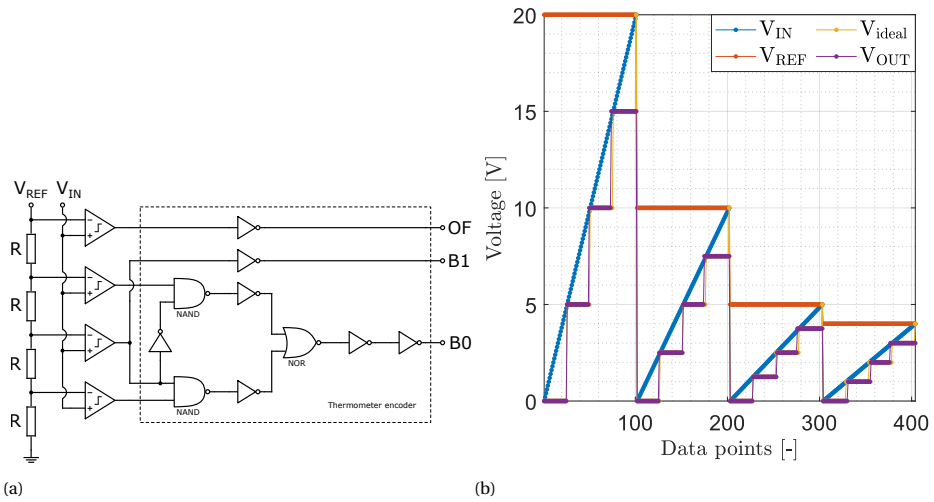


Figure 3.20: The SICCMOS9 2-bit flash ADC a) circuit design and b) measured V_{out}/V_{in} curves for input ranges set by V_{ref} at 20 V, 10 V, 5 V and 4 V on die (-3,-2). The circuit is biased at 1.5 V using an off-chip voltage source and the comparator in Figure 3.17a and 20 kΩ SN resistors are used in this design.

version with a straightforward circuit design, as provided in Figure 3.20a. However, it should be noted that the area consumption increases rapidly for higher amounts of bits and that resistor mismatching or comparator offsets directly impact the accuracy of the ADC. The implementation in BICMOS7 used an incorrect thermometer encoder circuit and is therefore not included in the results.

The 2-bit flash ADC allows for a tunable range that is set by providing the range at V_{REF}, of which the results are given in Figure 3.20b. The ideal ADC response V_{ideal} is included and the two digital output bits B_0 and B_1 are used to calculate the corresponding output voltage V_{out}. The overflow bit OF is not measured due to the 7 probe maximum taken into account in the layout design. The maximum differential non-linearity (DNL) equals to 1.5 ± 0.5 LSB, the maximum integral non-linearity (INL) equals to 1.3 ± 0.5 LSB and the yield is > 75 % over 28 dies at room temperature.

To expand the achieved results, the architecture is expanded to a 4-bit flash ADC by use of the same blocks, which has a footprint of 8.0×1.5 mm. This translates to an area increase by a factor of 3.5, which is explained by looking at the requirements for each bit. The comparator bank requires 2^n comparators, which means that the 4-bit ADC has four times more comparators. On the other side, the thermometer encoder logic scales close to linear with the amount of bits, thus requiring two times more logic gates. Depending on the sizes of the comparators and logic gates respectively, the complete design is scaled by a factor between two and four. Due to the long fabrication time of each multi-project wafer run, the 4-bit flash ADC could not be characterized within the timeline of this work. It is expected to see comparable behavior to the 2-bit flash ADC on a 5 V range, as the step size would be identical for the 4-bit flash ADC on a 20 V range.

3.4. EFFECTS AND SENSING OF TEMPERATURE

The work on temperature sensing was performed in collaboration with L. M. Middelburg. Parts of this section have been included in his dissertation [54].

As one of the prominent applications of silicon carbide is in the domain of high temperature, it is vital to investigate the SICCMOS9 technology further for elevated temperature. Unfortunately, the measurement probe stations in the EKL facilities only allow up to 200 °C at present, which is still far under what is possible in silicon carbide. These higher temperatures above 200 °C are left for future investigation, as these are not of direct interest to the sun position sensor application. As the effect of temperature on the device behavior is characterized by an interplay of many temperature dependent parameters, this section aims to identify changing behavior rather than provide a physical model for a complete explanation of the behavior.

3.4.1. REVISITING CMOS DEVICES AT HIGH TEMPERATURE

The reported BICMOS7 and SICCMOS9 CMOS devices are investigated on single chips for the effects of elevated temperature. For this purpose the I_{ds}/V_{gs} curves of different size devices are listed in Figures 3.21 and 3.22. As a first observation, it is identified that all of the measured devices are still operational at 200 °C. The parameters in Table 3.2 at room temperature are not again extracted for these higher temperatures, but a selection is qualitatively discussed in the paragraphs below.

Looking closer at the BICMOS7 NMOS devices, the I_{ds} reduces with temperature for the highest V_{gs} levels, by steps of roughly 20–25 % per temperature increment. This implies that the device mobility is also reducing with temperature. Another effect is a shift of the threshold voltage to a lower level, with a calculated average of 0.4 V per 100 °C. This suggests that the device threshold voltage will approximate 0 V around 300 °C, making it impossible to bring the device in cut-off in conventional circuits. Finally, the insets on a logarithmic scale indicate the vast increase of leakage current in the cut-off state, reaching roughly 0.1 µA at 200 °C. The leakage current increase does not scale linearly, so might already be catastrophic for the device behavior below 300 °C. The BICMOS7 PMOS devices are affected similarly as the NMOS devices. Again, the I_{ds} reduces with temperature for the highest V_{gs} levels, but now the decrease is roughly 20 % at 100 °C and another 15 % at 200 °C. This indicates that the I_{ds} in this region may not be affected much at even higher temperatures. The threshold voltage is also shifting to a lower level, with a calculated average of 0.5 V per 100 °C this suggests that the threshold voltage will reach 0 V around 500 °C. The leakage current in the cut-off state is reaching roughly 0.1 µA at 200 °C, indicating that this effect is independent of the channel dopant.

Considering the SICCMOS9 NMOS devices, the opposite trend for I_{ds} is observed as it increases with temperature for the highest V_{gs} levels, by steps of roughly 35–40 % per temperature increment. The SICCMOS9 device mobility is thus going up with temperature. The threshold voltage shifts to a lower level, with a calculated average of 0.7 V per 100 °C. This suggests that the device threshold voltage will approximate 0 V around 350 °C, which is only a minor improvement over the BICMOS7 devices. Finally, the insets on a logarithmic scale indicate no increase of leakage current in the cut-off state whatsoever. The shape of the I_{ds}/V_{gs} curve therefore is not showing signs of degradation, with the exception of the threshold voltage shift, and is arguably even improving for

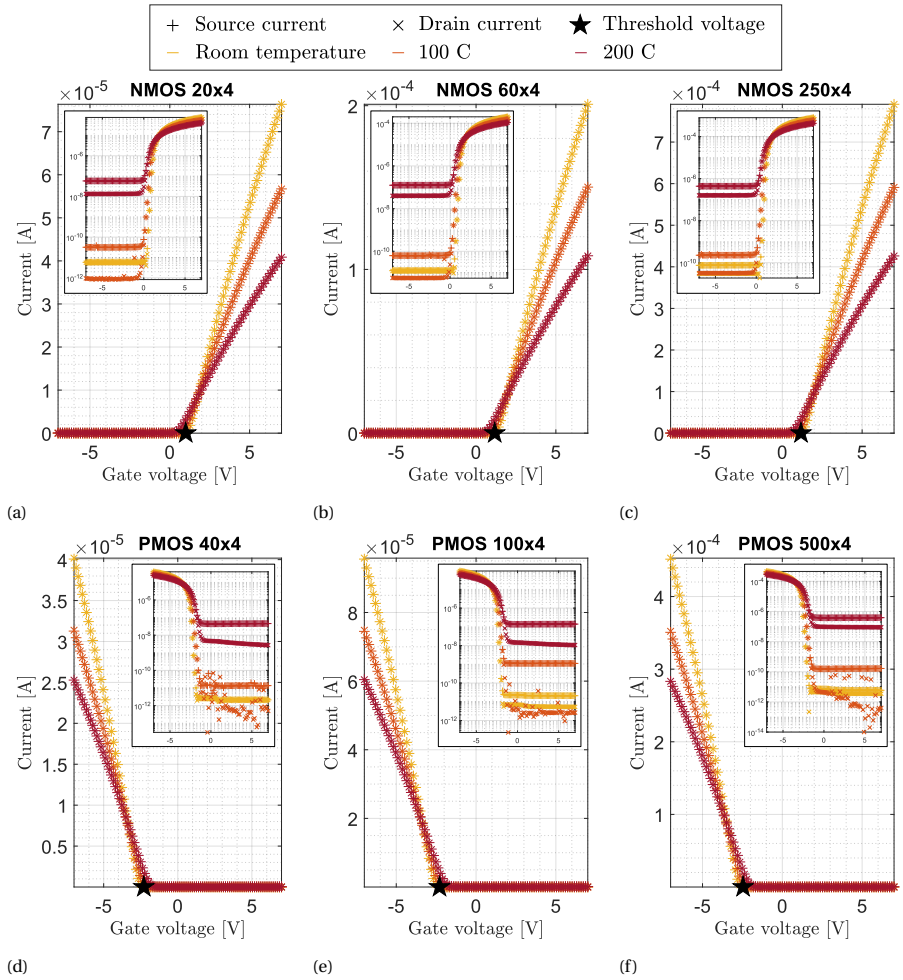


Figure 3.21: The measured I_{ds}/V_{gs} curves at different temperature levels with marked threshold voltage for the room temperature data on die (1,1) of the a) 20 × 4 µm NMOS, b) 60 × 4 µm NMOS, c) 250 × 4 µm NMOS, d) 80 × 4 µm PMOS, e) 200 × 4 µm PMOS and f) 500 × 4 µm PMOS Si devices. The devices are biased in the linear region at 0.1 V and −0.1 V for NMOS and PMOS respectively.

higher temperatures as for example the mobility is increased, which allows for faster circuits. Lastly, the SICCMOS9 PMOS devices show a similar trend with increasing I_{ds} with temperature for the highest V_{gs} levels. Moreover, the reported saturation effects at room temperature are vastly reduced at the elevated temperature levels, which dramatically increases the device mobility and its ability to drive off-chip loads. This is explained if the source and drain contact series resistance is considered as a narrow Schottky barrier, which cannot be crossed by the charge carriers at room temperature. At the elevated temperature, thermally excited charge carriers are able to cross the Schottky barrier and/or tunnel through [55]. Furthermore, the threshold voltage also shifts towards

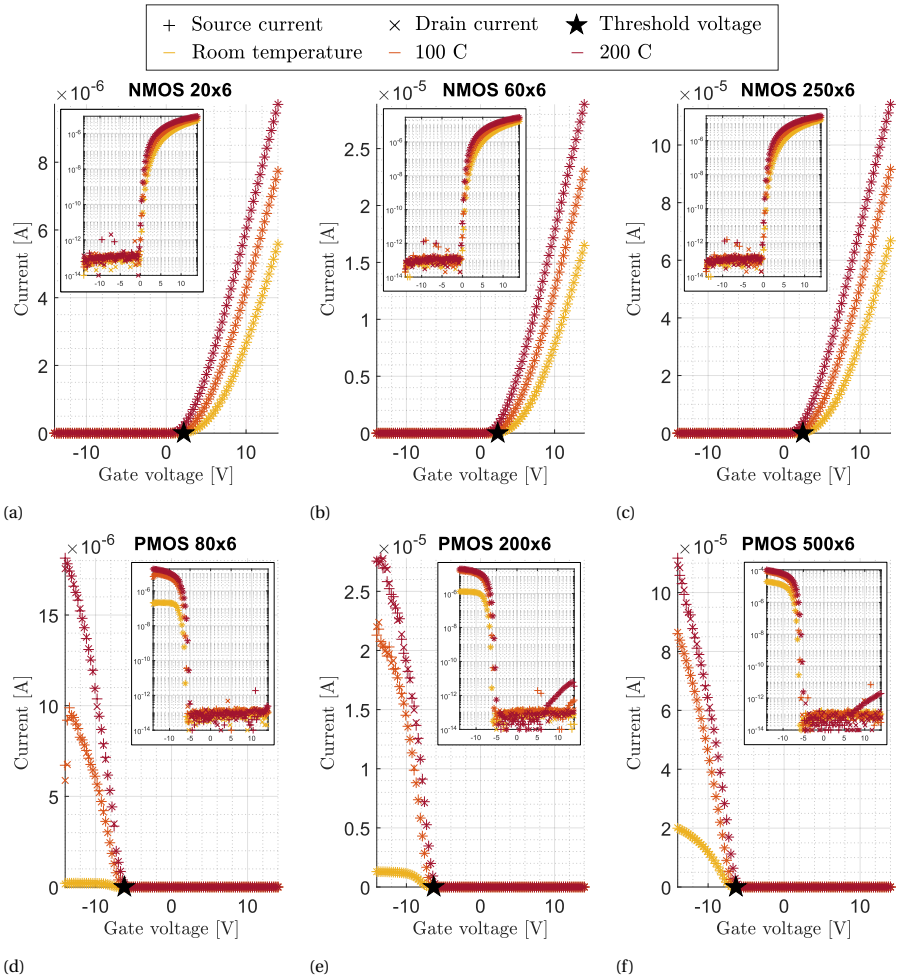


Figure 3.22: The measured I_{ds}/V_{gs} curves at different temperature levels with marked threshold voltage for the room temperature data on die (0,0) of the a) 20 × 6 µm NMOS, b) 60 × 6 µm NMOS, c) 250 × 6 µm NMOS, d) 80 × 6 µm PMOS, e) 200 × 6 µm PMOS and f) 500 × 6 µm PMOS SiC devices. The devices are biased in the linear region at 0.2 V and −2 V for NMOS and PMOS respectively.

lower levels, but due to the changing behavior is not calculated. Finally the leakage current in the cut-off state is again not affected by temperature, with the exception of a minor increase deep in the cut-off region for the two largest devices at 200 °C.

3.4.2. RESISTIVE AND CTAT TEMPERATURE SENSORS

Accurately sensing the temperature in silicon carbide devices is of great importance to their reliable operation and monolithic integration alongside the sun position sensor would benefit further miniaturization of sensor systems in space, such as the AttoSats. It is desirable to integrate temperature sensors in systems that need to endure elevated

temperatures for monitoring and conditioning of the integrated systems. As such, implementation of SiC temperature sensors in integrated circuit technologies is required. A vertical p-i-n diode temperature sensor is already reported by Fraunhofer IISB in a comparable technology [56] and has a sensitivity of 2.3–3.4 mVK^{-1} for a wide operating range and shows excellent linearity. However, this sensor is not compatible with the presented planar SiC CMOS technology. For this reason, some temperature sensors by resistive and CMOS structures are investigated in this work.

The resistive test structures are characterized on wafer-level by means of 4-point measurement on 30 dies. The normalized sheet resistance of the doped SN and PO layers is extracted for different temperatures in the range of 25–200 °C by measuring the Van der Pauw Greek cross structures (Figure 3.7). The polysilicon layer has a positive temperature coefficient of resistance (TCR) that is linear in the measured range, with a maximum change of 15 %. This corresponds to reported values in literature [57, 58]. In contrast, the doped SN layer has a negative TCR and is not linear in the measured range, with a maximum change of 19 %. This is explained by the higher ionization energies of dopant atoms in the hexagonal silicon carbide compared to the cubic silicon crystal structure. Therefore, the dopant atoms are not fully ionized at room temperature [47], explaining the negative TCR and non-linear behavior. Though the doped SN layer has a larger variation, the non-linear TCR is a drawback for reliable temperature sensors.

Next, resistors are integrated and measured over the 20 V operating range of the SiC CMOS (Figure 3.23b), in which the resistors show linear behaviour. There is a small deviation between the results found from the sheet resistance measurement and the integrated resistors, which is likely due to very different bias conditions (−0.1–0.1 V for the Van der Pauw structures). The maximum deviation in resistance of the monolithic resistors is 20 %. Furthermore, the SN integrated resistor is measured and compared with

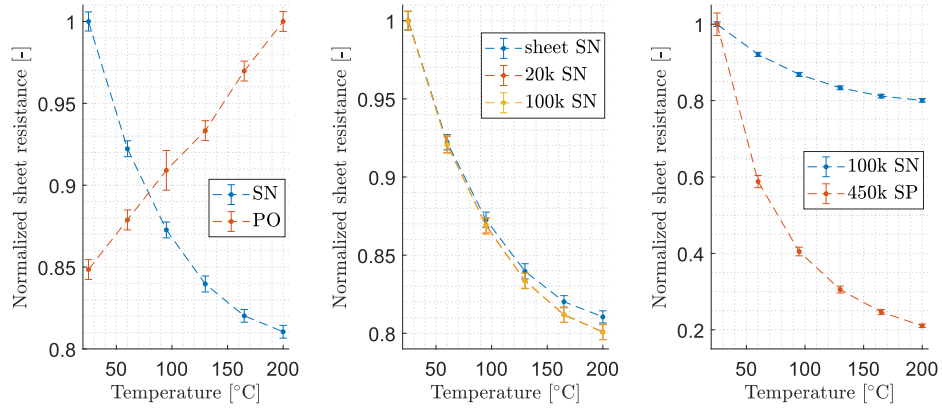
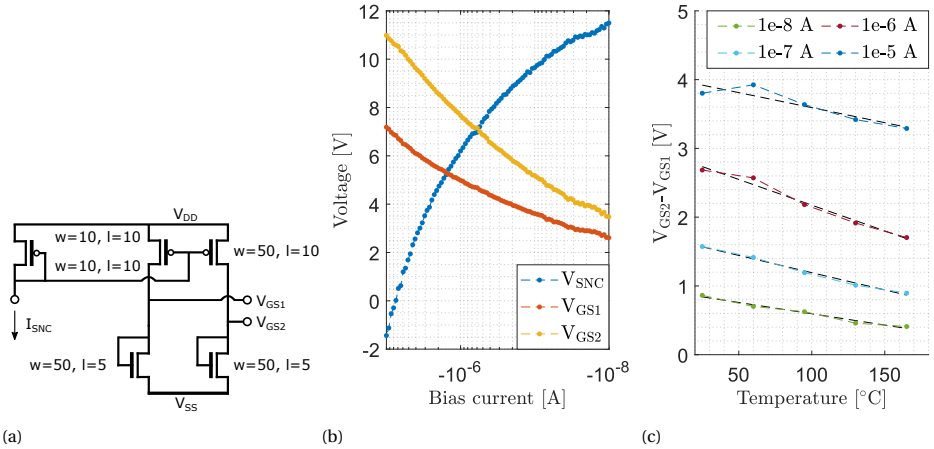


Figure 3.23: Normalized resistance (R/R_{max}) for different temperatures of a) the doped SN and PO layers sheet resistance, b) monolithic SN resistors compared with the SN sheet resistance and c) monolithic SN and SP resistors. The sheet resistance is extracted from IV curves through a linear fit on 101 data points. The errorbars correspond to the standard deviation on wafer-level.



(a) (b) (c)

Figure 3.24: CMOS circuit a) of the five transistor diode-based CTAT. The transistor channel width and length is annotated for each device. The circuit requires an external current bias source I_{SNC}, which corresponds to a bias voltage V_{SNC} at that node. Response of the CTAT in b) for different current biasing and a temperature of 25 °C, listing the bias voltage V_{SNC} and differential outputs V_{GS1} and V_{GS2}. For a selection of current bias conditions, the differential output is plotted in c) for different temperatures. Linear fits are added to each respective curve, of which the slope gives the sensitivity in VK^{-1}.

its SP counterpart (Figure 3.23c). This reveals that the SP layer has a significantly higher sensitivity to temperature increase, reaching a change in resistance up to 79 %. The difference is again attributed to the ionization energy, as the aluminum p-type dopant shows a larger variation in the fraction of ionized dopants compared to phosphorus or nitrogen over this temperature range [47].

A five-transistor diode-based complementary to absolute temperature (CTAT) sensor is implemented (Figure 3.24a), with a footprint of 0.30×0.32 mm, and characterized by a logarithmic sweep of its current biasing I_{SNC} in the range of 10^{-8} to 10^{-5} A. The corresponding voltage bias V_{SNC} and differential outputs V_{GS1} and V_{GS2} are measured and given in Figure 3.24b. The magnitude of the differential output ($V_{GS2} - V_{GS1}$) depends on the current bias but is also sensitive to temperature. To visualize this, four bias levels are selected, and the corresponding differential output is fitted to a linear curve for different temperature points in Figure 3.24c. The resulting sensor sensitivities are in the range of -3.3 to $-7.5\,\mathrm{mVK}^{-1}$, of which the highest sensitivity corresponds to a bias of 1 µA. This sensitivity is two times higher than the previously reported temperature sensor [56], within this temperature range.

3.4.3. EVALUATION OF CIRCUIT OPERATION AT HIGH TEMPERATURE

The effect of elevated temperature on the inverters in both technologies is given in Figure 3.25, indicating functional circuits with unchanged switching voltage and minimal degradation in performance. This degradation is similar for both results, with less sharp transitions around the switching voltage. Of course, the BICMOS7 circuit static power consumption goes up dramatically, because of the leakage currents in Figure 3.21.

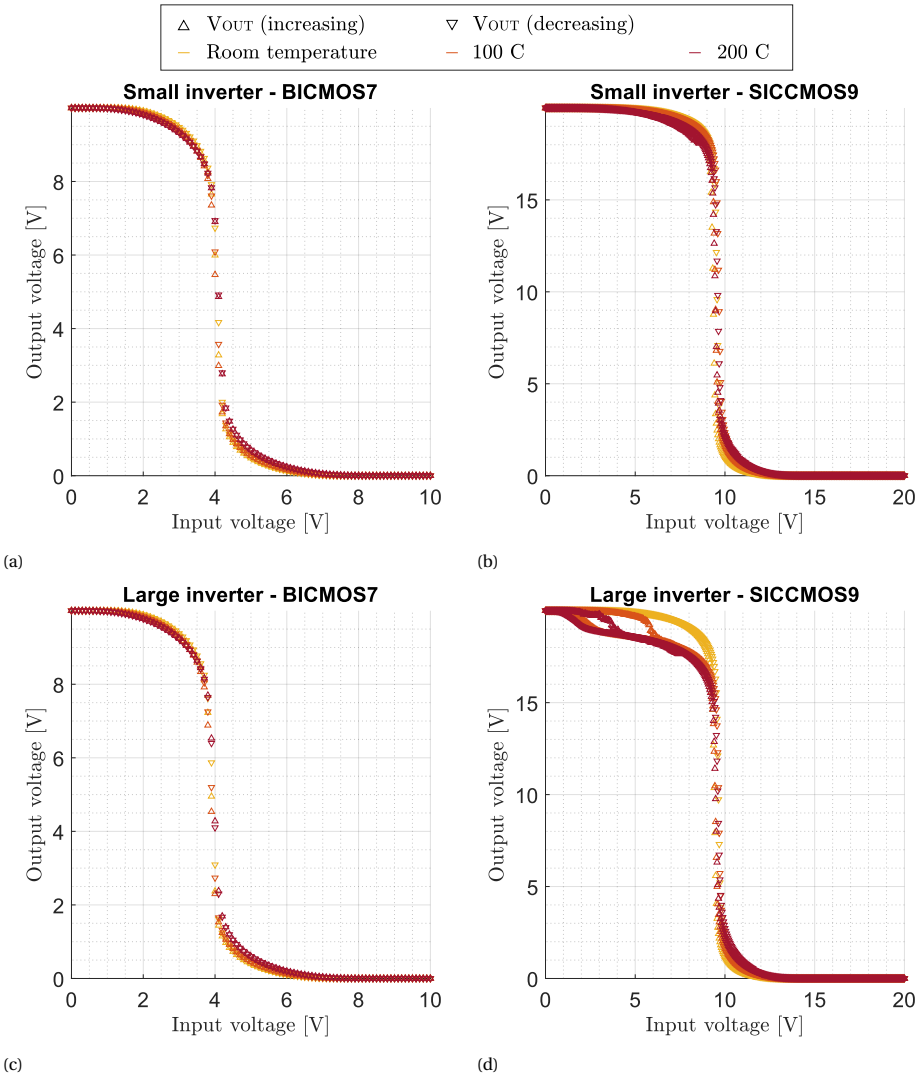


Figure 3.25: DC response of minimum sized inverters in a) BICMOS7 and b) SICCMOS9 technology and digital drivers in c) BICMOS7 and d) SICCMOS9 technology. Note that the SICCMOS9 large inverter shows deviation and hysteresis in the high output region.

The previously reported SICCMOS9 circuits are verified for operation at higher temperature and an overview is given in Figure 3.26. Starting with the SRAM cell, all the SNM values are reduced for the higher temperature levels as result of the less sharp transition of the inverters, which is a negative effect for the stability of the circuit. Fortunately, the measurement results (Figures 3.26a to 3.26c) reveal that the SRAM cell retains correct function even at 200 °C. Next, the offset voltage of the comparator and source follower is measured (Figures 3.26d and 3.26e), indicating an increase of the offset for increas-

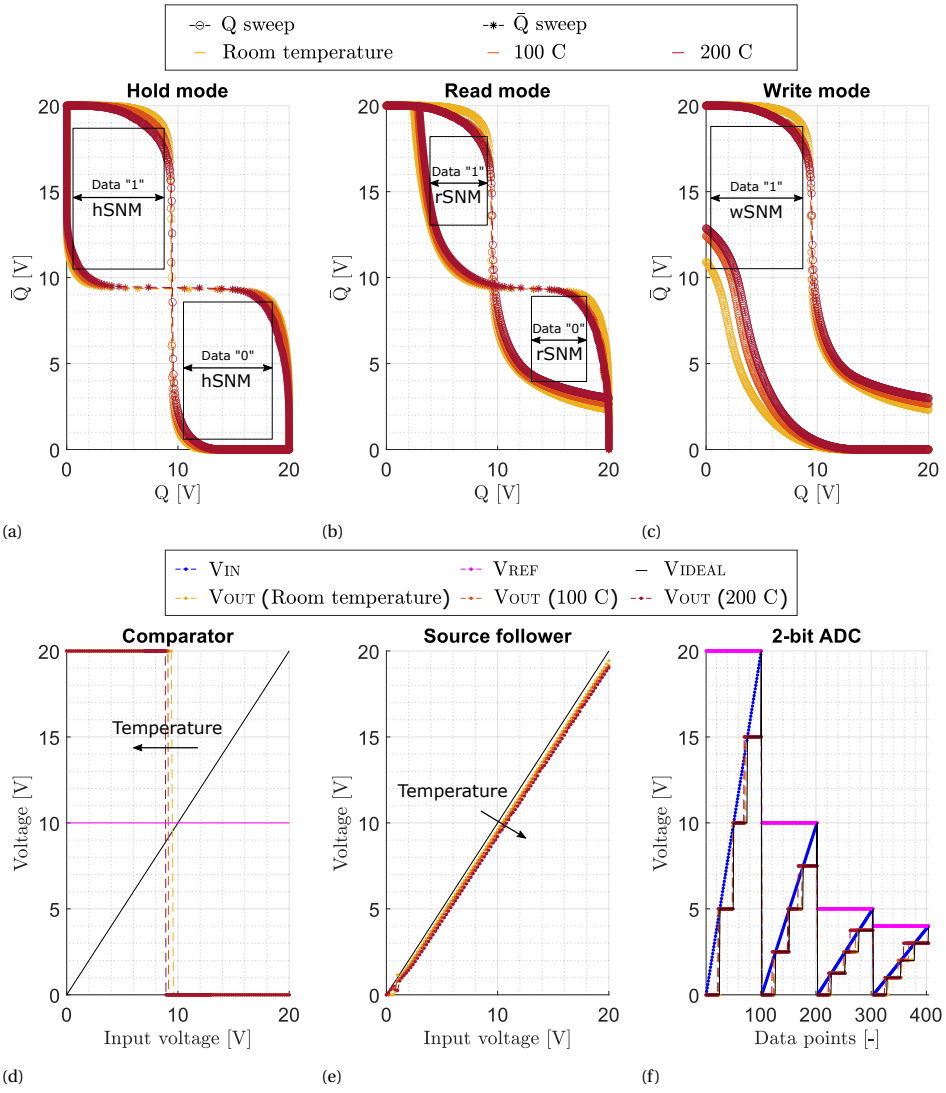


Figure 3.26: Summary of SiC CMOS circuit measurements at elevated temperatures. The measured $Q/\bar{Q}$ SRAM cell butterfly curves for different temperature levels of the a) hold, b) read and c) write modes on die (0,-2). The maximum size squares are drawn for the room temperature data for SNM derivation. The measured V_{out}/V_{in} curves at different temperature levels of the d) comparator for a threshold of 10 V and e) source follower on die (0,0). The measured V_{out}/V_{in} curves of e) the 2-bit ADC at different temperature levels, for input ranges set by V_{ref} at 20 V, 10 V, 5 V and 4 V on die (-3,-2). All circuits are biased at 1.5 V using an off-chip source.

ing temperature. Fortunately, the range of operation of these circuits is not affected and reproduce the behavior expected from the room temperature characterization. Finally, the 2-bit ADC is revisited, whose performance is directly affected by the increased comparator offset. This is most dominantly the case for the highest discretization level,

which translates to almost skipping the before last discretization level in the cases of V_{ref} of 5 and 4 V. Overall, these circuits would benefit from research into mechanisms for compensation of the increasing offsets as a result of temperature increase.

3.5. CONCLUSIONS AND RECOMMENDATIONS

This chapter presented the fabrication and characterization of silicon and silicon carbide CMOS technologies of similar device structure. The 4 µm silicon technology, called BICMOS7, utilizes seven design layers and offers two levels of metal interconnect. Similarly, the 6 µm silicon carbide technology, called SICCMOS9, utilizes nine design layers and offers two levels of interconnect consisting of one metal and one polysilicon layer. The main differences in SICCMOS9 with respect to BICMOS7 apart from the different substrate material, are the much higher dopant activation temperature and the extensive focus on ohmic contacts to the source and drain areas by means of silicides.

The reported devices and circuits are measured to a large extend on wafer-level, to provide parameter deviations and preliminary yield figures. The extracted parameters include the threshold voltage, subthreshold slope, slope factor, mobility and process transconductance. Looking purely at these parameters, the SICCMOS9 devices are inferior to the BICMOS7 devices. It should be noted that the performed mobility extraction is dependent on the source and drain series resistance, which is much higher in SICCMOS9. Therefore, the extraction would benefit from a different approach that is independent of this resistance. The investigated circuit blocks are inverters, NAND gates, NOR gates, 1-bit digital multiplexer, 1-bit analog multiplexer, d-flipflop, push-pull transconductance amplifier, comparator, unity-gain buffer, 2-bit ADC and SRAM cell. The yield figures of these circuits are high (> 70 %), considering the still premature level of the technology, and indicates great potential for future integration of higher device count systems. The performance does not compare with state-of-the-art silicon implementations, but shows correct function which allows use in environments where silicon based devices would not be functional at all.

Effects of elevated temperature levels are investigated up to 200 °C, as this is the tool capability limit at the EKL facilities at present. The BICMOS7 devices are still operational, but the technology parameters are degrading and the leakage current in the cut-off region is vastly increasing with increasing temperature. In contrast, the SICCMOS9 devices have improved technology parameters with negligible change of leakage current for higher temperature levels. This suggests that it is not needed to look into specialized layout design for harsh environment, such as enclosed layout transistors (ELT), that typically consume more chip area. The SICCMOS9 circuit blocks are also verified for correct operation at higher temperature levels. Even though the single SICCMOS9 devices are improved, the circuit blocks performance is degraded at higher temperature with higher offset voltages for example. The device and circuit verification is complemented by reporting on resistive and CMOS temperature sensors in the same range. The resistive sensors consist of polysilicon, n++ doped and p++ doped design layers, of which the p++ doped layer showed the largest change in resistance of 79 % over a range of 25–200 °C. Finally, a five-transistor CTAT was implemented and characterized for different external bias currents. The device showed a maximum sensitivity of $-7.5\,\text{mVK}^{-1}$ for a bias current of 1 µA and linear behavior over a temperature range of 25–165 °C.

Several improvements are recommended for future work on and in the SICCMOS9 technology in the coming years. The implementation of ohmic contacts to the doped semiconductor regions is challenging and would benefit from optimized metal stacks for the silicidation. To allow efficient interconnect with low resistance, the technology would benefit from upgrading to two levels of metal interconnect. The device footprints can be improved by investigation of shorter channels and migrating the BEOL fabrication to a wafer stepper to greatly relax the overlay constraints. Regarding circuit design, the community would greatly benefit from improved simulation models that accurately predict the behavior in both DC and AC simulation. This opens up more possibilities in analog circuit design towards amplifiers and for example the integration of on-chip biasing. The work towards better simulation models has already started at both Fraunhofer IISB and ECTM at present, but is still in its starting phase so no results are presented in this chapter. Expanding the portfolio of available devices with BJT devices will help to improve current drive capability of analog circuitry and attract new research interests in various sensor implementations. Finally, to aid in the adaptation in industry and integration in systems, it would be beneficial to allow interfacing with the chip at conventional signal levels, e.g. 5 V or lower. This could either mean that the power supply voltage should be reduced to this level, or that level-shifters are employed on chip to interface with off-chip electronics. Previous work hints that this should be feasible, as inverters where successfully tested at a 5 V operation range [37].

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4

OPTO-ELECTRONICS AND 64 PIXEL IMAGE ARRAY IN SILICON CARBIDE

Engineering is achieving function
while avoiding failure.

Henry Petroski

The sensing elements are integrated with on-chip readout electronics to implement an opto-electronic system, which benefits sun position sensors by providing on-chip signal conditioning and overall sensor miniaturization. This concept is beneficial for harsh environment sensing systems in general, as it omits the need for off-chip readout electronics that need protection against the harsh environment, while enabling sensor scaling and thus cost reduction. The quadrant sun position sensor and pixel array sun position sensor are considered in this chapter in both the BICMOS7 and SICCMOS9 technologies, for prototyping and comparison purposes. Without the integration of the sensor optics that define the sun position sensor, the pixel array can be used as a UV imager on which preliminary light spot emulation measurements are performed.

Parts of this chapter have been published in 2021 IEEE 34th International Conference on Micro Electro Mechanical Systems (MEMS) (2021) [1], IEEE 35th International Conference on Micro Electro Mechanical Systems (MEMS) (2022) [2] and Nature Microsystems and Nanoengineering (2022) [3].

EXTENSIVE research effort was made over the last decades on silicon carbide photodetectors, as they make excellent visual-blind UV detectors. Over the years the technology has come a long way, leading for example to a UV-index monitoring demonstrator board [4] and UV imager [5]. Reliability studies on the aging effects of silicon carbide photodetectors show promising results, revealing little to no change in the device performance [6–8]. Schematic cross-sections of the most widely used semiconductor photodetector types are illustrated in Figure 4.1. This includes the photoconductor, Schottky, metal-semiconductor-metal (MSM), p-type/n-type doped regions (PN) junction, p-type/intrinsic/n-type doped regions (PIN) junctions and avalanche photodiode (APD). The operating principles of these different photodetector types are very similar as they all rely on the fundamental photoelectric effect. A selection of different photodetector implementations is provided in Table 4.1. The responsivity, reported in the research, is listed for specific wavelengths, with peak responsivities close to a wavelength of 300 nm for all devices. Another promising exotic topology is the graphene-based silicon carbide Schottky photodiode, reaching extremely high responsivity values [9]. None of the listed photodetectors was previously integrated with on-chip readout.

Integrating the UV photodetectors with on-chip readout allows for signal conditioning and processing. Such monolithic integration of the optical sensors and circuits is called opto-electronics and furthermore allows for UV optical sensors to be integrated in SoCs in silicon carbide technology. UV opto-electronics have applications in flame detection, satellites, astronomy, UV photography, and healthcare. At present, the only previously reported opto-electronic system in SiC was achieved in the BJT technology at the KTH in Sweden in 2020 by Hou et al. [5]. This system includes 256 addressable pixels, 1959 transistors and runs at 8.25 W and 7.7 mHz. To improve this already excellent achievement and tailor it for the sun position sensor, the Fraunhofer IISB CMOS technology from the previous chapter is used to allow for lower power consumption, faster operation and complementary devices for the photodetector readout.

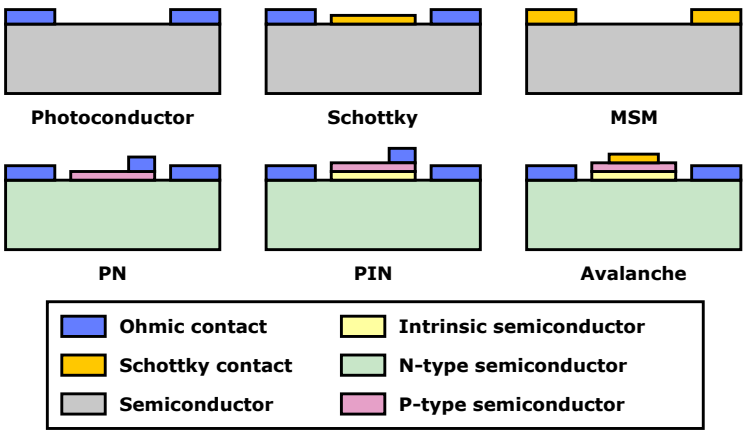


Figure 4.1: Schematic illustrations of several different semiconductor photodetector types [10, 11]. Note that the doped regions are stacked in these illustrations, but implementation in the substrate through selective ion implantation is also possible.

Table 4.1: A short overview of the extensive research already done on silicon carbide photodetectors. The listed responsivity values are rough estimates, taken from the reported graphs. Note that the biasing conditions are not equal for each reported work. Some works only reported quantum efficiency values or no spectral analysis.

Technology	Responsivity [AW^{-1}]			Material	Researchers	Year
	250 nm	300 nm	350 nm			
MSM	-[a]	-[a]	-[a]	4H-SiC	Su *et al.*	2002 [12]
Schottky	0.025	0.065	0.06	6H-SiC	Sciuto *et al.*	2017 [13]
Schottky	0.019	0.046	0.006	4H-SiC	Mazzillo *et al.*	2016 [14]
Schottky	0.018	0.044	0.01	4H-SiC	Mazzillo *et al.*	2014 [15]
Schottky	0.018	0.042	0.01	4H-SiC	Sciuto *et al.*	2014 [7]
Schottky	0.048	0.099	0.02	4H-SiC	Mazzillo *et al.*	2009 [16]
Schottky	0.16	0.13	0.04	4H-SiC	Sciuto *et al.*	2006 [17]
Schottky	-[a]	-[a]	-[a]	4H-SiC	Hu *et al.*	2006 [18]
PN	0.10	0.10	0.015	4H-SiC	Matthus *et al.*	2017 [19]
PN	0.07	0.1	0.06	4H-SiC	Prasai *et al.*	2012 [8]
PN	0.13	0.12	0.05	6H-SiC	Brown *et al.*	1993 [20]
APD	0.08	0.08	0.02	4H-SiC	Yang *et al.*	2017 [21]
APD	0.082	0.09	0.005	4H-SiC	Liu *et al.*	2008 [22]
APD	80	50	4	4H-SiC	Yan *et al.*	1999 [23]
SPAD	0.3[b]	0.15[b]	0.02[b]	4H-SiC	Hu *et al.*	2008 [24]
SPAD	0.2[b]	0.15[b]	0.03[b]	4H-SiC	Xin *et al.*	2005 [25]

[a] No spectral analysis are reported.
[b] Only quantum efficiency values are given [e-/photon].

This chapter investigates UV opto-electronics in the Fraunhofer IISB SICCMOS9 silicon carbide technology and compares it with the in-house BICMOS7 silicon technology, by first investigating single integrated photodetector devices. This is expanded by integration of CMOS readout blocks for signal conditioning that are used in the large scale system design of the imager array. The resulting system demonstrates the first implementation of an on-chip UV opto-electronic integration in 4H-SiC CMOS, which includes an image sensor with 64 active pixels and 1263 transistors on a 100 mm^2 chip.

4.1. SINGLE PHOTODETECTOR CHARACTERIZATION

The core of the opto-electronic design is the photodetector, which is sensitive only to the UV spectral band due to the implementation in SiC. This section describes the hardware design of the used photodetectors and comparison to the BICMOS7 counterparts, followed by verification of the visible blind response. Finally, considerations for the quadrant sun position sensor are given, which is deliberately kept of low complexity in favor of success rate. The pixel array image sensor is described in the proceeding sections.

4.1.1. IMPLANTED VERTICAL PHOTODETECTOR ARCHITECTURES

Most photodetectors reported in Table 4.1 are implemented in 4H-SiC, which is also the used substrate in SICCMOS9 and therefore incorporated in this work. The 4H-SiC poly-

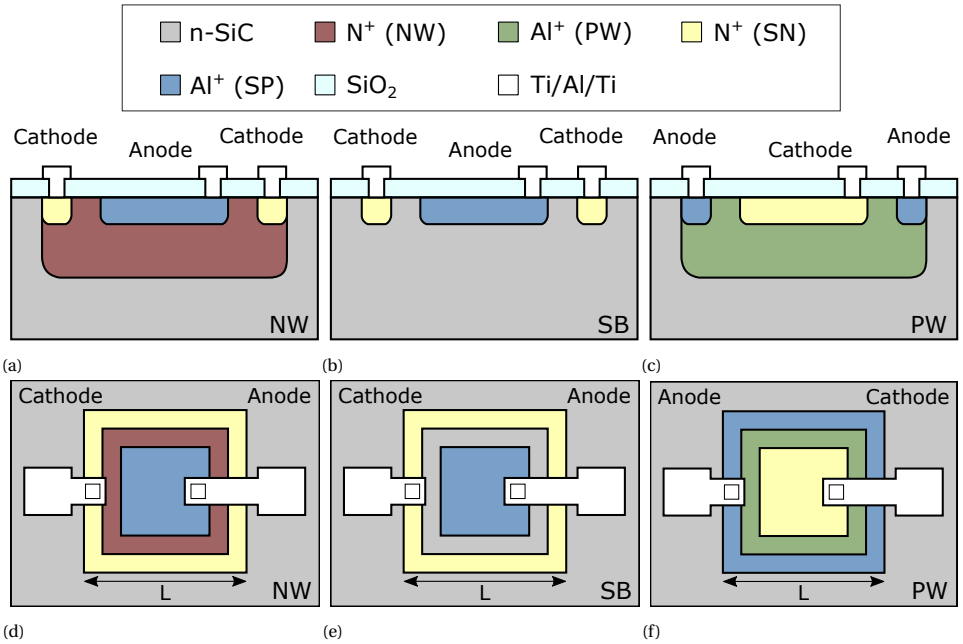


Figure 4.2: Schematic illustration of three different vertical PN photodiodes in the Fraunhofer IISB technology, using the existing CMOS design layers. The implementations are inside the n-well (NW), substrate (SB) and p-well (PW), of which the a)-c) cross-sections are provided with the d)-f) top views. Note that the substrate is n-type of similar dopant concentration as the n-well. The BICMOS7 implementation is of the NW design inside a p-type substrate (and thus complete opposite of the SICCMOS9 PW design).

type is preferred over the 6H-SiC polytype for visual-blind UV detection, as it has a larger bandgap and higher carrier mobilities (see Table 1.3) which enable superior responsivity in the UV range [8, 13]. Another reason specific for the APD, is the positive temperature dependence of the avalanche breakdown voltage in 4H-SiC, while that of 6H-SiC is negative. This is an advantage of 4H-SiC, because devices with a negative temperature coefficient are potentially unstable when driven into the breakdown regime [26].

At present, both the BICMOS7 and SICCMOS9 technologies do not include optional epi-layer stacks, which rules out the PIN and APD types. Furthermore, the Schottky and MSM types are not favorable due to reduced EQE caused by blocking and absorption of incident photons for parts of the active area. Finally, the photoconductor changes its conductivity opposed to generating a signal, which is identified as not favorable for conventional readout strategies. This leaves the PN type for integration in the SICCMOS9 opto-electronic system, of which three different vertical PN photodiodes are considered using the SICCMOS9 technology design layers. At this point it should be noted that all the mentioned types are passive photodetectors, but active alternatives exist such as the phototransistor [27]. However, these are not considered in this work as the on-chip readout is more demanding. The schematic cross-section and top view of these architectures are listed in Figure 4.2 and include implementations inside the n-well (NW), substrate (SB) and p-well (PW). The wells are contacted using highly doped guard rings,

to achieve ohmic contacts and help reducing potential cross-talk between devices. The square photodetector dimension L is measured at the guard ring and is used to label the different devices. As the BICMOS7 technology incorporates a single implanted well design layer, only a single architecture is implemented for rapid prototyping. This architecture is the opposite of the SICCMOS9 PW architecture, by using an SP anode inside an n-well cathode that is implemented in a p-type substrate. The BICMOS7 and SICCMOS9 devices have a 700 nm and 50 nm SiO_2 active area passivation layer respectively.

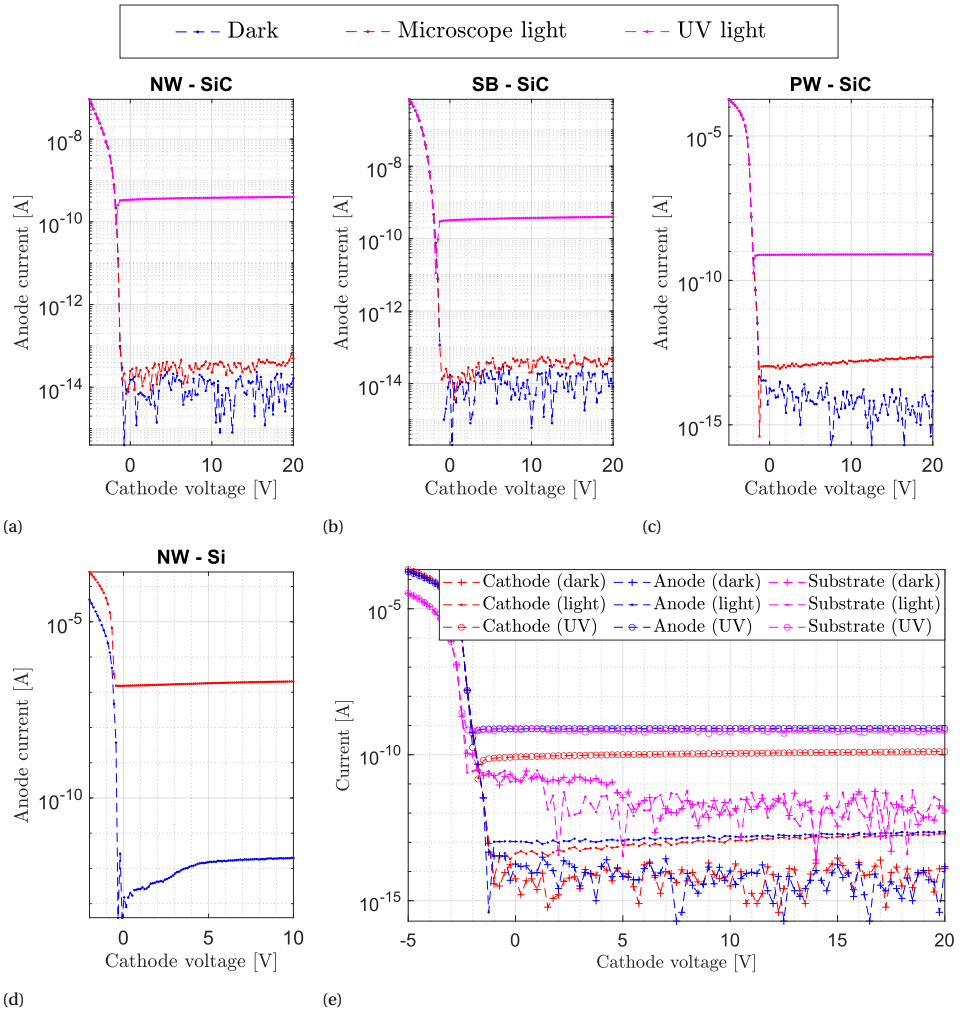


Figure 4.3: The measured anode current for different cathode biasing on die (-1,0) of the different vertical SiC photodiode 80 × 80 µm implementations in the a) n-well (NW), b) substrate (SB) and c) p-well (PW). Similarly, the measured anode current on die (0,0) of d) the Si reference implementation. All signals are reported of the e) PW implementation for further analysis. The anode is biased at 0 V and the PW substrate connection at 20 V. Different illumination conditions are used to extract PDCR indications.

The photodiode response is measured on wafer-level using the setup described in Section 3.1.1, with the addition of four mounted discrete 5 mW SMD3535 265 nm UV-C LEDs, with a full width at half maximum (FWHM) of 10 nm. The response of the three SiC designs in Figure 4.2 is reported in Figures 4.3a to 4.3c for different light conditions and bias, showing strong responses to UV light that are constant over positive cathode bias. In contrast, the response to microscope light shows a small but measurable increase of the anode current. The response of the Si reference in Figure 4.3d shows a strong response to microscope light that is not as constant in dark mode over the measured bias range. Since the NW and SB cathodes are connected to the substrate, the current at the cathode is generated at multiple devices and therefore not reported in the plot. In contrast, the PW variant separates the cathode and substrate contacts and all signals are reported separately in Figure 4.3e, the same holds for the Si NW (Figure C.5).

The photo-to-dark current ratio (PDCR) figure of merit [28, 29] is calculated by

$$\mathrm{PDCR}(\lambda) = \frac{I_{\mathrm{photo}}(\lambda) - I_{\mathrm{dark}}}{I_{\mathrm{dark}}}, \tag{4.1}$$

where λ is the wavelength, I_{photo} the wavelength dependent generated photo current and I_{dark} the dark current. The dark current and PCDR towards microscope light and UV light are listed in Table 4.2. The SiC devices show a very low dark current that is constant over the different device areas, resulting in averages of 11 fA (NW), 11 fA (SB) and 8 fA (PW). Since the reported values are constant over area, the measured dark current is dominated by shared geometries such as the substrate and contacts. The NW and SB are therefore identical and differ from the PW, as the p-well is electrically insulated

Table 4.2: Overview of the PDCR results on wafer-level on 35 dies for different area (labels refer to L in Figure 4.2) and type of photodetector considering the anode current. For each respective case (dark/light/UV), the average anode current for a cathode voltage > 0 V is considered.

Device	Dark current [fA]	PDCR (light)	PDCR (UV)
SiC - SB50	11.9 ± 1.6	3.5 ± 1.6	$(1.1 \pm 0.3) \times 10^4$
SiC - SB60	11.4 ± 1.0	4.8 ± 1.5	$(3.1 \pm 0.7) \times 10^4$
SiC - SB70	10.8 ± 0.7	6.5 ± 1.7	$(6.3 \pm 1.4) \times 10^4$
SiC - SB80	11.3 ± 1.8	7.3 ± 2.8	$(9.4 \pm 3.3) \times 10^4$
SiC - NW50	11.3 ± 0.8	4.2 ± 1.4	$(1.3 \pm 0.4) \times 10^4$
SiC - NW60	11.4 ± 1.1	4.3 ± 1.6	$(3.0 \pm 0.8) \times 10^4$
SiC - NW70	11.1 ± 1.1	6.4 ± 1.6	$(6.7 \pm 1.6) \times 10^4$
SiC - NW80	11.8 ± 1.6	6.7 ± 2.4	$(9.4 \pm 3.0) \times 10^4$
SiC - PW50	7.4 ± 0.8	12.2 ± 2.9	$(9.5 \pm 2.1) \times 10^4$
SiC - PW60	8.6 ± 4.0	22.1 ± 7.0	$(13.6 \pm 4.1) \times 10^4$
SiC - PW70	7.9 ± 0.8	39.1 ± 8.4	$(23.1 \pm 4.8) \times 10^4$
SiC - PW80	8.0 ± 0.7	64.8 ± 16.2	$(32.8 \pm 8.3) \times 10^4$
Si - NW50	$(4.4 \pm 1.4) \times 10^2$	$(25.0 \pm 8.5) \times 10^4$	-
Si - NW60	$(5.8 \pm 1.7) \times 10^2$	$(33.2 \pm 11.9) \times 10^4$	-
Si - NW70	$(7.7 \pm 2.4) \times 10^2$	$(35.8 \pm 12.7) \times 10^4$	-
Si - NW80	$(10.5 \pm 2.8) \times 10^2$	$(36.1 \pm 16.2) \times 10^4$	-

from the substrate and the contact silicides are different. In stark contrast, the Si devices exhibit dark currents that are two orders of magnitude larger, and are proportional to the photodetector area. This difference in dark current magnitude originates from the difference in intrinsic carrier density, which is many orders of magnitude lower for silicon carbide compared to silicon [30]. Typical values for the dark currents in literature are 1 nA cm^{-2} and 5 pA cm^{-2} for silicon and 4H-SiC respectively [31]. From Table 4.2 values of 16 nA cm^{-2} and 0.3 nA cm^{-2} are extracted for Si and SiC respectively, indicating a good match for the Si devices and a higher found value for the SiC devices.

The response to microscope light of the SiC devices is very low, though noticeably higher for the PW implementation. In contrast, the Si devices PDCR to microscope light is in the order of 10^5. The PDCR towards UV light is only measured for the SiC devices and is above 1×10^5 for the PW and above 1×10^4 for the NW and SB implementations, making the PW implementation superior when measured at the anode. However, considering all PW connections in Figure 4.3e reveals that the anode current is equal to the cathode current in the dark/light cases, but equal to the sum of the substrate and cathode currents in the UV case. This shows that generated photocurrent is leaking away to the substrate, reducing the signal to what is measured at the cathode about ten times. Future implementations should improve the PW architecture in Figure 4.2 by suppressing the unintentional horizontal PN photodiode from anode to substrate, possibly by extending the p-well. A similar effect is observed in the Si implemenations (Figure C.5)

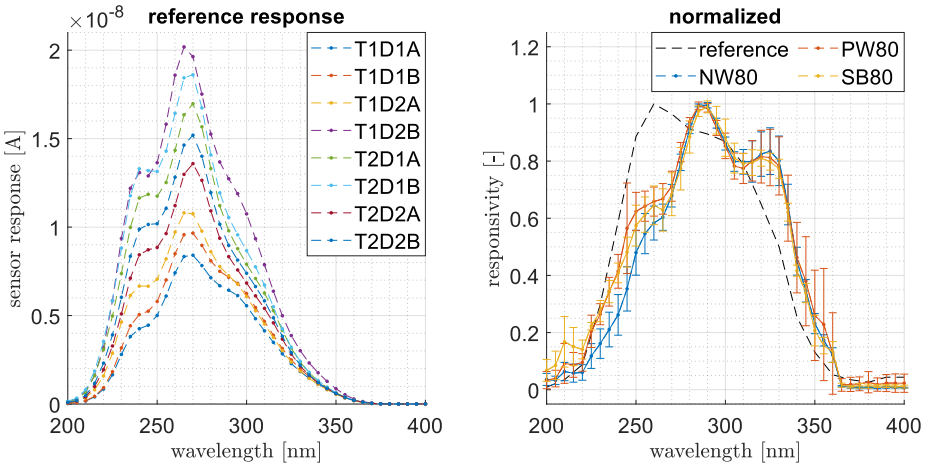
4.1.2. OPTICAL RESPONSIVITY COMPARISON

The work on optical responsivity measurements was performed by M. Orvietani as part of his thesis work in collaboration with and under supervision of the author.

The reported PDCR results of the three photodiode types for a UV and visible light source give clear indication that the devices work as intended. To investigate the spectral range deeper, the SiC device responsivity is measured for fixed wavelengths in the range of interest. The responsivity is an often used figure-of-merit that also takes into account the incident optical power through

$$R(\lambda) = \frac{I_{\text{photo}}(\lambda) - I_{\text{dark}}}{P_{\text{opt}}(\lambda)}. \tag{4.2}$$

The SiC photodiodes are connected to a large resistance in parallel to transform the generated photo current in a voltage for measurement. The samples are measured by an in-house UV responsivity measurement system, which used the ILD-D2-QH Deuterium-Halogen UV light source from Bentham that is coupled to an iHR320 monochromator from Horiba to selectively cycle through the spectral range of 200–400 nm. Using a total of eight identical reference photodiodes [19, 32] (consisting of two dies each containing four devices), it was found that the device response varies substantially in magnitude (Figure 4.4a). Therefore, it is opted to normalize the measured responsivity curves for comparison and the results are reported in Figure 4.4b. Compared to the reference, the three devices types exhibit a shifted peak responsivity from 260 nm to 290 nm. This shift is explained by differences in the doping profile or used ARC coating of the SICCMOS9 design layers and the process used for the reference diodes, as this strongly effects the absorption depth for photons at these wavelengths [19]. Unfortunately, the EQE (see



(a) (b)

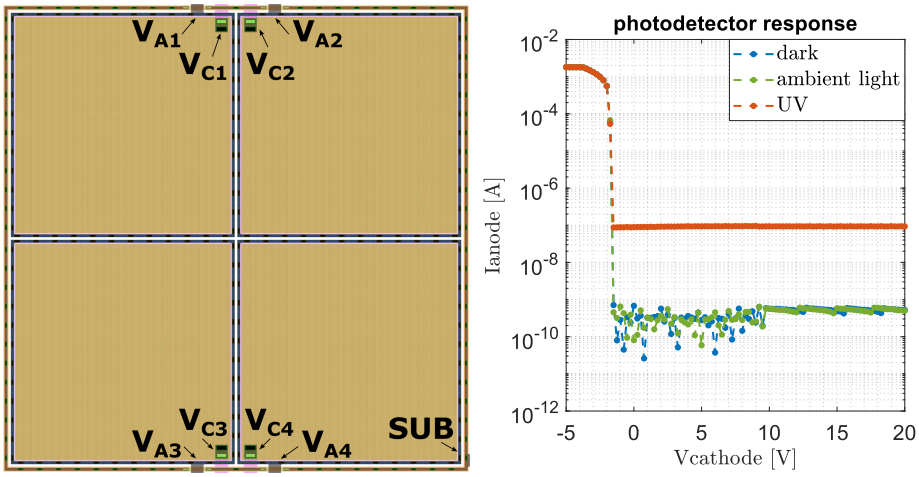
Figure 4.4: Sensor response of a) eight identical reference devices, showing significant deviations in the magnitude of the response, and the normalized responsivity measurements of b) the NW80, PW80 and SB80 devices. The normalization is done on the results of four different devices of the same type and then averaged to find the reported curves. Note that the standard deviation is derived as the deviation between the four normalized measurements results of each device type.

Section 2.4.2) is not extracted due to the large deviation in absolute signal levels, which should be pursued in future work by improving the in-house measurement setup and device matching. Other figure of merits exist, such as the specific detectivity [10, 33], but typically require more device parameters and are therefore not considered in this work.

The reported responsivity curves and PDCR factors for specific illumination conditions, provide a starting ground for tailoring the integrated photodetectors of the opto-electronic system. To complement this, one can use the strategy for estimating the photo current generation given in Section 2.4.1 to aid the decision regarding scaling (see Figure C.7). Using previous responsivity reports of photodetectors in BICMOS7 in the visible range [34], it is estimated to generate $I_{0,\mathrm{Si,sol}} = 16.1\,\mathrm{mA\,cm^{-2}}$ considering the solar spectrum without atmospheric absorption [35]. Following this procedure for the reported SiC reference responsivity [19] it is estimated to generate $I_{0,\mathrm{SiC,sol}} = 0.4\,\mathrm{mA\,cm^{-2}}$, which is a reduction by a factor of roughly 40. Comparing this to the measurements on the PW80 in Figure 4.3c, the used LEDs are considered instead of the solar spectrum, resulting in $I_{0,\mathrm{SiC,LED}} = 86\,\mu\mathrm{A\,cm^{-2}}$. The measured current that is generated is 0.79 nA, which equals $12\,\mu\mathrm{A\,cm^{-2}}$ normalized over area. This comes close to the estimated value, especially considering transmission losses. Finally, the albedo insensitivity figure-of-merit Ψ_{ARR} of Equation 2.34 is calculated for the two photodetector technologies. This equals 1.56 for Si BICMOS7 and 3.84 for SiC SICCMOS9.

4.1.3. QUADRANT SUN POSITION SENSOR LAYOUT DESIGN

The generated photocurrent of each photodetector in the quadrant sun position sensor are measured off-chip by dedicated measurement equipment, which mitigates any de-



(a) (b)

Figure 4.5: Overview of the quadrant sun position sensor photodetector a) layout design and b) PDCR response. The individual photodiode connections for the anode V_A and cathode V_C are given. The photodetectors share a single substrate connection SUB that is positioned as a ring around the active area.

sign difficulties of on-chip readout caused by the limited capability of simulating these sensors using the provided design models. Moving forward, a sensible first step would be to include a transconductance amplifier, preferable in photoconductive mode[1], to convert the photocurrent signal into a voltage, which is more convenient to transport off-chip or for use in on-chip circuit implementations of the readout algorithm. Integrating the readout algorithm on chip entails the circuit implementation of Equation 2.16, which then also allows for calibration of the sensor if needed. The circuit implementation can be analog based, by using blocks that do addition and division, or it can be digital based, which consists of analog-to-digital conversion and logic gates.

The quadrant sun position sensor photodetectors are implemented by the PW type, as these showed the largest PCDR. As no on-chip readout is integrated, the signal has to be transferred off-chip and measured with high accuracy. To reduce the impact of the packaging, interface boards and cables on the signal, it is decided to use larger photodetectors to have a higher absolute signal value. The area used is a trade-off with the needs of other test structures and so an optimal value for the multi-project design was selected at 0.9 × 0.9 mm for each photodetector. The layout overview is given in Figure 4.5a and houses four separated photodetectors that have off-chip connections for individual contacts to each anode or cathode. In contrast to the reported smaller photodetectors, the quadrant sensor photodiodes are covered by the 400 nm field oxide, to avoid potential difficulties in the subsequent wafer-level packaging in the next chapter due to large recessed areas. Therefore, the PDCR is again measured and reported in Figure 4.5b on a packaged device (connection diagram in Table C.1 and fig. C.8) with a single 5 mW

[1] In photoconductive mode, the diode bias is held constant and often at 0 V, providing a linear and fast response compared to the photovoltaic mode, which has a logarithmic and slow response.

SMD3535 265 nm UV-C LED spaced at a similar distance and paired to previously mentioned SMU equipment. The PDCR towards ambient light and UV equal 0.998 and 157 respectively, from which excellent preliminary visible blindness is concluded. The generated photocurrent under UV light is 92 nA, which equals 14 µA cm^{-2} normalized over area, and matches well with the found current generation for the smaller photodetectors. Hence it is concluded that the thicker passivation layer on top of the photodiodes has a negligible increase of absorption for the application. The dark current is much larger than reported in Table 4.2, which is due to the different measurement setup used here that includes a packaged device in a breadboard with unshielded connections.

4.2. ACTIVE PIXEL SENSORS

The single photodetectors are integrated with CMOS readout to implement addressable pixels, which allows for the design of a scalable array of integrated photodetectors. These addressable pixels are individually investigated in this section and paired with CMOS readout blocks that are reported in the preceding chapter.

4.2.1. THREE TRANSISTOR PIXEL READOUT

The addressable pixels are based on the three transistor active pixel sensor (3T APS), of which the text book circuit is illustrated in Figure 4.6a. The circuit operation starts by performing a RST cycle, that consists of a pulse to HIGH, which stores charge on the M_{sf} gate. After the RST cycle, the stored charge leaks away proportional to the generated photo current. The pixel is selected by forcing a HIGH signal at ROW that connects the M_{sf} and M_{al} devices to implement a source follower, which translates the charge

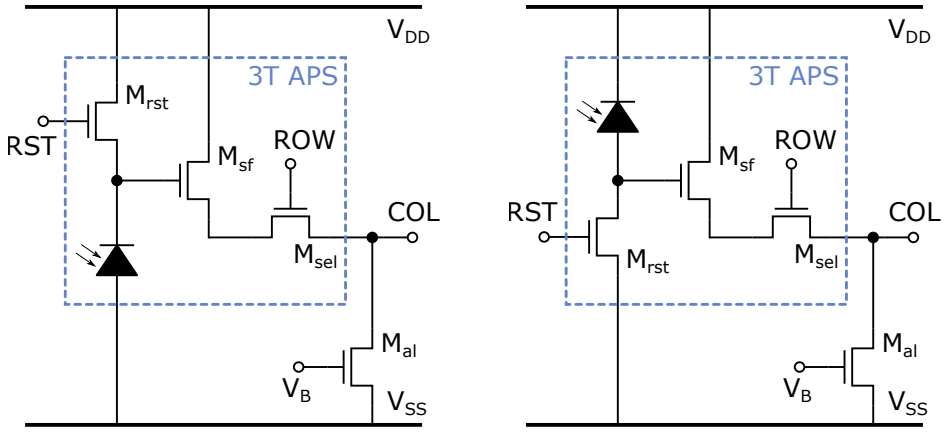


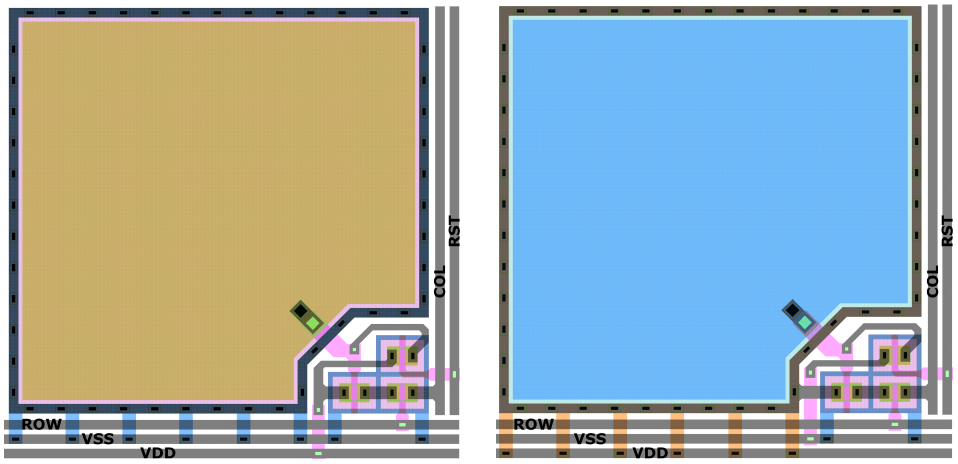
Figure 4.6: Illustration of a) the text book 3T APS in combination of the PW photodetector and b) the alternative 3T APS in combination of the NW or SB photodetector. Both variants require an active load biased by V_B to complete the source follower in the pixel. The pixel is controlled by a reset RST, row selection ROW, column output COL, high voltage V_{DD} and low voltage V_{SS}. The pixel design has minimum size devices and two 20 × 8 µm or 20 × 10 µm in series as the active load for BICMOS7 or SICCMOS9 respectively.

level to a voltage at the COL node. However, this architecture dictates that the anode is connected to ground and the cathode connected to a pixel specific node.

As the goal is to integrate this circuit in the SICCMOS9 technology, one should consider that the n-type wells are electrically connected through the n-type 4H-SiC substrate. As the PMOS body is generally biased at the power supply level, the cathode contacts of the NW and SB photodetector types are connected to the power supply level as a consequence. This contradicts the text book 3T APS and therefore a re-arranged topology is proposed for the NW and SB types, as depicted in Figure 4.6b. The roles of M_{rst} and the photodiode are swapped, meaning that the photodiode charges the gate proportional to generated photo current and the RST cycle discharges any stored charge.

The layout design of both 3T APS pixel types in SICCMOS9 is given in Figure 4.7, which both have a fill factor of 77 % and 0.25 mm^2 photodetectors. In comparison, the BICMOS7 3T APS layout (see Figure C.6) has a fill factor of 73 % and 0.18 mm^2 photodetectors. The ROW, COL and power lines are routed around the active area of the photodetectors. This ensures that no incident light is blocked or absorbed, but comes at the cost of area consumption and thus a lower fill factor. Future implementations would benefit from the use of UV transparent electrodes, like indium tin oxide (ITO) or other material [36], and a denser pixel array design by routing these lines over the pixels.

Both the 3T APS blocks are easily interconnected in an addressable array by connecting the ROW and COL pins of each block in the respective row or column, which is implemented in the next section (see Figure 4.13). Finally, it should be noted that there are several noise sources in the 3T APS circuit, including shot noise, thermal noise, 1/f noise and reset noise, which differ in magnitude for the respective components. A common noise problem when used in an array is the phenomena of fixed pattern noise, which is caused by non-uniformity between pixels. To counteract this noise, correlated



(a) (b)

Figure 4.7: Layout design in SICCMOS9 of the a) text book (using PW) and b) alternative (using NW) 3T APS architectures. The depicted blocks are 0.57 × 0.57 mm, which already accounts for some clearance when implementing in an array. Note that some local routing is implemented in the polysilicon layer.

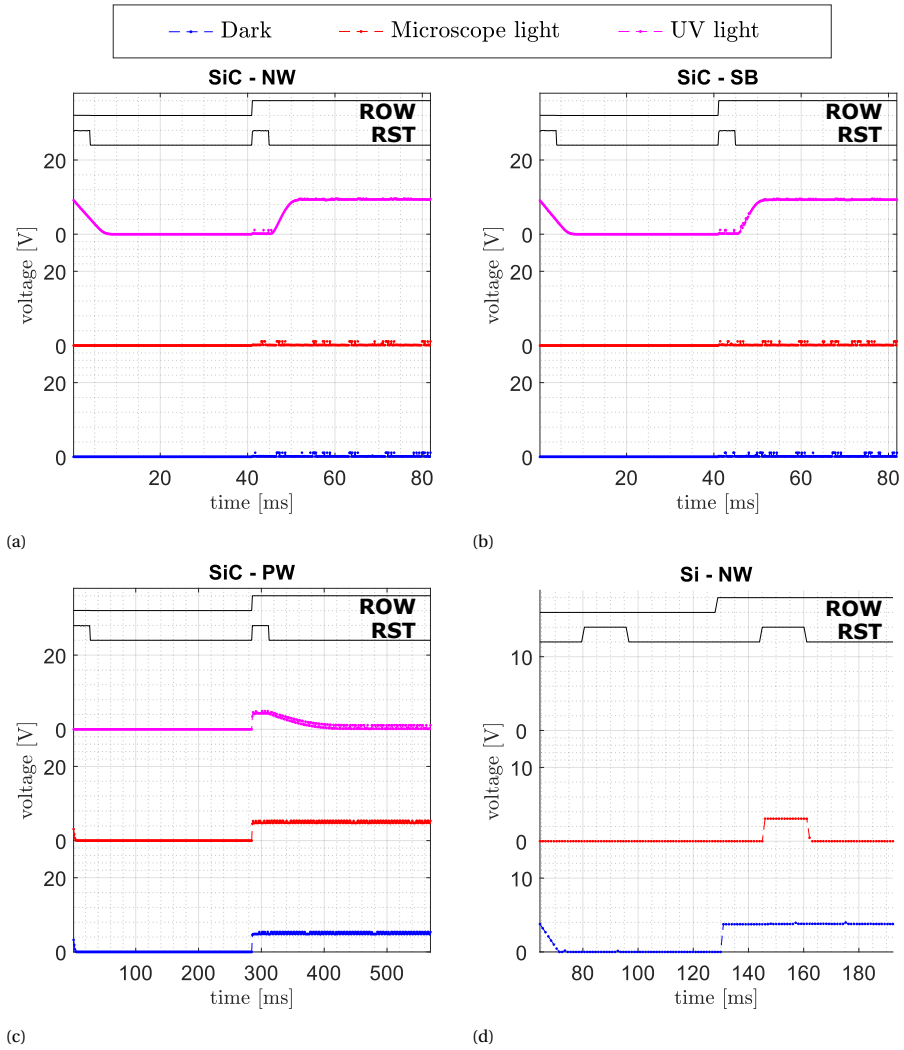


Figure 4.8: The measured raw 3T APS pixel response of the a) NW, b) SB and c) PW types in the SICCMOS9 technology on die (-1,0) and d) the NW type in the BICMOS7 technology on die (0,0). Note the minor difference in signal timing for the BICMOS7 measurement. The active load of the raw pixel is biased at 1.4 V and 6.0 V for BICMOS7 and SICCMOS9 respectively. Each measurement is a segment of a continuous measurement to avoid start-up discrepancies.

double sampling circuits are proposed [37], but not integrated in this work.

The transient measurements of the 3T APS are performed using the custom DAQ (see Section 3.1.1) and the raw pixel output results are given in Figures 4.8a to 4.8d for different illumination conditions. The pixel is disconnected (ROW = LOW) from and connected (ROW = HIGH) to the output. As expected from the single SICCMOS9 photodetector results, the NW and SB perform near identical and charge to a V_{high} of

(9.4 ± 0.2) V under UV illumination, while remaining at low voltage in the other cases. The PW implementation is reset to a V_{high} of (5.0 ± 0.3) V and discharges to low voltage under UV illumination, while remaining at high voltage in the other cases. The NW and SB charge time is (7 ± 1) ms and the discharge time of the PW is (87 ± 7) ms, which corresponds closely to the reduced PW signal of about ten times due to the unintentional PN junction to the substrate. The BICMOS7 implementation shows similar behavior as the SICCMOS9 PW implementation, but with much faster response that is attributed to the higher optical power of the microscope light.

4.2.2. DIGITAL OR ANALOG PIXEL OUTPUT

The reported 3T APS photodetectors operate as intended, and are designed to maximize the fill factor for later use in an array. CMOS readout blocks are connected at the 3T APS output for signal conditioning, relaxing requirements for readout systems. Two CMOS circuit blocks are connected at the APS output for signal conditioning before further on-chip manipulation and off-chip interfacing. First, the previously reported comparator is integrated (see Figure 4.9a) to effectively digitize and invert the photodetector response. Second, the previously reported unity-gain buffer is integrated (see Figure 4.9b) to provide a buffered analog version of the photodetector response. Note that the integration of these CMOS readout blocks is indifferent to the choice of 3T APS topology.

The transient measurement results of the integrated comparator topology in both technologies is given in Figure 4.10. The response time is the time between the RST falling edge and output response, while ROW is HIGH. The SICCMOS9 NW and SB response time is near identical to that of the raw pixel, while the PW response time is about 7 ms longer. This indicates a potential asymmetry in transition time of the comparator. The BICMOS7 implementation shows similar behavior to the SICCMOS9 PW, but with a significantly faster response time. Direct comparison is not of interest, as the optical power differences are not quantified.

The transient measurement results of the integrated unity-gain buffer topology in

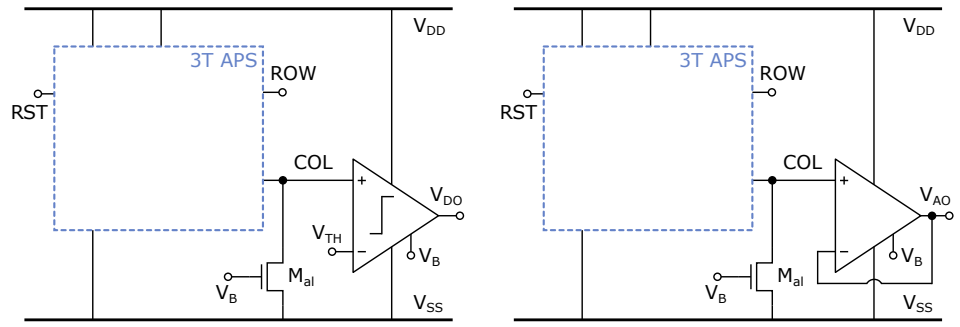


Figure 4.9: Illustration of CMOS readout blocks connected to the 3T APS, including a) the comparator and b) the unity-gain buffer. Note that both types of 3T APS are connected identically to the readout blocks. The bias levels are combined to a single pin V_B, which is also connected to the separately annotated comparator threshold V_{TH} to allow 6-pin wafer-level measurement.

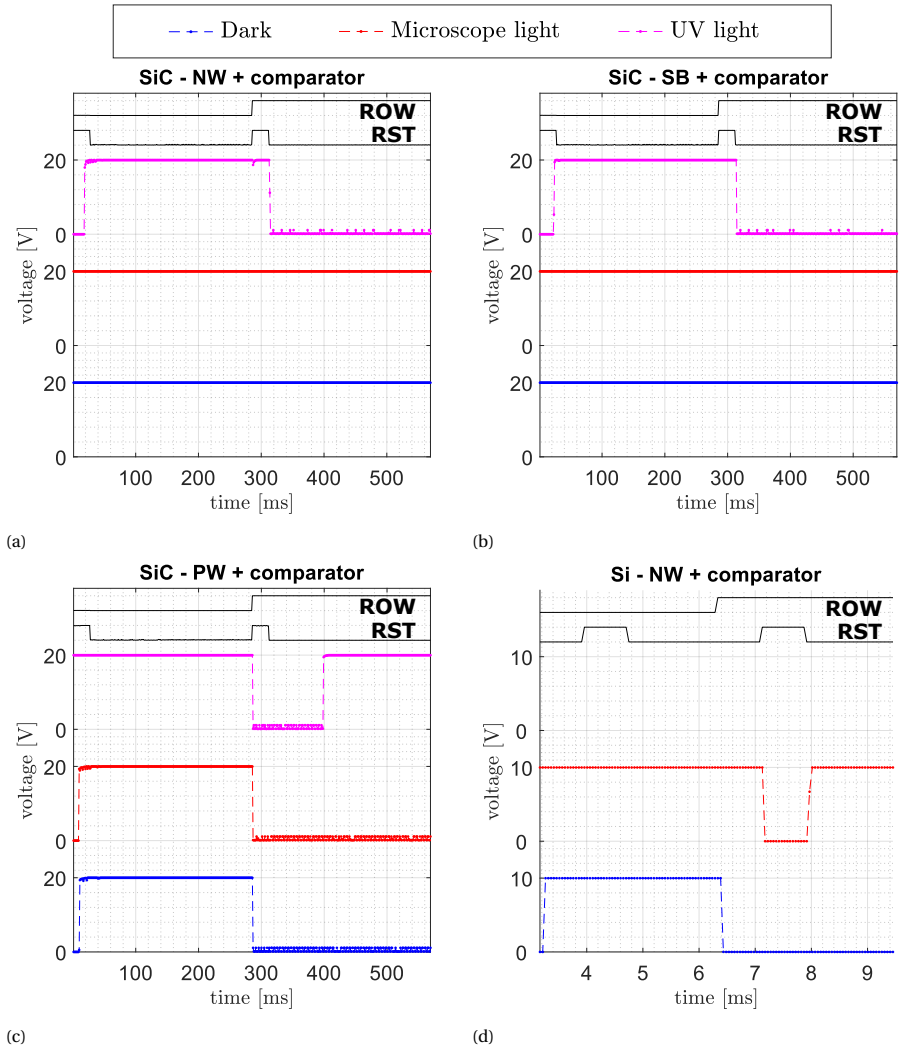


Figure 4.10: The measured 3T APS pixel response connected to an integrated comparator of the a) NW, b) SB and c) PW types in the SICCMOS9 technology on die (-1,0) and d) the NW type in the BICMOS7 technology on die (0,0). Note the minor difference in signal timing for the BICMOS7 measurement. The circuit is biased at 1.4 V and 1.5 V for BICMOS7 and SICCMOS9 respectively. Each measurement is a segment of a continuous measurement to avoid start-up discrepancies.

both technologies is given in Figure 4.11. The reset pulse brings the buffer output voltage to a high level in the UV case for all architectures. The NW and SB response times are (151 ± 67) ms and (168 ± 50) ms respectively and the PW decay time is (378 ± 160) ms. In these results, the voltage buffer is not able to keep up with the APS signals for the applied UV intensity. This could be improved by optimized hardware design and device modelling. The BICMOS7 NW shows similar behavior to the SICCMOS9 PW.

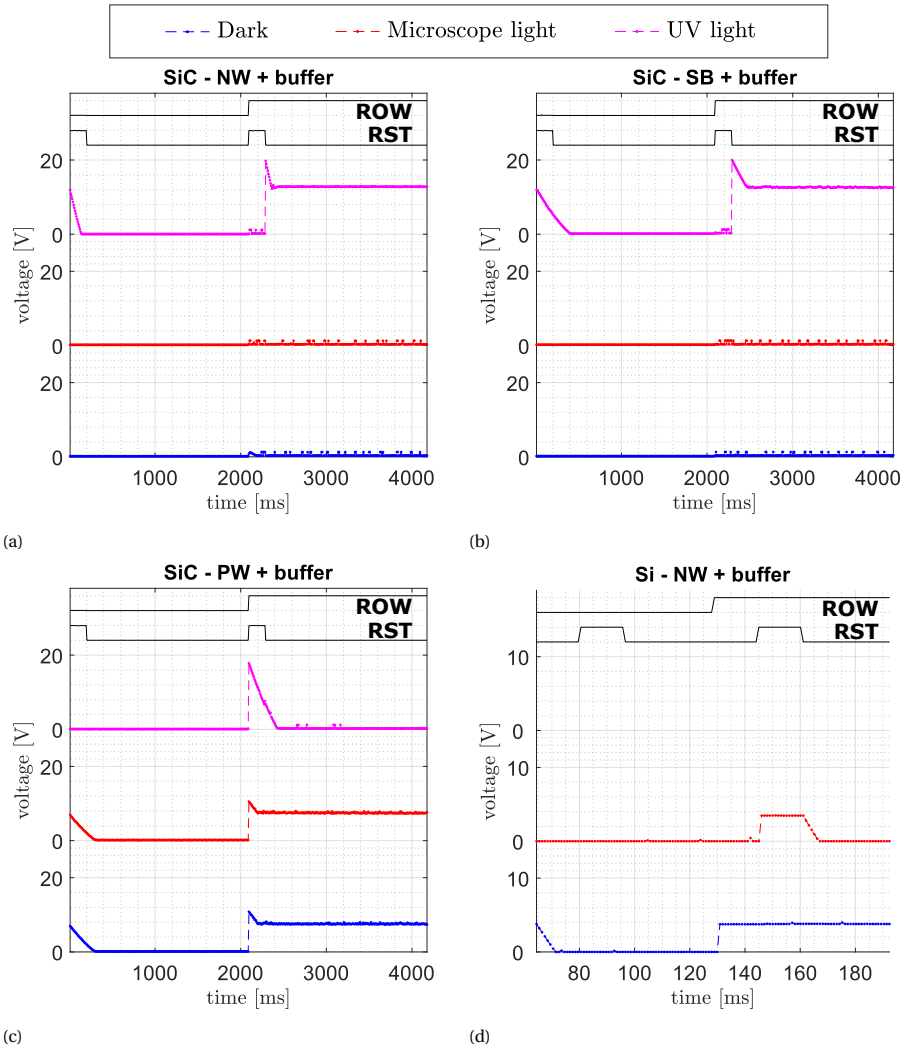


Figure 4.11: The measured 3T APS pixel response connected to an integrated unity-gain buffer of the a) NW, b) SB and c) PW types in the SICCMOS9 technology on die (-1,0) and d) the NW type in the BICMOS7 technology on die (0,0). Note the minor difference in signal timing for the BICMOS7 measurement. The circuit is biased at 1.4 V and 1.5 V for BICMOS7 and SICCMOS9 respectively. Each measurement is a segment of a continuous measurement to avoid start-up discrepancies.

4.2.3. PIXEL ARRAY LAYOUT DESIGN

Due to area constraints in the multi-project design, only a single integrated pixel array system can be integrated. From the investigated pixel types it is decided to integrate the PW photodetector, as it allows for the conventional 3T APS pixel topology, even though this photodetector was found to have leakage current issues. The pixel layout dimensions do not allow for a large array to most standards, though it is decided to not further

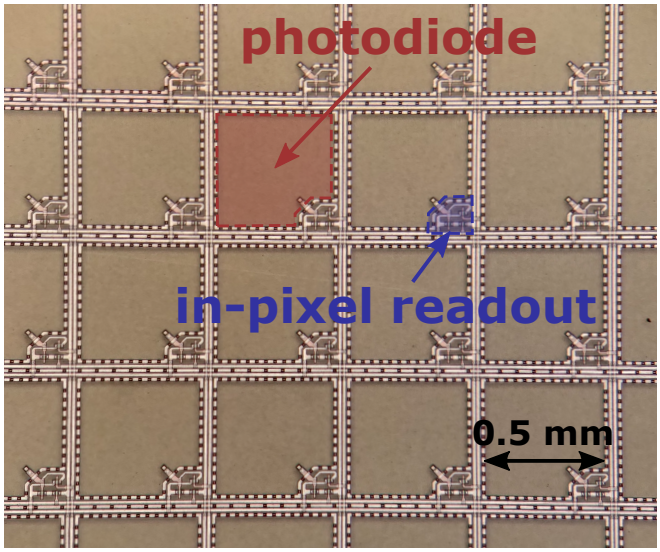


Figure 4.12: Micro photograph of the partial pixel array in SICCMOS9, implemented by the PW photodetector and text book 3T APS in-pixel readout. The global metal lines allow for connecting the ground, supply voltage and biasing to each pixel, as well as addressing each row and column.

attempt miniaturization in this stage, but rather aim for a functional prototype with a higher probability of success. As such, a 8×8 pixel array is designed with resulting dimensions of 4.6×4.6 mm. Comparing with the sole previous report of a pixel array in a SiC BJT technology [5], which is a 16×16 pixel array with dimensions of 4.8×5.9 mm.

The overview of the inter-pixel connections is depicted in Figure 4.12. Without further integration of CMOS readout and control blocks this array could be operated by 20 off-chip connections, which is considered not practical and not pursued in this work. Future implementations should focus on miniaturization, where anti-reflection coatings and transparent metal lines play roles towards increasing the signal per pixel area.

4.3. IMAGE ARRAY SENSOR SYSTEM

The 8×8 pixel array sensor is integrated with control and readout electronics to implement a sequential system[2]. This section illustrates the system circuit and layout design and the verification of its operation through measurements, for both Si and SiC technologies. The implementation in Si is used for rapid prototyping and feedback for the SiC design.

4.3.1. CIRCUIT DESIGN OF THE 64 PIXEL ARRAY SENSOR

The schematic block diagram of the image array system is highlighted in Figure 4.13, of which the separate blocks are discussed in the following paragraph. To address individual pixels, an address generator sequentially iterates through all pixels on a clock signal

[2] Sequential logic circuits not only depend on the current input values, but also on preceding input values [38].

using a 6-bit address word Q. The most significant 3-bit half is fed to the row decoder and the least significant 3-bit half to the digital and analog column decoders. Each pixel column COL is connected to an analog processor, which passes the analog pixel values COLA as well as a digitized representation COLD. These two separate output signal

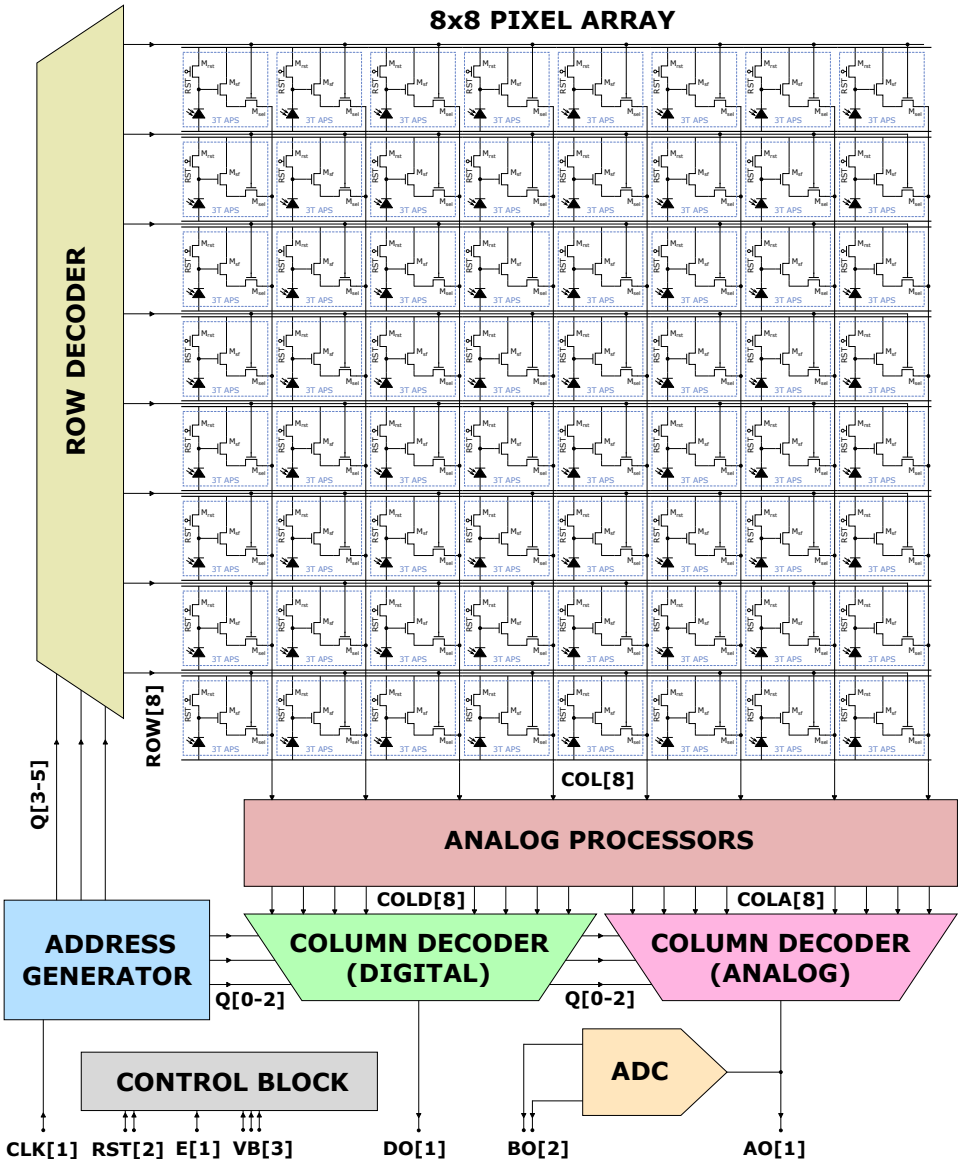


Figure 4.13: Schematic overview of the image array sensor system functional block design. The system is controlled by the global inputs CLK, RST, E and VB and has three output channels DO, AO and BO. Note that not all intermediate signals are depicted in favor of readability.

paths call for dedicated column decoders, to pass a single digital DO or analog AO column output off-chip. The analog output is furthermore connected to an ADC, which outputs a 2-bit representation BO of the analog output. Finally, the control block toggles on signal E between 7-pin or 10-pin mode for controlling the complete system[3]. The 7-pin mode allows for rapid wafer-level characterization to identify broken devices before packaging (the probe station allows up to 7 probe needles). The 10-pin mode provides control over separate bias levels and reset signals if required. When packaged, many intermediate signals are passed off-chip to validate the correct operation of the system. All signals passing off-chip go through buffers that are capable of driving larger loads.

The address generator (Figure 4.14a) is implemented by a basic 6-bit asynchronous binary counter, based on d-flipflops. The analog processor (Figure 4.14b) has eight channels, of which a single channel consists of the active load (transistor M_{al}), a comparator to digitize the output and a unity-gain buffer to pass the analog output. The control block (Figure 4.14c) consists of two analog 1-bit multiplexers and a single digi-

[3]The 7-pin mode includes VDD, GND, E, CLK, global RST, global VB and DO.

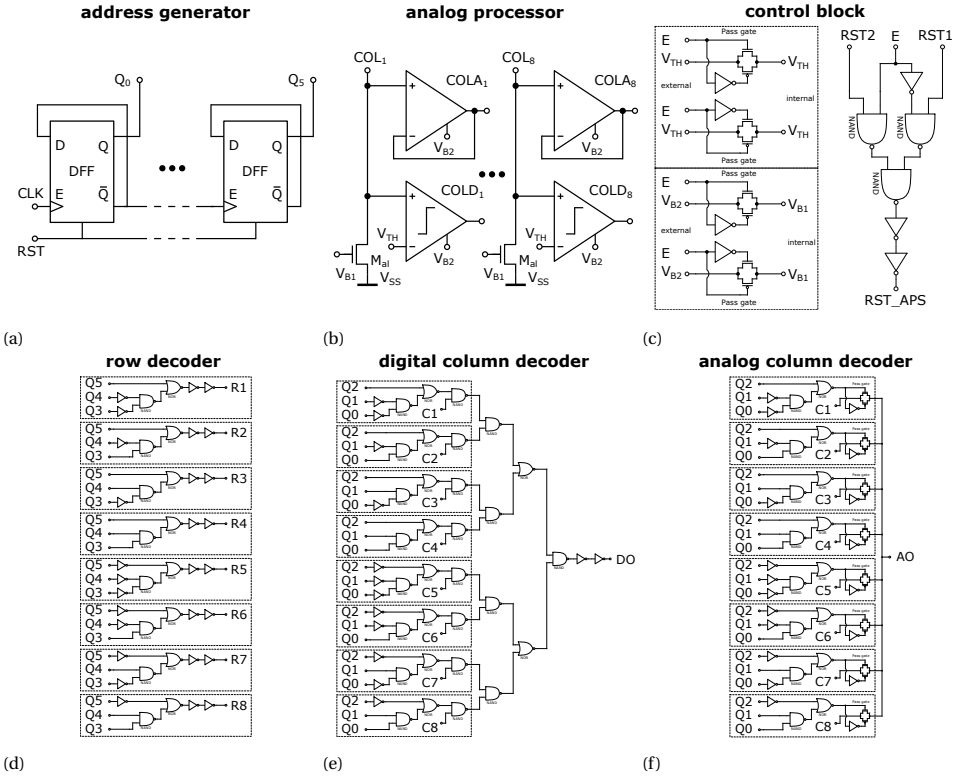


Figure 4.14: Circuit designs of the functional blocks in the opto-electronic system, including the a) address generator, b) analog processor, c) control block, d) row decoder, e) digital column decoder and f) analog column decoder. The used unit blocks are characterized in Section 3.3.

Table 4.3: Truth table of the digital and analog column decoders in both technologies, for inputs Q0-2 and outputs C1-8 (corresponding to COLD and COLA). A connection mistake in the BICMOS7 design results in an unconventional readout order, which is corrected in the SICCMOS9 design but still suffers from opposite readout orders for the analog and digital representation.

Column address			BICMOS7		SICCMOS9	
Q2	Q1	Q0	DO	AO	DO	AO
0	0	0	C6	C6	C8	C1
0	0	1	C5	C5	C7	C2
0	1	0	C8	C8	C6	C3
0	1	1	C7	C7	C5	C4
1	0	0	C2	C2	C4	C5
1	0	1	C1	C1	C3	C6
1	1	0	C4	C4	C2	C7
1	1	1	C3	C3	C1	C8

tal 1-bit multiplexer. For E = HIGH, the internal signals are connected to their external counterparts (10-pin mode), but for E = LOW the internal analog signals are all connected to V_{B2} and the internal digital signals to RST1. The row decoder (Figure 4.14d) consists of a NAND and NOR gate with two inverters to drive the ROW address lines. It should be noted that ROW1 is connected to the bottom or top row as design choice in BICMOS7 and SICCMOS9, respectively. The digital column decoder (Figure 4.14e) is implemented by a 3-bit multiplexer that consists of inverters, NAND and NOR gates. Finally, the analog column decoder (Figure 4.14f) is implemented by a 3-bit multiplexer that is comparable to the digital counterpart, with the important addition of pass-gates to pass the selected analog signal.

Connection errors in the column decoders causes different readout orders, as provided by Table 4.3. The order of Q0-2 is reversed in BICMOS7 (see Figure C.11), resulting in readout of the columns out of order. This error is corrected for the SICCMOS9 implementation, though the digital column outputs are connected in reversed order, meaning that the digital outputs are read out from right-to-left and the analog outputs are read out from left-to-right. So in conclusion, the BICMOS7 implementation moves through the rows bottom-to-top and through the columns out of order, while the SICCMOS9 implementation moves through the rows top-to-bottom and the columns in order but opposite direction for digital or analog outputs. These connection mistakes illustrate the importance of proper LVS checks when moving towards implementations with higher device counts.

4.3.2. HARDWARE DESIGN AND FABRICATION RESULTS

The showcased integrated system is the result of meticulously designing the layout of each functional block, while adhering to the square 10×10 mm design space. As no tools for automated layout generation are available in both technologies, the practised procedure contained many feedback loops to optimize the used area. The fabricated BICMOS7 chip is displayed in Figure 4.15 and the SICCMOS9 chip in Figure 4.16, with the complete layout designs provided in Figures C.3 and C.4. Note that the BICMOS7 de-

sign houses the pixel array, quadrant sensor and PCM structures within the 10 × 10 mm design space, while the SICCMOS9 design only houses the pixel array. The SICCMOS9 quadrant sensor and PCM are placed on the multi-project chip (see Figure C.2) and PCM chips (see Figure C.1) respectively. Bondpads of 0.19 × 0.19 mm are spaced evenly at the chip outline, which allows for ease in the wire bonding process, and the bottom right of the chip houses the 7 probe pads for wafer-level measurement. Circuits that required many pin connections could not be measured on wafer level and thus required wire bonding. The silicon chip wire bonding connections are listed and indicated in Ta-

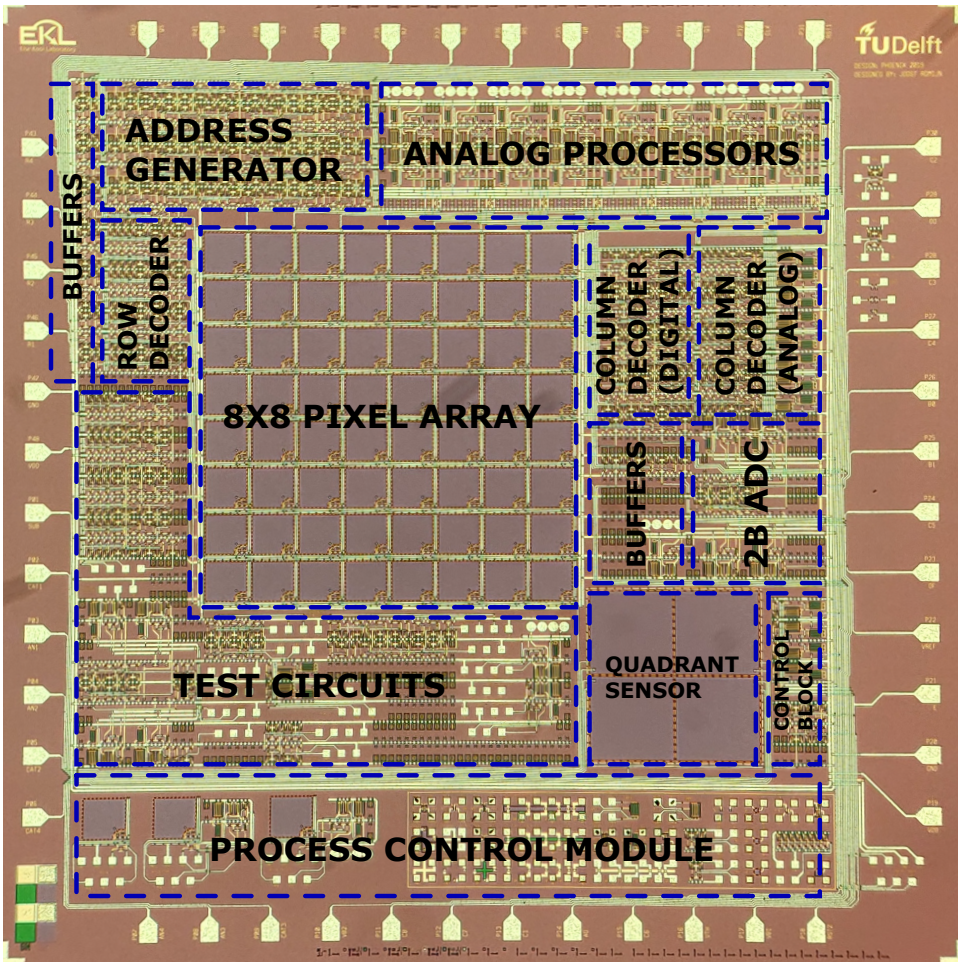


Figure 4.15: Micro photograph of the 64 pixel array sensor with integrated readout electronics in Si on a 10 × 10 mm chip in BICMOS7. The functional blocks are highlighted and the incorporated pixels are the 3T APS design in Figure 4.6a with the NW photodiode architecture. The 7-pin or 10-pin modes are selected by forcing E to LOW or HIGH respectively, with the 7-pin mode site located at the bottom right. Note that the design integrates the pixel array, quadrant sensor and PCM in the same design space. The quadrant sensor is not integrated with CMOS readout and its connections are directly routed to bondpads.

ble C.2 and Figure C.9 and the silicon carbide wire bonding connections are listed and indicated in Tables C.1 and C.3 and Figures C.8 and C.10. Finally, the SICCMOS9 image sensor system is integrated with the on-chip five transistor diode-based CTAT sensor (see Section 3.4.2), enabling the system to monitor temperature in future applications.

In order to efficiently implement manual dense circuit designs for the CMOS blocks, a basic sea-of-gates topology is followed in both the BICMOS7 and SICCMOS9 designs. A fragment of the fabricated CMOS circuitry in SICCMOS9 is depicted in Figure 4.17, following three basic design rules. Firstly, the global power supply lines are routed in ver-

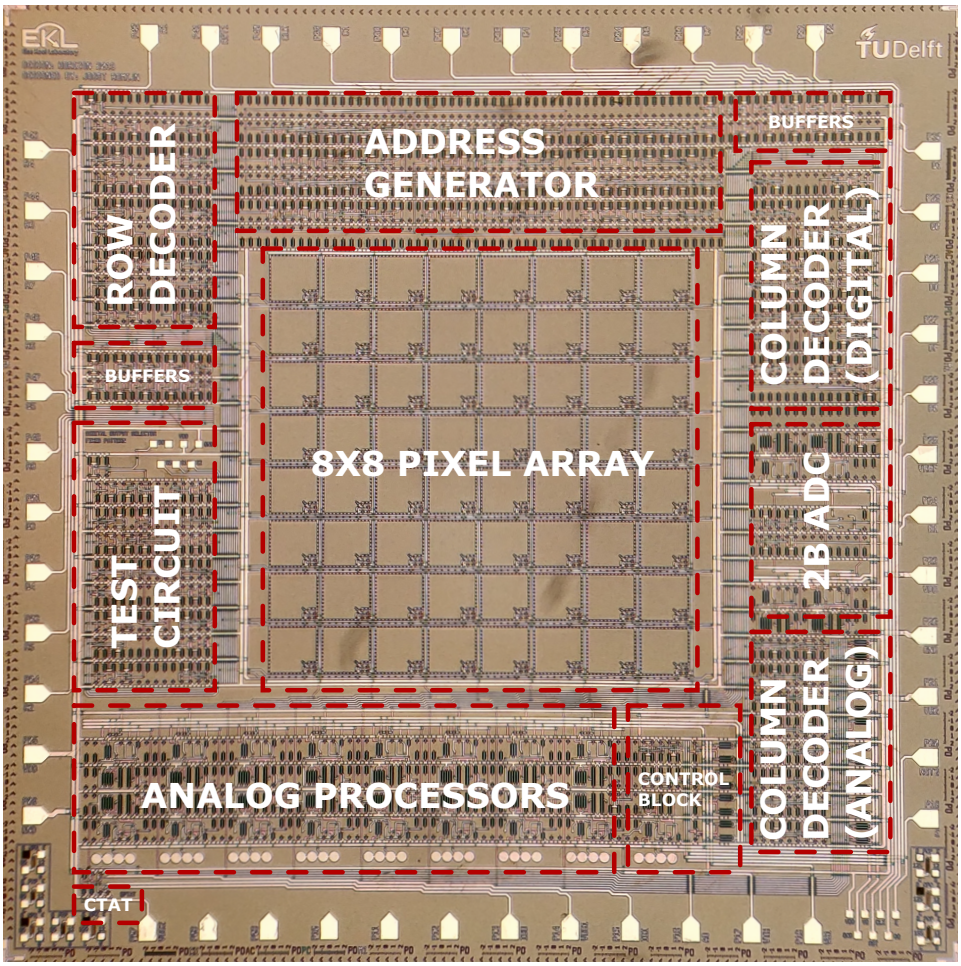


Figure 4.16: Micro photograph of the 64 pixel array sensor with integrated readout electronics in 4H-SiC on a 10 × 10 mm chip in SICCMOS9. The functional blocks are highlighted and the incorporated pixels are the 3T APS design in Figure 4.6a with the PW photodiode architecture. The 7-pin or 10-pin modes are selected by forcing E to LOW or HIGH respectively, with the 7-pin mode site located at the bottom right. Note that some darker spots out of focus can be observed, which are actually some roughened areas on the backside caused by tool handling that are visible through the transparent substrate.

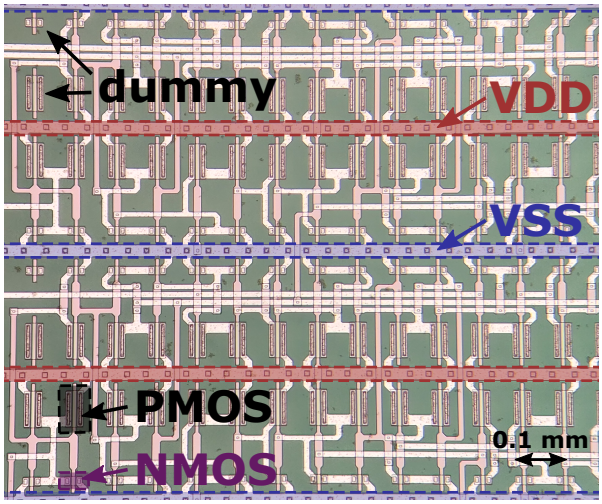


Figure 4.17: Micro photograph of a fragment of the CMOS circuitry in SICCMOS9, following a basic sea-of-gates topology. The power supply lines are transported in horizontal direction, with fixed spacing in vertical direction. The two-level interconnect traces are routed outside of the MOSFET area.

tical direction, with a fixed horizontal spacing. As many parallel power supply lines are incorporated as the design area requires, while always alternating between V_{SS} and V_{DD}. Secondly, the MOSFET devices are placed at fixed locations, considering the distance to the power supply lines and distance between devices. This implies that dummy devices are placed to keep the continuity of the topology, whenever the extra area is needed for routing. Finally, the interconnect traces are routed outside of the MOSFET area, as it is at present not investigated if routing signals over MOSFETs would influence their operation. Note that the second design rule is occasionally broken, as for example in the analog processors the MOSFET sizes are diverse.

4.3.3. SYSTEM VERIFICATION MEASUREMENTS

Before the complete image sensor is measured, some vital functional blocks are verified by measuring intermediate signals. First, the response of the address generator is given in Figure 4.18a, which is implemented by a 6-bit counter, and performs as designed as its LSB flips state for every rising edge of the CLK input. Next, the row decoder response is provided in Figure 4.18b, which takes the three MSB of the address (Q3-5) as its input. The row decoder operates as designed by iterating through all eight rows, while never selecting two rows at the same time. Finally, the digital column decoder is investigated by the implementation of a separate test structure with a fixed output pattern. This fixed pattern is formed by connecting the column inputs to either V_{DD} or ground and is set to '10010110'. The digital column decoder takes the three LSB of the address (Q0-2) as its input, which are here provided from an off-chip source as S0-2.

The measured response is given in Figure 4.18c and shows the correct output. The BICMOS7 address generator and row decoder results are given in Figure C.12, but the digital column decoder is not reported as a hardware layout design error does not allow

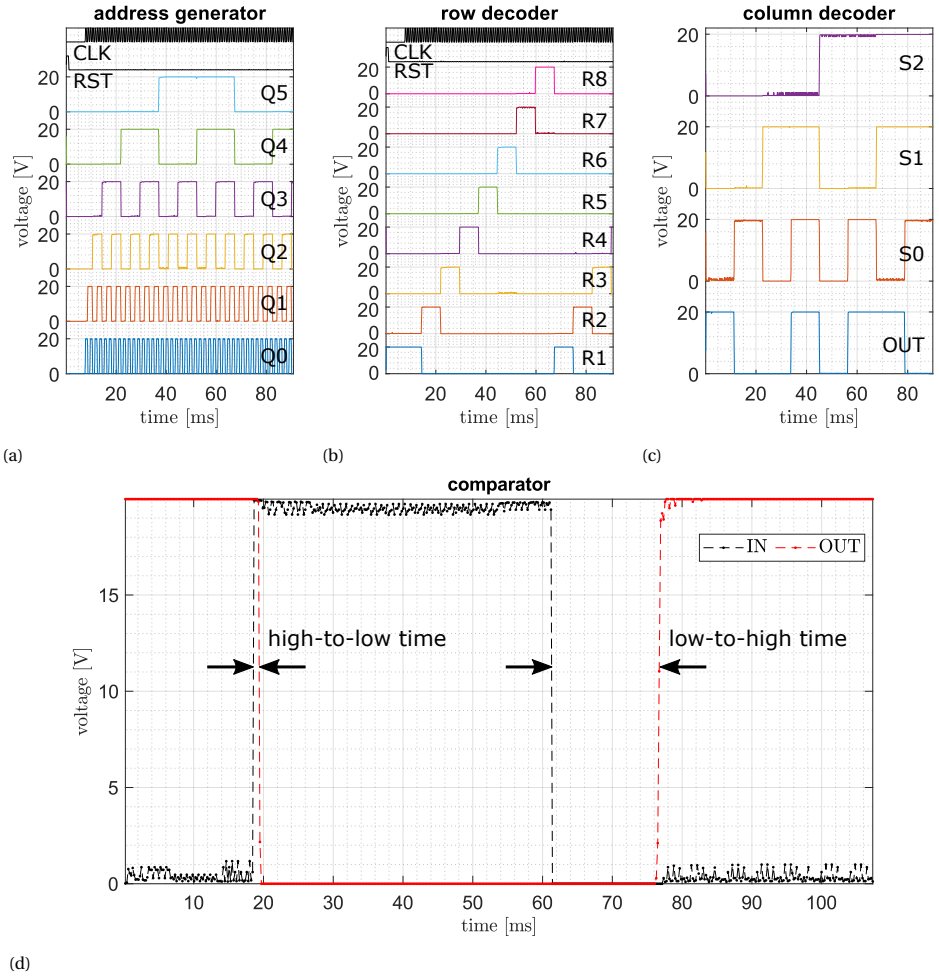


Figure 4.18: The measured response of the a) 6-bit address generator, b) row decoder, c) fixed pattern output selector in SICCMOS9 on die (-2,-1) and d) comparator on die (-1,0). The 6-pin fixed pattern output selector test structure and comparator were measured on wafer-level, while the 10-pin address generator and 12-pin row decoder could only be measured on chip-level after packaging due to the increased amount of pins.

for measuring the output. The used clock frequency in these measurements is 1 kHz for SICCMOS9 with eight data points per clock cycle. The response times for all these SICCMOS9 blocks are below the time step resolution of the measurement, from which it is concluded that the digital control and readout circuits are capable of operation at frequencies above 8 kHz.

In order to determine timing constraints for the complete system in SICCMOS9, information on the response times of the pixels and digital circuits is not enough. Each row transition the analog processors need to update as well, which may take longer than the column selector responses. The comparator response times are characterized and

a typical result is given in Figure 4.18d. It was found that the high-to-low transition time is (1.4 ± 0.4) ms and the low-to-high transition time (24.6 ± 13.1) ms, with outliers of 52 ms. This asymmetry is undesirable and becomes addressable when the available design models are no longer limited to DC analysis only, which is the case presently. If considering 100 ms to ensure all comparator outliers are caught, the analog processor blocks are limited by a maximum operating frequency of 10 Hz.

4.3.4. IMAGE ARRAY SENSOR VERIFICATION

The image array sensor system is first measured on wafer level, using the 7-pin mode (control block E = LOW). This implies that a single pin is used for the system reset and that all bias levels are connected to a single pin. As a first identifier, the wafer is probed under light and dark environments, which should give opposite response from each pixel in the array. The only output mode available in wafer level measurements is the digital output, implying that the measured signal is expected to be either HIGH under dark environment or LOW under light environment.

The BICMOS7 image sensor system operates as intended with yield of 37 % over 52 dies (Figure F.66), though some rejected chips could still operate with reduced performance as they appear to have one or more broken pixels. A noteworthy observation from the wafermap is that the functional chips are in the center of the wafer, while such a yield dependence was not observed for previous circuits. This could be a characteristic of the BICMOS7 technology for higher device count systems, but is not further investi-

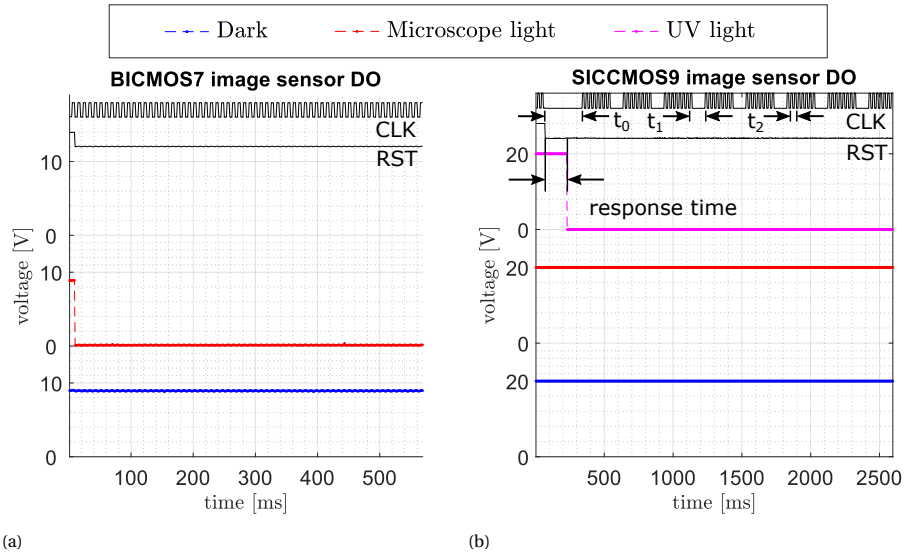


Figure 4.19: The measured response to different illumination cases of the pixel array sensor on wafer level on a) BICMOS7 die (1,0) and b) SICCMOS9 die (-2,-1). Input E of the control block is connected to ground and the bias is set to 1.4 V and 1.5 V for BICMOS7 and SICCMOS9 respectively. The control signals RST and CLK are annotated, as well as the clock timings t_0, t_1 and t_2 of the SICCMOS9 asynchronous clock. Each measurement is a segment of a continuous measurement to avoid start-up discrepancies.

gated in this work. The response of a BICMOS7 chip is given in Figure 4.19a for different illumination conditions. Each cycle starts with a system reset by RST and then counts through all 64 pixels on the rising edge of a synchronous CLK at 0.1 kHz. The digital serial output DO is oversampled and provides 4 measurements per clock pulse, to track the stability of the output. The image sensor output complies with the expected pixel response and no instability in the output signal is observed. Note that for the illuminated case, the first pixel transitions faster than the timestep resolution (<1 ms).

Similarly, the SICCMOS9 image sensor system operates as intended with yield of 78 % over 9 dies (Figure F.67). This yield is much larger then the BICMOS7 counterpart, which is indicating great potential for future implementations in SICCMOS9 with similar or higher device counts. The response of a functional SICCMOS9 chip is given in Figure 4.19b for different illumination conditions. Again, each cycle starts with a system reset by RST and then counts through all 64 pixels on the rising edge of CLK. The digital serial output DO is oversampled and provides 4 measurements per clock pulse, to track the stability of the output. The image sensor output complies with the expected pixel response and no instability in the output signal is observed.

However, an asynchronous CLK signal is employed with three different timings used in the clock signal, which are response times t_0 for the individual pixel, t_1 for the comparator and t_2 for the digital circuitry. When considering a synchronous clock signal, the longest of these response times must be taken as the time of one clock cycle. This is t_0 and is set to 274 ms, which would result in a total time of 35 s, or 29 mHz, for the full array. To improve the sensor refresh rate, the non-synchronous clock signal is applied with tailored timings that match measured response times. Firstly, all pixels need to respond to the illumination and time t_0 is waited before switching from the first to the second pixel. Secondly, each time that the system moves to the next row in the array, all the analog processor channels need to respond. For the digital readout, this concerns the comparator and a t_1 of 108 ms is waited before switching from the first to the second column in the row of pixels. Finally, the digital output selector responds to moving through the columns in the array. For this, a t_2 of 27 ms is waited between pixel switches. The clock timings are conservative considering the reported response times in the previous sections, to ensure that any deviations are covered. This brings the total readout time down to 2.6 s, or 0.39 Hz, which is a 13 times improvement to the synchronous clock.

4.4. IMAGE CAPTURE AND EFFECTS OF TEMPERATURE

With the wafer-level verification measurements of the image sensor through dark or flood light exposure conditions, the system can now be employed to attempt the capturing of an image. Since the application in this work is the sun position sensor, the typical image would be a light spot cast by the light mask. Furthermore, the effects of temperature on the photodetectors is investigated, as first verification of the possibility for extending the temperature range of the device.

4.4.1. PRELIMINARY LIGHT SPOT EMULATION MEASUREMENT

The image sensor is read out on chip-level using the 7-pin mode set by the control block, as this proved adequate for correct operation in both technologies. Furthermore, the

other two image sensor output modes are now also measured, which includes the analog output and 3-pin ADC outputs. As mentioned previously, the ADC in the BICMOS7 design has design errors and is therefore not included in the measurements. The BICMOS7 chip was placed in an optical setup (see Figure 4.20a) with the ability of generating a light spot of several microns using a laser with a wavelength of 633 nm (setup is generally used for Raman spectroscopy). The light spot is aligned to the center of a single pixel in the array and the resulting serial outputs DO and AO are provided in Fig-

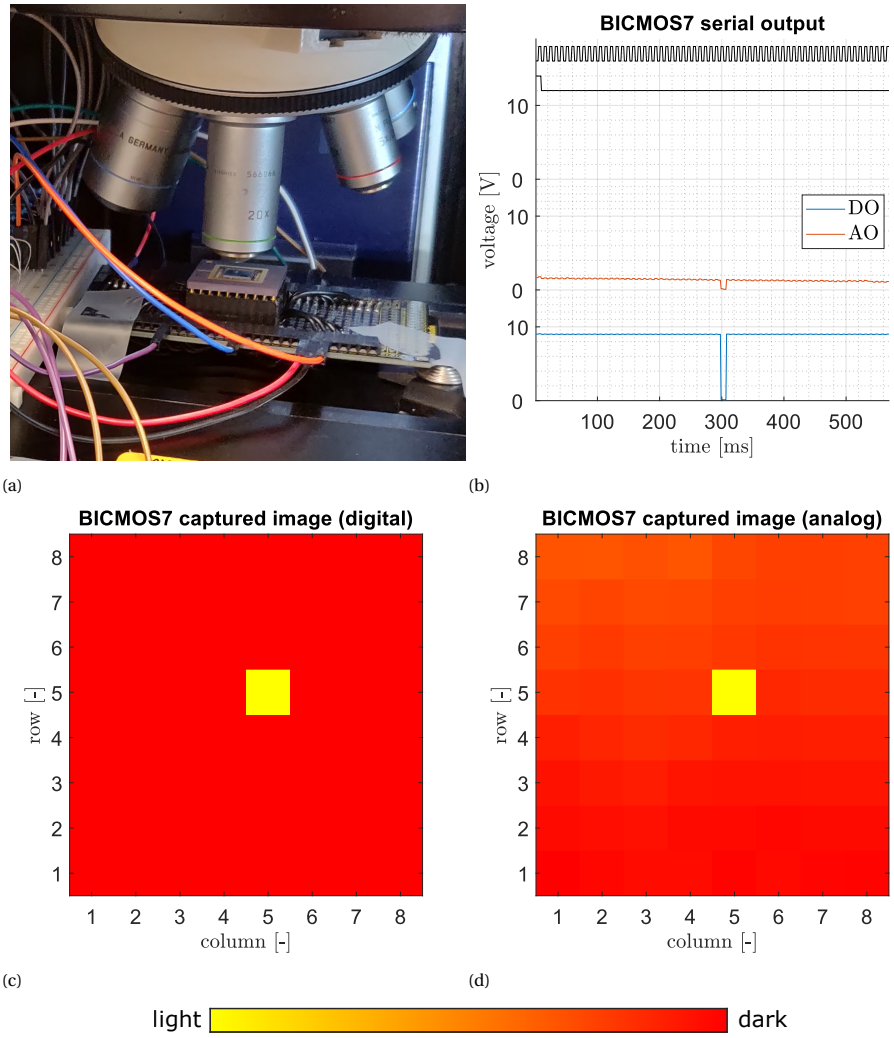
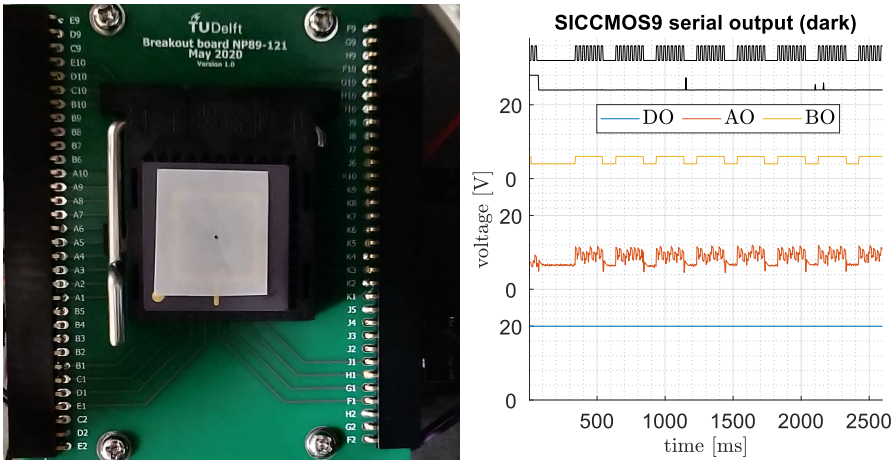


Figure 4.20: Light spot emulation measurement on the BICMOS7 chip in a) an optical setup capable of casting several micron wide light spots with a wavelength of 633 nm. The image sensor b) serial outputs, operated at a CLK frequency of 0.1 kHz and biased at 1.4 V. The serial outputs are transformed to 2D images for the c) digital and d) analog output streams.

ure 4.20b. The serial outputs are transformed to the 2D image, taking into account the address sequence of the rows and columns, resulting in the digital and analog images given in Figures 4.20c and 4.20d. The images provide a crystal clear representation of the light spot that is cast on one of the center pixels. Inspecting the analog image closer, it is concluded that the signal is slowly decaying at the rate at which the sensor is read out, which will result in a minor offset if employed to find angular information. This could be corrected for by performing a reference measurement in a dark environment, but is not further improved in this work. The analog serial output signal shows minor modulation of the CLK, indicating some cross-talk, but this does not have noticable effect on the generated image. It is furthermore concluded that no noticeable fixed pattern noise is present in the image.

Similarly, a light spot is emulated on the SICCMOS9 chip by casting light from the UV light source through a paper light mask. The sensor is covered by the light mask as shown in Figure 4.21a and a first measurement in dark environment is performed, resulting in the serial outputs DO, AO and BO listed in Figure 4.21b. It is observed that during timing t_1 the AO and BO outputs dip to lower levels, which would falsely ascribe a lower value to the first column of each row. This could be due to a faulty first channel in the analog processor on this chip, or the layout design has an asymmetry for the first column and/or first channel of the analog processor. To combat this undesired effect, each pixel is read out using only the first eight sampled data points in the CLK cycle.

Switching on the UV light source, the resulting sensor serial outputs DO, AO and BO are given in Figure 4.22a. Note that BO is represented by transforming the 2-bit digital output to an analog representation. The transformed 2D images of the three outputs modes are given in Figures 4.22b to 4.22d. The cast light spot spans over two pixels, as



(a) (b)

Figure 4.21: Light spot emulation setup on the SICCMOS9 chip by means of a) a paper light mask aligned on the sensor. The light source is a single discrete single 5 mW SMD3535 265 nm UV-C LED placed at 6 cm distance. The image sensor is readout in dark environment, resulting in b) serial outputs, operated by an asynchronous CLK and biased at 1.5 V.

the digital image representation clearly shows. The analog representation shows this less clearly, which is ascribed to several potential sources. Firstly, the serial AO output signal shows stronger modulation by the CLK signal with respect to the BICMOS7 results. Secondly, the basic pinhole configuration would allow for more stray light to hit surrounding pixels, which is indeed observed in the image. Lastly, the sensor could suffer more from fixed pattern noise than the BICMOS7 implementation. Two more configurations are measured, containing two pinholes, and the results are listed in Figures C.13 and C.14.

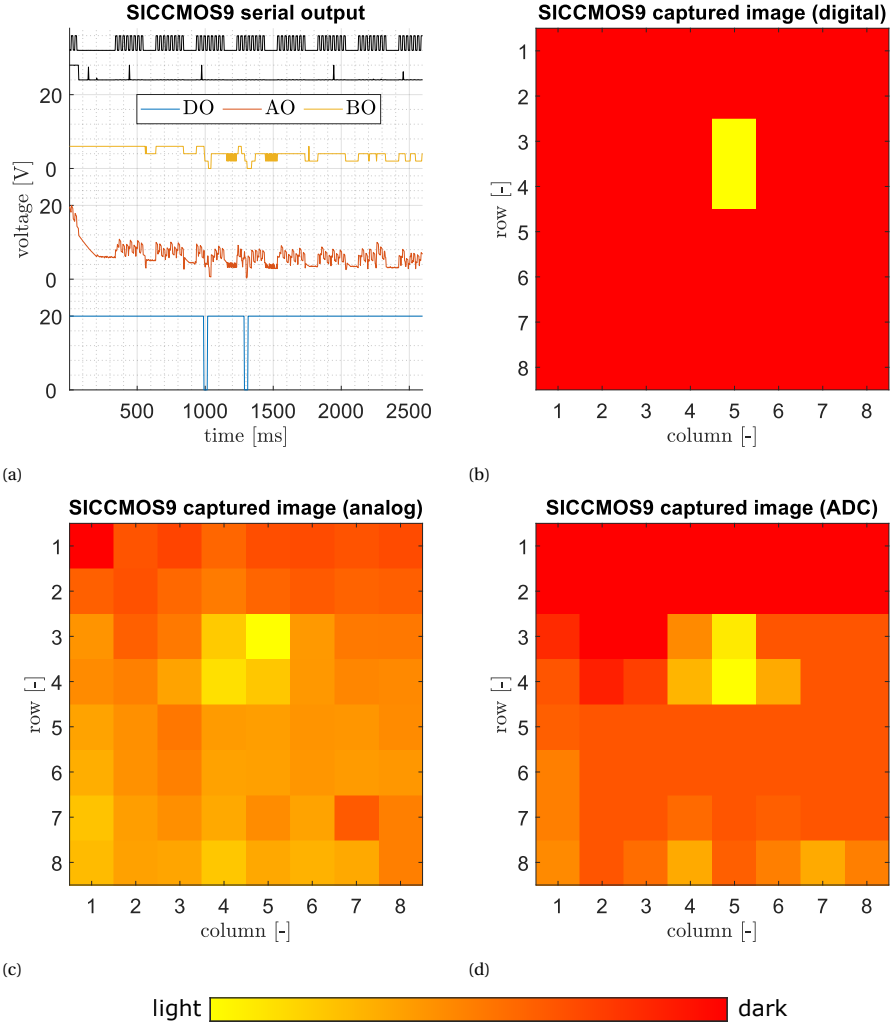


Figure 4.22: Light spot emulation measurement on the SICCMOS9 chip. The image sensor a) serial outputs, operated by an asynchronous CLK and biased at 1.5 V. The serial outputs are transformed to 2D images for the b) digital, c) analog and d) 2-bit ADC output streams.

Finally, the power consumption of the image sensor is determined by measurement of the DC input current at the positive power supply terminal using an HP 34401A multimeter. Without UV illumination, the power consumption is 8 µW and 30 µW when idle and during readout, respectively. This is increased for UV illumination to a power consumption of 30 µW and 60 µW when idle and during readout. It should be noted that in the case of no UV illumination, after switching on the power supply and before a

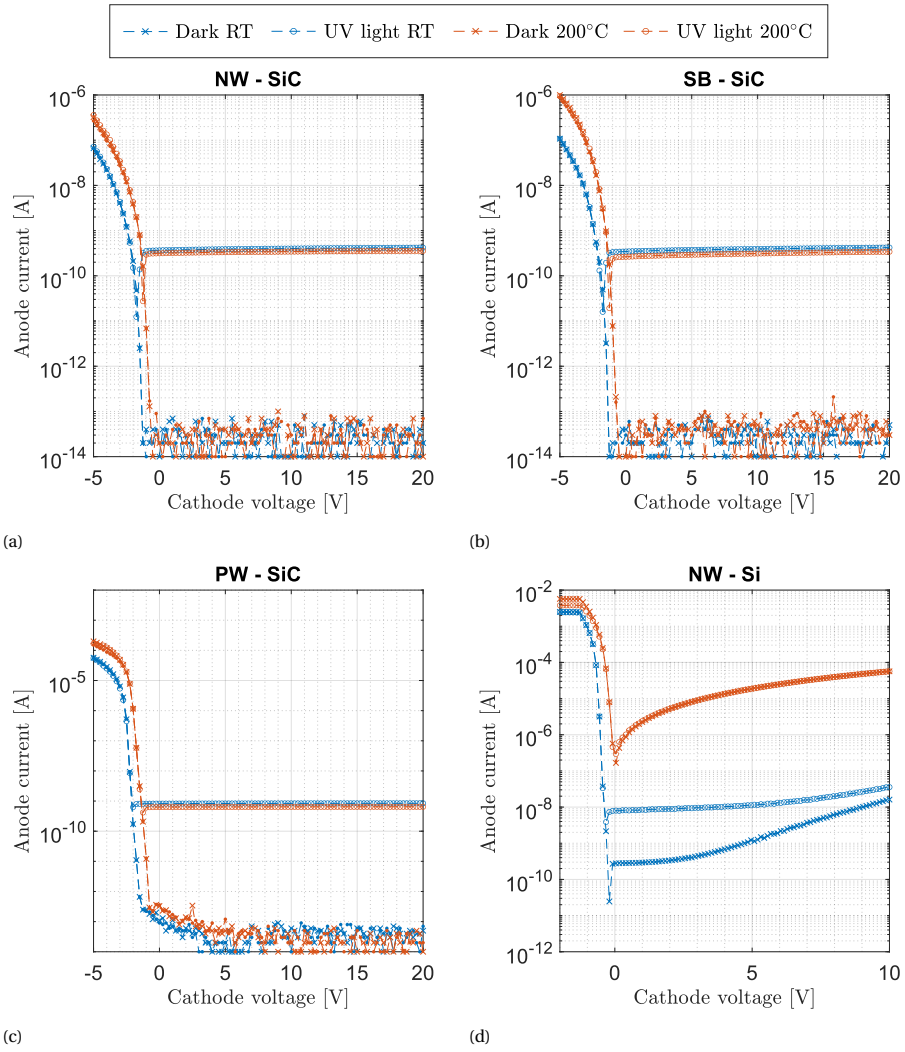


Figure 4.23: The measured anode current for different cathode biasing and temperature levels on die (1,0) of the different vertical SiC photodiode 80 × 80 µm implementations in the a) n-well (NW), b) substrate (SB) and c) p-well (PW). Similarly, the measured anode current on die (1,1) of d) the Si reference implementation. The anode is biased at 0 V and the PW substrate connection at 20 V. Different illumination conditions are used to extract PDCR indications.

first readout is started, the input current is large (0.13 mA) and decreases in minutes to the corresponding idle value. Starting a sensor readout immediately brings the power consumption down to the reported value. As such, it is recommended to perform a power-on reset for the system.

4.4.2. EXTENDING THE TEMPERATURE RANGE

The target operating temperature of the sun position sensor is not the reason for switching to silicon carbide. However, it is derived from the dependency of the state-the-art on silicon implementations and extending the range towards higher temperature would open up new possibilities for space missions. Therefore, the individual photodetectors are again investigated on chip level for higher temperature at 200 °C with the IV results displayed in Figure 4.23. The most prominent observation for the SiC photodetector results is the unchanged dark current. As mentioned previously, the dark current contributions are dominated by sources like the ohmic contacts or substrate. The junction dark current will increase, but this increase is so low at this temperature that it is still not dominating.

Three further observations for the photodetector operation can be made from the plots. Firstly, the dark current and photo current for microscope light are indistinguishable, in contrast to the results reported in Figure 4.3. The insensitivity towards visible light is thus improved after the dicing of the chips. This is possibly due to reduced contribution from the substrate or changes in the microscope light intensity. Secondly, the generated photo current at high temperature during UV exposure is noticeably lower. This will however have a negligible effect on the PDCR and thus not influence the pixel operation or timings. A possible explanation for this is increased charge recombination in the depletion layer with higher temperature. Lastly, the photodiode forward voltage[4] is shifted in the plot towards the right. Though the forward voltage is still below a bias of 0 V, which cannot occur in the 3T APS circuit, it should be considered when moving to even higher temperature levels to ensure the cathode bias does not overlap with the forward voltage.

In stark contrast, the anode current of the Si photodetector increases several orders of magnitude at 200 °C, and loses any distinction between dark an UV illumination modes. This will result in unresponsive 3T APS circuit in Si at this temperature, with no outlook on a working pixel array sensor. This illustrates the large improvement of SiC implementations and opens the door to new space missions with higher temperature exposure.

4.5. CONCLUSIONS AND RECOMMENDATIONS

The reported silicon carbide opto-electronic system is one of the largest device count implementations in silicon carbide to date, with 64 photodetectors and 1263 transistors, and offers serial digital, analog or 2-bit ADC output options. The system operates at 0.39 Hz using an asynchronous clock and has a maximum power consumption of 60 µW. These specifications are a leap forward in comparison to the only previous report on a

[4] The diode forward voltage is defined as $V_F = V_{anode} - V_{cathode}$ and is the point at which the diode becomes a conductor.

UV SiC imaging sensor, implemented in a BJT technology by the group of Zetterling *et al.* of the KTH in Sweden [5]. As a fair comparison to the previously reported SiC BJT 256 pixel array, the timing scheme of the pixel array in this work is extrapolated. This results in a total readout time for 256 pixels of 8.4 s, which is an improvement of 15 times. The reported power consumption of the pixel array in BJT technology [5] is 8.25 W, which implies that the sensor reported in this work has a reduced power consumption by a factor of 137 500, considering its maximum measured power consumption. The complexity of this opto-electronic SiC CMOS system paves the way for new applications such harsh environment microcontrollers.

For the photodetector building block, three vertical types are implemented in the SICCMOS9 design layers, which implies the use of doped regions formed by ion implantation. All three photodetector types are functional and are characterized for different illumination conditions. The highest PDCR towards UV was reported for the PW photodetector type (inside a p-well), ranging up to $(32.8 \pm 8.3) \times 10^4$, though its design suffers from leakage current. The extracted dark current is 0.3 nA cm^{-2}, which is dominated by technology effect like the contacts and substrate and therefore leaves room for future improvements. The spectral response of the three photodetector types is concluded to be identical, with peak responsivity at 290 nm. From the spectral response curves, the albedo rejection ratio equals 1.56 and 3.84 for silicon and silicon carbide respectively. The derived information is used in the hardware layout design of the photodetectors in the quadrant sun position sensor.

The reported photodetectors are integrated in active pixels, following the 3T APS circuit design. As the technology constraints the cathode connection of the photodiode, an alternative variant of the text book circuit is proposed with complementary operation. The pixel fill factors are 73 % and 77 % for the BICMOS7 and SICCMOS9 implementations respectively, with similar area consumption. The raw pixel outputs perform as expected, with no response in dark or microscope light conditions and signal transition under UV condition. A slower response from the PW type is reported, which is due to the leakage current in its implemented hardware design. The pixels are integrated with a comparator or unity-gain buffer from the previous chapter, to digitize or buffer the analog output signal. The comparator integration adds delay for the SiC PW implementation and the unity-gain buffer add delay for all types. Even though the SiC PW has its nonidealities, it is favored over the other types as the text book 3T APS circuit is used. The SiC PW is therefore the selected type for integration in the 8×8 pixel array.

The opto-electronic system design contains the 8×8 pixel array, address generator, analog processors, row decoder, column decoders and control block. The hardware layout design follows a basic sea-of-gates topology to ease the manual placement and routing process. The system is verified by measurement of intermediate signals that indicate the function of separate blocks. Moreover, information on response times is gathered to design a suitable readout scheme on an asynchronous clock signal, as a synchronous clock would extend the readout time to over half a minute. The full system is then tested on wafer level in dark and light conditions to identify functional chips for packaging.

Preliminary light spot emulation measurements reveal the capability of capturing an representative image in both technologies. The digital and analog modes are operational in the BICMOS7 implementation, and all three modes are functional in the SIC-

CMOS9 implementation. This validation provides freedom in the approach towards the final application. The power consumption of the SICCMOS9 chip is low at only 60 µW, which is a good match for space application. Furthermore, extending the operation temperature is investigated by measurement of the single photodetectors, which reveals negligible change in SICCMOS9 while it renders the BICMOS7 devices unusable.

The opto-electronic system can be improved in future work by improving the layout design of the SICCMOS9 PW type, to omit its leakage and optimize its response. In order to increase the imager system refresh rate, the analog processor channels require optimization of the comparator transition time. This may allow implementations that exceed 10 Hz refresh rates, which is highly desirable for application on spacecraft as it increases the ability of detecting rotation of the spacecraft. Finally, future work may investigate temperature above the reported 200 °C.

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5

Optics Integration and Sun Sensor Characterization

Sometimes, science is more art than science.
A lot of people don't get that.

Rick Sanchez (fictional character)

All the previous chapters set the stage for the final integration steps and characterization of the full device. This chapter therefore relies on the implementation choices made, and ties the final demonstrator together in order to achieve the research goals. The quote above captures this concept in an elegant way, and should be read as the challenge of integrating the complete design and fabrication of all system blocks of a complex device. With this in mind, this chapter focuses on the wafer-level integration of the sensor optics and concurrently the characterization of the devices. Some aspects are left open for future research, such as reliability investigation and effects of high temperature on the integrated system.

Parts of this chapter have been published in 2021 IEEE 34th International Conference on Micro Electro Mechanical Systems (MEMS) (2021) [1], 2022 IEEE 35th International Conference on Micro Electro Mechanical Systems (MEMS) (2022) [2], IEEE Sensors Letters (2022) [3] and Sensors and Actuators A: Physical (2022) [4].

ADVANCED wafer-level packaging is an enabling technology for integration of complex microsystems and MEMS. It allows for integration of different technologies in the same package in a highly miniaturized approach, used today for example in smartphones. The introduction chapter in this dissertation outlined different approaches and considerations for wafer-level packaging. The starting point for this chapter builds on this, by considering the preparation of a patterned wafer for wafer-to-wafer bonding, an additive printing approach and a chip-to-wafer bonding technology. One of these is selected to fully integrate the 3D optics of the sun position sensor. Two of these routes rely on the joining of two substrates, which is done in a variety of ways in industry.

Commonly used technologies for bonding substrates are direct, anodic, thermocompressive or glass frit bonding. Direct bonding or anodic bonding are considered not compatible with CMOS device wafers [5], and are therefore not compatible with the sun position sensor platforms in BICMOS7 and SICCMOS9. Glas frit bonding is performed by means of screen printing to obtain selective deposition, and requires temperature steps upto 450 °C to form a bond. Disadvantages of glas frit bonding are the general need for lead-containing glass and the cumbersome screen printing process, which makes rough mechanical contact to the substrate, has low throughput, and demands application specific setups [6–10]. Finally, thermocompressive bonding is divided in two classes, which are adhesive and metallic thermocompressive bonding. Metalic thermocompressive bonding, or eutectic bonding, forms a bond by diffusion of metal into a semiconductor interface layer at elevated temperature and controlled joining force [11]. The other class of adhesive thermocompressive bonding joins the two interfaces by activation of a polymer adhesive at elevated temperature and controlled joining force.

To complete the sun position sensor device, the attached optical window needs to be coated with an opaque light mask to obtain the angular sensitivity. One approach is to pre-coat and pattern the optical windows with an opaque layer, and rely on the pick-and-place alignment accuracy to ensure the aperture is aligned well to the photodetectors. However, this defeats the purpose of the die-to-wafer stacking approach over the dies stacking approach, as it still has a limited throughput and larger device-to-device variation. It is furthermore necessary to use lithography tools to completely implement the device by microfabrication, allowing future miniaturization.

In this chapter, three different approaches are investigated to implement the milimeter scale thick transparent optics. The wafer-level packaging technology for the 3D optics integration is first developed on the silicon platform, before application on the silicon carbide counterpart. The quadrant and pixel array sun position sensor devices are then characterized. Furthermore, the diffraction grating sensor architecture (see Section 2.3) is implemented as alternative to the bulky 3D optics, using conventional microfabrication technology. Lastly, the silicon carbide system with 3D optics is verified for higher temperature operation, before concluding the chapter.

5.1. TOWARDS INTEGRATION OF THE OPTICAL WINDOW

The processed device wafers with the integrated opto-electronic systems from the previous chapter are taken as starting material for the wafer-level integration of the optics. It should be noted that the top interconnect layer is exposed on these wafers for probing and wire bonding. The process therefore starts by deposition of a 0.8 µm silicon oxide

passivation layer by TEOS PECVD, followed by patterning using a mask aligner to expose the bond and probe pad openings. This effectively upgrades the two considered technologies by one design layer, resulting in BICMOS8 and SICCMOS10 (see Appendices E.2 and E.3). No polishing is performed to planarize the wafer front side, leaving step heights of ~1 µm as a result of the CMOS layers. This section considers different routes to integrate the transparent milimeter scale optics on wafer-level.

5.1.1. LASER CUTTING TRANSPARENT SUBSTRATES

The first approach that is considered, is based on the idea of performing aligned wafer-to-wafer bonding. In this concept, one would need one wafer with the integrated CMOS

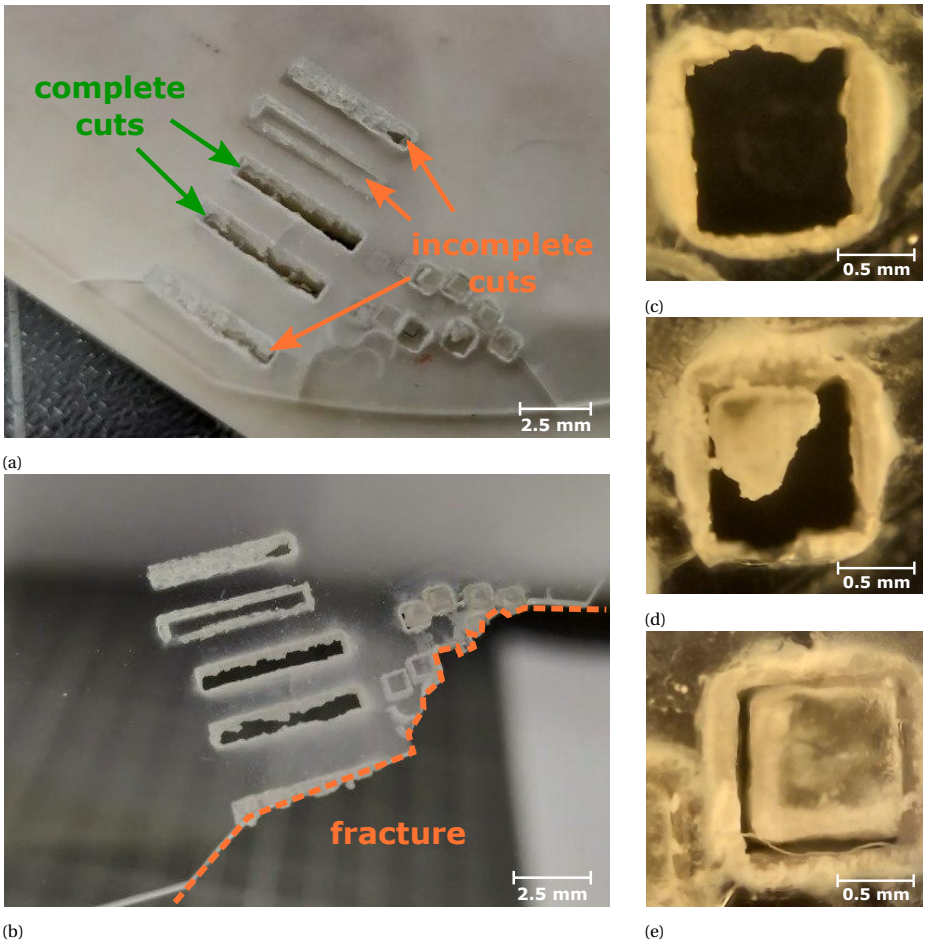


Figure 5.1: Images of the cuts made by laser ablation, including a) the substrate overview on the carrier and b) after removal from the carrier that resulted in a fracture. For closer inspection smaller structure images of c) complete cut, d) cut with residue and e) incomplete cut, are included. The used system is an Optec WS Starter based on the SpectraPhysics Talon nanosecond pulsed laser at a power of 15 W and wavelength of 355 nm.

system and another wafer that implements the transparent optical windows. To allow front side electrical contacting on the CMOS wafer, the transparent wafer must be patterned with holes with large enough clearance. Conventional wet or dry etching technologies are not feasible here, due to very long etch times and low selectivity. As preliminary investigation, a laser ablation system is used in effort to pattern a 700 µm thick standard 100 mm glass substrate [12]. This cutting procedure is time consuming to the point of several hours to complete the patterns on wafer level.

The test results are depicted in Figure 5.1 and reveal that it is challenging to achieve proper cuts, as within the range of five tested setup parameters only two resulted in successful cuts. The challenge is best described by balancing the setup parameters between too aggressive and too relaxed. As a result, the test batch either has cuts that in addition also severely damaged the carrier or did not cut through, as highlighted in Figure 5.1a. Moreover, the agressive process locally heats up the substrate, which causes discolorment and fracture formation in the substrate that can lead to actual cracking of the substrate upon release from the carrier, as shown in Figure 5.1b. Arguably, the test cuts are located too close to the substrate edge and the smaller test cuts too close to each other, causing the cracking. However, to clear the front side connections of the CMOS chip the cuts must still be spaced relatively close too each other.

The smaller test cuts are investigated, with an example of a complete cut in Figure 5.1c. An incomplete cut is given in Figure 5.1d, which actually shows that the pattern is opened, but some residue remains in the top left corner. From the incomplete cut in Figure 5.1e a possible explanation can be given, as it indicates that the residue is cut on two sides and appears to have sintered to the other two sides. This sintering process is induced by the local heating of the substrate and residue. Though migrating to a setup with a picosecond pulsed laser would already improve the results[1], to overcome the challenges of long etching time, substrate discoloring and substrate local heating, different approaches are required.

5.1.2. 3D PRINTED TRANSPARENT POLYMER

Over the past decade, manufacturing through 3D printing technology underwent rapid developments that improved the quality and accuracy while reducing the setup costs, with smaller printer systems now even finding their way into consumer homes. Some integration of 3D printing in the semiconductor industry is adopted, which is ground for the preliminary attempts in this work to assess the compatibility with the optical window fabrication. In this approach, the optical windows can be selectively build on top of the CMOS device wafer as an additive process. The technology of choice is stereolithography apparatus (SLA) printing, which operates by selective illumination (typically using a laser) to solidify a photo-polymerizing resin. As a starting point, the work on acrylate networks by Anastasio [13] at the Eindhoven University of Technology is simplified[2] to use of commercially available NanoClear resin from FTD in a conventional SLA printer for rapid prototyping. Unfortunately, the optical transmission of this resin

[1] Picosecond pulsed lasers decrease substrate heating and minimize the volume of damaged material during ablation with respect to nanosecond pulsed lasers.

[2] In the original work, the author prepared the resin to optimize material parameters and solidified the polymer in a custom UV exposure tool.

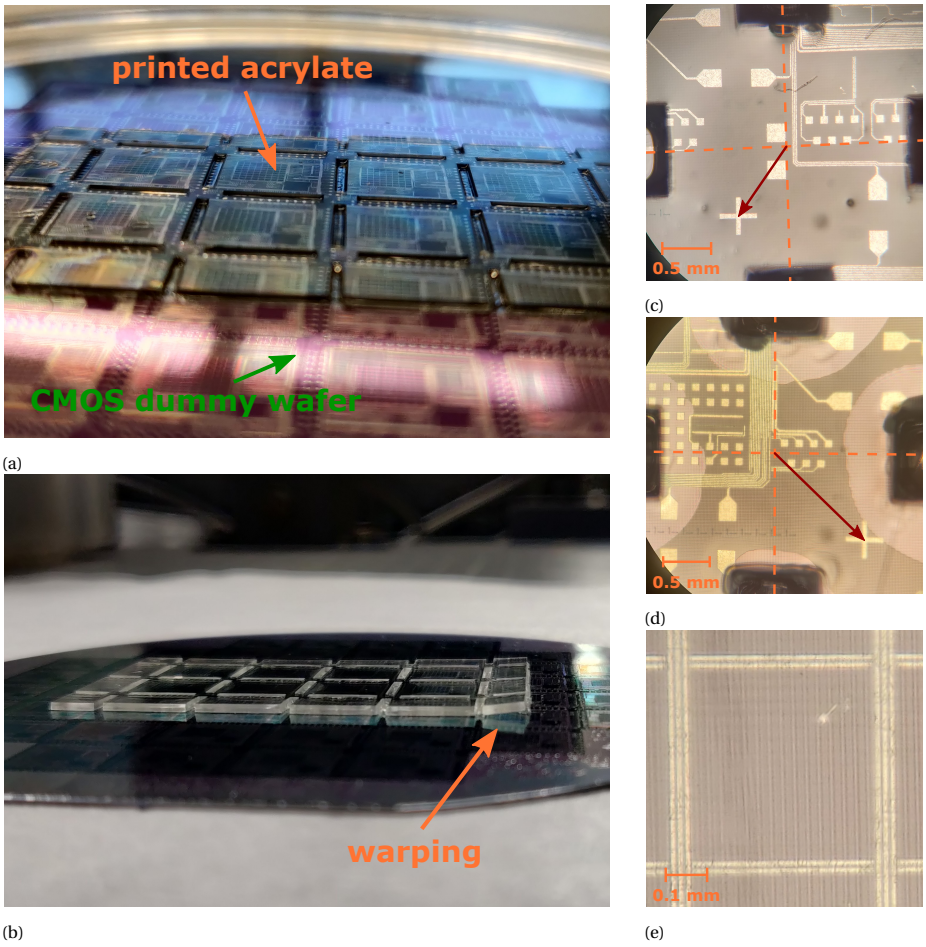


Figure 5.2: Images of the 3D printed acrylate layer, including a) the substrate overview of the structure on the wafer and b) the problem of layer warping upwards. For closer inspection smaller structure images c)-d) show the large shift in overlay with respect to the device wafer and e) the overview of single pixel that visualizes the discrete blocks that are printed.

is not reported by the manufacturer, but given the transparency in the visible range it is expected to at least work on the silicon based design for optical wavelengths.

Test wafers are prepared by formation of a 100 nm thermal oxide layer, on which the top metal layer (M2) of the BICMOS7 design is deposited and patterned. The batch is split in passivation layer material, including either 600 nm TEOS PECVD oxide or 800 nm silicon nitride. The bond and probe pads are exposed by dry etching vias in the passivation layer. These test wafers are considered fitting as they have similar interface layers and step heights to the device wafers. To perform the 3D printing, the substrate is manually aligned to the laser origin and secured on a chuck that is completely submerged in the resin. Upon completion of the printing process, the substrate is cleaned with ace-

tone to remove resin residue.

The printing setup is generally constrained by the trade-off between range and accuracy, which in this tool resulted in a range smaller than the wafer (see Figure 5.2a). The rudimentary cleaning was inadequate for removing residues in the rectangular openings to the front side electrical contacts, while submersion in acetone also degraded the printed area. An inherent challenge for SLA printing of transparent layers is warping (see Figure 5.2b), which is caused by stress in the layer due to re-exposing the bottom layers during the printing process. No difference of adhesion quality was observed for the two passivation interface layers in the test batch, by optical inspection directly after deposition and after a few weeks. The manual alignment is not sufficient yet, with the bondpads not in the opened area (see Figures 5.2c and 5.2d), and would benefit from implementation of alignment strategies. The printed layer is highly uniform and visually transparent, though the discrete printed blocks can be visually distinguished (see Figure 5.2e). Future work may also explore the hot embossing technique, which requires a transparent mold to be attached to the target wafer. The resin is then pumped into the mold and completely exposed equally, avoiding warping issues.

5.1.3. THERMOCOMPRESSIVE BONDING

A diced 8 × 8 mm optical window is manually pick-and-placed on a silicon device chip for chip-level thermocompressive bonding with a polymer adhesive. Polymers that are typically used are benzocyclobutene (BCB) [14] or epoxy-based SU-8 photoresist [15], where the latter is chosen as a result of prior art in EKL facilities. A droplet of SU-8 3000 series [16] is dispensed on the center of the device chip, followed by the manual placement of a glass optical window. The optical window is smaller than the device chip to allow for front side electrical connections. The stack is then bonded at 120 °C under controlled compressive force for a few hours in an AML wafer bonder.

The final result of the packaged test chip is depicted in Figure 5.3 and the silicon

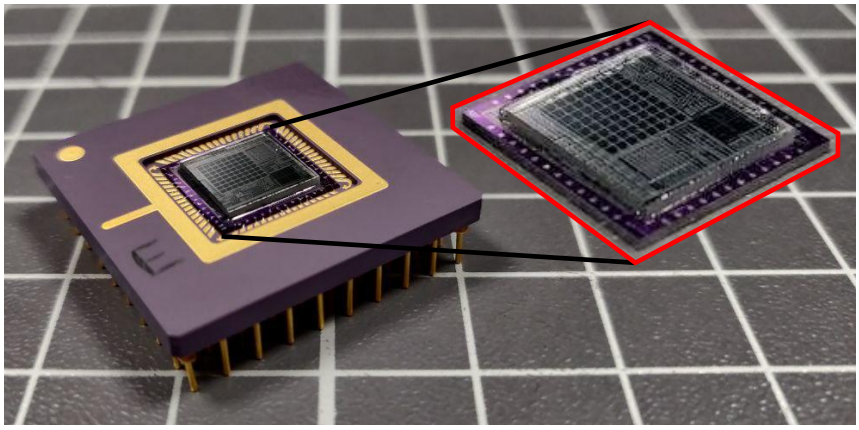


Figure 5.3: Packaged silicon device after adhesive thermocompressive bonding of the glass optical window. The inset shows the bare chip after adhesive bonding and before packaging. The SU-8 interface layer extends the complete interface of the optical window, including therefore the active area of the opto-electronic chip.

opto-electronic system operates as intended, with no performance difference observed before and after the adhesive bonding of the optical window on top of the sensor (see Section 4.4.1). This straightforward approach for attaching the optical window stands out as it does not require special care for the preparation of the optical window other than conventional dicing, nor the challenges of adhesion and strict alignment of direct printing the optical window. The following section focuses on scaling this to a chip-to-wafer bonding approach, implementing the selective deposition of SU-8 patterns to avoid interference in the active area and adds the light masking layer.

5.2. SUCCESSFUL INTEGRATION OF THE 3D OPTICS

This section dives deeper in the adhesive thermocompressive bonding on wafer-level, by design of appropriate SU-8 outlines and the implementation of the light mask on top of the optics. This is accompanied by layer thickness characterization, yield reports of the optical window attachment and die shear tests, for the selection of the pattern. The complete final flowchart is listed in Appendix E.4.

5.2.1. DESIGN OF THE ADHESIVE OUTLINE

The adhesive outline bond strength is designed by considering the three failure modes described by the SU-8 datasheet [16], which are; 1) detachment from the CMOS device chip (69 MPa), 2) detachment from the optical window (35 MPa) and 3) rupture of the SU-8 layer (73 MPa). As the bond strength between the SU-8 layer and the optical win-

Table 5.1: Listing of the 16 adhesive patterns in the design, of which site 0 is a fabrication reference. The total interface area, trace width, clearance and predicted bond strength are listed. The trace with and clearance are marked in Figure 5.5 and the bond strength is predicted through Equation 5.1.

Site	Area	Trace width	Clearance	Predicted bond strength
0	51.8 mm^2	N/A	0.4 mm	907 N
1	2.84 mm^2	0.1 mm	0.4 mm	50 N
2	5.60 mm^2	0.2 mm	0.4 mm	98 N
3	8.28 mm^2	0.3 mm	0.4 mm	145 N
4	2.92 mm^2	0.1 mm	0.3 mm	51 N
5	5.76 mm^2	0.2 mm	0.3 mm	101 N
6	8.52 mm^2	0.3 mm	0.3 mm	149 N
7	11.2 mm^2	0.4 mm	0.3 mm	196 N
8	5.92 mm^2	0.2 mm	0.2 mm	104 N
9	8.76 mm^2	0.3 mm	0.2 mm	153 N
10	11.5 mm^2	0.4 mm	0.2 mm	201 N
11	14.2 mm^2	0.5 mm	0.2 mm	249 N
12	9.00 mm^2	0.3 mm	0.1 mm	158 N
13	11.8 mm^2	0.4 mm	0.1 mm	207 N
14	14.6 mm^2	0.5 mm	0.1 mm	256 N
15	17.3 mm^2	0.6 mm	0.1 mm	303 N

dow is lowest, this is the most likely failure mode to consider. Literature reports on the bond strength are much lower than those reported in the datasheet and are in the order of 1–20 MPa, with varying fabrication parameters such as SU-8 layer thickness, bonding temperature and bonding time [15, 17–20]. The bond interface area is related to a target bond force by

$$A = f \frac{F_{\text{crit}}}{\sigma_{\text{adh}}}, \tag{5.1}$$

where A is the contact area, f the safety factor, F_{crit} the force criterion, and σ_{adh} the adhesion strength. For this adhesive pattern design, f is fixed at 2, σ_{adh} at 35 MPa and F_{crit} is set to 100 N, which results in a required minimum SU-8 contact area of >5.7 mm^2. The chosen F_{crit} is considered adequate for the first demonstrator, but should be reconsidered when aiming to match industry specific standards.

Suitable SU-8 outline patterns are investigated for integration in the bonding process, by variation of design parameters of the mask set in Figure D.1. This mask set contains 16 variants, varying in SU-8 trace width and clearance to the optical window edge, of which more details are highlighted in the final patterns in Figure 5.5, and the complete list of details for each pattern is given in Table 5.1. The SU-8 layer thickness is (9.27 ± 0.23) µm and was measured on five locations on 11 wafers (55 data points). The measured sample set is listed in Table 5.2, including Si and SiC test and device substrates that have varying interface layers.

The test mask set in Figure D.1 is applied on 10 silicon wafers for investigation of the best pattern. To select the pattern, a figure-of-merit (FoM) is defined by using predicted bond strength and fabrication yield through

$$\text{FoM} = \frac{\text{total samples} - \text{failed samples}}{\text{total samples}} \times \text{bond strength}. \tag{5.2}$$

Table 5.2: Listing of the SU-8 thickness measurement results. Each wafer is measured on five locations, and the data set consists of test and device wafers with different interface layers and substrate material. The measurements are performed using a Dektak 8 profilometer.

Wafer	Bottom right	Bottom left	Center	Top right	Top left
SI_W2	9.24 µm	9.36 µm	9.31 µm	9.13 µm	9.22 µm
SI_W3	9.36 µm	9.34 µm	9.31 µm	9.25 µm	9.37 µm
SI_KTH	9.05 µm	9.03 µm	9.06 µm	9.03 µm	9.06 µm
SI_T7	9.91 µm	9.27 µm	9.25 µm	9.43 µm	9.49 µm
SIC_W1	9.38 µm	9.34 µm	9.48 µm	9.36 µm	9.39 µm
SIC_W4	9.32 µm	9.39 µm	9.34 µm	9.29 µm	9.34 µm
SIC_W5	9.64 µm	9.70 µm	9.67 µm	9.80 µm	9.68 µm
SIC_W7	9.20 µm	9.42 µm	9.50 µm	9.45 µm	9.44 µm
SIC_T1	8.93 µm	8.96 µm	8.82 µm	8.97 µm	8.96 µm
SIC_T2	8.93 µm	8.92 µm	9.00 µm	9.01 µm	8.96 µm
SIC_P1	9.32 µm	9.59 µm	9.30 µm	9.28 µm	9.33 µm

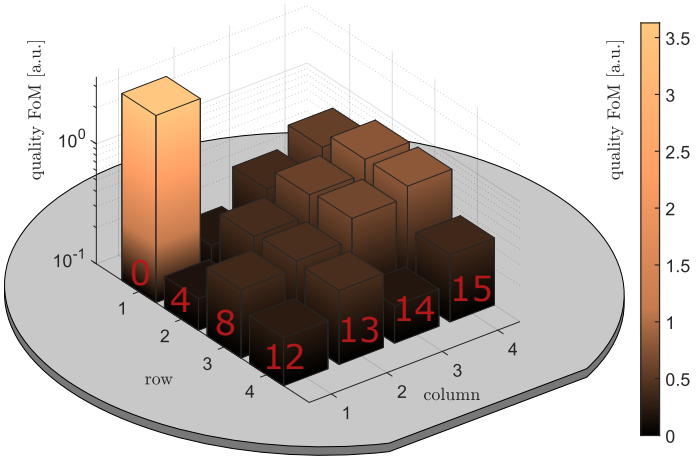


Figure 5.4: Representation of the FoM calculated by Equation 5.2 on a logarithmic scale, that considers calculated bond force and fabrication yield, of each adhesive pattern on 10 wafers. The sites are indicated in red and the full list is given in the 2D image in Figure D.1.

The calculated FoM of each pattern is plotted in Figure 5.4, clearly identifying the reference as the best performing pattern. This is expected as it has a much larger contact area and the optical windows never detached during experiments. As the reference would place the SU-8 directly on top of the sensor active area, it is not selected for fur-

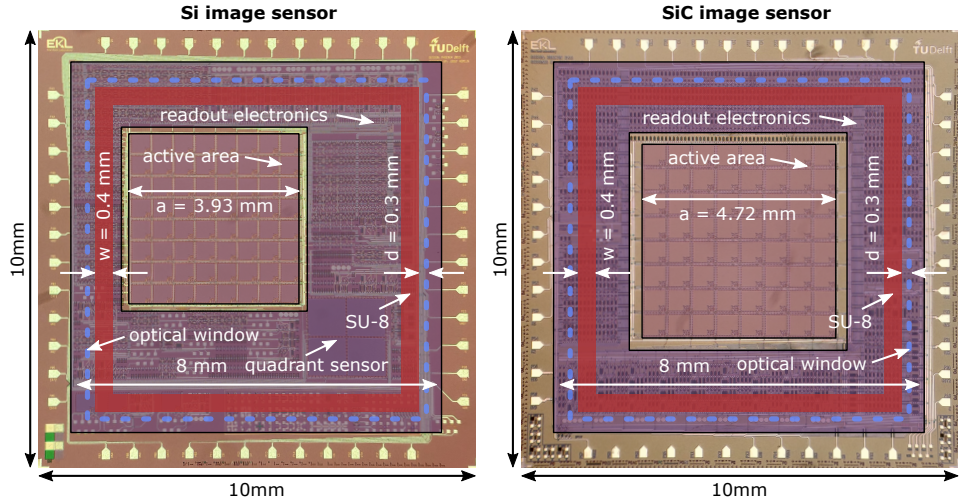
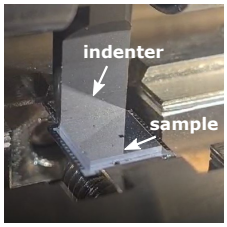


Figure 5.5: Illustration of the selected adhesive outline design on microphotographs of the fabricated chips in a) silicon and b) silicon carbide. The optical window outline, SU-8 pattern, readout electronics and active area are highlighted, with corresponding dimensions indicated. Note that the silicon quadrant sensor type is also well within the adhesive outline, whose location is identical on the SICCMOS9 chip A design.

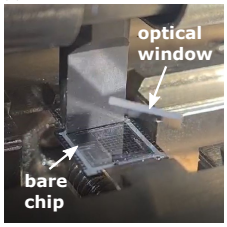
ther implementation. The next best option is a draw between pattern numbers 7 and 11, of which pattern number 7 is selected for further integration as the optical windows never detached during experiments. In comparison, there was one optical window detachment for pattern number 11. Selected pattern number 7 complies well with the design target with almost twice the minimum required contact area.

The selected adhesive outline is illustrated on microphotographs of the fabricated opto-electronics chips in Figure 5.5. Both designs have the adhesive outline directly on top of the readout electronics, which is area efficient compared to approaches that would require empty area for the bond interface, such as the eutectic bonding counterpart. Before the bond strength is characterized on fabricated samples, the light mask is implemented on top of the optical stack. The conclusions can therefore be made on the completed devices, rather than on an intermediate fabrication step. This light mask is implemented by sputter deposition of a 2 µm thick Al layer, patterned by lithography. More details on the light mask are given in the next section.

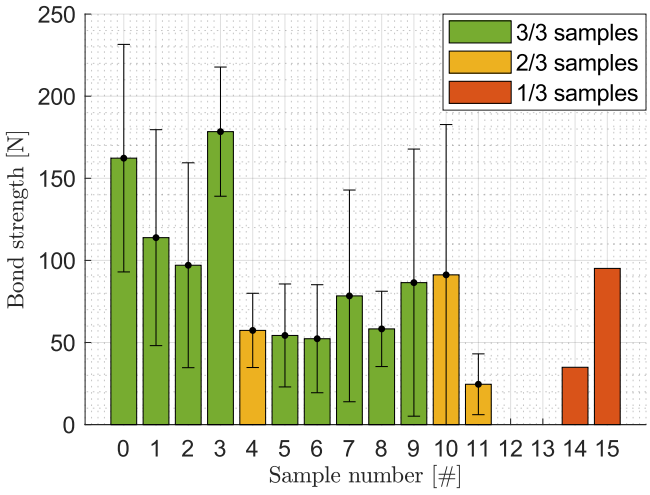
First implementations are made on the silicon test substrates, following the bonding procedures described in the proceeding paragraphs, and using the 16 outline patterns. This is a cost-effective approach as the silicon carbide wafers are at present still considered costly. The die shear tests are performed after dicing of three silicon test wafers, with the results listed in Figure 5.6. It is concluded that the bond strength magnitude is in the same order of magnitude for all samples, but smaller than the predicted bond strengths in Table 5.1. The selected pattern design of number 7 has a measured bond



(a)



(b)



(c)

Figure 5.6: Still images captured from a moving-picture of die shear tests performed in an indenter setup a) that pushes laterally against the optical window while measuring the applied force until the sample fails b) by detachment of the optical window. Die shear test results c) on 3 wafers indicating the bond force. Note that some sample numbers (see Table 5.1) have lower fabrication yield and thus could not be measured or with fewer samples.

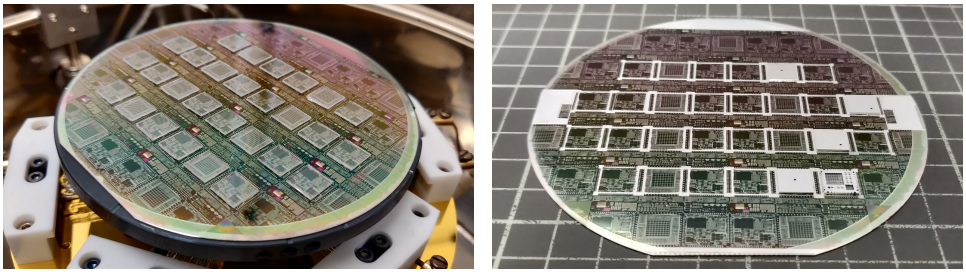
strength of (78 ± 65) N, or (6.9 ± 5.8) MPa, which is just short of the target. The prediction figures would be improved by increasing the safety factor f to 5, benefiting future work based on this wafer bonding approach. The detachment failure mode is between the SU-8 and optical window for all samples, that failed either during fabrication or during die shear testing, as no residues are found on the detached optical windows.

5.2.2. IMPLEMENTATION OF THE LIGHT MASK LAYER

Upon repetition of the developed procedure on the silicon carbide device wafers, the wet chemical processing involved in the light mask definition drastically reduced the yield (see Figure 5.7). Ultimately all remaining optical windows detached during the dicing of the wafer, thus demanding an addition to the fabrication to ensure proper adhesion of the optical windows. The discrepancy between the two processes is ascribed to the much larger wafer bow in the silicon carbide device wafers (several tens of µm), causing unintended intrinsic stress in the bond interface. Future work can optimize the bonding process, taking into account that silicon carbide CMOS wafers are costly.

The procedure is complemented by wafer-level deposition of glue at the optical window corners, resulting in the fabrication flow illustrated in Figure 5.8. The processed device wafers from Fraunhofer IISB are taken as the starting material for the wafer-level integration (Figure 5.8 step 1), and circuit interconnect is protected by a 0.8 µm silicon oxide passivation layer, with exposed bond and probe pad openings (Figure 5.8 step 2). The SU-8 adhesive outline is patterned by standard lithograyphy (Figure 5.8 step 3) and the 8 × 8 × 0.65 mm sapphire optical window[3] is centered on the larger device chip and attached by adhesive thermocompressive bonding (Figure 5.8 step 4), keeping access to the front side electrical connections. The complete wafer is coated by sputter deposition of 2 µm Al, which has good sidewall coverage (SEM images in Figure D.2), and additional glue is dispensed on the optical window corners (Figure 5.8 step 5). Finally, the aperture and bondpad clearance openings are patterned by wet etching to complete the device (Figure 5.8 step 6). Micro photographs of key steps in the fabrication are provided in

[3] Sapphire optical windows are used instead of glass due to the excellent optical transmission in the target UV range (60–80 % for 200–300 nm).



(a) (b)

Figure 5.7: Images of the silicon carbide CMOS wafer fully populated with 28 sapphire optical windows a) before thermocompressive bonding and b) after completion of the light mask module. Only five optical windows remain attached to the substrate, which corresponds to a yield of 18 %.

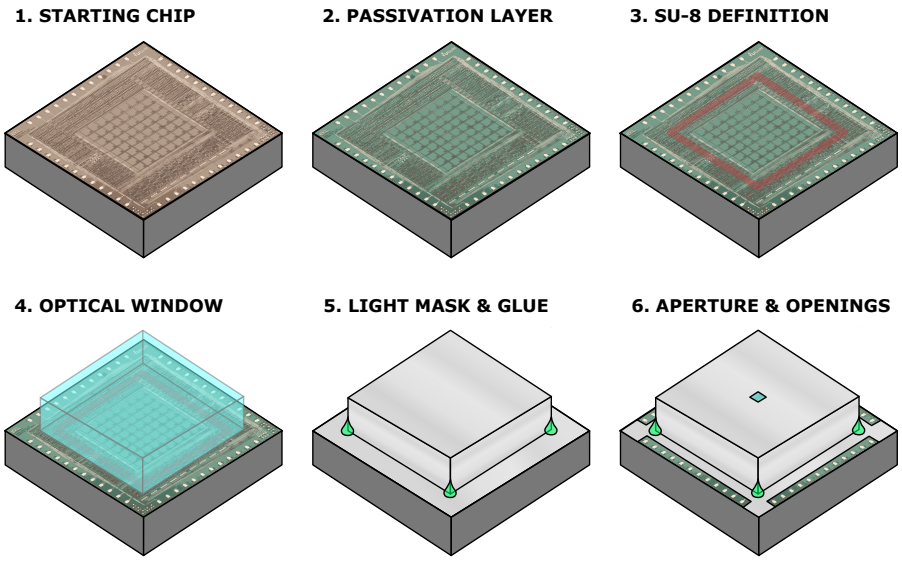
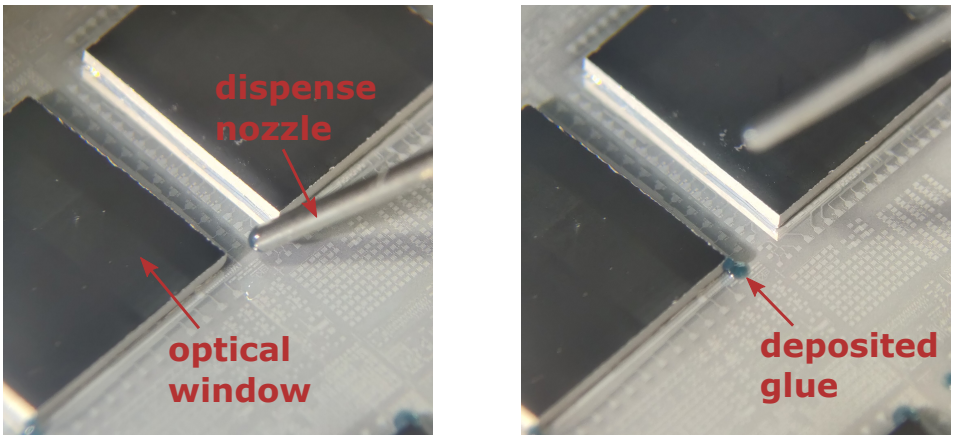


Figure 5.8: Fabrication of the 3D optics on the silicon carbide device wafers. The procedure starts with CMOS device wafers, that are protected by a passivation layer. The adhesive outline is patterned for thermocompressive bonding of the optical window, which is coated with an opaque light mask and secured further by added glue. The process is finalized by patterning the light mask layer to open the aperture and bondpads.

Figure 5.10 and the final result of the silicon counterpart is listed in Figure D.3.

The wafer-level glue dispension is captured in Figure 5.9, in which the dispense nozzle accurately deposits a glue droplet on each corner of the optical window by making



(a) (b)

Figure 5.9: Pictures illustrating the glue dispensing a) before deposition and b) after deposition. The dispense nozzle contacts the substrate at the very corner of the optical window. The dispensed glue droplet has a limited footprint, to ensure that the bondpads are not covered.

physical contact. The nozzle does not damage the CMOS devices, as these are covered by a thick passivation layer and the unpatterned metal light mask layer. It should be noted that it is not viable to replace the thermocompressive bonding completely with just the wafer-level glue dispension, as the glue will creep between the substrate and optical window interface. This is illustrated by the test samples in Figure D.4, with glue partially covering the active area of the sensor. As the glue will absorb the UV light, the

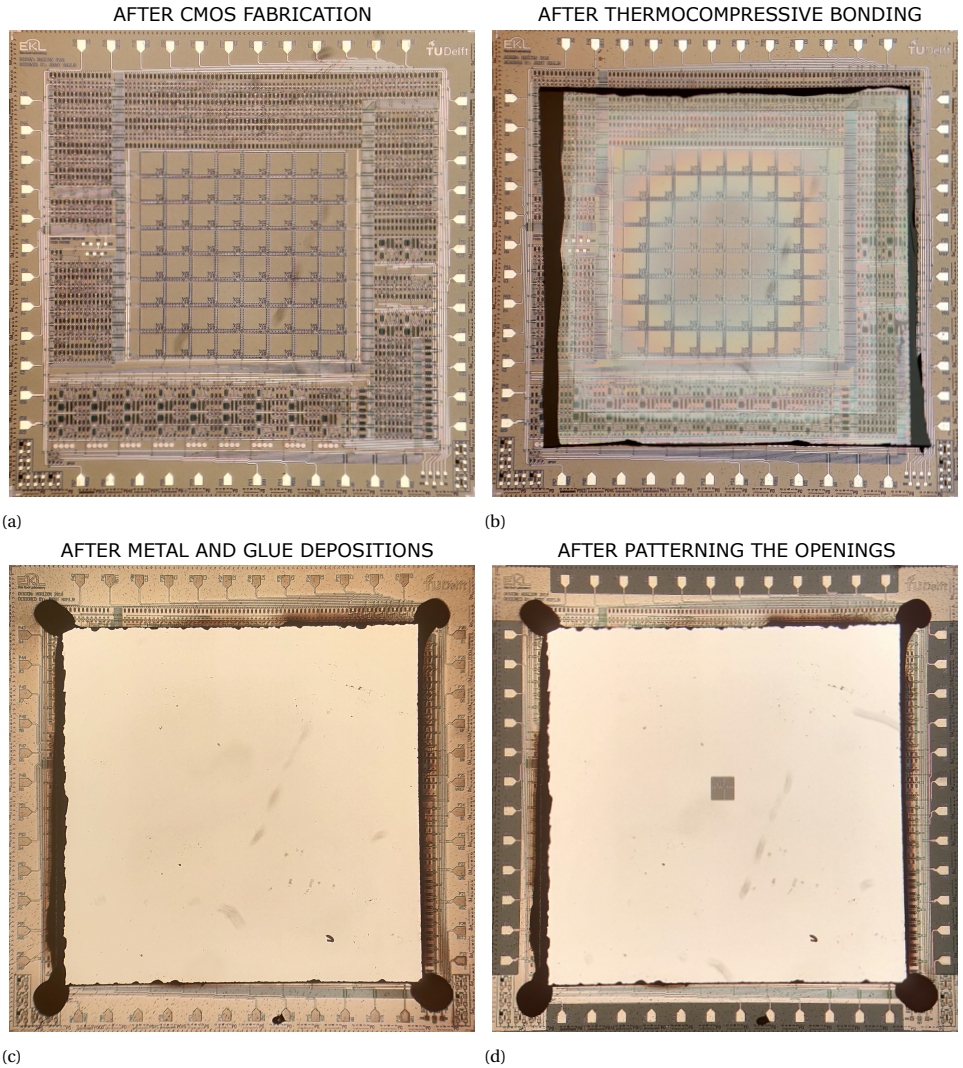


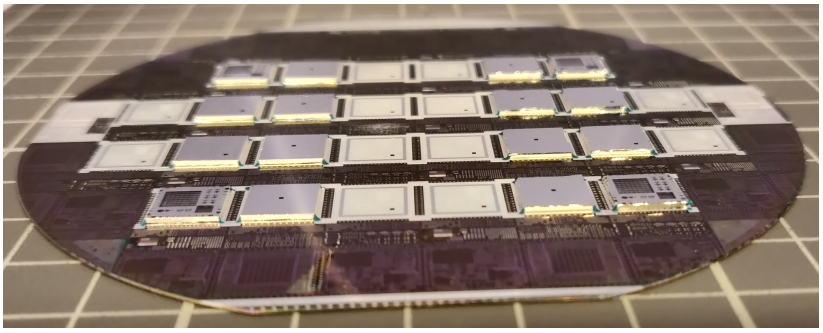
Figure 5.10: Overview by chip micro photographs of the key wafer-level fabrication steps in the successfully achieved patterned optical window integration. The results are given in the order of occurrence in the fabrication, including a) after the CMOS fabrication, b) after the thermocompressive wafer bonding, c) after sputter coating of Al and glue placement and d) the patterning of the aperture and bondpad regions.

sensor performance would reduce drastically as a result.

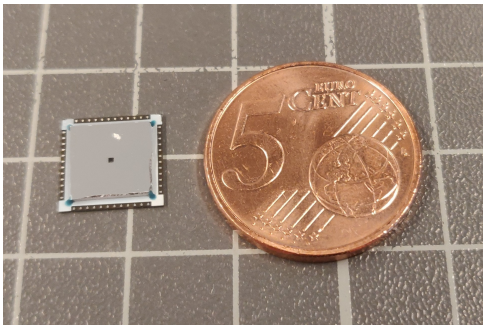
Finally, the metal light mask layer is patterned by spray coating the stack with positive photoresist and exposure in the mask aligner for the aperture and bondpad clearance regions separately, as the patterns are located in different focal depths. The wafer is developed in AZ400K 4:1, followed by wet etching in PES etchant at 35 °C for ~20 min.

5.2.3. VERIFICATION OF THE FABRICATED DEVICE

The aperture alignment in the light mask with respect to the photodetectors is investigated to ensure proper device operation. As the aperture pattern is at a vastly different focal depth than the alignment markers in the substrate, its pattern in the mask aligner alignment marker is not well exposed. The alignment must therefore be verified by a different approach. A look through the aperture from the wafer backside in Figure 5.12a is a quick indication that the alignment is adequate, as the metal traces around the pixels form a cross in the center of the aperture. A more accurate estimation is made by generation of the 3D image in Figure D.5 through the aperture, and leveling the top and bottom planes to ensure perpendicular inspection of the overlay alignment, which results in the alignment illustrated in Figure 5.12b.

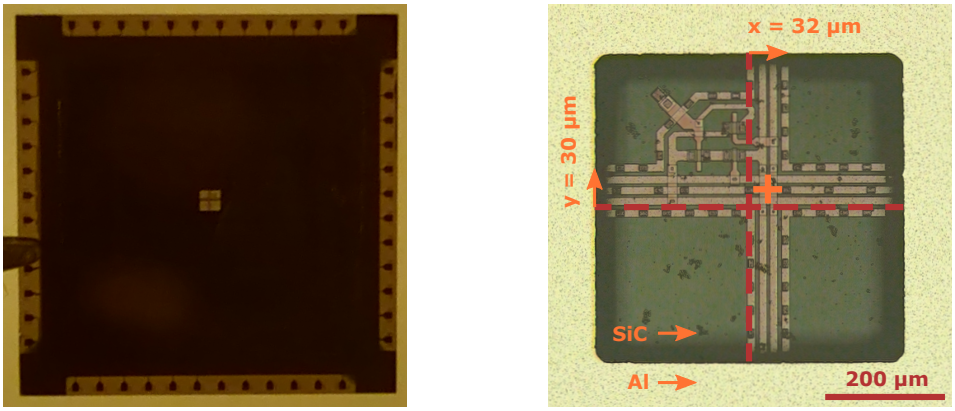


(a)



(b)

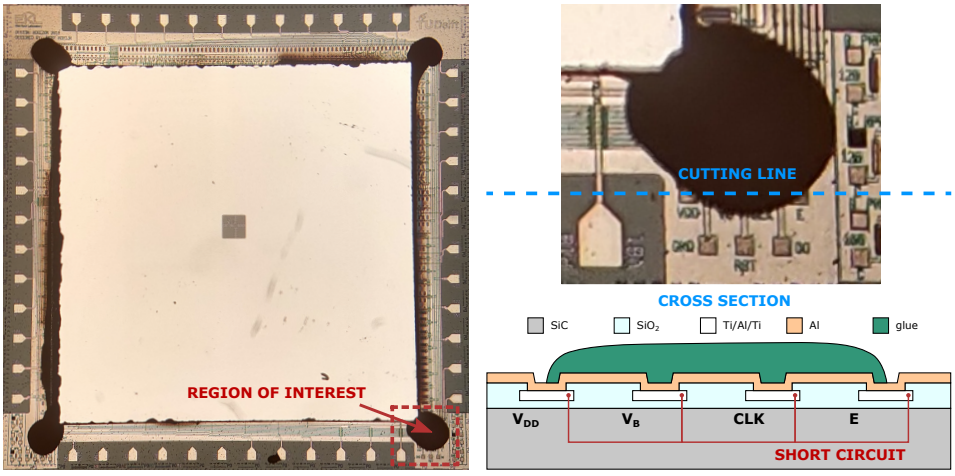
Figure 5.11: The wafer-level process a) on a 100 mm multi-project device wafer that incorporates 16 optical windows. Photograph of the fabricated sun position sensor chip next to a 5 eurocent coin for size reference, which successfully integrated 3D optics on the opto-electronic system in silicon carbide. The metal light mask on top of the integrated optics conceals the 1263 transistor system.



(a) (b)

Figure 5.12: Inspection of the aperture alignment a) through the backside of the transparent chip, which shows the centered cross inside the aperture opening. The generated perpendicular 2D image b) indicates the true alignment of the aperture to the photodetectors.

The achieved alignment is the result of front-side wafer alignment in a mask aligner, which is challenging due to the fact that the mask and alignment markers are in different focal depths. Though the overlay shift of 30 µm is deemed well enough for the much larger aperture and photodetectors (<6.5 %), it would be improved by upgrading the procedure to backside alignment. This was not yet possible, as it requires the addition of alignment markers on the wafer backside. Moving beyond this, the alignment would



(a) (b)

Figure 5.13: Micro photograph of the SICCMOS9 chip at a) the final stage of fabrication, highlighting the region of interest with a design error. At the region of interest, a cross section b) is illustrated to indicate the unintentional short circuits between all 7-probe mode pins.

become superior by using a wafer stepper. The present process did not yet allow this, due to the addition of a carrier wafer for contamination concerns that made the complete stack too thick (>1.2 mm). It is possible to combat the contamination concerns in future work to explore the alignment improvement.

It is almost inevitable to avoid all errors in complex system integration design, especially without the capability of automated layout verification and the addition of modules. As such, it was found at this stage that an error in the combination of the layout design and light mask design crept into this work, with devastating effects. To understand why, the problem is illustrated in Figure 5.13 by micro photographs and schematic cross-section. The problem is caused by the bond and probe pad opening mask, as the exposed probe pads for wafer-level 7-pin measurement are left exposed. The later deposited light mask is creating a short circuit between all the 7-pin connections, rendering the system inoperable. This error could be solved by updating the mask sets to not have these pins exposed, but due to the limited amount of SICCMOS9 device wafers this could not be pursued with the available resources. A quick fix was found by mechanically removing partial area of the glue and light mask metal layer.

5

5.3. ANGLE SENSITIVE DEVICE CHARACTERIZATION

The fabricated devices are characterized for their angular sensitivity. As these measurements are cumbersome, a selection of devices is reported in this section, including the silicon carbide quadrant sun position sensor, silicon carbide pixel array sun position sensor and the silicon diffraction grating sun position sensor. The used optical measurement setup is discussed, including the minor setup differences for each device.

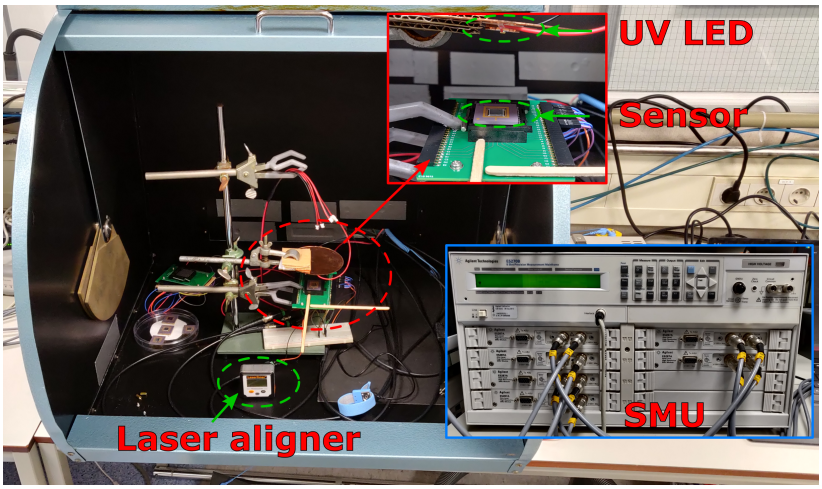


Figure 5.14: Optical measurement setup for angular response of the silicon carbide quadrant sun position sensor. A 5 mW SMD3535 265 nm UV-C LED is mounted on a copper plate perpendicular to the sensor and spaced 4–5 cm from the sensor. The PCB is rotated over one axis and aligned using a Laserligner DigiLevel Plus. The system maximum alignment error is estimated at 2°. The sensor outputs are measured by Agilent E5287A source-measurement units.

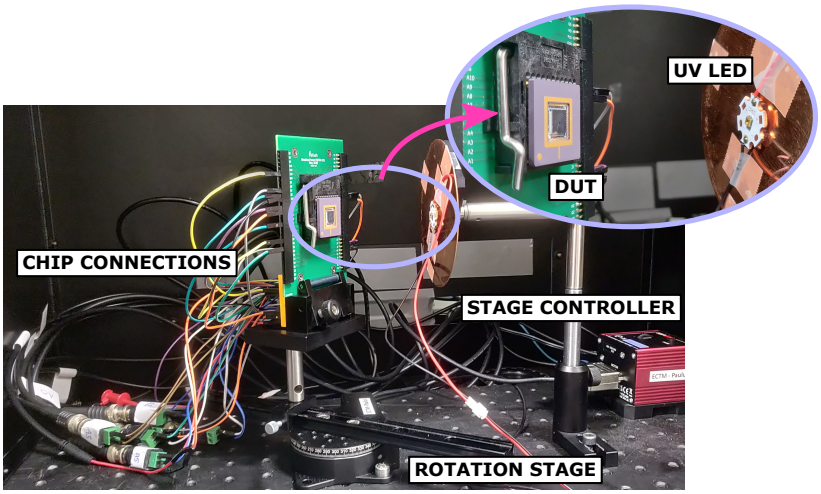


Figure 5.15: Optical measurement setup for angular response of the silicon carbide pixel array sun position sensor. A 5 mW SMD3535 265 nm UV-C LED is mounted on a copper plate and spaced 7 cm from the sensor. The PCB is rotated over one axis and aligned using an automatic rotation stage from Thorlabs. The system maximum alignment error is estimated at 0.1°. The sensor outputs are measured by the custom DAQ tool.

5.3.1. OPTICAL MEASUREMENT SETUP

The optical setup was subjected to continuous improvements, leading to slight differences between the setup details for each device characterization. The paragraphs and figures below provide the overview of used specifics for each measurement. Firstly, the

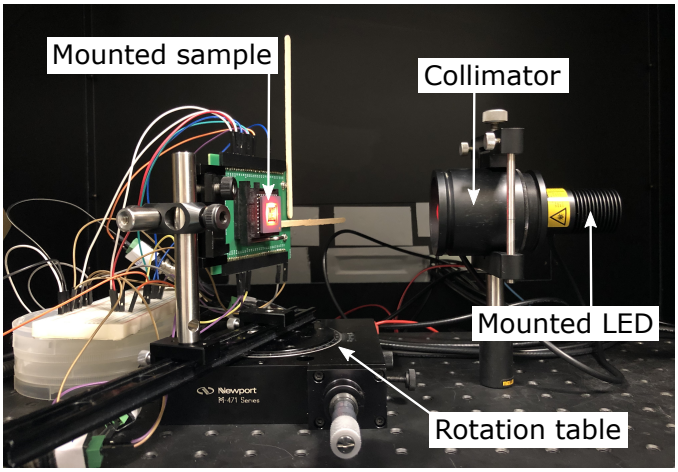


Figure 5.16: Optical measurement setup for angular response of the silicon diffraction grating sun position sensor. A 625 nm collimated light source is positioned perpendicular to the sensor. The PCB is rotated over one axis and aligned using a semi-automatic rotation stage. The system maximum alignment error is estimated at 0.1°. The sensor outputs are measured by the custom DAQ tool.

optical measurement setup in Figure 5.14 is used for the silicon carbide quadrant sun position sensor, and allows rotation of the interface PCB over a single axis. To measure the two perpendicular rotation axes, the PCB is rotated in the clamp. At each set angle, the quadrant photodetectors are read out over a bias range to investigate the best bias level. Secondly, the optical setup in Figure 5.15 is used for the silicon carbide pixel array sun position sensor. It is upgraded by an automatic rotation stage that is more accurate and is controlled by a PC, allowing automation of measurements over an angular range. The readout is switched to the described DAQ in Section 3.1, and external sources are supplied by TTi EL302RD power supplies. Finally, the silicon diffraction grating sun position sensor is measured under a collimated red light source in Figure 5.16.

5.3.2. QUADRANT SUN POSITION SENSOR

The silicon carbide quadrant sun position sensor fabrication is performed by the procedure described in the previous section. However, characterization of this device was done in an earlier stage of the process, involving chip-level fabrication of the 3D optics. In this early implementation, the optical window is pre-coated and patterned with the Al light mask and manually aligned to the device chip under an optical microscope. The optical window is attached to the substrate by using cyanoacrylate glue at one corner of the optical window to avoid interference with the optical sensor. Three devices are fab-

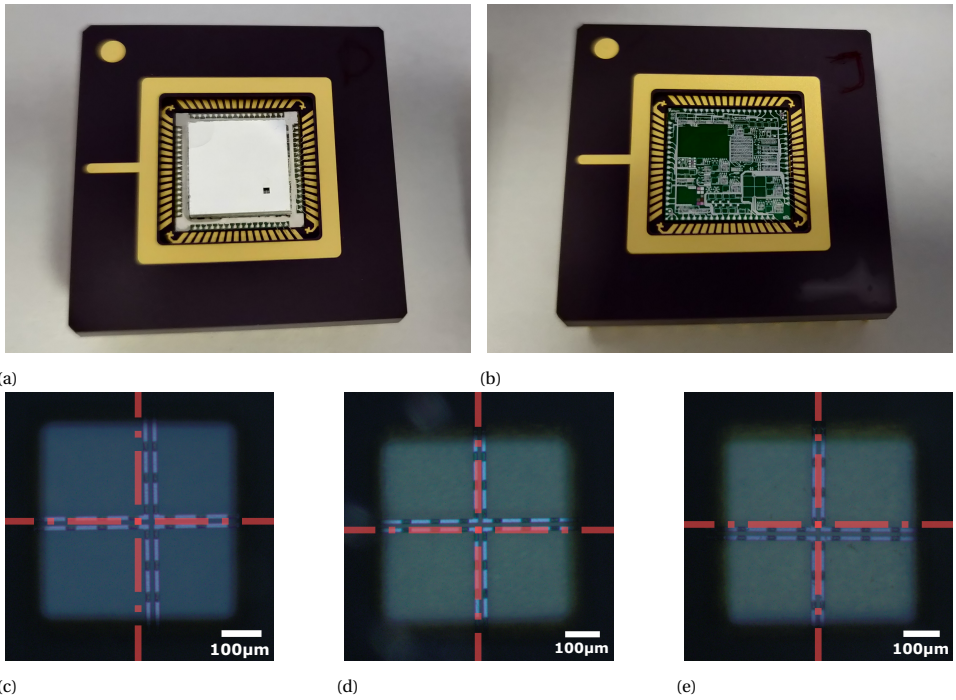
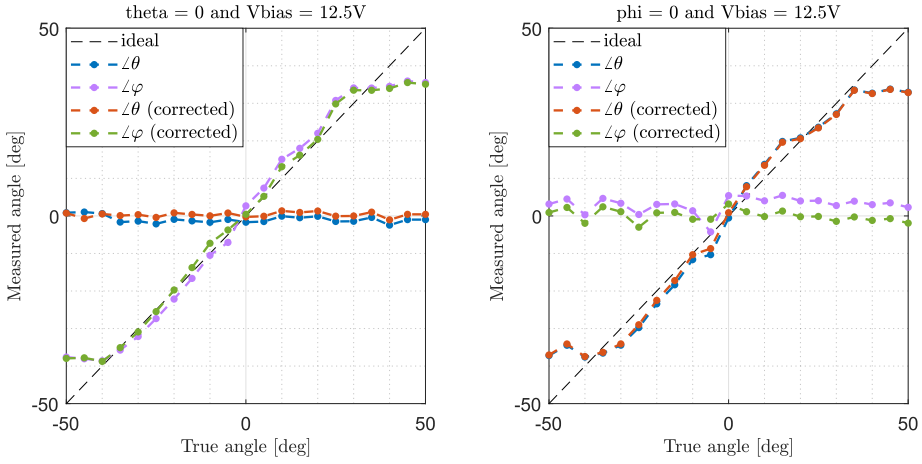


Figure 5.17: Photographs of the a) packaged quadrant sun position sensor and b) packaged bare multi-project chip. The aperture alignment is verified for c) device 1, d) device 2 and e) device 3 by optical inspection.

Table 5.3: Raw and corrected MAA within the FoV of three silicon carbide quadrant sun position sensor devices. The correction factors are numerically calculated and are unique for each device.

Device	MAA (raw)	MAA (corrected)
1	4.3°	2.8°
2	2.9°	1.9°
3	3.1°	2.6°



(a) (b)

Figure 5.18: Raw and corrected angular response of device 3, for a) constant $\angle\theta$ and b) constant $\angle\phi$. The substrate and each photodetector are biased at 0 V and 12.5 V respectively.

ricated, packaged and verified for the aperture alignment, as indicated in Figure 5.17.

The devices reach peak performance at a photodetector bias of 12.5 V, for which the angular responses of both rotational axes are reported in Figure 5.18 for device 3. These responses are calculated by following the readout methodology described in Section 2.1.2. The sensor responses show angular sensitivity in a FoV of ±33°, with a MAA of 2.9° for the best performing device in the sample set (see Table 5.3). This is further improved to a MAA of 1.9° by numerical calculation of calibration constants C_x and C_y, as specified in Section 2.1.3.

5.3.3. PIXEL ARRAY SUN POSITION SENSOR

The pixel array sun position sensor device is fabricated on wafer-level as described in Section 5.2, and the packaged chip is depicted in Figure 5.19a. The device suffers from fixed pattern noise[4], which is filtered out by capturing a dark measurement (see Figure D.6 and Equation D.2). The serial input and filtered output signal data of a single chip is reported in Figure 5.19b for an arbitrary incident angle of the light. The uncor-

[4]Fixed pattern noise is caused by discrepancies between individual photodiodes and/or pixel signal readout paths. It is furthermore characterized by its stable nature.

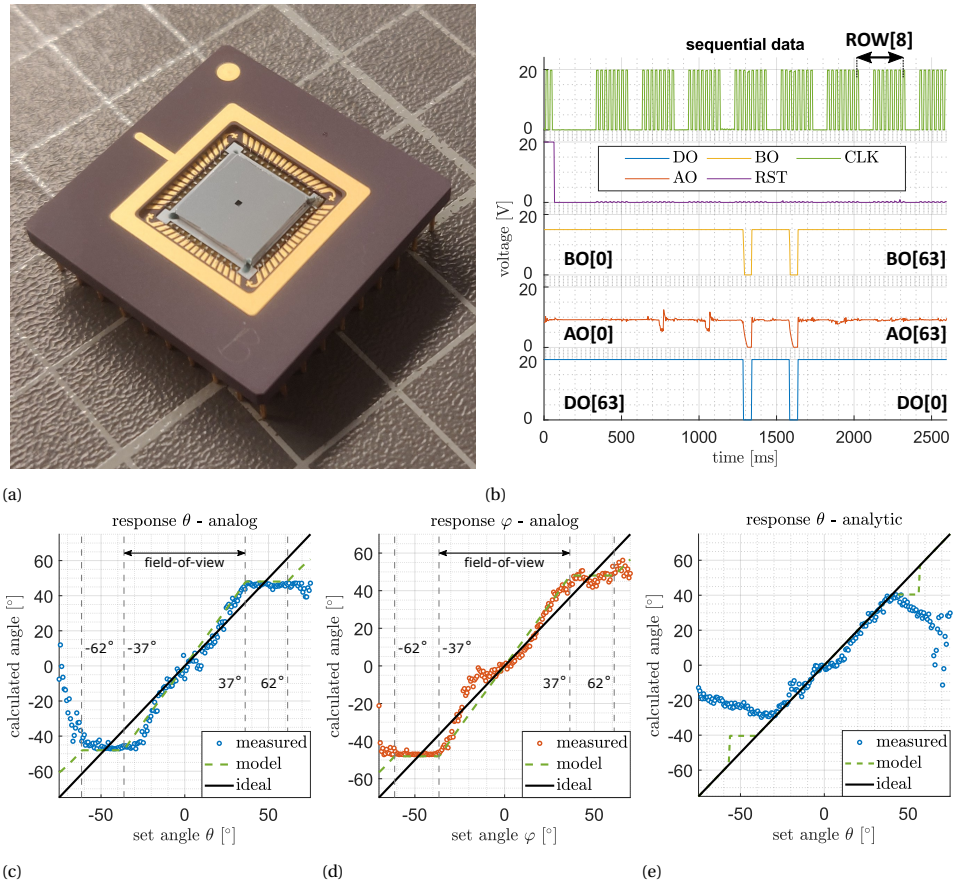


Figure 5.19: Overview image of a) the packaged silicon carbide pixel array sun position sensor, with the b) raw sequential input and output signal data. The system analog output mode is selected and corrected using a cosine function, for rotation over the c) θ and d) φ axes. An indication of e) using an analytic model instead of the weighted average model is provided. The incident light angle is swept over a ±70° range with 201 steps.

rected angular results of all three modes are provided in Figure D.7, with the comparator output mode resulting in just five levels for the extracted angle rendering it only useful for quick verification if the sun direction is perpendicular, under a medium angle or high angle. The 2-bit mode allows for much more output levels, which scaled proportionally with the added signal levels per pixel. The analog mode reveals the response curve of the sun position sensor device, which shows non-linearity and deviation from the model prediction.

The angular response is derived using the analog output mode over both rotation axes using the weighted average readout methodology described in Section 2.2.2, and reported in Figures 5.19c and 5.19d. This angular response is corrected by a cosine multiplication (see Figure D.7 and Equation D.1) and matches the predictive model well over a ±62° range, including the flat response near the limit of this range. On contrary, the

predicted field-of-view is the complete ±90° for this given geometry (due to refraction as shown in Section 2.1.1), but it must be noted that the signal quickly drops off by a combination of increased reflection and the cosine drop-off[5], that predicts that over half of signal is lost at high incident angles >60°.

The flat response at the higher incident angles is caused by blind spots whenever the cast light spot is completely inside a single pixel. This further validates the device, but to make full use of the captured range the aperture dimension should be made larger than the dimension of a single pixel (i.e. $L > (a/8)$) in future implementations. The effective field-of-view is therefore reduced to ±37°, in which a MAA of 5.7° is reached over both rotation axes. Finally, the angular information is extracted by an analytic model by direct comparison of pixels in a region of interest. As in this case the light spot is smaller than a photodetector, the basic quadrant methodology is employed locally to find the centroid. The result is given in Figure 5.19e and reaches an improved mean angular accuracy of 3.1° in the same field-of-view. Although the performance is increased, such analytic algorithms should be used with care as misidentification of the region of interest results in large errors in the extracted angular information.

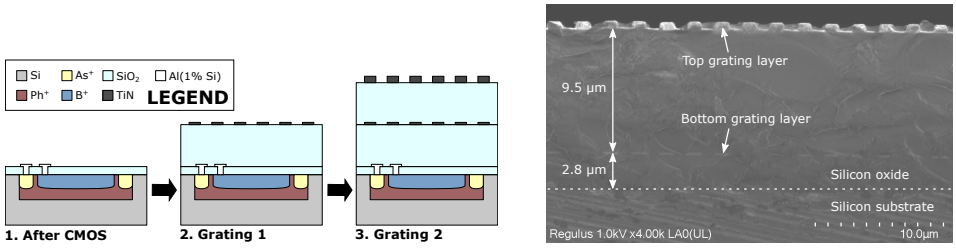
Though the analog mode is most accurate, application in harsh environment would benefit from a digital communication interface to mitigate environmental distortion effects. The comparator mode response is improved by scaling the amount of pixels in the array, but this is challenging considering the technology feature size constraints. Another approach is to increase the amount of bits in the ADC, which is less demanding on area consumption. Furthermore, future work can address the reduced signal in higher incident angle cases by implementation of a dynamic range, ensuring that large signals do not saturate pixels and small signals stick out from inter-pixel deviations. This mechanism may rely on a dynamic readout frequency to change the pixel integration time, or dynamic biasing to optimize the pixel response in both cases.

5.3.4. DIFFRACTION GRATING SUN POSITION SENSOR

The work on angle sensitive pixels was performed by S. Şanseven as part of her thesis work in collaboration with and under supervision of the author. Parts of this section have been included in her dissertation [21]. Further measurements and sample generation was carried out by P. van der End as part of his thesis work in collaboration with and under supervision of the author.

The double diffraction grating stack fabrication is performed after the BICMOS7 process and is illustrated in fig. 5.20a. It starts by deposition of a 2.7 µm PECVD oxide layer followed by sputter deposition of 100 nm TiN, which is patterned by standard lithography and dry etching to implement the bottom grating layer. This procedure is repeated by a 9.5 µm oxide and a 500 nm TiN layer to implement the top grating layer and finalize the device. The cross-section of the fabricated amplitude grating device is reported in fig. 5.20b and the bare chip overview image of a phase grating device in Figure 5.21a. No attempts are made to implement a corresponding grating stack on SIC-CMOS9, as this demands grating pitch dimensions below the capability of the stepper in the EKL facilities, and the amount SiC device wafers are limited for such prototyping.

[5] The cosine drop off is caused by reduced photon flux density on the photodetector with increased incident angle, which follows the relation $\Phi = \cos(\angle\theta)$.



(a) (b)

Figure 5.20: Schematic illustration a) of the diffraction grating stack fabrication steps on top of BICMOS7. The fabrication result b) SEM image of the cross section of a device with 2 µm pitch in-phase diffraction gratings. The oxide layer thicknesses between the substrate, first grating layer and second grating layer are highlighted.

The raw pixel outputs of an amplitude grating device are given in fig. 5.21b for an arbitrary fixed angle. Each pixel has a decaying signal during readout, of which the slope corresponds to the generated photo current. The readout cycle of an individual pixel spans a full CLK cycle and indicates that the linear decay of the pixel output signal is negatively affected at the high-to-low transition of the CLK. As the surrounding system updates its state on the CLK falling edge, a possible explanation for the affected pixel output is the brief change in the connected pixel load, which causes it to leak additional charge unintentionally. For reliable readout, only the first half of the readout cycle is therefore captured. Future work on this system would benefit from better mechanisms to protect the stored pixel charge.

Considering the readout methodology described in Section 2.3.2, the amplitude grating ASP outputs are used to extract the raw angular periodic information as depicted in Figure 5.21c, indicating close compliance to the simulation results of the same conditions. The minor deviation in the angular period is ascribed to process deviations such as the deposited oxide layer thickness. The periodic response is then transformed to the full angular range by identification of the angular period and fitted angular sensitivity β, as reported in Figure 5.21d. Manual identification of these periods and fitting β for each period results in a MAA of 0.4° in the investigated ±26° FoV, but such a look-up table is not desirable for device operation. Using a fixed mean period and mean β still results in a high MAA of 0.6° in the same FoV, but does reveal two large offsets as was predicted in Section 2.3.3. Lastly, a phase grating device is readout similarly and results in the angular response of Figure 5.21e, which reaches a MAA of 2.8° in an investigated ±45.5° FoV. The higher EQE of the phase grating device allows for the larger FoV operation.

The reported diffraction grating sensor is not yet verified for operation for different wavelengths or broadband light, but is expected to be severely distorted in different light source conditions. Further investigation would therefore benefit future work and alternatively the photodetectors could be integrated with optical bandpass filters or odd-symmetry spiral phase gratings [22, 23]. Furthermore, the angular period of the ASP devices is identified in post processing with knowledge of the set angle. The next generation of devices should integrate course ASPs on-chip to perform the angular period identification. Together with the addition of perpendicular fine ASPs for angular detection on two axis, a minimum of 12 pixels is required.

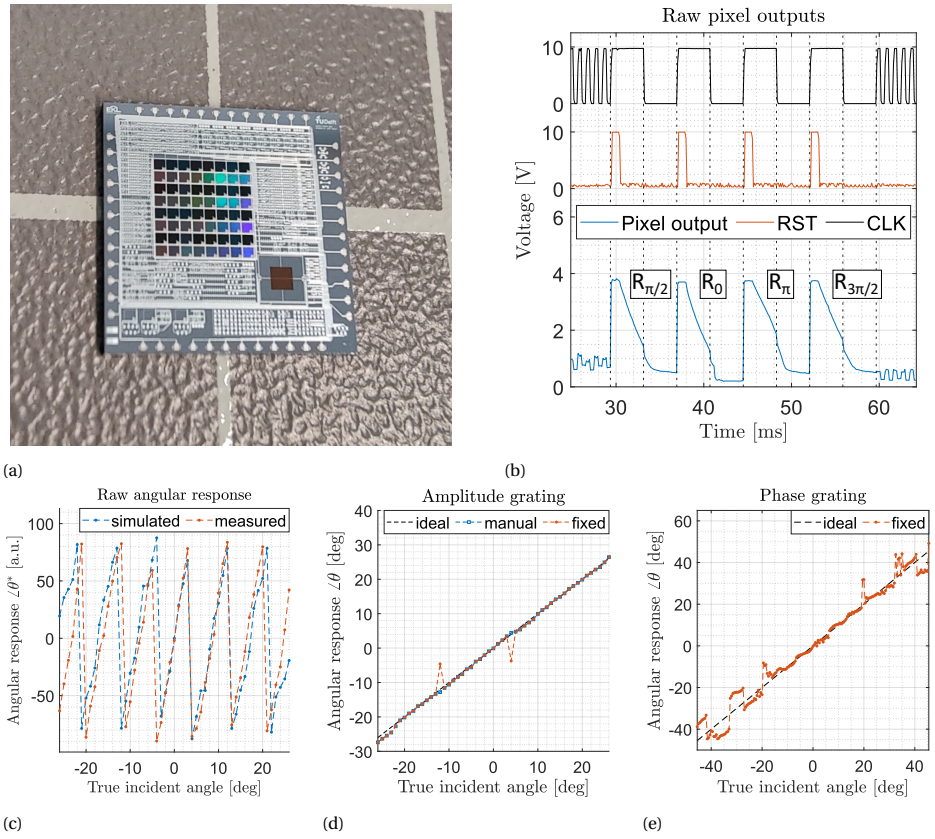


Figure 5.21: Overview image of a) the diffraction phase grating sun position sensor, exhibiting vibrant colors on the pixels caused by diffraction effects. Amplitude grating measurement results of b) raw pixel outputs for a fixed incident angle, were the fast CLK before and after the pixels of interest quickly cycle through the 64 pixel array. The extracted c) raw angular information $\angle\theta^*$ for a single rotation axis, which is translated to d) the full angular information $\angle\theta$ for the amplitude grating device. Similarly, the e) full angular information $\angle\theta$ for the phase grating device is reported.

5.4. HIGH TEMPERATURE OPERATION VERIFICATION

To extend the SiC sun position sensor temperature range, preliminary verification at elevated temperature up to 200 °C is investigated. This is performed on the pixel array sensor with fabricated wafer-level optics, including the CTAT temperature sensor that was integrated on-chip. In addition to the measurement equipment used previously, the temperature controlled measurements are performed in a Tenney TPS chamber in combination with a TENMA 72-7780 multimeter for temperature monitoring.

5.4.1. SILICON CARBIDE PIXEL ARRAY SENSOR AT HIGH TEMPERATURE

The pixel array sun position sensor is placed inside a temperature controlled chamber for verification. Unfortunately, the equipment necessary to perform angular dependent

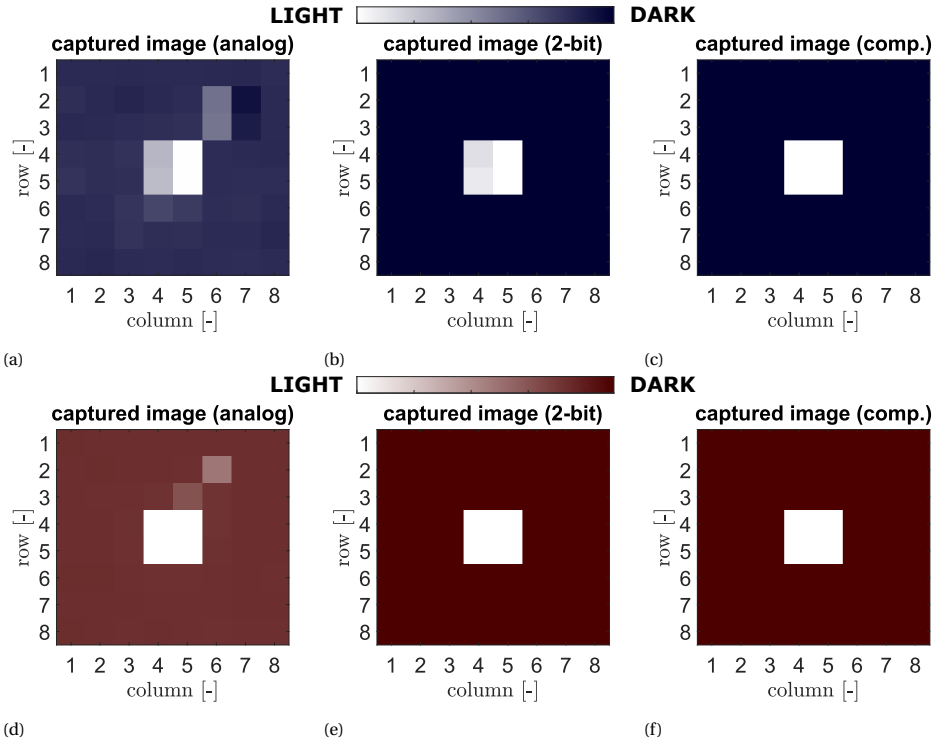


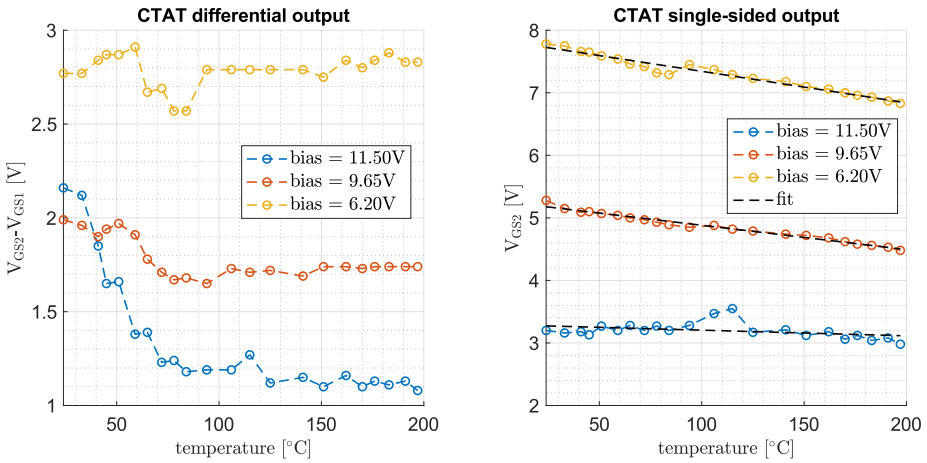
Figure 5.22: Overview of captured 8 × 8 pixel images of the a) analog, b) 2-bit and c) comparator output modes at room temperature. The repeated measurements at 200 °C of the d) analog, e) 2-bit and f) comparator output modes. Different colorbars are used for differentiation between the temperature levels.

measurements is not rated for the elevated temperature, so only perpendicular illumination is performed. The captured images of the three output modes at room temperature are listed in Figures 5.22a to 5.22c. The UV-C light source is placed much closer to the device than before for practical reasons, such as limited space and vibration, which saturates the pixel responses.

The measurement is repeated at 200 °C and results in sequential data without indications of signal degradation and no visible damage to the device. The imager fixed pattern noise does change at this temperature, which means that a separate dark measurement is taken to correct the images. Lastly, it should be noted that the UV-C light source is removed from the setup during the controlled heating and only placed for the measurements, to minimize degradation of the light source. Future characterization would benefit from placement of the light source outside of the temperature controlled chamber, as well as the addition of angular control functionality.

5.4.2. INTEGRATED CTAT SENSOR VERIFICATION

The pixel array sensor is integrated with the CTAT sensor reported in Section 3.4.2. This sensor was previously current biased, with peak performance below 1 µA. This is how-



(a) (b)

Figure 5.23: Electrical measurement results of the integrated CTAT sensor. The device is voltage biased using an off-chip power supply and read out by a) the differential output or b) the single-sided output.

5

ever less conventional for integration in harsh environments such as outer space. So instead, the CTAT sensor is now voltage biased and read out using its differential output. The temperature response in this mode is depicted in Figure 5.23a, but does not show the expected linear behavior. This is explained by the changing device parameters with temperature, which therefore not result in a constant current bias.

Fortunately, a linear response is obtained by considering only the single-sided output of the device. The best linearity is is found for a 9.65 V bias, reaching a $-3.9\,\mathrm{mVK^{-1}}$ sensitivity, which is just over half the sensitivity reached through current biasing. This shows that both the bias strategies can be used to read out this CTAT temperature sensor. Future work would benefit the implementation of on-chip biasing circuits and extending the temperature range.

5.5. CONCLUSIONS AND RECOMMENDATIONS

A scalable integration approach for the sun position sensor 3D optics was demonstrated. The proposed technology enables further miniaturization and cost reduction of these devices, which facilitates the satellite miniaturization trend. The BICMOS7 and SICCMOS9 technologies described in the previous chapters, are incremented by one design layer to include a passivation layer between the top interconnect layer and optics.

The first considered approach in this chapter for the integrated optics is laser cutting glass substrates. The laser cutting technology is slow, as it takes several hours to cut the patterns. On top of this, the process is destructive as it heats up the substrate locally. This results in discolorment, incomplete cuts due to sintering, or even fractures in the substrate. The process would be improved by migration to shorter wavelength systems or LIDE technology. The second approach is by 3D printed transparent polymer in an SLA printer. As such systems are not generally adopted for microfabrication, the overlay

alignment is poor and not usable for the optics integration. On top of this, the technology suffers from warping effects, which results in detachment of the printed layer over time. Both problems could be solved by adopting a hot embossing approach, which is presently not available in EKL facilities. Finally, thermocompressive bonding of optical windows with SU-8 photoresist is performed successfully. This approach does not have the challenges of special processing on the optical windows other than conventional dicing and manual placement of the optical window yields proper overlay alignment.

The thermocompressive bonding approach is scaled to wafer-level using standard lithography to spin coat and pattern the SU-8 photoresist directly on top of the device wafer. The selective deposition allows for the implementation of just an outline around the image sensor, thus avoiding absorption or interference with the incoming UV light. The sapphire optical window area is furthermore slightly smaller than the device chip area, to allow for front side electrical contacting in the packaging stage. The SU-8 thickness is reproduced at (9.27 ± 0.23) µm and a FoM is defined to select the best outline pattern, using the yield and calculated bond strength of a set of different samples. The selected outline pattern has an interface area of 11.2 mm^2 with a bond strength of (6.9 ± 5.8) MPa measured on the silicon chips by die shear testing. The failure mode for optical window detachment was always the interface between the SU-8 and optical window, regardless of the fabrication stage. Finally, the metal light mask layer is sputter coated on the wafer and patterned by use of spray coating photoresist and wet etching.

Repeating the developed fabrication approach on the silicon carbide device wafers unexpectedly resulted in drastically lower yield, predominantly in the implementation of the metal light mask. This is ascribed to the significantly larger wafer bow in the silicon carbide device wafers, which adds undesired stress in the bond interface. Process optimization possibility was limited in this work, due to the low availability of silicon carbide device wafers to test with. Instead, the developed procedure is complemented by deposition of glue on the optical window corners on wafer-level before the lithography on the metal light mask, which brought the yield of the optics to 100 % for the remaining device wafers. It is furthermore concluded that the SU-8 outline is still indispensable, as it acts as a blocking layer against glue that creeps in between the bonded interface into the active sensor area.

A crucial aspect is the overlay alignment of the aperture to the device chip. This proved to be challenging to verify, as separate exposures are used for the aperture and the bond pad clearance in the same metal light mask layer. The standard alignment markers are inadequate for verification due to the difference in focal depth, thus demanding additional attention in future fabrication processes. Alternatively, optical measurement through the aperture yields a typical 30 µm lateral overlay shift with negligible rotation. For the current technology, this corresponds to <6.5 % of the photodetector dimensions, which is considered good enough for correct operation. However, this alignment should be improved in future implementations when miniaturizing the photodetectors. The alignment strategy would be improved by tackling the problem of different focal depths, which may be done by switching to backside alignment. Improving the alignment further, the superior overlay accuracy of a wafer stepper is advised.

The integrated sun position sensors are packaged using wire bonding to a ceramic package and measured in an optical setup that allows for varying the incident light an-

gle. The silicon carbide quadrant sensor was characterized first, which was performed in an earlier stage of the project that involves chip-level fabrication of the optics. The measured devices reach peak performance at a photodetector bias of 12.5 V, reaching a MAA of 2.9° in a ±33° FoV without calibration. Upon calibration of the devices by numerical calculation, the MAA is improved to 1.9°. The silicon carbide pixel array sensor was characterized next and was fabricated by the developed wafer-level technology. After including signal conditioning, the device was able to reach a MAA of 5.7° in a ±37° FoV. Adopting an analytical readout scheme reaches an MAA of 3.1° in the same FoV, but is prone to misidentification of the region of interest. The found MAA matches well with the prediction made in Section 2.2.3 for the effects of overlay misalignment. The device could be optimized by reducing the fixed pattern noise, increasing the overlay alignment accuracy, increasing the amount of pixels, ensuring an aperture dimension larger than the pixel dimension and by increasing the ADC resolution. Lastly, the silicon diffraction grating sensors are characterized for monochromatic light, showing promising MAA of 0.6° in a ±26° FoV and 2.8° in a ±45.5° FoV for the amplitude grating and phase grating devices respectively. Future work should focus on broadband light sources and on-chip measurement of the angular period.

Finally, the silicon carbide pixel array sun position sensor is measured up to 200 °C for perpendicular UV illumination. The sequential outputs indicate no signal degradation and no visible damage to the device is observed. The three output modes operate as intended at elevated temperature, but require a separate dark measurement for fixed pattern noise correction. Additionally, the integrated CTAT sensor is measured in the same range and is voltage biased. The sensor output is linear considering its single-side output and reaches a sensitivity of $-3.9\,\mathrm{mVK^{-1}}$.

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6

CONCLUSIONS AND RECOMMENDATIONS

THIS final chapter summarizes the research conclusions, considering the research questions in Section 1.4. Recommendations are provided for each topic to help progress future endeavours on the respective topic.

6.1. SUN POSITION SENSOR ARCHITECTURES

Research question:

> *"What sun position sensor architecture is best suited for the envisioned proof-of-principle and how can this be determined?"*

It was already concluded in the introduction chapter of this work that the collimating sensor architecture is the best match with microfabrication technology due to its planar nature. However, even within this type of architecture, there are many different implementations reported in literature. In Chapter 2, the geometric dependencies are derived for the two leading design parameters, which are the field-of-view and accuracy. These parameters are orthogonal in nature, a larger field-of-view yields a lower accuracy, so the designer must compromise. Choosing a different optical window material than air positively affects the field-of-view and negatively affects the sensitivity, due to the effects of optical refraction.

Both the quadrant sensor and pixel array sensor are often used in literature reports and are therefore simulated extensively to help in the design choices. The advantage of the quadrant sensor is its simplicity, consisting of only four photodetectors, though its disadvantage is the need for calibration of each device. Calibration efforts are reduced for the pixel array sensor at the cost of higher device complexity. Considering the trade-off in calibration and complexity, both sensor architectures are selected for the proof-of-principle implementation.

Finally, a non-conventional architecture is considered, which omits the need for an optical window and uses fine-pitch diffraction gratings instead. Its principle of operation is different from the conventional counterparts, relying on intensity patterns below a grating stack instead of casting a light spot through an aperture.

Recommendations regarding sun position sensor architecture:

- In general, the field would benefit from new architectures that are planar in nature, such as the proposed diffraction grating sensor. In particular those that limit the need for thick millimetre scale layers that are not standard in microfabrication deposition technology.
- The terms 'analog' and 'digital' sun sensors are not cohesively defined in scientific reports. If used, the terms should therefore always be explicitly defined.
- Albedo insensitivity, or visible blindness, is often defined in datasheets for a fixed wavelength. This provides an approximation, but its responsivity curve should always be used in combination with the spectral information of the relevant light sources to calculate the exact ratio.

6.2. INTEGRATED SILICON CARBIDE ELECTRONICS

Research question:

> *"How can the sun position sensor devices be fabricated in silicon carbide and where can this be performed?"*

The implementation of integrated circuits in silicon carbide has been a field of research for the last few decades, spanning the BJT, CMOS, JFET and MESFET device types. The fabrication of such devices demands specialized equipment to realize for example implanted regions, ohmic electrical contacts or trenches in the substrate. As the in-house facilities of EKL do not offer such equipment, the fabrication in silicon carbide is outsourced. As this comes with long lead times, the in-house silicon CMOS technology is used for rapid prototyping.

At present, two silicon carbide technologies are accessible to external users, which are a BJT technology at the KTH in Sweden and a CMOS technology at Fraunhofer IISB in Germany. The BJT technology is implemented by epitaxial layer stacks, which is demanding if NPN, PNP and photodetector devices are required. In contrast, the CMOS technology is implemented by ion implantation, with proven integration of the NMOS, PMOS and photodetector devices. For this reason, the CMOS technology at Fraunhofer IISB is selected in this project.

Wafer-level investigation and comparison is performed in Chapter 3 for devices and circuits in both the EKL silicon and Fraunhofer silicon carbide technologies. The investigated circuits operate as intended in both technologies with promising preliminary yield figures >70 %. As expected, the silicon implementations are superior over the silicon carbide counterparts at room temperature. Increasing the operating temperature to 200 °C reveals increased leakage current in the silicon devices by several orders of magnitude, while no increase is observed for the silicon carbide devices.

The silicon carbide device performance increases with temperature, but this change in performance is not necessarily improving the circuit behavior. Additionally, resistive and five-transistor CTAT temperature sensors are characterized in the same silicon carbide technology. The resistive sensors reached a largest change in resistance of 79 % over a range of 25–200 °C and the current biased CTAT showed maximum sensitivity of $-7.5\,\mathrm{mV\,K^{-1}}$. Such temperature sensors are vital to control system implementations for a wide temperature range.

Recommendations regarding integrated electronics in silicon carbide:

- Given the rise and fall of several silicon carbide technologies over the past decades, it is vital that the ones in existence today remain available. This allows researchers to reproduce reported results and make incremental contributions to the field.
- With only two accessible silicon carbide technologies at present, diversification should be encouraged. This could be in the form of competing technologies, as well as joint research activities by heterogeneous integration (system-in-package) of different technologies.
- The temperature operating range of silicon carbide devices is impressive, but the changing performance makes stable circuit behavior challenging. Accurate temperature measurement on-chip is therefore vital to allow for compensation mechanisms in future implementations.
- The silicon carbide technologies can generally be improved by focus on reduced ohmic contact resistance, additional interconnect layers, device miniaturization and expanded device modelling.

6.3. OPTO-ELECTRONICS AND INTEGRATION OF THE OPTICS

Research question:

> *"How to implement the wafer-level integration of the aligned sensor 3D optics with the on-chip photodetectors?"*

Both the silicon carbide CMOS technology at Fraunhofer IISB and the silicon technology at EKL allow for the integration of photodetectors in the existing design layers. Basic quadrant sensors are implemented by four larger photodetectors, and do not include integrated readout in favor of reduced chance on design errors. Additionally, a monolithic opto-electronic system is implemented in both technologies, housing 64 addressable pixels with integrated readout and control circuitry. Chapter 4 reports on the electrical and opto-electrical characterization of these systems, reaching faster refresh rates and lower power consumption compared to a reported similar system in the BJT silicon carbide technology.

Using the responsivity curves of the silicon and silicon carbide technologies in combination with solar intensity data, the albedo rejection ratios are 1.56 and 3.84 respectively. This seemingly small increase means a world of difference, as the silicon carbide image sensor did not record any signal for ambient light. Preliminary light spot

emulation on the silicon imager reveals some hardware layout design errors, which are successfully corrected in the silicon carbide imager, which in turn shows that the sensor operates completely as intended. Furthermore, individual photodetectors are measured up to 200 °C, exhibiting negligible change in the silicon carbide devices while it renders the silicon devices unusable.

Three different approaches towards the optics integration are investigated in Chapter 5, of which the thermocompressive bonding using SU-8 photoresist was found as best match with microfabrication technology. In the developed methodology, an outline of SU-8 is implemented around the active area of the image sensor by standard lithography. From predictive calculation and empirical investigation of the yield, the outline pattern is selected and found to have a bond strength of (6.9 ± 5.8) MPa on silicon samples. If was furthermore found that the failure mode was always the interface between the SU-8 and optical window, regardless of the fabrication stage.

The die-to-wafer bonding approach is highly repeatable on the silicon platform, but was found to drastically fall in reproducibility on the silicon carbide platform, predominantly during the wet chemical processing of the metal light mask. This discrepancy is ascribed to the larger wafer bow in the silicon carbide substrates, which induce unintended stress on the bond interface. As limited resources did not allow for process optimization, it was decided to add a fabrication step that secures the yield. For this purpose, glue droplets are dispensed at the optical window corners on wafer-level, directly after the metal light mask is deposited. This addition raised the yield of the optical windows to 100 % and allows for characterization of the devices. The SU-8 bonding layer is still a necessity, as the added glue droplets would otherwise creep in between the bond interface and cover the sensor active area.

Lastly, the overlay alignment of the aperture to the photodetectors is investigated. It is challenging to measure offsets, as the apertures are in a vastly different focal plane then its alignment markers. Optical inspection resulted in typical offsets of 30 µm, which are acceptable for the current device dimensions, but should be improved in further miniaturization.

Recommendations regarding silicon carbide opto-electronics and optics integration:

- The quantum efficiency of integrated silicon carbide photodetectors is adequate for UV imaging and the sun sensor, but should be improved for applications that exceed ~100 Hz.
- To pave the road towards VLSI design in silicon carbide, such as the reported 64 pixel imager, it is vital to develop automated design tools such as DRC or LVS.
- The reported silicon carbide imager may be improved by optimizing its photodetector hardware layout design, to reduce its leakage current and increase its signal. Additionally, the imager refresh rate could be improved by optimizing the comparator circuit for reduced output signal transition time.
- The die-to-wafer bonding by means of thermocompressive bonding is demonstrated on the silicon platform. Future work should aim to optimize this process

for the silicon carbide platform as well, to secure the optical window yield and omit the need for addition of glue.

- The alignment overlay of the aperture could be improved by switching to a back-side alignment in the mask aligner or by switching to a wafer stepper.

6.4. CHARACTERIZATION AND TESTING OF THE DEVICE

Research question:

"How reliable is the proof-of-principle in the current technology and what is the impact of the albedo and temperature?"

The fabricated sun position sensors are packaged in ceramic packages using wire bonding for electrical contacting to the chip front side bond pads. No attempts were made to cover the exposed wire bonds or chip in this stage. The opto-electrical characterization was performed in a custom setup that allows for angular rotation of the sample over a single rotation axis at a time. Only a selection of sun position sensor devices are characterized for angular response.

Firstly, the silicon carbide quadrant sun position sensor was tested, which was implemented in an earlier stage of the project using chip-level fabrication of the optics. It was found that a 12.5 V bias results in the best performance, reaching a MAA of 2.9° or 1.9° in a ±33° FoV before or after calibration, respectively. Secondly, the silicon carbide pixel array sun position sensor was measured, which was fabricated by the developed wafer-level integration of the optics. Its visual comparison to the conceptual design is illustrated in Figure 6.1. This device reaches a MAA of 5.7° in a ±37° FoV by weighted average readout, or 3.1° in the same FoV by analytical readout. The latter should be used with care, as it is prone to large offset if the region of interest is misidentified. The found MAA is matching well with predictive model in Chapter 2, given the overlay misalignment. Thirdly, the silicon diffraction grating sun position sensor was investigated, which was fabricated without bulky optics. This sensor is designed for a fixed wavelength and thus was measured using monochromatic light. In these conditions, the device reaches promising MAAs of 0.6° in a ±26° FoV and 2.8° in a ±45.5° FoV for the amplitude grating and phase grating variants respectively.

The reported silicon carbide pixel array sun position sensor is furthermore exposed to elevated temperature up to 200 °C. In such environment, its raw output signals show negligible change and the sensor is well able to capture the cast light spot. The only observed difference is the change in fixed pattern noise, which is captured separately in a dark measurement at the high temperature level for signal conditioning. Integrated on-chip is the CTAT sensor, which has a linear response in the investigated temperature range when considering its single-sided output for constant voltage bias. The sensitivity is $-3.9\,\mathrm{mVK}^{-1}$ for a 9.65 V bias level.

The >10 hours in the controlled temperature chamber at 200 °C did not cause any observed degradation to the device. The thermal budget is dominated by the added glue droplets and SU-8 layer, which are cured at 140 °C and 180 °C, respectively. Lastly, measurement of the albedo sensitivity is challenging as it requires sophisticated optical

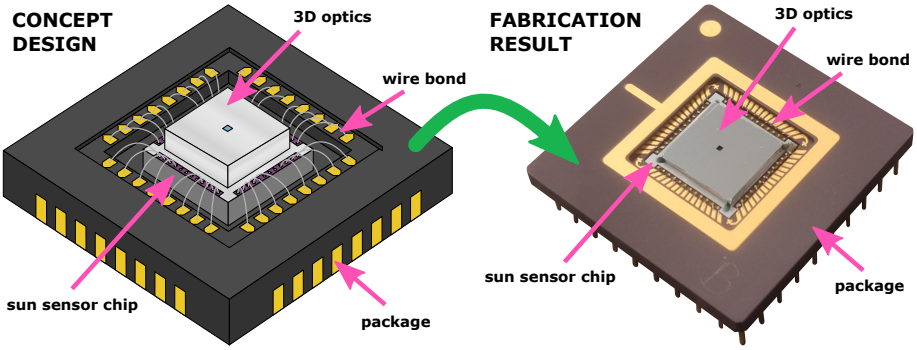


Figure 6.1: Side-by-side comparison between the conceptual design illustration and the photograph of the fabricated silicon carbide pixel array sun position sensor.

measurement setups. For this reason, a characterization comparable to in-orbit operation was not extracted in this research work, but preliminary characterization was achieved by comparing a UV-C light source and artificial ambient light. The seemingly small difference in extracted albedo insensitivity extracted in Chapter 4 for the silicon and silicon carbide devices, translates to a huge difference considering the used UV-C light source or microscope light. For the silicon carbide devices, no signal was measured for the microscope light cases. This preliminary characterization points to a solid albedo insensitivity improvement for the silicon carbide devices.

Recommendations regarding performance improvement:

- The proof-of-principle devices are packaged in bulky packages without covering the bond wires. Future work should incorporate optimized packaging solutions that follow the miniaturization trend and properly protect the electrical contacts.
- The presented silicon carbide quadrant sun position sensor devices should be integrated with on-chip readout electronics, such as transimpedance amplifiers.
- The pixel array sun position sensor device would be improved by higher overlay accuracy of its aperture, larger amount of pixels, an aperture larger than the pixel dimension and by increased resolution of the on-chip ADC.
- The technology would benefit from on-chip biasing structures for the amplifier stages and CTAT temperature sensor, reducing the off-chip electrical connections.
- The temperature range of the fabricated device could be explored further by exposure to >200 °C and temperature cycling tests.
- The sun position sensor based on the diffraction grating architecture is promising for its miniaturization and performance. Future work should investigate broadband light sources and integrated its course sensor for angular period detection.

A

SUPPORTING INFORMATION CHAPTER 2

The equations below represent the derivation of the quadrant sun position sensor sensitivity. The procedure is given for a single angle, but is identical for the second angle. Starting from Equation 2.2:

$$\angle\theta = \sin^{-1}\left(\frac{n_2}{n_1}\sin\left(\tan^{-1}\left(\frac{\Delta x}{h}\right)\right)\right) \tag{A.1}$$

This is then solved for Δx:

$$\Delta x = h\tan\left(\sin^{-1}\left(\frac{n_1}{n_2}\sin\left(\angle\theta\right)\right)\right) \tag{A.2}$$

To find the sensitivity, the partial derivative to $\angle\theta$ is taken of Δx:

$$S_{\angle\theta} = \frac{\partial}{\partial\angle\theta}\left(h\tan\left(\sin^{-1}\left(\frac{n_1}{n_2}\sin\left(\angle\theta\right)\right)\right)\right) \tag{A.3}$$

The chain rule $h(x) = f\left(g\left(x\right)\right) \rightarrow h'(x) = f'\left(g\left(x\right)\right)g'\left(x\right)$ and identity $\frac{\partial}{\partial x}\tan\left(x\right) = \sec^2\left(x\right)$ are applied:

$$S_{\angle\theta} = h\sec^2\left(\sin^{-1}\left(\frac{n_1}{n_2}\sin\left(\angle\theta\right)\right)\right)\frac{\partial}{\partial\angle\theta}\left(\sin^{-1}\left(\frac{n_1}{n_2}\sin\left(\angle\theta\right)\right)\right) \tag{A.4}$$

The identity $\sec^2\left(\sin^{-1}\left(x\right)\right) = \frac{1}{(1+x)(1-x)}$ is applied:

$$S_{\angle\theta} = \frac{h}{\left(1+\frac{n_1}{n_2}\sin\left(\angle\theta\right)\right)\left(1-\frac{n_1}{n_2}\sin\left(\angle\theta\right)\right)}\frac{\partial}{\partial\angle\theta}\left(\sin^{-1}\left(\frac{n_1}{n_2}\sin\left(\angle\theta\right)\right)\right) \tag{A.5}$$

The chain rule $h(x) = f\left(g\left(x\right)\right) \rightarrow h'(x) = f'\left(g\left(x\right)\right)g'\left(x\right)$ and identity $\frac{\partial}{\partial x}\sin^{-1}\left(x\right) = \frac{1}{\sqrt{1-x^2}}$ are applied:

A

$$S_{\angle\theta} = \frac{h}{\left(1+\frac{n_1}{n_2}\sin(\angle\theta)\right)\left(1-\frac{n_1}{n_2}\sin(\angle\theta)\right)} \frac{1}{\sqrt{1-\left(\frac{n_1}{n_2}\sin(\angle\theta)\right)^2}} \frac{\partial}{\partial\angle\theta}\left(\frac{n_1}{n_2}\sin(\angle\theta)\right) \tag{A.6}$$

Finally, this is simplified to:

$$S_{\angle\theta} = \frac{h n_1 n_2^2 \cos(\angle\theta)}{\left(n_2^2 - n_1^2\sin^2(\angle\theta)\right)\sqrt{n_2^2 - n_1^2\sin^2(\angle\theta)}} \tag{A.7}$$

Following the steps above, the similar $S_{\angle\varphi}$ is obtained.

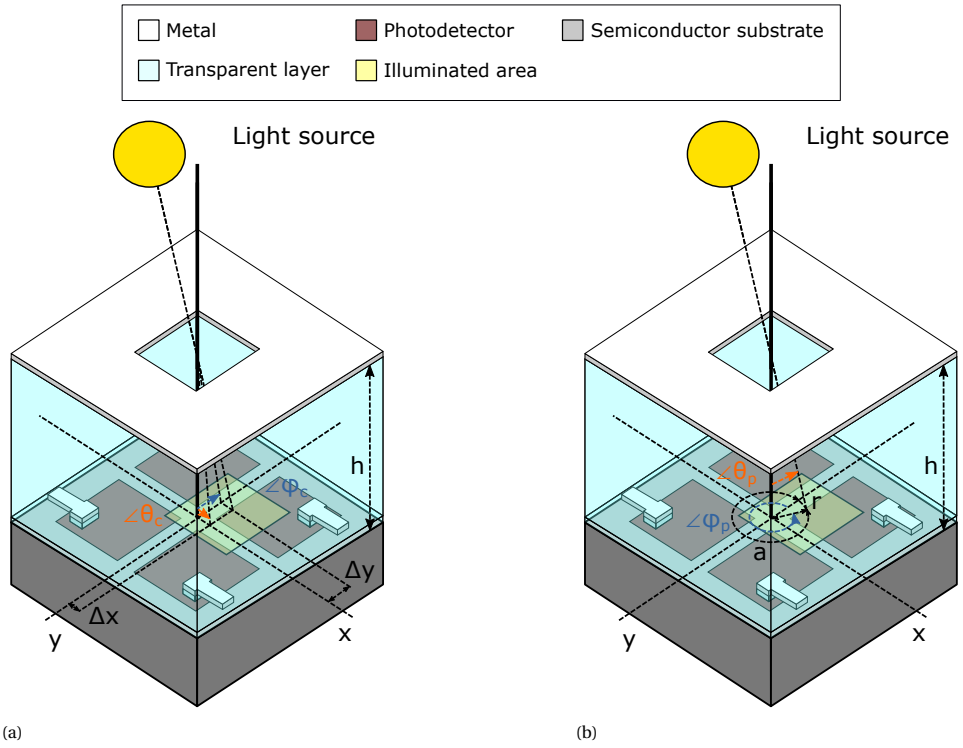
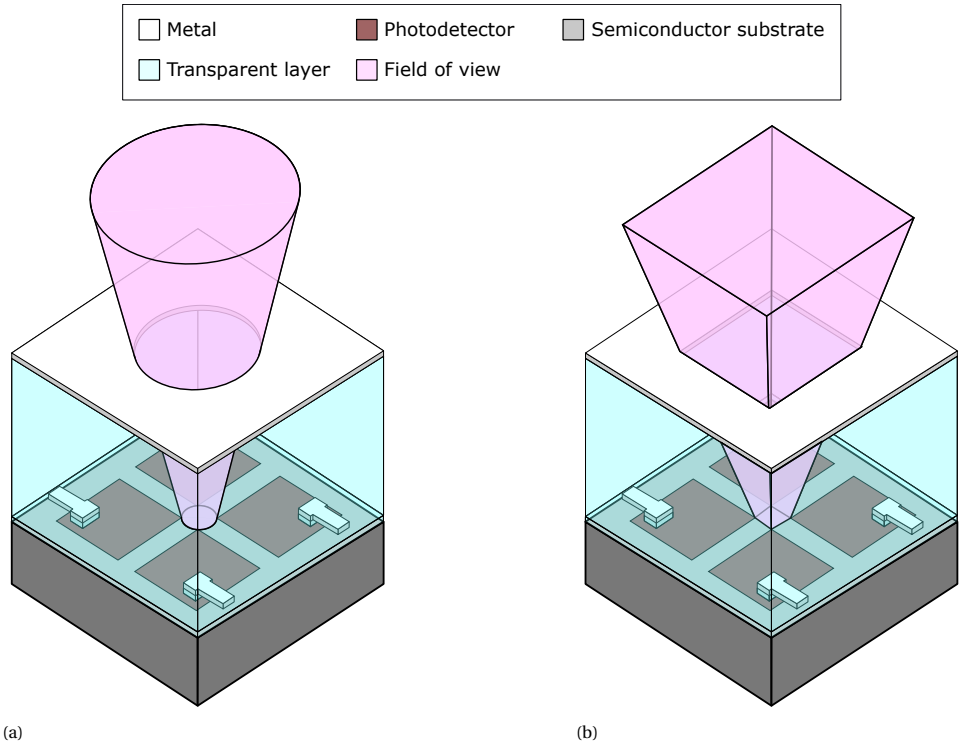


Figure A.1: Schematic illustration of the a) cartesian and b) polar coordinate systems, using the quadrant sun position sensor as an example. The annotations mark the optical window thickness h, the x-axis, the y-axis, the lateral displacement in x direction Δx, the lateral displacement in y-direction Δy, the angle $\angle\theta_c$ over the y-axis caused by Δx, the angle $\angle\varphi_c$ over the x-axis caused by Δy, the absolute lateral displacement r, the circular arc a, the elevation $\angle\theta_p$ caused by r and the azimuth $\angle\varphi_p$ caused by a.

The equations below describe the direction vector angles of the cartesian (Figure A.1a and Equation A.8) and polar (Figure A.1b and Equation A.9) systems respectively.

$$\angle\theta_c = \tan^{-1}\left(\frac{\Delta x}{h}\right) \quad \text{and} \quad \angle\varphi_c = \tan^{-1}\left(\frac{\Delta y}{h}\right), \tag{A.8}$$

$$\angle\theta_p = \frac{a}{r} \quad \text{and} \quad \angle\varphi_p = \tan^{-1}\left(\frac{r}{h}\right), \tag{A.9}$$



(a) (b)

Figure A.2: Schematic illustrations of a) circular aperture with a symmetrical FoV and b) square aperture with an asymmetrical FoV, in the collimating sun position sensor type.

B

SUPPORTING INFORMATION CHAPTER 3

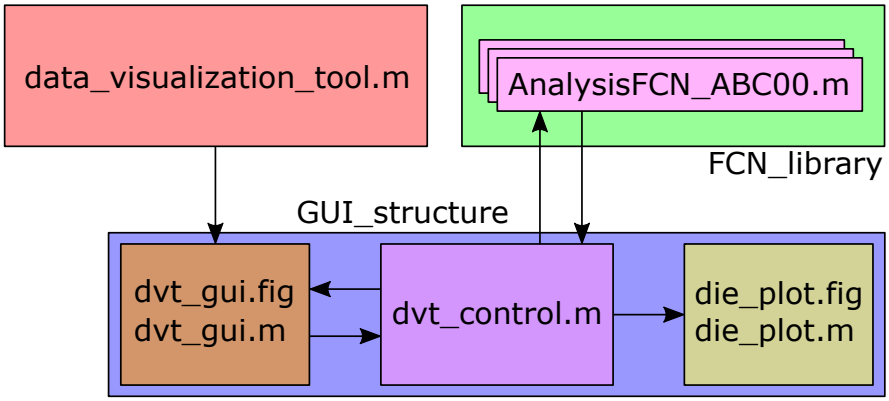


Figure B.1: Overview of the DVT GUI structure, taking the individual MATLAB files as functional blocks. The tool is started by running *data_visualization_tool.m*, which calls on *dvt_gui.m* to initialize the wafermap figure stored in *dvt_gui.fig*. When the user interacts with the GUI, it will trigger updates that are controlled by *dvt_control.m*. The device specific analysis is defined by the user in a library of functions that are identified by a tag ('ABC00' in the example). Finally, analysis on single die level is handled by *die_plot.m*.

B

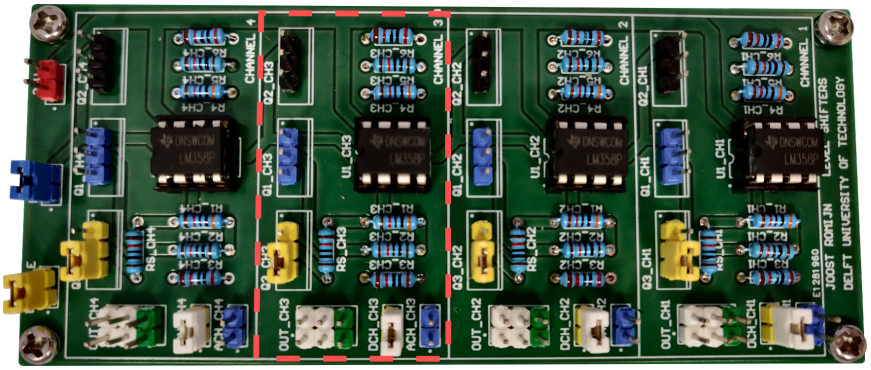


Figure B.2: Picture of the level-shifter PCB with an overlay that identifies one of the four level-shifter channels. Each channel consists of both analog 5-to-10 V and 10-to-5 V level-shifters in the current configuration. By adding the blue and black jumpers in the same configuration as the yellow jumpers, the level-shifters are configured to 5-to-20 V and 20-to-5 V.

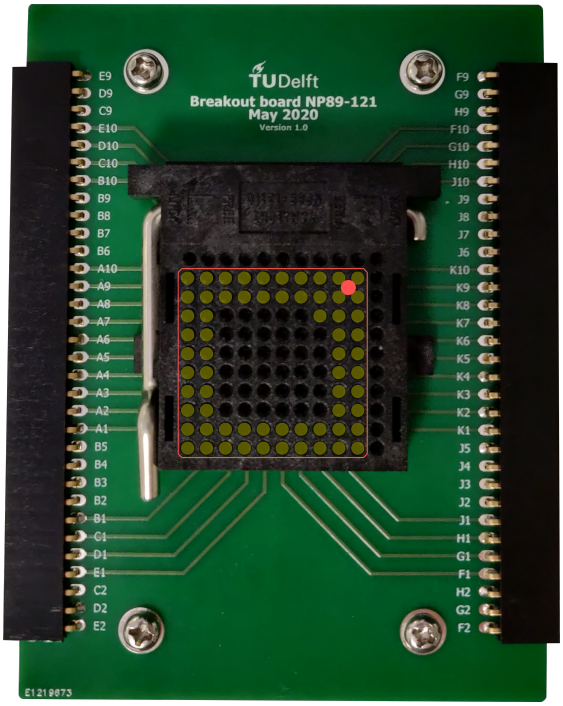


Figure B.3: Picture of the interface PCB for connection to the PGA64 package with an overlay of the package outline and identifier dot (red) and output pins (yellow). The package pin-out labels are annotated on the two pinheaders. Note that the ZIF socket allows a 11 × 11 pin array, while the used package has an 10x10 pin array, which requires a bottom-left alignment.

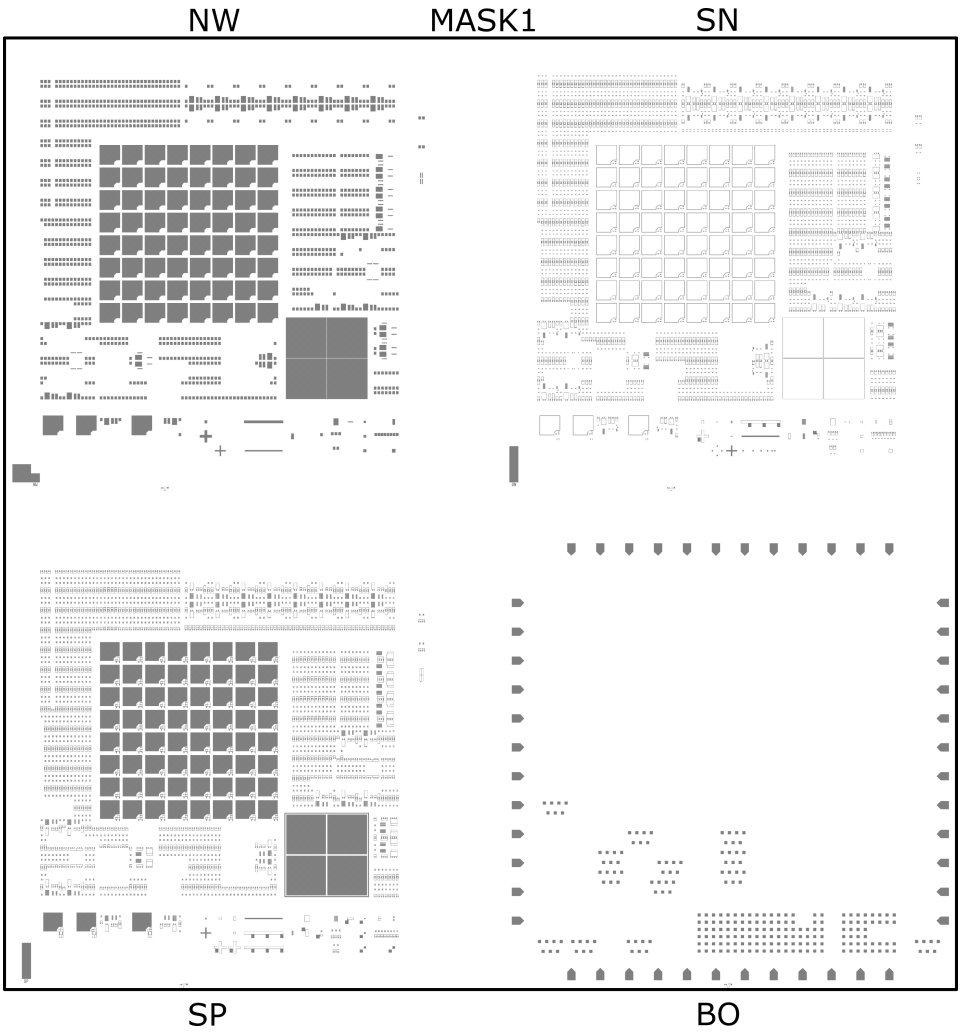


Figure B.4: Organization of the stepper mask 1 used for the silicon CMOS chip design, including the NW, SN, SP and BO layers. The reticles have 2x2 images each and the individual design layers are annotated. Note that the actual reticles also include additional markers that are used for handling in the ASML wafer stepper.

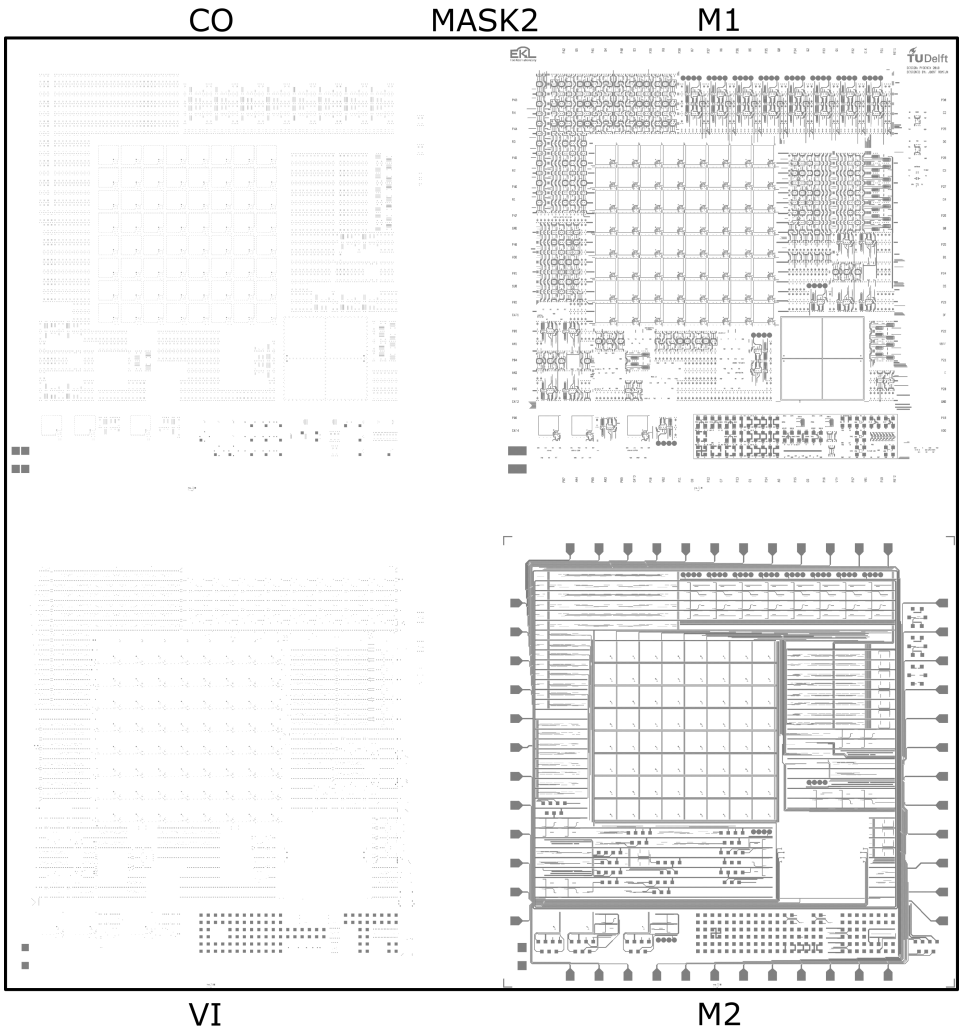


Figure B.5: Organization of the stepper mask 2 used for the silicon CMOS chip design, including the CO, M1, VI and M2 layers. The reticles have 2x2 images each and the individual design layers are annotated. Note that the actual reticles also include additional markers that are used for handling in the ASML wafer stepper.

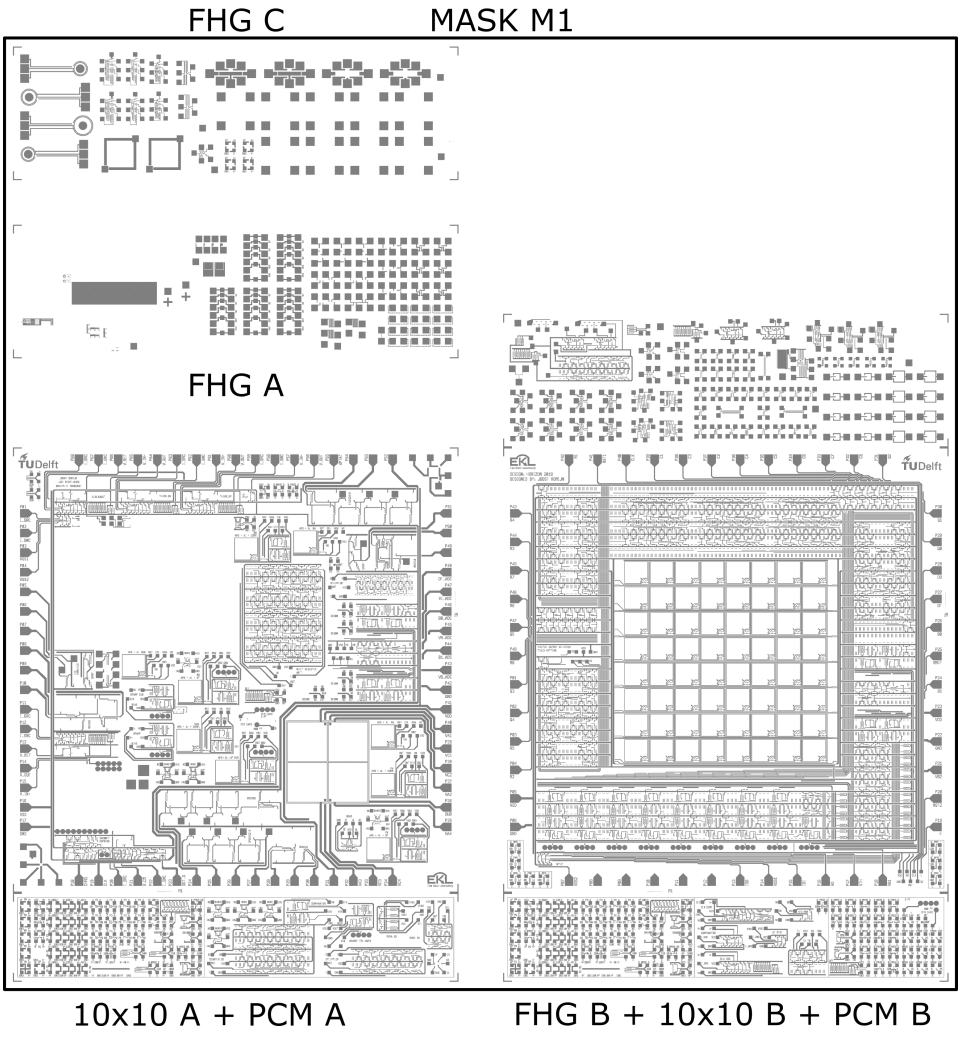


Figure B.6: Organization of the stepper mask M1 used for the silicon carbide CMOS chip design, including the 7 unique chips in the multi-project design. The multi-project chip is too large to fit regularly on the mask, which is reason for cutting it in pieces that are stitched together by the stepper. Note that the actual reticles also include additional markers that are used for handling in the ASML wafer stepper.

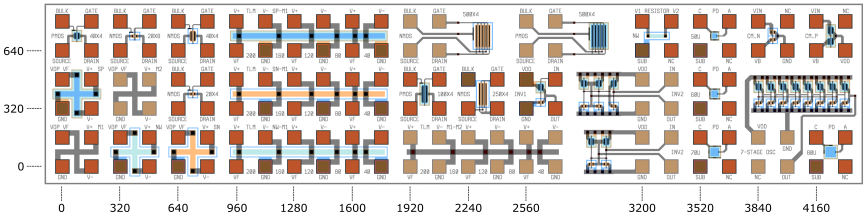


Figure B.7: Organization of the 4-probe PCM in the silicon CMOS chip (BICMOS7). The coordinates of the bottom left pad of each structure are annotated in microns.

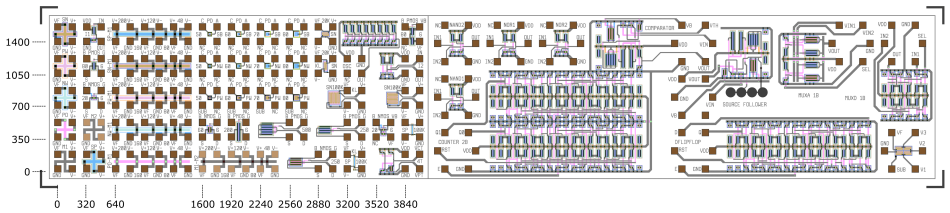


Figure B.8: Organization of PCM A in the silicon carbide CMOS chip (SICCMOS9), containing both 4-probe and 6-probe structures. The coordinates of the bottom left pad of each 4-probe structure on the left side are annotated in microns.

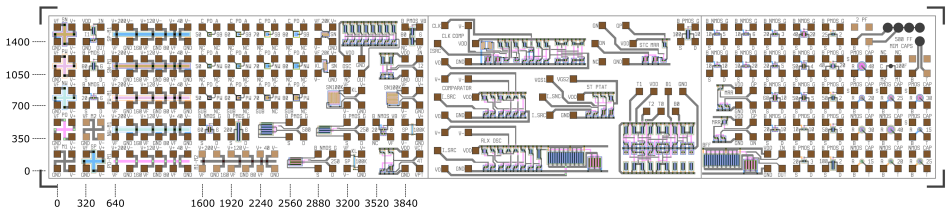


Figure B.9: Organization of PCM B in the silicon carbide CMOS chip (SICCMOS9), containing both 4-probe and 6-probe structures. The coordinates of the bottom left pad of each 4-probe structure on the left side are annotated in microns.

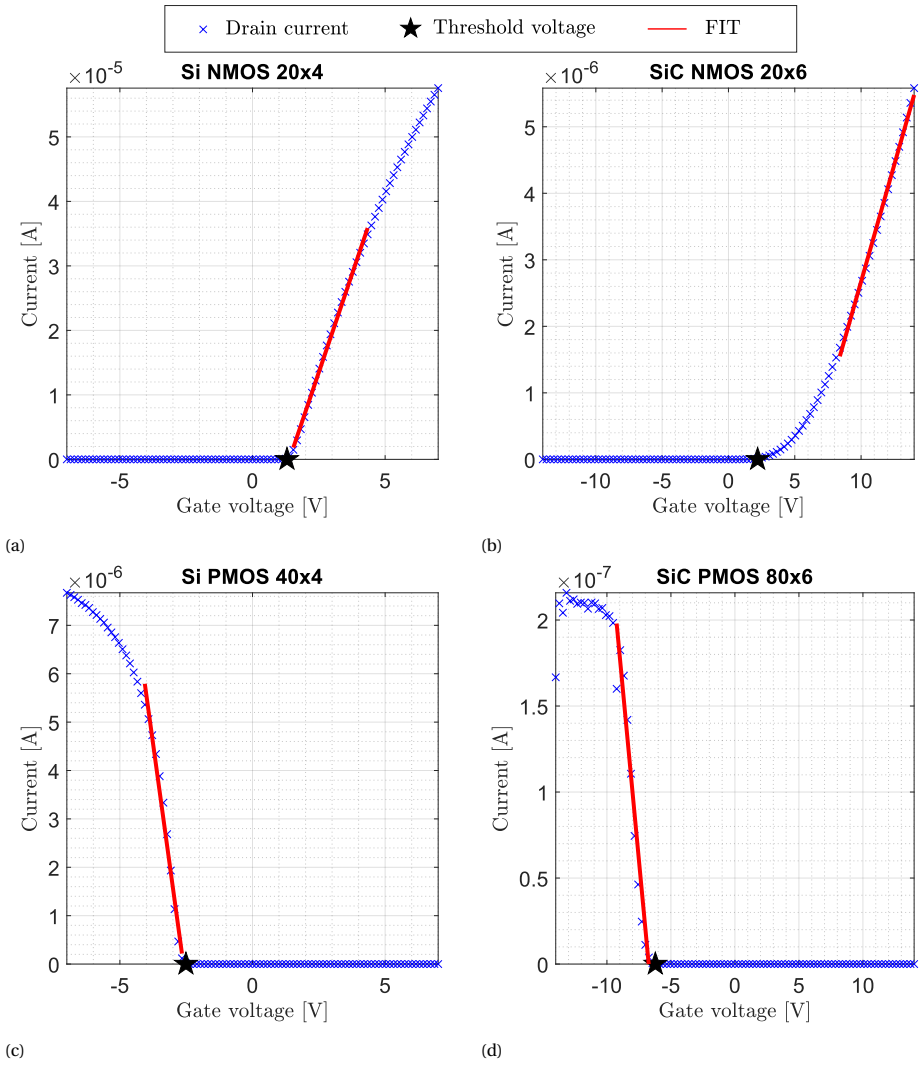


Figure B.10: I_{ds}/V_{gs} curves of the a) $20 \times 4\,\mu$m Si NMOS, b) $20 \times 6\,\mu$m SiC NMOS, $40 \times 4\,\mu$m Si PMOS and $80 \times 6\,\mu$m SiC PMOS devices. A linear fit is made on the linear part of the curves for $|V_{gs}| > |V_{th}|$ over 20 or 10 data points for the NMOS and PMOS respectively. The slope of the found fits is used to calculate the carrier mobility of the devices.

C

Supporting Information Chapter 4

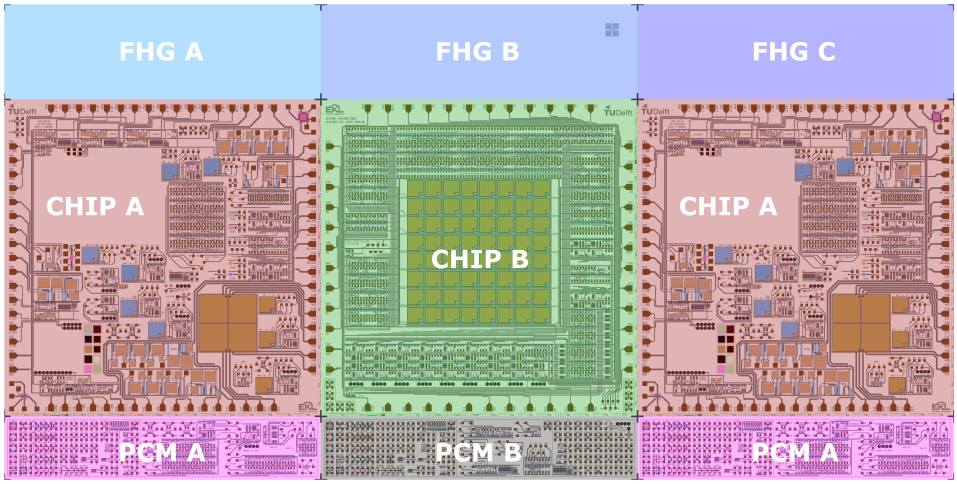


Figure C.1: Organization of the multi-project chip using a 12-layer layout design in 4H-SiC on a 15×30 mm chip. Chip A contains various smaller test structures, chip B houses the complete pixel array sensor system, PCM A and B consist of many smaller structures and devices for wafer-level measurement. The reserved FHG A, B and C chips are filled by Fraunhofer IISB (not shown in favor of confidentiality). The additional three design layers on top of SICCMOS9 are vias (VI), second metal layer (M2) and bondpad openings (BO).

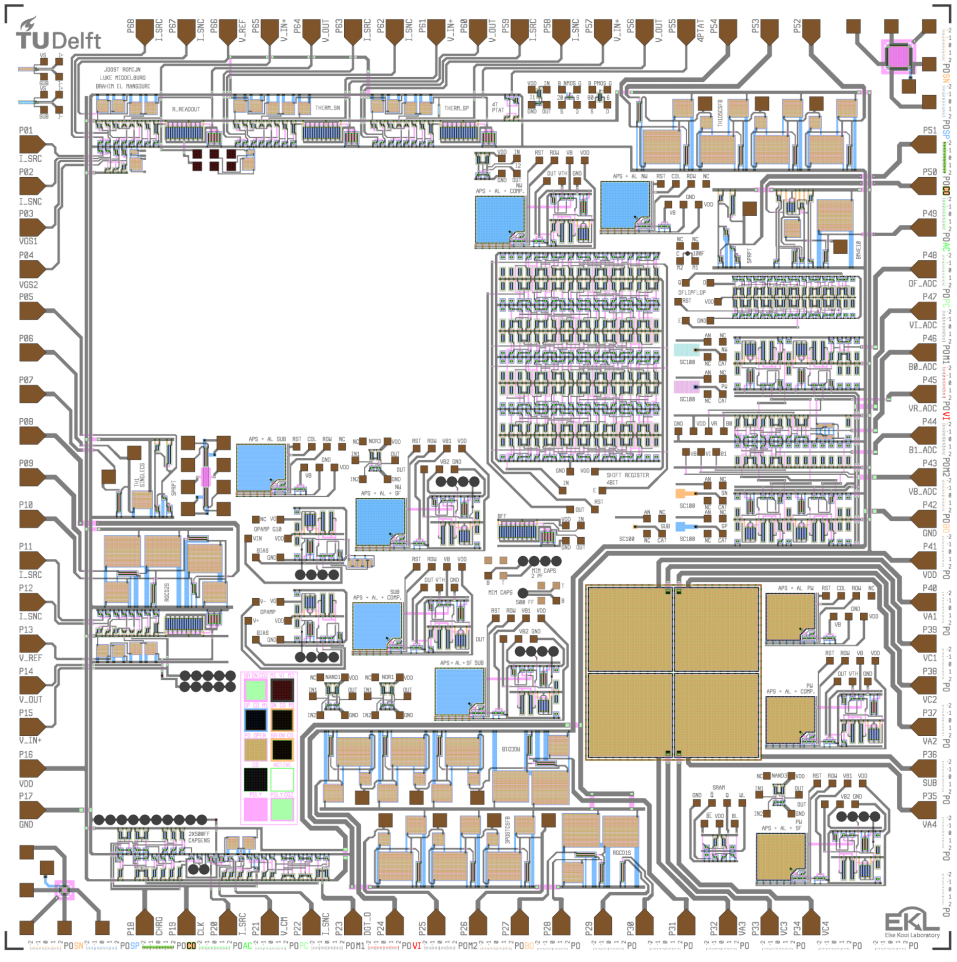


Figure C.2: Complete 12-layer layout of the multi-project design, including single pixel measurement structures, a 4-bit shift register, a 2-bit ADC and the quadrant sun position sensor, in 4H-SiC on a 10 × 10 mm chip. The additional three design layers on top of SICCMOS9 are vias (VI), second metal layer (M2) and bondpad openings (BO).

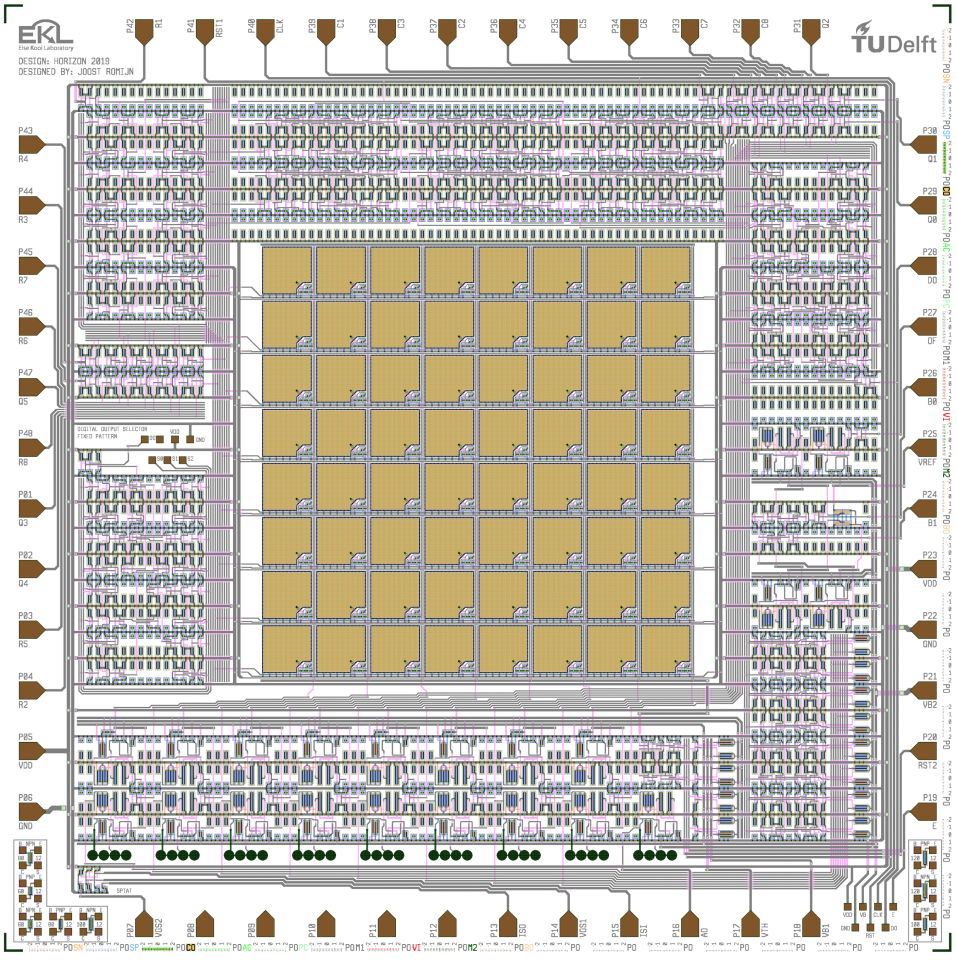


Figure C.3: Complete 12-layer layout design of the 64 pixel array sensor with integrated readout electronics in 4H-SiC on a 10 × 10 mm chip. The additional three design layers on top of SICCMOS9 are vias (VI), second metal layer (M2) and bondpad openings (BO).

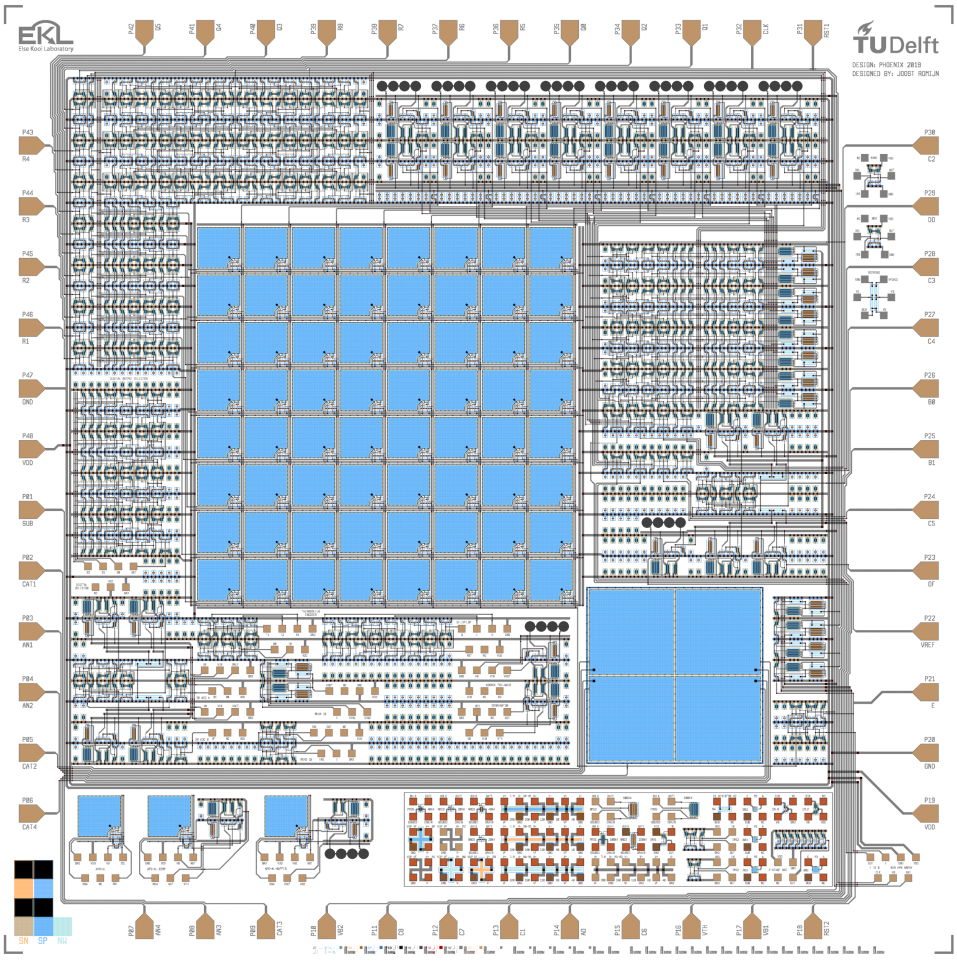


Figure C.4: Complete 8-layer layout design of the 64 pixel array sensor with integrated readout electronics in Si on a 10 × 10 mm chip. The additional design layer on top of BICMOS7 is the bondpad openings (BO).

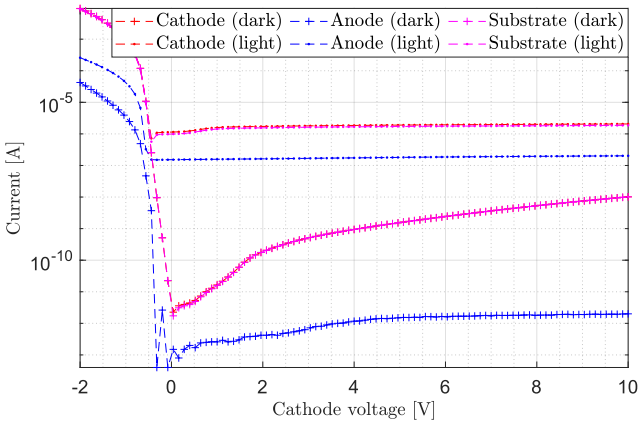


Figure C.5: The measured currents for different cathode biasing on die (0,0) of the vertical Si photodiode 80 × 80 µm implementation in the n-well (NW). The anode and substrate are biased at 0 V.

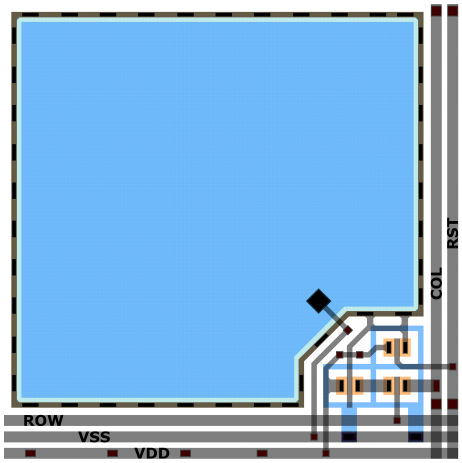


Figure C.6: Layout design in BICMOS7 of the text book (using NW) 3T APS architectures. The depicted blocks are 0.50 × 0.50 mm, which already accounts for some clearance when implementing in an array.

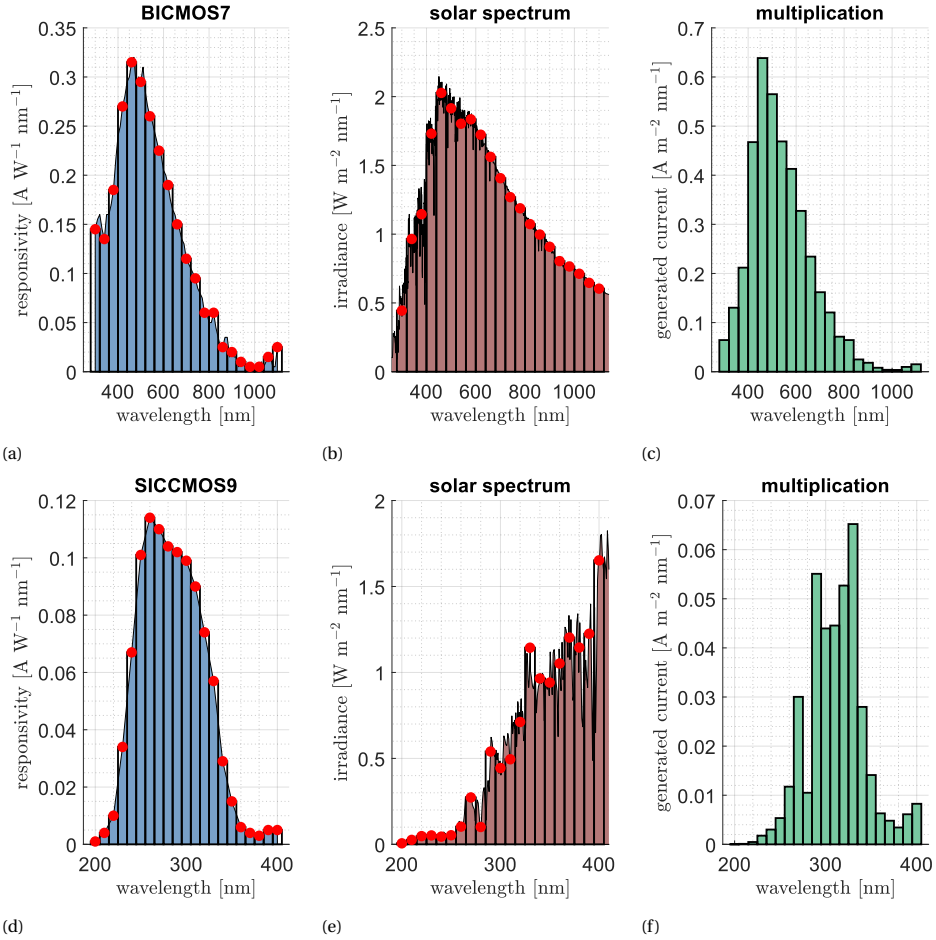


Figure C.7: Radiometry estimation of the generated photo current of photodiodes in the BICMOS7 and SICCMOS9 technologies, by using the strategy in Section 2.4.1. Including the BICMOS7 a) responsivity, b) solar range and c) generated current and the SICCMOS9 d) responsivity, e) solar range and f) generated current.

Table C.1: Connection diagram for silicon carbide chips, design A (only quadrant sensor and 2-bit ADC). The PAD columns identify the package wire bond pads (outer ring in Figure C.8), the PIN columns correspond to the package pin-out (used on the interface PCB in Figure B.3) and the NAME columns are the wire bonded chip pins/signals. Pads that are not wire bonded to are marked by an 'X'.

PAD	PIN	NAME	PAD	PIN	NAME	PAD	PIN	NAME	PAD	PIN	NAME
1	F1	X	17	J6	X	33	E10	P43/VB_ADC	49	B5	X
2	F2	X	18	K6	X	34	E9	P44/B1_ADC	50	A5	X
3	G1	X	19	K7	X	35	D10	P45/VR_ADC	51	A4	X
4	G2	X	20	J7	X	36	D9	P46/B0_ADC	52	B4	X
5	H1	X	21	J8	X	37	C10	P47/VI_ADC	53	B3	X
6	H2	X	22	K8	P32/VA3	38	C9	P48/OF_ADC	54	A3	X
7	J1	X	23	K9	P33/VC3	39	B10	X	55	A2	X
8	J2	X	24	K10	P34/VC4	40	B9	X	56	A1	X
9	K1	X	25	J9	P35/VA4	41	A10	X	57	B2	X
10	J3	X	26	J10	P36/SUB	42	B8	X	58	B1	X
11	K2	X	27	H9	P37/VA2	43	A9	X	59	C2,C3	X
12	K3	X	28	H10	P38/VC2	44	A8	X	60	C1	X
13	J4	X	29	G9	P39/VC1	45	B7	X	61	D2	X
14	K4	X	30	G10	P40/VA1	46	A7	X	62	D1	X
15	K5	X	31	F10	P41/VDD	47	A6	X	63	E1	X
16	J5	X	32	F9	P42/GND	48	B6	X	64	E2	X

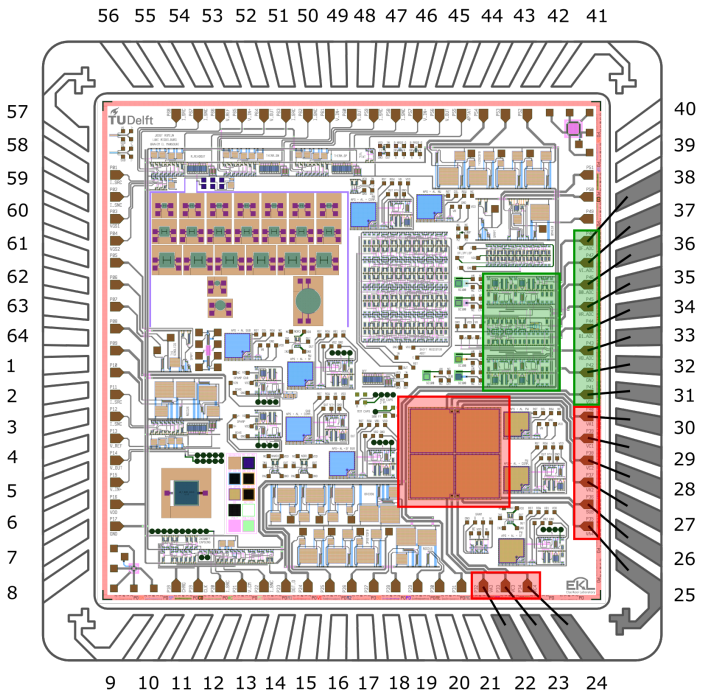


Figure C.8: Connection scheme of the wire bonds from the PGA64 package to the silicon carbide chip, design A (only quadrant sensor and 2-bit ADC). Not all package bond pads are utilized, which is highlighted by marking used pads in dark grey. The connection diagram of all signals is listed in Table C.1.

Table C.2: Connection diagram for silicon chips. The PAD columns identify the package wire bond pads (outer ring in Figure C.9), the PIN columns correspond to the package pin-out (used on the interface PCB in Figure B.3) and the NAME columns are the wire bonded chip pins/signals. Pads that are not wire bonded to are marked by an 'X'.

PAD	PIN	NAME	PAD	PIN	NAME	PAD	PIN	NAME	PAD	PIN	NAME
1	F1	P01/SUB	17	J6	P13/C1	33	E10	P25/B1	49	B5	P37/R6
2	F2	X	18	K6	X	34	E9	X	50	A5	X
3	G1	P02/CAT1	19	K7	P14/AO	35	D10	P26/B0	51	A4	P38/R7
4	G2	P03/AN1	20	J7	P15/C6	36	D9	P27/C4	52	B4	P39/R8
5	H1	P04/AN2	21	J8	P16/VTH	37	C10	P28/C3	53	B3	P40/Q3
6	H2	X	22	K8	X	38	C9	X	54	A3	X
7	J1	P05/CAT2	23	K9	P17/VB1	39	B10	P29/DO	55	A2	P41/Q4
8	J2	P06/CAT4	24	K10	P18/RST2	40	B9	P30/C2	56	A1	P42/Q5
9	K1	P07/AN4	25	J9	P19/VDD	41	A10	P31/RST1	57	B2	P43/R4
10	J3	P08/AN3	26	J10	P20/GND	42	B8	P32/CLK	58	B1	P44/R3
11	K2	X	27	H9	X	43	A9	X	59	C2,C3	X
12	K3	P09/CAT3	28	H10	P21/E	44	A8	P33/Q1	60	C1	P45/R2
13	J4	P10/VB2	29	G9	P22/VREF	45	B7	P34/Q2	61	D2	P46/R1
14	K4	P11/C8	30	G10	P23/OF	46	A7	P35/Q0	62	D1	P47/GND
15	K5	X	31	F10	X	47	A6	X	63	E1	X
16	J5	P12/C7	32	F9	P24/C5	48	B6	P36/R5	64	E2	P48/VDD

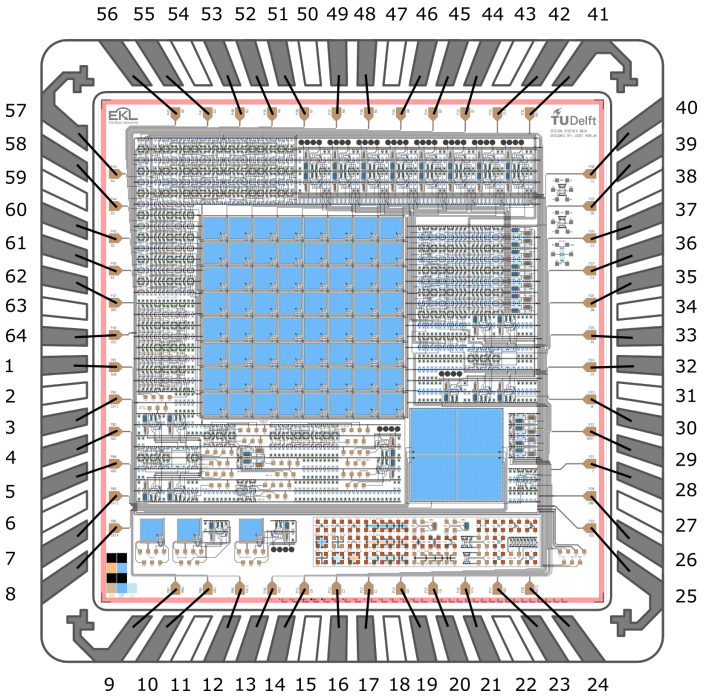


Figure C.9: Connection scheme of the wire bonds from the PGA64 package to the silicon chip. Not all package bond pads are utilized, which is highlighted by marking used pads in dark grey. The connection diagram of all signals is listed in Table C.2.

Table C.3: Connection diagram for silicon carbide chips, design B. The PAD columns identify the package wire bond pads (outer ring in Figure C.10), the PIN columns correspond to the package pin-out (used on the interface PCB in Figure B.3) and the NAME columns are the wire bonded chip pins/signals. Pads that are not wire bonded to are marked by an 'X'.

PAD	PIN	NAME	PAD	PIN	NAME	PAD	PIN	NAME	PAD	PIN	NAME
1	F1	P37/C2	17	J6	P01/Q3	33	E10	P13/ISO	49	B5	P25/VREF
2	F2	X	18	K6	X	34	E9	X	50	A5	X
3	G1	P38/C3	19	K7	P02/Q4	35	D10	P14/VGS1	51	A4	P26/B0
4	G2	P39/C1	20	J7	P03/R5	36	D9	P15/ISI	52	B4	P27/OF
5	H1	P40/CLK	21	J8	P04/R2	37	C10	P16/AO	53	B3	P28/DO
6	H2	X	22	K8	X	38	C9	X	54	A3	X
7	J1	P41/RST1	23	K9	P05/VDD	39	B10	P17/VTH	55	A2	P29/Q0
8	J2	P42/R1	24	K10	P06/GND	40	B9	P18/VB1	56	A1	P30/Q1
9	K1	P43/R4	25	J9	P07/VGS2	41	A10	P19/E	57	B2	P31/Q2
10	J3	P44/R3	26	J10	P08/-	42	B8	P20/RST2	58	B1	P32/C8
11	K2	X	27	H9	X	43	A9	X	59	C2,C3	X
12	K3	P45/R7	28	H10	P09/-	44	A8	P21/VB2	60	C1	P33/C7
13	J4	P46/R6	29	G9	P10/-	45	B7	P22/GND	61	D2	P34/C6
14	K4	P47/Q5	30	G10	P11/-	46	A7	P23/VDD	62	D1	P35/C5
15	K5	X	31	F10	X	47	A6	X	63	E1	X
16	J5	P48/R8	32	F9	P12/-	48	B6	P24/B1	64	E2	P36/C4

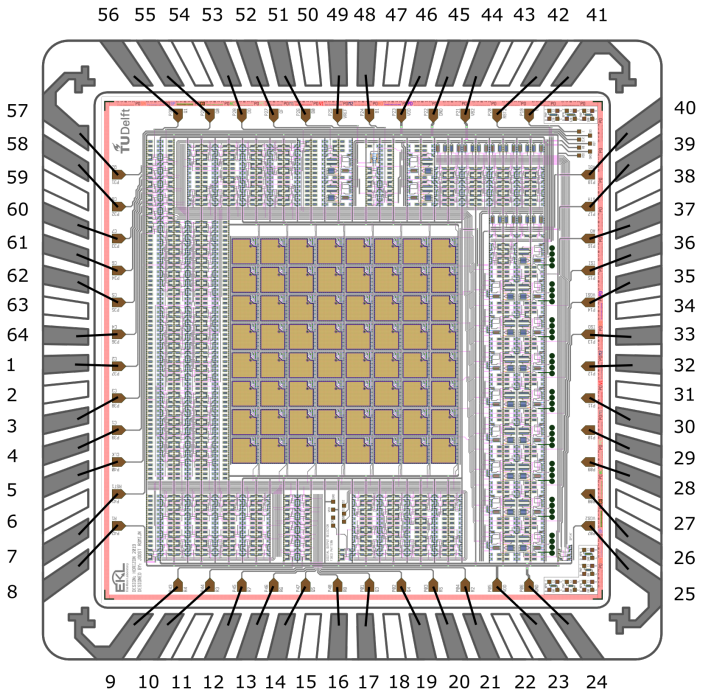
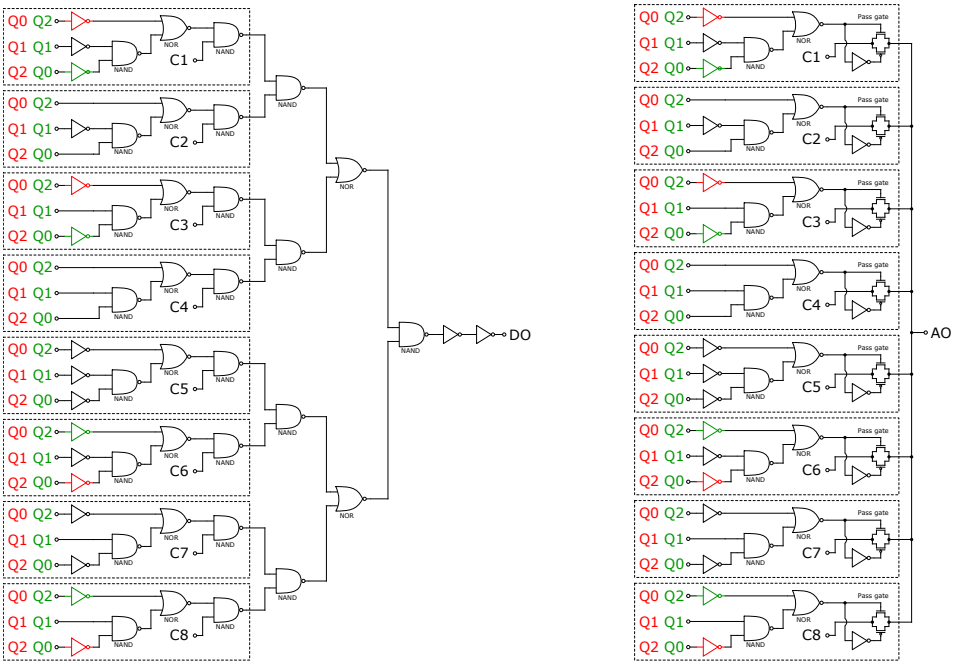
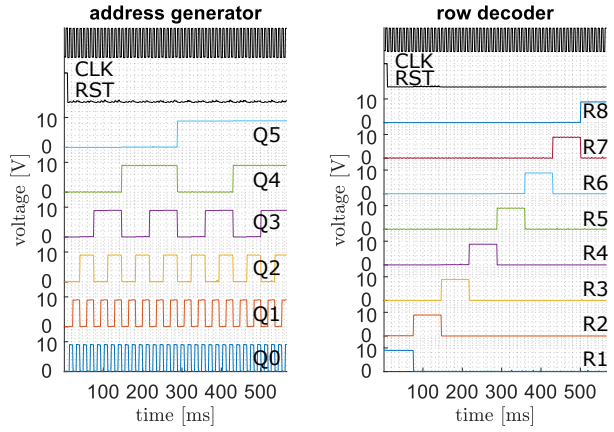


Figure C.10: Connection scheme of the wire bonds from the PGA64 package to the silicon carbide chip, design B. Not all package bond pads are utilized, which is highlighted by marking used pads in dark grey. The connection diagram of all signals is listed in Table C.3.



(a) (b)

Figure C.11: Circuit design of the a) digital and b) analog column decoders. The BICMOS7 design contains connection errors, indicated here by faulty connections in red and correct connections in green.



(a) (b)

Figure C.12: The measured response of the a) 6-bit address generator and b) row decoder in BICMOS7 on die (1,0). The 10-pin address generator and 12-pin row decoder could only be measured on chip-level after packaging due to the increased amount of pins.

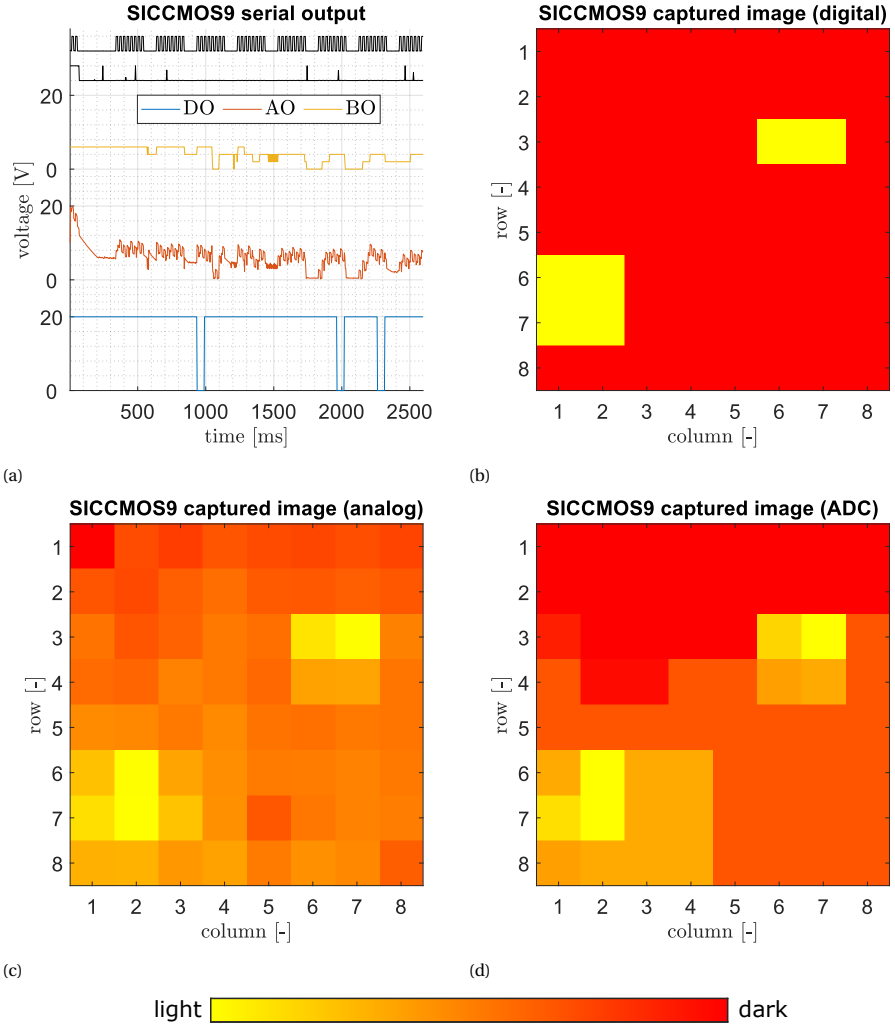


Figure C.13: Light spot emulation measurement on the SICCMOS9 chip including two light spots (variation 1). The image sensor a) serial outputs, operated by an asynchronous CLK and biased at 1.5 V. The serial outputs are transformed to 2D images for the b) digital, c) analog and d) 2-bit ADC output streams.

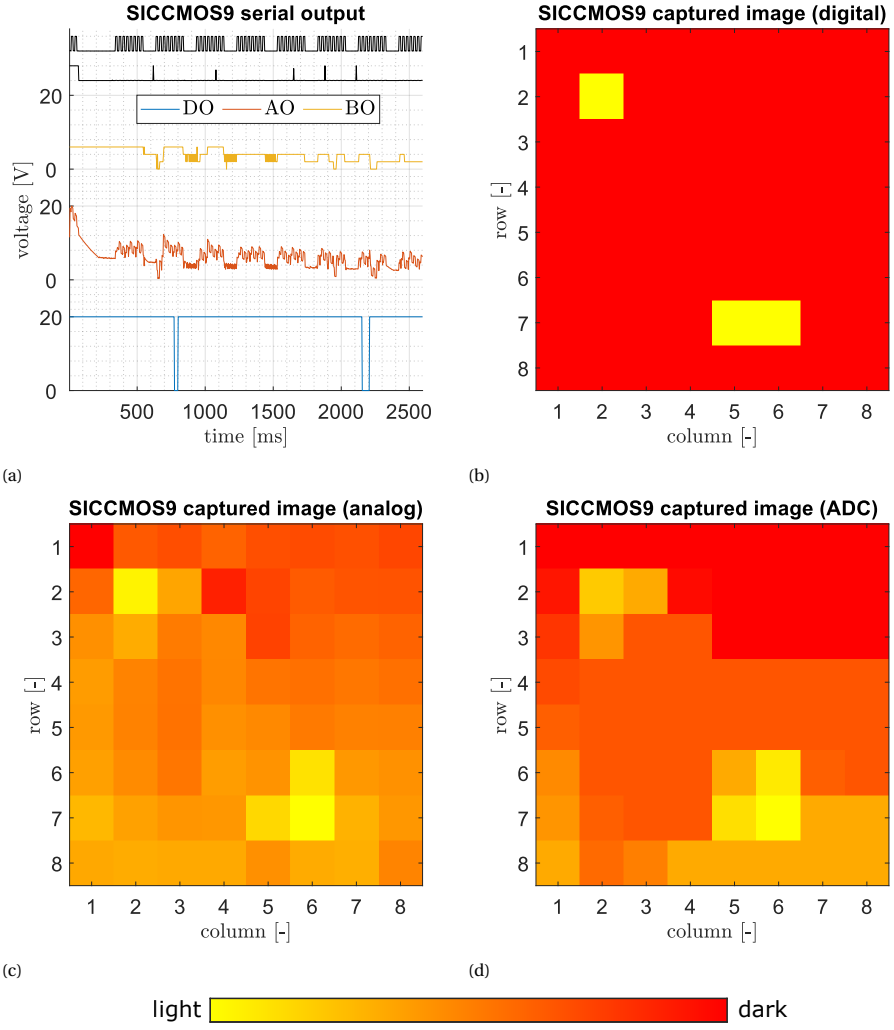


Figure C.14: Light spot emulation measurement on the SICCMOS9 chip including two light spots (variation 2). The image sensor a) serial outputs, operated by an asynchronous CLK and biased at 1.5 V. The serial outputs are transformed to 2D images for the b) digital, c) analog and d) 2-bit ADC output streams.

D

Supporting Information Chapter 5

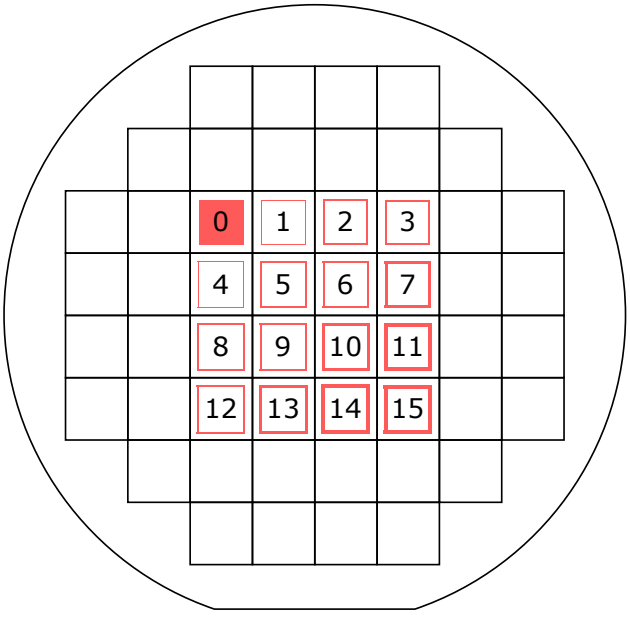
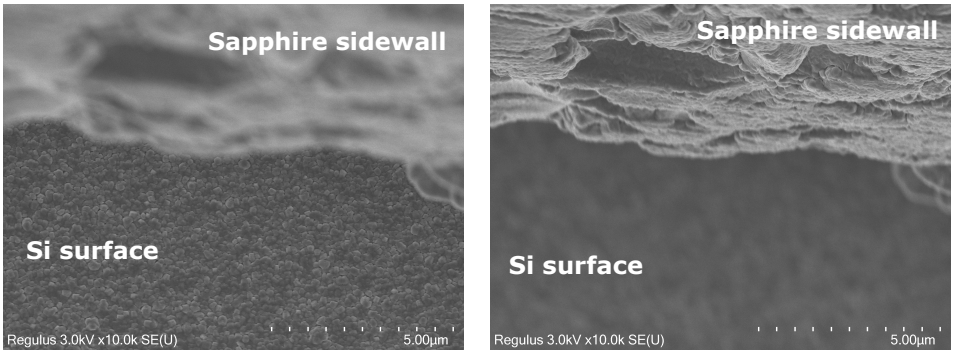


Figure D.1: Overview of the adhesive pattern design set, with the set of 16 different SU-8 adhesive patterns in red with variation in trace width w and clearance to the optical window edge d. The complete four inch wafer is depicted, housing 52 10 × 10 mm dies.



(a) (b)

Figure D.2: SEM images of the sputter coated Al coverage on a) the silicon front side surface and b) the sapphire sidewall. The substrate surface is notably flat, whereas the optical window is not due to the dicing process. Still, the morphology of the light mask layer is similar. This was further verified by optical inspection under a microscope.

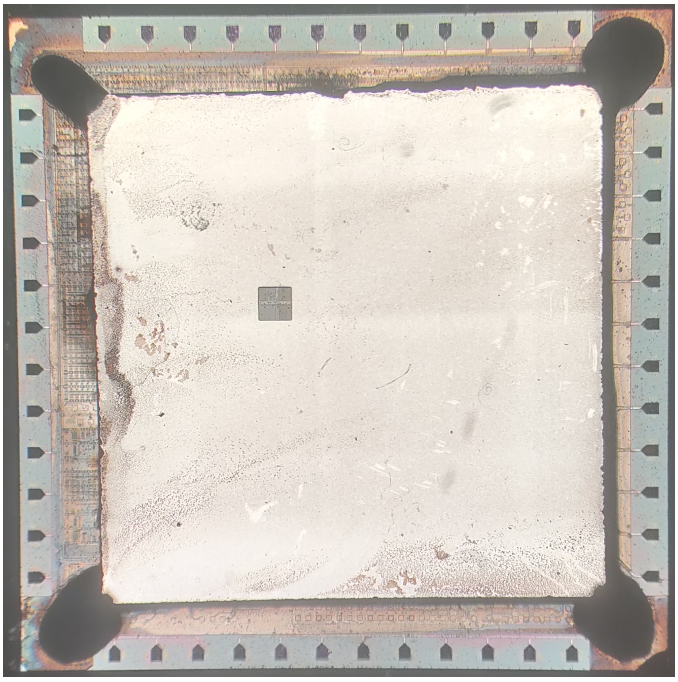
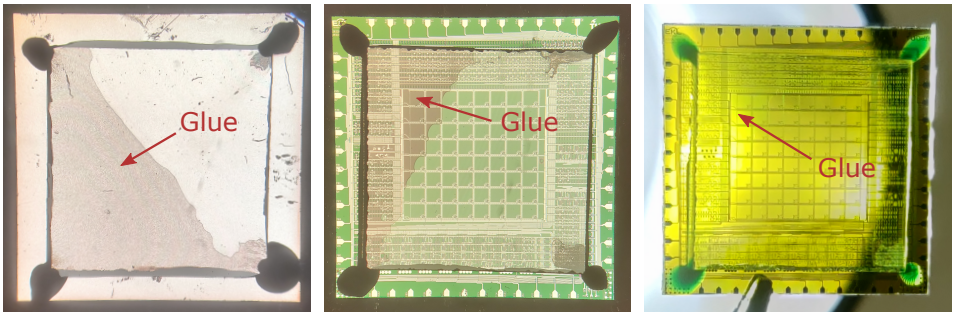


Figure D.3: Overview micro photograph of the silicon device chip with integrated 3D optics by means of the reported wafer-level fabrication, including the additional glue at the optical window corners. Note that the used glue dispense nozzle was larger on this chip, which resulted in larger glue areas. It is furthermore observed that the bondpads are black instead of white metallic, which is caused by major surface roughing and silicon haze as a result of the light mask wet etch that landed directly on the AlSi(1 %) interconnect of BICMOS7.



(a) (b) (c)

Figure D.4: Test samples that illustrate the glue in the optical window and substrate interface, including a) bare silicon and b) silicon carbide device chip. In the visible light spectral range, the silicon carbide, SU-8 and sapphire stack is still highly transparent, as depicted by c) the sample picture in front of a light source.

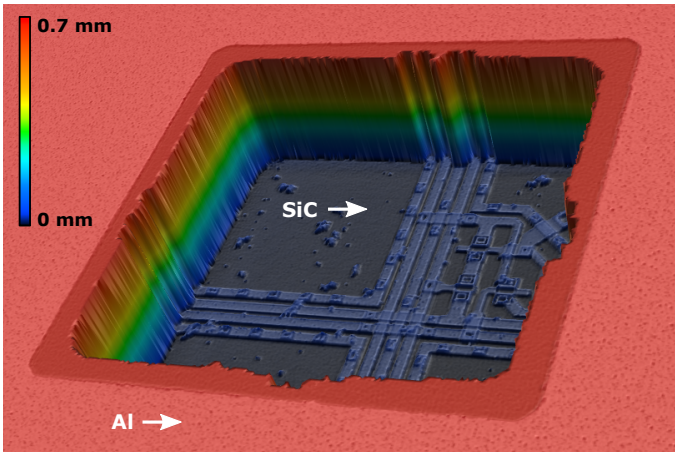


Figure D.5: The 3D capture of the device aperture, generated by a Keyence VK-X250 system. The top area is Al and the bottom plane shows pixels in the SiC substrate. The system is used to level the top and bottom planes respectively, to ensure perpendicular measurement of the extracted overlay alignment image.

It was found that the extracted angular information curve from the pixel array device deviated from the predictive model due to secondary effects, which is corrected for by a cosine multiplication (not to be confused with the cosine drop-off) as related by the equation below. Here, $\alpha = 2.5$ and $\beta = 1.3$ are fitting parameters.

$$\angle\theta = \angle\theta_{\text{raw}}\left(\cos\left(\alpha\angle\theta_{\text{raw}}\right) + \beta\right), \tag{D.1}$$

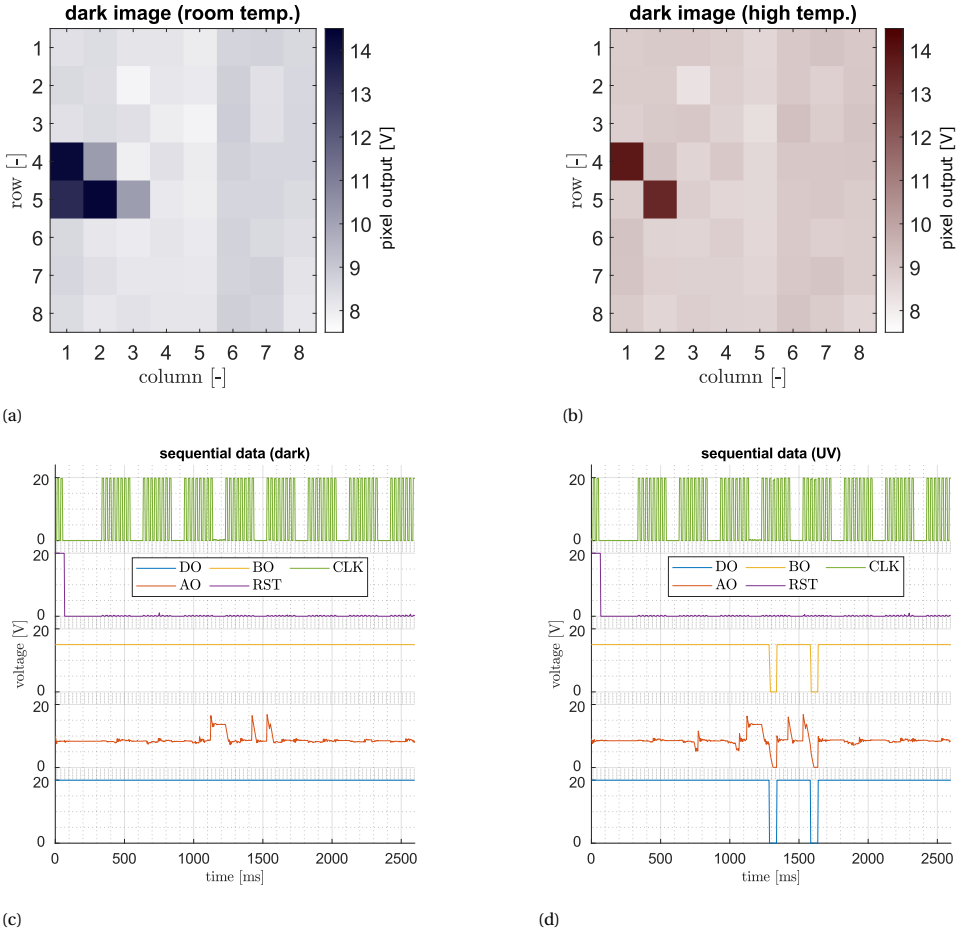


Figure D.6: Captured dark 8 × 8 images at (a) room temperature and (b) 200 °C used for fixed pattern correction. The raw sequential data (c) of the dark measurement at room temperature is used on all the raw sequential data (d) under UV exposure at room temperature, to obtain the reported conditioned data.

The equation below is used to correct the fixed pattern noise in the silicon carbide pixel array sun positon sensor device. Here, AO_{dark} is the analog output in dark condition and AO_{UV} the analog output in UV exposure condition.

$$AO = \frac{AO_{dark}}{AO_{UV}} \times 10. \tag{D.2}$$

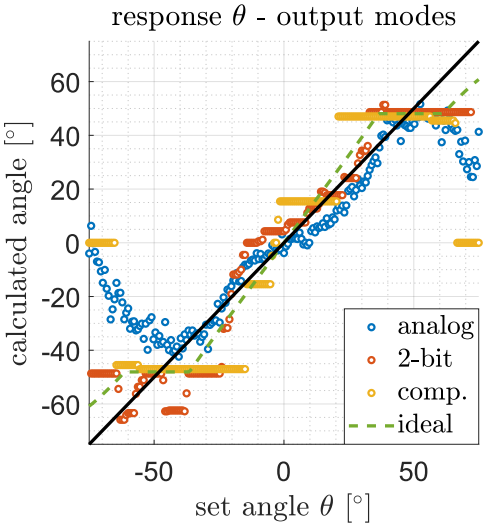


Figure D.7: Extracted angular information over a single rotation axis for all three output modes of the pixel array device, without further data processing.

E

FABRICATION FLOWCHARTS

E.1. BICMOS7

Starting material: 4 inch process wafers, p-type, boron, 1-0-0 orientation, 0° off orientation, resistivity of 2–5 Ω cm, thickness of (525 ± 15) µm, diameter of (100.0 ± 0.2) mm.

Step 1. Cleaning procedure (Si)

Step 2. Marangoni cleaning procedure (Si)

Step 3. Epitaxial layer growth

- Thickness: 2 µm
- Doping: 1×10^{16} cm^{-3} boron

Step 4. Coating and baking

- Thickness: 1.4 µm
- Photoresist: SPR3012 positive

Step 5. Alignment and exposure (ZERO LAYER)

- Energy: 120 J m^{-2}
- Focus: 0

Step 6. Development

- Developer: Shipley MF322

Step 7. Plasma etching Si

- Trikon Ωmega 201 plasma etcher

Step 8. Cleaning procedure (Si)

Step 9. Dry oxidation

- Dirt barrier formation
- Time: 35 min

Step 10. Coating and baking

- Thickness: 3.1 µm
- Photoresist: SPR3012 positive

Step 11. Alignment and exposure (NW)

- Energy: 420 J m^{-2}
- Focus: -1

Step 12. Development

- Developer: Shipley MF322

Step 13. Implantation (phosphorus)

- Ion: P^+
- Energy: 150 keV
- Dose: 6.0×10^{12} cm^{-2}

Step 14. Cleaning procedure (Si)

Step 15. Anneal

- N-well drive-in
- Time: 240 min

Step 16. Oxide wet etch

- Chemical: Buffered HF
- Etch rate: (1.3 ± 0.2) nm s^{-1}

Step 17. Cleaning procedure (Si)

Step 18. Dry oxidation
- Dirt barrier formation
- Time: 35 min

Step 19. Coating and baking
- Thickness: 1.4 µm
- Photoresist: SPR3012 positive

Step 20. Alignment and exposure (SN)
- Energy: 120 J m^{-2}
- Focus: 0

Step 21. Development
- Developer: Shipley MF322

Step 22. Implantation (arsenic)
- Ion: As^+
- Energy: 40 keV
- Dose: 5.0×10^{15} cm^{-2}

Step 23. Cleaning procedure (Si)

Step 24. Coating and baking
- Thickness: 1.4 µm
- Photoresist: SPR3012 positive

Step 25. Alignment and exposure (SP)
- Energy: 120 J m^{-2}
- Focus: 0

Step 26. Development
- Developer: Shipley MF322

Step 27. Implantation (boron)
- Ion: B^+
- Energy: 15 keV
- Dose: 5.0×10^{15} cm^{-2}

Step 28. Cleaning procedure (Si)

Step 29. Implantation (boron)
- Ion: B^+
- Energy: 25 keV
- Dose: 9.0×10^{11} cm^{-2}

Step 30. Cleaning procedure (Si)

Step 31. Oxide wet etch
- Chemical: Buffered HF
- Etch rate: (1.3 ± 0.2) nm s^{-1}

Step 32. Cleaning procedure (Si)

Step 33. Anneal/oxidation
- Dopant activation and gate oxidation
- Time: 15 min and 9 min

Step 34. Coating and baking
- Thickness: 2.1 µm
- Photoresist: SPR3012 positive

Step 35. Alignment and exposure (CO)
- Energy: 315 J m^{-2}
- Focus: 0

Step 36. Development
- Developer: Shipley MF322

Step 37. Plasma etching SiO_2
- Drytek plasma etcher

Step 38. Cleaning procedure (Si)
- No boiling HNO_3 to improve contacts

Step 39. Marangoni cleaning procedure (Si)

Step 40. Sputter deposition
- Material: AlSi(1 %)
- Thickness: 200 nm

Step 41. Coating and baking
- Thickness: 2.1 µm
- Photoresist: SPR3012 positive

Step 42. Alignment and exposure (M1)
- Energy: 340 J m^{-2}
- Focus: -1

Step 43. Development
- Developer: Shipley MF322

Step 44. Plasma etching AlSi
- Trikon Ωmega 201 plasma etcher

Step 45. Cleaning procedure (Metal)

Step 46. Deposition of SiO_2
- Novellus Concept One
- Thickness : 600 nm
- Layer: TEOS SiO_2

Step 47. Coating and baking
- Thickness: 2.1 µm
- Photoresist: SPR3012 positive

Step 48. Alignment and exposure (VI)
- Energy: 315 J m^{-2}
- Focus: 0

Step 49. Development
- Developer: Shipley MF322

Step 50. Plasma etching SiO_2
- Drytek plasma etcher

Step 51. Cleaning procedure (Metal)

Step 52. Sputter deposition
- Material: AlSi(1 %)
- Thickness: 2 µm

Step 53. Coating and baking
- Thickness: 2.1 µm
- Photoresist: SPR3012 positive

Step 54. Alignment and exposure (M2)
- Energy: 340 J m^{-2}
- Focus: -1

Step 55. Development
- Developer: Shipley MF322

Step 56. Plasma etching AlSi
- Trikon Ωmega 201 plasma etcher

Step 57. Cleaning procedure (Metal)

E.2. BICMOS8

Starting material: finished BICMOS7 device wafers.

Step 1. Cleaning procedure (Metal)

Step 2. Deposition of SiO_2
- Novellus Concept One
- Thickness : 800 nm
- Layer: TEOS SiO_2

Step 3. Coating and baking
- Thickness: 2.1 µm
- Photoresist: SPR3012 positive

Step 4. Alignment and exposure (BO)
- Energy: 315 J m^{-2}
- Focus: 0

Step 5. Development
- Developer: Shipley MF322

Step 6. Plasma etching SiO_2
- Drytek plasma etcher

Step 7. Cleaning procedure (Metal)

E.3. SICCMOS10

Starting material: finished SICCMOS9 device wafers.

Step 1. Cleaning procedure (Metal, Ti)

Step 2. Sputter deposition **backside**
- Material: Al
- Thickness: 100 nm

Step 3. Deposition of SiO_2
- Novellus Concept One
- Thickness : 800 nm
- Layer: TEOS SiO_2

Step 4. Coating and baking
- Thickness: 2.1 µm
- Photoresist: SPR3012 positive

Step 5. Alignment and exposure (BO)
- Energy: 315 J m^{-2}
- Focus: 0

Step 6. Development
- Developer: Shipley MF322

Step 7. Plasma etching SiO_2
- Drytek plasma etcher

Step 8. Cleaning procedure (Metal, Ti)

E.4. OPTICAL WINDOW INTEGRATION

Starting material: silicon or silicon carbide device wafers, that are complemented with a passivation layer (i.e. BICMOS8 or SICCMOS10).

Step 1. Manual coating and baking SU-8

- Thickness: 10 µm
- Photoresist: SU-8 negative
- Process: 3000 rpm
- Bake: 3 min at 95 °C

Step 2. Alignment and exposure (GL)

- Time: 20 s
- PEB: 3 min at 95 °C

Step 3. Manual development

- Developer: PGMEA, 6 min
- Rinse: perform acetone and isopropanol dip

Step 4. Manual pick and placement

- Position the optical windows on each device chip

Step 5. Thermocompressive bonding

- AML aligner bonder
- Temperature: 120 °C on heaters
- Controlled force: 1–2 kN
- Time: >15 h

Step 6. Hard bake

- Koyo oven
- Temperature: 180 °C
- Time: >48 h

Step 7. Sputter deposition

- Material: Al
- Thickness: 2 µm at 25 °C

Step 8. Manual glue deposition

- Dispense glue droplet on each corner of the optical windows
- Bake: >1 h at 140 °C

Step 9. Spray coating and baking

- Thickness: 1000 mbar, 2 mL and 8 layers
- Bake: 1 min and 20 s at 100 °C
- **Repeat above** 3 **times**
- Extra bake: 6 min at 100 °C

Step 10. Alignment and exposure (OP)

- Mask: Bondpad clearance
- Time: 55 s
- Mask: Aperture openings
- Time: 85 s

Step 11. Manual development

- Developer: AZ400K 4:1, 30 s
- Rinse: serial DI baths

Step 12. Wet etching Al

- Etchant: PES at 35 °C
- Time: ~20 min

Step 13. Cleaning procedure (acetone and isopropanol)

F

WAFER-SCALE MEASUREMENT RESULTS

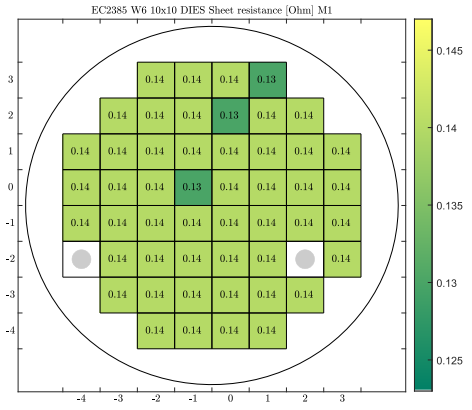


Figure F.1: BICMOS7 M1 layer sheet resistance, with an average of $(138 \pm 2)\,\mathrm{m}\Omega\,\square^{-1}$. Measured using Van der Pauw greek cross structures on W6. Grey circles mark broken devices.

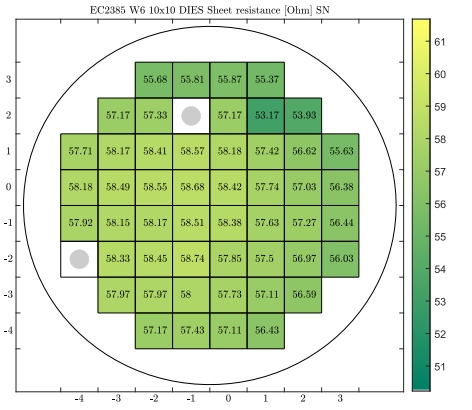


Figure F.2: BICMOS7 SN layer sheet resistance, with an average of $(57 \pm 1)\,\Omega\,\square^{-1}$. Measured using Van der Pauw greek cross structures on W6. Grey circles mark broken devices.

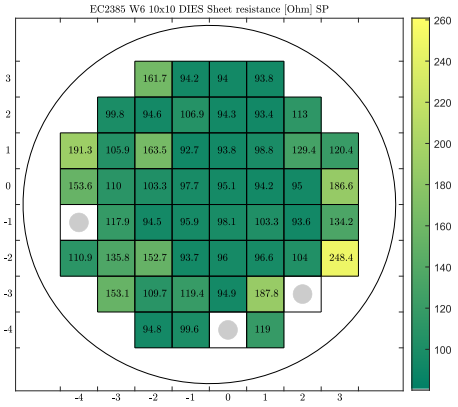


Figure F.3: BICMOS7 SP layer sheet resistance, with an average of $(117 \pm 33)\,\Omega\square^{-1}$. Measured using Van der Pauw greek cross structures on W6. Grey circles mark broken devices.

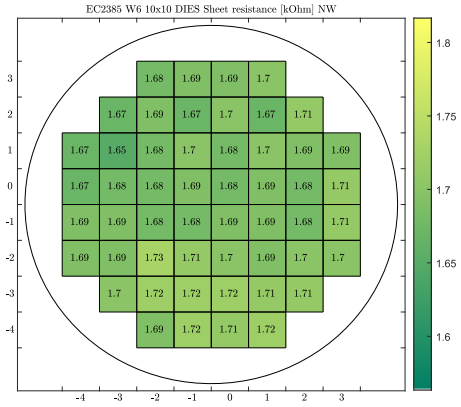


Figure F.4: BICMOS7 NW layer sheet resistance, with an average of $(1.69 \pm 0.02)\,\mathrm{k}\Omega\square^{-1}$. Measured using Van der Pauw greek cross structures on W6. Grey circles mark broken devices.

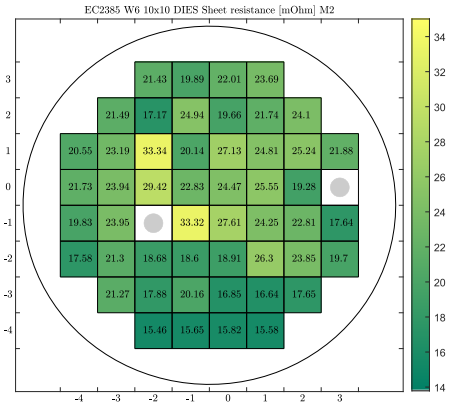


Figure F.5: BICMOS7 M2 layer sheet resistance, with an average of $(22 \pm 4)\,\mathrm{m}\Omega\square^{-1}$. Measured using Van der Pauw greek cross structures on W6. Grey circles mark broken devices.

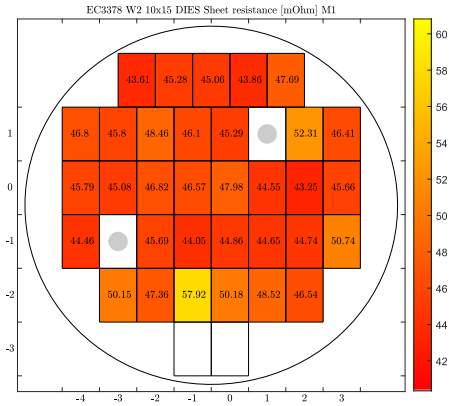


Figure F.6: SICCMOS9 M1 layer sheet resistance, with an average of $(47 \pm 3)\,\mathrm{m}\Omega\square^{-1}$. Measured using Van der Pauw greek cross structures on W2. Grey circles mark broken devices.

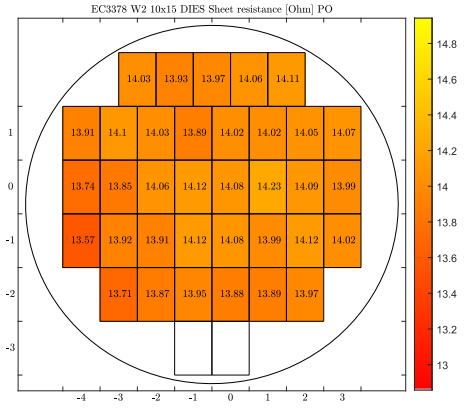


Figure F.7: SICCMOS9 PO layer sheet resistance, with an average of $(14.0 \pm 0.1)\,\Omega\square^{-1}$. Measured using Van der Pauw greek cross structures on W2. Grey circles mark broken devices.

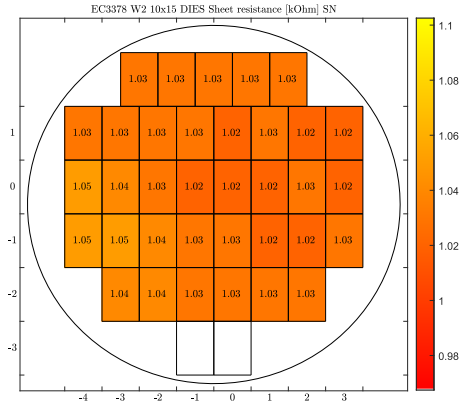


Figure F.8: SICCMOS9 SN layer sheet resistance, with an average of $(1.03 \pm 0.01)\,\mathrm{k}\Omega\square^{-1}$. Measured using Van der Pauw greek cross structures on W2. Grey circles mark broken devices.

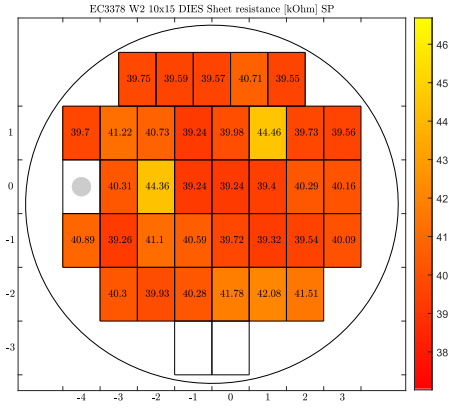


Figure F.9: SICCMOS9 SP layer sheet resistance, with an average of $(40.4 \pm 1.3)\,\mathrm{k}\Omega\square^{-1}$. Measured using Van der Pauw greek cross structures on W2. Grey circles mark broken devices.

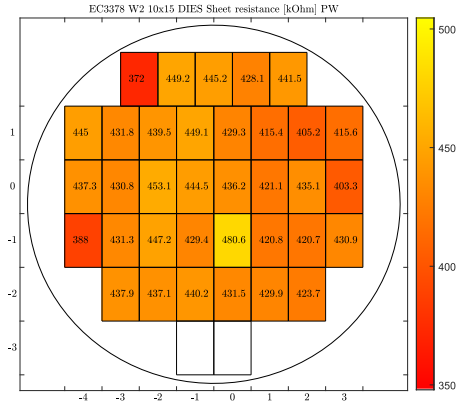


Figure F.10: SICCMOS9 PW layer sheet resistance, with an average of $(431 \pm 19)\,\mathrm{k}\Omega\square^{-1}$. Measured using Van der Pauw greek cross structures on W2. Grey circles mark broken devices.

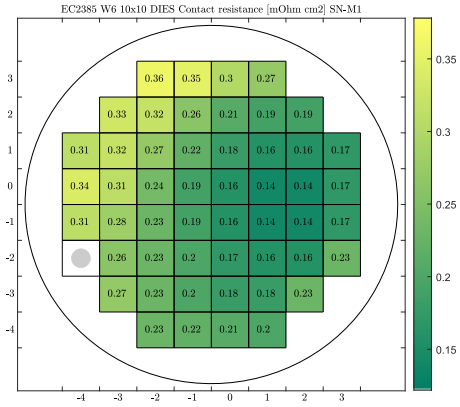


Figure F.11: BICMOS7 SN-M1 layer contact resistance, with an average of $(0.22 \pm 0.06)\,\mathrm{m\Omega\,cm^2}$. Measured using 4-probe electric line measurement on W6. Grey circles mark broken devices.

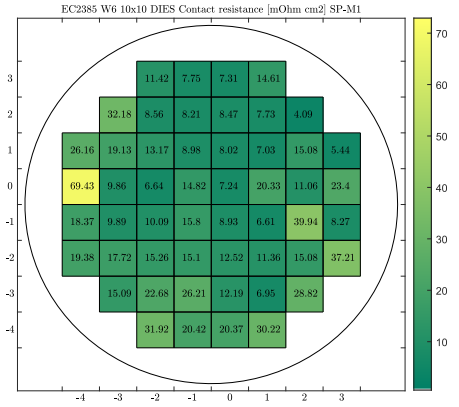


Figure F.12: BICMOS7 SP-M1 layer contact resistance, with an average of $(16 \pm 11)\,\mathrm{m\Omega\,cm^2}$. Measured using 4-probe electric line measurement on W6. Grey circles mark broken devices.

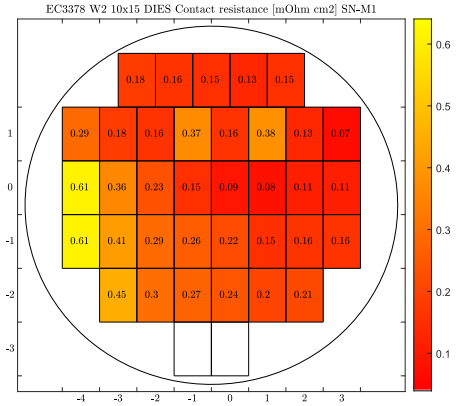


Figure F.13: SICCMOS9 SN-M1 layer contact resistance, with an average of $(0.23 \pm 0.13)\,\mathrm{m\Omega\,cm^2}$. Measured using 4-probe electric line measurement on W2. Grey circles mark broken devices.

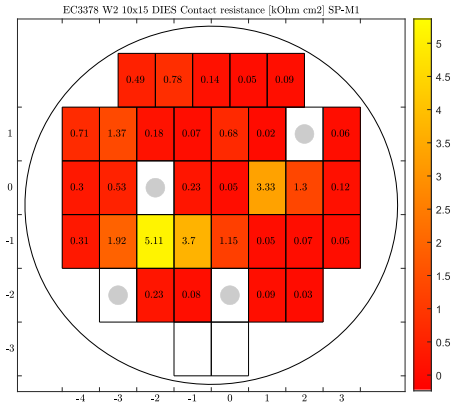


Figure F.14: SICCMOS9 SP-M1 layer contact resistance, with an average of $(0.75 \pm 1.22)\,\mathrm{k\Omega\,cm^2}$. Measured using 4-probe electric line measurement on W2. Grey circles mark broken devices.

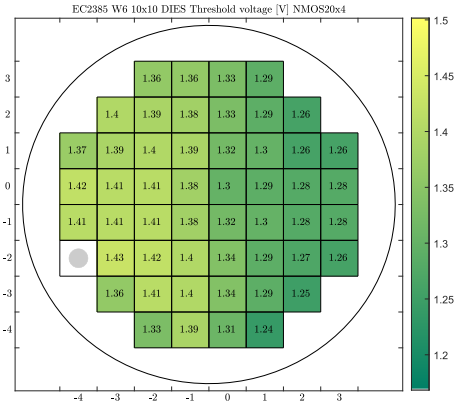


Figure F.15: The BICMOS7 NMOS 20 × 4 µm threshold voltage, with an average of (1.34 ± 0.06) V. Measured with 0.1 V drain-source voltage bias on W6. Grey circles mark broken devices.

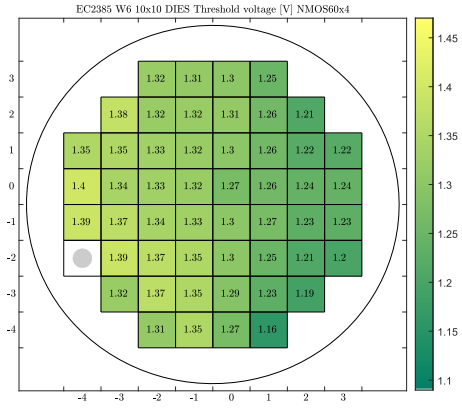


Figure F.16: The BICMOS7 NMOS 60 × 4 µm threshold voltage, with an average of (1.30 ± 0.06) V. Measured with 0.1 V drain-source voltage bias on W6. Grey circles mark broken devices.

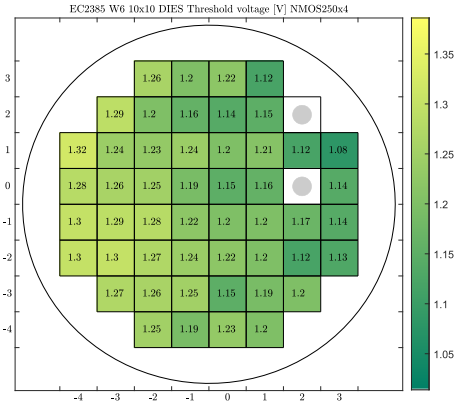


Figure F.17: The BICMOS7 NMOS 250 × 4 µm threshold voltage, with an average of (1.21 ± 0.06) V. Measured with 0.1 V drain-source voltage bias on W6. Grey circles mark broken devices.

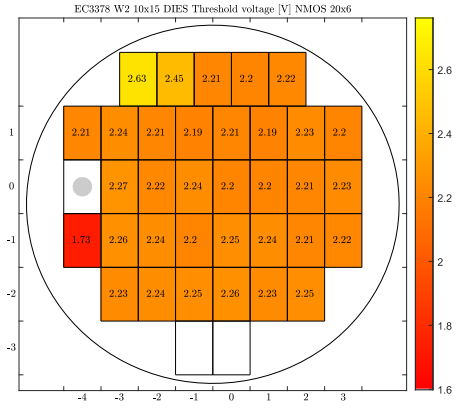


Figure F.18: The SICCMOS9 NMOS 20 × 6 µm threshold voltage, with an average of (2.23 ± 0.12) V. Measured with 0.2 V drain-source voltage bias on W2. Grey circles mark broken devices.

F

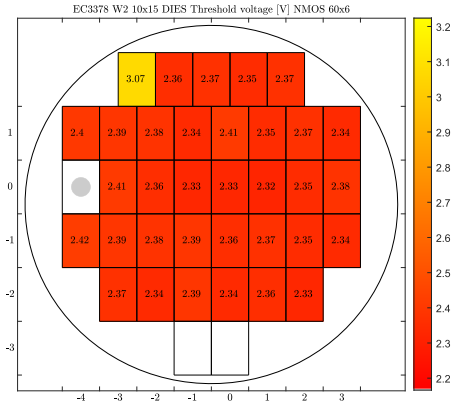


Figure F.19: The SICCMOS9 NMOS 60 × 6 µm threshold voltage, with an average of (2.39 ± 0.12) V. Measured with 0.2 V drain-source voltage bias on W2. Grey circles mark broken devices.

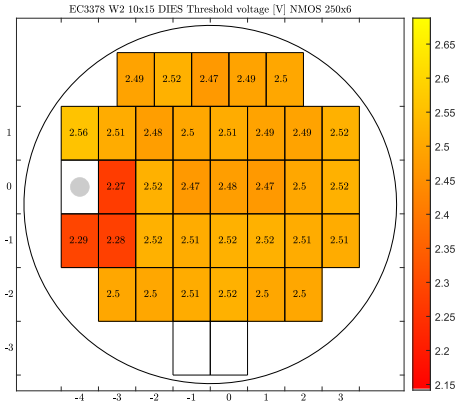


Figure F.20: The SICCMOS9 NMOS 250 × 6 µm threshold voltage, with an average of (2.48 ± 0.07) V. Measured with 0.2 V drain-source voltage bias on W2. Grey circles mark broken devices.

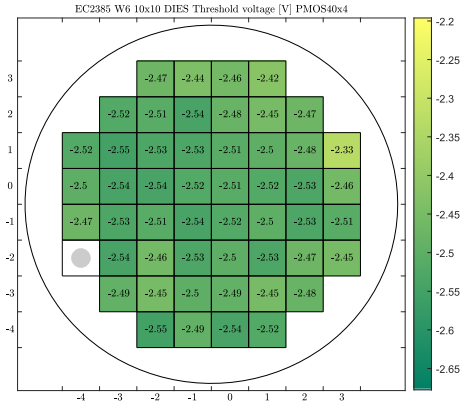


Figure F.21: The BICMOS7 PMOS 40 × 4 µm threshold voltage, with an average of (−2.50 ± 0.04) V. Measured with −0.1 V drain-source voltage bias on W6. Grey circles mark broken devices.

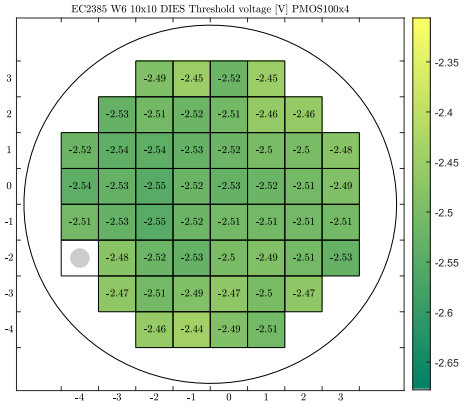


Figure F.22: The BICMOS7 PMOS 100 × 4 µm threshold voltage, with an average of (−2.50 ± 0.03) V. Measured with −0.1 V drain-source voltage bias on W6. Grey circles mark broken devices.

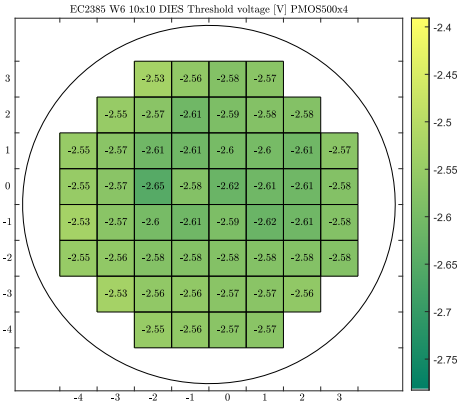


Figure F.23: The BICMOS7 PMOS 500 × 4 µm threshold voltage, with an average of (−2.58 ± 0.02) V. Measured with −0.1 V drain-source voltage bias on W6. Grey circles mark broken devices.

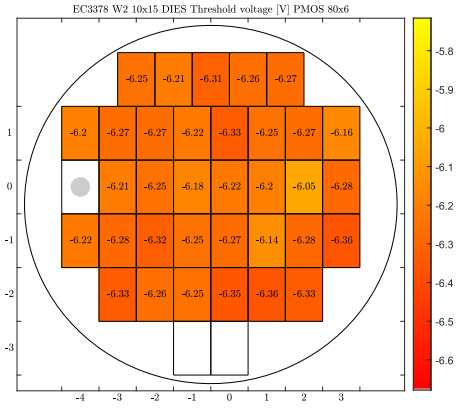


Figure F.24: The SICCMOS9 PMOS 80 × 6 µm threshold voltage, with an average of (−6.25 ± 0.07) V. Measured with −2 V drain-source voltage bias on W2. Grey circles mark broken devices.

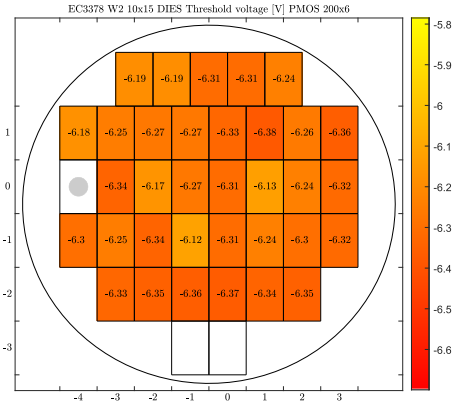


Figure F.25: The SICCMOS9 PMOS 200 × 6 µm threshold voltage, with an average of (−6.28 ± 0.07) V. Measured with −2 V drain-source voltage bias on W2. Grey circles mark broken devices.

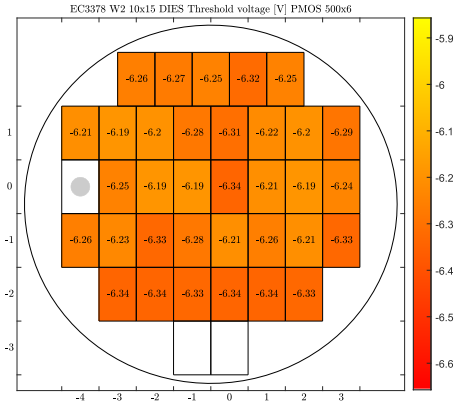


Figure F.26: The SICCMOS9 PMOS 500 × 6 µm threshold voltage, with an average of (−6.26 ± 0.05) V. Measured with −2 V drain-source voltage bias on W2. Grey circles mark broken devices.

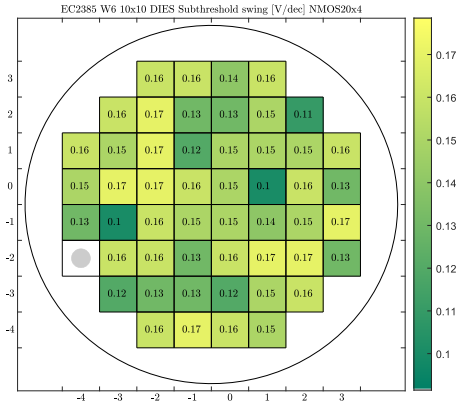


Figure F.27: Subthreshold slope of BICMOS7 NMOS $20 \times 4\,\mu m$, with average of $(0.15 \pm 0.02)\,V dec^{-1}$. Measured with 0.1 V drain-source voltage bias on W6. Grey circles mark broken devices.

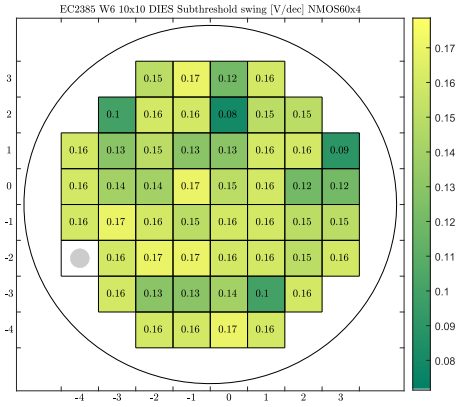


Figure F.28: Subthreshold slope of BICMOS7 NMOS $60 \times 4\,\mu m$, with average of $(0.15 \pm 0.02)\,V dec^{-1}$. Measured with 0.1 V drain-source voltage bias on W6. Grey circles mark broken devices.

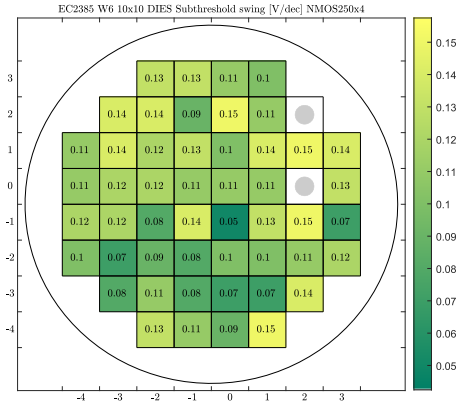


Figure F.29: Subthreshold slope of BICMOS7 NMOS $250 \times 4\,\mu m$, with average of $(0.11 \pm 0.03)\,V dec^{-1}$. Measured with 0.1 V drain-source voltage bias on W6. Grey circles mark broken devices.

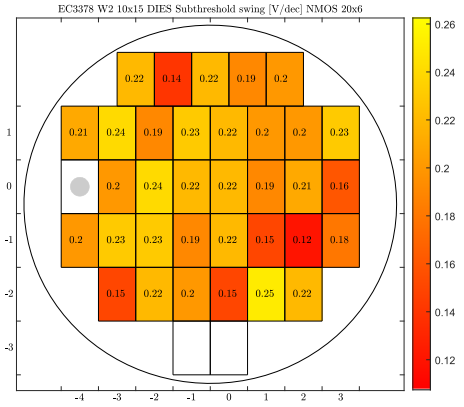


Figure F.30: Subthreshold slope of SICCMOS9 NMOS $20 \times 6\,\mu m$, with average of $(0.20 \pm 0.03)\,V dec^{-1}$. Measured with 0.2 V drain-source voltage bias on W2. Grey circles mark broken devices.

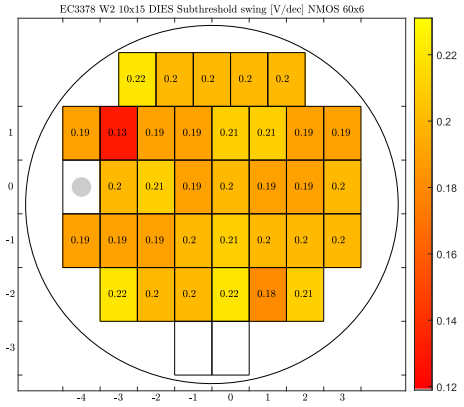


Figure F.31: Subthreshold slope of SICCMOS9 NMOS $60 \times 6\,\mu m$, with average of $(0.20 \pm 0.01)\,V\,dec^{-1}$. Measured with 0.2 V drain-source voltage bias on W2. Grey circles mark broken devices.

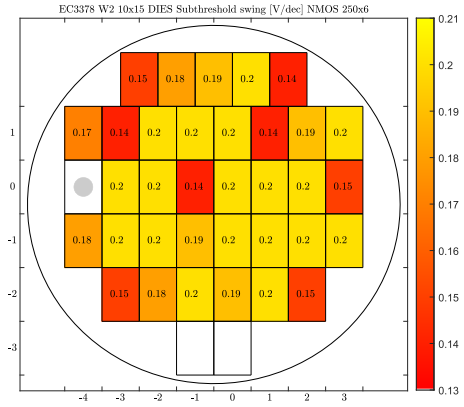


Figure F.32: Subthreshold slope of SICCMOS9 NMOS $250 \times 6\,\mu m$, with average of $(0.18 \pm 0.02)\,V\,dec^{-1}$. Measured with 0.2 V drain-source voltage bias on W2. Grey circles mark broken devices.

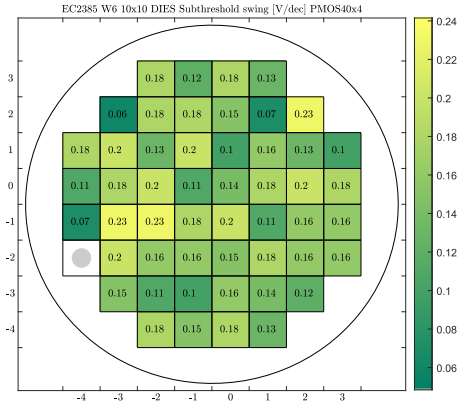


Figure F.33: Subthreshold slope of BICMOS7 PMOS $40 \times 4\,\mu m$, with average of $(0.16 \pm 0.04)\,V\,dec^{-1}$. Measured with -0.1 V drain-source voltage bias on W6. Grey circles mark broken devices.

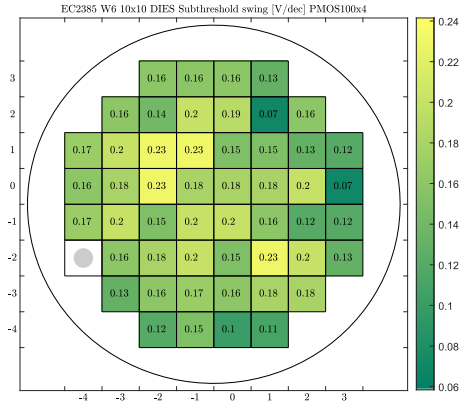


Figure F.34: Subthreshold slope of BICMOS7 PMOS $100 \times 4\,\mu m$, with average of $(0.16 \pm 0.04)\,V\,dec^{-1}$. Measured with -0.1 V drain-source voltage bias on W6. Grey circles mark broken devices.

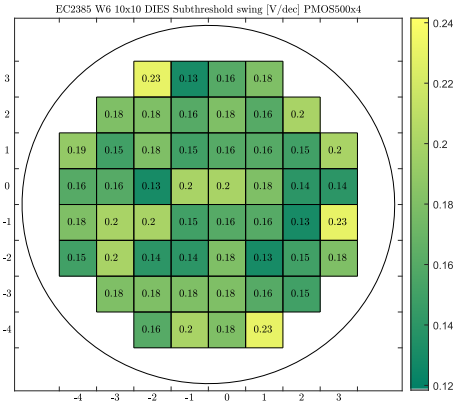


Figure F.35: Subthreshold slope of BICMOS7 PMOS $500 \times 4\,\mu m$, with average of $(0.17 \pm 0.02)\,V dec^{-1}$. Measured with $-0.1\,V$ drain-source voltage bias on W6. Grey circles mark broken devices.

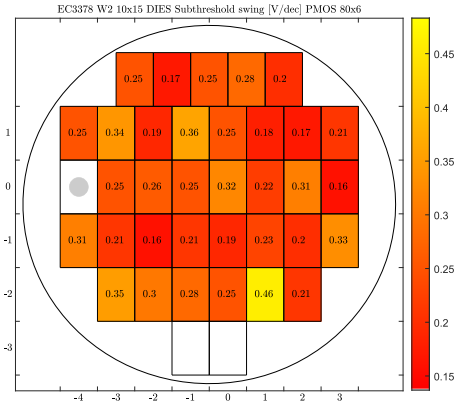


Figure F.36: Subthreshold slope of SICCMOS9 PMOS $80 \times 4\,\mu m$, with average of $(0.25 \pm 0.07)\,V dec^{-1}$. Measured with $-2\,V$ drain-source voltage bias on W2. Grey circles mark broken devices.

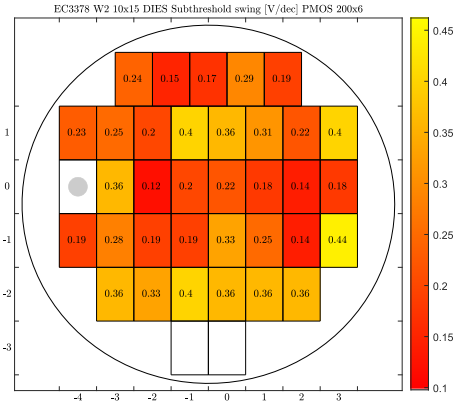


Figure F.37: Subthreshold slope of SICCMOS9 PMOS $200 \times 4\,\mu m$, with average of $(0.26 \pm 0.09)\,V dec^{-1}$. Measured with $-2\,V$ drain-source voltage bias on W2. Grey circles mark broken devices.

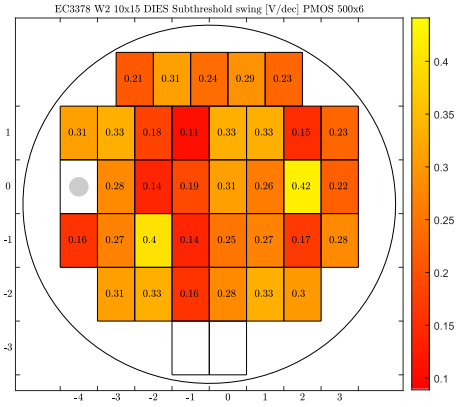


Figure F.38: Subthreshold slope of SICCMOS9 PMOS $500 \times 4\,\mu m$, with average of $(0.26 \pm 0.08)\,V dec^{-1}$. Measured with $-2\,V$ drain-source voltage bias on W2. Grey circles mark broken devices.

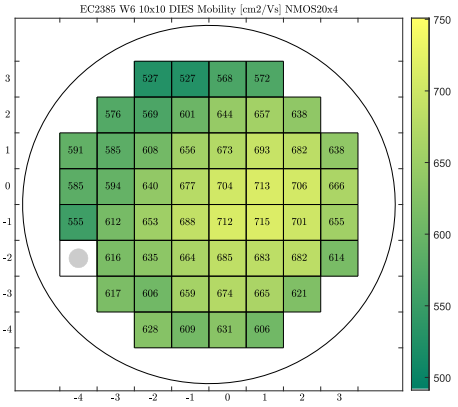


Figure F.39: The BICMOS7 NMOS $20 \times 4\,\mu m$ mobility, with an average of $(637 \pm 49)\,cm^2\,V^{-1}\,s^{-1}$. Measured with 0.1 V drain-source voltage bias on W6. Grey circles mark broken devices.

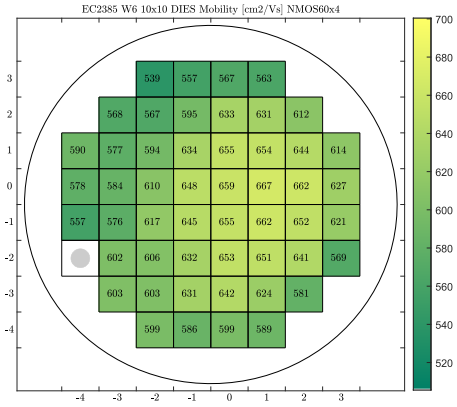


Figure F.40: The BICMOS7 NMOS $60 \times 4\,\mu m$ mobility, with an average of $(612 \pm 34)\,cm^2\,V^{-1}\,s^{-1}$. Measured with 0.1 V drain-source voltage bias on W6. Grey circles mark broken devices.

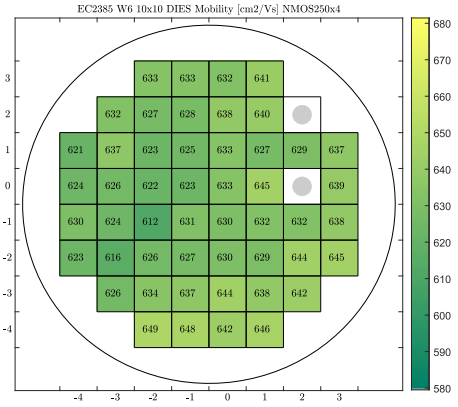


Figure F.41: The BICMOS7 NMOS $250 \times 4\,\mu m$ mobility, with an average of $(632 \pm 8)\,cm^2\,V^{-1}\,s^{-1}$. Measured with 0.1 V drain-source voltage bias on W6. Grey circles mark broken devices.

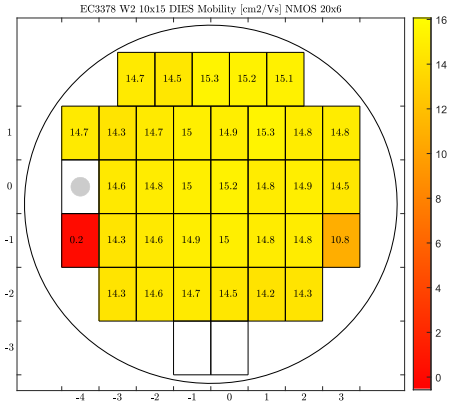


Figure F.42: The SICCMOS9 NMOS $20 \times 6\,\mu m$ mobility, with an average of $(14.2 \pm 2.6)\,cm^2\,V^{-1}\,s^{-1}$. Measured with 0.2 V drain-source voltage bias on W2. Grey circles mark broken devices.

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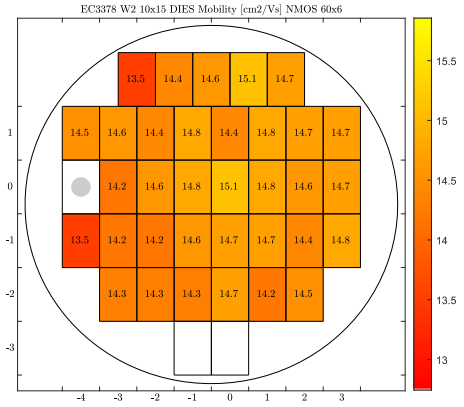


Figure F.43: The SICCMOS9 NMOS 60 × 6 µm mobility, with an average of $(14.5 \pm 0.4)\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$. Measured with 0.2 V drain-source voltage bias on W2. Grey circles mark broken devices.

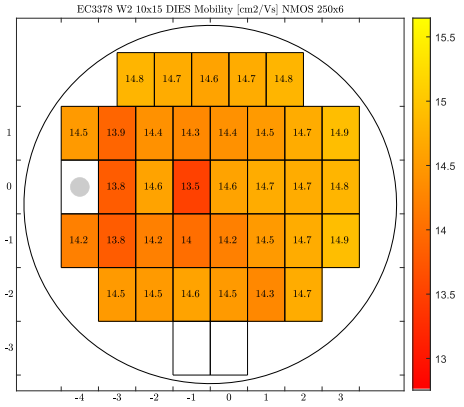


Figure F.44: The SICCMOS9 NMOS 250 × 6 µm mobility, with an average of $(14.5 \pm 0.3)\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$. Measured with 0.2 V drain-source voltage bias on W2. Grey circles mark broken devices.

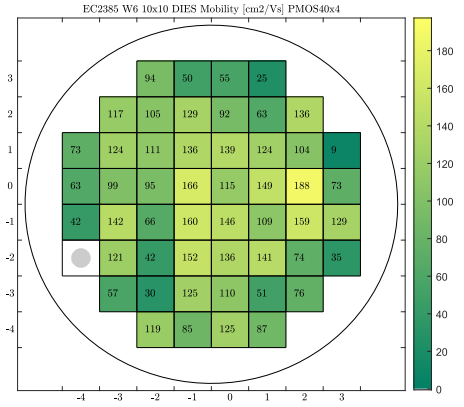


Figure F.45: The BICMOS7 PMOS 20 × 4 µm mobility, with an average of $(101 \pm 42)\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$. Measured with −0.1 V drain-source voltage bias on W6. Grey circles mark broken devices.

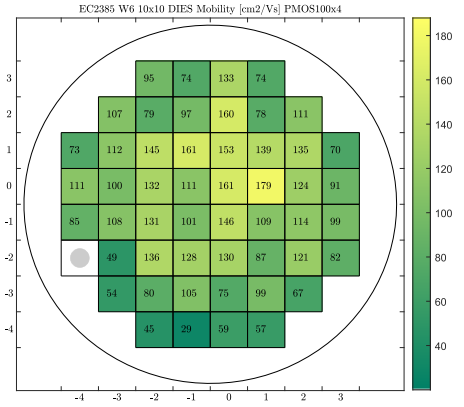


Figure F.46: The BICMOS7 PMOS 100 × 4 µm mobility, with an average of $(104 \pm 34)\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$. Measured with −0.1 V drain-source voltage bias on W6. Grey circles mark broken devices.

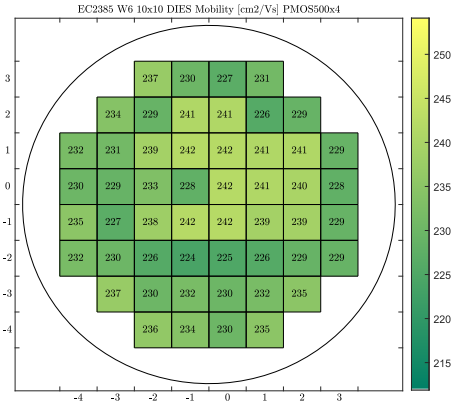


Figure F.47: The BICMOS7 PMOS 500 × 4 µm mobility, with an average of $(233 \pm 6)\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$. Measured with −0.1 V drain-source voltage bias on W6. Grey circles mark broken devices.

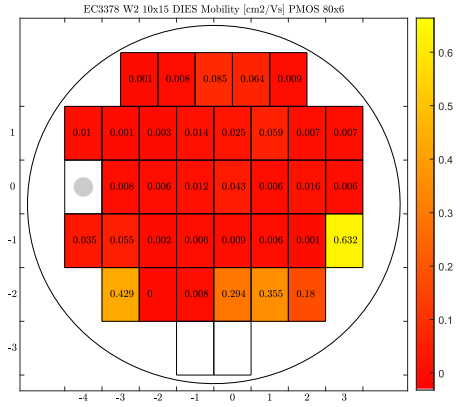


Figure F.48: The SICCMOS9 PMOS 80 × 6 µm mobility, with an average of $(0.1 \pm 0.1)\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$. Measured with −2 V drain-source voltage bias on W2. Grey circles mark broken devices.

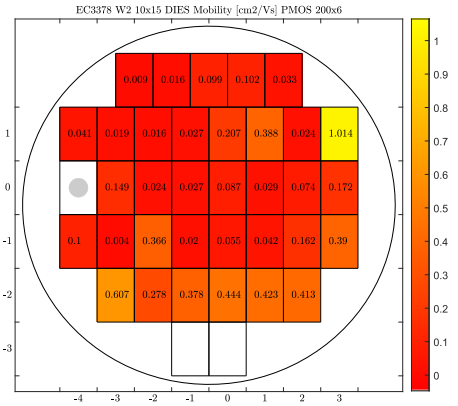


Figure F.49: The SICCMOS9 PMOS 200 × 6 µm mobility, with an average of $(0.2 \pm 0.2)\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$. Measured with −2 V drain-source voltage bias on W2. Grey circles mark broken devices.

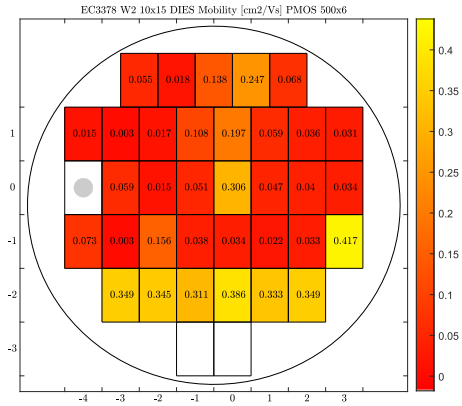


Figure F.50: The SICCMOS9 PMOS 500 × 6 µm mobility, with an average of $(0.1 \pm 0.1)\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$. Measured with −2 V drain-source voltage bias on W2. Grey circles mark broken devices.

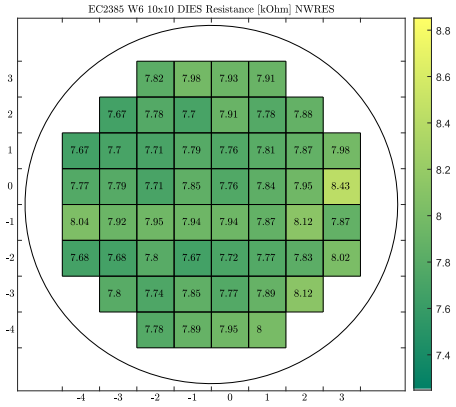


Figure F.51: BICMOS7 NW resistor, with an average of $(7.85 \pm 0.14)\,\mathrm{k\Omega}$. Grey circles mark broken devices.

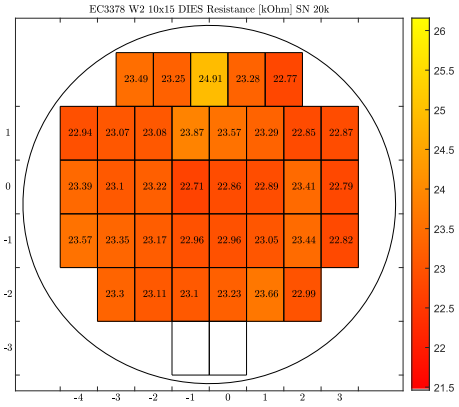


Figure F.52: SICCMOS9 SN resistor, with an average of $(23.2 \pm 0.4)\,\mathrm{k\Omega}$. Grey circles mark broken devices.

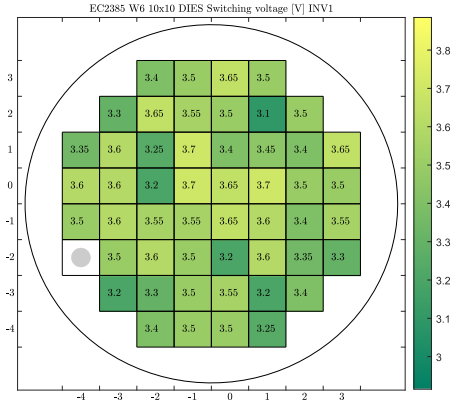


Figure F.53: BICMOS7 small inverter, with an average switching voltage of $(4.0 \pm 0.1)\,\mathrm{V}$. Grey circles mark broken devices.

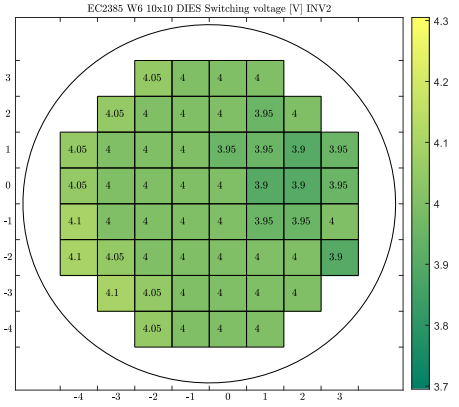


Figure F.54: BICMOS7 driver inverter, with an average switching voltage of $(3.5 \pm 0.2)\,\mathrm{V}$. Grey circles mark broken devices.

F

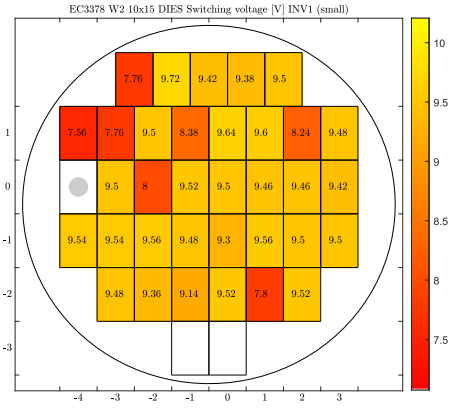


Figure F.55: SICCMOS9 small inverter, with an average switching voltage of (9.2 ± 0.7) V. Grey circles mark broken devices.

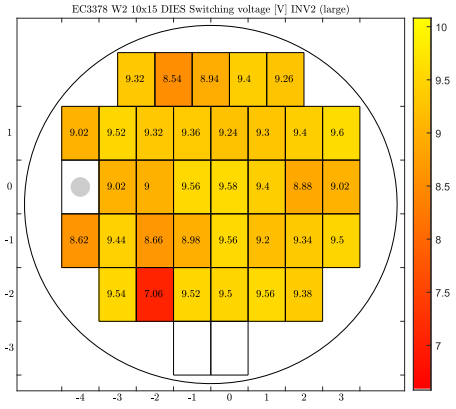


Figure F.56: SICCMOS9 driver inverter, with an average switching voltage of (9.2 ± 0.5) V. Grey circles mark broken devices.

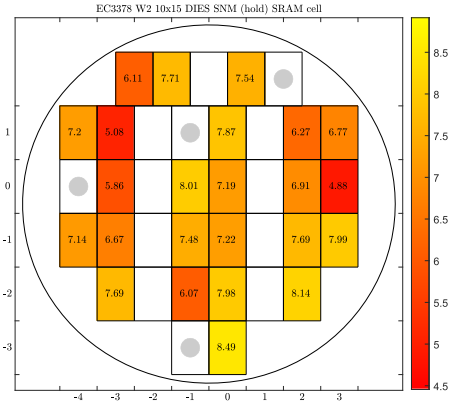


Figure F.57: SICCMOS9 SRAM cell, with an average hSNM voltage of (7.1 ± 1.0) V. Grey circles mark broken devices.

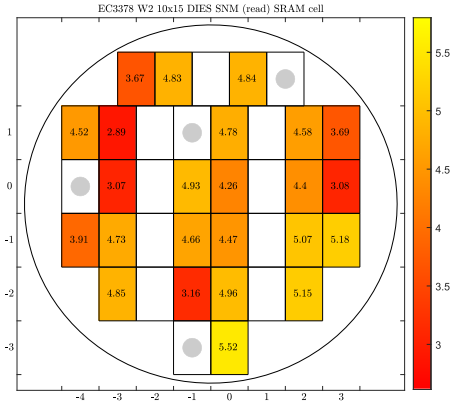


Figure F.58: SICCMOS9 SRAM cell, with an average rSNM voltage of (4.4 ± 0.7) V. Grey circles mark broken devices.

F

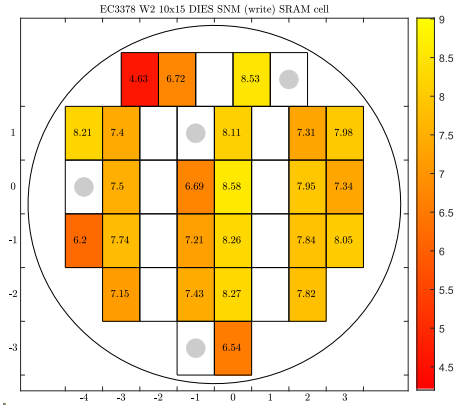


Figure F.59: SICCMOS9 SRAM cell, with an average wSNM voltage of (7.5 ± 0.9) V. Grey circles mark broken devices.

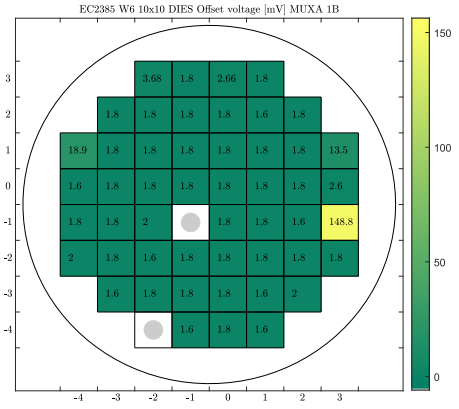


Figure F.60: BICMOS7 analog 1-bit multiplexer, with an average offset voltage of (5 ± 21) mV. Grey circles mark broken devices.

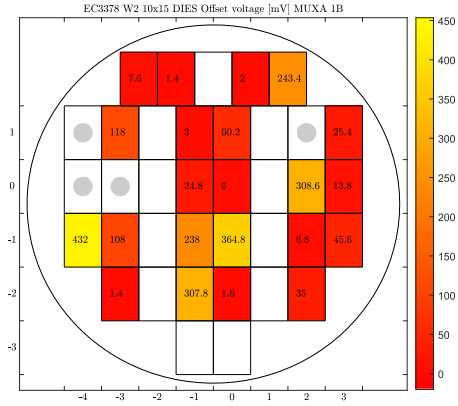


Figure F.61: SICCMOS9 analog 1-bit multiplexer, with an average offset voltage of (107 ± 139) mV. Grey circles mark broken devices.

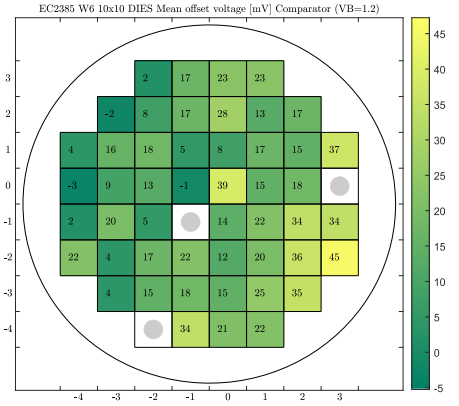


Figure F.62: BICMOS7 comparator biased at 1.2 V, with an average offset voltage of (17 ± 11) mV. Grey circles mark broken devices.

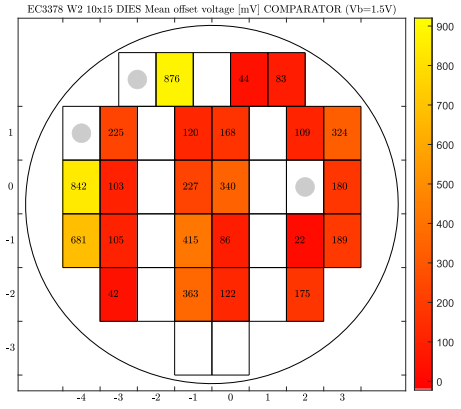


Figure F.63: SICCMOS9 comparator biased at 1.5 V, with an average offset voltage of (254 ± 242) mV. Grey circles mark broken devices.

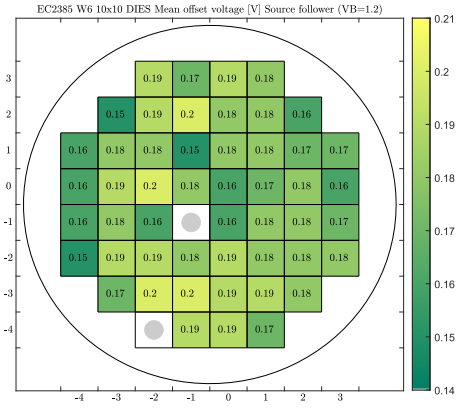


Figure F.64: BICMOS7 unity-gain buffer biased at 1.2 V, with an average offset voltage of (0.18 ± 0.01) V. Grey circles mark broken devices.

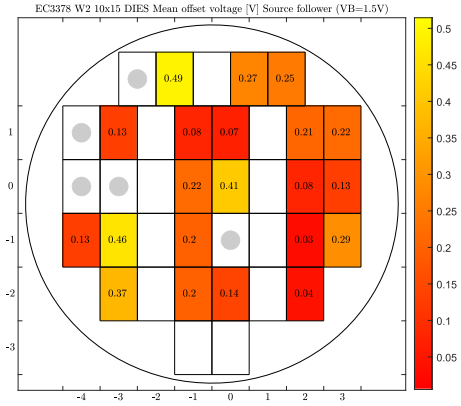


Figure F.65: SICCMOS9 unity-gain buffer biased at 1.5 V, with an average offset voltage of (0.21 ± 0.13) V. Grey circles mark broken devices.

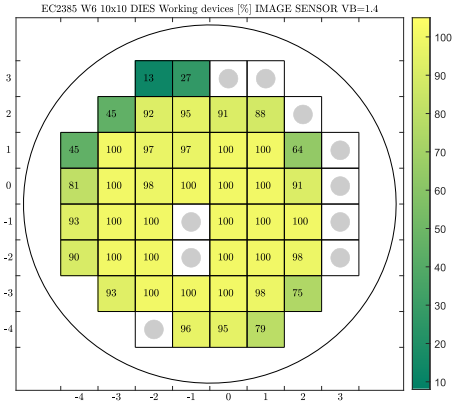


Figure F.66: BICMOS7 image sensor biased at 1.4 V, with working pixels indicated. Grey circles mark broken devices.

F

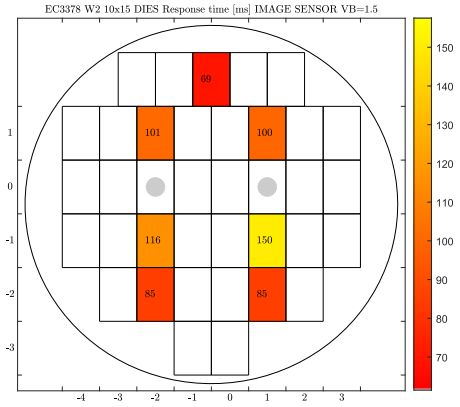


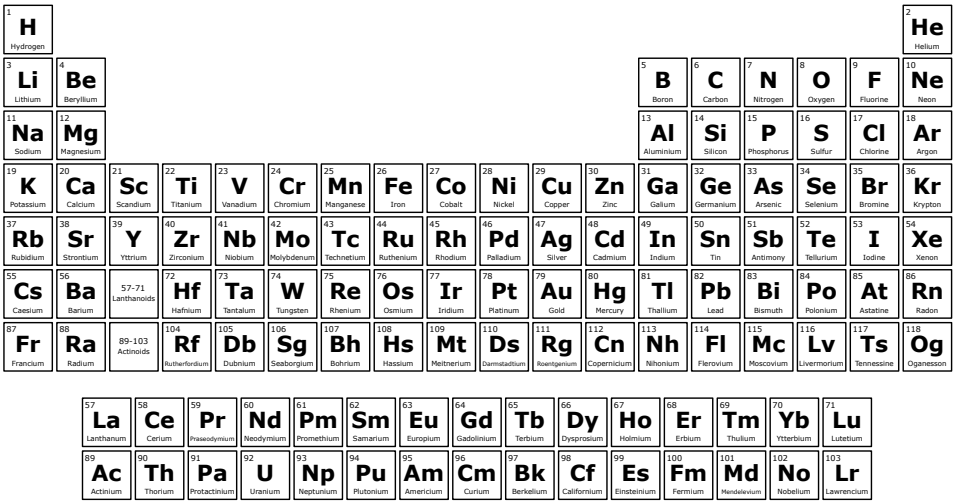
Figure F.67: SICCMOS9 image sensor biased at 1.5 V, with response times indicated. Grey circles mark broken devices.

Acronyms and Abbreviations

3T APS	Three transistor APS topology
AC	Active area design layer
ADC	Analog-to-digital converter
APD	Avalanche photodiode
APS	Active pixel sensor
ARC	Anti-reflection coating
ARR	Albedo rejection ratio
ASP	Angle sensitive pixel
BEOL	Back-end-of-line
BICMOS7	Seven mask BJT and CMOS silicon based technology
BICMOS8	Eight mask BJT and CMOS silicon based technology
BJT	Bipolar junction transistor
CMOS	Complementary metal-oxide-semiconductor
CO	Contact openings design layer
CPGA	Ceramic pin-grid array
CTAT	Complementary to absolute temperature
DAC	Digital-to-analog converter
DAQ	Data acquisition tool
DNL	Differential non-linearity
DRC	Design rule check
DVT	Data visualization and analysis tool
ELT	Enclosed layout transistor
EQE	External quantum efficiency
EV	Electric vehicle
FEOL	Front-end-of-line
FoM	Figure-of-merit
FoV	Field of view
FWHM	Full width at half maximum
HEMT	High electron mobility transistor
IQE	Internal quantum efficiency
GUI	Graphical user interface
HRSMU	High-resolution source-measurement unit
IISB	Institute for Integrated Systems and Devices Technology
INL	Integral non-linearity
JFET	Junction field-effect transistor
LSB	Least significant bit
LVS	Layout-versus-schematic

LUT	Look-up table
M1	First metal interconnect design layer
M2	Second metal interconnect design layer
MAA	Mean angular accuracy
MEMS	Microelectromechanical system
MESFET	Metal-semiconductor field-effect-transistor
MOSFET	Metal-oxide-semiconductor field-effect-transistor
MIM	Metal-insulator-metal
MSB	Most significant bit
MSM	Metal-semiconductor-metal
ND	Not determined
NMOS	N-type channel metal-oxide-semiconductor device
NW	N-well design layer
PC	Contact to polysilicon design layer
PCB	Printed circuit board
PCM	Process control module
PDCR	Photo-to-dark current ratio
PECVD	Plasma-enhanced chemical vapor deposition
PFCA	Planar Fourier capture array
PIN	P-type/intrinsic/n-type doped regions
PMOS	P-type channel metal-oxide-semiconductor device
PN	P-type/n-type doped regions
PO	Polysilicon design layer
PW	P-well design layer
RTA	Rapid thermal annealing
SB	Substrate design layer
SEU	Single event upset
SICCMOS10	Ten mask CMOS silicon carbide based technology
SICCMOS11	Eleven mask CMOS silicon carbide based technology
SICCMOS9	Nine mask CMOS silicon carbide based technology
SiP	System-in-package
SLA	Stereolithography apparatus
SN	Shallow n-type design layer
SNM	Static noise margins
SNR	Signal-to-noise ratio
SoC	System-on-chip
SP	Shallow p-type design layer
SRAM	Static random-access memory
STI	Shallow trench isolation
TCR	Temperature coefficient of resistance
TSV	Through-substrate-via
VI	Via openings design layer
VMU	Voltage measurement unit
VSU	Voltage source unit
ZIF	Zero insertion force

Periodic Table of the Elements and Materials



3C-SiC	3 bilayer cubic polytype of silicon carbide
4H-SiC	4 bilayer hexagonal polytype of silicon carbide
6H-SiC	6 bilayer hexagonal polytype of silicon carbide
α-SiC	Other name for non 3C-SiC polytypes
β-SiC	Other name for 3C-SiC polytype
AlSi(1 %)	Aluminum with 1 % silicon
BCB	Benzocyclobutene
Epi-layer	Epitaxial layer
PDMS	Polydimethylsiloxane
SU-8	Epoxy based negative photoresist
TEOS	Tetraethylorthosilicate

List of Publications

Journal papers

1. ***In review*** - **J. Romijn**, S. Vollebregt, V. G. de Bie, L. M. Middelburg, B. El Mansouri, H. W. van Zeijl, A. May, T. Erlbacher, J. Leijtens, G. Q. Zhang and P. M. Sarro, *Microfabricated albedo insensitive sun position sensor system in silicon carbide with integrated 3D optics and CMOS electronics*, Sensors and Actuators A: Physical (2022).

2. **J. Romijn**, S. Vollebregt, L. M. Middelburg, B. El Mansouri, H. W. van Zeijl, A. May, T. Erlbacher, J. Leijtens, G. Q. Zhang and P. M. Sarro, *Integrated 64 pixel UV image sensor and CMOS readout in silicon carbide*, Nature Microsystems & Nanoengineering **8**, Art no. 114 (2022).

3. **J. Romijn**, S. Şanseven, G. Q. Zhang, S. Vollebregt and P. M. Sarro, *Angle sensitive optical sensor for light source tracker miniaturization*, IEEE Sensors Letters **6**(6), pp 1–4, Art no. 3501404 (2022).

4. **J. Romijn**, S. Vollebregt, L. M. Middelburg, B. El Mansouri, H. W. van Zeijl, A. May, T. Erlbacher, G. Q. Zhang and P. M. Sarro, *Integrated digital and analog circuit blocks in a scalable silicon carbide CMOS technology*, IEEE Transactions on Electron Devices **69**, pp 4–10 (2021).

5. **J. Romijn**, R. J. Dolleman, M. Singh, H. S. J. van der Zant, P. G. Steeneken, P. M. Sarro and S. Vollebregt, *Multi-layer graphene Pirani pressure sensors*, Nanotechnology **32**(33), 335501 (2021).

Conference proceedings

1. ***Accepted*** - **J. Romijn**, S. Şanseven, G. Q. Zhang, S. Vollebregt and P. M. Sarro, *Angle sensitive optical sensor for light source tracker miniaturization*, IEEE Sensors, (2023).

2. ***In press*** - H. J. van Ginkel, M. Orvietani, **J. Romijn**, G. Q. Zhang and S. Vollebregt, *ZnO nanoparticle printing for UV sensor fabrication*, IEEE Sensors, Dallas, United states (2022).

3. X. Ji, **J. Romijn**, H. J. van Ginkel, X. Liu, H. W. van Zeijl and G. Q. Zhang, *Low temperature sapphire to silicon flip chip interconnects by copper nanoparticle sintering*, 2022 IEEE 9th Electronics System-Integration Technology Conference (ESTC), pp 368–372, Sibiu, Romania (2022).

4. **J. Romijn**, S. Vollebregt, A. May, T. Erlbacher, H. W. van Zeijl, J. Leijtens, G. Q. Zhang and P. M. Sarro, *Visible blind quadrant sun position sensor in a silicon carbide*

technology, 2022 IEEE 35th International Conference on Micro Electro Mechanical Systems (MEMS), pp 535–538, Tokyo, Japan (2022).

5. **J. Romijn**, L. M. Middelburg, S. Vollebregt, B. El Mansouri, H. W. van Zeijl, A. May, T. Erlbacher, G. Q. Zhang and P. M. Sarro, *Resistive and CTAT temperature sensors in a silicon carbide CMOS technology*, IEEE Sensors, online (2021).

6. H. J. van Ginkel, **J. Romijn**, S. Vollebregt and G. Q. Zhang, *High step coverage interconnects by printed nanoparticles*, 2021 23rd European Microelectronics and Packaging Conference & Exhibition (EMPC), online (2021).

7. **J. Romijn**, S. Vollebregt, G. Q. Zhang and P. M. Sarro, *Towards a scalable technology for albedo insensitive sun sensors in silicon carbide*, 2021 11th International ESA Conference on Guidance, Navigation & Control Systems (GNC), online (2021).

8. **J. Romijn**, S. Vollebregt, H. W. van Zeijl, G. Q. Zhang, J. Leijtens and P. M. Sarro, *Towards a scalable sun position sensor with monolithic integration of the 3D optics for miniaturized satellite attitude control*, 2021 IEEE 34th International Conference on Micro Electro Mechanical Systems (MEMS), pp 642–645, online (2021).

9. **J. Romijn**, S. Vollebregt, H. W. van Zeijl and P. M. Sarro, *A wafer-scale process for the monolithic integration of CVD graphene and CMOS logic for smart MEMS/NEMS sensors*, 2019 IEEE 32nd International Conference on Micro Electro Mechanical Systems (MEMS), pp 260–263, Seoul, South-Korea (2019).

10. S. Vollebregt, **J. Romijn**, H. W. van Zeijl and P. M. Sarro, *Wafer-scale integration of CVD graphene on CMOS devices using a transfer-free approach*, Graphene Week, Helsinki, Finland (2019).

11. **J. Romijn**, S. Vollebregt, R. J. Dolleman, M. Singh, H. S. J. van der Zant, P. G. Steeneken and P. M. Sarro, *A miniaturized low power Pirani pressure sensor based on suspended graphene*, 2018 IEEE 13th International Conference on Nano/Micro Engineered and Molecular Systems (NEMS), pp 11–14, Singapore, Singapore (2018).

12. S. Vollebregt, F. Ricciardella, **J. Romijn**, M. Singh, S. Shi and P. M. Sarro, *A transfer-free approach to wafer-scale graphene deposited by chemical vapour deposition*, Graphene Conference, Dresden, Germany (2018).

MISCELLANEOUS

1. **J. Romijn**, S. Vollebregt, G. Q. Zhang and P. M. Sarro, *Exploring integrated circuit blocks in an open silicon carbide CMOS technology*, ProRISC & SAFE, Delft (2021).

2. **J. Romijn**, *EnABLES/NiPS Powering the Internet of Things Virtual Winter School*, University of Perugia, online (2020).

3. **J. Romijn**, H. J. van Ginkel, L. van Dam, H. W. van Zeijl and S. Vollebregt, *A modular Matlab based data visualization tool for wafer-scale parameter analysis*, Microelectronics Department, Delft University of Technology (2019).

4. **J. Romijn**, S. Vollebregt, G. Q. Zhang and P. M. Sarro, *Monolithically integrated sun sensors based on silicon carbide for space application*, ProRISC & SAFE, Delft (2019).

5. **J. Romijn**, *Sino-Dutch International High Level Talent Forum and Summer School on Semiconductor Technologies*, Tsinghua University, Beijing, China (2018).

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