Cryo-CMOS Integrator-Based DAC for Scalable Biasing of Semiconductor Qubits

Luc Enthoven, *Graduate Student Member, IEEE*, Job van Staveren, Jiang Gong, Masoud Babaie, *Senior Member, IEEE*, and Fabio Sebastiano, *Senior Member, IEEE*

***Abstract*—Semiconductor-based cryogenic quantum processors require the accurate biasing of a large number of gate electrodes, which are typically individually wired to room-temperature DACs. To prevent the wiring bottleneck when scaling to future very large processors, this work proposes a scalable cryo-CMOS DAC that can operate with a S&H demultiplexer close to the quantum processor. By adopting an integrator-based switched-capacitor DAC with a dynamically-biased high-voltage output stage, both the required large output range and high resolution can be achieved while sharing the DAC over a large number of electrodes, thus improving the power efficiency. Fabricated in a 22-nm FinFET technology, the DAC occupies 0.076 mm^2. At 4.2 K (RT), it achieves an LSB of 57.1 μV (68.3 μV) over a 3 V range with 188 μV_{rms} (192 μV_{rms}) noise and 36.5-LSB (12.6-LSB) INL while dissipating 157 μW (138 μW). The low power dissipation and the potential to drive more than 30,000 electrodes paves the way for scalable biasing of quantum processors operating down to mK temperatures.**

***Index Terms*—Cryo-CMOS, quantum computing, spin qubit, biasing, high-voltage, integrator, switched capacitor, demultiplexer, S&H, qubit, FinFET.**

I. Introduction

SEMICONDUCTOR spin qubits are a promising platform for quantum computing: they have demonstrated high-fidelity qubit control and readout [1], [2], and operation at temperatures above 1 K [3], [4], [5], while being compatible with CMOS processing [6], thus offering the potential co-integration with their electronic interface [7]. In semiconductor qubits, electrons or holes are confined in quantum dots formed by accurately voltage biasing nearby metal electrodes, while coupling AC signals enables qubit initialization, operation, and readout. While room-temperature (RT) electronics typically generates the AC and DC signals to control the few qubits available today, this approach is not scalable to the large number of qubits required in a practical application due to size, cost, and reliability limitations of the many cables between the cryogenic qubits and the RT electronics [8]. CMOS circuits operating at cryogenic temperatures (cryo-CMOS) have been proposed to alleviate such an interconnect bottleneck [9], [10], [11], [12], [13]. For DC biasing, the number of DACs and wires can be reduced by using a sample-and-hold (S&H) demultiplexer with sampling switches and hold capacitors to store the DC voltages, as shown in Fig. 1 [14], [15], while moving the DAC at cryogenic temperatures allows for simplified integration and timing with the demultiplexer.

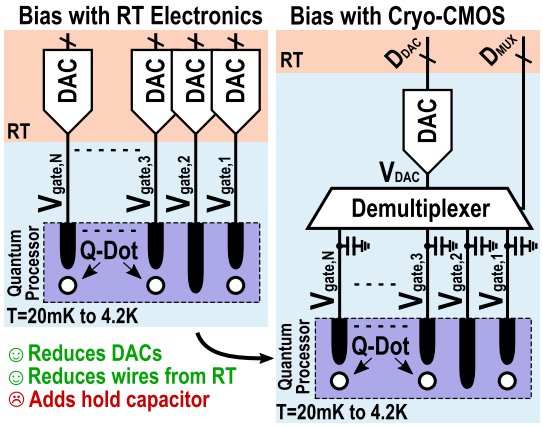

Fig. 1. DC bias generation with room-temperature (RT) or cryo-CMOS electronics.

The biasing DAC must generate voltages that are calibrated for each individual electrode to account for device variations, with the required bias voltage range exceeding 3 V, depending on the layer stack, materials and pinch-off variability [6], [16], [17]. Monolithic integration of qubits and electronics could require this voltage range to be implemented in scaled nodes that do not offer devices compatible with such a range. In addition to the large output range, a high voltage resolution with an LSB less than 100 μV is preferred for sufficient tuning accuracy of the tunnel barriers and for compensation of capacitive crosstalk [18], [19]. If the voltage-resolution specifications are met, the requirements on DAC linearity can be relaxed, since the extensive calibration typically needed by quantum devices can be also used to compensate for DAC nonlinearity at no additional cost. Nevertheless, having a monotonic DAC will simplify the convergence of the biasing calibration algorithm [20]. In addition, the DAC should be able to drive the large (parasitic) capacitive load of the demultiplexer, which becomes significant (> 150 pF) for large electrode arrays (> 10^4). Finally, the cryo-CMOS biasing electronics should dissipate a very low power ($\ll$ 1mW) to

Received 17 February 2026; revised 29 April 2026; accepted 10 May 2026. This work was supported in part by Intel and in part by the Research Program Open Technology Program (OTP) through The Netherlands Organization for Scientific Research (NWO) under Project 16278. This article was recommended by Associate Editor J. Goes. *(Corresponding authors: Luc Enthoven; Fabio Sebastiano.)*

Luc Enthoven was are with the Department of Quantum and Computer Engineering, Delft University of Technology, 2628 CD Delft, The Netherlands, and also with QuTech, 2628 CJ Delft, The Netherlands. He is now with FrostByte, 2628 CJ Delft, The Netherlands (e-mail: luc.enthoven@gmail.com).

Job van Staveren and Fabio Sebastiano are with the Department of Quantum and Computer Engineering, Delft University of Technology, 2628 CD Delft, The Netherlands, and also with QuTech, 2628 CJ Delft, The Netherlands (e-mail: F.Sebastiano@tudelft.nl).

Jiang Gong was with the Department of Quantum and Computer Engineering, Delft University of Technology, 2628 CD Delft, The Netherlands, and also with QuTech, 2628 CJ Delft, The Netherlands. He is now with the University of Electronic Science and Technology of China, Chengdu 610056, China.

Masoud Babaie is with the Department of Microelectronics, Delft University of Technology, 2628 CD Delft, The Netherlands, and also with QuTech, 2628 CJ Delft, The Netherlands.

Digital Object Identifier 10.1109/TCSI.2026.3692714

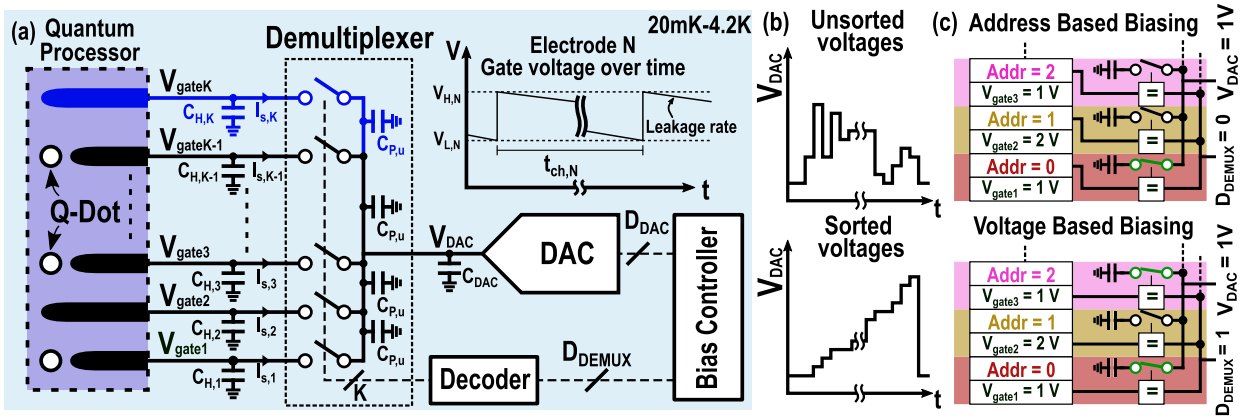

Fig. 2. (a) Diagram of the electrode biasing system consisting of the quantum processor, sample-and-hold demultiplexer (S&H DEMUX), and DAC. The voltage over time of channel N is highlighted to illustrate the effect of leakage over time. (b) Waveforms of V_{DAC} over time comparing unsorted and sorted voltages. (c) Waveforms of V_{DAC} over time showing the difference between address-based biasing, where D_{DEMUX} communicates the address, and voltage-based biasing, where D_{DEMUX} communicates the voltage.

comply with the cooling power available at the mK stage of dilution refrigerators typically employed for spin qubits [21], thus asking for excellent power efficiency of a 15-bit high-voltage high-load DAC.

Although prior work mainly focused only on cryo-CMOS demultiplexers combining biasing and dynamic operations without local signal generation [14], [22], [23], the biasing of a 7-electrode double quantum dot by a capacitive DAC and a S/H operating at mK temperatures has been demonstrated [24], but only over a limited range (1 V) with a relatively large LSB of (122 μV) and a poor monotonicity (DNL > 2.5 LSB) [15]. Charge-stability diagrams for a single-electron transistor showing the typical Coulomb diamonds have also been demonstrated by a R-2R cryo-CMOS DAC with a high resolution (< 10 μV) and linearity (< 1 LSB) [25], but the DAC uses a large area (0.37 mm^2) and has limited output range (1.2 V). Cryo-CMOS DACs for electrode voltage biasing have also been developed for trapped-ion quantum processors, but their specifications are targeting much larger voltages (> 25 V), which leads to orders of magnitude larger power despite the lower required resolution [26], [27].

To offer scalability to thousands of electrodes while ensuring a large output range, high resolution, and low power dissipation, this paper, as an extension of [28], presents a cryo-CMOS DAC that uses a dynamically-biased output stage to achieve output voltages well beyond the process' nominal supply and takes advantage of an integrating-DAC architecture to devise a massively scalable electrode addressing scheme, thus achieving the target specifications with an energy efficient approach. While recent work demonstrates the efficacy of the DAC with a 24-channel multiplexer to bias, characterize, and calibrate quantum devices at 66 mK [29], this work analyzes the DAC architecture, its circuit implementation, and performance. The rest of the paper is organized as follows: Section II introduces the biasing scheme and analyzes its scalability and design trade-offs; Section III continues with the circuit implementation of the integrating DAC and highlights how the reliable high-voltage operation is achieved; Sections IV and V present the experimental characterization and draw the conclusions, respectively.

II. Scalable Electrode Biasing

An overview of an electrode biasing system is shown in Fig. 2. For this system, the primary assumption is that the DAC, the S&H demultiplexer, and the electrodes are closely integrated, e.g., in monolithic or 3D integration, without strict limitations in the number of interconnects between the S&H demultiplexer and the quantum processor. Consequently, the qubits and the cryo-CMOS electronics likely operate at the same temperature. Furthermore, the following analysis assumes a cryogenic digital controller driving the DAC and a demultiplexer that operate at the same temperature, such that the thermal load of the digital control lines can be neglected [30]. Each additional channel of the demultiplexer requires an extra switch and an extra hold capacitor and adds parasitic capacitance, as highlighted in blue in Fig. 2(a), requiring a fixed area per channel that is mainly determined by the size of the switch and the hold capacitor C_H. Considerations on optimizing the S&H demultiplexer for charge injection and leakage are presented in [29], and are outside the scope of this work.

A. Refresh Time

When sampling a voltage $V_{gate,N}$ on the hold capacitor $C_{H,N}$ connected to channel N of the S&H demultiplexer, switch leakage currents $I_{s,N}$ will cause a decay of the stored voltage. This requires the electrode voltages to be periodically refreshed to ensure the voltage is in the allowed range between $V_{H,N}$ and $V_{L,N}$ [Fig. 2(a)]. For simplicity, this work assumes a decreasing voltage droop from $V_{H,N}$ to $V_{L,N}$; a similar argument applies to an increasing voltage droop. The maximum allowed refresh time for electrode N is then:

$$t_{ch,N} = \frac{C_{H,N}}{I_{s,N}}(V_{H,N} - V_{L,N}). \quad (1)$$

(1) suggests that the refresh time is channel-dependent, since some electrodes may allow for a larger voltage droop or suffer from more leakage $I_{s,N}$, e.g., as the switch leakage may depend on $V_{gate,N}$ [29], [31]. The refresh time for all electrodes combined, t_{ch}, can then be set by the minimum $t_{ch,N}$ or, alternatively, the electrodes can be combined into different groups depending on the electrode requirements or bias-voltage level, enabling various biasing strategies to be devised. Generally, the maximum size of the hold capacitor C_H is limited by the total area occupation, while the minimum size of C_H is constrained by the allowed kT/C noise and voltage droop due to leakage. Recently published cryo-CMOS demultiplexers have been able to achieve low leakage

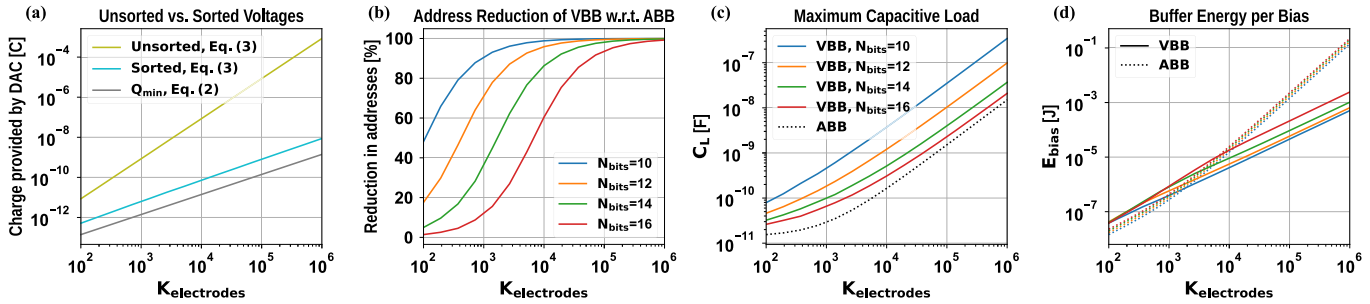

Fig. 3. Scaling properties of various biasing schemes. The simulations assume a distribution of electrode voltages following a normal distribution with 1.5 V mean and σ = 50mV, comparable to [17], using a 3 V DAC range with N_{bits} resolution, C_H = 14pF and $V_{H,N} - V_{L,N}$ = 100μV. (a) Charge provided by the DAC with N_{bits} = 16. (b) Reduction in addresses when using voltage-based biasing (VBB) compared to address-based biasing (ABB) as the number of electrodes in the system grows. (c) Maximum capacitive load that needs to be driven by the DAC caused by the eventual connection of multiple electrodes simultaneously when using VBB. (d) Energy required to bias the electrodes based on the buffer requirements.

rates dV_{gate}/dt below 1 μV/s when using C_H capacitors from 2 pF to 6 pF [14], [24], suggesting leakage currents in the order of $\sim$ 1 aA due to the switches and allowing for a refresh period beyond 1 s. In this work, a C_H of 14 pF is targeted which could lead to refresh periods of more than 20 minutes for $V_{H,N} - V_{L,N}$ = 100μV and assuming a similar $\sim$ 1 aA leakage current.[1] Ideally, t_{ch} is designed to be as long as possible to reduce the power dissipation of the electrode biasing: The refresh occurs periodically, and the active electronics can idle to reduce power dissipation, e.g., they can be disabled for > 99% of the time. Combined with the reduced leakage currents at cryogenic temperatures [32], the combined power dissipation for biasing and idling can be very low.

B. Required Electrode Charge

When an electrode needs to be refreshed, the minimum charge that needs to be provided by the DAC is:

$$Q_{min,N} = (V_{H,N} - V_{L,N})C_{H,N}. \tag{2}$$

Although this charge may be extremely small, thus indicating a negligible impact on the power consumption, the charge in the parasitic capacitance C_P at the input of the demultiplexer may be significant, as C_P scales with the total number of channels K. Each channel contributes a parasitic capacitance $C_{P,u}$ due to the increased interconnect and the added switch, so that $C_P = KC_{P,u} + C_{DAC}$, where C_{DAC} is the DACs output capacitance. Assuming that C_H = 14 pF occupies $\approx$ 70 μm $\times$ 70 μm, $C_{P,u}$ is estimated to be $\sim$ 15 fF.[2] Considering C_P, the charge provided by the DAC is then

$$Q_{DAC,N} = (V_{H,N} - V_{L,N})C_{H,N} + (V_{H,N} - V_{H,N-1})C_P, \tag{3}$$

where $V_{H,N-1}$ is the previous DAC output voltage just before the refresh and $Q_{DAC,N}$ is the charge that needs to be provided by the DAC. For simplicity, two scenarios can be considered: 1) the demultiplexer has a small number of electrodes, i.e., $K \ll 1000$, such that $C_P \ll C_H$, or 2) the demultiplexer has a large number of electrodes and the parasitic capacitance is significant, i.e., $K > 1000$, such that $C_P \gtrsim C_H$.

In the first case ($C_P \ll C_H$,) the charge redistribution between C_H and C_P is negligible and (3) can be simplified to (2), thus requiring a refresh charge mostly independent of $V_{H,N-1}$ and C_P. Since little charge needs to be added to the electrode, the charge can be driven to the electrode with active and passive DAC architectures, e.g., with a charge-redistribution capacitive DAC, as shown in [15]. To ensure that the parasitic capacitance remains smaller than the hold capacitor as the number of electrodes in the system grows larger, separate DACs, with the relative S&H demultiplexer, may be added.

In the second case ($C_P \gtrsim C_H$), i.e., for demultiplexers with many channels sharing a single DAC, connecting the DAC to a S&H channel for refreshing causes charge redistribution with a stronger dependency on $V_{H,N-1}$ and C_P following (3). To minimize the dissipated charge, the electrode voltages can be sorted in increasing or decreasing order, such that V_{DAC} increases or decreases monotonically during the refreshing process to minimize the second term in (3), as shown in Fig. 2(b). Sorting the voltages is crucial when the number of electrodes grows and Fig. 3(a) plots the charge provided by the DAC for an increasing number of electrodes. The required charge scales quadratic with the number of electrodes (K^2) for unsorted voltages, while using sorted voltages scales linearly with K, similar to $K \cdot Q_{min,N}$ of (2). Hence, voltage sorting serves as a best practice since it reduces switching losses, especially as K grows large, e.g., the DAC needs to provide 1000$\times$ less charge for K = 10,000, resulting in even larger energy savings [33].

C. Electrode Addressing

The most straightforward way to address the electrodes is *address-based biasing* (ABB): the controller sequentially communicates the address of each electrode to the demultiplexer via D_{DEMUX} and in parallel drives the DAC to generate the respective voltage level as shown in Fig. 2(c). After all electrodes have been addressed, the DAC can idle until the next refresh cycle to reduce power dissipation. For a given clock frequency, the time required to bias all the electrodes, $t_{bias,a}$, scales linearly with the number of electrodes. Consequently, for a given refresh time t_{ch}, having a larger t_{bias} results in a lower idle time t_{idle} as $t_{ch} = t_{bias,a} + t_{idle}$, causing the DAC to be on for a longer period of time and resulting in more dissipation.

As an alternative to address-based biasing, *voltage-based biasing* (VBB) can be adopted to reduce t_{bias}. With voltage-based biasing, the bias controller drives the DAC to generate a given voltage and, in parallel, communicates the voltage

[1] In practice, larger bias voltages may affect the leakage currents present, and the refresh period may be reduced [14], [29].

[2] Extracted parasitic capacitance of a 10 μm metal line that is connected to a minimum-sized switch, sized for minimal charge injection, and runs along one side of the square metal fringe capacitor C_H.

level via D_{DEMUX} to connect simultaneously all the demultiplexer channels that require such a voltage level, as shown in Fig. 2(c). If each electrode has a unique voltage level, voltage-based biasing and address-based biasing will result in similar t_{bias}, i.e., $t_{bias,a} = t_{bias,v}$. However, if K is comparable to the number of voltage levels of the DAC ($N_{voltages}$), significant reduction of addresses (beyond 75%), and hence time, can be achieved as shown in Fig. 3(b), depending on the voltage distribution. Since this work targets a large number of electrodes, a large reduction is expected such that $t_{bias,a} \gg t_{bias,v}$. Consequently, if the electrodes can be connected to the DAC simultaneously, iterating over the voltages will require less time, since any electrode requiring the same voltage code can be connected simultaneously in a single clock cycle, and dissipate less energy for driving D_{DEMUX}, since less digital lines with a capacitive load similar to C_P need to be driven.[3] Furthermore, the DAC resolution fixes the upper limit of $t_{bias,v}$ while $t_{bias,a}$ continues to scale with the number of electrodes of the demultiplexer and improvements to the uniformity of quantum dots will result in a reduction in $N_{voltages}$ and hence $t_{bias,v}$.

In essence, both ABB and VBB require the same hardware for each additional electrode: registers to store the voltage required for a particular address, slightly more complex decoders to read and write the voltage levels for each address and to drive the S&H switch; these elements could be centrally located in the bias controller for ABB, while VBB may benefit from placing the registers closer to the S&H switch. The main disadvantage of voltage-based biasing is that the DAC needs to drive a variable capacitive load C_L, since depending on the voltage code, C_L might vary anywhere between C_P and C_P+gC_H when g electrodes require the same bias voltage. The simulated capacitive load is plotted in Fig. 3(c), which shows that when fewer voltage levels are present, i.e., the DAC has lower N_{bits}, C_L for VBB is larger compared to ABB since more electrodes are connected simultaneously, while C_L for both ABB and VBB scales similarly as the number of electrodes increases. Even though the capacitive load may be larger for VBB with lower N_{bits}, the required energy per bias cycle can be 100× lower for larger K due to the reduced t_{bias} as shown in Fig. 3(d). Fig. 3(d) estimates the energy required for biasing all the electrodes by estimating the power dissipation of a buffer based on the required settling for N_{bits} and driven maximum capacitive load [34] and multiplying it with t_{bias} [33]. For a low number of electrodes, VBB requires slightly more energy due to the increased C_L, but as the number of electrodes grows, the energy required for ABB scales proportionally to K^2 as both t_{bias} and C_L keep increasing. Consequently, voltage-based biasing is attractive thanks to the shorter t_{bias}. Combining voltage-based biasing with sorted voltages simply requires the generation of a uniform voltage ramp spanning the full voltage range and stepping over all the DAC LSBs.

III. Circuit Implementation

Efficient, scalable biasing of a large S&H demultiplexer requires a DAC able to drive a large capacitive load while generating a ramp over a large 3 V range with sub-100 μV LSB steps, and ensuring monotonicity and low power dissipation. Such a voltage ramp can easily be generated with an integrator supplied with a constant input voltage [35]. Hence, this work proposes an integrating-DAC architecture that is inherently monotonic due to its integrating nature, simplifying its design and eliminating the need for additional calibration techniques to address the increased mismatch at cryogenic temperatures [15], [25], [36]. Although the circuit could only be simulated for RT operation, the design is optimized for cryogenic operation by taking into account the expected device parameter variations, e.g., higher threshold, lower thermal noise, higher mobility [32], [36], and by adopting the design techniques and sizing described in the following. The integrating DAC is implemented as a non-inverting switched-capacitor integrator (SC-integrator) as shown in Fig. 4, where the switched-capacitor nature of the integrator simplifies the timing synchronization between the DAC and demultiplexer. Even though the integrator could operate at very low frequencies thanks to the low required refresh rate presented in Section II-A, the nominal operating speed of the integrator is set at 62 kHz, such that a full ramp is generated within 1 s, so as to limit the characterization time and to mitigate the eventual effect of leakage currents.

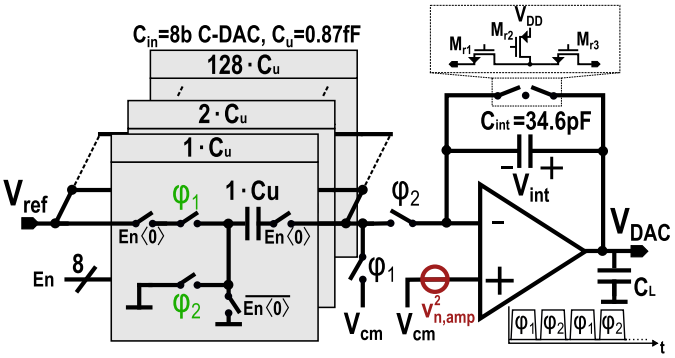

Fig. 4. DAC implemented as an SC-integrator with variable input C-DAC. The labeled clock phases are used for non-inverting integration, while the clock phases inside the C-DAC (highlighted in green) are swapped when inverting integration is needed.

To further reduce the DAC on-time and hence reduce the power consumption, it would be advantageous to speed up the ramp for specific unused output ranges, since not all voltage levels in the generated ramp may be needed for biasing electrodes. To implement such functionality, the input capacitor C_{in} is implemented as an 8-bit C-DAC, as shown in Fig. 4. This allows dynamic switching between a large C_{in} to create larger voltage steps during the ramp and a small C_{in} when smaller voltage steps are required to achieve the target resolution (*gear-shifting*). Gear-shifting enables skipping DAC voltage codes not required by any electrodes, reducing the operation time and integration cycles. Ideally, a large C_{in} should be used to minimize integration cycles, and a small C_{in} should only be used in small sections of the ramp where electrodes require finer voltage control. Since the electrodes are calibrated using the generated ramp, the primary consideration is avoiding missing codes and the matching for the C-DAC implementing C_{in} is relaxed.

A. SC-Integrator

In the non-inverting SC-integrator in Fig. 4, the reference voltage V_{ref} is sampled on the input capacitor C_{in} with respect to the common mode V_{cm} during ϕ_1 and integrated on the integration capacitor C_{int} during ϕ_2. The positive input of the differential amplifier is connected to V_{cm}=0.3V, which

[3]The address space for addressing the voltages can be represented with less bits if the number of electrodes is very large.

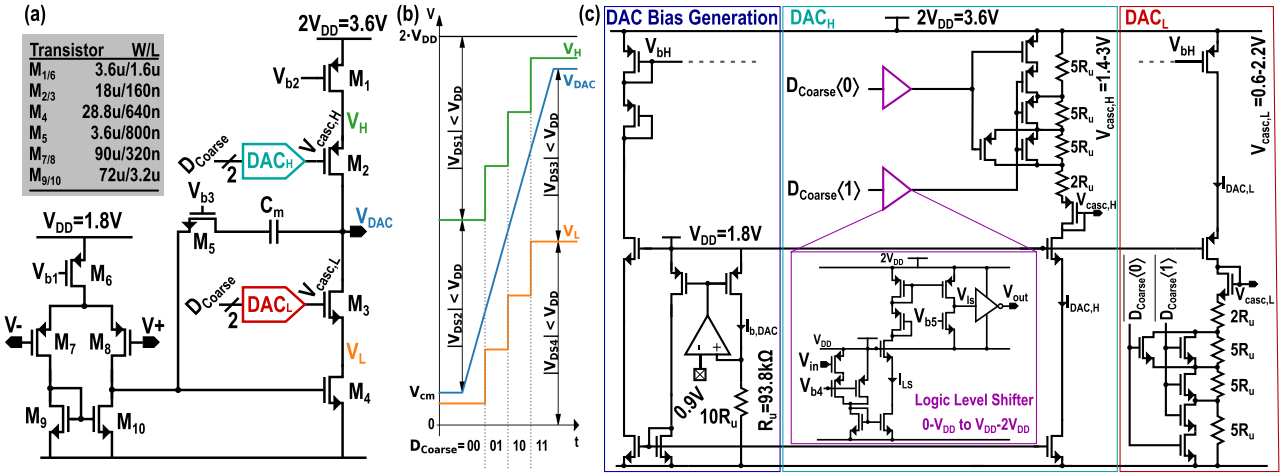

Fig. 5. (a) Miller-compensated amplifier with high-voltage output stage and transistor sizing. (b) Coarse DAC switching to ensure limited drain-to-source voltage on $M_1 - M_4$. (c) Coarse DAC implementation with reference generation and additional transistors ensuring reliability.

provides the lower bound of the DAC's output range, and it is chosen high enough to relieve the constraints on input common-mode range of the amplifier. The output during ϕ_2 can then be approximated by

$$V_{int}[M] = \frac{\frac{C_{in}}{C_{int}} V_{ref} - V_{cm}\frac{C_{in}}{C_{int}}\frac{1}{A+1} + V_{int}[M-1]}{1 + \frac{C_{in}}{C_{int}}\frac{1}{A+1}} \quad (4)$$

$$V_{DAC}[M] = \frac{A}{A+1} V_{int}[M] + \frac{A}{A+1} V_{cm}, \quad (5)$$

where M is the number of integration cycles, A is the amplifier DC gain, and V_{int} is the voltage across C_{int}. The term $V_{ref}(C_{in}/C_{int})$ determines the voltage step at the output of the integrator, setting the resolution of the ramp, while the output range can be increased by using more integration cycles and is only limited by the amplifier output range. According to (4) and (5), high DAC linearity can be achieved as long as A is sufficiently large. This work then requires A> 82 dB for INL< 1 LSB.

Similar to the output voltage, the output noise on V_{DAC} accumulates, so that the output noise after M cycles is given by:

$$v^2_{n,DAC}[M] \approx \frac{q^2_{n,int}[M]}{C^2_{int}} + \frac{kT}{C_{int}} + \rho\frac{kT}{C_m}\left(1 + \frac{C_{in}}{C_{int}}\right) \quad (6)$$

where the first term represents the charge noise accumulated in C_{int}, the second term represents the initial kT/C noise of resetting the integrator, and the third term is a simplified expression for the integrated white noise of the amplifier $v^2_{n,amp}$, which has noise excess factor ρ and is assumed to be bandwidth limited by the Miller capacitance C_m [Fig. 5(a)] [37]. The charge noise accumulating on C_{int} can be described by:

$$q^2_{n,int}[M] \approx MkTC_{in} + (M-1)\rho\frac{kT}{C_m}C^2_{in}, \quad (7)$$

and includes the noise sampled on C_{in} in ϕ_1 and the noise that is sampled on C_{int} when opening the switches during ϕ_2, which is assumed to be dominated by $v^2_{n,amp}$. The large voltage output range limits the use of commonly adopted offset compensation techniques since the C_{int} path cannot be easily switched. Hence, the amplifier input stage is sized at RT for sufficiently low 1/f noise in the 1 Hz to 10 MHz bandwidth, as the 1/f noise is expected to remain similar when operating at cryogenic temperatures [38], [39]. Similarly, shot noise will remain, resulting in a limited noise reduction when moving to cryogenic temperatures [40]. Consequently, C_m = 34.8pF is used with ρ = 2.5, leading to $v^2_{n,amp} \approx 19\ \mu V_{rms}$. Based on (6, 7), a maximum V_{ref} = 1.8V is chosen so that the ratio C_{in}/C_{int} can be minimized for lower noise. Then, to limit $v^2_{n,DAC}$ for M = 10,000 to below 100 μV_{rms} in this design, a large C_{int} = 34.6pF is used at the expense of increased area.

Since the DAC targets a 3 V output range, which exceeds the nominal V_{DD}=1.8V for thick-oxide devices in the adopted 22-nm FinFET technology, it is non-trivial to implement the output range. For V_{cm} = 0.3V, V_{DAC} can range from 0.3 V to 3.3 V. To ensure reliability, the design exclusively uses thick-oxide devices and avoids violating any voltage compliance, e.g., drain-to-source voltages V_{DS} or gate-to-source voltages V_{GS} exceeding 1.8 V. Drain/source-body junctions are not a concern thanks to their higher breakdown voltage. A dedicated high-voltage output stage of the amplifier ensures the amplifier can generate outputs above 1.8 V (see section III-B), while the integration capacitor, which has a higher compliance voltage, can shield the input of the amplifier from the high voltage at V_{DAC}. However, the reset switch for C_{int} presents a problem, since V_{int} increases to 3 V during integration. Consequently, the reset switch is implemented with the transistors M_{r1-3}. During operation, when V_{DAC}< 1.8V, the gates of $M_{r1,3}$ are connected to ground and the gate of M_{r2} is connected to V_{DD}, turning it off. When V_{DAC} exceeds 1.8 V, the gate of M_{r3} is connected to V_{DD} and the gate of M_{r2} is connected to ground, so that the shared node between M_{r1-3} is biased to V_{DD}. By doing so, M_{r3} will still be turned off with a $V_{GS} \leq 0$, but this allows for V_{DAC} to increase up to 3.6 V without the V_{DS} or V_{GS} of M_{r3} exceeding 1.8 V. To reset the integrator, the clock phases driving the C-DAC (see green labels in Fig. 4) are swapped to perform inverting integration and reduce V_{DAC}. Then, when the output V_{DAC} is sufficiently below 1.8 V, $M_{r1,3}$ can both be connected to V_{DD} to fully discharge C_{int}.

B. High-Voltage Amplifier

To enable the amplifier reliably generating voltages between 0.3 V to 3.3 V, the amplifier is implemented as a 2-stage Miller amplifier with an output stage that operates with a 3.6 V supply as shown in Fig. 5(a). To improve the reliability of the

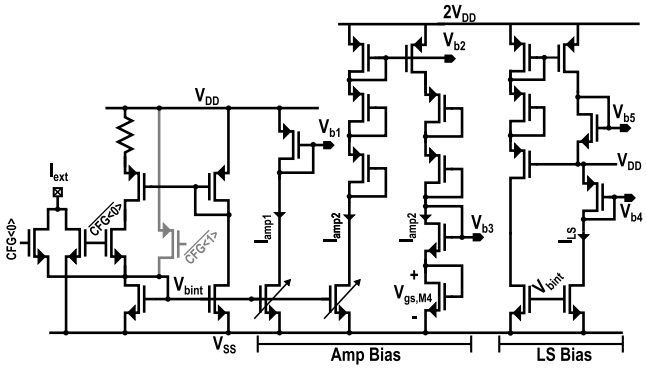

Fig. 6. Bias generation for the Miller compensated amplifier (Amp Bias) and logic level shifter (LS Bias). The pull-up transistor in gray can be used to start-up the circuit.

high-voltage output stage, the transistors $M_{1,4}$ should have V_{DS} and V_{GS} below 1.8 V. Therefore, cascode transistors M_2 and M_3 are added, which are dynamically biased by coarse DACs (DAC_H and DAC_L). Effectively, this sets the node voltages V_L and V_H, and, as the voltage at node V_{DAC} increases, V_L and V_H should coarsely track the output as illustrated in Fig. 5(b). The coarse DACs only require two bits to ensure that no transistor has a $V_{DS} > V_{DD}$ during operation, and can switch based on the stepsize and the integration cycle.

The bias generation for the high-voltage output stage and the logic level shifter [Fig. 5(c)] is shown in Fig. 6. A switchable constant-g_m circuit allows for generating an on-chip bias current or using an off-chip bias current. To start up the reference circuit, a pull-up transistor can be enabled. The resulting current is distributed to the two amplifier stages with the branches I_{amp1} and I_{amp2}, which are programmable with a 5-bit and 7-bit current DACs, respectively. Since V_{b2} is referred to the $2V_{DD}$ supply, additional diode-connected transistors are added to limit the V_{DS} voltages of the individual transistors. Finally, the amplifier has a Miller capacitance C_m and a Miller resistance to improve the stability. The Miller resistance is implemented with a transistor [M_5, Fig. 5(a)] to ensure reliable operation down to cryogenic temperatures, where the threshold voltage and mobility increase [32], [36] cause both the transconductance and on-resistance to change. By biasing M_5 with a voltage of $\sim 2(V_{OV4} + V_{th})$ as shown in Fig. 6, the transconductance of M_4 and on resistance of M_5 change similarly, allowing for stable operation, even at cryogenic temperatures [41].

For integrator operation at 62 kHz, the amplifier is designed to have > 500 kHz unity-gain bandwidth at RT to provide a robust $> 20\tau$ settling while driving a nominal load capacitance of 500 pF, leading to a simulated power dissipation of 108 μW from the V_{DD} and $2V_{DD}$ supplies. The load capacitance creates a pole at the output that may cause instability. Thus, to ensure the robustness of the design, the amplifier is designed to remain stable across a wide range of load capacitances, with the phase margin remaining above 80° for load capacitances from 200 pF to 800 pF. The DC gain and the bandwidth of the amplifier have been sized to limit the non-linearity of the DAC to INL < 1 LSB. Room-temperature simulations show an amplifier gain larger than 90 dB for an output voltage range between 0.3 V and 3.3 V, which exceeds the 82-dB requirement mentioned in Section III-A. While a gain-bandwidth product (GBW) of ~ 180 kHz would ensure a similar linearity performance, the simulated GBW was designed to exceed 500 kHz for the target output-load range, so as to make settling-induced non-linearity negligible.

C. Coarse DACs

During operation, node V_H and V_L must be accurately biased to ensure that transistors M_{1-4} are all in saturation, since large variations in the gain could change the integrator step size and limit the linearity. To bias V_H and V_L in a PVT-robust manner, the coarse DACs shown in Fig. 5(c) are used. Depending on the code D_{coarse}, V_H and V_L need to be biased between 1.8 V to 3.4 V, and 0.2 V to 1.8 V, and similar voltages needs to be generated across the resistive ladders in DAC_H and DAC_L, respectively. The cascodes M_2 and M_3 in the output stage shift the V_H/V_L voltages by V_{GS}; hence, a diode-connected transistor is cascoded to the resistive ladder in DAC_H and DAC_L to reduce the sensitivity to the transistor parameters, such as V_{th}. For biasing DAC_H and DAC_L, A feedback loop regulates a reference voltage across a resistor matched to the resistor ladder, and the resulting current $I_{b,DAC}$ is distributed to the coarse DACs to generate PVT-insensitive output voltages. The coarse DAC output voltages, $V_{casc,L}$ ($V_{casc,H}$), are between 0.2 V + V_{GS} ≈ 0.6V to 1.8 V+V_{GS} ≈ 2.2V (1.8 V−V_{GS} ≈ 1.4V to 3.4 V−V_{GS} ≈ 3V), requiring both DACs to operate with an increased supply. Therefore, the same 3.6 V supply of the output stage is also used for the coarse DACs. To prevent excessive V_{DS} across devices in the coarse-DAC bias generation, additional diode-connected transistors and cascode transistors connected to V_{DD} are added.

The resistors in DAC_H and DAC_L are switched using two control bits D_{Coarse}. For DAC_L, these can be driven directly by a 0-1.8 V logic signal, while DAC_H requires the logic levels to be shifted from 0-1.8 V to 1.8-3.6 V. Fig. 5(c) shows the logic level shifters that implement this functionality, differing from conventional level shifters that would exceed their voltage compliance in this scenario [42]. The logic level shifter mirrors a current from the 0-1.8 V domain to the 1.8-3.6 V domain. When V_{in} is high, I_{LS} is a small current that ensures that the transistors in the I_{LS} branch still meet the voltage compliance while V_{ls} is low. When V_{in} is low, the I_{LS} current increases and causes V_{ls} to increase, triggering the cascaded inverter and hence level shifting the incoming digital signal. As in the coarse DAC, voltage compliance in the I_{LS} branch is ensured by using cascode transistors connected to V_{DD} and diode-connected transistors.

IV. Measurement Results

The DAC has been fabricated in a 22-nm FinFET process using 1.8-V I/O thick oxide devices, and has been characterized at room temperature (RT) and 4.2 K by placing the chip on a sample PCB at the bottom of a dipstick [43], using the measurement setup in Fig. 7. For characterization at 4.2 K, the sample is immersed in liquid helium, which is a good indication of the performance below 100 mK, since no significant changes in transistor characteristics are expected [44].[4] Measurement data and post-processing routines can be found in [33], and extensive testing and biasing using a modified version of the DAC together with a S&H demultiplexers and

[4]Particular thin-film resistors could become superconducting as in [45], but using other resistor types or exceeding the critical current could avoid this issue.

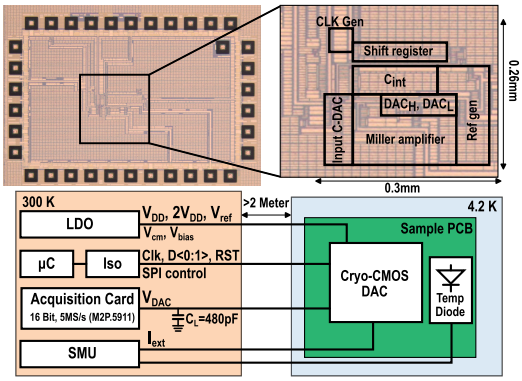

Fig. 7. Die micrograph of the cryo-CMOS DAC and measurement setup.

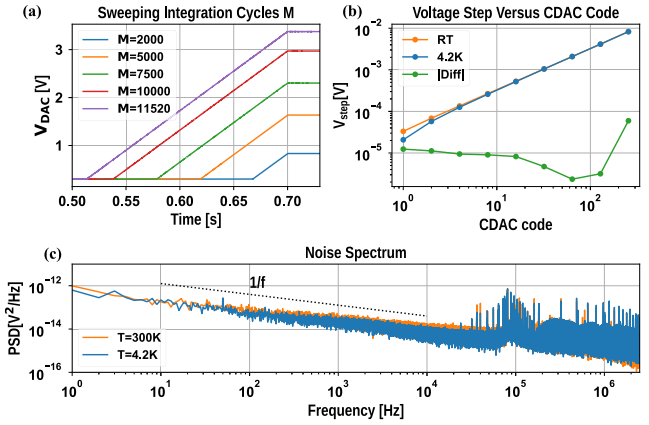

Fig. 8. (a) Running the integrating DAC with increasing number of integration cycles (RT) with $C_{in} = 8C_u$. (b) Stepsize V_{DAC} versus input C_{in} at both RT and 4.2 K. (c) Noise spectrum measured at the output.

quantum devices at mK temperatures can be found in [29]. The transient output of the DAC is measured with an 16-bit 5 MS/s acquisition card, connected to the DAC output by a coaxial cable that acts as a 480 pF load capacitance. This C_L, together with the $C_{P,u}$ of ~ 15 fF (Section II), suggests that the DAC can drive a demultiplexer consisting of more than 30,000 electrodes. The DAC is operated with a clock frequency of 62 kHz and uses a reference voltage V_{ref} = 1.8V, which could be supplied by a voltage reference in future iterations [35]. The continuous DAC power dissipation at 4.2 K is 157 μW, which is sufficiently low to continuously operate the DAC below 100 mK in a dilution refrigerator [29]. In practice, power dissipation can be much lower by idling the DAC between biasing cycles (Section II). During operation, D_{coarse} increments at the MSB and MSB-1 steps in accordance with Fig. 5(b).

Typical operation is plotted in Fig. 8(a), showing that the DAC can reach voltages up to 3.4 V, thus meeting the range requirement of 0.3 V to 3.3 V. In the following characterization, the range is limited to 0.3 V to 3.3 V since the performance of the integrator might degrade outside this range due to the lower amplifier gain.

Fig. 8(b) shows the step size at the output V_{DAC} as a function of C_{in}. Depending on the setting of C_{in}, an output stepsize of 0.02 mV to 8.3 mV can be measured at both 4.2 K and RT. The difference in the step size at RT and 4.2 K does not change significantly when moving to cryogenic temperatures, illustrating the robustness of the architecture

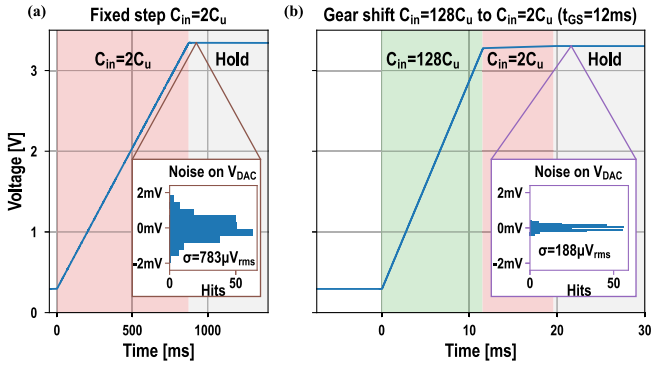

Fig. 9. Operation of the switched capacitor integrator at 4.2 K (a) without and (b) with gear shifting, respectively. The insets show the standard deviation of the measured noise [28].

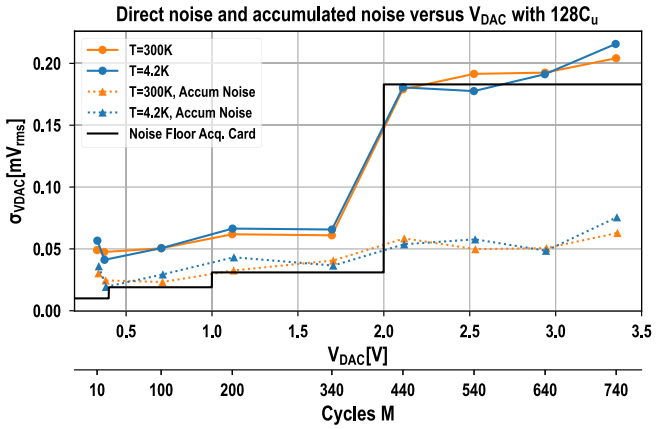

Fig. 10. Measured noise using the acquisition card for $C_{in} = 128C_u$.

across temperature. The measured difference, while small, could be attributed to an reduction in charge injection at CT due to the increased threshold voltage [44].

A. Noise

The noise spectrum of the amplifier is shown in Fig. 8(c) and the 1 Hz-2.5 MHz integrated noise is equal to 44 μV_{rms} (44 μV_{rms}) at 4.2 K (RT). Both noise spectra show interferers around 90 kHz, which increases the noise compared to simulation and are coupled into the system due to the long wiring. Furthermore, the low-frequency noise remains at a similar level when comparing the PSD of 4.2 K and RT [38].

Fig. 9(a) shows the output sampled noise is 783 μV_{rms} at 4.2 K after 46,000 integration cycles. When gear shifting as introduced in Section II, the number of integration cycles, and hence the noise on $q^2_{n,int}[M]$ in (7) can be reduced. This is shown in Fig. 9(b) where during the first 12 ms, C_{in} is set to $128C_u$ to reach 3.27 V, after which the $2C_u$ setting is used to generate voltages with a small step in the range 3.27 V to 3.3 V. Using gear shifting, the time required to reach the maximum voltage is reduced from 800 ms to 20 ms while also the measured integrated noise reduces from 783 μV_{rms} to 188 μV_{rms} due to the reduction in integration cycles.

Further characterization of the noise as a function of integration cycles is shown in Fig. 10. For measuring the noise, statistics of 250 traces are captured for each of the output voltages. The captured traces are processed in two ways. The first approach (*single-shot*) computes the standard deviation at

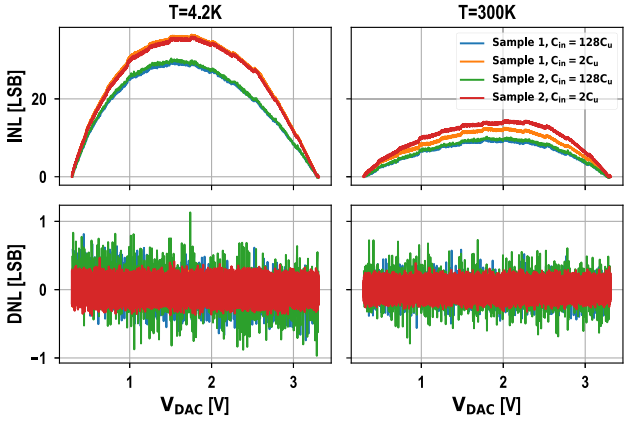

Fig. 11. DAC linearity measured for two different samples [28].

a particular time at the end of the generated ramp, as also used in Fig. 9. This approach includes all the noise terms from (6), including the noise sampled on C_{int} and the time-varying noise from the amplifier, in addition to the acquisition card noise. The second approach first averages multiple acquisition-card samples of the DAC output held at the end of the *same* trace, and then computes the standard deviation of these averages across *multiple* traces. This averages out the high-frequency noise from the acquisition card and the amplifier, and enables a more accurate measurement of the accumulated noise in the integration capacitor [$q^2_{n,int}[M]$ in (7)].

Fig. 10 shows both the measured single-shot and accumulated noise versus the number of integration cycles at both 4.2 K and RT. For single-shot measurements, a noise of 216 μV_{rms} (204 μV_{rms}) is measured at 4.2 K (RT) for M = 740, matching well with the single-shot noise of the gear shift measurement [Fig. 9]. It becomes clear that the noise is dominated by the noise floor of the acquisition card at voltages > 2 V due to the clear step increase in measured noise. The measured accumulated noise measures an accumulated noise of 76 μV_{rms} (63 μV_{rms}) at 3.3 V, which is likely a more accurate representation of the noise at the output. The noise increases proportional to $M^{0.8}$ instead of $M^{0.5}$ for white noise, suggesting that interferers or noise correlation is affecting the noise performance.

B. Linearity

The linearity of the DAC for two different samples at both 4.2 K and RT is shown in Fig. 11. The linearity has been computed by measuring 250 ramps, averaging them to remove the noise, taking equally sampled points along this ramp based on the number of integration cycles and comparing this to a fully linear slope in the range 0.3 V to 3.3 V. The linearity is measured for two different input capacitances, C_{in} = 128C_u and C_{in} = 2C_u, to show the range of nonlinearity of the DAC. The measured LSB step of 57.1 μV (68.3 μV) is set by C_{in} = 2C_u. This measurement captures both linearity of the DAC and acquisition card, the latter visible in the repeated ripples every 250 mV in the INL curve of Fig. 11. While the DNL of the SC-integrator is monotonic and seems mostly flat, the parabolic INL shape suggests a linear decay in the DAC step as the output voltage increases. The two samples that have been measured show similar INL curves, suggesting the source of the non-linearity is systematic. Time-dependent or leakage effects would not explain the observed systematic non-linearity, since the operation between 128C_u and 2C_u have

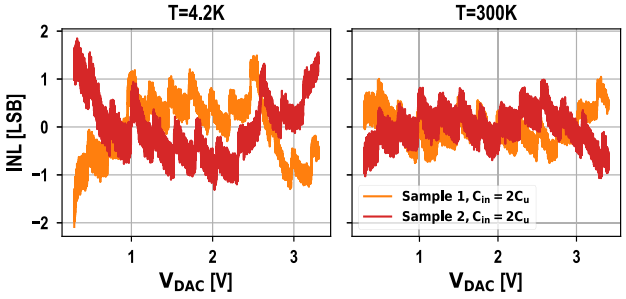

Fig. 12. INL after individual gain and offset calibration and higher-order systematic non-linearity removal.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON TABLE

Biasing DACs	**This work**		[15]	[25]	[27]
Technology [nm]	22		65	65	180
Qubit type	Spin		Spin	Spin	Ion trap
Temperature [K]	300	4	6	4	4.2
Output Range [V]	3		1	1.2	26
Avg. V_{lsb} [μV]	68.3	57.1	122.1	4.58	12.2×10^3
Noise [μV_{rms}]	192 (63$^\$$)	188 (76$^\$$)	N.A.	2.6‡	1.617 nV/$\sqrt{\text{Hz}}^\dagger$
INL [LSB]	12.6 (1.1$^\&$)	36.5 (2.1$^\&$)	N.A.	0.8	0.5
DNL [LSB]	0.6	0.8	2.5*	0.8	1.6
Refresh Rate [Hz]	1		3900	N.A.	12000
Maximum C_{Load} [pF]	480		N.A.	N.A.	N.A.
Supply [V]	1.8 & 3.6		1.1 & 2.5	1.2	-12, -7 & 16
Power [μW]	138	157	21.1	52.1	68.6×10^3
Core Area [mm^2]	0.076		0.14	0.377	9.553

$^\$$Integrated noise @ 3.3 V ‡Integrated 1Hz - 50kHz †Spot noise at 500 kHz @ 300 K
*Estimated from figure $^\&$ Calibrated

similar INL trends while having a 64× increase in operation time, while additional measurements with slower clock also show similar INL. Instead, using (4) to model the ramp, the behavior corresponds to a reduced amplifier gain of 50 dB (60 dB) at 4.2 K (RT), where the difference between the simulated gain and the gain predicted form the measurements is attributed, in addition to the uncertainties related to the lack of cryogenic-validated models, to inaccuracy of the device models. Indeed, the adopted devices are thick-oxide transistors operating at a supply voltage double than the nominal 1.8 V supply, at which the simulation models are rated. Without any calibration of the non-linearity, the integrating DAC achieves an INL of 36.5 LSB (12.6 LSB) and DNL of 0.8 LSB (0.6 LSB) at 4.2 K (RT). As the quantum devices to be biased require significant calibration, this non-linearity is acceptable, as it can be calibrated out together with the quantum-device non-idealities without incurring additional costs [29]. The non-linearity visible in the two samples can be corrected by a 2-point calibration of each sample to remove offset and gain error, and by applying a 5th-order polynomial correction, equal for both samples. The residual error is shown in Fig. 12 and shows that calibration improves the INL to 2.1 LSB (1.1 LSB) at 4.2 K (RT).

The measured performance is reported in Table I. Compared to the prior work targeting semiconductor spin qubits, a high resolution, larger output range, and monotonic linearity are achieved. Additionally, out of all the presented DACs, this work has the smallest footprint, can drive a large capacitive load, and presents an extensive characterization of its linearity and noise.

V. CONCLUSION

This work investigates a DAC for scalable biasing of the electrodes in semiconductor quantum processors using a S&H

demultiplexer. The system analysis suggests that 1) the DAC needs to drive a large capacitive load when the quantum processor grows large, 2) switching losses during biasing can be reduced by sorting the voltages that need to be generated, and 3) the time required for generating the bias voltages can be reduced by using voltage-based addressing. Following these considerations, this work demonstrates an integrating DAC architecture implemented in a 22-nm FinFET technology. The integrating DAC consists of a non-inverting switched-capacitor integrator that inherently offers monotonicity. To meet the large output swing requirements exceeding the nominal supply voltage, the output stage operates from a $2V_{DD}$ supply, thus requiring dynamic biasing to ensure high reliability. At 4.2 K and over a 0.3 V to 3.3 V output range, the DAC demonstrates a 57.1 μV step size, 192 μV_{rms} single-shot sample and 76 μV_{rms} accumulated noise, an INL of 36.5 LSB and monotonic DNL. The DAC can drive a large capacitive load up to 480 pF while dissipating only 157 μW, thus enabling the bias of more than 30,000 electrodes when operating at mK-temperatures, as needed for future large-scale semiconductor-based quantum processors.

REFERENCES

[1] A. R. Mills et al., "High-fidelity state preparation, quantum control, and readout of an isotopically enriched silicon spin qubit," *Phys. Rev. Appl.*, vol. 18, no. 6, Dec. 2022, Art. no. 064028.

[2] X. Xue et al., "Quantum logic with spin qubits crossing the surface code threshold," *Nature*, vol. 601, no. 7893, pp. 343–347, Jan. 2022.

[3] L. Petit et al., "Universal quantum logic in hot silicon qubits," *Nature*, vol. 580, no. 7803, pp. 355–359, 2020.

[4] C. H. Yang et al., "Operation of a silicon quantum processor unit cell above one Kelvin," *Nature*, vol. 580, no. 7803, pp. 350–354, Apr. 2020.

[5] L. C. Camenzind, S. Geyer, A. Fuhrer, R. J. Warburton, D. M. Zumbühl, and A. V. Kuhlmann, "A hole spin qubit in a fin field-effect transistor above 4 Kelvin," *Nature Electron.*, vol. 5, no. 3, pp. 178–183, Mar. 2022.

[6] A.-M. Zwerver et al., "Qubits made by advanced semiconductor manufacturing," *Nature Electron.*, vol. 5, no. 3, pp. 184–190, 2022.

[7] L. M. K. Vandersypen et al., "Interfacing spin qubits in quantum dots and donors—Hot, dense, and coherent," *npj Quantum Inf.*, vol. 3, no. 1, p. 34, Sep. 2017.

[8] B. Patra et al., "Cryo-CMOS circuits and systems for quantum computing applications," *IEEE J. Solid-State Circuits*, vol. 53, no. 1, pp. 309–321, Jan. 2018.

[9] X. Xue et al., "CMOS-based cryogenic control of silicon quantum circuits," *Nature*, vol. 593, no. 7858, pp. 205–210, 2021.

[10] J. Yoo et al., "Design and characterization of a <4-mW/qubit 28-nm cryo-CMOS integrated circuit for full control of a superconducting quantum processor unit cell," *IEEE J. Solid-State Circuits*, vol. 58, no. 11, pp. 3044–3059, Nov. 2023.

[11] S. Chakraborty et al., "A cryo-CMOS low-power semi-autonomous transmon qubit state controller in 14-nm FinFET technology," *IEEE J. Solid-State Circuits*, vol. 57, no. 11, pp. 3258–3273, Nov. 2022.

[12] K. Kang et al., "A cryo-CMOS controller IC with fully integrated frequency generators for superconducting qubits," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 65, Feb. 2022, pp. 362–364.

[13] J. Anders et al., "CMOS integrated circuits for the quantum information sciences," *IEEE Trans. Quantum Eng.*, vol. 4, pp. 1–30, 2023, Art. no. 5100230.

[14] S. J. Pauka et al., "A cryogenic CMOS chip for generating control signals for multiple qubits," *Nature Electron.*, vol. 4, no. 1, pp. 64–70, Jan. 2021.

[15] P. Vliex et al., "Bias voltage DAC operating at cryogenic temperatures for solid-state qubit applications," *IEEE Solid-State Circuits Lett.*, vol. 3, pp. 218–221, 2020.

[16] W. I. L. Lawrie et al., "Quantum dot arrays in silicon and germanium," *Appl. Phys. Lett.*, vol. 116, no. 8, pp. 1–8, 2020.

[17] P. L. Bavdaz et al., "A quantum dot crossbar with sublinear scaling of interconnects at cryogenic temperature," *npj Quantum Inf.*, vol. 8, no. 1, p. 86, Jul. 2022.

[18] J. Darulová, *Automated tuning gate-defined quantum dots*,Ph. D. thesis, Dept. Phys., ETH Zurich, 2020.

[19] C. J. van Diepen et al., "Automated tuning of inter-dot tunnel coupling in double quantum dots," *Appl. Phys. Lett.*, vol. 113, no. 3, pp. 1–5, Jul. 2018.

[20] R. Durrer et al., "Automated tuning of double quantum dots into specific charge states using neural networks," *Phys. Rev. Appl.*, vol. 13, no. 5, May 2020, Art. no. 054019.

[21] Bluefors.(2024). *XLDsl Dilution Refrigerator Measurement System*. [Online]. Available: url{https://bluefors.com/products/dilution-refrigerator-measurement-systems/xldsl-dilution-refrigerator-measurement-system/

[22] S. Subramanian et al., "A scalable mK cryo-CMOS demultiplexer chip for voltage biasing and high-speed control of silicon qubit gates," in *Proc. IEEE Symp. VLSI Technol. Circuits (VLSI Technol. Circuits)*, Jun. 2024, pp. 1–2.

[23] A. Ruffino, T.-Y. Yang, J. Michniewicz, Y. Peng, E. Charbon, and M. F. Gonzalez-Zalba, "A cryo-CMOS chip that integrates silicon quantum dots and multiplexed dispersive readout electronics," *Nature Electron.*, vol. 5, no. 1, pp. 53–59, Dec. 2021.

[24] L. Schreckenberg et al., "SiGe qubit biasing with a cryogenic CMOS DAC at mK temperature," in *Proc. ESSCIRC - IEEE 49th Eur. Solid State Circuits Conf. (ESSCIRC)*, Sep. 2023, pp. 161–164.

[25] Y. Li, Y. Zhang, and C. Wang, "13.4 xiling: Cryo-CMOS 18-bit dual-DAC manipulator with 4.6 v precision and 4.1nV/Hz^0.5 noise co-integrated with the single electron transistor at 60mK," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2025, pp. 228–230.

[26] J. Stuart et al., "Chip-integrated voltage sources for control of trapped ions," *Phys. Rev. Appl.*, vol. 11, no. 2, Feb. 2019, Art. no. 024010.

[27] S. Park, S. Song, K. Kim, H. Lee, M. Lee, and J.-Y. Sim, "A cryo-CMOS 64-channel bias generator IC for surface ion trap," in *Proc. IEEE Eur. Solid-State Electron. Res. Conf. (ESSERC)*, Sep. 2024, pp. 488–491.

[28] L. Enthoven, J. van Staveren, J. Gong, M. Babaie, and F. Sebastiano, "A 3 V 15b 157 μW cryo-CMOS DAC for multiplexed spin-qubit biasing," in *Proc. IEEE Symp. VLSI Technol. Circuits (VLSI Technol. Circuits)*, Jun. 2022, pp. 228–229.

[29] J. van Staveren et al., "Cryo-CMOS bias-voltage generation and demultiplexing at mK temperatures for large-scale arrays of quantum devices," *IEEE Trans. Quantum Eng.*, vol. 6, pp. 1–19, 2025.

[30] S. Krinner et al., "Engineering cryogenic setups for 100-qubit scale superconducting circuit systems," *EPJ Quantum Technol.*, vol. 6, no. 1, p. 2, Dec. 2019.

[31] J. M. Boter et al., "Spiderweb array: A sparse spin-qubit array," *Phys. Rev. Appl.*, vol. 18, no. 2, Aug. 2022, Art. no. 024053.

[32] R. W. J. Overwater, M. Babaie, and F. Sebastiano, "Cryogenic-aware forward body biasing in bulk CMOS," *IEEE Electron Device Lett.*, vol. 45, no. 2, pp. 152–155, Feb. 2024.

[33] L. Enthoven, J. van Staveren, Y. Li, Y. Zhang, and C. Wang, "Data underlying the publication: Cryo-CMOS integrator-based DAC for scalable biasing of semiconductor qubits," 4TU.ResearchData, May 2026, doi: 10.4121/B5750C19-6CF2-4929-8A1C-2B41E2DD9B1B.V1.

[34] K. Bult, M. S. Akter, and R. Sehgal, "High-efficiency residue amplifiers," in *Low-Power Analog Techniques, Sensors for Mobile Devices, and Energy Efficient Amplifiers: Advances in Analog Circuit Design*. Cham, Switzerland: Springer, 2019, pp. 253–296.

[35] J. van Staveren et al., "Cryo-CMOS voltage references for the ultrawide temperature range from 300 k down to 4.2 k," *IEEE J. Solid-State Circuits*, vol. 59, no. 9, pp. 2884–2894, Sep. 2024.

[36] P. A. 'T Hart, M. Babaie, E. Charbon, A. Vladimirescu, and F. Sebastiano, "Characterization and modeling of mismatch in cryo-CMOS," *IEEE J. Electron Devices Soc.*, vol. 8, pp. 263–273, 2020.

[37] M. A. Pertijs and J. Huijsing, *Precision Temperature Sensors in CMOS Technology*. Cham, Switzerland: Springer, 2006.

[38] G. Kiene, S. İlik, L. Mastrodomenico, M. Babaie, and F. Sebastiano, "Cryogenic characterization of low-frequency noise in 40-nm CMOS," *IEEE J. Electron Devices Soc.*, vol. 12, pp. 573–580, 2024.

[39] J. H. Fischer, "Noise sources and calculation techniques for switched capacitor filters," *IEEE J. Solid-State Circuits*, vol. JSSC-17, no. 4, pp. 742–752, Aug. 1982.

[40] B. Prabowo et al., "29.3 a cryo-CMOS receiver with 15K noise temperature achieving 9.8dB SNR in 10 μs integration time for spin qubit readout," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2024, pp. 474–476.

[41] T. C. Carusone, K. W. Martin, and D. Johns, *Analog Integrated Circuit Design*, 2nd ed., Hoboken, NJ, USA: Wiley, 2011.

[42] Y. Osaki, T. Hirose, N. Kuroki, and M. Numa, "A low-power level shifter with logic error correction for extremely low-voltage digital CMOS LSIs," *IEEE J. Solid-State Circuits*, vol. 47, no. 7, pp. 1776–1783, Jul. 2012.
[43] P. A. T. Hart, M. Babaie, E. Charbon, A. Vladimirescu, and F. Sebastiano, "Subthreshold mismatch in nanometer CMOS at cryogenic temperatures," *IEEE J. Electron Devices Soc.*, vol. 8, pp. 797–806, 2020.
[44] R. M. Incandela, L. Song, H. Homulle, E. Charbon, A. Vladimirescu, and F. Sebastiano, "Characterization and compact modeling of nanometer CMOS transistors at deep-cryogenic temperatures," *IEEE J. Electron Devices Soc.*, vol. 6, pp. 996–1006, 2018.
[45] T. H. Swift, "A superinductor in a deep sub-micron integrated circuit," 2025, *arXiv:2507.13202v4*.

Luc Enthoven (Graduate Student Member, IEEE) received the B.Sc. and M.Sc. degrees (cum laude) in electrical engineering from Delft University of Technology, The Netherlands, and the Ph.D. degree in cryo-CMOS circuits for scalable quantum computing from the Group of Fabio Sebastiano, Delft University of Technology.

In 2019, he worked as an Intern in analog devices with the BMS Group, Munich, Germany. Since 2025, he has been the CTO and one of the founders of FrostByte, where he works on cryo-CMOS for scaling quantum devices. His research interests are in analog and mixed-signal circuit design and low power cryo-CMOS circuits and systems.

Job van Staveren received the B.Sc. degree in electrical engineering and the M.Sc. degree in electrical engineering, with a specialization in microelectronics from Delft University of Technology in 2016 and 2018, respectively, where he is currently pursuing the Ph.D. degree in electrical engineering. His research interests include analog/mixed-signal design, with a particular focus on design for the cryogenic temperature range and measurement of CMOS-electronics at cryogenic temperatures.

Jiang Gong received the B.Sc. degree (Hons.) in electrical and electronic engineering from Jilin University, Changchun, China, in 2015, and the M.Sc. (cum laude) and Ph.D. degrees from Delft University of Technology, Delft, The Netherlands. From May 2022 to January 2024, he was with SiTime Netherlands, Rijswijk, The Netherlands, as a Senior Analog/Mixed-Signal Integrated Circuit Designer, focusing on phase-locked loop design for precision timing applications. From January 2024 to November 2024, he was with ETH Zürich, Zürich, Switzerland, as a Post-Doctoral Researcher. Since December 2024, he has been a Full Professor with the University of Electronic Science and Technology of China (UESTC), Chengdu, China. His current research interests include high-spectral-purity and wide-tuning-range frequency synthesizers, high-speed data converters, high-precision analog design for wireless, wireline, and quantum computing applications. He was a recipient of the IEEE Solid-State Circuits Society (SSCS) Predoctoral Achievement Award (2021–2022) and Chinese Government Award for Outstanding Self-Financed (non-government sponsored) Students Abroad and a co-recipient of the Best Student Paper Award at IMS-2023 (second place). He is a reviewer of IEEE JOURNAL OF SOLID-STATE CIRCUITS (JSSC), IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, and IEEE SOLID-STATE CIRCUITS LETTERS (SSCL).

Masoud Babaie (Senior Member, IEEE) received the B.Sc. degree (Hons.) in electrical engineering from the Amirkabir University of Technology, Tehran, Iran, in 2004, the M.Sc. degree in electrical engineering from the Sharif University of Technology, Tehran, Iran, in 2006, and the Ph.D. degree (cum laude) in electrical engineering from Delft University of Technology, Delft, The Netherlands, in 2016.

He is currently an Associate Professor with the Department of Microelectronics, Delft University of Technology. His research interests include RF and millimeter-wave integrated circuits and systems for wireless communications and cryogenic electronics for quantum computing.

Dr. Babaie served on the technical program committee for the IEEE International Solid-State Circuits Conference (ISSCC) from 2021 to 2026, including as the RF Subcommittee Vice Chair in 2025 and 2026. Since 2022, he has been the Chair of the Emerging Computing Devices and Circuits Subcommittee of the IEEE European Solid-State Electronics Research Conference (ESSERC). He also serves as an Associate Editor for IEEE SOLID-STATE CIRCUITS LETTERS (SSCL) and has served as a Guest Editor for the IEEE JOURNAL OF SOLID-STATE CIRCUITS (JSSC). He has received several awards, including the (2015–2016) IEEE Solid-State Circuits Society Pre-Doctoral Achievement Award, the 2019 IEEE ISSCC Demonstration Session Certificate of Recognition, the 2020 IEEE ISSCC Jan Van Vessem Award for Outstanding European Paper, the 2022 IEEE CICC Best Paper Award, the 2023 IEEE IMS Best Student Paper Award (Second Place), the 2024 IEEE Solid-State Circuits Society Outstanding Reviewer Award, and the 2025 IEEE Solid-State Circuits Society New Frontier Award. In 2019, he was awarded the Veni Grant from the Netherlands Organization for Scientific Research (NWO).

Fabio Sebastiano (Senior Member, IEEE) received the B.Sc. and M.Sc. degrees (cum laude) in electrical engineering from the University of Pisa, Italy, in 2003 and 2005, respectively, the M.Sc. degree (cum laude) in engineering from the Sant'Anna School of Advanced Studies, Pisa, Italy, in 2006, and the Ph.D. degree in electrical engineering from Delft University of Technology, The Netherlands, in 2011.

From 2006 to 2013, he was with NXP Semiconductors Research, Eindhoven, The Netherlands, where he conducted research on fully integrated CMOS frequency references, nanometer-CMOS temperature sensors, and area-efficient interfaces for magnetic sensors. In 2013, he joined Delft University of Technology, where he is currently an Associate Professor. He has authored or co-authored one book, 12 patents, and over 120 technical publications. His main research interests are cryogenic electronics, quantum computing, sensor read-outs, and fully integrated frequency references.

Dr. Sebastiano has been on the technical program committee of the ISSCC, IMS, and the IEEE RFIC Symposium. He also serving as an Associate Editor for the IEEE JOURNAL OF SOLID-STATE CIRCUITS and has also served as a Guest Editor for the IEEE JOURNAL OF SOLID-STATE CIRCUITS and as an Associate Editor for IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS. He was a co-recipient of several awards, including the 2008 ISCAS Best Student Paper Award, the 2017 DATE Best IP Award, the ISSCC 2020 Jan van Vessem Award for Outstanding European Paper, the 2022 IEEE CICC Best Paper Award, and the 2023 Best Student Paper Award of the Joint ESSDERC/ESSCIRC Tracks. He has served as a Distinguished Lecturer for the IEEE Solid-State Circuit Society.