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***Abstract*— The heat produced within the device in its package depends on the power supplied to each IP block. The improper placement of an IP block with high power consumption can become a reliability risk for IC packages, as it can significantly affect the reliability of solder balls due to thermal, mechanical, and electrical factors. It also mitigates the effect of thermal cycling, because it depends upon heat management within the package. Improper IP block placement can block heat flow paths, which results in poor thermal dissipation and higher temperature which can create a higher strain on the solder balls affecting their lifetime. Therefore, it is crucial to understand the interplay between the correct placement of IP blocks and solder balls to enhance solder ball reliability. COMSOL-based simulation study will be done on a WLCSP (Wafer Level Chip Scale Package) mounted on a PCB board on which solder balls are connected to copper layers on the die and PCB sides. Variations in the placement of the IP blocks. Thermal cycling and the variations in the placement of the IP block within the package will be taken as a loading condition. Therefore, this influences the susceptibility of device failure due to solder ball fatigue. Based on board-level passive cycling, the solder balls which are located under the IP blocks are the most likely ones affected by this stress.**

The results will be analyzed to optimize the layout of the IP blocks, concerning accumulated plastic strain on the solder balls at different locations of the IP block placement. It can help to understand the influence of the position of the IP block, reduce stress concentration, and minimize thermal cycling effects, which leads to an increase in the reliability of the solders joint and IC package itself.

Keywords—WLCSP, IP block, CTE, Equivalent plastic strain, Combined thermal cycles, Finite element Modelling.

I. Introduction

The ongoing trend for the usage of smart and smaller devices is escalating rapidly within the electronics industry. It requires a substantial transformation towards miniaturization of IC packages to the microns level, to be integrated in device applications. WLCSP is the packaging technology that turned out to be the most competent to meet the requirement of being size-efficient[1]. An example of the WLCSP package is shown in Fig 1. Its size can be reduced to correspond with the size of the die itself, with good reliability and optimal electrical and thermal performance. This technology was introduced back in the late 90s and since then it gained significant growth in its usage, predominantly in small consumer products like cell phones[2], [3]. At present its application area continues to broaden into various portable applications, such as wearable electronics, tablet devices, and even some automotive applications.

In this paper, the focus will be on WLCSP technology based on the direct bumping of solder balls on the bond pad, as shown in Fig 2[3]. Like any other package, WLCSP also faces some reliability challenges and issues. Due to its structure, the reduced package height and smaller solder ball size increases the interaction between the device and the PCB. It intensifies the stress transfer to the solder joints, especially during thermal cycling, leading to fatigue failure that can cause the entire system to break down[4], [5], [6].

The thermo-mechanical stress within the package occurs due to thermal cycling, which can be either passive or active cycling. Active cycles (Power cycles) do not only relate to switching on and off the package continuously. During these cycles the application-specific IP blocks within the die switches and induces internal heat. The amount of heat generated depends on the power supplied to each IP block, which depicts the die acting as a heat source. However Passive cycling refers to a consistent change in the ambient conditions (environmental change). It can be done by means of the climatic chambers in which the whole device experiences temperature change. The effect of thermo-mechanical stress can be observed as package deformation due to a mismatch of the Coefficient of Thermal Expansion (CTE) among the package components. It leads to various failure modes within the package and solder joints.

The degradation in the solder joints due to passive thermal cycling has been already researched extensively. However, the combination of both active and passive cycles, which is closer to real-life applications, is still less researched[7]. Therefore the intent of this work is to investigate the damage accumulation on the solder joints due to combined cycling. Along with the temperature variations, variations in the package parameter (IP block placement) are also taken as the loading condition. As the IP block is the primary heat source of self-heating, the reliability of solder joints can be significantly affected by incorrect placement. It can disturb

the thermal management within the package by blocking the heat flow paths, leading to a rise in internal temperature, increased strain, and shorter lifetime. Despite extensive research over the years, the solder joint is still a crucial location that needs to be researched for the reliability of microelectronics systems[8].

For this assessment, thermomechanical simulations are performed on COMSOL for thermal cycling with varying the IP block position. A comparison analysis is conducted using the Equivalent Plastic Strain (EPS) and the lifetime of solder balls at various locations. This analysis is supported by board-level passive temperature cycling on a similar package. The results can assist in optimizing IP block placement, which can improve the reliability of the solder joints and the package.

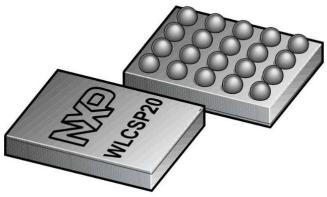

Figure 1: WLCSP20, wafer-level chip scale package; 20 bumps

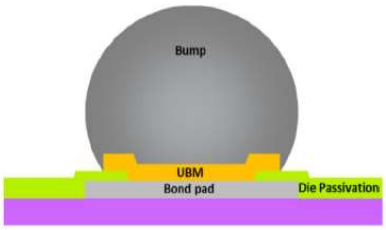

Figure 2: Example of WLCSP construction

II. Related Work

As mentioned above, limited research is available on combined thermal cycling (CTC) and IP block placement effects on solder joints. To grasp a comprehensive understanding, key existing studies are mentioned below.

Denira et al.[9] present the analysis of board-level solder joint reliability for two different boards (FR4 and Megtron 6) under CTC (Accelerated thermal cycles + Power cycles). Their findings show stress (Von Mises and Elastic strain) on the FR4 board is comparatively higher than Megtron 6. It also states that maximum stress appears on the corner solder balls of the package. Further analyses were made on the basis of the change in plastic work. The analyses show that plastic work increases after applying CTC as a loading condition. Plastic work for the FR4 board almost doubled as compared to the Megtron series. Rahangdale et al.[10] conducted similar research but on a different package named Quad Flat No-Lead (QFN) and took the thickness of the board into account. The results presented in this research are analyzed based on the effect of PCB thickness on the plastic work under CTC. In comparison with three different board**s** based on thickness (62mil, 93mil, and 134mil), 134mil experienced less plastic work. It highlights that increasing board thickness will decrease the plastic work, resulting in more cycles to failure. In contrast, the trend is the opposite for passive thermal cycles

The work from Otto et al.[11] shows the experimental evidence for the device (T0-220) failure under CTC. The failure is defined on the basis of End of Life criteria, which are defined as a +5% increase in forward voltage and a +20% increase in thermal resistance (Rth). Wire bond failure comes out to be a predominant failure mode. Additionally, Rth and ΔT were also increased by 6% and 3%, indicating that the solder beneath the bond wire is also degrading. Therefore as the experiment continues wire bond lift-off becomes the main cause of failure.

Liu et al.[12] uses area ratio (between chip region and direct copper bonding) and the load current duration of the power cycle (t_{on}) to vary the temperature gradient within the package. The findings have shown that, by varying t_{on} the dominating failure mode can be shifted, within the same power cycle test (PCT). Failure mode trends are given below:

- For a smaller area ratio and a high t_{on}, wire bond failure dominates.
- For high area ratio and high t_{on}, solder degradation becomes the dominant failure mode.
- For high area ratio and short t_{on}, wire bond is the primary cause of failure.
- For short area ratio and short t_{on}, solder degradation is the main cause of failure.

Kumar et al. [13] conducted a comparative study for two different solder joint geometries (Hourglass and barrel) under CTC. SEM analysis revealed that under passive thermal cycling, the crack that appears on barrel-type solder (BT) is about 265um and on hourglass type (HT) it is about 208um on the neck side. On the other hand, when CTC is applied simultaneously, the crack appears on the BT is about 300um, and on the HT it reaches about 425um. As per the criteria of the crack growth and length, BT is more reliable in CTC while HT is more reliable at passive thermal cycling.

Bhanu et al.[14] proposed an approach similar to the concept of our work. The die position and number of dies have a significant effect on the solder layer. Fig 3 (with permission) depicts that, placing the die in the symmetric and asymmetric placements got higher strain on the corners of the solder layer. Meanwhile, It can be also observed that the additional die in the full module leads to the entire edge being highly strained as compared to a single die.

The research conducted by Korpati et al[15] also, aligns with the study of our interest. Simulations are performed to analyze the solder joints concerning die placement variations within the X and Y direction compared to center placement. Seven designs of experiments (DOE) have been simulated to analyze the effects of die placement variations. DOE1 to DOE 4 the die was placed at different locations in the Y direction, from top to bottom. DOE 5 to DOE 6 die placed at different locations in X direction towards the right. .DOE 7 represents the center package condition, which shows uniform strain energy density (SED) for solder balls. Apart from DOE 7, DOE 3 and 5 have shown the trend for balanced SED for corner solder balls. The die drifts slightly in the Y and X directions.

III. Methodology

As mentioned above in Section 1, during power cycling, the application-specific IP blocks generate self-heating within the package. Depending on package size and product

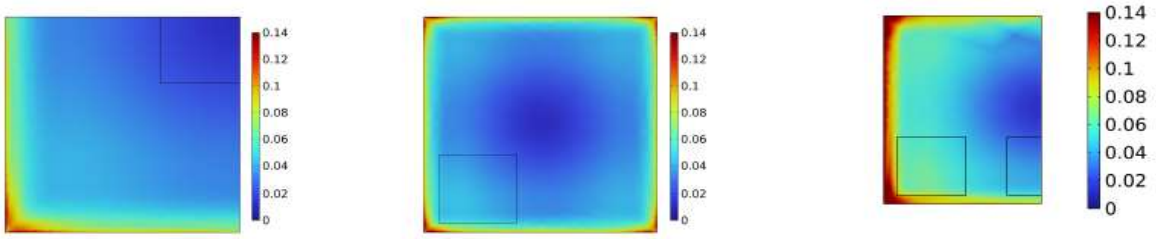

Figure 3 (a) Quarter model for symmetric die placement, (b)Half model for asymmetric die placement, (c) Full model for Full module (two dies), significantly show a higher strain due to the presence of a second die.(with permission)

functionality, there could be a few tens of IP blocks. Each IP block within the package operates within a specific range (current and voltage) based on its functionality.

For Example, Electric vehicles come up with many electronic modules (Battery management, Braking system, Thermal management, ADAS, etc.) to operate vehicles. Each module is made with several devices, with each device containing several IP blocks based on their functionality, as depicted in Fig 4. However, It is not limited to automotive applications, other applications such as cell phones, the Internet of Things (IoT), Ultra-wideband (UWB) devices, Near-field communications (NFC), etc. also use single IC packages with different sensors integrated into it.

The device's internal heat depends upon the power supply to each block. Improper placement of the IP block with higher power consumption causes a reliability risk for the whole package. It can significantly degrade the solder balls, due to thermal, mechanical, and electrical influences leading to solder fatigue.

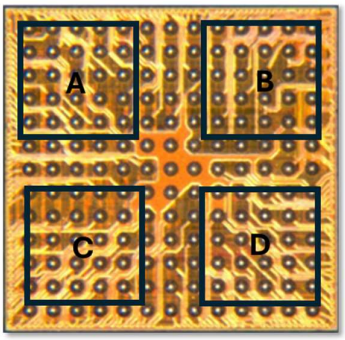

Figure 4 An Example of a single package with several IP blocks

A. Thermomechanical Modeling

Thermal cycling tests are crucial for analyzing the reliability of the solder joints. In experimentation, it can run up to more than 1000 cycles at 1 to 2 cycles per hour. This test to failure can take up to several months to analyze the failure modes or degradation of solder joints. However, if the results show poor reliability and require adjustment in the product design, it will significantly prolong the product's time to market. To overcome this issue, R&D teams from academia and industry use finite element modeling simulations to assess the solder joint reliability during the design phase, enabling timely optimization. It is a valuable tool that performs strain and stress calculations, including reliability predictions for solder joints. Therefore, in this study, we use COMSOL for Finite Element Modelling modeling. The package consists of 5x4 WLCSP also known as WLCSP20 as shown in Fig 1. It has 20 solder bumps with a pitch of 0.5mm. The PCB size (8mmx8mmx1.23mm) has been taken three times larger than the chip size to lower the effects of PCB on the solder joints. It consists of two layers top layer contains copper and the bottom layer contains FR4 material.

The solder joints are directly attached to the copper layers within the die and PCB side. The SAC 305, a lead-free solder joint material model is used from the COMSOL library with 0.2mm sphere radius. The upper and lower areas of the solder balls attached to the pads are 0.13mm in diameter. The size of the package is (2mmx2.5mmx0.57mm), and it consists of two layers of silicon and copper. The complete Finite Element Model can be seen in Fig 5.

The mesh quality plays an important role because it influences how the model represents the actual object. A model divided into small, well-shaped elements is a sign of good-quality meshing and helps to generate reliable and precise results. The mesh quality has be to fine in the regions, where higher stress and strain values are expected to be concentrated. For example: the edges of the package, and the corners of solder balls.

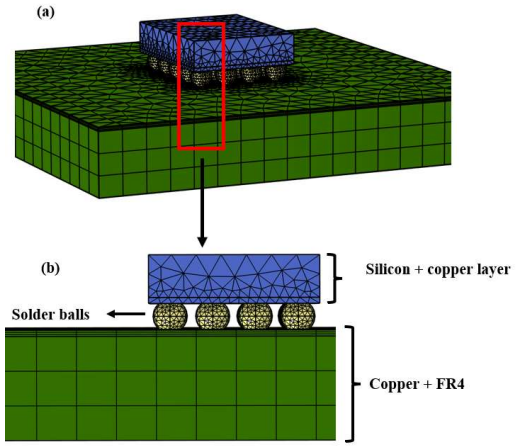

Figure 5 (a) FEM of WLCS20 with PCB, (b) Detailed structure of WLSCP, showing a close-up view of solder balls (With mesh)

In this model, a tetrahedral mesh is used for the IP block, die, and solder balls, while the triangular mesh is implemented on the faces of the copper layer where solder balls are attached. FR4 is meshed using swept mesh. The final mesh is refined and selected by increasing the number of domain elements up to 62000 until the strain values become almost constant.

Two thermal cycling profiles (active and passive) have been taken as loading conditions, depending on case studies. The passive thermal profile is the JEDEC standard from -40 to 125°C. The active thermal profile acts as a function of power cycles applied to the IP block within the die from -40 to 150°C. The temperature difference in both profiles is about 25°C because in power cycles the IP block generates more internal heat. This accurately corresponds to the impact of an actual occurrence. The thermal profiles can be seen in the Fig 6 below.

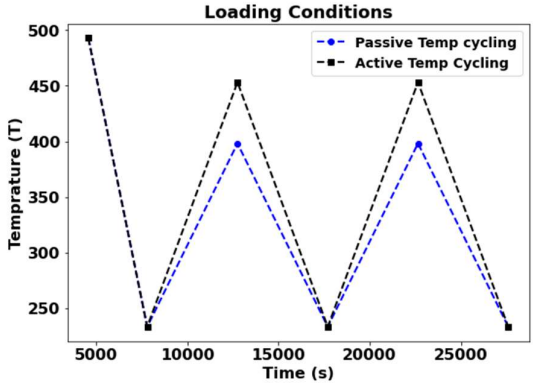

Figure 6 Applied thermal cycling profile

Three case studies have been performed with different loading conditions and different internal package structures.

1. Board-level passive temperature cycling without IP block.
2. Combine active and passive cycling with IP block as almost the same size of die.
3. Combine Active and passive cycling with variations of small IP block position.

The representation of case studies 2 and 3 can be seen in Fig 7 below.

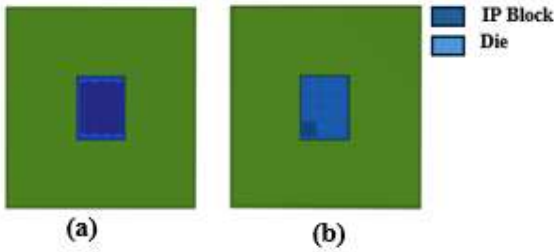

Figure 7 IP block representation according to case studies, (a) IP block as the same size of the die represents case 2, (b) Application-specific IP block at bottom left represents case 3.

For the observation of the stress, strain, and deformation of the materials an elastoplastic model with hardening effect has been used. Von misses stress and Equivalent Plastic Strain (EPS) analysis methods are used to determine the location with maximal strain and stress.

IV. Results and Discussion

Evaluating stress and strain location within the solder balls is crucial to determine the reliability of the package. The findings of this study align with the existing literature, that the higher stress and strain concentrations are mostly found at the corner solder balls of the package. Therefore, the EPS distribution on the corner solder balls will be taken as a reference.

A. Comparison of the case studies

Fig 8 illustrates the EPS distribution in the solder balls, along with the plots representing the average EPS at the corner solder joints. The average has been taken at the component side of the solder joints where higher stress is observed. Case 1 represents the actual stress testing practice adopted by researchers within the laboratory for reliability. Case 2 represented a hypothetical yet simplified scenario in which the self-heating is assumed to be dissipated at the whole die surface. On the other hand, Case 3 simulates a more realistic scenario, including an application-specific IP block placed at the bottom left of the die.

A distinct difference can be seen from the EPS values between these two cases 1 and 2. The difference is due to the presence of the IP block. In case 1 the passive temperature profile is applied to the whole package. In case 2 passive temperature cycles are applied to the whole package, while an active temperature profile is applied in parallel to the IP block. In case 2 the EPS is comparatively lower than in case 1, due to more internal heat generated by the IP block which compensates for the CTE mismatch. It weakens the solder joint reliability as it gets closer to a stress-free temperature.

Even if the CTE is compensating, the repeated thermal cycles can create fatigue issues and micro-cracks generated within the solder balls or different materials of the package. The crack side in the simulations appears to be the same as seen in the experimentation presented in[3] .

In case 3, the loading condition is also Combined Thermal cycles, in which the passive profile is applied to the whole package and the active profile is applied to the application-specific IP block. It can be seen from the plots that the EPS value for the bottom left corner ball is affected by the self-heating. As compared to case 1, the EPS values of the bottom left corner balls for cases 2 and 3 are lower but the same due to self-heating at that region.

However, other corner balls (top and bottom right) in case 3 have an EPS value closer to case 1 as shown in Fig 10. It highlights that in case 3 the package exhibits the combined response of case 1 and case 2. In the region where self-heating is present, the package experiences CTE compensation, and the EPS plot for the solder ball follows the trend of case 2. Contrarily, the region without self-heating has higher strain values and follows the EPS trend observed in case 1.

B. IP block variations (Case 3)

In application-specific IP blocks, a major challenge comes with a block placement having higher self-heating. To optimize the layout of IP blocks, several variations with IP block placement were simulated. Variations have been done in the X-axis from left to right. The plots for the EPS in Fig 9 clearly show that in each case the solder joint under the IP block is highly affected. In Fig 9 (a) and 9 (c), it can be seen that corner balls have the lowest strain values, indicating that higher temperatures induced by the IP block compensate for the CTE mismatch. In case (b) it can be seen that stress on the corner solder balls is uniform. Therefore, placing an IP block

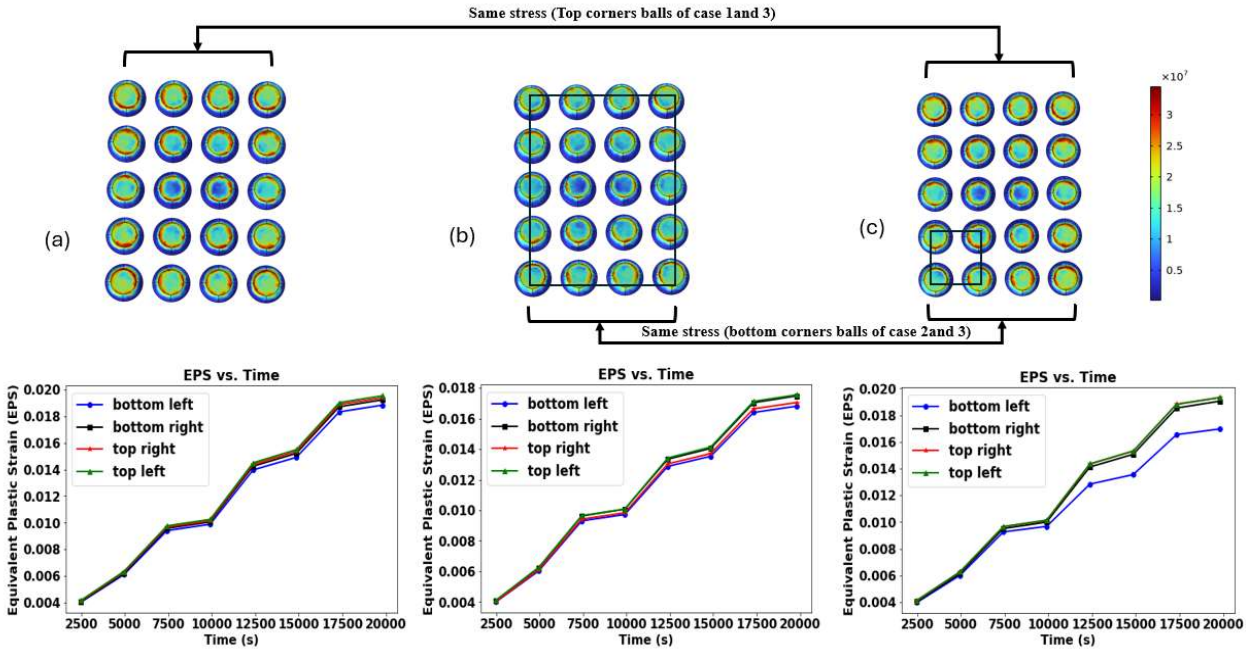

Figure 8 Stress and strain representation (a) package without IP block, (b) package with IP block (as big as the entire die), (c) package with IP block (small size-application specific)

between the corner balls is better from a solder joint perspective.

V. Conclusion and Future Work

This research highlights the proof of concept of how IP block variations and IP block size affect the reliability of solder joints. The results indicate that the self-heating within the device is counterbalancing the CTE mismatch between silicon and PCB.

The paper also presents a comparative analysis based on IP block variations. In each case, the location for maximum EPS correlates with results from the literature on stress-based experimental testing.

This work can be expanded further to predict the strain values and Remaining Useful Lifetime (RUL) by estimating the number of cycles to failure in relation to variation in location or power dissipation of the IP block within the package. There can be numerous variations based on X and Y direction, and conducting it by user-controlled simulations is time-consuming. Approaches using Artificial Intelligence (AI), Machine Learning (ML), Meta Model, and Digital Twins (DT)[16], [17], [18], [19], offer a potential alternative for reliability testing. It requires data to train the model.

Based on the research presented in this paper, running six more variations of IP block within the package's center and top layers is enough to collect the data. K-nearest Neighbors

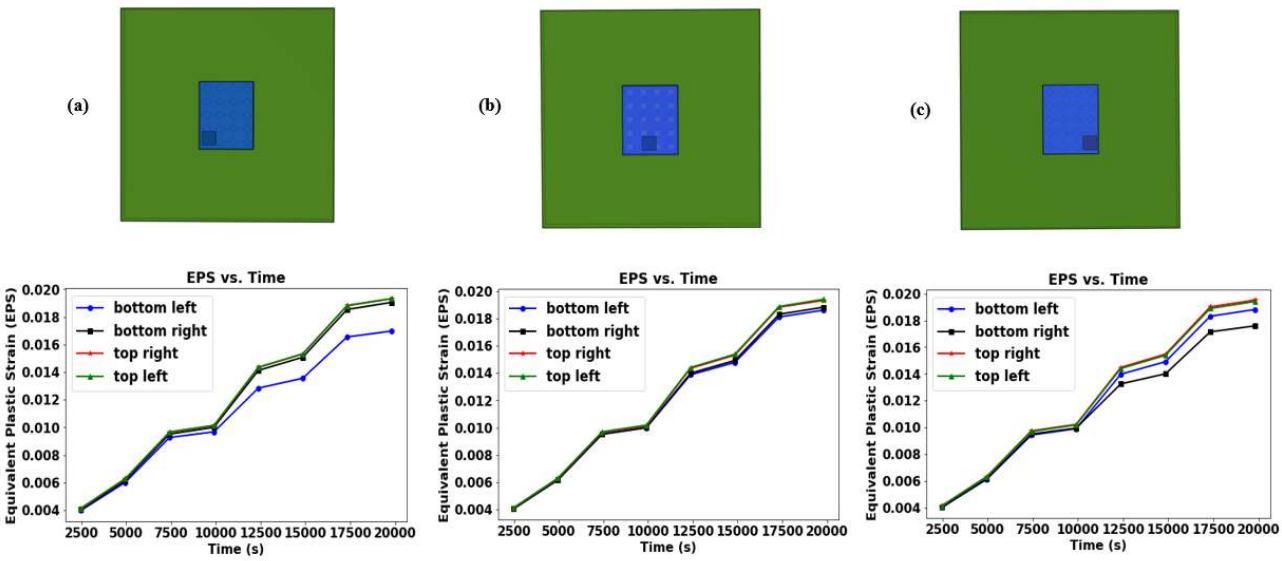

Figure 9 Variations of IP Block Placement

Algorithm (KNN) is most likely the best fit for this research to train the model, enabling easy variations and predictions.

VI. Acknowledgment

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