Dependence of Single-Crystalline Si TFT Characteristics on the Channel Position Inside a Location-Controlled Grain

Vikas Rana, Ryoichi Ishihara, Yasushi Hiroshima, Daisuke Abe, Satoshi Inoue, Tatsuya Shimoda, Wim Metselaar, and Kees Beenakker

***Abstract*—To obtain high-performance thin-film transistors (TFTs), a comprehensive study of the channel position of TFTs inside a location-controlled grain was carried out. The location of the grain is precisely controlled by the μ-Czochralski process using an excimer laser. The grain was grown from a thin Si column embedded in SiO_2 (grain filter). The characteristics of the TFTs drastically improved when the channel region was not centered above the grain filter. With TFTs whose current-flow direction is parallel to the radial direction of the grain filter, an electron mobility and subthreshold swing of $\sim$ 600 $cm^2/V \cdot s$ and 0.21 V/dec respectively were obtained.**

***Index Terms*—Excimer laser, location control, poly Si, subthreshold slope, thin-film transistor (TFT).**

I. Introduction

EXCIMER laser crystallization of a-Si is an attractive technique for realizing low-temperature (< 350 °C) poly Si thin-film transistors (TFTs) on glass [1], [2]. The field-effect electron mobility, μ_{FEe}, of the poly Si TFTs fabricated by conventional excimer laser crystallization is around 100 $cm^2/V \cdot s$, which limits the use of poly Si TFTs for other circuitries, such as DAC and pixel memory. The μ_{FEe} of poly Si is lower than that of MOS transistors since the electrically active grain boundaries create potential barriers that hinder the motion of carriers in poly Si TFTs. However, the performance of these TFTs can be improved by fabricating them such that their current flow direction is parallel to the grain boundaries (GBs) [3]. Many ways to achieve the lateral solidification [4] (one-dimensional location control of grain) and TFT fabricated parallel to the GBs have been reported [5], [6]. However, the presence of random GBs and its spread in number and direction leads to transistor characteristics inferior to their MOSFET counterparts. TFTs fabricating inside a grain, i.e., single-crystalline Si (c-Si) TFTs [7] have improved the characteristics, however the improved electrical performance of the c-Si TFTs compared to that of the poly Si TFTs will allow us to integrate system circuits as well as driver circuits with display, i.e., "to produce a system on glass." For producing c-Si TFTs on glass, it is essential to locate the large grain at the desired position on the substrate, i.e., two-dimensional location control. Precise location control of the grain allows us to eliminate the grain boundaries from the active area of the TFT. The position of the grain can be controlled by local melting/unmelting of the Si film. We controlled the position of the grain by modifying the substrate with conventional photolithography rather than by spatially modifying the incident laser energy density. The μ-Czochralski (grain filter) process [8] provides a precise way to control the position of the grain in excimer laser crystallization. The c-Si TFTs fabricated inside a location-controlled grain by this μ-Czochralski (grain filter) process showed on average a μ_{FEe} of 430 $cm^2/V \cdot s$ [9]. The rather high subthreshold swing S (0.70 V/dec) was improved to 0.45 V/dec by employing a high-quality electron cyclotron resonance plasma-enhanced chemical vapor deposition (ECR-PECVD) SiO_2 as a gate insulator [10] owing to the remote plasma process and the high electron density in the plasma.

The *S* value is, however, still higher than those of MOSFETs [11] and recently reported poly Si TFTs [12]. In this paper, mainly to improve the *S* value, we investigated the following effects on the TFT characteristics. First of all, we studied the effect of the position of the TFTs inside a grain. So far, we located the channel of the c-Si TFTs above the grain filter. The characteristics might be limited by defects near the bottom of grain filter. Furthermore, the location-controlled grain has planar defects, which are mainly coherent $\Sigma 3$ twin boundaries and are radially distributed from the grain filter center. It has been suggested that the defective planes that are perpendicular to the current flow direction impede the ON-current [13]. In this paper, we have fabricated TFTs with and without a grain filter and with various current flow directions. Moreover, we have investigated the effect of the pulse duration of the excimer laser. It was reported that by using an excimer laser with a long pulse duration, one can improve the crystal quality [14] and grain size [15] as it offers slow heat flow toward the substrate. Furthermore, thin Si and thin gate oxide should lead to a decrease in the *S* value. The effects of Si and the gate oxide thickness were also investigated.

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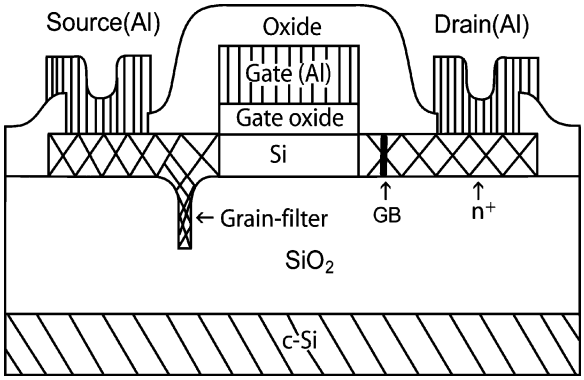

Fig. 1. Schematic view of the c-Si TFT fabricated inside a location-controlled grain.

II. Experiment

The TFTs used in this experiment were fabricated with the μ-Czochralski process [8]; a schematic diagram of the c-Si TFT is shown in Fig. 1. Thermally oxidized c-Si wafers were patterned with a grid of 0.75 μm deep cavities with a diameter of 1.0 μm by plasma etching. Subsequently, a silicon dioxide was deposited by plasma-enhanced chemical vapor deposition (PECVD) using tetraethylorthosilicate (TEOS) and oxygen at 350 °C. With this process, the diameter of the larger cavity was decreased to a final value below 100 nm. Next, 100, 150, or 250-nm-thick a-Si was deposited by LPCVD using silane at 545 °C. The samples having 250-nm a-Si were crystallized with an XeCl excimer laser ($\lambda = 308$ nm, pulse duration $=$ 56 ns) with various energy densities at an elevated temperature of 450 °C. Some of the samples with 250 nm a-Si were crystallized with an XeCl excimer laser having longer pulse duration of 200 ns. The samples having 100 or 150 nm a-Si were crystallized with a longer pulse duration of 200 ns, using an XeCl excimer-laser with various energy densities at an elevated temperature of 400 °C. In both cases the samples are irradiated with one shot of the excimer laser. Fig. 2 shows a cross-sectional transmission electron microscope (TEM) image of grain, which shows that grain growth starts from the unmelted Si seed and a single grain is selected during the vertical growth. A scanning electron microscope (SEM) image of the grid of location-controlled grains with a spacing of 6 μm after Seccos etching is shown in Fig. 3. After the formation of the location-controlled grains, oxygen plasma treatment was carried out to passivate the trap states and dangling bonds in the bulk silicon. Subsequently, the crystallized Si film was patterned into islands by reactive ion etching. The channel region of the TFTs is designed such that the single grain covers the entire channel area. The channel position with respect to the grain filter determines the direction of the channel current flow with respect to the grain structure, as shown in Fig. 3.

Then, 80- or 120-nm ECR-PECVD SiO_2 was deposited as a gate insulator at room temperature and annealed in water vapor at 333 °C [12]. As reference, 150-nm LPCVD SiO_2 was deposited on some of the samples at 425 °C. The gate electrode was then formed with sputtered Al at room temperature. The channel length and width, measured by SEM, was 1.87 and

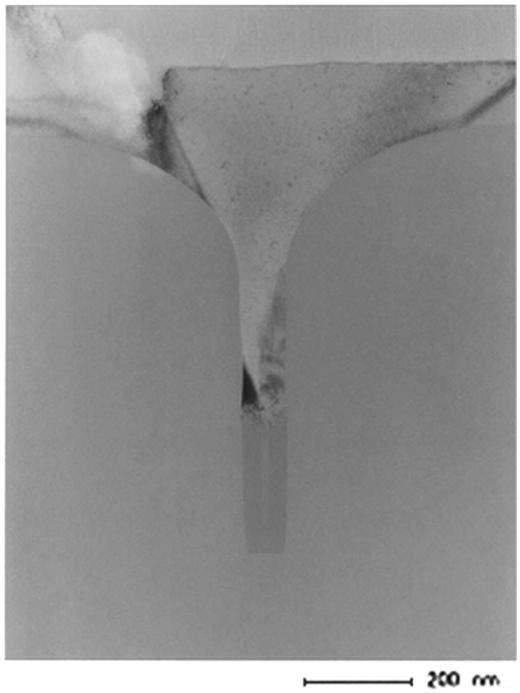

Fig. 2. Cross-sectional TEM image of location-controlled gain formed by the μ-Czochralski process. Selection of single grain during vertical growth in grain filter can be observed. The white part at the left is a damage caused during TEM specimen preparation.

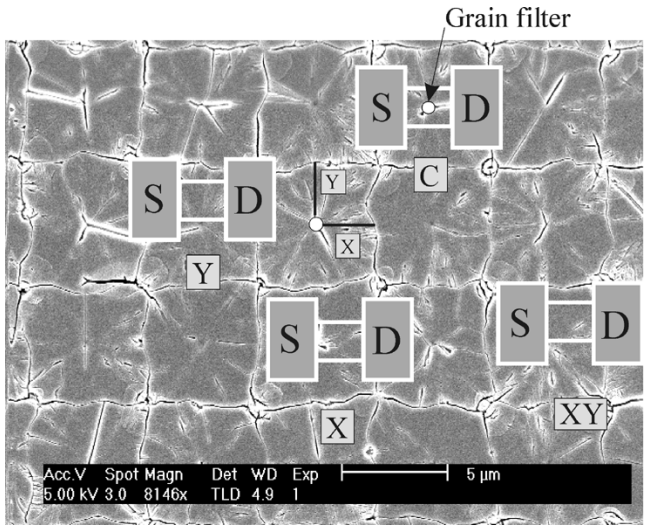

Fig. 3. SEM image of a grid of location-controlled grains formed by the μ-Czochralski process. The schematic shows the position of grain filter and TFTs at different positions X, Y, XY, C with respect to the grain filter.

2.03 μm, respectively. The source and drain were doped with phosphorus by ion shower [16] using an Al gate pattern as a mask, and subsequently annealed at 300 °C for 4 h in nitrogen ambient. Afterward, a passivation oxide, source and drain electrode were formed. No hydrogenation was carried out later. As reference, TFTs on silicon on insulator (SOI) with {100} orientation and a Si thickness of 100, 150, or 250 nm were fabricated with the same process conditions. For statistical study of the TFT characteristics, 30 transistors were measured for each position and process condition.

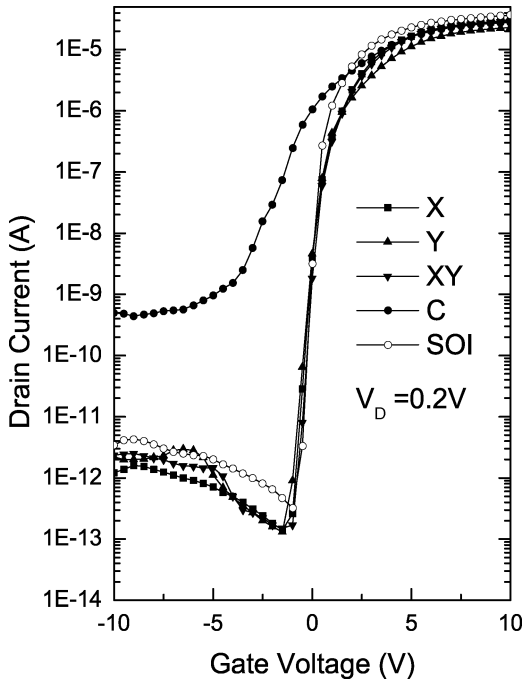

Fig. 4. I_D–V_G characteristics of c-Si TFTs of 250-nm-thick silicon having a 120-nm ECR-PECVD as a gate insulator for a short pulse duration for various TFT positions in the location-controlled grain. TFT made with silicon-on-insulator (SOI) wafer is also plotted as a reference.

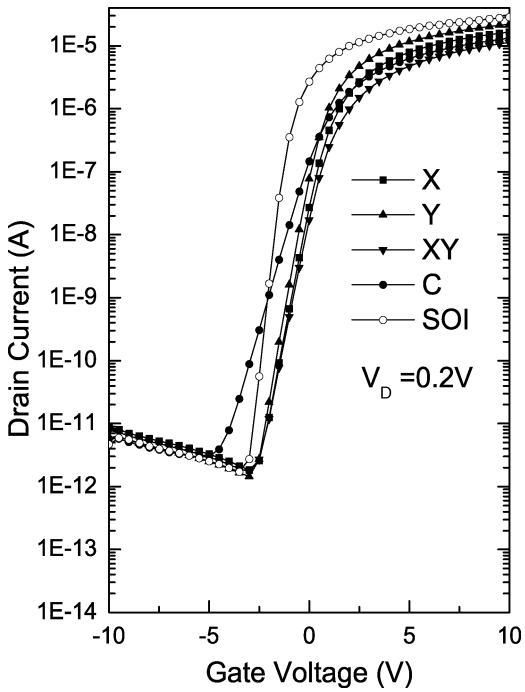

Fig. 5. I_D–V_G characteristics of c-Si TFTs of 250-nm-thick silicon having 150-nm LPCVD as a gate insulator for a long pulse duration for various TFT positions in the location-controlled grain. TFT made with SOI wafer is also plotted as a reference.

TABLE I
CHARACTERISTICS OF c-Si TFTS HAVING A 120-nm ECR-PECVD AS A GATE INSULATOR

TFTs	Channel position	μ_{FEe} (cm^2/V·s)	S (V/dec.)	I_{OFF}* 1E-13(A)	V_{TH} (V)
Grain-filter	X	597± 101	0.21± 0.03	1.3± 0.5	1.7± 0.2
	Y	528± 57	0.25± 0.04	1.7± 0.8	1.8± 0.3
	XY	505± 55	0.22± 0.01	1.4± 0.1	1.9± 0.1
	C	471± 32	1.1± 0.13	16800± 16900	0.86± 0.3
SOI		727±18	0.18± 0.006	3.57± 0.26	1.1± 0.09

TABLE II
CHARACTERISTICS OF c-Si TFTS HAVING A 150-nm LPCVD AS A GATE INSULATOR

TFTs	Channel position	μ_{FEe} (cm^2/V·s)	S (V/dec.)	I_{OFF}* 1E-13(A)	V_{TH} (V)
Grain-filter	X	415± 56	0.59± 0.05	21± 4.4	1.05± 0.18
	Y	428± 100	0.53± 0.06	15.3± 0.62	0.6± 0.4
	XY	351± 68	0.57± 0.04	19± 3.1	1.03± 0.22
	C	366± 69	0.74± 0.13	24.8± 5.6	0.44± 0.5
SOI		714±17	0.34± 0.02	16.6± 2.6	-0.7± 0.07

III. RESULTS AND DISCUSSION

A. Effect of Channel Position

As shown in Fig. 3, the position of the TFT channel was shifted along X, Y or diagonal XY direction with respect to the center of the grain filter (*C*), while the current flow direction was kept in the X direction. The shift of the channel with respect to the center of the grain filter is 1.5 μm.

Fig. 4 shows the transfer characteristics of the c-Si TFTs having 250-nm-thick silicon crystallized with the short pulse duration and 120-nm-thick ECR-PECVD SiO_2 as a gate insulator fabricated for various channel positions. The energy density of the excimer laser pulse was 1.025 J/cm^2. when the channel position was shifted from the top of the grain filter (*C*), the transfer characteristics improved dramatically. Table I shows μ_{FEe}, *S* value, off-current (I_{OFF}) and threshold voltage $(\mathrm{V_{TH}})$ with standard deviation for c-Si TFTs having ECR-PECVD SiO_2 as a gate insulator. The μ_{FEe} for these devices is evaluated in the linear region at a low drain voltage (V_D). The subthreshold slope *S* was calculated as the maximum slope in the subthreshold region. It is obvious from Table I that c-Si TFTs at the *X* position give the highest μ_{FEe}, lower *S*, and lower I_{OFF}, while c-Si TFTs on the *C* position give the lowest μ_{FEe}, the highest *S*, and the highest I_{OFF}. The high μ_{FEe} of the c-Si TFTs (597 $\mathrm{cm}^2/V \cdot \mathrm{s}$) at the *X* position is attributed to the fact that the carriers do not encounter the boundaries because these are parallel to the direction of current flow. The drastic improvement in *S* is a result of the absence of the grain filter, which has a high trap state density near the bottom, in the active channel region. Fig. 5 shows the transfer characteristics of the c-Si TFTs having 250-nm-thick silicon crystallized with short pulse duration and 150-nm-thick LPCVD SiO_2 as a gate insulator fabricated at various positions at laser energy density 1.025 J/cm^2. Table II shows the μ_{FEe}, *S*, I_{OFF} and V_{TH} of the

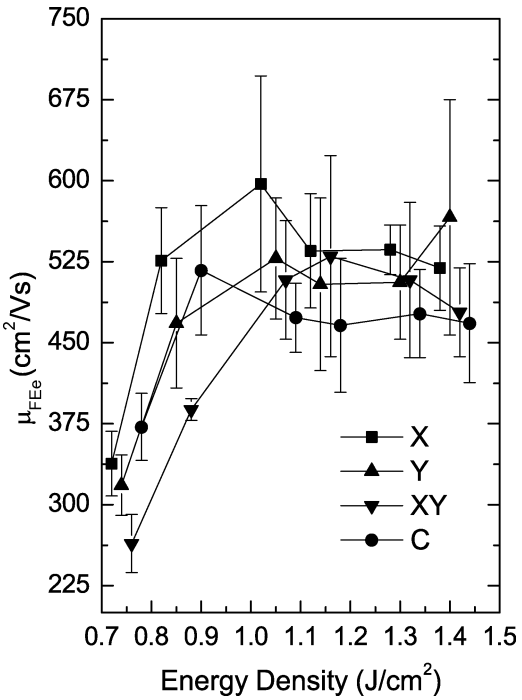

Fig. 6. Field-effect mobility of c-Si TFTs of 250-nm-thick silicon having a 120-nm ECR-PECVD gate insulator as a function of laser energy density for different channel positions with respect to the grain filter for a short pulse duration.

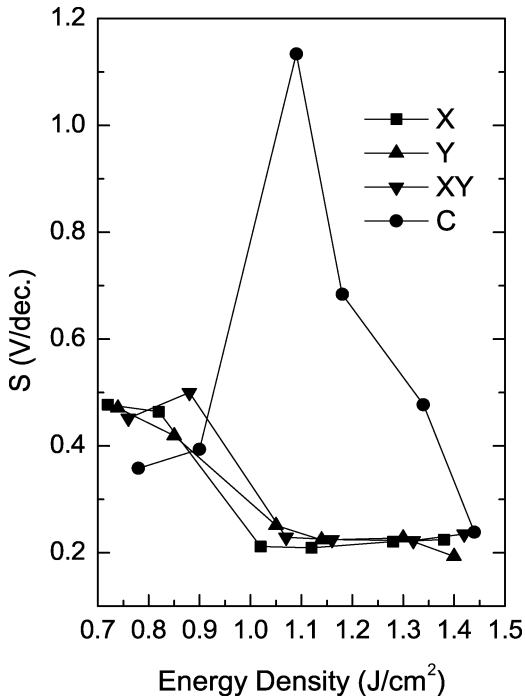

Fig. 7. Subthreshold slope of c-Si TFTs of 250-nm-thick silicon having a 120-nm ECR-PECVD gate insulator as a function of laser energy density for different channel positions with respect to the grain filter for a short pulse duration.

c-Si TFTs having 150-nm-thick LPCVD SiO_2 as a gate insulator. The shifting of channel position from the center of grain filter hardly improved the characteristics of the TFTs. This difference originates from the worse interface characteristics of LPCVD SiO_2, which screens the effects of trap states in the grain filter. The value of the interface density of states $(D_{\rm it})$ of SiO_2 deposited by ECR-PECVD and LPCVD calculated from the high-frequency and quasi-static capacitance–voltage (*C–V*) characteristics of a MOS capacitor was 2×10^{10} and 5×10^{11} cm^{-2}eV^{-1}, respectively [10].

B. Effect of Crystallization Energy Density

Fig. 6 shows the $\mu_{\rm FEe}$ value with the standard deviation as a function of laser energy density for each position of the c-Si TFTs having ECR-PECVD SiO_2 as a gate insulator. At low energy density, $\mu_{\rm FEe}$ is lower for all positions due to small grain size. As crystallization energy density increases, the melt depth of grain filter and hence grain size increases [17]. On other hand, the *C* position gives the highest $\mu_{\rm FEe}$ at low energy density, because the grain size is too small to cover the entire channel at the other positions at this energy density. However, the $\mu_{\rm FEe}$ for *XY* starts to saturate at the highest energy density because this position is farthest from the grain filter. For all positions, the $\mu_{\rm FEe}$ value increased with the energy density. This is because of a large melt depth with higher irradiation energy and hence a decreased number of random GBs. After reaching its maximum $\mu_{\rm FEe}$ slightly decreases with high irradiation energy densities. This could be caused by an increased surface or interface roughness. Fig. 7 shows *S* as a function of laser energy density for TFTs having ECR-PECVD SiO_2 as a gate insulator. The *S* value followed a similar trend as for $\mu_{\rm FEe}$ except the behavior of TFTs at *C*: an abnormal peak at moderate energy densities shown in Fig. 7. It is not well understood, but this might be attributed to the fact that the melt reaches the void of a-Si inside the grain filter. As the melt depth reaches the void in the grain filter, increasing the total amount of trap states by the increased surface area. Like $\mu_{\rm FEe}$, $I_{\rm OFF}$ and $V_{\rm TH}$ improved with increasing the laser energy density.

C. Effect of Pulse Duration

Crystallization was performed with an excimer laser having pulse duration of 200 ns for some of 250-nm-thick silicon samples. Fig. 8 shows $\mu_{\rm FEe}$ with standard deviation of the c-Si TFTs of 250-nm-thick Si having 120-nm-thick ECR-PECVD SiO_2 as a gate insulator for various channel positions in a grain as a function of energy density for the crystallization. As in the case of a shorter pulse duration, the mobility increases with energy density and the X direction gave the best value. Compared with the shorter pulse duration counterparts, the maximum of the mobility is slightly higher. This is attributed to the fact that the long pulse duration excimer laser [14] creates crystallized film with a better microstructure owing to the slow heat conduction to the substrate during solidification and hence a low solidification velocity [15]. Fig. 9 shows the S value of 250-nm-thick Si having 120-nm-thick ECR-PECVD SiO_2 as a gate insulator for various channel positions in a grain as a function of energy density for crystallization. There is no significant difference in the S values for the different positions, as compared that for the shorter pulse duration counterparts. This suggests that the longer pulse excimer laser crystallization produces a grain filter with a better microstructure as well.

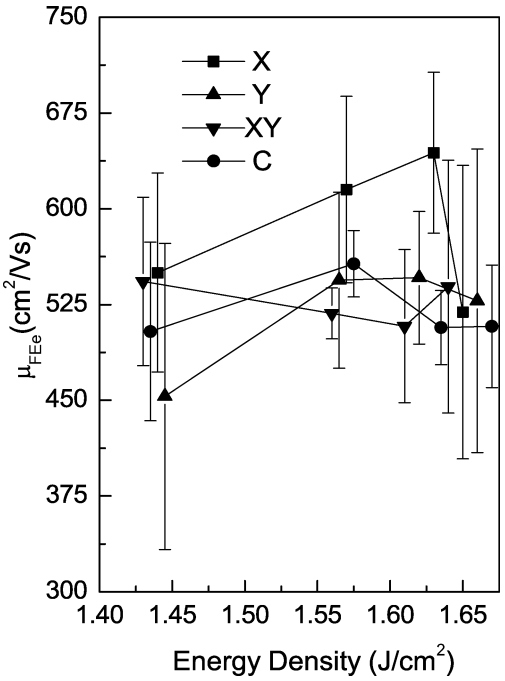

Fig. 8. Field effect mobility of c-Si TFTs of 250-nm-thick silicon having a 120 nm ECR-PECVD gate insulator as a function of laser energy density for different channel positions with respect to the grain filter for a longer pulse duration.

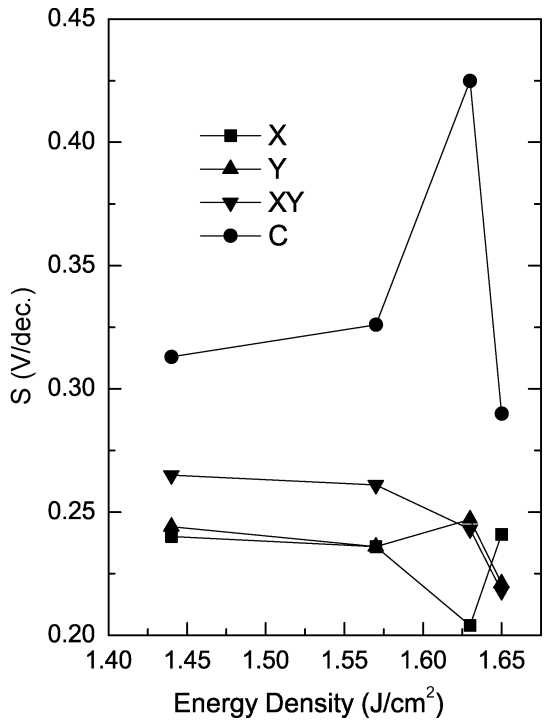

Fig. 9. Subthreshold slope of c-Si TFTs of 250-nm-thick silicon having a 120 nm an ECR-PECVD gate insulator as a function of laser energy density for different channel positions with respect to the grain filter for longer pulse duration.

D. Effect of Silicon Thickness

To investigate the effect of the silicon thickness, we have fabricated TFTs with various silicon thicknesses, $t_{\rm Si}$, of 100, 150, or 250 nm having a 120-nm ECR-PECVD SiO_2 as a gate insulator. Fig. 10 shows that both $\mu_{\rm FEe}$ and S degraded with decreasing silicon thickness. *S* can be described as [10]

$$S \cong \frac{\kappa T}{q} \ln 10 \left(1 + \frac{qN_{\rm bt}t_{\rm si} + qD_{\rm it}}{C_{\rm ox}}\right) \quad (1)$$

where $N_{\rm bt}$ is the bulk trap state density per unit volume, $t_{\rm si}$ the thickness of Si, and $C_{\rm ox}$ the gate oxide capacitance per unit area. The increase in S suggests that $N_{\rm bt}x\, t_{\rm si}$ increased although $t_{\rm si}$ decreased. This means that $N_{\rm bt}$ increases significantly with decreasing $t_{\rm Si}$. It has been reported that with the decreasing $t_{\rm si}$, planar defects inside the location-controlled grain increase [17].

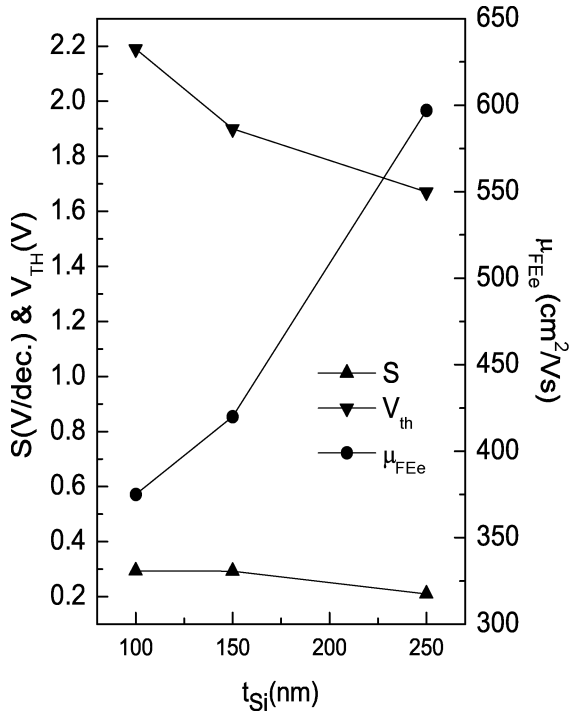

Fig. 10. Subthreshold slope, threshold voltage and field effect mobility of c-Si TFTs with an ECR-PECVD (120 nm) gate insulator as a function of silicon thickness for *X* channel position with respect to the grain filter for a longer pulse duration.

TABLE III
EFFECT OF GATE OXIDE THICKNESS ON CHARACTERISTICS OF c-Si TFTS OF 150-nm THICK SILICON

Gate oxide (nm)	μ_{Fee} (cm^2/V·s)	S (V/dec.)
120nm	420	0.29
80nm	254	0.17

E. Effect of Gate Insulator Thickness

To examine the effect of the gate insulator thickness, TFTs were fabricated with a 80- or 120-nm-thick ECR-PECVD SiO_2 gate insulator having a silicon thickness of 150 nm. Table III shows the $\mu_{\rm FEe}$ and S value of the c-Si TFTs for different gate oxide thicknesses with a 150-nm-thick silicon. The *S* value drastically improved to 0.17 V/dec by applying the 80-nm gate oxide. It is quite clear from (1) that as we increase the $C_{\rm ox}$ by thinning the gate insulator, the *S* value improves dramatically and approaches the thermal voltage. $\mu_{\rm FEe}$, however, decrease with the gate insulator thickness. The reason for this decrease is not well understood.

IV. Conclusion

The influence of the channel position inside a location-controlled grain on the characteristics of TFTs was investigated. For 250-nm-thick silicon, S drastically improved to 0.2 V/dec when the grain filter was not located in the channel region. This suggests a higher trap state density in the grain filter. The c-Si TFTs with LPCVD gate SiO_2 do not show such a significant improvement in S since the large $D_{\rm it}$ value for LPCVD SiO_2 screens the effect of the position inside a grain. The c-Si TFTs having no grain filter in the channel and whose current flow is directed radially with respect to the grain filter gave a high $\mu_{\rm FEe}$ of 597 $\rm cm^2/V \cdot s$ on average. This is because here, planar defects, which are mainly coherent grain boundaries and often grow radially from the grain filter, do not impede the carrier motion. Furthermore, S was improved to 0.17 V/dec by thinning of the gate insulator and the active Si layer thickness down to 80 and 100 nm, respectively. Nevertheless, $\mu_{\rm FEe}$ decreased with the gate insulator thickness as well as with Si layer thickness. Since thin silicon produces more defects during laser crystallization, the increased number of defects inside a grain causes the decrease in $\mu_{\rm FEe}$. The superior performance suggests that the c-Si TFT is attractive for future system circuit integration in AMLCD and also for three-dimensional integration of ICs.

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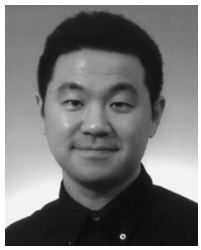
Vikas Rana was born in India in 1977. He received the M.Tech. degree from the Indian Institute of Technology, Delhi, in 2000. He is currently pursuing the Ph.D. degree at the Delft University of Technology, Delft, The Netherlands.

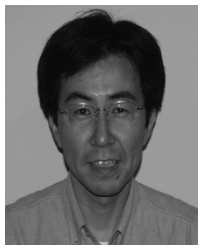
Since 2002, he has been a Research Member with Dr. R. Ishihara at the Delft Institute of Microelectronics and Submicrontechnology. He has been an active member of the Laboratory of Electronic Components, Technology and Materials as a Ph.D. student since 2002. His main research activities focus on location control of grains through a novel excimer laser crystallization process and fabrication and characterization of high-performance TFTs inside a single grain.



Ryoichi Ishihara received the Ph.D. degree from the Tokyo Institute of Technology, Tokyo, Japan, in 1996.

His main research activities were low-temperature CVD of silicon nitride film, fabrication of amorphous-Si TFTs, and excimer-laser crystallization of silicon films and fabrication of polycrystalline-Si TFTs. Since 1996, he has been with the Delft Institute of Microelectronics and Submicrontechnology, Delft University of Technology, Delft, The Netherlands, where he has been focusing on location control of grains through a novel excimer-laser crystallization process and fabrication and characterization of high-performance TFTs inside a single grain. He is currently an Associate Professor with the Faculty of Electrical Engineering, Mathematics and Computer Science, Delft University of Technology.

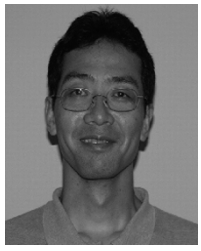
Dr. Ishihara is a member of the Society for Information Display, Material Research Society, and the Japan Society of Applied Physics.



Yasushi Hiroshima received the M.S. degree in electronic engineering from the Shinsyu University, Matsumoto, Japan, and the Ph.D. degree in electrical engineering from Nagaoka University of Technology, Nagaoka, Japan, in 1991 and 1997, respectively.

He joined Kawasaki Heavy Industries, Ltd. in 1991, and the Applied Laser Research Institute in 1993. He joined the Seiko-Epson Corporation, Nagana, Japan, in 2000. He has been working on research on low-temperature poly-Si TFTs at the Technology Platform Research Center.

Dr. Hiroshima is a member of the Society of Applied Physics.



Daisuke Abe received the M.S. degree in electrical engineering from the Osaka University, Osaka, Japan, in 1996.

He joined the Nippon Steel Corporation in 1996 and worked on DRAM development at the Semiconductor Division. He joined the Seiko-Epson Corporation, Nagano, Japan, in 1999 and has been engaged in research on low-temperature poly-Si TFT at the Technology Platform Research Center.

Mr. Abe is a member of the SID and the Japan Society of Applied Physics.

Satoshi Inoue received the B.S. degree in applied physics from the Nagoya University, Nagoya, Japan, and the Ph. D. degree in electrical and electric engineering from the Tokyo University of Agriculture and Technology, Tokyo, Japan, in 1982 and 2002, respectively.

He joined the Toshiba Corporation in 1982, and worked on research on EEPROMs, DRAMs, and ULSI technology at the ULSI Research Center. He joined Seiko-Epson Corporation, Nagano, Japan, in 1990, and has been working on research on TFTs and displays using TFTs at the Technology Platform Research Center.

Dr. Inoue is a member of the SID, Japan Society of Applied Physics, and the IEEE Electron Devices Society.

Tatsuya Shimoda received the Ph.D degree in materials engineering from the University of Tokyo, Tokyo, Japan in 1987.

He joined the Seiko-Epson Corporation, Nagano, Japan in 1977 as Research Staff and was engaged in the research and development of magnetic material, including rare earth magnets and magnet-optical memory and several devices using magnetism. He then focused on research and development on several kinds of thin-film devices for displays, printers, semiconductor devices, telecommunications, etc. He is now a Director of the Technology Platform Research Center, Seiko-Epson Corporation and a Visiting Professor with the Japan Advanced Institute of Science and Technology (JAIST), Ishikawa.

Wim Metselaar received the PhD degree in 1973 from Leiden University, Leiden, The Netherlands, in solid state physics.

He was an Assistant Professor, Department of Medical Physics, Free University, Amsterdam, The Netherlands, from 1973 until 1987. Since 1987, he has been an Associate Professor with the Electrical Engineering Department, Delft University of Technology, Delft, The Netherlands, performing research, and leading a research group on amorphous silicon thin-film solar cells. Since 1996, he has been responsible for the research and fabrication technologies related to the processing of low-temperature deposited thin silicon films.

Kees Beenakker studied chemistry and physics at Leiden University, the Netherlands. He received the Ph.D. degree at the FOM-Institute for Atomic and Molecular Physics, Amsterdam, The Netherlands, in 1974.

In 1974, he joined Philips' Research Laboratories, Eindhoven, The Netherlands. In 1982, he moved to the Philips Semiconductor Division, Nijmegen, Nijmegen, The Netherlands. In 1987, he co-founded Eurasem, a European hi-rel IC Assembly Company. Since 1990, he has been a Full Professor, Faculty of Electrical Engineering, Mathematics and Computer Science (EEMCS), Delft University of Technology, Delft, The Netherlands, a Member of the management team of the Delft Institute of Microelectronics and Submicrontechnology (DIMES), and Chairman of the Department of Microelectronics.