MASTER OF SCIENCE THESIS

Area-Efficient Readout IC with High Panel Noise Rejection for Capacitive Touchscreens

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Area-Efficient Readout IC with High Panel Noise Rejection for Capacitive Touchscreens

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December 17, 2015

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Area-Efficient Readout IC with High Panel Noise Rejection for Capacitive Touchscreens

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Abstract

As capacitive sensing provides flexible and reliable touch user interfaces for a varied set of applications, it has gained popularity over other touch sensing techniques. Consequently, capacitive touchscreens when interfaced with large display panels increases the number of channels that a readout IC has to support. As existing area-intensive touchscreen controllers are upgraded to support increased channel counts, the additional silicon area requirement increases the product cost. In addition, the touchscreen performance is highly affected by LCD noise and external noise from battery chargers.

This thesis describes the design and implementation of a new area-efficient touchscreen readout architecture. The proposed mixed-signal architecture is a compact solution implemented in a 0.15 µm CMOS process with a per channel area of 40 kµm^2. The readout architecture has a bandpass channel response to filter the strong panel noise sources more effectively. An SNR of 18 dB with panel noise in a measurement bandwidth of 200 Hz was obtained for a 4.3″ capacitive touchscreen panel with a channel pitch of 4.1 mm.

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-Rishi Raghav

ॐ सर्वे भवन्तु सुखिनः सर्वे सन्तु निरामयाः ।
सर्वे भद्राणि पश्यन्तु मा कश्चिद् दुःखभाग्भवेत ।।
ॐ शान्तिः शान्तिः शान्तिः ।।

May all be happy
May all be healthy
May all enjoy prosperity
May none suffer
Let Peace, Peace and only Peace prevail

- A quote from the Upanishad

Chapter 1

Introduction

Innovative techniques in touch sensing have revolutionized the way we interact with display devices over the past decade. The expanding market for smartphones and tablets has resulted in continuous improvements for durable touchscreens and cost-effective touchscreen controllers. With increasing size of display panels, the readout electronics has to support larger channel counts without degrading performance against various panel noise sources. This provides designers new challenges to explore better readout architectures for touchscreen controllers.

This thesis presents the design and implementation of an area-efficient touchscreen channel with improved panel noise rejection capabilities. Section 1.1 provides an overview of the different touch sensing techniques. Section 1.2 describes the touchscreen readout challenges and the design objectives for a new touchscreen controller. The last section outlines the organization of the rest of the thesis.

1.1 Touch sensing techniques

Common touchscreen solutions are based on capacitive, resistive, infrared or surface acoustic wave sensing techniques [1.1]. Resistive sensing detects a touch when two electrically conductive layers separated by a small air-gap are mechanically brought together. Resistive touchscreens are less durable and decreased optical clarity due to the wide electrode tracks has relegated it to low cost applications. Infrared sensing detects the interruption of light due to a touch object with the help of an array of LED emitters and photodiodes [1.1]. The requirement of a large screen frame for the sensor array and inaccurate sensor readings due to changes in ambient light are some of the drawbacks of this sensing technique.

Surface acoustic wave (SAW) sensing [1.3] provides another alternative for detecting touch. In this technique, ultrasound waves are continuously generated and reflected across the touchscreen surface. Some of these waves are absorbed when a user's finger or a stylus makes contact with the screen. It is possible to identify this with the help of transducers mounted on the screen edge. Though this technique provides greater accuracy and optical

clarity compared to previously mentioned techniques, it is not suitable for low cost touchscreen solutions.

Capacitive sensing [1.4] offers significant advantages compared to the above mentioned techniques. They rely on the fact that a conductive touch object can alter the effective capacitance of an electrode. The majority of touch-enabled user interfaces are based on capacitive touchscreens due to its low cost and better optical clarity. There are two different sensing mechanisms used in capacitive sensing [1.5]. Self-capacitance sensing measures the change in electrode capacitance while mutual capacitance sensing detects the change in capacitance between two electrodes due to a touch event. Self-capacitance sensing enables gesture recognition while mutual-capacitance sensing provides multi-touch functionality.

Each of the above described sensing techniques is employed in specific touchscreen applications. Resistive touch sensors are inexpensive and are used in pressure-sensitive industrial applications while infrared and SAW sensors are used in information kiosks and other interactive indoor touchscreens. With capacitive touchscreens supporting multi-touch and easy integration with the display panel, they remain the best choice as a graphical user interface for hand-held devices and other consumer applications.

1.2 Motivation and objectives

As the size of the display panel increases, the required number of channels that a readout IC has to support increases proportionally. This increases the silicon area required to implement the converter. A similar problem in neural signal acquisition readouts has been solved by using a digitally intensive architecture [1.6].

Figure 1.1 shows the block diagram of the mixed-signal feedback loop employed in [1.6]. This readout technique uses a digital lowpass filter in the negative feedback path to suppress the low frequency signal components. As a result, the ADC provides a digitized version of the high-frequency signal band while the feedback filter digitizes the low frequency signal components. A similar architecture with a mixed-signal servo loop is investigated in this thesis to reduce the chip area for touchscreen controllers.

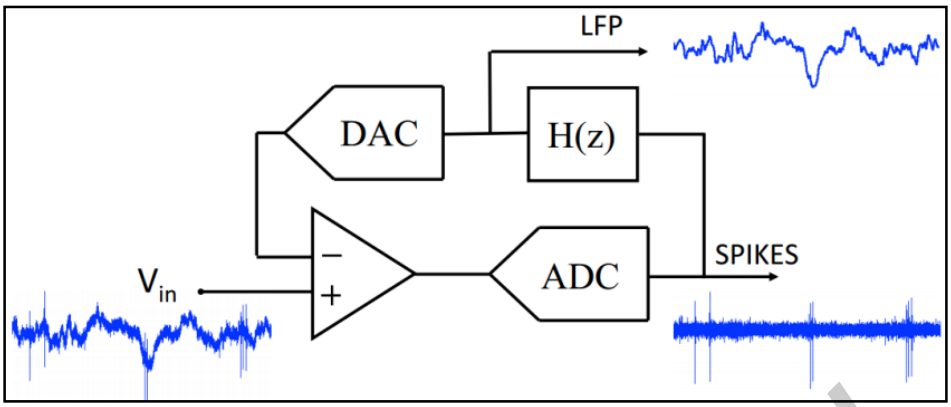

Figure 1.1: Mixed-signal feedback architecture [1.6]

In addition, touchscreen performance is highly affected by panel noise. The readout interface has to filter out LCD panel noise as well as reject the noise coupled onto the touchscreen from inexpensive battery chargers. Hence, a readout architecture that can accurately digitize the signal and simultaneously filter the unwanted panel noise is highly desirable. This thesis presents the design and implementation of an area-efficient capacitive touchscreen readout IC with high panel noise rejection capabilities.

1.3 Organization of thesis

The rest of the thesis is organized as follows. Chapter 2 describes a RC-based circuit model for touchscreens and elaborates on the capacitive touch sensing techniques. Chapter 3 reviews the state-of-the-art capacitive touch controllers and outlines the features for the proposed readout IC. Chapter 4 describes the readout architecture with system-level simulations. Chapter 5 presents the circuit and layout implementation details of the converter. Chapter 6 reports the measurement results of the test-chip and Chapter 7 concludes this work and outlines some possibilities for future work.

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Chapter 2

Touchscreen Fundamentals

This chapter describes the touchscreen sensor details and other concepts related to touch sensing. Section 2.1 explains the structure of a touchscreen panel (TSP) while section 2.2 describes the sensing techniques employed in touchscreen readouts. Section 2.3 shows an RC model of the touchscreen and finally section 2.4 discusses panel noise sources and its impact on touchscreen performance.

2.1 Structure of Capacitive TSP

Figure 2.1 shows an example capacitive TSP consisting of a two-layer grid of conductive electrodes patterned on a pair of plates separated by a dielectric layer [2.1]. The electrodes are made of indium/fluoride tin oxides as they are highly transparent and electrically conductive (< 100 Ω/□) [2.2].

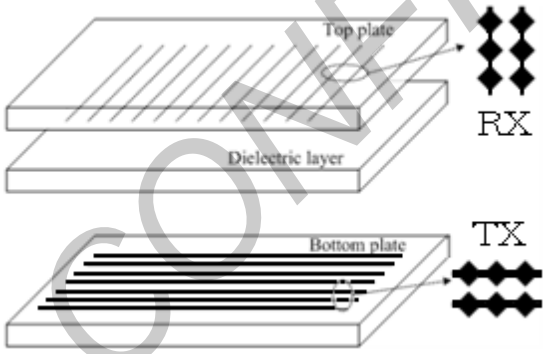

Figure 2.1: Structure of a capacitive TSP [2.1]

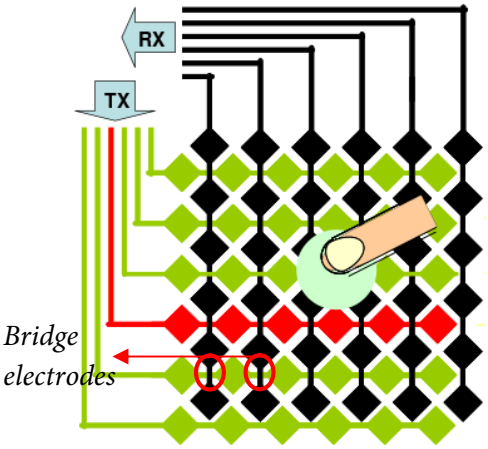

Figure 2.2: TSP with a diamond pattern

The sensing lines (RX electrodes) are patterned on the top plate while the driving lines (TX electrodes) are patterned on the bottom plate. The RX electrodes are patterned on top to reduce the noise coupled from the LCD panel. In addition, the wider TX lines act as a shield and further reduce the noise coupled from the display section. Compared to a rectangular electrode pattern, an interlocking diamond shaped pattern as shown in Figure 2.2 offers better touch sensitivity [2.3]. This pattern is implemented on a single electrode layer using bridge electrodes at the overlapping regions between the driving and sensing

electrodes. These bridge electrodes are separated from the driving electrodes by a dielectric material.

2.2 Capacitive Sensing Principles

For capacitive touchscreens, a touch event results in a change in the electrode capacitance that can be determined by using self and mutual capacitance sensing techniques. The first technique (in Figure 2.3) measures the change in the RX electrode capacitance while the second technique (in Figure 2.4) measures the change in the mutual capacitance between the TX and the RX electrodes. This is better illustrated in the below figures that show the variation in electric field due to a touch stimulus for both the sensing modes.

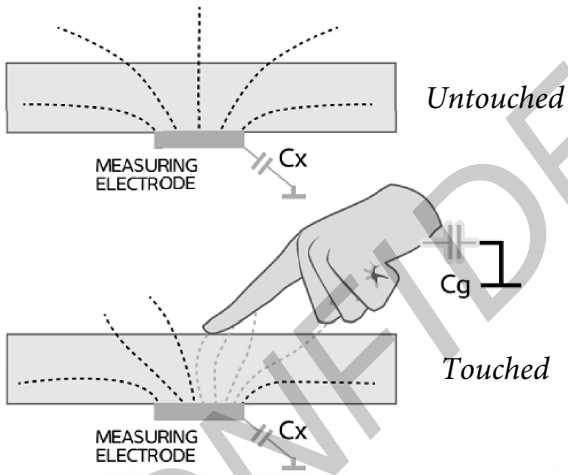

Figure 2.3: Self-capacitance sensing [2.4]

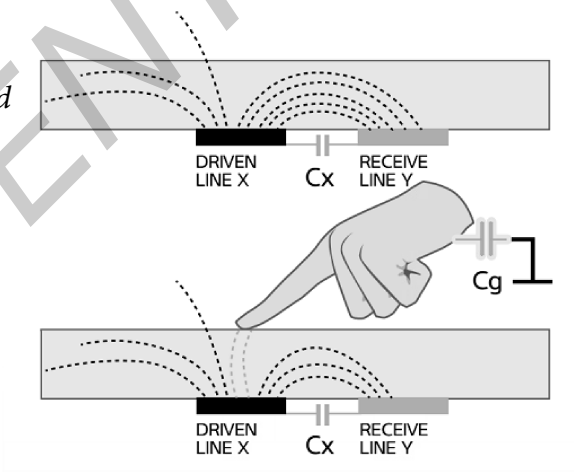

Figure 2.4: Mutual-capacitance sensing [2.4]

In a self-capacitance measurement, the touch object increases the net capacitance at the RX electrode. In contrast, the touch object decreases the mutual capacitance due to the reduced coupling between the TX and the RX electrodes. The readout electronics measures the change in the self- or mutual-capacitance to determine the strength of the touch stimulus.

2.3 Circuit Model for Touchscreens

TX and RX electrodes of a touchscreen can be modelled as distributed RC wire segments [2.5]. The entire touchscreen can then be divided into a grid composed of multiple RC sections. Figure 2.5 shows one such RC segment.

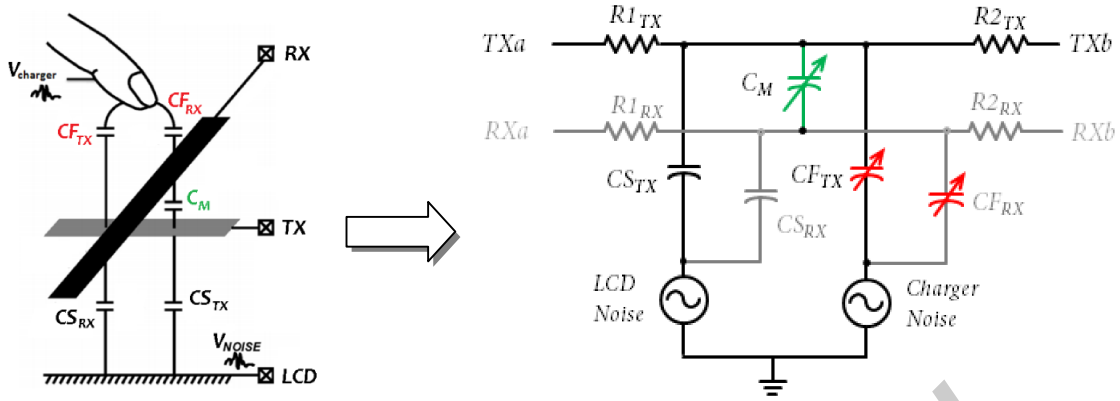

Figure 2.5: Distributed model of TSP

The TX electrode segment consists of two resistors ($R1_{TX}$, $R2_{TX}$) and two capacitors (CS_{TX}, CF_{TX}). Similarly, resistors $R1_{RX}$, $R2_{RX}$ and capacitors CS_{RX}, CF_{RX} model the RX electrode. The parasitic capacitance between the electrodes and the LCD panel is modelled by CS_{TX} and CS_{RX} while the capacitors CF_{TX} and CF_{RX} model the additional capacitance due to a touch stimulus. C_M represents the mutual capacitance between the TX and the RX electrodes. LCD panel noise couples to the electrodes via the CS capacitors while external noise such as those from battery chargers couple to the electrodes via the CF capacitors during a touch event.

The distributed RC touchscreen model can also be converted to an equivalent lumped circuit as shown in Figure 2.6 and Figure 2.7. R_{TX} and C_{TX} represent the TX electrode resistance and the parasitic capacitance to the panel while R_{RX} and C_{RX} represent the same for the RX electrode.

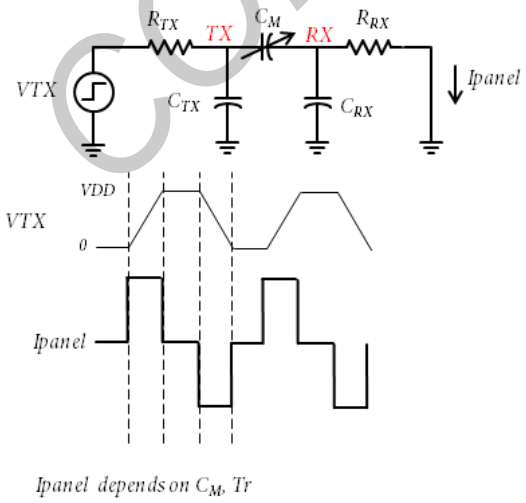

Figure 2.6: Mutual-capacitance measurement

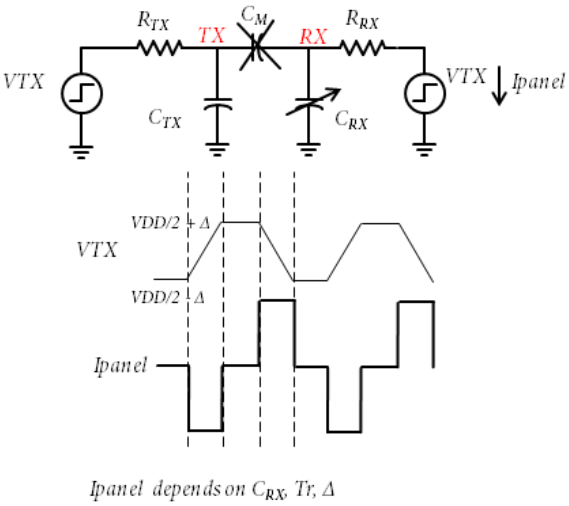

Figure 2.7: Self-capacitance measurement

Figure 2.6 shows the mutual-capacitance measurement principle using the lumped circuit model. The TX electrode is driven by a voltage source (V_{TX}) with a ramp-like waveform while the RX electrode is connected to ground. The increasing and decreasing voltage ramps on the TX line generates a panel current whose amplitude is dependent on the ramp slew rate and the mutual capacitor C_M. A touch stimulus at the intersection of a TX and a RX electrode decreases the mutual capacitance resulting in a reduction in the panel current amplitude.

Figure 2.7 shows the self-capacitance measurement principle. To cancel the effect of the mutual capacitor, the voltage at both the terminals of C_M is made equal by driving the TX and the RX electrodes with identical voltage sources. The circuit simplifies to a RC circuit with the TX drive voltage and self-capacitor C_{RX} determining the panel current amplitude. The readout IC detects the change in panel current to determine the touch signal strength.

2.4 Panel Noise

The dominant noise source that interferes with capacitive touch sensing originates from display panels and battery chargers [2.6] [2.7]. LCD and charger noise have different noise profiles and couple in different ways to the touchscreen. For instance, Figure 2.8 shows the spectra of the panel current corrupted by LCD and charger noise. Depending on the panel characteristics, the frequency of the TX drive usually varies from 50 kHz to 500 kHz. As indicated in Figure 2.8, the noise floor of LCD noise is around 10 dB while charger noise is more tonal with many harmonics in the signal frequency range. The following section discusses these noise sources in some detail.

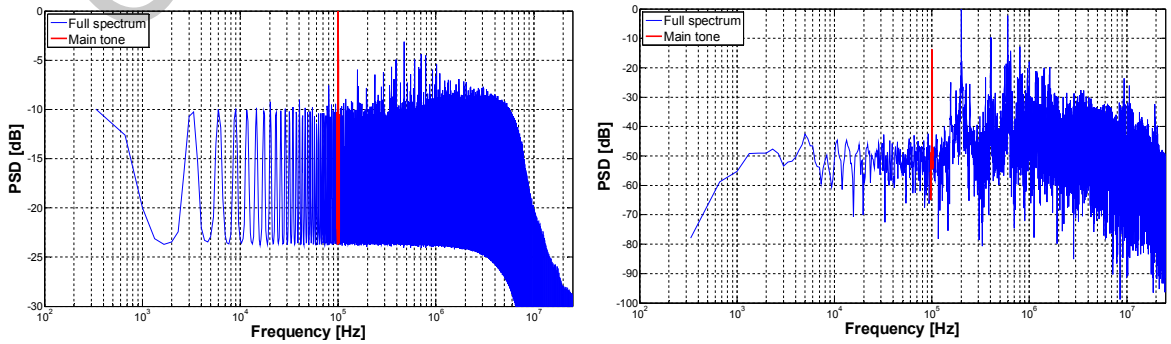

Figure 2.8: Frequency spectrum of panel current with a) LCD noise b) Charger noise

2.4.1 Display Noise

As smartphone manufacturers move towards thinner displays and sensor stack-ups, the reduced distance between the display panel and the touchscreen results in significant LCD noise coupling via the panel parasitics. Consequently, the close proximity (~0.5 mm) of the display panel and the touch sensitive layer reduces the SNR of the converter. This problem is exacerbated with on-cell and in-cell touchscreen panels where the touch sensor is integrated with the phototransistors of the LCD [2.3].

2.4.2 Charger Noise

Nowadays, manufacturers try to reduce product cost with inexpensive battery chargers. As these chargers provide insufficient suppression of power supply noise, it has resulted in decreased touchscreen performance. Charger noise physically couples onto the touchscreen during a touch event elevating the required filtering capabilities of the readout IC [2.6].

Unlike display noise, charger noise is wide-band and its spectrum can vary significantly depending on the charging current and the battery state. Various techniques such as frequency hopping, nonlinear filtering and charge pump boosted TX drive are commonly used to improve the SNR against charger noise.

To summarize, it is important for the readout IC to have strong filtering capabilities to suppress the above mentioned panel noise sources for providing an accurate estimation of the touch signal.

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Chapter 3

Literature Review

The previous chapter described the details of the touchscreen sensor and the nature of the interference that the readout circuit has to deal with. This chapter begins with a review of three touchscreen controllers whose readout techniques are commonly employed for capacitive TSP's.

Section 3.4 and 3.5 discuss sigma-delta based and other converter architectures that enable digitization with inherent noise filtering capabilities. Reviewing the pros and cons of these techniques provide a good starting point for explaining the architecture of the proposed readout IC in Chapter 4.

3.1 Two-Step Dual-Mode Capacitance Scan

The readout IC described in [3.1] combines self and mutual capacitance sensing techniques. The converter works in two phases. In the first phase, a self-capacitance measurement identifies the potential touch location. In the second phase, a mutual capacitance measurement in the selective regions of the panel given by the earlier phase determines the strength of the touch stimulus. Figure 3.1 shows the block diagram of the dual-mode capacitive sensor.

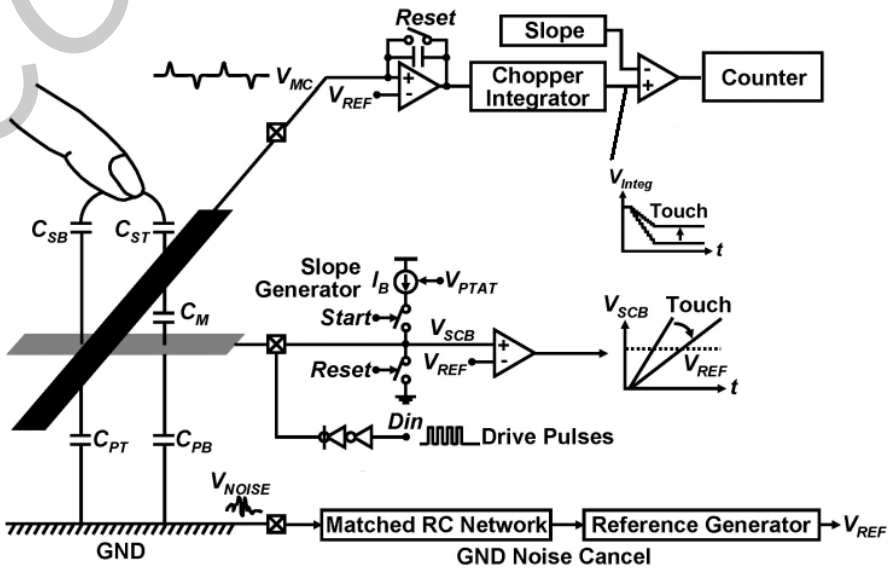

Figure 3.1: Block diagram of dual mode capacitive sensor [3.1]

For a self-capacitance measurement, the parasitic panel capacitance is charged by a constant current till the capacitor voltage reaches a reference value. This time interval is digitized using a counter to obtain a measure of the self-capacitance of the panel.

For a mutual-capacitance measurement, the TX lines are driven by a square wave voltage waveform that results in pulse-shaped voltages on the RX line due to the mutual capacitor C_M. The pulses are then integrated to generate a voltage output. This voltage level is increased by a touch event and the change in mutual capacitance can be digitized using the same time-domain counter-based ADC. The offset and flicker noise of the mutual sensing readout circuit is reduced by employing choppers in the integrator.

As shown in Figure 3.1, a matched RC network is used to replicate the LCD noise on the reference voltage. A front-end opamp with a high common-mode rejection ratio (CMRR) is used to cancel the display noise appearing as a common mode component. However, as CMRR decreases at higher frequencies, this technique will not be efficient when dealing with high frequency noise from battery chargers.

The readout scheme proposed in [3.1] achieves 40 dB SNR with a 322 Hz frame rate using a channel pitch of 1 mm. The per channel area requirement is 215 kμm^2 and the panel noise cancellation scheme is effective up to 400 Hz.

3.2 Baseline Charge Cancellation Readout Scheme

Figure 3.2 shows the analog front-end of the readout IC published in [3.2]. The SNR of the converter is improved by using a 10 V excitation signal and a code-driven parallel TX drive that is similar to spread-spectrum techniques. The use of baseline charge cancellation is particularly useful in this regard as the incoming baseline charge from multiple RX channels can be reduced significantly before it enters the first stage of the readout circuit. As the net input panel charge is integrated on the feedback capacitor C_f, baselining results in significant savings in chip area due to a smaller feedback capacitor.

Furthermore, baseline charge cancellation using a current subtraction circuit improves the dynamic range of the converter. Measurements show that the dynamic range is increased by a factor 4 and the feedback capacitor can be reduced by the same factor with baselining.

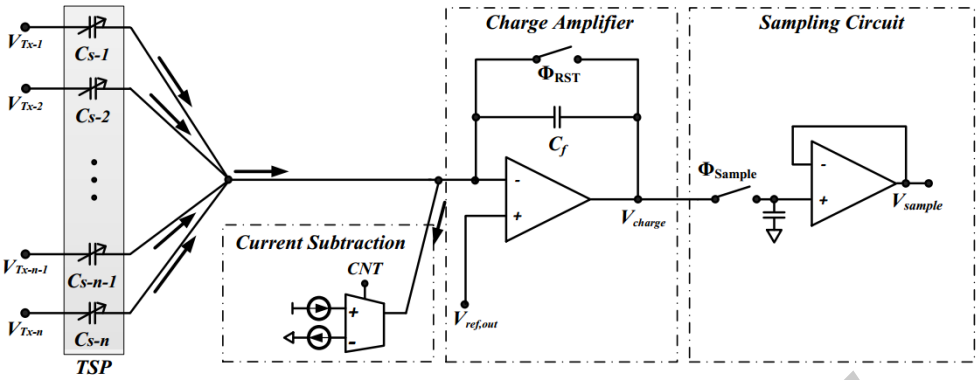

Figure 3.2: Analog front-end with current subtraction circuit [3.2]

As the readout circuit is in an open loop configuration, synchronization of the current-subtraction circuit, the TX drive and the sampling instant of the feedback charge is important. Any clock jitter, clock feedthrough or charge injection of switches has a potential impact on the converter performance.

However, the bottleneck of the converter is the limited suppression of panel noise. The benefit of reducing the feedback capacitor with baseline charge cancellation may be limited if it has to accommodate a larger input charge due to panel noise. The per channel area requirement is ~500 kμm² and the dynamic range is limited due to panel noise[1].

3.3 Filtered-Delta-Integration and Charge-Interpolation

Another analog front-end to suppress display and charger noise of a capacitive TSP is reported in [3.3]. Figure 3.3 shows the block diagram of the proposed front-end. A differential sensing scheme is employed to cancel display noise under the assumption that this noise source behaves as a common mode component across two closely spaced RX channels. In order to suppress charger noise that couples to the panel during a touch event, the readout circuit integrates the input charge multiple times to cancel the noise in the output. This technique is termed as filtered-delta-integration in [3.3].

However, the charger noise component can be strong enough to saturate the input charge amplifiers at the front-end. To avoid this, a charge interpolation technique is proposed and implemented using the shaded blocks of Figure 3.3. The main function of these blocks is to detect a saturation condition of the input charge amplifiers due to charger noise and then override the input charge to the final integrating amplifier from a previous

[1] *The authors of [2] do not report or comment on SNR measurements with a touchscreen panel*

sample. By replacing the large noisy charge packets with an interpolated value, the authors claim to improve the touchscreen performance with charger noise.

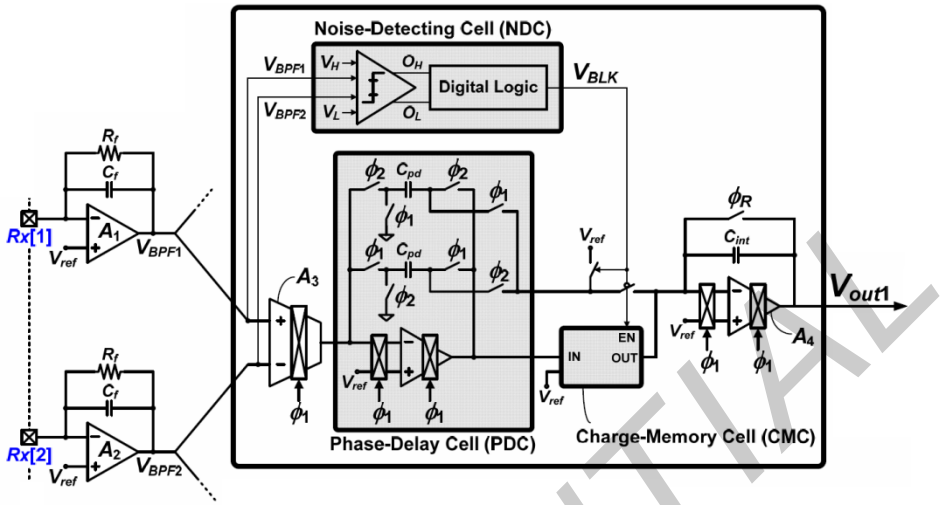

Figure 3.3: Block diagram of charge interpolating and filtered delta integration readout scheme [3.3]

[3.3] is one of the few works in literature that discusses charger noise. However, interpolating high energy input charge packets only achieves a limited SNR. The per channel area requirement of this readout scheme is ~150 kμm² and it achieves an SNR of 39 dB without panel noise at a frame rate of 120 Hz for a 10.1″ display panel.

3.4 Capacitive Sensing using Sigma-Delta Modulators

As digital circuits become faster and smaller with technology scaling, integration of digital signal processing techniques and analog circuits have resulted in low power and area-efficient readout architectures. The sigma–delta modulator is a well known architecture to convert narrow band signals using this concept [3.4]. The underlying principle to increase the resolution of the converter is to compensate a reduced accuracy per sample with a high sample rate.

Figure 3.4 shows the block diagram of a sigma-delta converter. It consists of a loop-filter and a single/multi-bit ADC in the forward path and a low resolution DAC in the feedback path. The modulator operates at a frequency fs that is much larger than the Nyquist frequency 2·fb; where fb is the bandwidth of the input signal.

The converter achieves high resolution through oversampling and quantisation noise shaping techniques. These concepts are briefly explained as follows. Quantization results in

an error signal that can be modelled as white noise distributed over the band 0 to fs/2. This approximation is generally valid when there are many quantizer levels and the frequency of the input signal is not an integer multiple of the sample rate. If the input to the quantizer is sampled at the Nyquist frequency, the total power of the quantization error signal can be derived as $V^2_{LSB}/12$ [3.7]; where V_{LSB} represents the quantization step size. However, if the quantizer operates at a frequency fs >> 2·fb, the quantization noise within the signal band is much lower than before. The improvement in SNR within the signal bandwidth of an ideal oversampled ADC is $10 \cdot \log_{10}(OSR)$ in dB's; where OSR is the ratio of the sampling frequency to the Nyquist frequency. For example, increasing the OSR by a factor 4, results in 1-bit improvement in the converter's resolution.

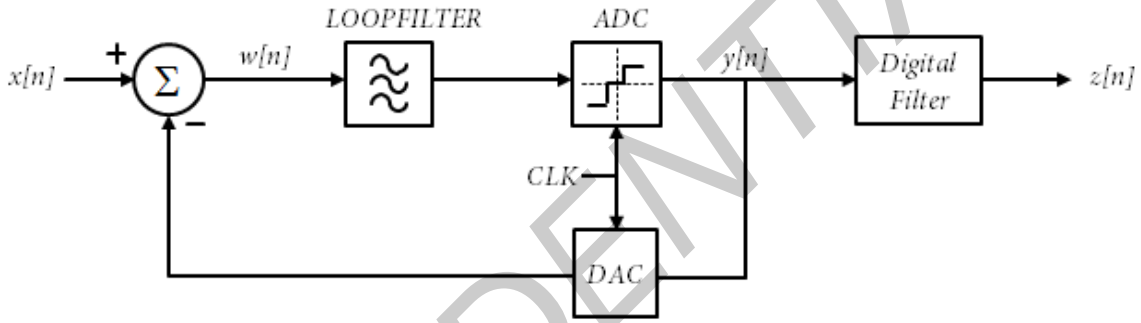

Figure 3.4: Block diagram of sigma-delta ADC

In addition to the above mentioned increase in resolution due to oversampling, the sigma-delta action also shifts the quantization energy from the signal band of interest to a different frequency range. This is known as noise shaping. The out-of-band quantization energy can be suppressed with relatively simple digital filters. The output of the sigma delta modulator (SDM) can be written in terms of the input signal X(z) and the quantization error signal Q(z) as follows:

$$Y(z)=\frac{H(z)}{1+H(z)}\cdot X(z)+\frac{1}{1+H(z)}\cdot Q(z) \qquad (3.1)$$

In the above equation, H[z] represents the transfer function of the loop filter. If H[z] is designed to have a high gain within the signal band of X(z), the signal transfer is approximately unity while the quantization error is filtered with the transfer function 1/(1+ H[z]). Configuring the loop filter as a simple integrator, $H[z] = z^{-1}/(1-z^{-1})$, results in a 1^{st} order SDM with a signal transfer z^{-1} and a noise transfer $1-z^{-1}$. Figure 3.5 shows the frequency spectrum of the SDM output. The fact that the loop filter shifts the quantisation noise energy to higher frequencies is clearly visible. The figure also plots the output spectrum

for a 3rd order loop filter. The third order SDM shows a 60 dB/decade slope with fewer idle tones compared to a 20 dB/decade slope of a 1st order SDM.

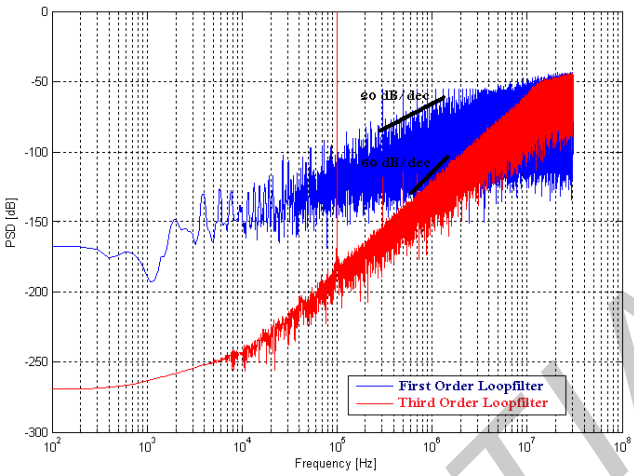

Figure 3.5: Frequency spectrum showing quantization noise-shaping for 1st and 3rd order SDM's

Section 3.4.1 and 3.4.2 discuss capacitive sensing readout IC's reported in literature based on sigma-delta principles.

3.4.1 Sigma-Delta Based Converter: Example – 1

The readout IC reported in [3.5] uses a first order discrete-time SDM to measure the change in panel capacitance due to touch. Notable features of the readout circuit include very low power consumption of 100 µW and a relatively small per channel area requirement of 100 kµm². Figure 3.6 shows the simplified circuit diagram of the converter.

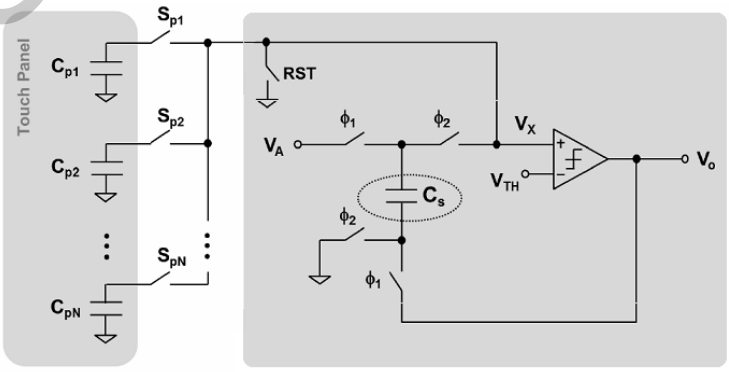

Figure 3.6: Readout circuit of touch sensor reported in [3.5]

The working of the above converter can be explained as follows. Every RX electrode of the panel is sequentially connected to the readout circuit using the switches S_{p1} - S_{pN}. The

reset signal, RST is then used to discharge the panel capacitance. In the first phase, the sampling capacitor Cs is charged by a fixed DC voltage V_A. In the second phase, Cs and the panel capacitor Cp are connected in series. The charge on Cs at the end of phase 1 and the ratio of Cp and Cs determines the input voltage of the 1-bit comparator during phase 2. This consecutive action of charge sampling and charge division is repeated for the allotted time of the RX node. Based on the value of the panel capacitance, the comparator generates different pulse patterns. The panel condition (touched or untouched) can be detected by using a simple digital counter.

Though this implementation is effective in terms of area and power, the authors in [3.5] do not consider the effect of panel noise as described in section 2.4. The large panel noise currents will require the use of a substantially larger sampling capacitor to avoid saturation or may require an attenuator in the signal path to reduce the incoming charge from the panel. The first solution increases the readout area significantly while the second solution decreases the dynamic range of the converter.

3.4.2 Sigma-Delta Based Converter: Example – 2

Figure 3.7 shows another example of a sigma-delta ADC based touch readout IC [3.6]. Though the authors do not mention the addition of panel noise for the measurements, the converter is reported to achieve a high SNR of 60 dB with a scan rate of 200 Hz.

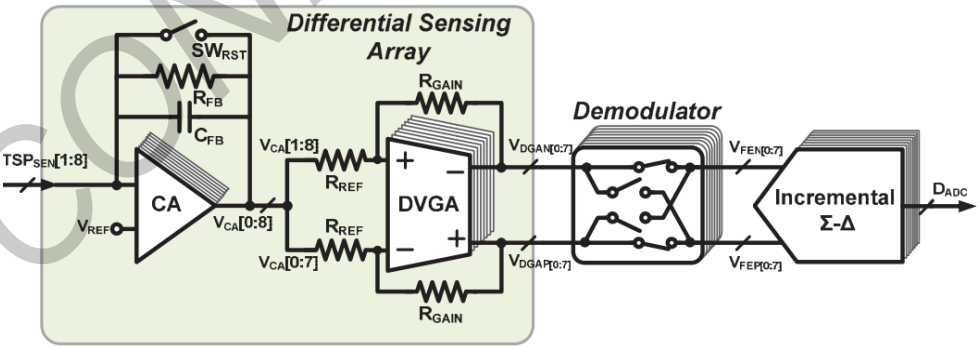

Figure 3.7: Readout circuit of touch sensor reported in [3.6]

The signal chain consists of a charge amplifier (CA), a differential gain block (DVGA), a demodulator and an incremental Σ-Δ ADC. The output voltage of the single-ended CA is proportional to the integrated value of the input panel current. The combination of the panel parasitics and the CA's feedback capacitor results in a 1st order bandpass filter response. The authors of [3.6] primarily rely on this to filter the external panel noise. Though this provides for a 20 dB/decade roll-off for out-of-band noise, panel

noise profiles as described in section 2.4 are not sufficiently suppressed. This was confirmed with system-level simulations for a converter with an integrator at the front-end followed by a first-order discrete-time SDM. SNR is reduced by more than 20 dB with the worst-cast LCD noise profile while charger noise saturated the integrator output (with a sampling capacitor of 20 pF and 5V supply voltage).

The next section of the signal chain converts the single ended CA output to a differential input for the incremental Σ-Δ ADC. The ADC is a 2nd order Σ-Δ modulator and the number of conversion cycles set by the scan rate decides the resolution of the converter. The main drawback of the converter is the per channel area of ~300 kμm² excluding the decimation filters required to implement the analog front-end (AFE).

As inferred from the above discussion, capacitive touch readout circuits based on sigma-delta techniques offer some benefits as well as some implementation constraints to realize area-efficient converters with high panel noise suppression. Similar solutions such as bandpass Σ-Δ ADC's would improve the touchscreen performance to digitize and filter narrow band limited touch signals.

3.5 Mixed-Signal Feedback Architecture

Similar requirements of smaller readout channels and digitization in the presence of strong external noise for neural and touch sensor signals motivated the analysis of a neural signal readout IC presented in [3.8]. An important function of a neural-signal front-end is to separate the μV-level input signal from low-frequency noise sources and DC offsets as large as 50 mV. The neural signal has both low frequency (< 300 Hz) and high frequency (300 - 10 kHz) components that require simultaneous digitization. Figure 3.8 shows the block diagram of a traditional neural signal acquisition chain. It consists of a low-noise amplifier (LNA), band-pass filter and analog sample-and-hold circuitry with a multiplexer to serialize multiple channels into a single high sample rate ADC [3.8].

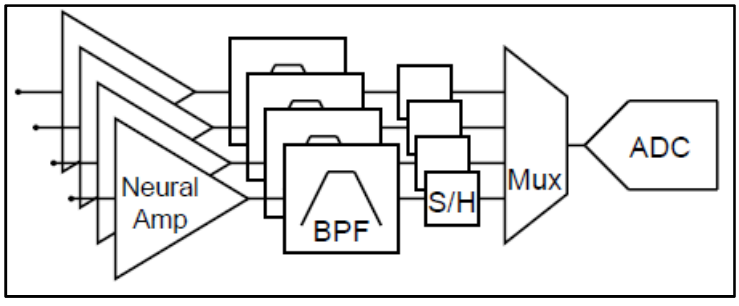

Figure 3.8: Traditional multi-channel signal acquisition chain [3.8]

To enable continuous recording of multiple sites with a dedicated front-end for every channel requires significant chip area with the above mentioned neural readout technique. For practical neural converters, the authors in [3.8] estimate that the area has to be reduced by a factor 5 if they are implemented with conventional AC-coupled instrumentation amplifiers, signal-conditioning analog filters and state-of-the-art ADC designs. In order to alleviate the above mentioned problem, a compact solution with a digitally intensive readout architecture as shown in Figure 3.9 is proposed and implemented. When compared with the state-of-the-art, the area of the AFE (0.013mm^2) is reduced by a factor 3, resulting in significant savings in area for a multi-channel readout IC.

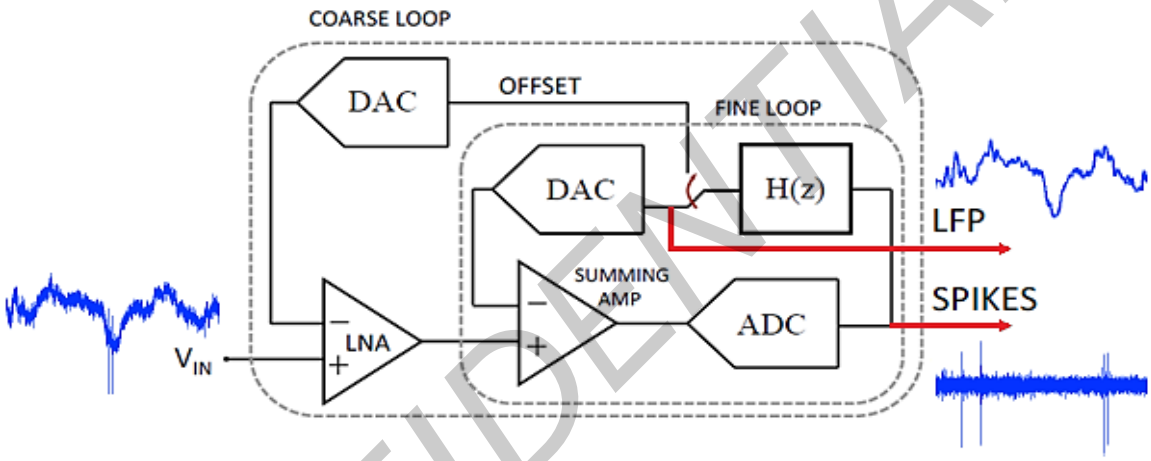

Figure 3.9: Mixed-signal feedback architecture [3.8]

This architecture replaces AC coupling capacitors and analog filters with a dual mixed-signal servo loop, which allows for input offset suppression and simultaneous digitization of both the components of the desired signal. The forward path contains a pair of broadband low-noise amplifiers and an ADC while the feedback paths of the coarse and fine loop contain a DAC and a programmable digital filter H[z]. Negative feedback via the coarse loop forces the digital low-pass filter to reproduce the very low-frequency content of Vin at the inverting terminal of the first amplifier. This achieves coarse offset cancellation and also reduces the dynamic range requirement of the first amplifier. The finer loop operating with a higher DAC resolution suppresses the residual offset and the low frequency component of the desired signal. As a result of the subtraction of this DAC output, the ADC provides a digitized version of the high frequency content of the neural signal. At the same time, the digital filter in the feedback path provides a digitized version of the low-frequency signal component. The coarse loop operates at slow rates (<1 Hz) while the fine loop operates with a bandwidth comparable to the low-frequency component of the input.

Comparison with the state-of-the-art neural converters in [3.9] clearly indicates that the chip area required for implementing the mixed-signal servo loop is significantly lower compared to conventional readout techniques. Thus, as already highlighted in section 1.2, the area-efficient mixed-signal feedback architecture is a promising design that can be adapted to touchscreen readout IC's.

3.6 Summary

Pros and cons of different touchscreen readout techniques and an area-efficient mixed-signal neural converter have been discussed in this chapter. The choice of the readout scheme depends on which among the three indices: area [3.1, 3.5, 3.8], dynamic range [3.2, 3.8] or suppression of panel noise [3.3, 3.6] is critical.

The implementation of the readout circuit with a smaller channel footprint and better immunity to panel noise are the critical issues related to touchscreen readout design. In this regard, Chapter 4 discusses the architecture of the proposed touchscreen readout IC.

3.7 References

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Chapter 4

Readout Architecture

Chapter 3 reviewed the common capacitive touchscreen sensing techniques and summarized with the desired features of the readout IC. The main challenge of the readout circuit as outlined in section 3.1 - 3.3 is to improve panel noise suppression and reduce the area of the channel. This chapter describes the readout architecture with system-level simulations to address these challenges.

The chapter is organized as follows. Section 4.1 describes the basic MATLAB model of the proposed readout architecture. Section 4.2 provides the system level implementation details and section 4.3 provides an analysis of the readout error sources.

4.1 Proposed Readout Topology

The proposed readout architecture is a combination of the mixed-signal feedback technique [4.1] and sigma-delta based converter topologies discussed in Chapter 3. A basic block diagram of the architecture is shown in Figure 4.1. It is based on a mixed-signal servo loop comprising of an N-bit ADC, a programmable digital filter H[z] and an M-bit DAC.

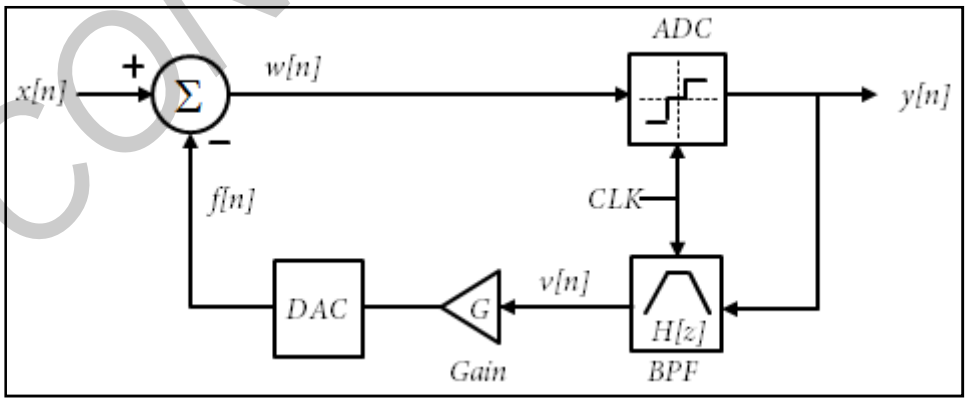


Figure 4.1: Architecture of the proposed capacitive touch sensing readout IC

The operation of the converter to digitize and filter the input panel current using a servo control loop can be explained as follows. The loop digitizes the difference between the input signal x[n] and its estimate f[n] (generated via negative feedback) using an N-bit ADC. The ADC and the digital blocks in the feedback path operate with a sampling frequency greater than the Nyquist frequency to improve resolution with oversampling as

discussed in section 3.4. The bit-stream of the error signal is processed by a programmable digital filter H[z]. As the touch information is amplitude modulated with a carrier frequency set by the TX drive, the generated estimate f[n] can be made to track the input signal in a small bandwidth by configuring H[z] as a bandpass filter. The digital filter is programmed with a center frequency equal to the TX frequency to obtain a bandpass channel response and suppress the effect of panel noise on the converter.

The gain (G) in the feedback path compensates for the passband attenuation of the digital filter and determines the loop-gain to reduce the error signal, w[n] to zero. The final block of the converter is an M-bit DAC that generates the feedback signal f[n] at the input summation node. The mixed-signal approach and the absence of integrators in the AFE results in significant area savings as large capacitors to accommodate panel noise as discussed in section 3.4 can be avoided.

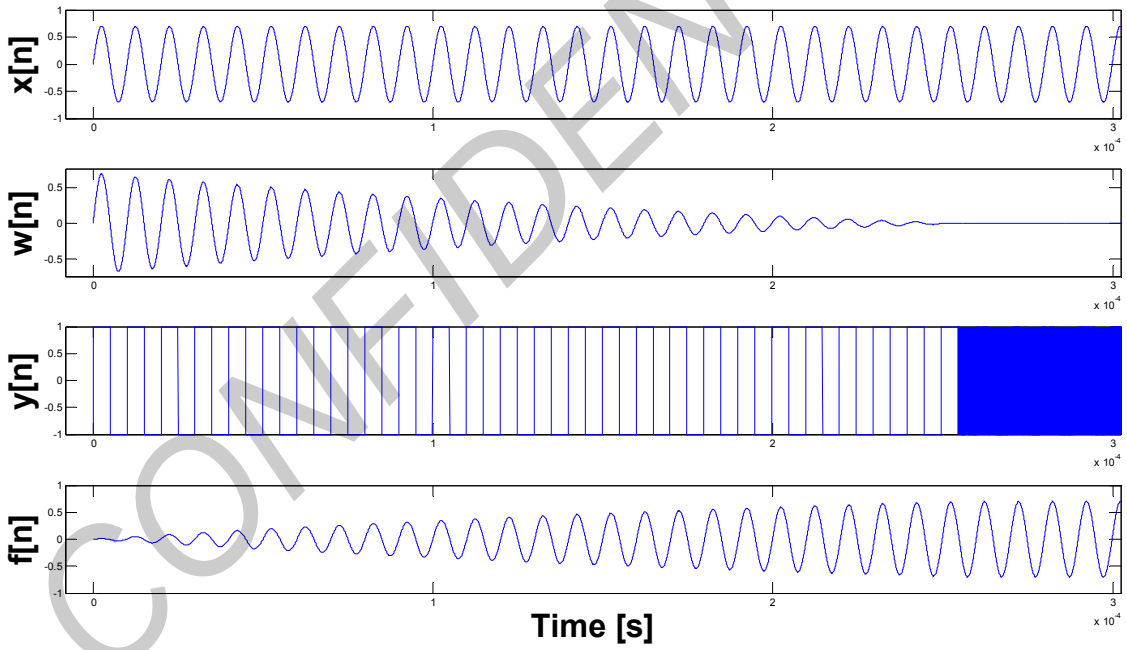


Figure 4.2: Transient simulation with 1-bit ADC and no quantization in feedback path

Figure 4.2 plots the waveforms of a transient simulation of the proposed converter with a 1-bit ADC at a sampling frequency of 50 MHz (OSR=250). The input to the converter is a –3 dB_{FS}, 100 kHz tone and the BPF is programmed with a center frequency of 100 kHz and a bandwidth of 2 kHz. The effect of the DAC resolution on the converter is described later and it is replaced by a unity gain block in the current simulation. Figure 4.2.b shows the error signal w[n] decaying to zero due to the negative feedback action of the loop while Figure 4.2.d shows the generated feedback signal as a close replica of the input signal in steady state.

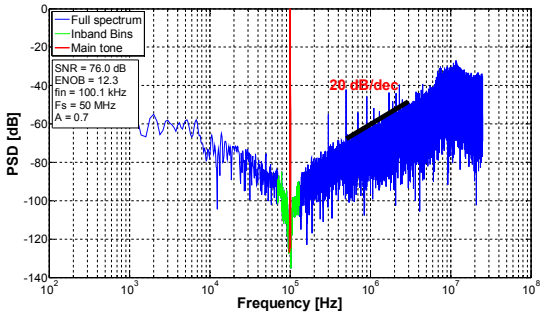


Figure 4.3: Frequency spectrum at ADC output, y[n]

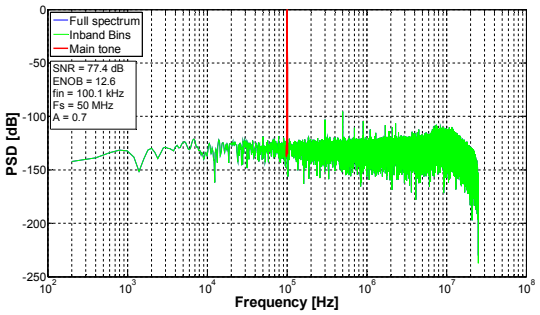


Figure 4.4: Frequency spectrum at BPF output, v[n]

Figure 4.3 and Figure 4.4 plot the frequency spectrum at the output of the ADC and the BPF respectively. Unlike an ideal oversampled converter where the loop-filter defines a distinct STF and NTF, the proposed topology filters the input and the quantization errors of the ADC and the DAC with the same transfer function: 1/(1+ H[z]). With a 2^{nd} order BPF in the feedback path, the ADC output shows a first-order noise shaping of 20 dB/decade. To take advantage of the noise shaping, an oversampled converter employs a digital filter after the modulator. However the proposed topology can reuse the BPF in the feedback path to suppress the out-of-band quantization noise. The BPF output, v[n] provides a digital representation of the input signal and can be used to recover the touch information modulated over the TX carrier.

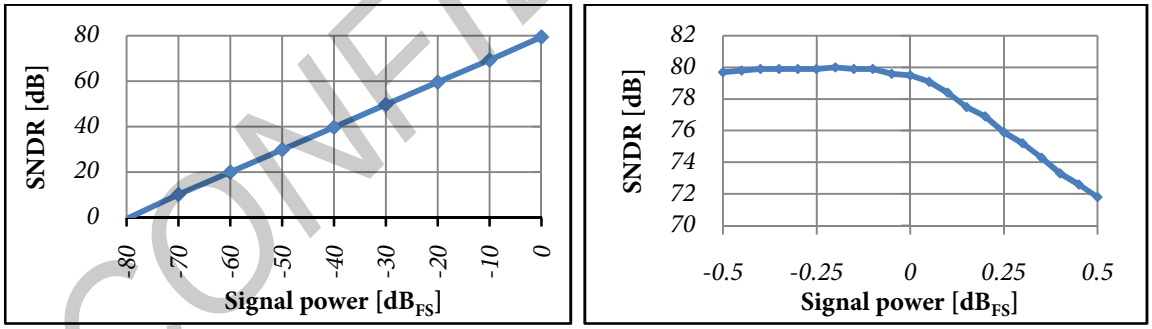


Figure 4.5: Simulated SNDR at BPF output with 1-bit ADC

Figure 4.5 plots the variation in SNDR with the input signal strength. As is the case with a conventional oversampled converter (with a single bit quantizer), the SNDR drops when the input signal is close to the maximum limits of the feedback DAC. This input signal strength is referred to as the overload level. By configuring the DAC range according to the expected input panel current amplitude, any reduction in SNR due to the overload effect can be avoided. For input signals greater than the overload level, the DAC can no longer track the input and the modulator only recovers when the input signal strength is reduced below the overload level.

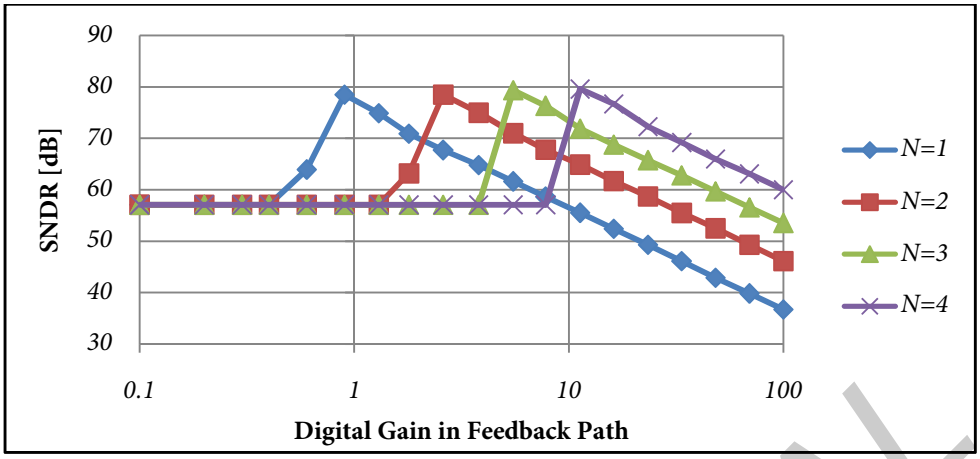


Figure 4.6: SNDR versus digital gain in feedback path with N-bit ADC (DAC modelled as a unity gain block)

Figure 4.6 plots the SNDR of the converter for different values of the digital gain in the feedback path (on a log-scale). Depending upon the ADC resolution, there is an optimum gain that can maximize the SNDR of the converter. If the gain is too small, the feedback signal does not track the input in amplitude, resulting in a large error signal, w[n]. Similarly, if the gain is too large, the modulator is overloaded and results in increased distortion components in the ADC and the BPF output.

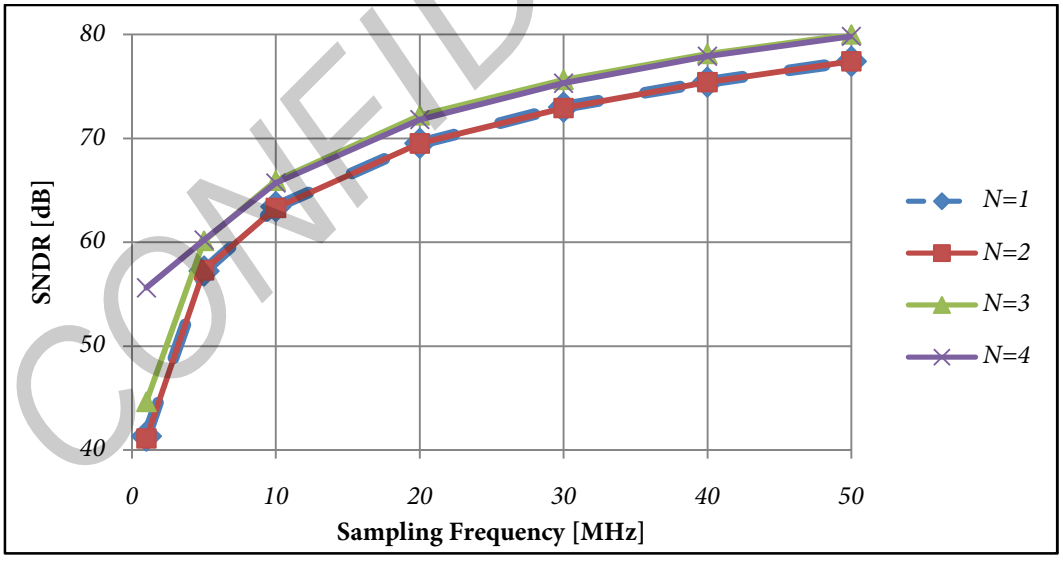


Figure 4.7: SNDR versus sampling frequency with N-bit ADC (DAC modelled as a unity gain block)

Figure 4.7 plots the improvement in SNDR with increasing sampling frequency for a single-bit and multi-bit ADC in the loop filter. The improvement in SNDR with oversampling as discussed in section 3.4 is evident in the above graph.

Compared to oversampling and noise shaping, the improvement in performance with a multi-bit quantizer in the servo loop is limited. This can be explained by observing

the transient simulation waveforms of the converter with a single bit and a 4-bit ADC in the servo loop as shown in Figure 4.8. For the case of a single-bit ADC, the oversampling action results in a bit-stream with more number of 1's and -1's at the positive and negative input signal excursions and an equal number of 1's and -1's near the mid-level. If the single bit ADC is replaced by a multi-bit quantizer along with an increase in the loop-gain, the bit-stream shows a similar pattern in steady state as before but with a different quantization step as set by the ADC resolution. Coupled with the fact that the quantization noise is bandpass filtered before it reaches the DAC, improvement in SNR with multi-bit quantizers is limited.

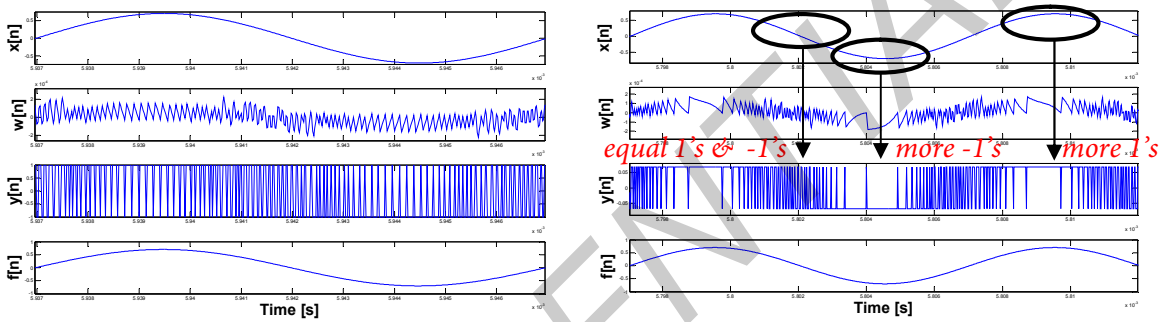


Figure 4.8: Transient simulation with 1-bit ADC (left) and 4-bit ADC (right)

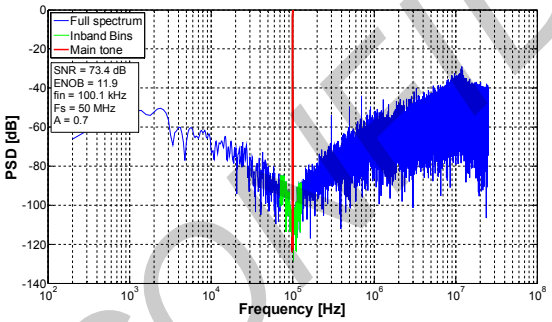


Figure 4.9: Frequency spectrum at ADC output

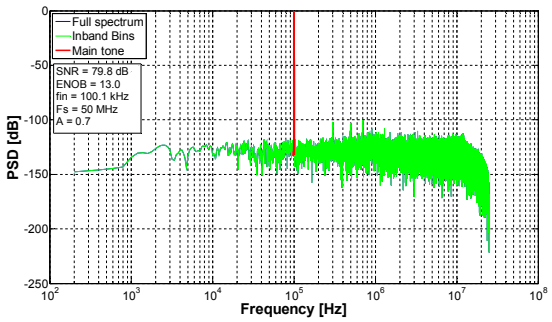


Figure 4.10: Frequency spectrum at BPF output

Figure 4.9 and Figure 4.10 show the output spectra with a 4-bit ADC in the servo loop. The improvement in SNDR is 2.4 dB, when compared with a single bit quantizer.

Figure 4.11 shows the limited improvement in SNDR with a multi-bit ADC as discussed before. The graph also shows the reduction in SNDR as the resolution of the DAC is reduced. Figure 4.12 shows the output spectrum with a 10-bit DAC in the feedback path. The noise floor of the out-of-band quantisation noise is significantly higher when compared with the earlier simulation of Figure 4.9, where quantization in the feedback DAC is not considered.

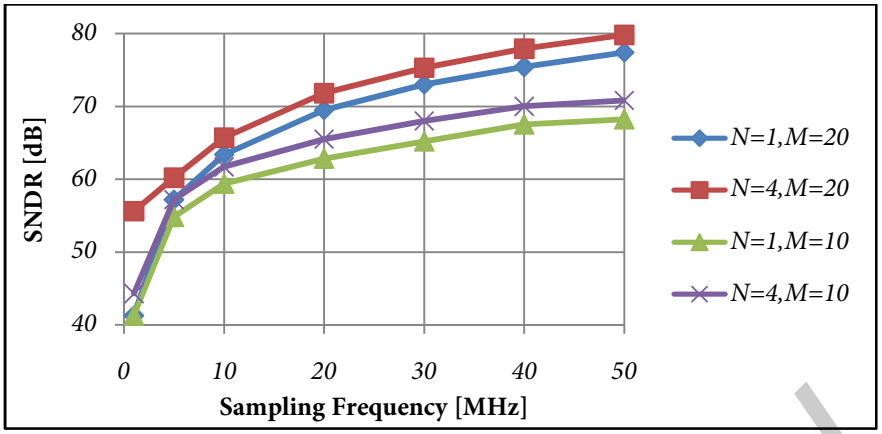


Figure 4.11: SNDR versus sampling frequency with N-bit ADC and M-bit DAC

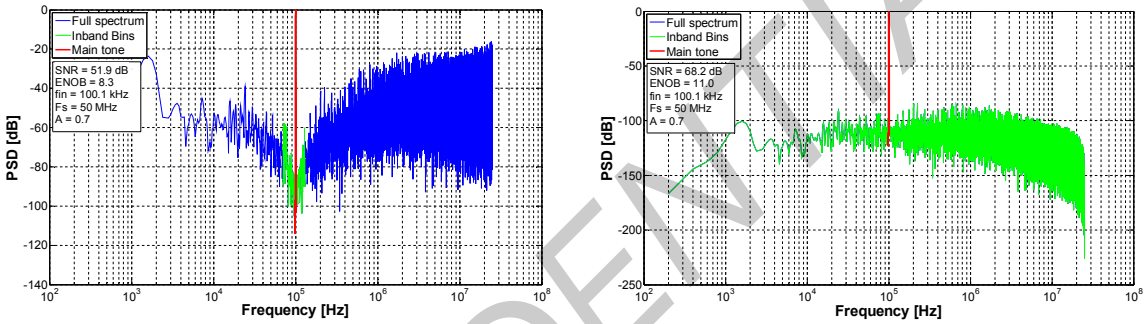


Figure 4.12: Frequency spectrum with 1-bit ADC and 10-bit DAC

The variation in SNDR with an M-bit DAC (and a 1-bit ADC) is plotted in Figure 4.13. SNDR increases linearly for sampling frequencies greater than 5 MHz and DAC resolutions better than 7-bit.

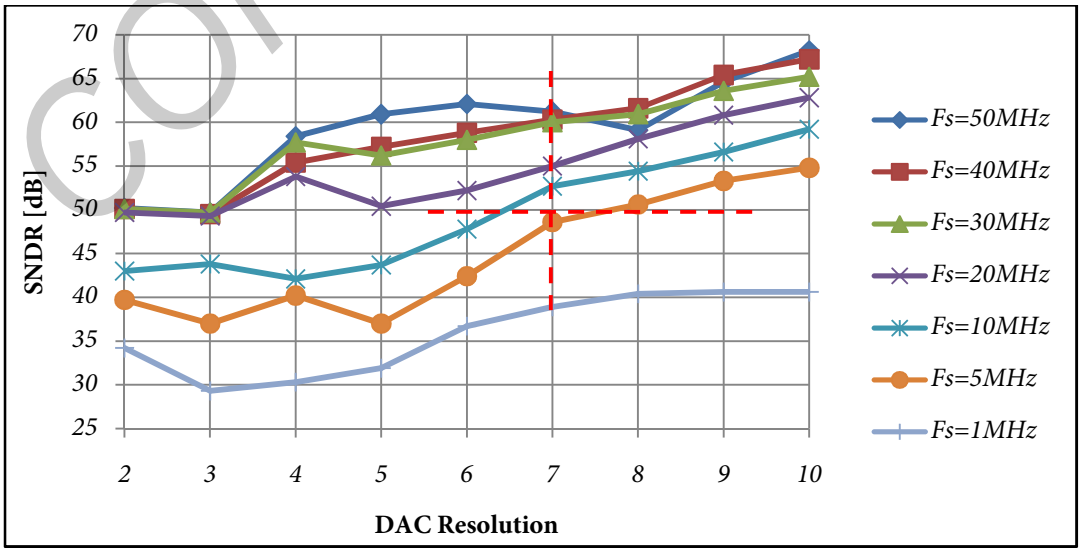


Figure 4.13: SNDR variation with multi-bit DAC at different sampling frequencies

The details of the digital filter in the servo loop are discussed next. As mentioned earlier, H[z] is configured as a bandpass filter to suppress the effect of panel noise on the converter. With the quantization noise of the ADC and the DAC shaped by a transfer function 1/(1+ H[z]), the proposed readout architecture results in a bandpass response as shown in the output spectrum plots of Figure 4.4 and Figure 4.10.

The main selection criteria for H[z] is to achieve a SNR of at least 40 dB with the worst case panel noise profiles and require the least silicon area for implementation. With regard to the latter, a FIR-based bandpass filter for H[z] requires more number of computational elements compared to an IIR filter. For example, a FIR-bandpass filter with a sampling frequency of 6 MHz and a bandwidth of 5 kHz requires ~1000 multipliers and adders compared to a single biquad section as shown in Figure 4.14 for an IIR filter with similar specifications. Also, the computational cost of FIR filters increases linearly with sampling frequency. Consequently, only IIR-based filters are considered to reduce the area requirements.

A second-order IIR filter can be implemented using a single biquad section as shown in Figure 4.14. Higher order filters can be designed by cascading multiple biquad sections. The transfer function of a biquad is given in equation 4.1.

$$\frac{Y(z)}{X(z)} = K \cdot \frac{b_1 + b_2 \cdot z^{-1} + b_3 \cdot z^{-2}}{1 + a_1 \cdot z^{-1} + a_2 \cdot z^{-2}} \qquad (4.1)$$

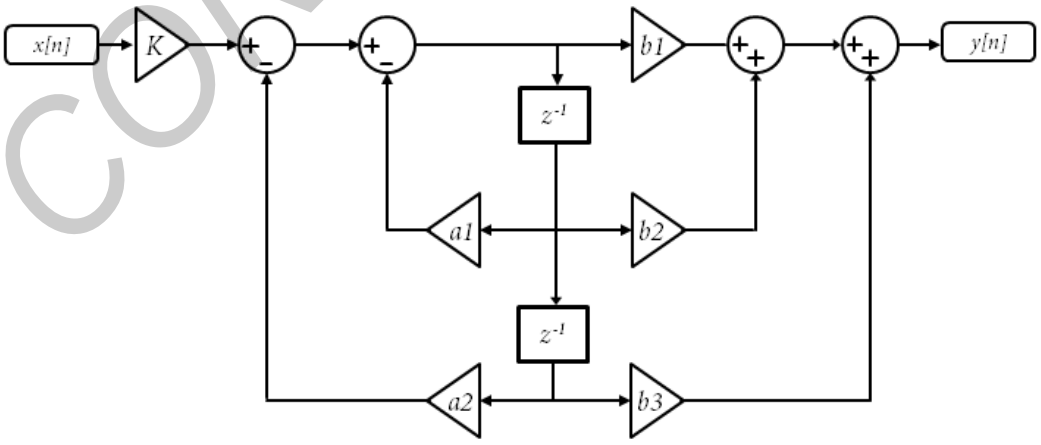


Figure 4.14: Structure of a digital biquad section

With different coefficients, the biquad can be designed for a Butterworth, Chebyshev or elliptic type bandpass frequency response. For the all the different types, a bandpass transfer results in the numerator coefficients simplifying to $b_1 = 1$, $b_2 = 0$ and $b_3 = -1$. As a result, a 1-bit input requires 3 adders and 2 multipliers for designing a second-order IIR

bandpass filter. Among the various frequency responses, the chebyshev–II filter provides maximum SNDR. The magnitude response for a 2nd order filter with 2 kHz bandwidth and a sampling frequency of 50 MHz using a single biquad section is shown in Figure 4.15.

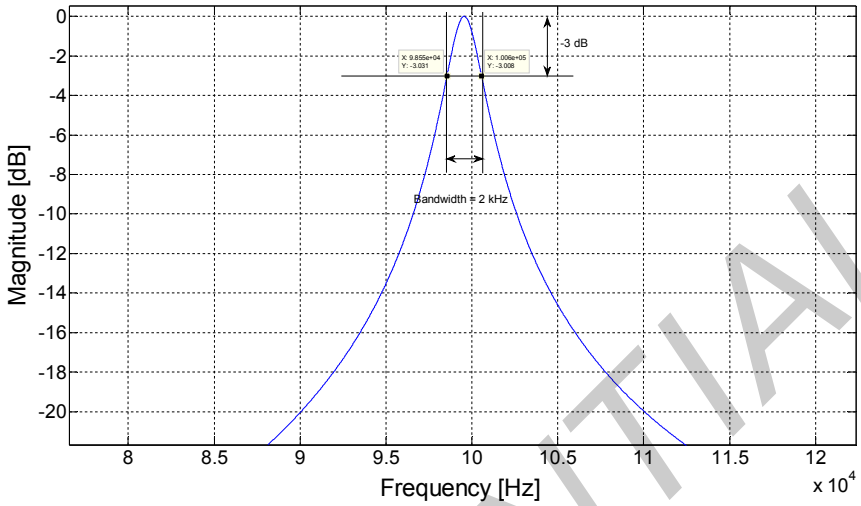


Figure 4.15: Magnitude response of Chebyshev type-II IIR filter

The digital filter also allows for flexibility to program the center frequency to a different TX drive by changing the coefficients a_1 and a_2. To reduce the area of the digital filter, we would like to implement the computational filter blocks with as few bits as possible. The variation in SNDR with the number of bits used to represent the fractional part of the adders and multipliers is shown in Figure 4.16. A fraction length of 16 bits or more limits the SNDR degradation due to rounding errors.

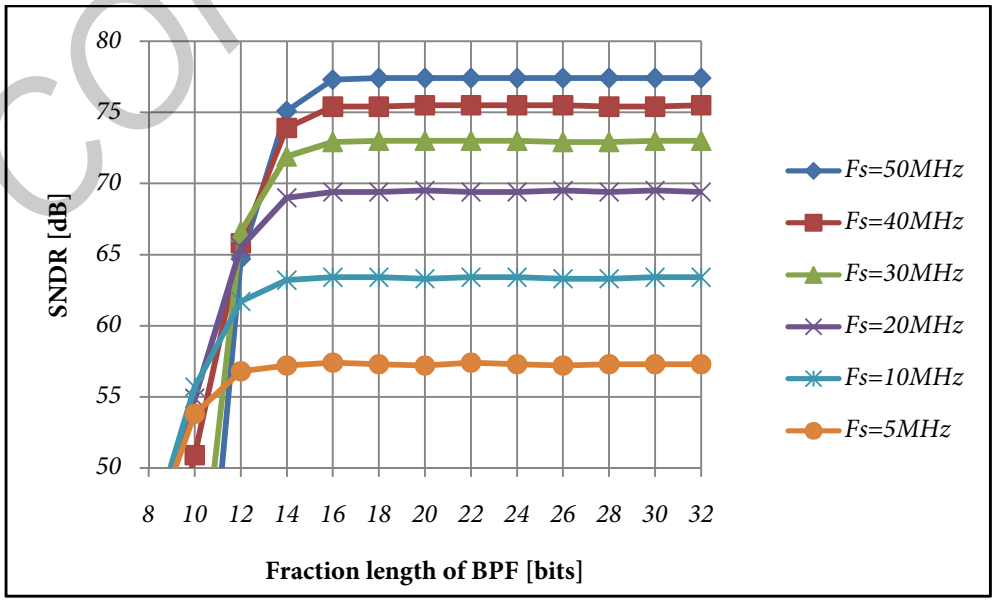


Figure 4.16: SNDR versus fraction length of BPF for different sampling frequencies

The variation in SNDR of the converter with the bandwidth of the bandpass filter is shown in Figure 4.17. It is desirable to implement a stable filter with the least fractional length and the least bandwidth to achieve maximum panel noise rejection and minimum silicon area.

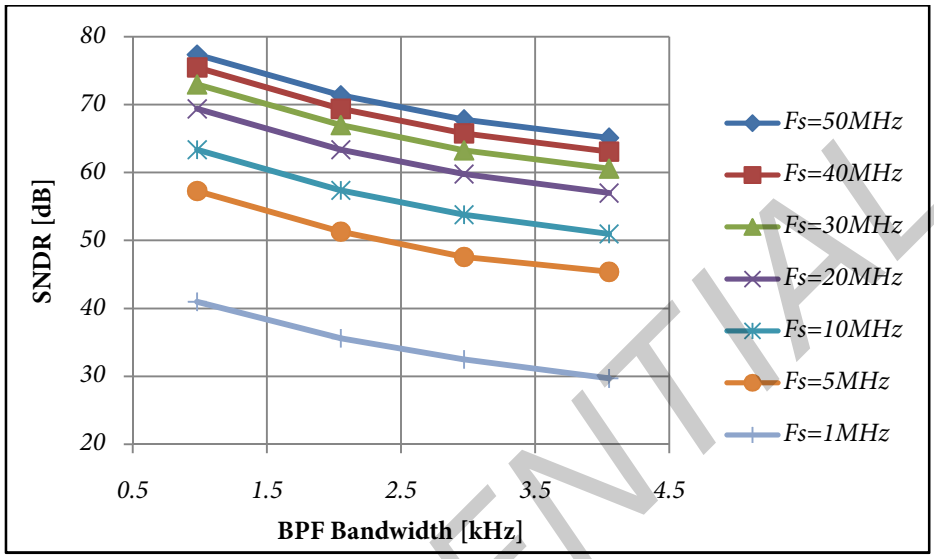


Figure 4.17: SNDR versus BPF bandwidth for different sampling frequencies

As a final simulation example, a noise tone is added to the input and its effect on the SNDR is shown in Figure 4.18. The frequency of the main tone is 100 kHz and the noise tone is 10 dB lower in amplitude at 255 kHz. The output spectrum of the BPF shows that the converter achieves a SNDR of 40 dB and suppresses the noise tone to -40 dB. The detailed block diagram of the readout architecture and the expected SNR with worst-case panel noise profiles is discussed in the next section.

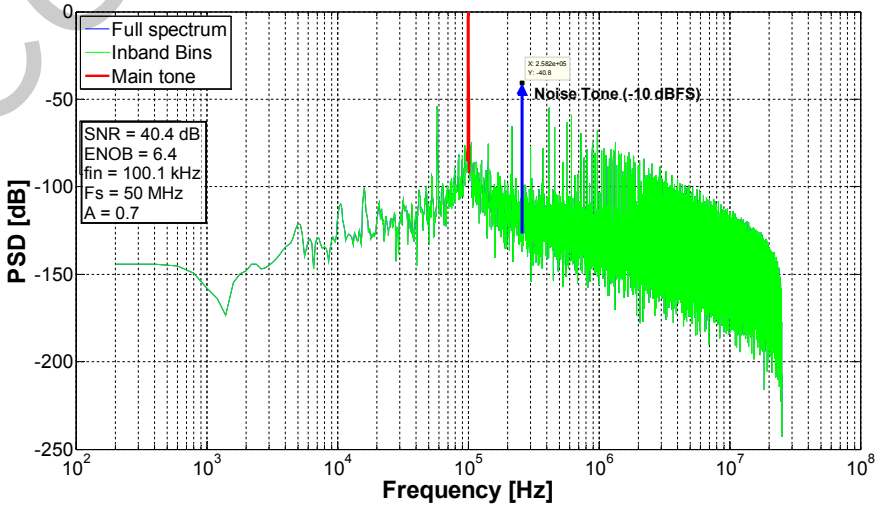


Figure 4.18: Frequency spectrum at BPF output with additional noise tone

4.2 System-Level Design

This section describes the system-level design of the touchscreen readout circuit introduced previously. Figure 4.19 shows the block diagram of the proposed converter. The TX drive and the panel capacitance determine the input panel current to the mixed-signal servo readout circuit. To achieve a SNR of at least than 40 dB in a bandwidth of 200 Hz with the worst case panel noise profiles, a 1-bit ADC and a 7-bit DAC were chosen based on the previous simulation results. The current DAC generates the feedback signal for the servo loop while the resulting error current is processed using a transimpedance amplifier (TIA) and digitized with a 1-bit ADC. The digital blocks process the ADC output bitstream to generate the input word for the DAC.

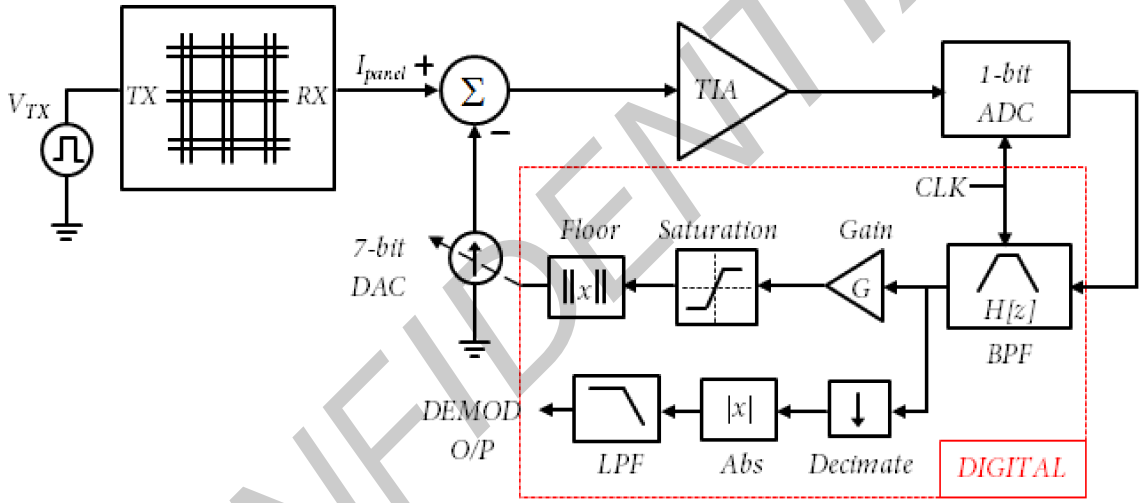


Figure 4.19: Block diagram of proposed readout architecture

The feedback action of the servo loop changes the amplitude of the DAC output relative to the input panel current. The change in panel current due to a touch stimulus results in a proportional change in the digital output of the BPF. As the touch stimulus modulates the amplitude of the filter output, an AM demodulator can be used to detect the touch signal strength.

Either an envelope or a synchronous detector can be used as the demodulator for the proposed readout circuit. An envelope detector tracks the low frequency content of the desired signal. This is achieved by lowpass filtering a rectified input to obtain the signal information. A synchronous detector [4.2] multiplies the modulated signal with the carrier to recover the input content. The desired signal is recovered easily using a low pass filter.

As the SNR obtained with the worst case panel noise profiles for both the demodulator types are comparable, the simpler envelope detector was chosen. Moreover, envelope detection is less sensitive to the phase distortion introduced by an IIR filter when compared with a synchronous detector. An optional decimation stage is added at the input of the demodulator to reduce the output data rate and area requirements of the digital lowpass filter.

Figure 4.20 shows the variation in SNDR with the input signal power for two different sampling frequencies. The converter is linear across a broad range of input power levels and the SNDR improves with higher sampling frequencies.

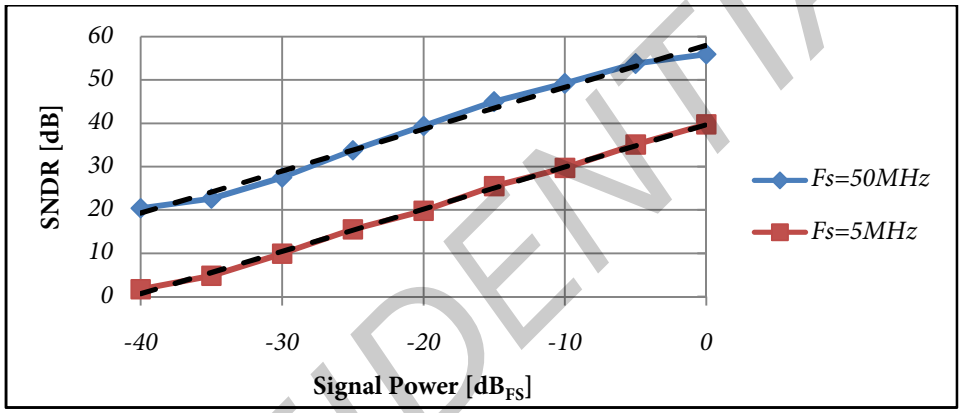


Figure 4.20: SNDR versus signal power for different sampling frequencies

Figure 4.21 shows the waveforms of a transient simulation using the panel current obtained from spice simulations with the panel models described in section 2.3. The TX line is driven by a 5 V square wave at 100 kHz. This results in a panel current with the same frequency as indicated in blue. A touch event reduces the mutual capacitance between the TX and the RX lines, thus resulting in a decrease in the panel current amplitude. The converter responds to this change by reducing the feedback current through the IDAC as indicated in red. The response time for the feedback action to take effect is around 1 TX cycle, which corresponds to 10 µs in this case.

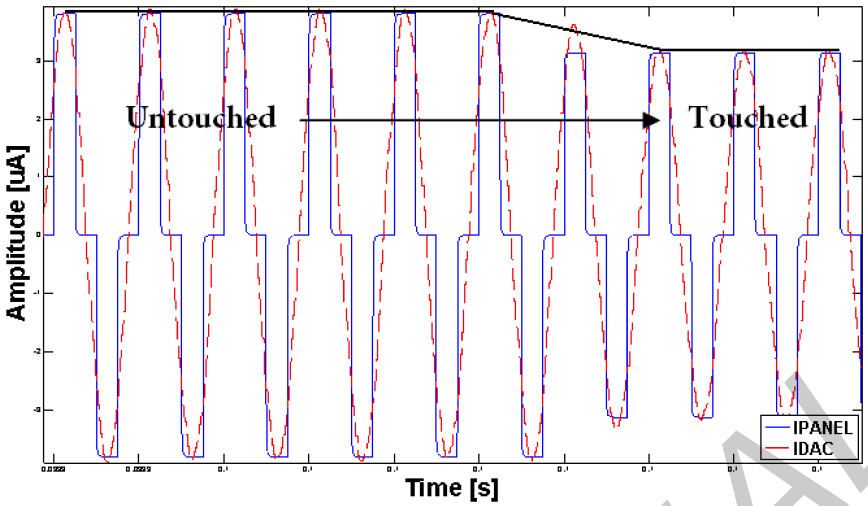


Figure 4.21: Transient waveforms of servo control loop

Figure 4.22 shows the effect of charger noise on the converter. As charger noise is coupled to the panel during a touch event, the panel current amplitude can increase by an order of magnitude. But the converter with its bandpass response suppresses the effect of this panel noise. Demodulation of the BPF output (shown in red) results in a SNR of 40 dB in a 200 Hz bandwidth with an OSR of 30. The SNR definition used for touchscreens [4.3] is given in Appendix A.

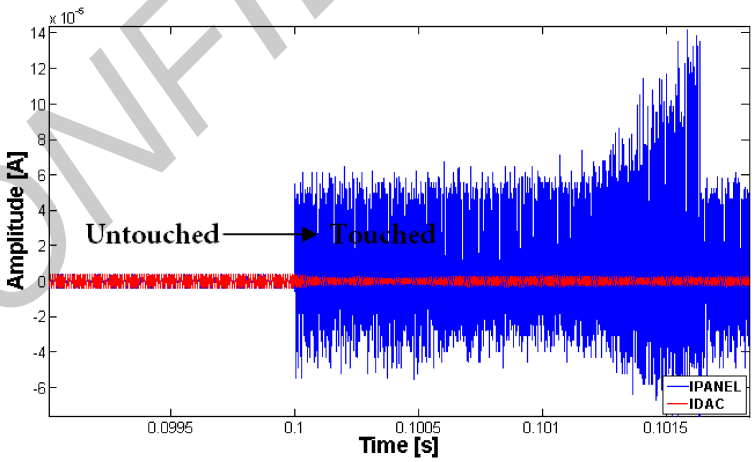


Figure 4.22: Transient waveforms of servo control loop with charger noise

Figure 4.23 shows a plot of SNR versus TX frequency for different noise profiles. The SNR obtained from the proposed converter is compared with a reference converter comprising of a first-order lowpass filter and a 7-bit ENOB 1st order sigma delta modulator. The comparison clearly indicates the better panel noise suppression achieved with the bandpass channel response of the proposed converter.

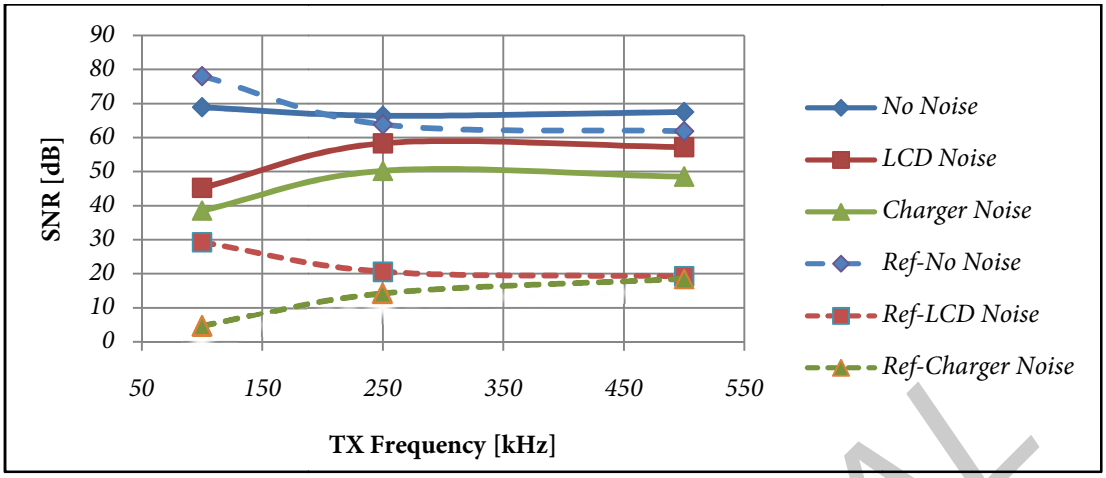


Figure 4.23: SNR versus TX frequency for different noise profiles

4.3 Analysis of Circuit-Level Error Sources

This section discusses the important circuit-level error sources that can have an impact on the performance of the converter. These error sources include offset of analog blocks, non-linearity due to large panel capacitance, mismatch in IDAC elements and sensitivity of the converter to additional delay in the loop.

4.3.1 Offset

The circuit implementation of any analog block results in an offset as a source of error due to systematic and random mismatch between the circuit components. The major sources of offset error in the proposed converter of Figure 4.19 can be listed as follows:

1. *Mismatch in the unit current elements of the IDAC*
2. *Offset of the opamp used for the TIA*
3. *Offset of comparator*
4. *Leakage currents originating from ESD protection circuitry connected to the RX lines of the readout circuit*

Figure 4.24 plots the variation in SNR against an equivalent offset modelled at the TIA output at different sampling frequencies. The plot clearly indicates that the loop is not as effective as before in the presence of a large DC offset. Figure 4.25 shows the frequency spectra of the ADC and BPF outputs at a sampling frequency of 30 MHz with a 50 mV output-referred TIA offset. The ADC output spectrum has an offset and an increased

distortion component at the input harmonics. This results in a 10 dB decrease in the SNR of the converter at the BPF output.

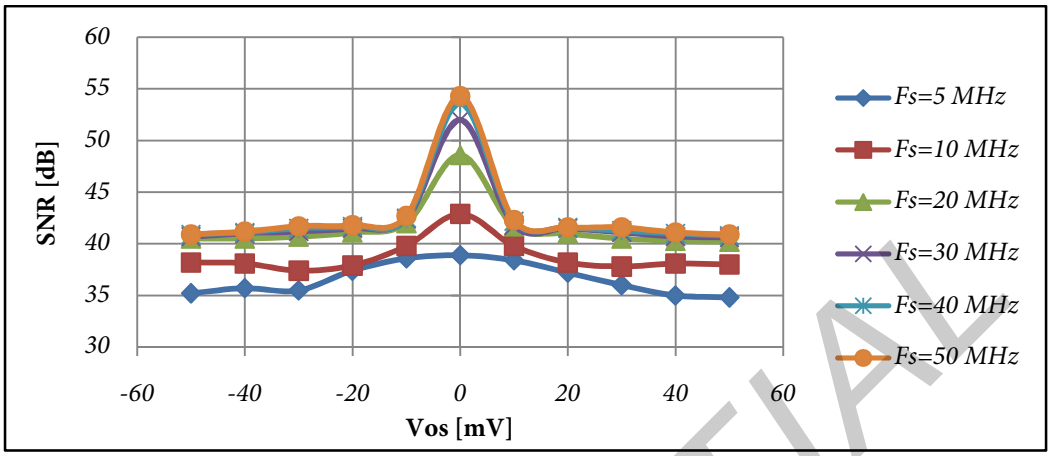


Figure 4.24: SNR versus equivalent offset at TIA output (N=1, M=10)

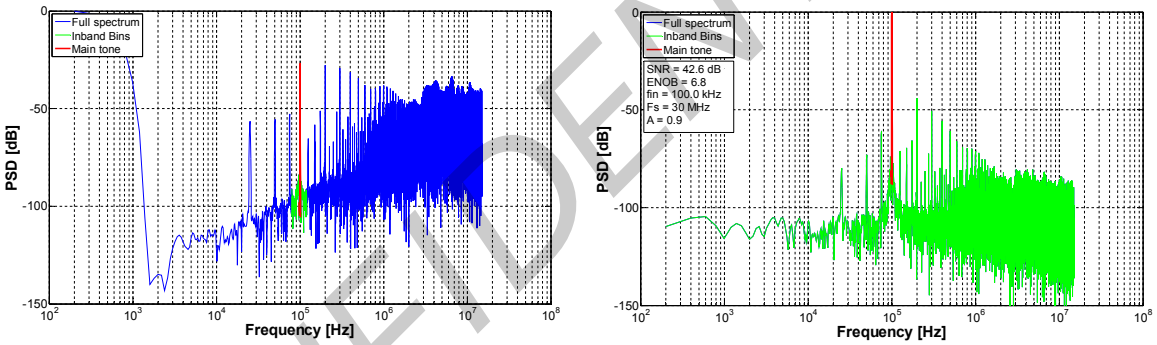


Figure 4.25: Frequency spectrum with 50 mV offset at TIA output a) ADC output b) BPF output

An easy solution to negate the effect of offset error is to trim the DAC using the digital output of the comparator. This can be done in an initial calibration phase, before the TX drive is made active. An alternate solution as shown in Figure 4.26 is to modify the transfer function of the feedback path with the addition of an accumulator to track the DC offset of the converter and dynamically change the DC value of the feedback current. This solution is more robust than the first solution to track temperature and supply voltage variations but increases the per channel area requirement.

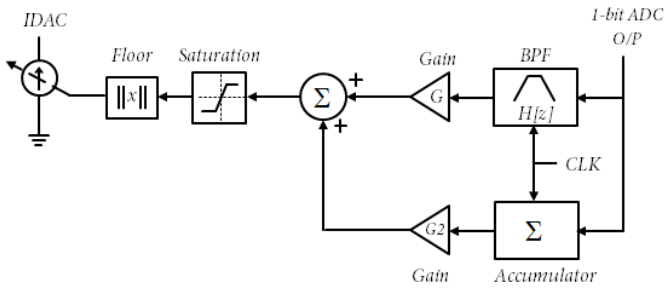


Figure 4.26: Introduction of accumulator for offset cancellation

Figure 4.27 shows the output spectra using the offset cancellation scheme of Figure 4.26. The ADC output spectrum shows a reduced DC offset and distortion component at the input harmonics compared to Figure 4.25 and the BPF output has a SNR comparable to the case with zero offset.

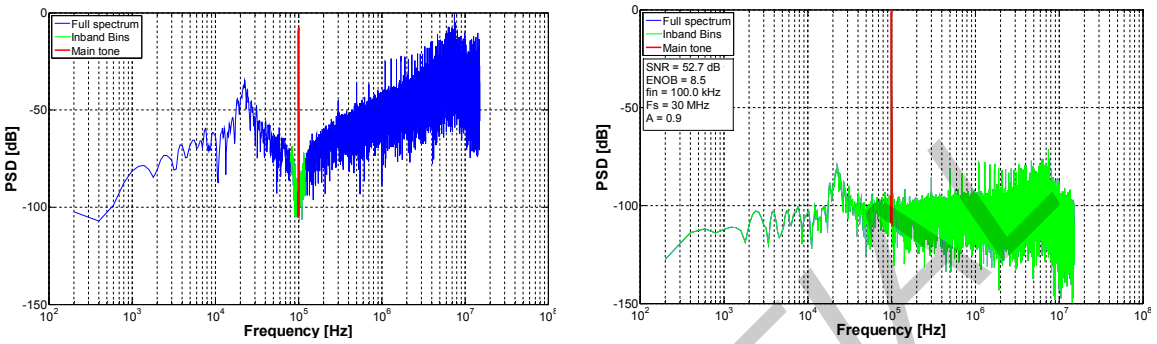


Figure 4.27: Frequency spectrum with offset cancellation a) ADC output b) BPF output

4.3.2 Panel Capacitance

The error signal of the feedback loop is converted from a current domain to a voltage input for the ADC using a transimpedance amplifier. The effect of the large panel capacitance on the TIA is discussed in this section. Figure 4.28 shows the interface schematic of the panel to the readout circuit. I_{in} represents the input panel current while C_p is the sum of the panel capacitance and the output capacitance of the individual current sources of the feedback DAC. The loop-gain of the TIA using a 1-pole transfer function for the opamp is expressed in equation 4.2.

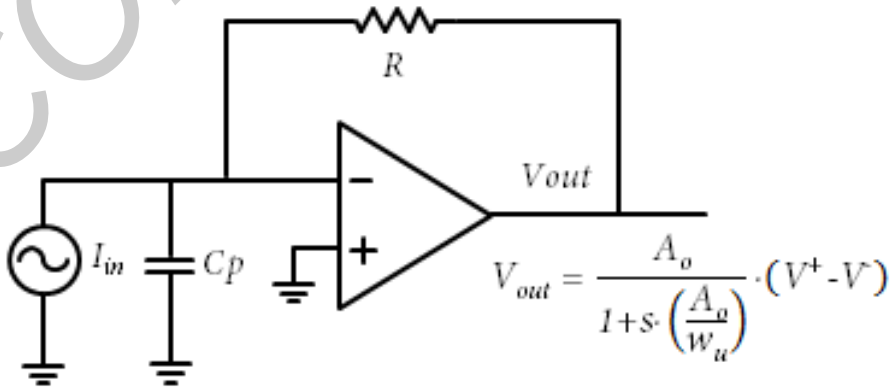


Figure 4.28: Schematic of the front-end TIA

$$Loopgain(s) = \frac{-A_o}{\left(R \cdot C_p \cdot \frac{A_o}{w_u}\right) s^2 + \left(R \cdot C_p + \frac{A_o}{w_u}\right) s + 1} \qquad (4.2)$$

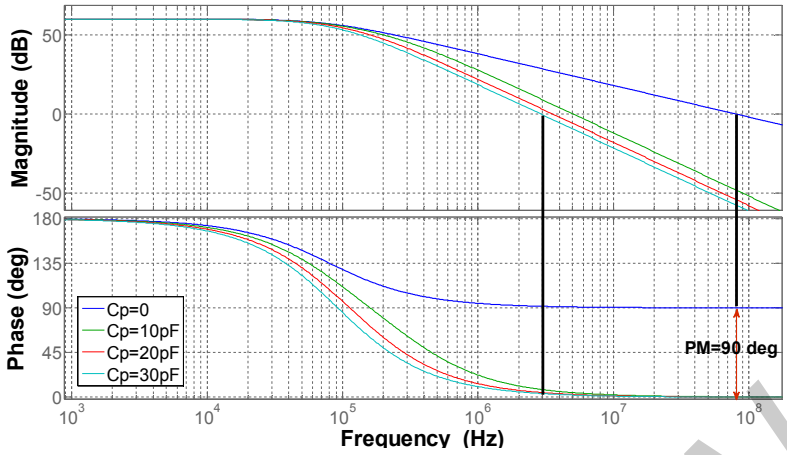


Figure 4.29: Bode plot of TIA's loop-gain Aβ

Figure 4.29 shows the Bode plot of the above mentioned transfer for different values of C_p. The open-loop DC gain (A_o) of the opamp is 60 dB and the unity gain frequency (w_u) is 80 MHz. With zero input capacitance and a single-pole opamp, the available phase margin for loop-gain is 90°. The addition of C_p introduces a 2nd pole in the transfer function and results in a reduction in the phase margin. The TIA would require frequency compensation to ensure stability. Figure 4.30 shows the decrease in SNR due to the absence of compensation for the additional panel capacitance.

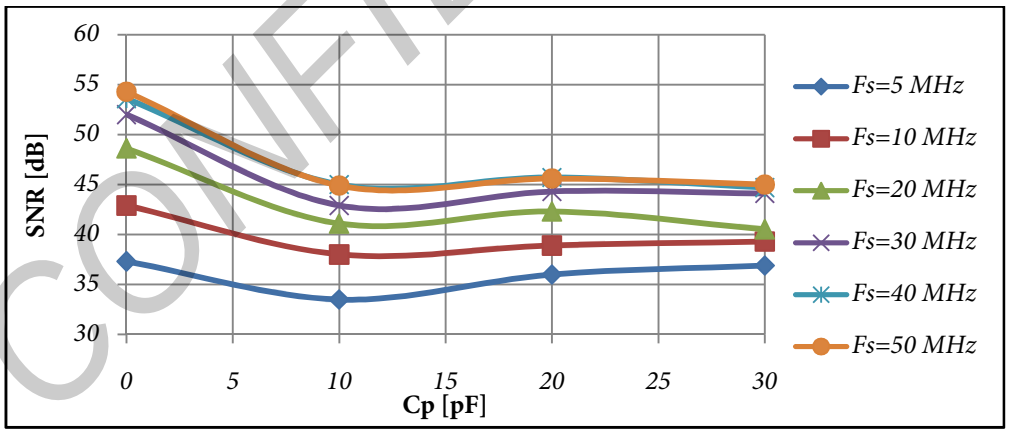


Figure 4.30: SNR versus panel capacitance without opamp compensation

4.3.3 Nonlinearity of Feedback DAC

The proposed readout IC uses a 7-bit IDAC to generate the feedback current to track and cancel the input panel current. The conventional implementation of an IDAC requires identical current sources that can be combined according to the input code to generate the required output current. The primary requirement of the DAC is to always have a DNL < 1 LSB to avoid missing codes. If this is not satisfied, the non-monotonic behaviour the DAC

could change the negative feedback of the control loop to positive feedback, corrupting the readout behaviour.

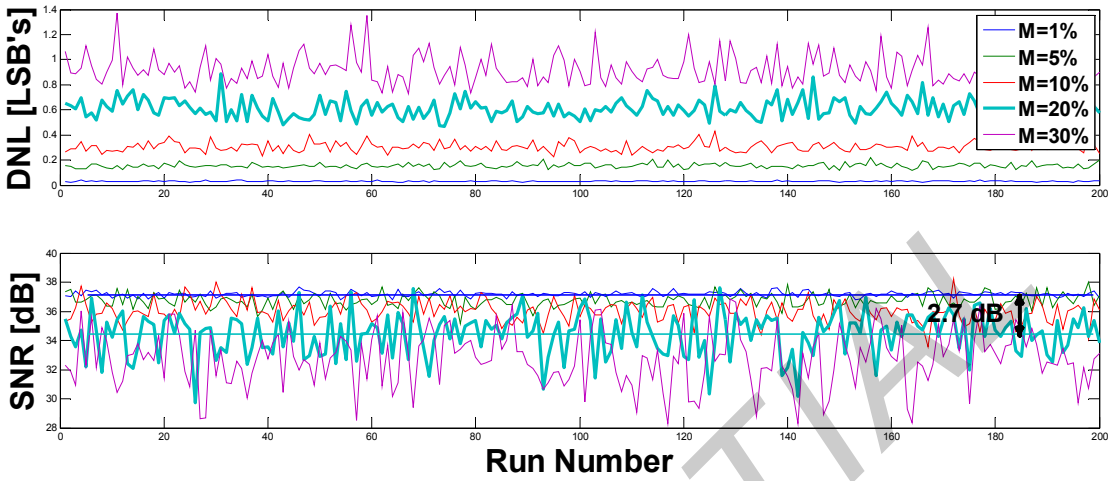


Figure 4.31: Monte Carlo simulation for mismatch in IDAC elements

Figure 4.31 shows the results of a Monte Carlo simulation of the mismatch in the IDAC elements and its influence on the SNR of the converter. A 20% mismatch in the IDAC elements result in an average DNL of 0.6 LSB and a 2.7 dB decrease in SNR. Consequently, Figure 4.32.a shows multiple tones at the signal harmonics in the spectrum of the ADC output due to this mismatch. Appropriate design techniques and good layout practises have to be adhered to reduce the DNL of the DAC.

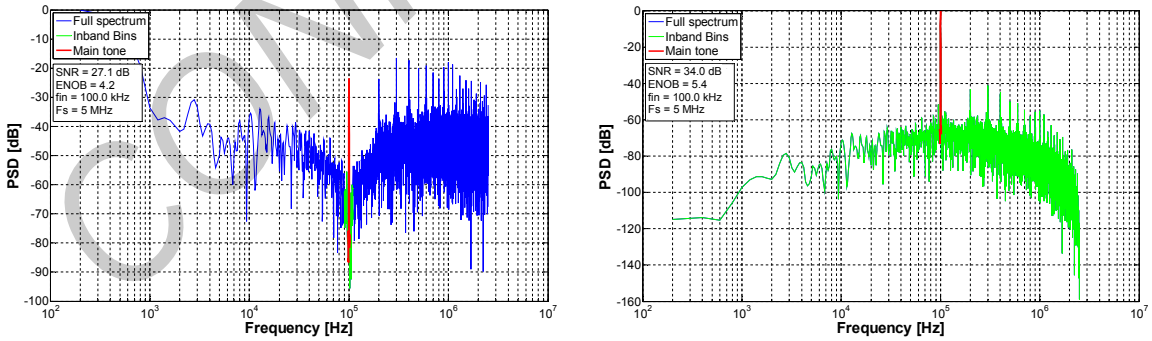


Figure 4.32: Frequency spectrum with 20% IDAC mismatch a) ADC output b) BPF output

4.3.4 Loop Delay Sensitivity

As the digital portion of the proposed converter is implemented off-chip, any delay in the control loop can have a negative impact on performance. Figure 4.33 shows the variation in SNR due to additional clock-cycle delays in the feedback loop. The effect is more pronounced at lower sampling frequencies. If the converter operates with a sampling

frequency greater than 30 MHz, 1-2 clock-cycle delays results in a SNR drop of less than 5 dB.

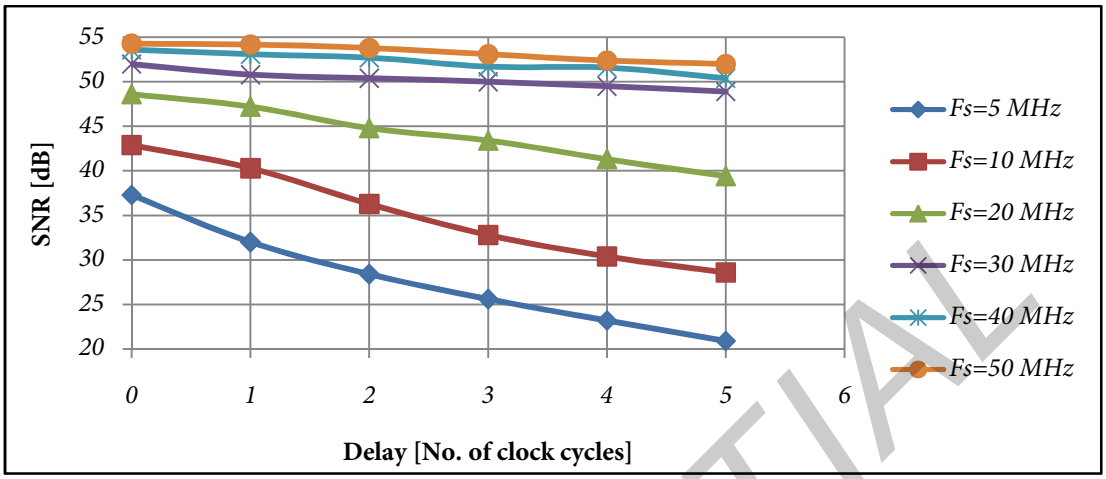


Figure 4.33: Variation in SNR due to external delay in digital logic

4.4 Summary

This chapter explained the architecture of the proposed touchscreen readout IC with system level simulations. The benefit of the bandpass channel response for suppressing panel noise has been illustrated. In addition, the effect of major circuit-level error sources was discussed. Chapter 5 presents the circuit level implementation details of the proposed readout architecture.

4.5 References

[4.1] *Muller, R.; Gambini, S.; Rabaey, J.M., "A 0.013 mm2, 5 uW, DC-Coupled Neural Signal Acquisition IC With 0.5 V Supply," in Solid-State Circuits, IEEE Journal of , vol.47, no.1, pp.232-243, Jan. 2012*

[4.2] *Analog Devices, Technical Article: MS-2698, Synchronous Detection to make Precision, Low Level Measurements*

[4.3] *Atmel Application Note: QTAN0079, Button, Sliders and Wheels, Sensor Design Guide*

Chapter 5

Circuit Design

Chapter 4 described the system-level architecture of the proposed touchscreen readout IC. This chapter explains the circuit details of the converter designed using a 0.15 μm CMOS process. Section 5.1 translates the system-level model into a circuit-level block diagram. Section 5.2 - 5.4 describes the design of a transimpedance amplifier, a current steering DAC and a comparator. Lastly, section 5.6 shows the layout details of the converter.

5.1 Circuit-Level Block Diagram

Figure 5.1 shows the circuit-level block diagram of the proposed readout IC. The negative feedback loop uses an IDAC to track and cancel the incoming panel current. The input current has an AC waveform as a result of the positive and negative voltage variations across the panel capacitance. Instead of using a separate PMOS and an NMOS DAC, the converter employs a single NMOS DAC and a PMOS current source to cancel the input current and reduce the area of the AFE. The DC value of the feedback current can be adjusted by adding a suitable offset to the digital input code of the DAC.

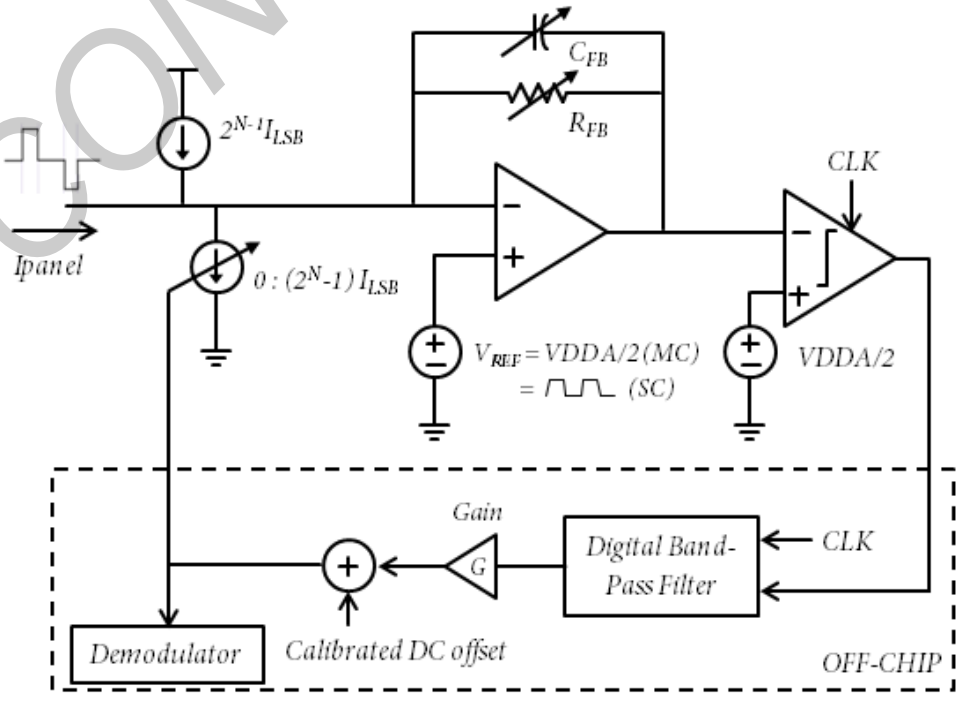


Figure 5.1: Circuit-level block diagram of proposed readout IC

The error signal in the current domain is converted to a voltage using a transimpedance amplifier (TIA). The amplifier requires frequency compensation due to the large panel capacitance. The reference voltage for the TIA is at half the supply voltage for the mutual-sensing mode and is changed to a square waveform for sensing the self-capacitance of the panel.

The TIA output is digitized with a 1-bit ADC using a clocked comparator. The digital section of the readout IC comprising of the bandpass filter and other calibration blocks are implemented on a FPGA off-chip.

5.2 Transimpedance Amplifier

The specifications of the TIA are listed in Table 5.1. The TIA is required to amplify and provide a low impedance node for the μA-level input panel current. To ensure an input impedance less than 100 Ω for frequencies up to 500 kHz (maximum TX frequency), the opamp requires an open-loop DC gain of 60 dB and a unity gain-bandwidth of at least 70 MHz.

Specifications	
Open-Loop DC Gain, A_o	*> 60 dB*
Unity Gain Bandwidth, ω_u	*> 70 MHz*
Power	*< 300 μA*
Output Referred Offset (3σ), V_{os}	*< 10 mV*
Input Referred RMS Noise Current, $i_{n,rms}$	*< 20 nA_{rms}*
Transimpedance Gain, Z_{TIA}	*25 kΩ – 100 kΩ*
Slew Rate	*> 10 V/μs*
Output Voltage Swing	*0.2 V – 2 V*
Input Common Mode Range	*VDD/2 ± 1 V*

Table 5.1: TIA Specifications

As the readout IC is required to operate with an analog power supply of 2.7 V – 5 V, the TIA uses high voltage thick-oxide transistors. The nominal threshold voltage of these MOSFETs is around 1 V and designing the TIA to meet the above specifications using a single-stage amplifier is not feasible. Hence, a two-stage opamp configuration [5.1] as shown in Figure 5.2 is used for designing the TIA.

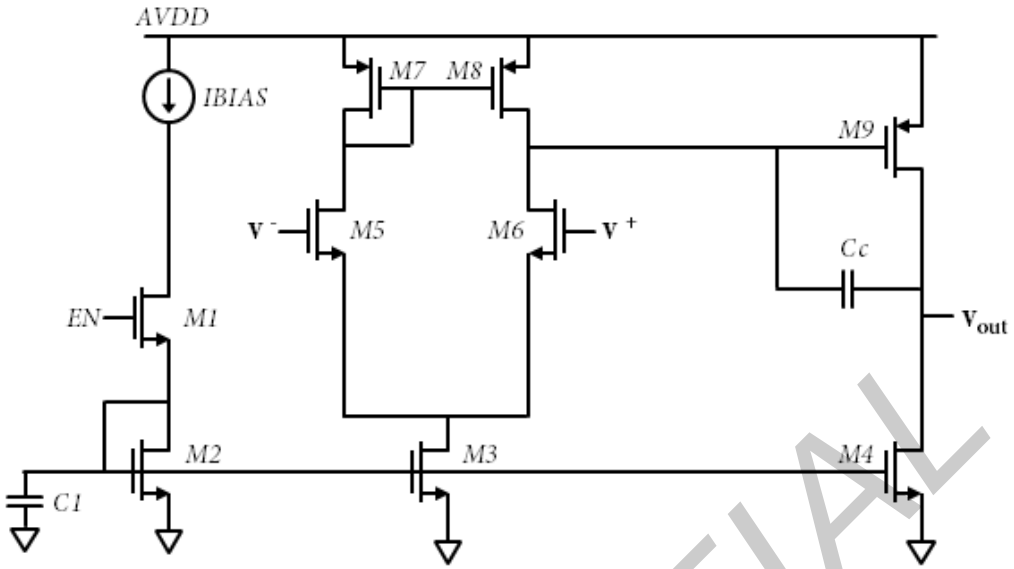


Figure 5.2: Schematic of a 2-stage amplifier

The first stage has a gain 50 dB ($-g_{m5}(r_{o6} \parallel r_{o8})$) while the second stage common source amplifier has a gain of 30 dB ($-g_{m9}(r_{o9} \parallel r_{o4})$). The opamp has a unity-gain-bandwidth (UGBW) of 90 MHz (g_{m5}/C_C) and a phase margin of 80° after Miller compensation.

5.2.1 AC Response

In order to ensure closed-loop stability due to the additional poles and zeros introduced by the panel capacitance and the output capacitance of the current sources, a capacitor (C_{FB}) is added across the feedback resistor to modify the β-network. This introduces a pole in the closed loop transfer (1/β) as given in equation 5.1, where C_{in} denotes the sum of the panel capacitance, output capacitance of current sources and the input capacitance of the opamp.

$$\frac{1}{\beta} = \frac{(R_{FB} \parallel 1/(C_{FB}s)) + 1/(C_{IN}s)}{1/(C_{IN}s)} = \frac{1 + R_{FB}(C_{FB} + C_{IN})s}{1 + R_{FB}C_{FB}s} = \frac{1 + j\frac{f}{f_z}}{1 + j\frac{f}{f_p}} \qquad (5.1)$$

The addition of C_{FB} decreases the 3-dB bandwidth of the TIA but at the same time improves the phase margin of the loop-gain (Aβ). Figure 5.3.a plots the above transfer function along with the open-loop gain of the opamp while Figure 5.3.b shows the phase plot for Aβ. The reduced phase margin due to the additional input capacitance is clearly visible. With a feedback capacitor of 0.8 pF, the phase margin improves by 30°.

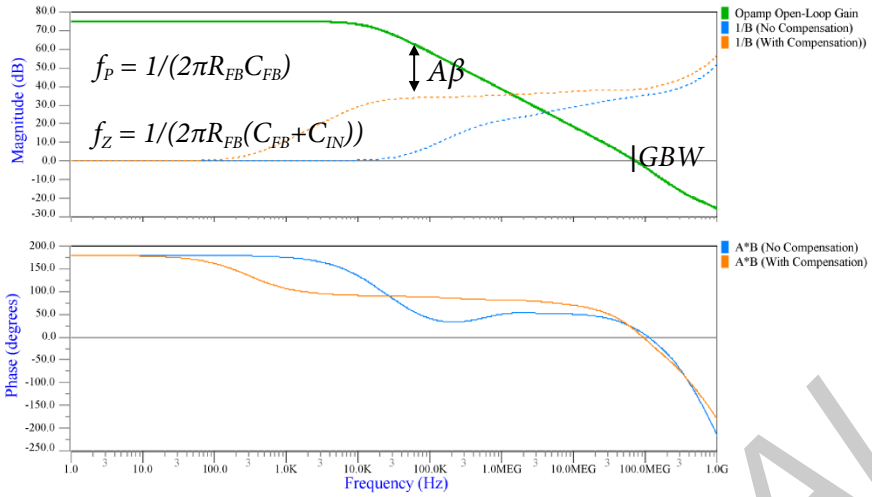


Figure 5.3: AC Response showing the effect of compensation in the feedback network

Figure 5.4 shows the circuit diagram used to measure the phase margin of the TIA's loop-gain while Figure 5.5 shows the loop-gain Bode plot with the RC extracted opamp at different process corners (VDD = 2.7 V, Temperature = 30 °C). The open loop DC gain of the opamp is 75 dB and the phase margin is 75°. Table 5.2 summarizes the same at different process corners.

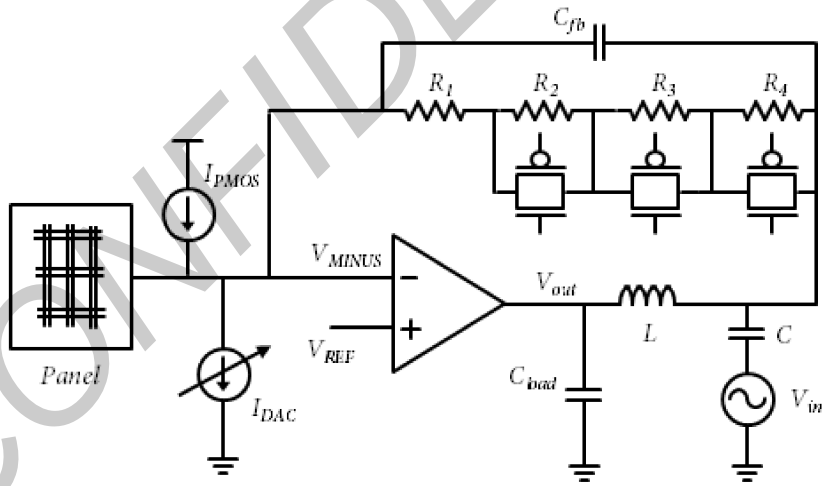


Figure 5.4: Circuit diagram to simulate the loop-gain of the opamp

corner	A_o [dB]	ω_u [MHz]	pmg	gmg
hrhc_sscell	74.90	72.02	74.70	35.38
hrlc_ttcell	75.17	69.00	75.04	38.13
lrhc_sfcell	74.00	67.95	75.10	35.30
lrlc_ffcell	75.22	60.60	74.10	37.79
trtc_fscell	74.76	66.67	72.62	36.48
trtc_ttcell	75.22	69.15	74.31	36.58
Min	74.00	60.60	72.62	35.30
Max	75.22	72.02	75.10	38.13

Table 5.2: Opamp parameters with extracted RC netlist at different process corners

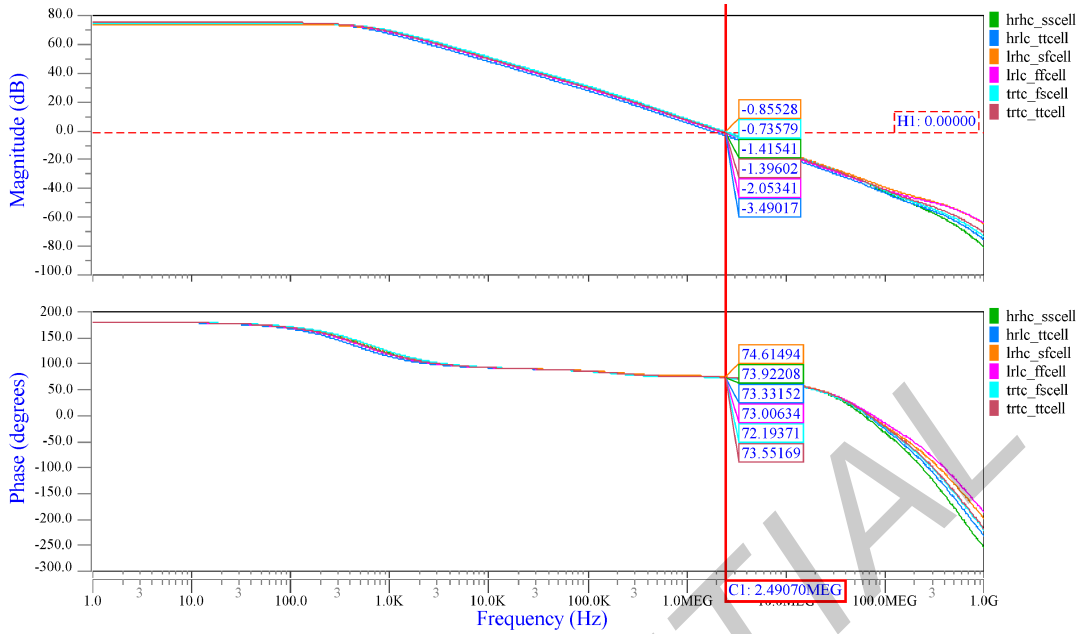
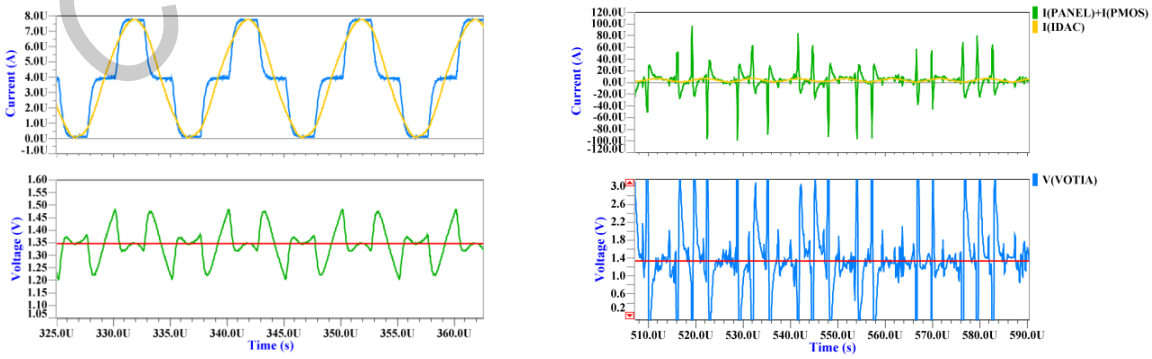


Figure 5.5: Loop-gain Bode plot at different process corners

5.2.2 Output Swing

As the amplitude of the input panel current is proportional to the TX frequency, a transimpedance gain of 50 kΩ would require an output voltage swing of up to 2 V. If the swing is too small, the TIA would saturate with panel noise and the virtual ground node may vary by ±300 mV. This will have an impact on the linearity of the DAC connected to the virtual ground node and would affect the readout circuit performance as highlighted in section 4.3.3. Figure 5.6 shows the output voltage of the TIA with and without panel noise. The large output voltage swing available from the second stage of the amplifier is beneficial in this regard.



a) *b)*

Figure 5.6: Transient waveforms of TIA a) without panel noise b) with panel noise

5.2.3 Offset

With an output referred (3σ) offset of less than 10 mV for the opamp, the IDAC (using an I_{LSB}=100nA) can be calibrated to reduce the offset to within ±5 mV. Higher levels of offset would require the IDAC to operate with a larger I_{LSB} unit current and thereby reduce the resolution of the converter. Systematic offset error is reduced using a symmetric layout and a LOD (length of diffusion) of 4 µm for each of n-type MOSFETs of the input differential pair. A current imbalance in the output stage of a two-stage opamp would also lead to a systematic offset voltage [5.1]. This occurs when the first stage output with a zero differential input voltage results in a bias current for M9 different from that of the bias current of M4. The current imbalance in the output stage can be reduced using the W/L ratio requirement mentioned in equation 5.2 [5.2].

$$\frac{(W/L)_9}{(W/L)_8} = 2 \cdot \frac{(W/L)_4}{(W/L)_3} \tag{5.2}$$

The threshold voltage mismatch and β-mismatch of the input differential pair and the current mirror load results in a random offset component [5.3]. Based on the quadratic MOSFET model, equation 5.3 defines $\sigma_{\Delta Vgs}$ of the input differential pair and equation 5.4 defines the fractional mismatch in the 1:1: current mirror load. The current mismatch is reflected to the input through the input transconductor and equation 5.5 defines the total offset voltage of the opamp due to random mismatch. The mismatch due to the differential pair can be reduced with a high g_m/I_D or low overdrive and the current mirror mismatch can be reduced with a low g_m/I_D or high overdrive.

$$\sigma^2_{\Delta V_{gs}} = \sigma^2_{\Delta V_T} + \left(\frac{\sigma_{\Delta\beta}}{\beta} \cdot \frac{I_D}{g_m}\right)^2 \; ; \; \sigma_{\Delta V_T} = \frac{A_{V_T}}{\sqrt{W \cdot L}} \; ; \; \frac{\sigma_{\Delta\beta}}{\beta} = \frac{A_\beta}{\sqrt{W \cdot L}} \tag{5.3}$$

$$\left(\frac{\sigma_{\Delta I_D}}{I_D}\right)^2 = \left(\sigma_{\Delta V_T} \cdot \frac{g_m}{I_D}\right)^2 + \left(\frac{\sigma_{\Delta\beta}}{\beta}\right)^2 \tag{5.4}$$

$$\sigma^2_{V_{OS}} = \sigma^2_{\Delta V_{gs}} + \left(\frac{\sigma_{\Delta I_D}}{I_D}\right)^2 \cdot \left(\frac{I_D}{g_m}\right)^2 \tag{5.5}$$

Table 5.3 shows the offset distribution of the TIA with a Monte-Carlo simulation at nominal PVT conditions. The 3σ random offset of the TIA is 2.9 mV and is well within the limits for a simple calibration using the IDAC.

```
Number of runs: 200
Nominal value:  1.3506 V
Standard Deviation:  0.9564 mV

[ 1.34750   1.34825 ] NB =   3  FREQ =    1.5% |
[ 1.34825   1.34900 ] NB =   7  FREQ =    3.5% |*
[ 1.34900   1.34975 ] NB =  25  FREQ =   12.5% |******
[ 1.34975   1.35050 ] NB =  51  FREQ =   25.5% |************
[ 1.35050   1.35125 ] NB =  69  FREQ =   34.5% |*****************
[ 1.35125   1.35200 ] NB =  27  FREQ =   13.5% |******
[ 1.35200   1.35275 ] NB =  17  FREQ =    8.5% |****
[ 1.35275   1.35350 ] NB =   1  FREQ =    0.5% |
```

Table 5.3: Distribution of V_{OS} with extracted opamp; (Ideal output voltage of TIA, VDD/2 = 1.35 V)

5.3 Current Steering DAC

This section describes the details of the current DAC connected in the feedback path of the readout circuit. The specifications of the IDAC are listed in Table 5.4. The main challenge was to design a monotonic and an area-efficient IDAC operating with a conversion rate of 48 MHz (maximum speed allowed for this product platform). DNL less than 1 LSB ensures that the IDAC is monotonic and prevents positive feedback inside the control loop. The IDAC can be realized using a current output DAC or a voltage-mode DAC followed by a G_m stage. A current-steering DAC was chosen over voltage-mode DAC's based on R-2R or capacitor array topologies as the implementation area was smaller.

Specifications	
Maximum Conversion Rate, F_s	*48 MHz*
Unit Current, I_{LSB}	*60 – 300 nA*
DNL	*< 1 LSB*
Output Impedance	*> 50 kΩ*
Input Referred RMS Noise Current, $i_{n,rms}$	*< 0.5 I_{LSB}*
Minimum Output Compliance Voltage	*1.35 V*

Table 5.4: IDAC Specifications

The current steering DAC architecture [5.4, 5.5] uses a set of current sources to steer a fraction of the full-scale reference current in the desired output branch. The DAC can be implemented with a binary or a thermometer based set of current references. The disadvantage of the latter scheme is the increased chip area required for implementing the digital decoder to generate a thermometer code for the DAC. On the other hand, thermometer-based DAC's are always monotonic and the mismatch between the current references has a smaller effect on DNL when compared to a fully-binary weighted DAC. The reduced matching requirements of a thermometer DAC require a smaller chip area for implementing the current references. As a result of the contrasting area requirements for the

digital and analog portions of the DAC based on the input code pattern, area efficiency of high resolution (> 10 bit) DAC's is achieved using a segmentation scheme [5.4]. The MSB's are thermometer coded while the LSB's are binary coded to achieve the best DNL performance with maximum area-efficiency.

As the converter requires a nA-range unit current DAC, the size of the tail current transistor is relatively large to have a high overdrive voltage. Hence, the difference in area considering mismatch alone is minimal for both the types of input schemes. As a result, a binary DAC without the additional thermometer decoder complexity was adopted for the converter.

Figure 5.7 shows the architecture of a conventional 7-bit fully-binary weighted IDAC. It is composed of 128 identical current elements. The N^{th} bit of the DAC contains 2^{N-1} ($1 < N < 7$) current sources and the current can be switched between the two output rails using a pair of switches. One of the output rails is connected to the panel input to track and cancel the incoming current while the other rail is connected to a low impedance node to sink the current from the unused current sources.

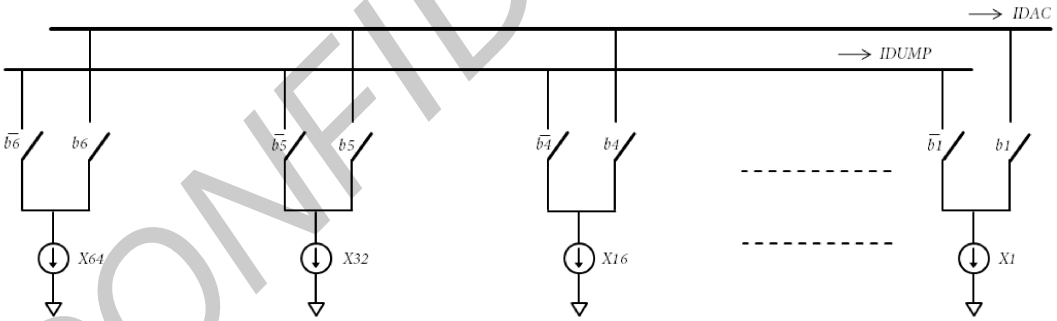


Figure 5.7: Binary-weighted IDAC Architecture

Figure 5.8 shows the schematic of a single unit current cell of the IDAC. It consists of a composite long tail current transistor, M_{1a} and M_{1b} (as process rules only allow the use of fixed-size transistors) with an overdrive voltage of 150 mV for an I_{LSB} of 100 nA. M_2 is the cascode transistor of the current source with a relatively smaller overdrive voltage. M_3 and M_4 define the steering direction of the tail current. The cascode transistor has two advantages in this structure. Firstly, it increases the output impedance of the current source. But the more important function of the cascode in this case is to shield the V_x node from the relatively large drain capacitance of the tail current transistor. The reduced parasitic capacitance at the source of M_3 - M_4 decreases the glitch in the output DAC current when it is steered from one output branch to another.

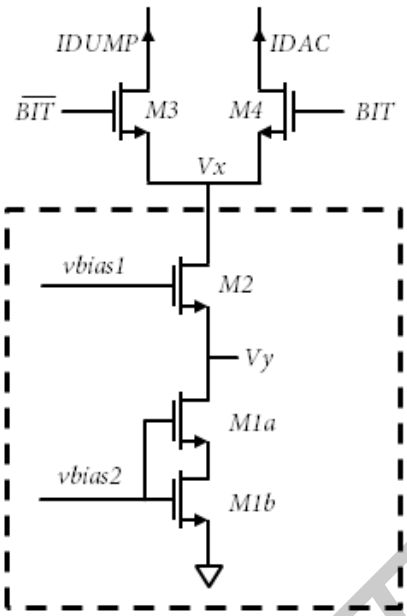


Figure 5.8: Schematic of a unit current cell of the IDAC

The transistor dimensions of M_1 and its overdrive voltage defines the static mismatch between the current sources and the resulting lower limit on DNL. Equations 5.6 - 5.8 indicate the effect of β-mismatch and V_T-mismatch on the variation in the output current of a unit current cell. V_T-mismatch is reduced by using a high overdrive while ensuring the output compliance voltage is within the specification and β-mismatch is reduced using a larger W and L while maintaining the same W/L ratio.

$$I_D = \frac{\beta}{2} V_{gt}^{\,2} \quad ; \quad \beta = \mu C_{ox}(W/L) \tag{5.6}$$

$$\frac{\Delta I_D}{I_D} = \frac{\partial I_D}{\partial \beta} \cdot \frac{\Delta \beta}{I_D} + \frac{\partial I_D}{\partial V_T} \cdot \frac{\Delta V_T}{I_D} \quad ; \quad \frac{\Delta I_D}{I_D} = \frac{\Delta \beta}{\beta} - \frac{2 \cdot \Delta V_T}{V_{gt}} \tag{5.7}$$

$$\frac{\sigma_{I_D}^{\,2}}{I_D^{\,2}} = \frac{\sigma_\beta^{\,2}}{\beta^2} + \frac{4 \cdot \sigma_{V_T}^{\,2}}{V_{gt}^{\,2}} \text{ where, } \sigma_\beta = \frac{A_\beta}{\sqrt{(W.L)}} \text{ and } \sigma_{V_T} = \frac{A_{VT}}{\sqrt{(W.L)}} \tag{5.8}$$

The above discussion considered the effect of static error sources on the DNL performance. However, DNL is also affected by dynamic error sources. The major error source in this regard is the glitch in the output current when it is steered from one branch to another due to the parasitic capacitance of the current source. This increases the DNL at higher conversion rates when the DAC currents are switching at a faster rate between the two output branches. The use of the cascode transistor helps in this regard as discussed before, but a further improvement can be achieved by modifying the IDAC as shown in Figure 5.9.

In this configuration, each of the first 3 MSB elements of the IDAC is sub-divided into smaller groups. For instance, the MSB that was composed of 64 unit current sources in the earlier configuration is made up of 8 groups with each group containing only 8 unit current sources in the modified structure. This arrangement significantly improves the DNL due to dynamic errors at higher conversion speeds at the cost of a small increase in area due to the addition of extra current steering switches.

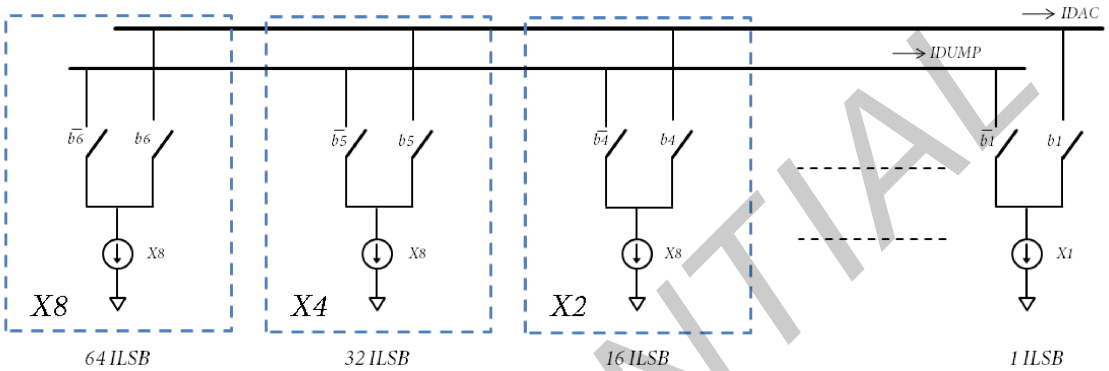


Figure 5.9: Schematic of IDAC with improved dynamic performance

Another source of dynamic error arises from a bad signal transition on the pair of switches controlling the direction of the tail current. If both the switches are OFF at the same time as shown in Figure 5.10.b, the tail current transistor is OFF for a brief period and results in a large glitch in the IDAC current at a later instant. Hence, the optimum switch drive is to ensure that both the control signals transition simultaneously near the mid-level. Figure 5.10.a shows a reduction in the IDAC glitch magnitude with a symmetric gate drive obtained using two flip-flops clocked at the same instant. Also, it is required to ensure that all the IDAC bits are synchronized and clocked into the IDAC simultaneously on-chip to reduce the DNL error due to dynamic errors.

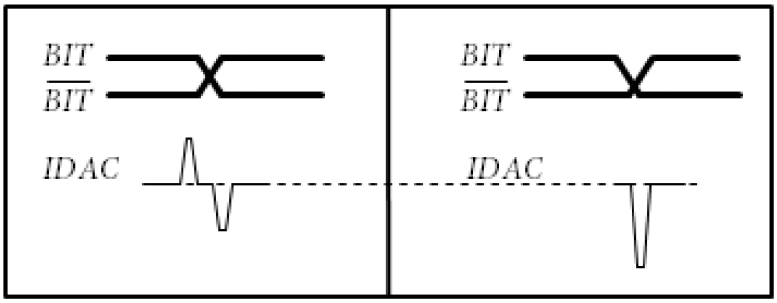


Figure 5.10: a) Symmetric and b) Un-symmetric glitch in IDAC current due to switch drive signals

Table 5.5 shows the DNL distribution at the mid-code transition of the IDAC with a pre-layout Monte Carlo simulation. The worst-case DNL is at the mid-code transition as all

the LSB current sources are turned OFF and the current sources of the MSB element are turned ON. A (3σ) DNL less than 1 LSB ensures that the IDAC is monotonic.

Number of runs : 200
Average value of I_{LSB} : 191.46 nA $\{I(DAC)_{64} - I(DAC)_{63}\}$
Standard Deviation of I_{LSB} : 41.701 nA **(3σ DNL = 0.653 I_{LSB})**

[75.00000N	100.00000N]	NB =	4	FREQ =	2% |*
[100.00000N	125.00000N]	NB =	8	FREQ =	4% |**
[125.00000N	150.00000N]	NB =	22	FREQ =	11% |*****
[150.00000N	175.00000N]	NB =	38	FREQ =	19% |*********
[175.00000N	200.00000N]	NB =	39	FREQ =	19.5% |*********
[200.00000N	225.00000N]	NB =	46	FREQ =	23% |**********
[225.00000N	250.00000N]	NB =	31	FREQ =	15.5% |*******
[250.00000N	275.00000N]	NB =	8	FREQ =	4% |**
[275.00000N	300.00000N]	NB =	4	FREQ =	2% |*

Table 5.5: DNL distribution of IDAC at mid-code

Lastly, Figure 5.11 shows the schematic of the PMOS current source used to apply a DC shift to the input panel current. It is derived from 64 unit current elements of the IDAC, which results in an accurate and close tracking of the PMOS current with the NMOS DAC current. This will ensure that the range of the IDAC used to calibrate the total offset of the converter is kept at a minimum and the IDAC will a larger set of levels to detect a change in the panel current due to a touch stimulus.

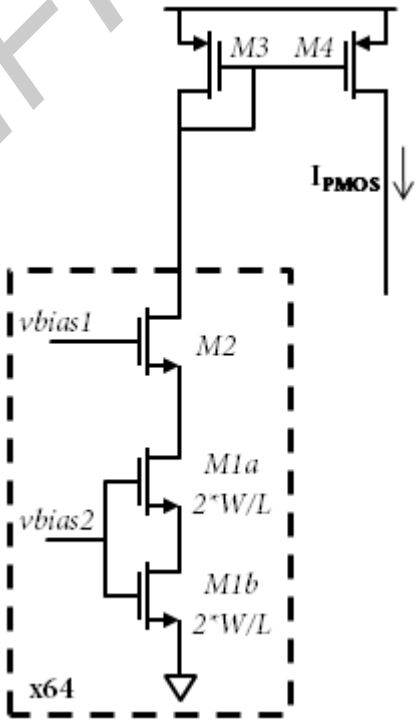


Figure 5.11: Schematic of the input PMOS current source

5.4 Comparator

The comparator is used to make a digital decision of the sign of the error signal in the servo loop. It operates with the same sampling frequency as the IDAC. The effect of the comparator's offset on the converter performance is similar to that of the TIA. As a result, a single calibration of the IDAC can reduce the overall offset of the converter as discussed earlier. The required specifications of the comparator are listed in Table 5.6.

It is also important to reduce any kickback charge from the comparator, as this charge can transfer to the low-impedance input via the feedback network. This will introduce unwanted spikes on the virtual ground node of the opamp and affect the linearity of the current sources connected to this node. Lastly, the comparator should have a small decision time to allow for processing of the bitstream with minimum delay in the off-chip digital logic.

Specifications	
Maximum Sampling Rate	*48 MHz*
Input Referred Offset (3σ), V_{os}	*<10 mV*
Decision time	*< 0.5*clock period*
Minimum Kickback Charge	

Table 5.6: Comparator Specifications

Due to time constraints for completing the full-chip layout before the tapeout deadline, a comparator from a previous project was integrated into this converter. Figure 5.12 shows the circuit diagram of the comparator. It is a 2-stage pre-amplifier based comparator with a wide common mode input voltage range. The kickback effect is reduced due to the separation of the positive feedback regeneration circuit from the input differential pair.

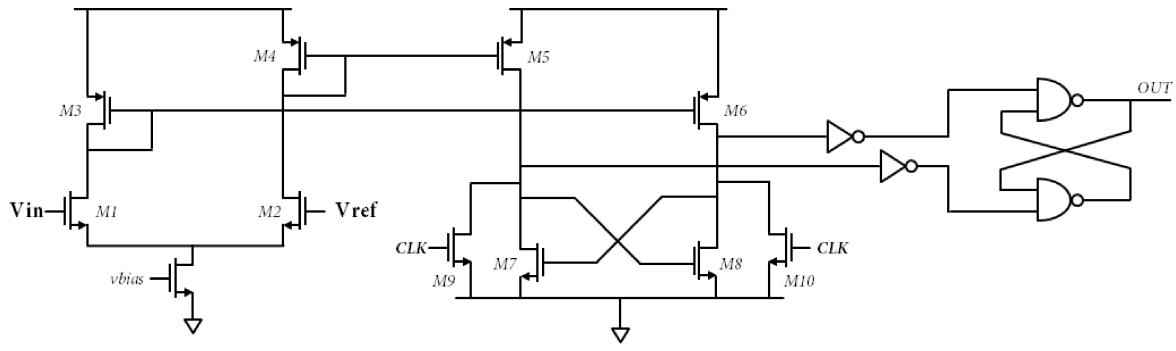


Figure 5.12: Schematic of 2-stage comparator

As the clocked comparator is reset every cycle, it does not suffer from any memory effects. Finally, the cross-coupled NAND gates at the output make sure the comparator retains its previous state if the positive feedback circuit is unable to resolve the input to full logic levels within the current clock cycle.

5.5 Bias Circuitry

The bias current for the readout circuit is obtained using a self-biased μA-current generator [5.6]. Figure 5.13 shows the schematic of the biasing circuit. The main bias current is generated using the current mirror pairs of M_3-M_4 and M_{16}-M_{17}. With all the transistors operating in strong inversion, the bias current is determined by the difference in V_{GS} of M_{16} and M_{17} and the resistor array of R_1-R_5.

It is necessary to use a start-up circuit to ensure that the current mirrors are driven to the correct operating point when the circuit is powered-on. The start-up circuit consists of transistors M_1, M_2 and capacitor C_1. At the instant the power supply turns on, the voltage across C_1 is zero and the gate-source voltage of M_2 is equal to the supply voltage. This injects a current into the bias circuit through M_{16}. Simultaneously, the drain current of M_1 will charge the capacitor towards VDD. As a result, M_2 and M_1 will turn off as the capacitor voltage reaches VDD and the constant current flowing through M_4 can be mirrored to the required analog blocks.

Transistors M_5-M_7 is used to mirror the bias current and generate a nA-range I_{LSB} current for the IDAC. An alternate option to override the internal bias current generator with an external bias current source is also provided.

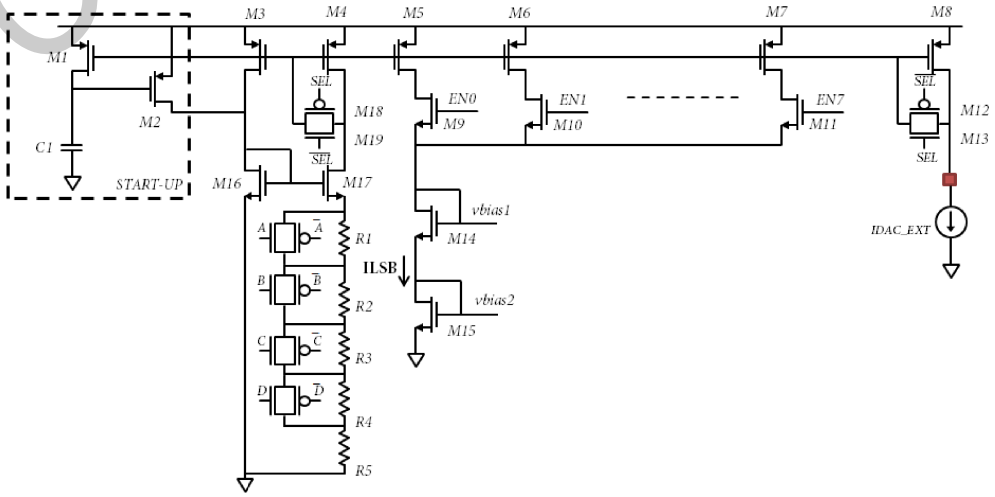


Figure 5.13: Schematic of self-biased current generator

5.6 Layout Details

Figure 5.14 shows the layout of the proposed readout channel. The area of the channel is 40 kμm² and is dominated by the opamp and the large tail current transistors of the input current sources. The unit current sources of the first 3 MSB's of the IDAC are evenly distributed to reduce the effect of gradient process variations on DNL. Each of the analog blocks is placed in a separate deep-nwell to provide better isolation from substrate noise.

Figure 5.15 shows the layout of the full-chip. The die occupies an area of 4 mm². It includes 2 channels, bias circuitry, special ESD cells for panel inputs and decoupling capacitors for the analog references and power supplies.

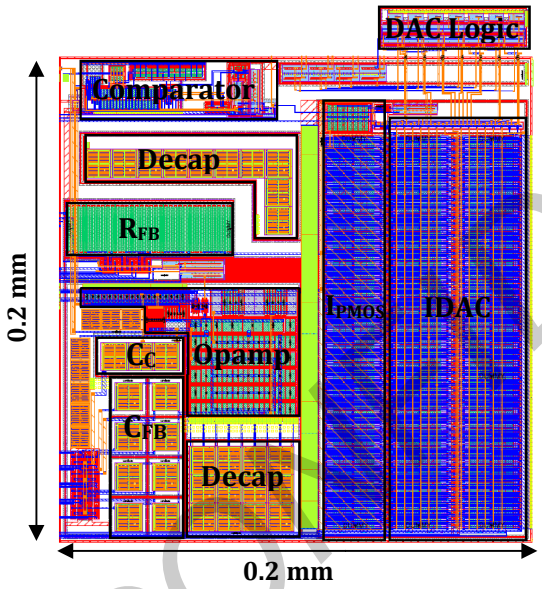


Figure 5.14: Layout of proposed channel

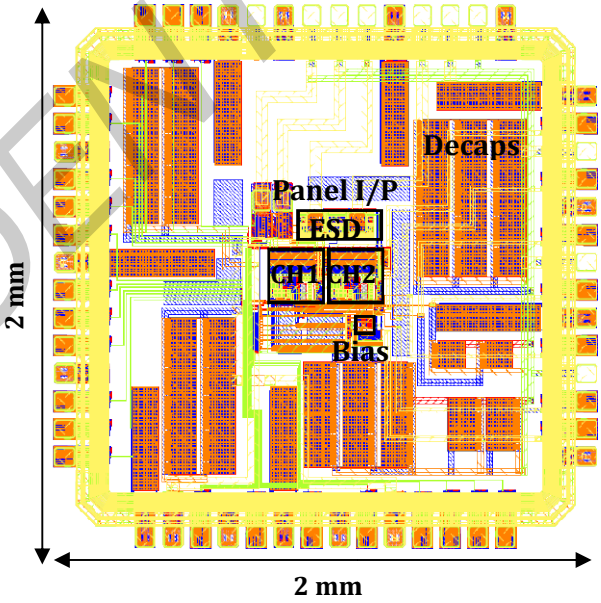


Figure 5.15: Full-chip layout

5.7 Summary

This chapter discussed the circuit implementation of the analog blocks of the converter. The transimpedance amplifier and the results of its frequency compensation were discussed in brief. This was followed by the design details and simulation results of a 7-bit current-steering DAC optimized for high speed and small area. The next section discussed the details of the comparator and the bias circuitry. Lastly, layout of the area-efficient channel and the full-chip were shown.

Chapter 6 presents the measurement results of the test-chip.

5.8 References

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Chapter 6

Measurement Results

This chapter describes the measurement details of the fabricated touchscreen readout IC. Section 6.1 explains the measurement setup used for characterizing the test-chip. Section 6.2 shows the AC response and summarizes the measurement results of the readout IC obtained with a capacitive touch panel. Section 6.3 shows the chip micrograph and section 6.4 presents a performance comparison of the designed converter with the state-of-the-art.

6.1 Measurement Setup

Figure 6.1 shows a block diagram of the measurement setup used to characterize the test-chip. The chip requires 3 separate power supplies: analog VDD, digital VDD and IO VDD. A function generator drives the excitation voltage waveforms on the TX electrodes of the panel while an arbitrary waveform generator is used to create and replay the panel noise patterns. The voltage references for the converter, V_{REF1} and V_{REF2} are selected based on the sensing mode (mutual/self).

The input code for the 7-bit DAC is generated in real-time using an FPGA. The bitstream from the comparator output of the test-chip drives the bandpass filter inside the FPGA to generate the DAC code. The DAC bits are synchronized on-chip to reduce DNL due to the dynamic errors of the IDAC resulting from different PCB route delays.

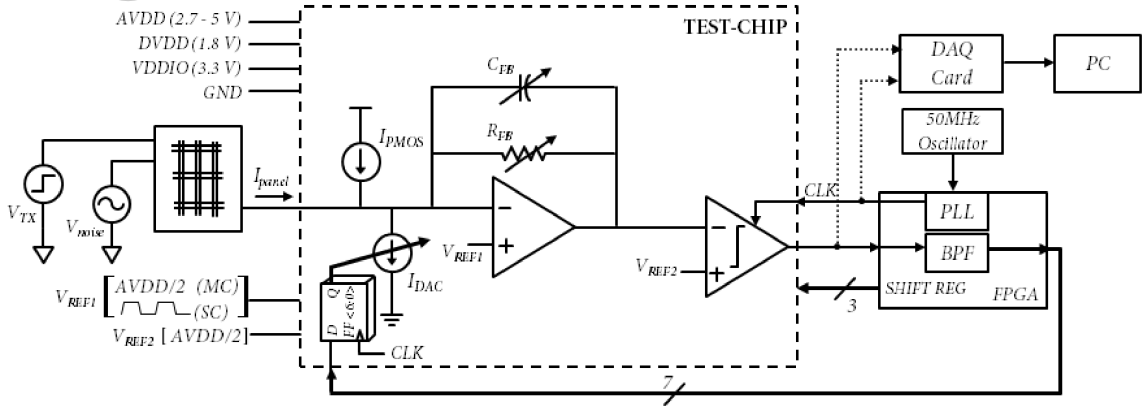

Figure 6.1: Block-diagram of measurement setup

The touch information in the digital domain can be deduced from the output bitstream of the comparator or from the FPGA output of the bandpass filter. The bitstream is captured using a 50 MHz data-acquisition (DAQ) card and further processed in MATLAB.

All the clocks for the converter are obtained from an on-chip PLL of the FPGA while the reference clock for the PLL is derived from a 50 MHz crystal oscillator. Figure 6.2 shows the timing diagram of the critical I/O paths of the converter. The input and output stages of the FPGA should be synthesized with realistic timing constraints to ensure that there are no setup or hold violations due to insufficient timing margins. As a failsafe option, the second channel of the converter has a separate clock pin to trigger the IDAC after all the data bits sent from the FPGA are valid.

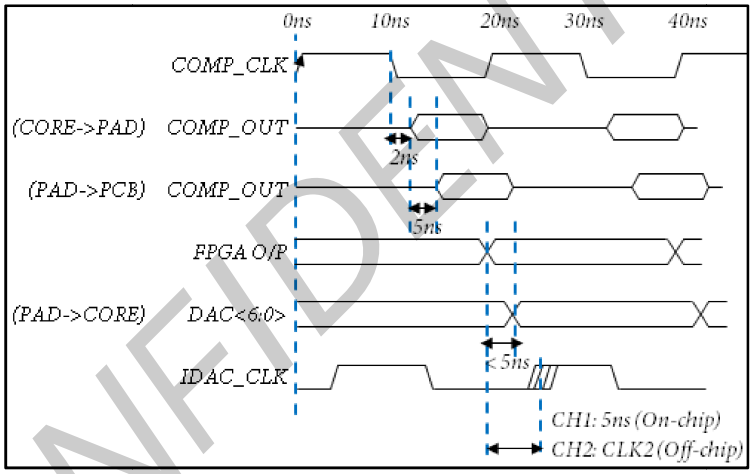

Figure 6.2: Timing-diagram of critical I/O paths (Fs = 50 MHz)

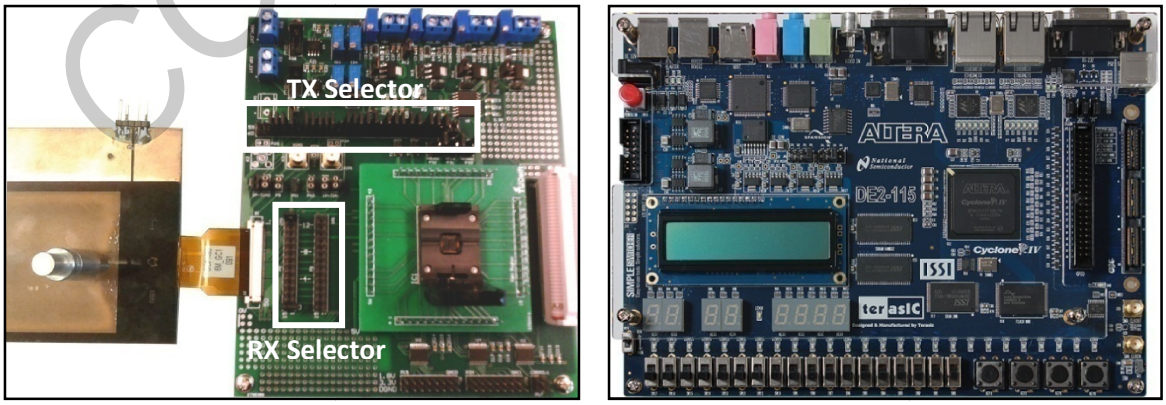

Figure 6.3: a) PCB for test-chip with panel interface b) Evaluation FPGA board

Figure 6.3 shows the PCB details of the readout IC. A capacitive touch panel is directly interfaced to the main PCB while the test-chip connects to the PCB via a daughter card. Using a jumper selection the appropriate TX and RX lines of the panel can be

connected to the readout IC. LCD noise is added to the copper plate attached to the panel while charger noise requires a high-voltage function generator to couple the noise to the panel through a metal object. Offset calibration and the digital bandpass filter is implemented using an ALTERA FPGA evaluation board.

6.2 Measurement Results

Figure 6.4 shows the setup for evaluating the readout IC response for a single-tone input. The opamp is configured as an inverting amplifier (gain: $-R_{FB}/R_{IN}$) and the DC offset of the IDAC is calibrated to trim the overall offset of the converter. The input to the converter is a sinusoidal voltage with an offset of V_{REF}.

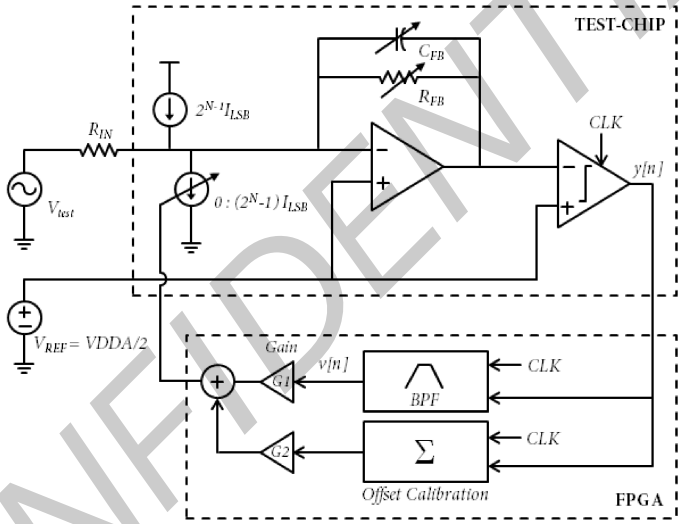

Figure 6.4: Measurement setup for single-tone test

Figure 6.5.a shows the spectrum at the ADC output while Figure 6.5.b shows the spectrum at the bandpass filter output. The ADC output has a bandpass response with a 20 dB/decade noise shaping but with a higher PSD for the distortion components at the input harmonic frequencies when compared with the simulation results of Chapter 4.

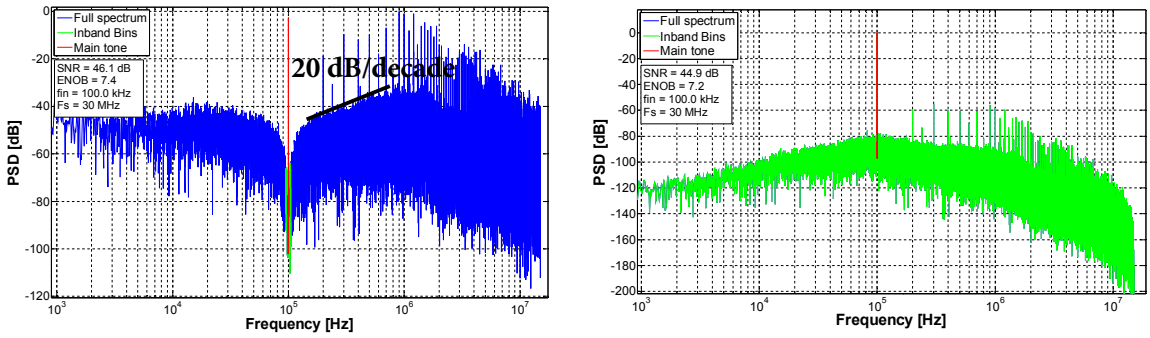

Figure 6.5: Measured frequency spectrum at a) ADC output, y[n] b) BPF output, v[n]

To investigate the increased distortion in the ADC output, Figure 6.6 shows the resulting spectrum after disconnecting the input. When compared to the simulation result of Figure 6.7.a, the measured spectrum shows a peaking of the higher order harmonics at 1 MHz. This is approximately at a decade lower compared to the peaking observed at Fs/2 (15 MHz) in the simulation.

A possible explanation for the above behaviour may be due to the fact that an extra delay element at the input stage of the digital filter was not modelled in the AC output response described in Chapter 4. Figure 6.7.b shows the simulated spectrum with an additional 1-clock cycle delay at the input of the digital filter. This input delay is necessary to model the synchronization of the comparator output inside the FPGA. The frequency shift observed in Figure 6.7.b due to the additional delay in the loop confirms this proposition and limits the measured ENOB of the converter to 7.5 (at OSR = 300) as against an ENOB of 9 in the simulation without the extra delay element in the feedback path.

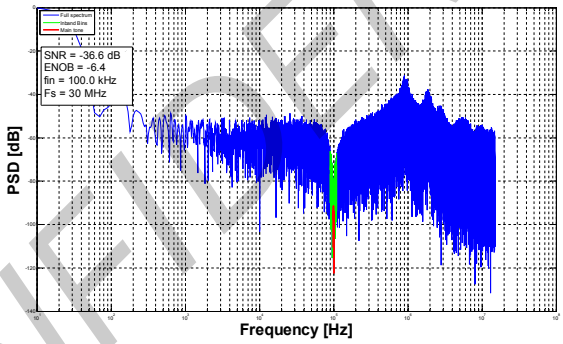

Figure 6.6: Measured ADC output spectrum with zero-input

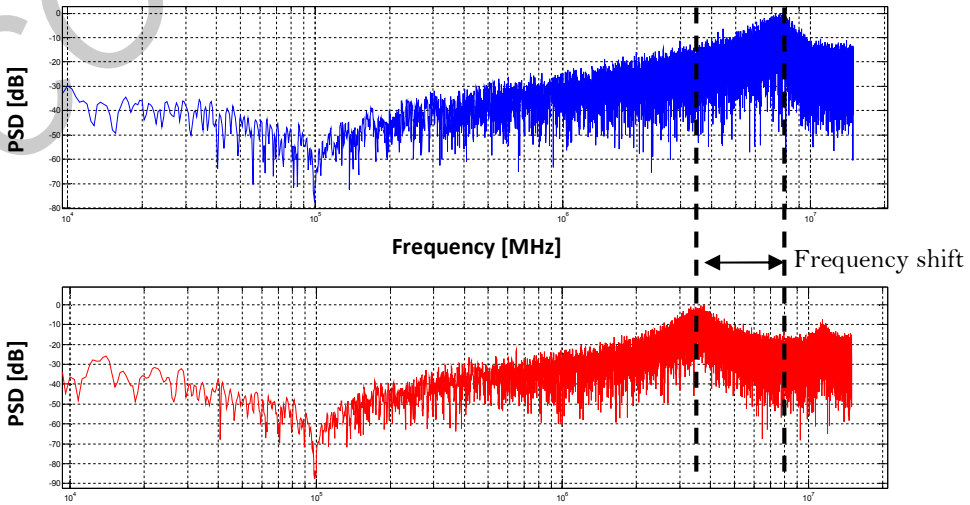

Figure 6.7: Simulated ADC output spectrum with zero-input and: a) No additional delay in feedback b) 1-clock cycle input delay to model FPGA constraints

Figure 6.9 compares the measured SNR of the fabricated readout IC for a 4.3″ capacitive touchscreen panel with a reference converter shown in Figure 6.8. The reference converter is based on the open-loop readout architecture discussed in section 3.4.1 with the addition of an attenuator at the input. The attenuator prevents panel noise from saturating the readout front-end but at the same time reduces the dynamic range of the panel current that can be sensed. The output of the attenuator is lowpass filtered using an ideal integrator and digitized using a first-order discrete-time Σ-Δ ADC with an ENOB of 7.

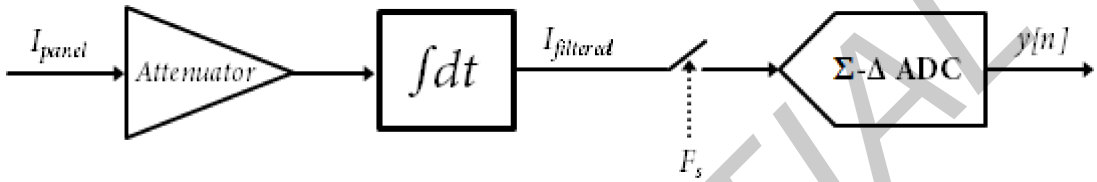

Figure 6.8: Block diagram of reference converter

The measurement bandwidth for the SNR plots of Figure 6.9 is 200 Hz. The plot compares SNR with and without panel noise for the fabricated readout IC (in bold lines) and the modelled reference converter (in dashed lines). The difference in SNR with LCD noise is small compared to the significant improvement in SNR with charger noise (in blue). This is a result of the increased panel noise rejection achieved with the bandpass channel response of the converter compared to the lowpass filtering action of the integrator of the reference converter. The proposed readout IC requires a minimum sampling frequency of 10 MHz (OSR=50) to achieve an ENOB of 7 in the absence of panel noise.

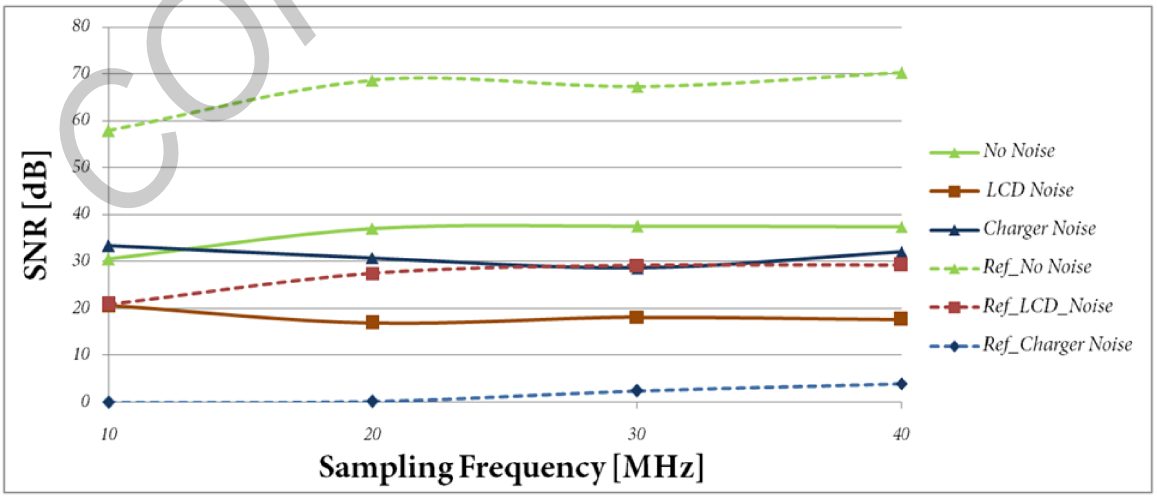

Figure 6.9: SNR comparison of test-chip measurements with reference converter

6.3 Chip Micrograph

Figure 6.10 shows the chip micrograph of the fabricated touchscreen readout IC. The test-chip is realized in a 0.15 µm CMOS process and uses a 56-pin QFN glob-top package. The digital I/O's are on the left and bottom sides of the die, while the analog references are on the right-side. The input pads connecting to the RX channels of the touchscreen are placed on the top-side of the die.

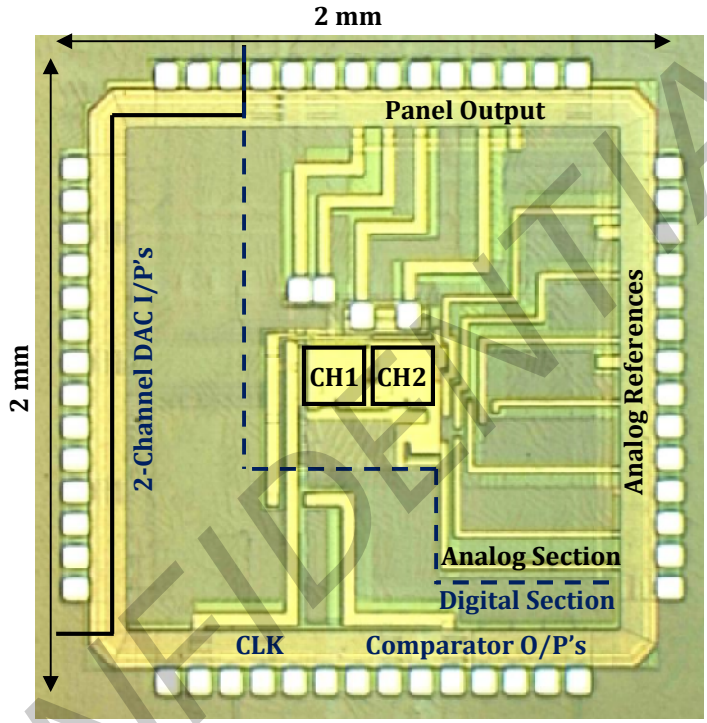

Figure 6.10: Chip micrograph

6.4 Summary

Table 6.1 shows a performance summary of the proposed converter and a comparison with the state-of-the-art. The designed converter achieves the best area-efficiency with an SNR of 18 dB with panel noise at a scan rate of 200 Hz for a 4.3″ touchscreen panel with a channel pitch of 4.1 mm.

		ISSCC 13' [6.1]	ISSCC 14' [6.2]	JSSC 14' [6.3]	This Work
Panel size [inch]		10.1″	4.5″	4.3″	4.3″
TSP Type		Mutual	Self/Mutual	Mutual	Self/Mutual
# of channels (TX/RX)		27/43	80/80	12/8	23/13
Sensor channel pitch		5 mm	1 mm	-	4.1 mm
Scan rate		120 Hz	322 Hz	200 Hz	200 Hz
SNR	Without panel noise	39 dB	41 dB	60 dB	38 dB
	With panel noise	-	-	-	**18 dB**
Technology		0.35 µm	0.35 µm	0.18 µm	0.15 µm
Supply voltage		3.3 V	2.6-3.6 V	2.1-3.3 V	2.7-5 V
Area/channel		896 kµm²	214 kµm²	225 kµm²	**40 kµm²** †

Table 6.1: Performance summary and comparison

6.5 References

[6.1] J.-H. Yang, S.-H. Park, J.-M. Choi, H.-S. Kim, C.-B. Park, S.-T. Ryu, and G.-H. Cho, "A highly noise-immune touch controller using Filtered-Delta-Integration and a charge-interpolation technique for 10.1-inch capacitive touch-screen panels," in IEEE ISSCC Dig. Tech. Papers, Feb. 2013

[6.2] N. Miura, S. Dosho, S. Takaya, D. Fujimoto, T. Kiriyama, H. Tezuka, T. Miki, H. Yanagawa, and M. Nagata, "A 1 mm-pitch 80 80-channel 322 Hz-frame-rate touch sensor with two-step dual-mode capacitance scan," inIEEE ISSCC Dig. Tech. Papers, Feb. 2014, pp. 216–217.

[6.3] Jun-Eun Park; Dong-Hyuk Lim; Deog-Kyoon Jeong, "A Reconfigurable 40-to-67 dB SNR, 50-to-6400 Hz Frame-Rate, Column-Parallel Readout IC for Capacitive Touch-Screen Panels," in Solid-State Circuits, IEEE Journal of , vol.49, no.10, pp.2305-2318, Oct. 2014

† The area does not include the digital BPF in the feedback path

Chapter 7

Conclusions

7.1 Recap of Thesis Objectives

As capacitive sensing provides flexible and reliable touch user interfaces for a varied set of applications, it has gained popularity over other touch sensing techniques. As a consequence, capacitive touchscreens are interfaced with many different sizes of display panels. With increasing size of display panels, the required number of channels that a readout IC has to support increases proportionally. As existing area-intensive touchscreen controllers are upgraded to support increased channel counts, the additional silicon area requirement increases the product cost. In addition, the touchscreen performance is highly affected by LCD noise and external noise from battery chargers. Better readout techniques to filter panel noise without sacrificing the dynamic range of the converter is an important requirement.

Hence, the objective of this thesis was to define and implement an area-efficient readout architecture that can digitize the touchscreen signal with sufficient accuracy and filter out the unwanted panel noise.

7.2 Conclusions

This thesis discussed the design and implementation of a new touchscreen readout architecture. The proposed mixed-signal architecture is a compact solution whose AFE has been implemented with a per channel area of 40 kμm^2. This represents a significant reduction in the RX channel area requirements for a multi-channel touchscreen readout IC. Integration of both the digital and analog blocks of the converter would lead to 2-3x improvement in area-efficiency when compared with the state-of-the-art.

In addition, the architecture is designed to have a bandpass channel response to filter the strong panel noise sources more effectively. Consequently, the reduced dynamic range of conventional readout techniques that employ input attenuators to suppress panel noise is no longer necessary with the architecture described in this thesis. An SNR of 20-35 dB (in a measurement bandwidth of 200 Hz) was obtained with the worst case panel noise

profiles for a 4.3″ capacitive touchscreen panel with a channel pitch of 4.1 mm. As system-level solutions can be developed to provide gesture recognition and multi-touch detection with the above SNR, the proposed converter can be integrated in touchscreen controllers to operate effectively in harsh panel noise environments.

7.3 Future Work

There are many readout techniques reported in literature for optimizing the different parameters affecting touchscreen performance. While decreasing channel area and improving panel noise rejection were the main goals of this thesis, below is a list of possible enhancements that can be investigated for future readout circuits:

1. *Spread-spectrum techniques employed in touchscreen readout circuits to boost SNR can be combined with the proposed converter to further improve the dynamic range.*
2. *Implementing a differential sensing front-end for the proposed converter to improve the common-mode rejection of display noise for 2 closely spaced RX channels.*
3. *Implementing higher-order modulators to achieve better noise shaping and ENOB.*
4. *A 2-step converter using the proposed converter to reject panel noise and digitizing a replica of the remaining signal charge with a high resolution bandpass Σ-Δ ADC.*
5. *Feasibility study of whether the proposed architecture can be adapted to digitize and filter the extremely small signal levels of a fingerprint sensor.*

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Appendix A

A.1 SNR Calculation

In the context of capacitive touch sensors, figure A shows the definition of the signal levels used in the SNR calculation of A.1 - A.3 [1]. The measurement bandwidth for touchscreen readout circuits ranges from 100 Hz - 1 kHz depending upon the number of channels to be digitized and the scan rate requirements.

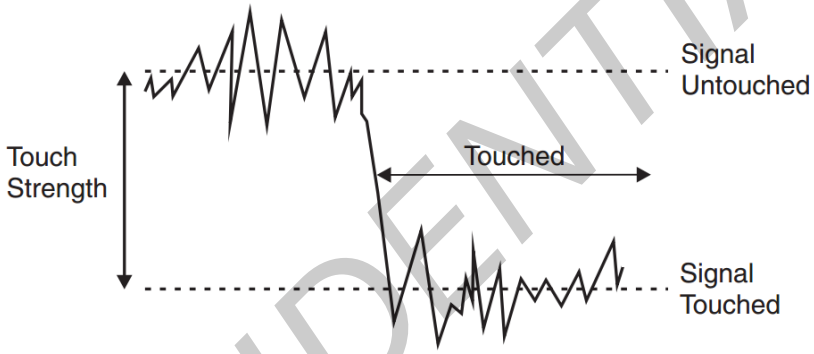

Figure A: Touch signal levels for SNR calculation [1]

$$SNR\ [dB] = 20\log_{10}(TouchStrength/NoiseTouched_{RMS}) \quad (A.1)$$

$$TouchStrength = SignalTouched_{AVG} - SignalUntouched_{AVG} \quad (A.2)$$

$$NoiseTouched_{RMS} = \sqrt{\frac{\sum\ (Signal[n] - SignalTouched_{AVG})^2}{TimeTouched}} \quad (A.3)$$

A.2 References

[1] Atmel Application Note: QTAN0079, Button, Sliders and Wheels, Sensor Design Guide