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DOI
10.1109/JSSC.2024.3393478

Publication date
2024

Document Version
Final published version

Published in
IEEE Journal of Solid-State Circuits

Canceling Fundamental Fractional Spurs Due to Self-Interference in a Digital Phase-Locked Loop

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***Abstract*— Parasitic coupling between the building blocks within a fractional-*N* phase-locked loop (PLL) can result in noticeable spurs in its output spectrum, thus affecting the PLL's usability in ultralow jitter applications. In this article, we focus on a chief contributor—"self-interference" caused by coupling from the PLL's frequency-reference (FREF) clock buffer to the RF oscillator, while exploiting the fact that the resulting phase-disturbance pattern: 1) exhibits a sinusoidal shape and 2) is synchronized with the PLL's output clock phase. Accordingly, we propose a digitally intensive pattern-aware approach to suppress the fundamental fractional spur raised by this self-interference mechanism. The proposed technique is applied to a fabricated digital PLL chip and reduces the worst spur level by 13 dB, thus proving its effectiveness.**

***Index Terms*— Coupling, fractional spurs, phase-locked loop (PLL), self-interference, spur cancellation (SC).**

I. Introduction

FRACTIONAL spurs in a phase-locked loop's (PLL) output spectrum are largely attributed to a periodic error pattern arising from its phase detector's (PD) transfer-function nonlinearity that cannot be attenuated by the subsequent loop filter [1], [2], [3], [4], [5]. To tackle such spurs, many strategies have been developed, e.g., adaptively eliminating the periodic disturbance pattern by predistorting the phase detection nonlinearity [6], [7], randomizing the periodic disturbance pattern [8], [9], [10], [11], or improving the phase detection linearity [1], [12], [13], [14], [15]. However, fractional spurs can also arise from another interference mechanism that involves parasitic coupling between the various constituent PLL blocks, e.g., between the RF digitally/voltage-controlled oscillator (DCO/VCO) and PD. Such a coupling mechanism is now becoming prominent in commercial system-on-chip (SoC) implementations, which inevitably entail aggressive cost-down and area minimization by bringing closer the aggressor and victim circuitry while sharing their supply/ground pads [8], [16].

The case where the PD is a victim and the RF oscillator is an aggressor [16] results in spurs behaving similarly as when induced by the PD's nonlinearity, since both mechanisms ultimately inject the interference into the loop filter. Therefore, such spurs can be addressed by some of the aforementioned spur-mitigation techniques, e.g., an adaptive predistortion. However, these popular techniques are invalid when the oscillator is a victim because the interference is not injected into the loop filter and the spur behavior has a completely different nature [17].

So far, some works [17], [18], [19], [20] have proposed targeted techniques to address the fractional spurs when the oscillator is a victim. However, their hardware cost is relatively high. For example, Ho and Chen [17] need a large memory to store the coupling pattern, and Chen et al. [20] require a dedicated circuit to measure the coupling signal and to inject the cancellation pattern. Considering that the exact strength and effects of the coupling signals are nearly impossible to predict during the design phase [16], it is thus difficult to justify the effort of finalizing these coupling mitigation methods until after the chip is measured.

The existing coupling-mitigation methods with the oscillator being the victim require a high hardware cost mainly because they intend to address the interference injected from outside (e.g., Chen et al. [20] tackle the interference of supply ripple raised by a dc–dc converter), whose frequency and pattern are independent of the PLL operation. However, in many cases, the most critical interference signals originate from *within* the PLL itself and so this is termed "self-interference" [16]. In this article, we specifically study the self-interference signal coupled from a PLL's reference clock (FREF) to the RF oscillator, while noting that the interference pattern is: 1) almost sinusoidal and 2) synchronized with the oscillator phase (when the PLL is locked).

Based on these two features of self-interference, we propose a new method to suppress such oscillator-victimized fundamental fractional spurs by injecting a well-designed cancellation pattern into the PD. Although this inject-and-cancel behavior might look similar to the existing counterparts addressing arbitrary spurs raised by external interference (e.g., [17], [20]), there is a significant difference between their respective starting points—The prior arts must blindly learn the spur cancellation (SC) pattern, while the proposed

Manuscript received 7 October 2023; revised 3 January 2024 and 23 March 2024; accepted 13 April 2024. Date of publication 7 May 2024; date of current version 24 October 2024. This article was approved by Associate Editor Jaehyouk Choi. This work was supported by Sony Europe B.V. *(Corresponding authors: Zhong Gao; Robert Bogdan Staszewski.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/JSSC.2024.3393478.

Digital Object Identifier 10.1109/JSSC.2024.3393478

method readily exploits the two aforementioned features of self-interference to construct the desired SC pattern. This pattern-aware design methodology benefits in a much lower hardware overhead and higher flexibility, especially when used in frequency hopping. First, by assuming a sinusoidal interference pattern, the large memory typically used for learning the interference pattern becomes thus unnecessary and can be straightforwardly replaced by a more compact sinusoidal generator. A simple sinusoidal waveform also makes it possible to agilely adjust the amplitude and phase of the SC pattern according to the precisely known PLL's transfer function when the PLL hops to nearby channels, thereby saving the efforts on recalibration. Second, by exploiting the condition that the self-interference signals are synchronized with the PLL's output-clock phase, injecting the canceling signal can be achieved by simply reusing the same hardware as in some of the aforementioned strategies mitigating the PD-nonlinearity-raised spurs, e.g., a lookup table (LUT) predistorting the PD's nonlinearity according to the expected PLL output phase [6], [7], [21].

Consequently, the proposed method requires no additional hardware and can be applied as a firmware patch to fix unexpected spurs on a fabricated chip, as an alternative to a costly new retape-out cycle. For example, after the chip's fabrication, the firmware can perform a foreground calibration of the desired *sinusoidal* SC pattern at the chosen frequencies and temperatures, and then store the corresponding phase and amplitude parameters in a parameter table. During the chip's regular operation, the firmware can read the temperature and operating frequency information from the chip, and then interpolate a suitable SC pattern according to the parameters prestored in the parameter table. The timeline to complete this parameter table depends on the chip's application case. For applications less sensitive to cost, the content table can be completely measured and frozen during the factory testing; for cost-sensitive applications, the table can be updated incrementally during the chip's idle time by the embedded controlling software when the chip is experiencing a case not yet covered by the existing table. Regardless of which strategy is finally adopted to update the table, the spur issue can be fixed without the additional chip redesign cycle. This can significantly accelerate the time to market.

This article is organized as follows. Section II discusses the characteristics of fractional spurs caused by interference injected at two domains, i.e., through the PD and into the oscillator, thus providing the foundation for distinguishing the spur-raising mechanisms and to develop the proposed SC method. Section III analyzes the features of self-interference, especially that injected into the DCO, paving the way for developing the SC strategy in Section IV. Section V discloses how the proposed SC strategy was applied to a fabricated digital PLL chip modified from [21]. Then, Section VI demonstrates the measured cancellation performance.

II. Frequency-Dependent Behavior of Spurs

Fig. 1(a) depicts a simplified diagram of a digital type-II PLL,[1] which generates a variable clock (CKV) at frequency f_0

[1]Although the spur behavior is discussed within the framework of a digital PLL, the conclusions are equally valid for analog PLLs.

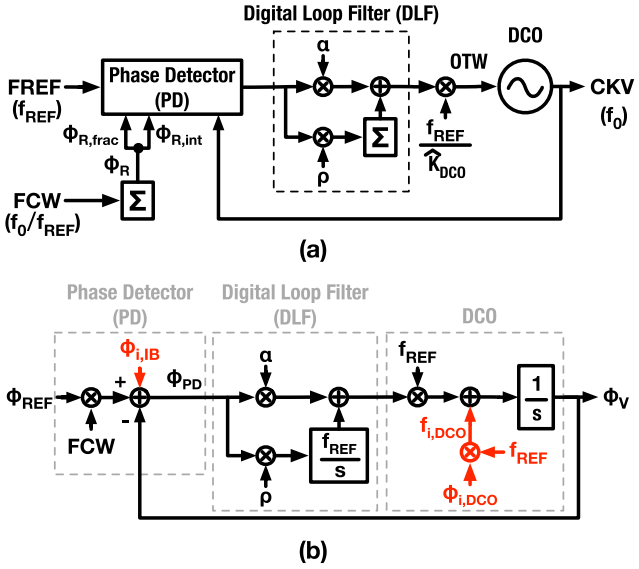

Fig. 1. (a) Block diagram and (b) phase domain model of a type-II PLL.

according to a FREF clock with frequency f_{REF}. The frequency multiplication ratio of f_0/f_{REF} is defined by the frequency control word (FCW). During the PLL operation, the PD constantly samples the CKV phase at the FREF timing grid, then compares it with the normalized[2] prediction, ϕ_{R}, obtained by accumulating FCW and consisting of a fractional part $\phi_{\mathrm{R,frac}}$ and an integer part $\phi_{\mathrm{R,int}}$, in order to extract the phase error of CKV. The detected error first feeds into the digital loop filter (DLF), consisting of the parallel proportional and integration paths, respectively, scaled by coefficients α and ρ. Then, the filtered error is denormalized into the oscillator tuning word (OTW) by $f_{\mathrm{REF}}/\widehat{K}_{\mathrm{DCO}}$, where $\widehat{K}_{\mathrm{DCO}}$ is the estimated gain (i.e., step size) of the DCO. Finally, OTW tunes the DCO frequency to correct the phase error on the output clock CKV.

To assist with analyzing the PLL behavior in face of disturbances, Fig. 1(b) sketches the phase-domain model of Fig. 1(a). Signals ϕ_{REF} and ϕ_{V} are, respectively, the normalized *excess* phase of FREF and CKV, which are additional phase departure components from their respective carrier phase.[3] All phase signals in this model refer to the CKV period, except for ϕ_{REF}, which refers to the FREF period. Consequently, ϕ_{REF} is rescaled by multiplying FCW before subtracting ϕ_{V}. In addition, $\widehat{K}_{\mathrm{DCO}}$ is assumed to be well estimated so as to perfectly cancel out with the DCO resolution, thereby invisible in this phase domain model.

Generally, a PLL suffers from two types of interference mechanisms which generate spurs in the DCO output spectrum under the natural condition that the corresponding disturbance signals are periodic. The first type may originate in the circuitry along the FREF path, but ultimately injects disturbance into the loop through the PD, as $\phi_{\mathrm{i,IB}}$ in Fig. 1(b). The transfer

[2]Generally, phase is 2π-periodic. However, for convenience sake, it is preferred to utilize a *normalized* phase with a period of 1 in the phase-domain model of digital PLLs [22]. In this article, ϕ represents a normalized phase, and θ represents a 2π-periodic phase.

[3]Due to this consideration, the ϕ_{R}-related component, which predicts the ideal CKV carrier phase in Fig. 1(a), is not visible in Fig. 1(b).

function from $\phi_{\mathrm{i,IB}}$ to ϕ_{V} reads as

$$\frac{\phi_{\mathrm{V}}(s)}{\phi_{\mathrm{i,IB}}(s)} = \frac{\alpha \cdot s/f_{\mathrm{REF}} + \rho}{(s/f_{\mathrm{REF}})^2 + \alpha \cdot s/f_{\mathrm{REF}} + \rho} \tag{1}$$

which is low-pass and indicates the $\phi_{\mathrm{i,IB}}$-induced spurs can be attenuated by lowering the PLL bandwidth, more specifically through decreasing α. Therefore, such interference is named "in-band interference" in this work. An example of this would be an interference signal that superimposes on FREF and disturbs the FREF clock buffer's output delay [16]. Another example would be a supply ripple, which modulates the output time of a digital-to-time converter (DTC) [23], a subblock inside the PD. From a behavioral perspective, the nonlinearity of the phase detection blocks (e.g., DTC nonlinearity [6]) disturbs the PLL in the same way as $\phi_{\mathrm{i,IB}}$ would. Thus, this can also be categorized as a source of $\phi_{\mathrm{i,IB}}$ for conceptual convenience.

The second type of interference mechanism is the parasitic coupling to the DCO, denoted as $\phi_{\mathrm{i,DCO}}$ in Fig. 1(b). Such interference can directly disturb (as a physical mechanism) either the DCO phase or its frequency. However, both types of influence can be time-averaged to a disturbing frequency for the sake of simplifying the analysis [24]. Therefore, Fig. 1(b) interprets $\phi_{\mathrm{i,DCO}}$ as disturbing the DCO frequency by $f_{\mathrm{i,DCO}}$ which gradually affects ϕ_{V} by means of the DCO's phase integration property (described by $1/s$). The resulting phase error exhibits a bandpass frequency characteristic according to the following transfer function from $\phi_{\mathrm{i,DCO}}$ to ϕ_{V}, i.e.,

$$\frac{\phi_{\mathrm{V}}(s)}{\phi_{\mathrm{i,DCO}}(s)} = \frac{1}{\alpha + (s/f_{\mathrm{REF}} + \rho \cdot f_{\mathrm{REF}}/s)}. \tag{2}$$

The peak value of this function is $1/\alpha$ [reached at frequency $f = (\rho)^{1/2} \cdot f_{\mathrm{REF}}/(2\pi)$], indicating the $\phi_{\mathrm{i,DCO}}$-induced spurs can be suppressed by increasing α or, in other words, by widening the PLL bandwidth. This is the opposite trend compared with the spurs raised by $\phi_{\mathrm{i,IB}}$. Therefore, these two types of interference-induced spurs can be distinguished by observing how the spur levels change with α (or generally with the PLL bandwidth).

The above discussion considers $\phi_{\mathrm{i,IB}}$ and $\phi_{\mathrm{i,DCO}}$ independently. However, if $\phi_{\mathrm{i,IB}}$ and $\phi_{\mathrm{i,DCO}}$ originate from synchronized sources, i.e., at the same frequency and with a fixed phase offset, $\phi_{\mathrm{i,IB}}$ and $\phi_{\mathrm{i,DCO}}$ will exhibit a fixed phase and amplitude relationship, e.g.,

$$\phi_{\mathrm{i,IB}}(s) = \lambda \cdot \phi_{\mathrm{i,DCO}}(s) \tag{3}$$

where λ is a *complex* number. Interestingly, the effects of synchronous $\phi_{\mathrm{i,IB}}$ and $\phi_{\mathrm{i,DCO}}$ ultimately imposed on ϕ_{V} may cancel each other at a particular frequency according to

$$\begin{aligned}\phi_{\mathrm{V}}(s) &= \frac{\phi_{\mathrm{V}}(s)}{\phi_{\mathrm{i,IB}}(s)}\phi_{\mathrm{i,IB}}(s) + \frac{\phi_{\mathrm{V}}(s)}{\phi_{\mathrm{i,DCO}}(s)}\phi_{\mathrm{i,DCO}}(s) \\ &= \frac{\phi_{\mathrm{V}}(s)}{\phi_{\mathrm{i,IB}}(s)} \cdot \lambda \cdot \phi_{\mathrm{i,DCO}}(s) + \frac{\phi_{\mathrm{V}}(s)}{\phi_{\mathrm{i,DCO}}(s)}\phi_{\mathrm{i,DCO}}(s) \\ &= \frac{(\alpha\lambda + 1) \cdot s/f_{\mathrm{REF}} + \lambda\rho}{(s/f_{\mathrm{REF}})^2 + \alpha \cdot s/f_{\mathrm{REF}} + \rho} \cdot \phi_{\mathrm{i,DCO}}(s)\end{aligned} \tag{4}$$

which contains a zero at

$$f_z = -\frac{\lambda\rho}{\alpha\lambda + 1} \cdot \frac{f_{\mathrm{REF}}}{2\pi}. \tag{5}$$

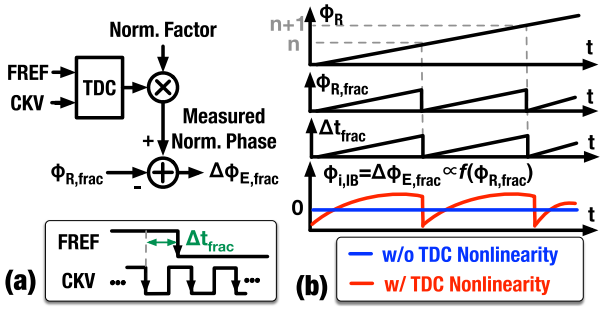

Fig. 2. In-band interference caused by the TDC-nonlinearity is synchronous with $\phi_{\mathrm{R,frac}}$. (a) Hardware setup of using the TDC to detect the fractional part of CKV's phase error. (b) Waveforms illustrating the TDC-nonlinearity-induced in-band interference pattern ($\phi_{\mathrm{i,IB}}$) being synchronous with the $\phi_{\mathrm{R,frac}}$ sequence.

Therefore, when $\phi_{\mathrm{i,DCO}}$ gives rise to spurs in the PLL output spectrum, we can design a synchronous $\phi_{\mathrm{i,IB}}$ pattern for their elimination.

III. Theory of Synchronous Self-Interference

According to Section II, spurs can be readily canceled, provided they are caused by *synchronized* sources. In a locked PLL, most of the self-interference signals, which originate from within the PLL, are synchronized, i.e., each showing a fixed phase offset relative to the ϕ_{R} sequence, or more accurately its wrapped version—the $\phi_{\mathrm{R,frac}}$ sequence.[4]

This section will first explain the synchronicity with an example of in-band self-interference, and then specifically discuss the synchronicity of DCO-interference arising from the aggressor being the FREF clock, thus paving the way for developing a strategy of canceling the resulting spurs.

A. Example Illustrating Synchronicity

The synchronicity of self-interference can be understood with an example of an in-band phase-error pattern caused by the phase-detection nonlinearity (which is also categorized as an in-band interference from the behavioral perspective): In a fractional-N PLL shown in Fig. 1(a), the fractional part of the sampled CKV phase is proportional to the time difference between the significant (here, falling) FREF edge and its preceding significant (here, falling) CKV edge, denoted as Δt_{frac}. At the implementational level, such a fractional phase can be obtained by quantizing Δt_{frac} with a time-to-digital converter (TDC) and then normalizing the quantized result [22], as shown in Fig. 2(a). In an ideal locked PLL, i.e., without noise, TDC nonlinearity, and quantization error, the measured fractional phase would be perfectly equal, and thereby cancel out, the predicted value $\phi_{\mathrm{R,frac}}$. Consequently, the fractional part of the detected phase error, i.e., $\Delta\phi_{\mathrm{E,frac}}$, would always be zero and would not disturb the loop. However, if the TDC nonlinearity is present, the TDC output will contain a Δt_{frac}-related error [see Fig. 2(b)]. This error results

[4]Note that the *synchronized* phase relationship is more general than the narrow case of clock edge *synchronization*. The former requires the aligned/synchronous clock edges to be constrained by a fixed phase offset, while the latter requires the phase offset to be (nearly) zero.

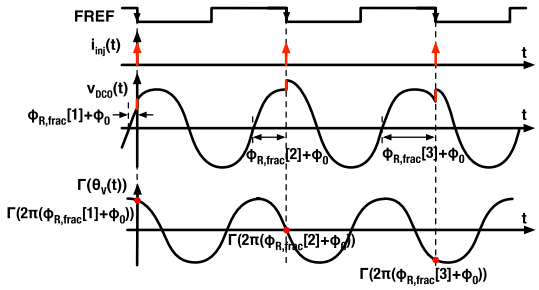

Fig. 3. Waveforms illustrating how FREF events can disturb the DCO phase that is embedded in the waveform $v_{\mathrm{DCO}}(t)$. This is by means of injecting current $i_{\mathrm{inj}}(t)$ into a locked PLL.

in a $\phi_{\mathrm{R,frac}}$-related pattern in $\Delta\phi_{\mathrm{E,frac}}$, acting as an in-band interference. The interference pattern is a function of $\phi_{\mathrm{R,frac}}$, naturally synchronized with it.

Regarding the other types of self-interference, as long as the relationship between the victims and aggressors can be described with $\phi_{\mathrm{R,frac}}$, the corresponding interference signals are also synchronized. One noteworthy example would be the DCO interference raised by FREF circuitry through parasitic coupling paths.

B. Synchronous Interference From FREF to DCO

The waveform diagram in Fig. 3 illustrates how FREF can disturb the DCO phase that is embedded in the DCO waveform $v_{\mathrm{DCO}}(t)$ (i.e., before being rectified or sliced to CKV by a DCO buffer). The FREF clock is typically input to the chip as a sinusoidal waveform, but then its edges are sharpened by an on-chip reference buffer [25], [26], which consumes a large transient current.[5] A tiny portion of the current may be injected into the DCO through various parasitic paths, in the end disturbing the $v_{\mathrm{DCO}}(t)$ waveform and, consequently, its phase. The injected current $i_{\mathrm{inj}}(t)$ is ideally represented as periodic impulses occurring around the FREF's significant (here, falling) edges. This is because the transient current of the reference buffer, the root cause of $i_{\mathrm{inj}}(t)$, is predominantly consumed by a significant-FREF-edge associated transistor, whose size is particularly increased to minimize the jitter degradation [28]. Although the magnitude of the $i_{\mathrm{inj}}(t)$ impulses is the same at each FREF cycle, their impact on the DCO phase varies and can be estimated by the DCO's impulse-sensitivity function (ISF), represented by the 2π-periodic $\Gamma[\theta_{\mathrm{V}}(t)]$, where $\theta_{\mathrm{V}}(t)$ is the instantaneous DCO phase. If n is an integer index number assigned to the i_{inj} impulses, the phase disturbance due to the nth impulse

[5]One might argue that using a reference buffer to perform the sinusoidal-to-square-wave conversion is not so common in commercial SoCs, which typically have an on-chip circuitry directly providing a square-wave FREF. However, this is not the typical case because most of the on-chip clock generators still need an off-chip resonator, e.g., crystal. Such a resonator features a high-quality (Q) factor, indicating strong frequency selectivity, thereby producing a high-purity sinusoidal waveform. Therefore, a reference-like buffer is nearly always needed on-chip to perform the sinusoidal-to-square conversion. Consequently, the corresponding effects discussed with sinusoidal input and reference buffers are always valid (a notable exception would be a PLL using a divided-down DCO clock to directly oversample the sinusoidal reference waveform [27]).

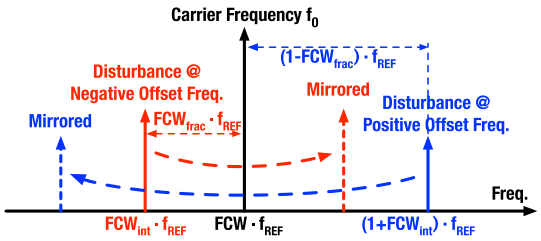

Fig. 4. PLL's output spectrum with spurs caused by the reference interference coupled into the RF oscillator.

can be expressed as $\theta_{\mathrm{dis}}[n] = A_0\Gamma(\theta_{\mathrm{V}}[n])$, where A_0 is the amplitude scaling factor related to the impulse's DCO-coupling strength, and $\theta_{\mathrm{V}}[n]$ stands for the instantaneous DCO phase when it is disturbed by the nth i_{inj} impulse. Since the PLL continuously tracks the DCO phase, $\theta_{\mathrm{V}}[n]$ can be readily estimated by $\phi_{\mathrm{R,frac}}$, which is $\theta_{\mathrm{V}}[n] = 2\pi(\phi_{\mathrm{R,frac}}[n] + \phi_0)$, where $2\pi\phi_{\mathrm{R,frac}}[n]$ is the expected instantaneous component of the DCO phase at the nth significant FREF edge, which raises the nth i_{inj} impulse, and $2\pi\phi_0$ is a constant phase offset accounting for the propagation delay from the i_{inj} impulse generation to the actual moment the DCO phase is disturbed. Consequently, the phase disturbance value becomes $\theta_{\mathrm{dis}}[n] = A_0\Gamma(2\pi(\phi_{\mathrm{R,frac}}[n] + \phi_0))$, indicating the phase disturbance pattern of the i_{inj} impulse train resembles the $\Gamma(2\pi\phi_{\mathrm{R,frac}}[n])$ sequence.

Considering $\phi_{\mathrm{R,frac}}$ is generated by accumulating FCW at the FREF rate [see Fig. 1(a)], the fluctuation frequency of $\phi_{\mathrm{R,frac}}$ can be precisely reconstructed with $\mathrm{FCW_{frac}}$, the fractional part of FCW, i.e., $\mathrm{FCW_{frac}}\cdot f_{\mathrm{REF}}$ or $(1-\mathrm{FCW_{frac}})\cdot f_{\mathrm{REF}}$.[6] Consequently, the DCO phase disturbance pattern resembling $\Gamma(2\pi\phi_{\mathrm{R,frac}}[n])$ also fluctuates at the same frequencies, resulting in fractional spurs at the offset frequencies equal to (or of integer multiples of) $\mathrm{FCW_{frac}}\cdot f_{\mathrm{REF}}$ and $(1-\mathrm{FCW_{frac}})\cdot f_{\mathrm{REF}}$, as shown in Fig. 4, where the spurs at higher order harmonics are ignored for simplicity. Interestingly, the solid-line spurs at the offsets of $-\mathrm{FCW_{frac}}\cdot f_{\mathrm{REF}}$ and $(1-\mathrm{FCW_{frac}})\cdot f_{\mathrm{REF}}$ (relative to the carrier at $\mathrm{FCW}\cdot f_{\mathrm{REF}}$) are located exactly at the absolute FREF harmonics, i.e., $\mathrm{FCW_{int}}\cdot f_{\mathrm{REF}}$, and at $(\mathrm{FCW_{int}}+1)\cdot f_{\mathrm{REF}}$, where $\mathrm{FCW_{int}}$ is the integer part of FCW. Consequently, these spurs may be intuitively attributed to the disturbance of FREF harmonics, as in [8].

Since the fractional spurs that are closer to the carrier tend to be stronger [due to the lower suppression by the PLL dynamics, e.g., the low-pass filtering parts in (1) and (2)], this work focuses on the spurs at the lower offset frequency, i.e., either $\mathrm{FCW_{frac}}\cdot f_{\mathrm{REF}}$ or $(1-\mathrm{FCW_{frac}})\cdot f_{\mathrm{REF}}$. In other words, we concentrate on the *fundamental* fractional spurs at the offset frequency of $|\mathrm{FCW_{frac,s}}|\cdot f_{\mathrm{REF}}$, where $\mathrm{FCW_{frac,s}}$ is the signed fractional FCW and equals the difference between FCW and its closest integer, i.e.,

$$\mathrm{FCW_{frac,s}} = \mathrm{FCW} - \lfloor \mathrm{FCW} \rceil. \tag{6}$$

To explore the possibility of canceling the fundamental fractional spurs by utilizing the zero indicated by (4), the waveform of the DCO interference [$\phi_{\mathrm{i,DCO}}$ or $f_{\mathrm{i,DCO}}$ in

[6]Here, the digital replicas outside the range of [0, f_{REF}) are not considered.

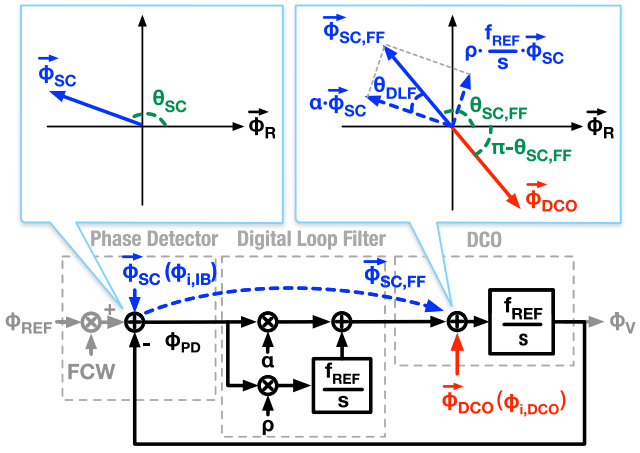

Fig. 5. Phasor diagram illustrating how the in-band interference designed for SC ($\vec{\phi}_{SC}$) is fed-forward by the loop filter (as $\vec{\phi}_{SC,FF}$) and then cancels with the DCO interference ($\vec{\phi}_{DCO}$). Vectors representing these patterns are observed in the coordinate with axes parallel/perpendicular with $\vec{\phi}_R$ representing the $\sin(2\pi\phi_{R,frac}[n])$ sequence.

Fig. 1(b)] should be first mathematically described as a means of assisting with designing the required in-band anti-interferer [$\phi_{i,IB}$ in (3)]. Therefore, the Appendix quantitatively analyzes the DCO phase perturbation, leading to two important findings: First, a sinusoidal waveform can well approximate the phase-perturbation pattern. Second, the frequency of the phase interference and the corresponding SC pattern can be described by

$$f_{SC} = -\text{FCW}_{frac,s} \cdot f_{REF}. \tag{7}$$

These two findings provide in Section IV the foundation for developing the proposed approach for canceling fundamental fractional spurs.

IV. Digitally Intensive Approach for Canceling the DCO-Interference-Induced Fractional Spurs

Section III-B explains how the DCO suffers from synchronous interference by the FREF clock aggressor. As indicated by the zero in (4), the effect of such DCO interference can be canceled by a synchronous in-band interference signal with the proper amplitude and phase. This section will develop a procedure for designing such an in-band anti-interferer.

A. Principle of Designing the In-Band Interference Sequence

To illustrate how the DCO interference can be canceled, its pattern is represented by a vector $\vec{\phi}_{DCO}$ in the phasor diagram in Fig. 5 (top-right). The phasor diagram is observed in a coordinate system with axes parallel/orthogonal to $\vec{\phi}_R$, a virtual unit vector representing the pattern of $\sin(2\pi\phi_{R,frac}[n])$. In such a coordinate system, $\vec{\phi}_{DCO}$ is stationary, i.e., exhibiting a fixed phase offset relative to $\vec{\phi}_R$, since $\vec{\phi}_{DCO}$ is self-interfering and synchronous with $\vec{\phi}_R$ (according to Section III-B). To tackle the spurs raised by $\vec{\phi}_{DCO}$, an in-band interference signal $\vec{\phi}_{SC}$ is deliberately *input* through the PD [see Fig. 5 (top-left)] for the purpose of SC. $\vec{\phi}_{SC}$ is rescaled and rotated by the loop filter and then fed-forward to the DCO as $\vec{\phi}_{SC,FF}$ (the rotation due to the loop filter will be explained later in Section IV-B). To completely cancel the DCO interference, $\vec{\phi}_{SC}$ should be well-constructed to ensure $\vec{\phi}_{SC,FF}$ exhibits the same amplitude as $\vec{\phi}_{DCO}$ but with the 180° phase difference.

Because the $\vec{\phi}_{DCO}$ waveform resembles and is synchronous with $\sin(2\pi\phi_{R,frac}[n])$ (according to Section III-B), the corresponding cancellation signal $\vec{\phi}_{SC}$ should also be a similar sinusoidal wave, i.e., $\vec{\phi}_{SC} = A_{SC} \cdot \sin(2\pi\phi_{R,frac}[n] + \theta_{SC})$, where θ_{SC} is the phase offset relative to $\vec{\phi}_R$, and A_{SC} is the amplitude. Logically, θ_{SC} consists of two parts, i.e., $\theta_{SC} = \theta_{SC,FF} + \theta_{DLF}$. As shown in Fig. 5, $\theta_{SC,FF}$ is the angle between $\vec{\phi}_{SC,FF}$ and $\vec{\phi}_R$, thereby complementary with that between $\vec{\phi}_{DCO}$ and $\vec{\phi}_R$, which is determined by the physical coupling characteristics; θ_{DLF} reflects the angle by which the DLF rotates $\vec{\phi}_{SC}$ to generate $\vec{\phi}_{SC,FF}$, and thereby is a function of the loop parameters and operating frequency. Consequently, the pattern of $\vec{\phi}_{SC}$ is finally described as

$$\vec{\phi}_{SC}[n] = A_{SC} \cdot \sin(2\pi\phi_{R,frac}[n] + \theta_{SC,FF} + \theta_{DLF}). \tag{8}$$

Sections IV-B–IV-D will discuss how to calculate θ_{DLF}, to measure $\theta_{SC,FF}$, and to determine A_{SC}.

B. Calculating θ_{DLF}

θ_{DLF} is incurred while propagating $\vec{\phi}_{SC}$ to $\vec{\phi}_{SC,FF}$ through the two parallel paths of the PLL's loop filter [see Fig. 1(b)]. One path linearly scales the input to $\alpha \cdot \vec{\phi}_{SC}$. The other path, in addition to scaling, rotates the input by −90°, i.e., $(\rho \cdot f_{REF}/s) \cdot \vec{\phi}_{SC}$, where the rotation is attributed to the imaginary factor (i.e., i) in s. The orthogonal components of these two paths superimpose at the final output $\vec{\phi}_{SC,FF}$ [see Fig. 5 (top-right)], which naturally rotates from $\vec{\phi}_{SC}$ by $\theta_{DLF} = \arctan[(\rho f_{REF})/(2\pi\alpha f_{SC})]$. Here, f_{SC} represents the fluctuation frequency of the $\vec{\phi}_{SC,FF}$ pattern, which equals to that of $\vec{\phi}_{DCO}$ expressed in (7) because these two phasors should always rotate at the same speed and be antiphase with each other. Replacing f_{SC} in the above θ_{DLF} expression with (7) yields

$$\theta_{DLF} = -\arctan\left(\frac{\rho}{\alpha} \cdot \frac{1}{2\pi\,\text{FCW}_{frac,s}}\right). \tag{9}$$

This angle can be readily calculated in a digital PLL since $\text{FCW}_{frac,s}$ is easily derived from the system's FCW and ρ/α is easily obtained from the parameter settings of the DLF [see Fig. 1(a)].

C. Measuring $\theta_{SC,FF}$

In a nearly ideal PLL, i.e., without noise and in-band interference, the PD output pattern, represented by $\vec{\phi}_{PD}$, would be entirely determined by the DCO interference, $\vec{\phi}_{DCO}$. Denoting the angle between $\vec{\phi}_{PD}$ and $\vec{\phi}_R$ as θ_{PD} [see Fig. 6(a)], $\theta_{SC,FF}$ can be determined by measuring the curve of θ_{PD}-versus-$|\text{FCW}_{frac,s}|$, whose positive and negative $\text{FCW}_{frac,s}$ branches cross at the point where $\theta_{PD} = \theta_{SC,FF}$ [see Fig. 6(b) (bottom-right)].

The principle of this $\theta_{SC,FF}$-measurement method is explained as follows: By definition, $\theta_{SC,FF}$ is an angle between $\vec{\phi}_R$ and $\vec{\phi}_{SC,FF}$, which is set antiphase with $\vec{\phi}_{DCO}$ (see Fig. 5).

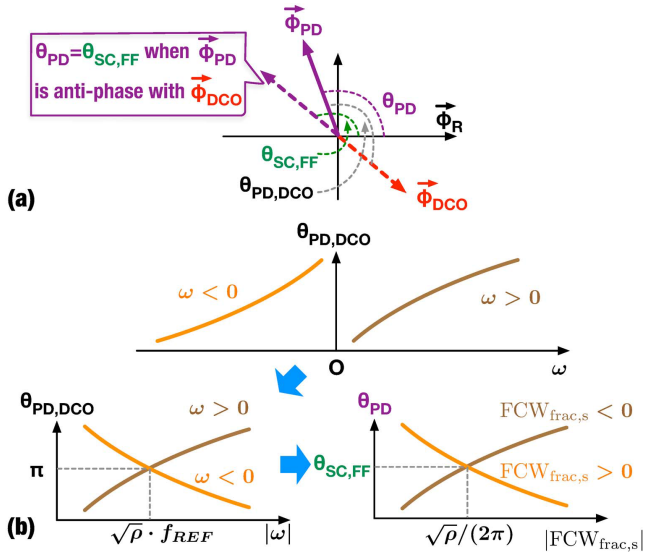

Fig. 6. Principles of $\theta_{SC,FF}$ measurement. (a) Phasor diagram defining the critical angles. (b) Mathematical principle behind the measurement.

Hence, $\theta_{PD} = \theta_{SC,FF}$ when $\vec{\phi}_{PD}$ is antiphase with $\vec{\phi}_{DCO}$. This condition is mathematically described as $\theta_{PD,DCO} = \pi$, where $\theta_{PD,DCO}$ denotes the angle between $\vec{\phi}_{DCO}$ and $\vec{\phi}_{PD}$. Considering θ_{PD} can be measured by correlating $\vec{\phi}_{PD}$ with $\vec{\phi}_R$ (to be explained later), searching for the point where $\theta_{PD,DCO} = \pi$ becomes the key item in measuring $\theta_{SC,FF}$. Actually, $\theta_{PD,DCO}$ is a strong function of the DCO interference angular frequency ω and can be expressed as

$$\theta_{PD,DCO} = \arctan\left(\frac{\frac{\omega}{f_{REF}} - \frac{\rho \cdot f_{REF}}{\omega}}{\alpha}\right) + \pi \tag{10}$$

according to the PLL's phase-domain model in Fig. 1(b). This equation is sketched in the top side of Fig. 6(b), where the $\theta_{PD,DCO}$-versus-ω curve splits into two branches in positive and negative ω. If we fold this curve around the vertical axis, i.e., plotting the $\theta_{PD,DCO}$-versus-$|\omega|$ curve, the two branches will cross at a point with $\omega = (\rho)^{1/2}/(2\pi)$ [see Fig. 6(b) (bottom-left)]. Interestingly, at this crossing point, $\theta_{PD,DCO}$ exactly equals π, which is the case we are searching for. Therefore, measuring θ_{PD} at this point directly yields $\theta_{SC,FF}$. In the realistic measurement, we use the θ_{PD}-versus-$|\text{FCW}_{frac,s}|$ curve to replace $\theta_{PD,DCO}$-versus-$|\omega|$, because ω (the frequency of the DCO interference) is actually swept by tuning $\text{FCW}_{frac,s}$ [according to (7)]. Furthermore, $\theta_{SC,FF}$ is obtained by reading the θ_{PD} value at the crossing point of the positive and negative $\text{FCW}_{frac,s}$ branches [see Fig. 6(b) (bottom-right)], assuming $\vec{\phi}_{DCO}$ does not rotate (relative to $\vec{\phi}_R$) significantly within a narrow frequency range (e.g., $\omega/f_{REF} \in [-(\rho)^{1/2}, (\rho)^{1/2}]$).

The remaining question is how to measure θ_{PD} at each $\text{FCW}_{frac,s}$. Basically, θ_{PD} can be measured by correlating the detected phase error with the *orthogonal* $\vec{\phi}_R$, i.e., the $\cos(2\pi\phi_{R,frac}[n])$ sequence. In practice, the PD output is quantized into the $D_{TDC}[n]$ sequence by a TDC in a digital PLL. Then, θ_{PD} theoretically equals the phase offset θ_x at which the correlation function, i.e.,

$$R_{corr}(\theta_x) = \sum_{n=1}^{N} D_{TDC}[n] \cdot \cos(2\pi\phi_{R,frac}[n] + \theta_x) \tag{11}$$

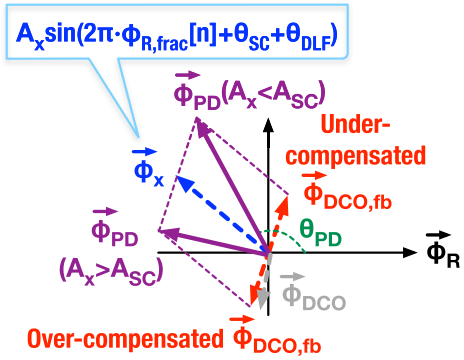

Fig. 7. Phasor diagram showing the sinusoidal component ($\vec{\phi}_{PD}$) at the PD output, which combines the acting stimulus vector $\vec{\phi}_x$ for SC and the detected phase error $\vec{\phi}_{DCO,fb}$ due to the under-/overcompensation of $\vec{\phi}_{DCO}$. Here, the case of $f_{SC} > 0$.

is zero. N here equals the length of a complete $\phi_{R,frac}[n]$ repetition pattern.[7] The reason why θ_{PD} can be measured in this manner lies in the fact that the $\vec{\phi}_{PD}$ pattern in $D_{TDC}[n]$ is proportional to $\sin(2\pi\phi_{R,frac}[n] + \theta_{PD})$, making $R_{corr}(\theta_x - \theta_{PD}) \propto \sin(\theta_x - \theta_{PD})$. In addition, considering $\sin(\theta_x - \theta_{PD})$ also crosses zero when $\theta_x = \pi + \theta_{PD}$, representing the cases $\langle\vec{\phi}_{DCO}, \vec{\phi}_{PD}\rangle = 0$ instead of $\langle\vec{\phi}_{DCO}, \vec{\phi}_{PD}\rangle = \pi$, the following condition must be checked to exclude that improper solution, i.e.,

$$R'_{corr}(\theta_x) = \sum_{n=1}^{N} D_{TDC}[n] \cdot \sin(2\pi\phi_{R,frac}[n] + \theta_x) > 0 \tag{12}$$

where N is the same as that in $R_{corr}(\theta_x)$. Note that the θ_{PD}-measurement method is merely used to conceptually demonstrate the concept. An implementation-oriented alternative can be realized with a gradient-decent algorithm [29].

D. Determining A_{SC}

Once θ_{DLF} and $\theta_{SC,FF}$ are known, the direction of $\vec{\phi}_{SC}$ (in the $\vec{\phi}_R$-based coordinate) is fixed. Then, the optimum amplitude A_{SC} can be determined iteratively as the PLL operates with the $\text{FCW}_{frac,s}$ satisfying $\theta_{PD} \approx \theta_{SC,FF}$, i.e., $|\text{FCW}_{frac,s}| \approx (\rho)^{1/2}/(2\pi)$[8]: A tentative version of $\vec{\phi}_{SC}$, i.e., $\vec{\phi}_x$, is added as an acting stimulus to the PD. Since $\vec{\phi}_x$ aligns with $\vec{\phi}_{SC}$, it takes a form of $\vec{\phi}_x = A_x \cdot \sin(2\pi\phi_{R,frac}[n] + \theta_{SC,FF} + \theta_{DLF})$, where A_x is the amplitude to be updated adaptively, and finally converges to the optimum A_{SC}. After rotated by the PLL's DLF, $\vec{\phi}_x$ adds to the DCO a vector in exact antiphase with $\vec{\phi}_{DCO}$ to cancel the latter's effects. If the amplitude of $\vec{\phi}_x$ is not large enough to cancel $\vec{\phi}_{DCO}$, i.e., $A_x < A_{SC}$, the undercompensated residual $\vec{\phi}_{DCO}$ results in a feedback vector $\vec{\phi}_{DCO,fb}$ at the PD side. Hence, the detected phase error $\vec{\phi}_{PD}$ is dominated by the vector sum of the undercompensated $\vec{\phi}_{DCO,fb}$ and the deliberately added acting stimulus vector $\vec{\phi}_x$, assuming other in-band interference sources are negligible. As shown in the case of $A_x < A_{SC}$ in Fig. 7, the undercompensated $\vec{\phi}_{DCO,fb}$

[7] As explained in [18], the complete length of $\phi_{R,frac}[n]$ is determined by the smallest bit of FCW_{frac}. For example, if $\text{FCW}_{frac} = 2^{-5} + 2^{-7}$, $\phi_{R,frac}[n]$ starts to repeat after 2^7 consecutive data samples.

[8] Operating at such a frequency simplifies the convergence analysis, as will be explained later.

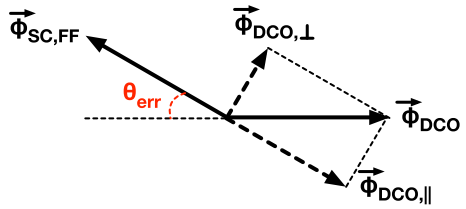

Fig. 8. Phasor diagram illustrating the $\vec{\phi}_{DCO}$ cancellation residue due to the phase offset error in $\vec{\phi}_{SC}$, i.e., θ_{err}.

is almost antiphase with $\vec{\phi}_{DCO}$, considering $\langle\vec{\phi}_{DCO}, \vec{\phi}_{DCO,fb}\rangle \approx \pi$ when the PLL operates with $|FCW_{frac,s}| \approx (\rho)^{1/2}/(2\pi)$ (see Section IV-C). Consequently, the angle between $\vec{\phi}_R$ and $\vec{\phi}_{PD}$ is smaller than that with $\vec{\phi}_x$, i.e., $\theta_{PD} < \theta_{SC,FF} + \theta_{DLF}$. On the contrary, if the amplitude of $\vec{\phi}_x$ is larger than the optimum, i.e., $A_x > A_{SC}$, the PD will get an overcompensated $\vec{\phi}_{DCO,fb}$, which is antiphase with the undercompensated one and finally results in $\theta_{PD} > \theta_{SC,FF} + \theta_{DLF}$ (see the case of $A_x > A_{SC}$ in Fig. 7). Consequently, A_x can be iteratively updated by accumulating the error between θ_{PD} and $\theta_{SC,FF} + \theta_{DLF}$, i.e., $\theta_{E,PD} = \theta_{SC,FF} + \theta_{DLF} - \theta_{PD}$. As a result, A_x should finally converge to the point $\theta_{PD} = \theta_{SC,FF} + \theta_{DLF}$, indicating $\vec{\phi}_x$ perfectly cancels the effect of $\vec{\phi}_{DCO}$ so that $\vec{\phi}_{DCO,fb} = \vec{0}$. At that moment, $A_x = A_{SC}$.

Note that the example in Fig. 7 merely demonstrates the case with a positive frequency of DCO interference, i.e., $f_{SC} > 0$. When $f_{SC} < 0$, both $\vec{\phi}_x$ and $\vec{\phi}_{DCO,fb}$ would be mirrored from the $\vec{\phi}_{DCO}$ vector, since the associated angles are inverted according to (9) and (10). Consequently, the cases of $A_x < A_{SC}$ and $A_x > A_{SC}$ would, respectively, result in negative and positive $\theta_{E,PD}$. This is opposite to the situation with $f_{SC} > 0$. Therefore, A_x needs to be updated by accumulating $-\theta_{E,PD}$, and can still converge to $A_x = A_{SC}$.

E. Residual Spur Level Due to Calibration Inaccuracy

The accuracy of the designed $\vec{\phi}_{SC}$ pattern determines the spur-suppressing performance. After applying the cancellation technique, the error in $\vec{\phi}_{SC}$ amplitude A_{SC} directly determines the residual spur level. Because $\vec{\phi}_{SC}$ is injected as the PLL's in-band interference, its error (i.e., the portion that cannot be canceled by $\vec{\phi}_{DCO}$) can directly add to the PLL's output phase and show up as spurs when within the loop's low-pass characteristics (this fact will be further exploited in Section V-C). The spur level can be estimated by inspecting (22) in the Appendix, which describes the oscillator's output waveform in the presence of phase interference. There, A_k can be treated as the *amplitude error* of $\vec{\phi}_{SC}$ strictly due to the inaccurate A_{SC}. Equation (22) indicates the resulting spur level is $20\log_{10}(A_k/2)$ dBc, where A_k represents the error of A_{SC} in the unit of 2π-periodic phase.

The error in the $\vec{\phi}_{SC}$ phase offset, i.e., $\theta_{SC,FF} + \theta_{DLF}$, determines the extent to which the original spur can be suppressed. A qualitative analysis is given below. In an ideal case with perfect $\vec{\phi}_{SC}$, the SC pattern fed-forward to the DCO, i.e., $\vec{\phi}_{SC,FF}$, should be exactly antiphase with the DCO interference $\vec{\phi}_{DCO}$, as shown in Fig. 5 (top-right). However, when the phase offset term of $\vec{\phi}_{SC,FF}$, i.e., $\theta_{SC,FF} + \theta_{DLF}$, contains the error of θ_{err}, as shown in Fig. 8, $\vec{\phi}_{SC,FF}$ will misalign with $\vec{\phi}_{DCO}$. As a result, the $\vec{\phi}_{DCO}$ component parallel with $\vec{\phi}_{SC,FF}$, i.e., $\vec{\phi}_{DCO,\parallel}$, can be properly canceled; but the component orthogonal to $\vec{\phi}_{SC,FF}$, i.e., $\vec{\phi}_{DCO,\perp}$, will remain uncompensated, thus causing spurs. The amplitude ratio between $\vec{\phi}_{DCO,\perp}$ and $\vec{\phi}_{DCO}$ is determined by $|\vec{\phi}_{DCO,\perp}|/|\vec{\phi}_{DCO}| = \sin(\theta_{err})$, indicating the spur level cannot be suppressed better than $-20\log_{10}(\sin(\theta_{err}))$ dB.

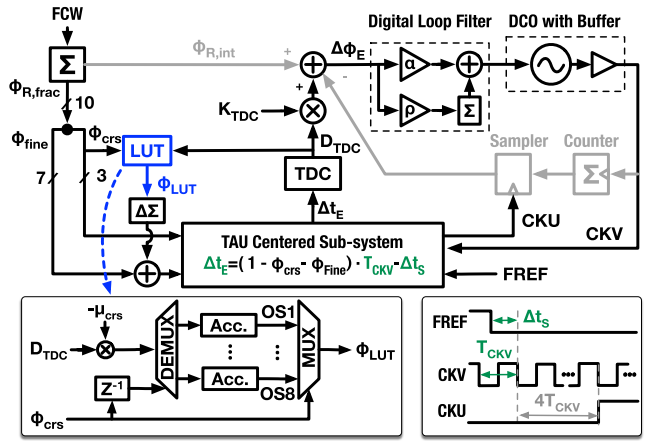

Fig. 9. PLL diagram emphasizing the details related to SC.

V. Implementation of the Spur Cancellation Strategy

The SC strategy proposed in Section IV is applied in an off-line manner to a fractional-N digital PLL chip modified from [21], which exhibits fractional spurs due to the FREF-induced DCO interference. The PLL operational information, i.e., sequences representing $\vec{\phi}_R$ and $\vec{\phi}_{PD}$, is stored in an on-chip memory for debugging. The information is then read out and processed by MATLAB to design the SC pattern $\vec{\phi}_{SC}$. Next, the $\vec{\phi}_{SC}$ pattern is written to an on-chip LUT, whose content is added to the appropriate phase-detection block signals according to the instantaneous $\phi_{R,frac}$ value. This guarantees that the injected $\vec{\phi}_{SC}$ pattern is synchronous with $\vec{\phi}_R$ and is able to cancel the fractional spurs raised by the synchronous DCO interference. This section will disclose the PLL chip details and the procedure for determining the $\vec{\phi}_{SC}$ parameters.

A. Details of the PLL Chip

Fig. 9 sketches a system diagram of the PLL. Similar to the simplified PLL in Fig. 1(a), the implemented PLL constantly samples the CKV phase at the grid of FREF clock. Then, the sampled CKV phase is compared with the ideal one predicted by accumulating FCW in order to extract the CKV phase error $\Delta\phi_E$. The extracted $\Delta\phi_E$ passes through the DLF and tunes the DCO to correct the CKV phase error. Considering the predicted CKV phase consists of the fractional and integer parts, respectively, $\phi_{R,frac}$ and $\phi_{R,int}$, the phase error extraction is performed in two parallel paths.

On the $\phi_{R,int}$-related branch, the number of CKV's significant (falling) edges is constantly monitored by the counter. At the rising edge of the update clock CKU, which aligns with the fifth CKV falling edge after FREF, the counter value

is sampled to obtain the *integer* part of the CKV phase at the FREF grid [22]. The sampled phase cancels with $\phi_{R,int}$ to extract the *integer* part of $\Delta\phi_E$.

Regarding the $\phi_{R,frac}$-associated path, CKV's fractional phase reflects on Δt_S, which is the instantaneous time offset between the FREF and the first subsequent CKV falling edges. In an ideal case without any noise and interference, $\Delta t_S = (1-\phi_{R,frac})\cdot T_{CKV}$, in which T_{CKV} is the nominal CKV period. Hence, the CKV's fractional phase error reflects on the time error, $\Delta t_E = (1-\phi_{R,frac})\cdot T_{CKV} - \Delta t_S$, which is extracted by the time-mode arithmetic unit (TAU) proposed in [1]. The TAU samples T_{CKV}, conceptually scales it with $(1-\phi_{R,frac})$, cancels it with the sampled Δt_S, and outputs the residue as the time offset Δt_E. At the implementation level, $\phi_{R,frac}$ splits into ϕ_{crs} and ϕ_{fine}, used for the coarse and fine T_{CKV} scaling, respectively. The realized Δt_E extraction expression is adapted accordingly (see Fig. 9).

The extracted Δt_E is quantized by a TDC and then normalized to the fractional phase error by multiplying with the factor of K_{TDC}. The fractional phase error finally adds to the integer part (extracted by the $\phi_{R,int}$-related branch) to arrive at the overall phase error $\Delta\phi_E$.

In the implemented PLL, the TAU scales T_{CKV} with 10-b accuracy, where ϕ_{crs} and ϕ_{fine}, respectively, tune the highest 3 and lowest 7 bits. Considering the ϕ_{crs}-associated T_{CKV}-scaling error dominates the TAU's overall integral nonlinearity (INL), an LUT tackles this issue by adding a ϕ_{crs}-dependent compensation signal ϕ_{LUT} to ϕ_{fine}. To prevent the TAU resolution from limiting the compensation accuracy, ϕ_{LUT} is noise-shaped by a first-order $\Delta\Sigma$-modulator before adding it to ϕ_{fine}.

The content of the LUT is calibrated by a least mean squre (LMS)-based algorithm [21] sketched in Fig. 9 (bottom-left): After the ϕ_{crs} code is used, the resulting TDC output D_{TDC} is scaled by the step-control factor μ_{crs} and then demultiplexed to the accumulator associated with the ϕ_{crs} code. The scaled D_{TDC} is accumulated to update the corresponding offset compensation word, i.e., OS. When this ϕ_{crs} code is used next time, the corresponding OS value is multiplexed out to ϕ_{LUT}, finally tuning the TAU for the ultimate purpose of reducing the time error. In the end, the resulting D_{TDC} reduces in magnitude and updates the OS accumulator less significantly. The OS value finally converges to a point that ensures the average D_{TDC} to be 0. Since ϕ_{crs} has 3 bits, only eight accumulators and OS values are needed in the LUT.

The realized chip utilizes a FREF of 40 MHz to synthesize frequencies from 2.6 to 4.0 GHz. It is fabricated in 40-nm CMOS and its micrograph is shown in Fig. 10.

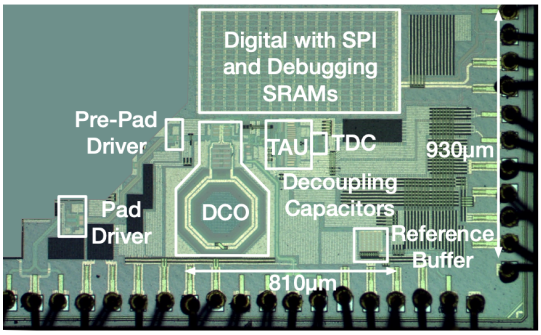

Fig. 10. Chip micrograph.

B. Procedure to Determine the Spur Cancellation Pattern

To tackle the fundamental fractional spurs due to DCO interference, the cancellation pattern $\vec{\phi}_{SC}$ is injected into the loop filter by means of *reusing* the LUT shown in Fig. 9. The LUT values are selected by ϕ_{crs} (the three MSBs of $\phi_{R,frac}$ with the values of $i/8$, $i \in 0, 1, \ldots, 7$), and then added to the PD via ϕ_{LUT}. This way, the reconstructed waveform of $\vec{\phi}_{SC}$ is always synchronized with $\vec{\phi}_R$. To distinguish the LUT content that addresses the in-band interference (e.g., due to TAU nonlinearity) and DCO interference, the LUT is *logically* divided into two parallel sub-LUTs—one, SC-LUT, stores the $\vec{\phi}_{SC}$ pattern for the purpose of SC; while the other, AIB-LUT, compensates the analog in-band interference, as shown in Fig. 11(a).

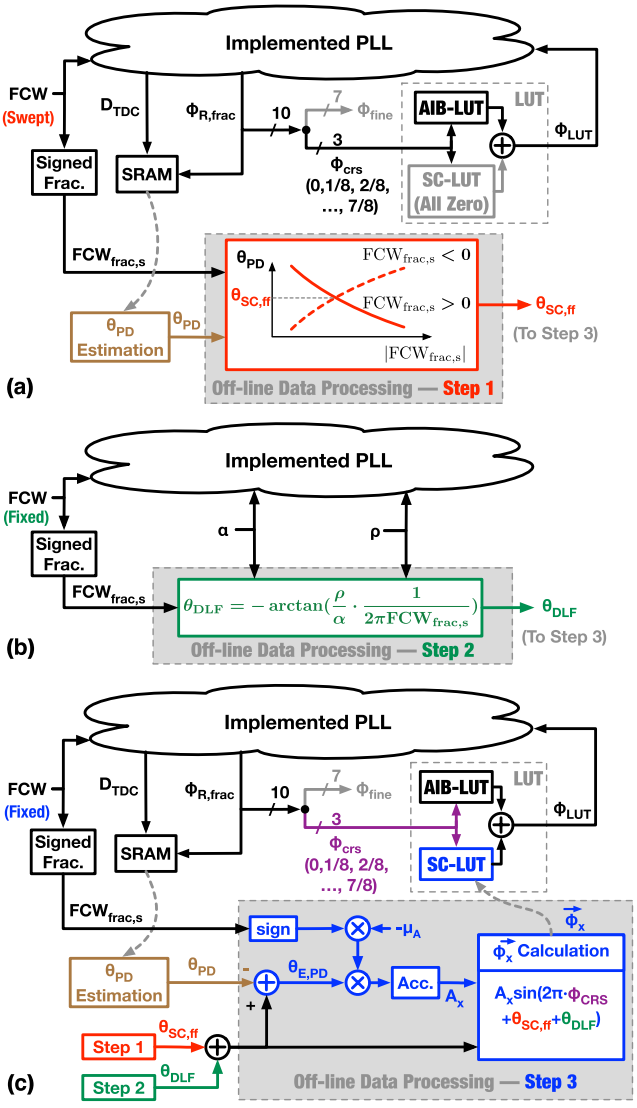

Fig. 11. Steps to determine the SC content of the LUT (in Fig. 9), i.e., the waveform of $\vec{\phi}_{SC}$ which is logically stored in the SC-LUT. (a) Step 1: Estimating $\theta_{SC,FF}$ (red). (b) Step 2: Calculating θ_{DLF} (green). (c) Step 3: Determining A_{SC} (blue).

The AIB-LUT content should be fixed before estimating the SC-LUT content because the processes determining the $\vec{\phi}_{SC}$ parameters (i.e., $\theta_{SC,FF}$ and A_{SC}) assume that the PLL in-band interference is negligible (e.g., already suppressed by the AIB-LUT). The AIB-LUT is calibrated with the LMS-based algorithm shown in Fig. 9 when the PLL is provisioned with $|\text{FCW}_{\text{frac,s}}| \approx 11/16$. The large $|\text{FCW}_{\text{frac,s}}|$ ensures the DCO interference is located at an offset frequency (i.e., $|f_{SC}|$) high enough to be suppressed by the $1/s$ filtering of the DCO.

Regarding the SC-LUT content, the key parameters of $\vec{\phi}_{SC}$, i.e., $\theta_{SC,FF}$, θ_{DLF}, and A_{SC}, are sequentially determined through the three steps, with each shown as a subfigure in Fig. 11. In these steps, measuring θ_{PD} is a common procedure because $\theta_{SC,FF}$ and A_{SC} are estimated based on observing θ_{PD} [as can be found in both steps shown in Fig. 11(a) and (c)]. To measure θ_{PD}, an on-chip SRAM collects the sequences of $\phi_{R,frac}[n]$ and quantized phase error $D_{TDC}[n]$ in the background, after the PLL is locked. These two sequences are read out by software and correlated to estimate θ_{PD} as discussed in Section IV-C.

During the first step of determining $\vec{\phi}_{SC}$, i.e., estimating $\theta_{SC,FF}$ [see Fig. 11(a)], the θ_{PD}-versus-$|\text{FCW}_{\text{frac,s}}|$ curve is measured with all SC-LUT registers remaining at zero. Likewise, $\theta_{SC,FF}$ equals θ_{PD} at the crossing point of this curve's positive and negative $\text{FCW}_{\text{frac,s}}$ branches.

Next, θ_{DLF} is calculated according to (9), where the required parameters can be obtained from the PLL settings—ρ/α from the configurations of the DLF, and $\text{FCW}_{\text{frac,s}}$ from the FCW to be used for the A_{SC} optimization in the next step [see Fig. 11(b)]. After this step, the angle between $\vec{\phi}_{SC}$ and $\vec{\phi}_{R}$ [controlled by $\theta_{SC,FF} + \theta_{DLF}$ in (8)] is readily calculated.

The last step is to determine the optimum amplitude of $\vec{\phi}_{SC}$, i.e., A_{SC}, with the iteration process shown in Fig. 11(c): A $\vec{\phi}_{SC}$-aligned acting stimulus vector $\vec{\phi}_{x}$ with an arbitrary initial amplitude A_x is written into the SC-LUT. Then, θ_{PD} is measured to extract the error $\theta_{E,PD} = \theta_{SC,FF} + \theta_{DLF} - \theta_{PD}$. The extracted error is accumulated to update A_x, so is the acting stimulus vector $\vec{\phi}_{x}$ in SC-LUT. With the updated SC-LUT, θ_{PD} is measured again to correct A_x. Such an iterative process finally converges at a point where the detected phase error vector $\vec{\phi}_{PD}$ aligns with the acting stimulus vector $\vec{\phi}_{x}$ (i.e., $\theta_{E,PD} = 0$), indicating that A_x achieves the optimum value, i.e., $A_x = A_{SC}$. During the iterations, the convergence speed is controlled by the $\theta_{E,PD}$-scaling factor μ_A, and the polarity of accumulating $\theta_{E,PD}$ is controlled by the sign of $\text{FCW}_{\text{frac,s}}$.

C. Adjusting the Spur-Cancellation Pattern Across Frequencies

The process described in Section V-B determines $\vec{\phi}_{SC}$ at a *single* frequency point where A_{SC} is optimized because: 1) the DCO phase disturbance due to interference correlates with the DCO's ISF, which is frequency dependent, and 2) $\vec{\phi}_{SC}$ experiences a frequency-dependent rotation and rescaling by the loop filter. Therefore, $\vec{\phi}_{SC}$ should *theoretically* be recalibrated once the PLL hops to a different frequency. However, a single $\vec{\phi}_{SC}$, mathematically adjusted for N from a single-point calibration, can sufficiently suppress the spurs for the entire FCW range of $[N - 0.5, N + 0.5]$, where N is an arbitrary integer. The simplification comes from the observation that $\vec{\phi}_{SC}$ only needs to be accurate when $\text{FCW}_{\text{frac,s}}$ is in a subrange of $[-(\rho)^{1/2}/(2\pi), (\rho)^{1/2}/(2\pi)]$. This is because the FREF-to-DCO-interference-induced spur peaks at $|\text{FCW}_{\text{frac,s}}| = (\rho)^{1/2}/(2\pi)$, which corresponds to the fractional frequency of $(\rho)^{1/2} f_{REF}/(2\pi)$ [according to (2)], and requires accurate $\vec{\phi}_{SC}$ to cancel the spurs. The $\text{FCW}_{\text{frac,s}}$ range of $[-(\rho)^{1/2}/(2\pi), (\rho)^{1/2}/(2\pi)]$ corresponds to quite a narrow frequency range, e.g., less than 1 MHz in Fig. 13(b) shown later in Section VI. Since this range is so narrow compared to the DCO frequency (e.g., several GHz in this case), the DCO phase disturbance pattern $\vec{\phi}_{DCO}$ will hardly change. Hence, we assume the amplitude and phase of $\vec{\phi}_{DCO}$ to be constant in the FCW range of $[N - 0.5, N + 0.5]$,[9] and then recalculate the $\vec{\phi}_{SC}$ parameters according to PLL loop dynamics: $\theta_{SC,FF}$ does not need any adjustment because it is purely determined by the $\vec{\phi}_{DCO}$ phase, which is assumed constant. θ_{DLF} can be recalculated with (9). Regarding A_{SC}, it should guarantee that $\vec{\phi}_{SC}$ perfectly cancels $\vec{\phi}_{DCO}$ after getting rescaled by the loop filter, i.e.,

$$|\vec{\phi}_{DCO}|^2 = \left(\alpha^2 + \rho^2 f_{REF}^2/(2\pi f_{SC})^2\right) \cdot A_{SC}(f_{SC})^2. \tag{13}$$

Considering $|\vec{\phi}_{DCO}|$ as constant and inserting (7), A_{SC} should be rescaled across $\text{FCW}_{\text{frac,s}}$ as

$$A_{SC}\left(\text{FCW}_{\text{frac,s}}|_{op}\right) = A_{SC}\left(\text{FCW}_{\text{frac,s}}|_{meas}\right) \cdot \sqrt{\frac{1 + \beta\left(\text{FCW}_{\text{frac,s}}|_{meas}\right)^2}{1 + \beta\left(\text{FCW}_{\text{frac,s}}|_{op}\right)^2}} \tag{14}$$

where

$$\beta\left(\text{FCW}_{\text{frac,s}}\right) = \frac{\rho}{\alpha} \cdot \frac{1}{2\pi \text{FCW}_{\text{frac,s}}}. \tag{15}$$

$\text{FCW}_{\text{frac,s}}|_{meas}$ is the $\text{FCW}_{\text{frac,s}}$ with which A_{SC} is calibrated, and $\text{FCW}_{\text{frac,s}}|_{op}$ is the $\text{FCW}_{\text{frac,s}}$ with which the PLL operates in a new frequency.

VI. Measurement Results

This section presents the measurement results of the proposed SC strategy. Since it is only effective for the spurs raised by the DCO interference, we first identify the DCO's interference-induced fundamental fractional spurs, and then apply the proposed techniques to demonstrate the efficacy of the proposed scheme.

A. Identifying Sources of the Fundamental Fractional Spurs

Fig. 12(a) shows the measured spectrum at the PLL output before applying the LUT compensation at a near-integer channel with $\text{FCW}_{\text{frac,s}} \approx 0.00025$. The highest fractional spurs lie at the offset frequency of around ± 10 kHz from the carrier. The magnitude of the offset frequency coincides with $\text{FCW}_{\text{frac,s}} \cdot f_{REF}$, so the spurs are the fundamental fractional spurs in this channel and can be caused by both in-band

[9] Although $\vec{\phi}_{DCO}$ might slightly change within FCW $\in [N - 0.5, N + 0.5]$ but $\text{FCW}_{\text{frac,s}} \notin [-(\rho)^{1/2}/(2\pi f_{REF}), (\rho)^{1/2}/(2\pi f_{REF})]$. This does not raise critical issues because the corresponding spurs exhibit relatively low levels and do not require accurate $\vec{\phi}_{SC}$ for cancellation purpose.

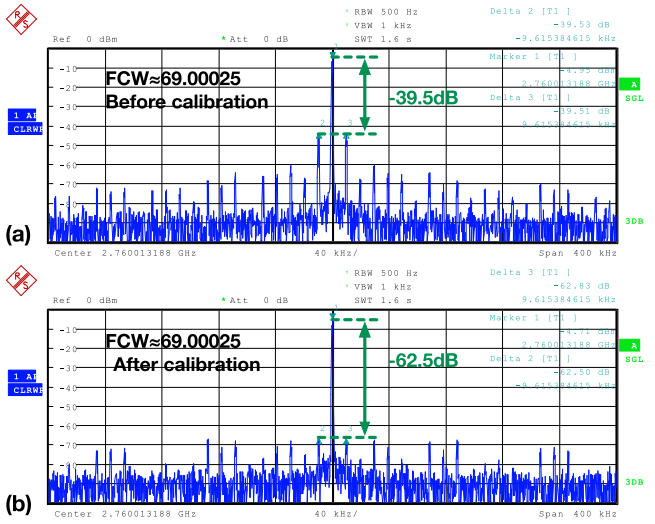

Fig. 12. CKV Spectra (a) before and (b) after utilizing the LUT to suppress the in-band interference.

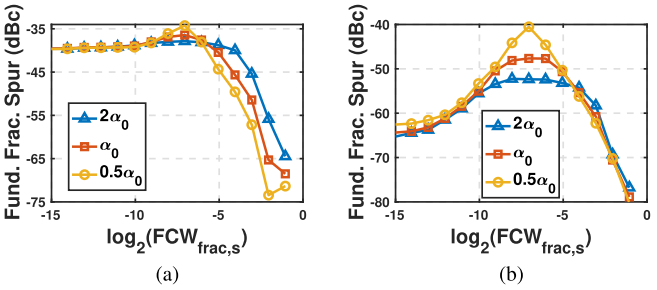

Fig. 13. Measured fundamental fractional-spur levels versus $\mathrm{FCW}_{\mathrm{frac,s}}$ (a) before and (b) after canceling the in-band interference with the LUT in Fig. 9.

and DCO interference.[10] To confirm the dominant source, the fundamental fractional spur level is observed while sweeping the FCW range of $(69, 69.5)$. Assuming the strength of the dominant interference is constant (which is reasonable in the narrow FCW range), the curve of the fundamental-spur-versus-$\mathrm{FCW}_{\mathrm{frac,s}}$ reflects the PLL's frequency response to the interference. As shown in Fig. 13(a), each fundamental-spur-versus-$\mathrm{FCW}_{\mathrm{frac,s}}$ curve exhibits a low-pass characteristic, and the bandwidth increases with the DLF's proportional coefficient α (shown in Fig. 9), which equals to $0.5 \sim 2$ times α_0, the default α value adopted to measure Fig. 12. This trend agrees with (1), indicating that the in-band interference dominates the fundamental fractional spurs.

Afterward, the LUT is calibrated to cancel the effects of in-band interference. Upon applying the LUT compensation, the fundamental fractional spurs in Fig. 12(a) are suppressed to below -62.5 dB, as shown in Fig. 12(b), indicating that the residual in-band interference almost practically vanishes. However, the spur-suppression performance tends to be less effective when the fractional channel frequency increases (but still within the loop bandwidth). As shown in Fig. 13(b), the fundamental fractional-spur curve exhibits a bandpass

[10]Although the phase-detection nonlinearity can also raise fundamental fractional spurs, this mechanism is categorized as in-band interference for conceptual convenience (see Section II).

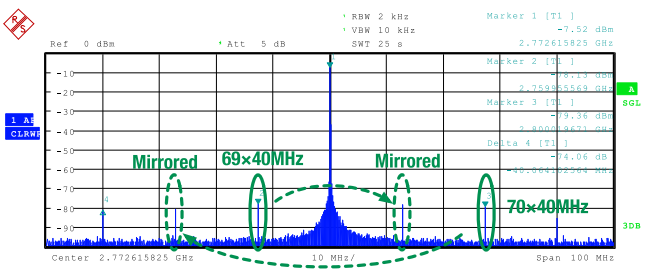

Fig. 14. Spectrum of the free-running DCO with spurs caused by FREF.

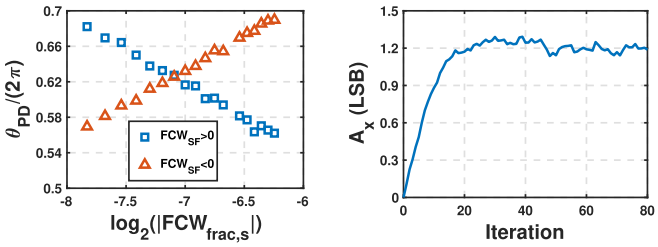

Fig. 15. (a) Measured θ_{PD}-versus-$|\mathrm{FCW}_{\mathrm{frac,s}}|$ curve used for searching $\theta_{\mathrm{SC,FF}}$. (b) Convergence curve of A_{x} to determine A_{SC}.

characteristic and peaks at $\mathrm{FCW}_{\mathrm{frac,s}}$ close to 2^{-7}. In addition, the peak value decreases as α increases. This trend matches (2) and confirms that the DCO interference remains the dominant spur contributor after the in-band interference gets resolved with the LUT.

The DCO interference is thus presumed to be coupled from FREF. Evidence can be found in the output spectrum of the free-running DCO shown in Fig. 14. The spectrum contains spurs at the f_{REF} harmonics (i.e., $69\times$ and $70\times$ of 40 MHz) and their mirrors relative to the main carrier. These spur positions agree with those caused by the mechanism of FREF-to-DCO coupling explained in Fig. 4. The spectrum is measured after disabling all the blocks in Fig. 9 except for the DCO (with buffer) and FREF buffer chain (till the TAU input), so that FREF is the only possible aggressor of DCO. Note that although the reference buffer is placed relatively far from the DCO (see Fig. 10), and also the PD and DCO have separated power domains, the coupling from the FREF to the RF oscillator still limits the PLL's spur performance.

B. Spur Cancellation Performance

After confirming that the fundamental fractional spur is dominated by the synchronous DCO-interference coupled from the FREF buffers, the proposed SC strategy is applied to tackle these spurs.[11] During the process of determining

[11]One might doubt whether it would be worthwhile to adopt the proposed SC strategy because Fig. 13 suggests that the DCO-victimized spur can be simply suppressed by increasing the PLL bandwidth, which is proportional to the loop filter's α coefficient. However, an excessive PLL bandwidth, beyond the optimal point, will increase the in-band noise contribution and eventually degrade the overall phase noise performance. In addition, a couple of factors can also limit the spur-suppression performance. First, the PLL bandwidth cannot be arbitrarily large due to the stability considerations (e.g., the PLL bandwidth is usually less than 1/10 of the reference frequency [30]). Second, the in-band-interference-induced spurs get less attenuated as the PLL bandwidth increases and could finally dominate the PLL's output spur levels. Therefore, suppressing the spurs by increasing the PLL bandwidth does not appear so attractive, given the alternative options.

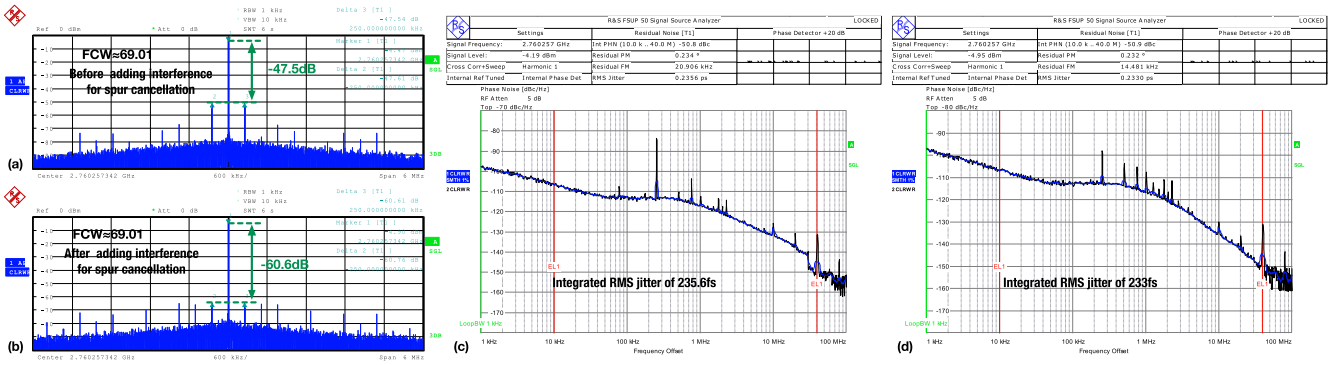

Fig. 16. PLL's output spectrum (a) before and (b) after applying the proposed SC technique at FCW $\approx$ 69.01, and (c) and (d) corresponding phase noise profiles.

the parameters for $\vec{\phi}_{SC}$, the behavioral AIB-LUT holds the same LUT content as that in measuring Fig. 13(b), where the spur levels in the near-integer channels are below -62 dB, indicating that the uncompensated in-band interference is sufficiently suppressed and would not significantly degrade the accuracy in the $\theta_{SC,FF}$ and A_{SC} estimation. Next, we determine the parameters of $\vec{\phi}_{SC}$, i.e., $\theta_{SC,FF}$, θ_{DLF}, and A_{SC}.

To search for $\theta_{SC,FF}$, the θ_{PD}-versus-$|FCW_{frac,s}|$ curve is measured and plotted in Fig. 15(a). $\theta_{SC,FF}$ equals θ_{PD} at the crossing point of the positive and negative $FCW_{frac,s}$ branches, i.e., $0.627 \times 2\pi$.

Then, A_{SC} is optimized at the frequency corresponding to $FCW_{frac,s} \approx 2^{-7}$, which is close to $(\rho)^{1/2}/(2\pi f_{REF})$ [i.e., $|FCW_{frac,s}|$ value at the crossover of the θ_{PD}-versus-$|FCW_{frac,s}|$ curve in Fig. 15(a)] and guarantees the convergence for the A_{SC} search. At this frequency, the corresponding θ_{DLF} is $-0.049 \times 2\pi$ according to (9), and $\rho/\alpha \approx 2^{-6}$. The procedure explained in Fig. 11 (see Step 3) is employed to search for the optimum amplitude of $\vec{\phi}_{SC}$. Fig. 15(b) plots the transient of the acting stimulus amplitude A_x, which starts from 0 and settles at 1.2 after 20 iterations. Since $\vec{\phi}_{SC}$ is injected into the PLL through the LUT related to the $\phi_{R,frac}$ processing (see Fig. 9), the unit of A_x is the LSB of $\phi_{R,frac}$, i.e., 0.001 of the normalized phase.

After setting A_{SC} to 1.2, the final A_x value in Fig. 15(b), $\vec{\phi}_{SC}$ is now fixed for the channel of $FCW_{frac,s} \approx 2^{-7}$. According to the PLL output spectra before and after applying $\vec{\phi}_{SC}$, respectively, shown in Fig. 16(a) and (b), the fundamental fractional spur is suppressed by as much as 13.1 dB, i.e., from -47.5 to -60.6 dB. One may notice that the second harmonic fractional spur grows to the level close to the fundamental one after applying $\vec{\phi}_{SC}$. The rise of harmonics may be attributed to the nonlinearity of the phase detection blocks, e.g., the TAU subsystem and TDC in Fig. 9, in response to the injected $\vec{\phi}_{SC}$.

We note that although the dominant fundamental spur is substantially suppressed by deliberately adding the in-band interference $\vec{\phi}_{SC}$, the phase noise does not degrade. This is supported by the unchanged value of integrated jitter in the case without and with $\vec{\phi}_{SC}$, respectively, shown in Fig. 16(c) and (d).

To showcase the SC performance over the fractional channels, the worst-spur-versus-$FCW_{frac,s}$ curve is swept across the channels with FCW $\in (69, 69.5)$. During this process, A_{SC} and θ_{DLF} are adjusted as per (9) and (14). According to the measurement results in Fig. 17(a), applying $\vec{\phi}_{SC}$ suppresses

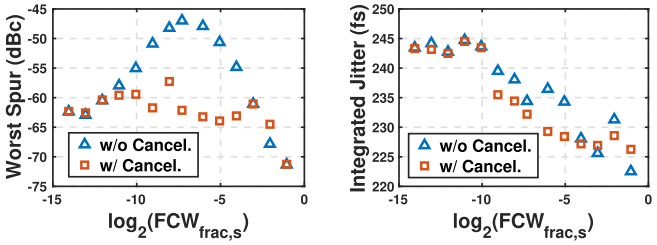

Fig. 17. Comparison of (a) worst fractional spur and (b) integrated jitter versus $FCW_{frac,s}$ before and after applying the proposed SC technique.

TABLE I
PERFORMANCE SUMMARY AND STATE-OF-THE-ART IN LOW-SPUR DIGITAL PLLS

	this work	JSSC'22 [20]	ESSCIRC'16 [17]	JSSC'21 [12]	JSSC'23 [32]	JSSC'23 [33]
Process (nm)	40	40	65	130	65	28
Reference Freq. (MHz)	40	50	--	80	150	250
DCO/VCO Freq. (GHz)	2.68	4.8	3.57	3.36	3.6	9.25
Int. RMS Jitter (fs)	233	428	515	101	96	76.7
Dominant Source of Spurs	Interference to DCO			Phase Detection Nonlinearity		
Canceling DCO/VCO-Victimized Spurs	Yes	Yes	Yes	No	No	No
Worst Spur (dBc)	-60.6	-54.3	-59[1]	-56	-57	-71.9
Spur Improvement (dB)	13.1	15.9	22	--	--	--
Power (mW)	4.4[2]	3.25	21.3	9.2	9.5	17.2
FoM[3] (dB)	-246.2	-242.3	-232.5	-250.3	-250.6	-249.9
Active Area (mm^2)	0.31[4]	0.39	0.63	0.27	0.38	0.31

1. Read from Fig.8 of [17] 2. Supplied by 1.0V except for DCO, which is supplied by 1.2V.
3. FoM=10·log10((Jitter/1s)^2·Power/1mW) 4. Excluding output drivers and debugging SRAMs

the worst spur levels to below −57.8 dB across the fractional channels, proving the effectiveness of the proposed strategy. Meanwhile, the integrated jitter does not degrade either, as per Fig. 17(b).

Table I summarizes the performance of this work as well as the state-of-the-art in low-fractional-spur digital PLLs which demonstrates the low spur level that a well-designed PLL can achieve. We need to point out that it is difficult to fairly compare this work with the majority of the prior arts (e.g., [12], [31], [32]). This is because those works mainly address spurs raised by the phase-detection nonlinearity, while this work (as well as [17] and [20]) addresses the spurs due to parasitic interference (e.g., via magnetic, capacitive, substrate, common ground paths) coupled to the RF oscillator, which nowadays is becoming more problematic, especially in tightly packed RF-SoCs [8], [16]. Compared with the few works also focusing on DCO-victimized spurs, i.e., [17] and [20], this work improves upon the spur and jitter-power FoM performance, mostly thanks to the proposed strategy featuring low overhead in noise, area, and power consumption.

VII. Conclusion

This article analyzed the characteristics of the PLL's self-interference raised by the coupling from the PLL's FREF buffer to the DCO. Based on two features of the self-interference, i.e., sinusoidal pattern and synchronicity with the predicted DCO phase, we developed a digitally intensive strategy that cancels the DCO-interference-induced fundamental fractional spurs utilizing a well-designed pattern injected to the PD, i.e., an in-band interference. The proposed approach reuses the same hardware that was originally designed to eliminate the in-band interference (e.g., the nonlinearity of the phase-detection blocks), thus can be readily applied to a fabricated chip without the need for the chip redesign in order to mitigate the unexpected spurs due to self-interference. More importantly, based on the concept of synchronous-interference cancellation, more strategies can be developed to suppress the impacts of mutual coupling between the blocks inside the PLL. This may help to relax the isolation specifications of each block, reduce the system complexity, and improve the power efficiency of the overall system.

Appendix
Quantitative Analysis of the Synchronous Interference From FREF to DCO

The 2π-periodic *total* phase of the DCO is represented as

$$\theta_{\mathrm{V}} = 2\pi f_0 t + \theta_{\mathrm{V,init}} + \theta_{\mathrm{R2V}}(t) \tag{16}$$

where f_0 is the DCO oscillation frequency, $\theta_{\mathrm{V,init}}$ is the DCO's initial phase at $t = 0$, and θ_{R2V} is the *excess* phase due to the $i_{\mathrm{inj}}(t)$ disturbance. According to [24], the instantaneous angular frequency of θ_{R2V} can be represented by

$$\frac{d\theta_{\mathrm{R2V}}(t)}{dt} = \tilde{\Gamma}[\theta_{\mathrm{V}}(t)] i_{\mathrm{inj}}(t) \tag{17}$$

where $\tilde{\Gamma}(\theta)$ is the 2π-periodic $\Gamma(\theta)$ (DCO's ISF) normalized by the maximum charge displacement across the corresponding node capacitor. Considering that $\theta_{\mathrm{V}}(t)$ is constantly tracked by the PLL, $\theta_{\mathrm{R2V}}(t)$ can be regarded as a tiny perturbation on the ideal DCO phase $(2\pi f_0 t + \theta_{\mathrm{V,init}})$. Hence, $\tilde{\Gamma}[\theta_{\mathrm{V}}(t)]$ can be approximated as $\tilde{\Gamma}(2\pi f_0 t + \theta_{\mathrm{V,init}})$. Moreover, the periodicity of $\tilde{\Gamma}(t)$ and $i_{\mathrm{inj}}(t)$ allows us to expand these two functions with a Fourier series and rewrite (17) as

$$\frac{d\theta_{\mathrm{R2V}}(t)}{dt} = \left[\frac{\tilde{\Gamma}_0}{2} + \sum_{m=1}^{\infty} |\tilde{\Gamma}_m| \cos\left(2\pi m f_0 t + m\theta_{\mathrm{V,init}} + \angle\tilde{\Gamma}_m\right)\right] \cdot \left[\frac{I_{\mathrm{inj,0}}}{2} + \sum_{k=1}^{\infty} |I_{\mathrm{inj,k}}| \cos\left(2\pi k f_{\mathrm{REF}} t + \angle I_{\mathrm{inj,k}}\right)\right] \tag{18}$$

where $\tilde{\Gamma}_m$ and $I_{\mathrm{inj,k}}$ are, respectively, the complex Fourier coefficients of $\tilde{\Gamma}(t)$ and $i_{\mathrm{inj}}(t)$. Abundant intermodulation terms in this equation result in all the sinusoidal phase-modulation components in $\theta_{\mathrm{R2V}}(t)$. According to [30], these sinusoidal components can be regarded as baseband signals that mix with the ideal DCO carrier (at the frequency of f_0) and finally become spurs at the corresponding offset frequencies. Therefore, only the low-frequency components in $d\theta_{\mathrm{R2V}}(t)/dt$ could constitute the root cause of the fundamental fractional spurs at $\pm|\mathrm{FCW}_{\mathrm{frac,s}}| \cdot f_{\mathrm{REF}}$, and so this is the focus in this work. In addition, noticing that $|\tilde{\Gamma}_1|$ is usually the largest among $|\tilde{\Gamma}_m|$'s (e.g., ISF of a conventional LC oscillator is almost sinusoidal [33], thus dominated by the fundamental term with coefficient $|\tilde{\Gamma}_1|$), we only search for the root cause of the fundamental fractional spurs among the low-frequency (LF) intermodulation terms containing $|\tilde{\Gamma}_1|$, and find two candidates represented by

$$\left.\frac{d\theta_{\mathrm{R2V}}(t)}{dt}\right|_{\mathrm{LF},k} = \left|\frac{\tilde{\Gamma}_1 I_{\mathrm{inj,k}}}{2}\right| \times \cos\left[2\pi f_{\mathrm{im}}(k) t + \angle I_{\mathrm{inj,k}} - \theta_{\mathrm{V,init}} - \angle\tilde{\Gamma}_1\right] \tag{19}$$

where $f_{\mathrm{im}}(k)$ is the intermodulation frequency, i.e.,

$$f_{\mathrm{im}}(k) = k f_{\mathrm{REF}} - f_0 \tag{20}$$

and $k = \mathrm{FCW}_{\mathrm{int}}, \mathrm{FCW}_{\mathrm{int}} + 1$. These two $f_{\mathrm{im}}(k)$'s coincide with the offset frequencies of the solid-line spurs in Fig. 4, i.e., $-\mathrm{FCW}_{\mathrm{frac}} \cdot f_{\mathrm{REF}}$ and $(1 - \mathrm{FCW}_{\mathrm{frac}}) \cdot f_{\mathrm{REF}}$. Therefore, the corresponding $d\theta_{\mathrm{R2V}}(t)/dt|_{\mathrm{LF},k}$ term could aptly represent the pattern of DCO interference frequency [proportional to $f_{\mathrm{i,DCO}}$ in Fig. 1(b)], which causes fractional spurs at $\pm\mathrm{FCW}_{\mathrm{frac,s}} \cdot f_{\mathrm{REF}}$.

Considering $\mathrm{FCW} = f_0/f_{\mathrm{REF}}$, the time-varying phase of $d\theta_{\mathrm{R2V}}(t)/dt|_{\mathrm{LF},k}$ observed at the FREF grid (e.g., at $t = n \cdot T_{\mathrm{REF}}$, where n is an arbitrary integer) can be represented by

$$\begin{aligned} 2\pi f_{\mathrm{im}}(k) t &= 2\pi \cdot n \cdot (k - \mathrm{FCW}) \\ &= 2\pi\left(p - \phi_{\mathrm{R,frac}}[n]\right) \end{aligned} \tag{21}$$

where p is an integer. Therefore, $d\theta_{\mathrm{R2V}}(t)/dt|_{\mathrm{LF},k}$ resembles and is synchronous with the sequence of $\sin\left(2\pi\phi_{\mathrm{R,frac}}[n]\right)$. Hence, it is possible to cancel such $d\theta_{\mathrm{R2V}}(t)/dt|_{\mathrm{LF},k}$-induced spurs by adding in-band interference of a scaled and phase-shifted $\sin\left(2\pi\phi_{\mathrm{R,frac}}[n]\right)$ sequence.

One might notice that the fractional spurs are always present in pairs, i.e., equally spaced on both sides of the carrier in Fig. 4, and wonder whether the pair can be canceled by a single-frequency in-band anti-interferer. In fact,

the DCO phase perturbation merely fluctuates at a single frequency $f_{\text{im}}(k)$, according to $\theta_{\text{R2V}}(t)|_{\text{LF},k} = A_k \sin[2\pi f_{\text{im}}(k)t + \theta_k]$, which is obtained by integrating $d\theta_{\text{R2V}}(t)/dt|_{\text{LF},k}$ over time [24] with A_k and θ_k conceptually representing the amplitude and phase offset, respectively. This single-frequency phase error shows up in the total phase of DCO [see (16)] as a tiny perturbation, so the DCO waveform is proportional to

$$\begin{aligned}&\sin\left[2\pi f_0 t + \theta_{\text{V,init}} + \theta_{\text{R2V}}(t)|_{\text{LF},k}\right]\\ &\quad\approx \sin\left(2\pi f_0 t + \theta_{\text{V,init}}\right)\\ &\qquad + \frac{A_k}{2}\sin\left\{2\pi\left[f_0 + f_{\text{im}}(k)\right]\cdot t + \theta_{\text{V,init}} + \theta_k\right\}\\ &\qquad - \frac{A_k}{2}\sin\left\{2\pi\left[f_0 - f_{\text{im}}(k)\right]\cdot t + \theta_{\text{V,init}} - \theta_k\right\}\end{aligned} \tag{22}$$

where the first term stands for the ideal carrier, and the last two terms represent the double-sided spurs around the carrier. Therefore, the double-sided spurs result from a single-side phase perturbation, as predicted by the frequency modulation theory [30]. In other words, once we have canceled the interference component at the frequency of f_{im}, the spurs on both sides of the carrier (with the offset frequency of $\pm|f_{\text{im}}|$) will automatically disappear. In addition, because this work focuses on canceling the fundamental fractional spurs, it cares only about the perturbation at frequency $f_{\text{im}} = -\text{FCW}_{\text{frac}} \cdot f_{\text{REF}}$ or $f_{\text{im}} = (1 - \text{FCW}_{\text{frac}}) \cdot f_{\text{REF}}$ [according to (20)], depending on which one exhibits a smaller absolute value. These two possible frequencies are finally unified as the SC frequency of

$$f_{\text{SC}} = -\text{FCW}_{\text{frac,s}} \cdot f_{\text{REF}}. \tag{23}$$

ACKNOWLEDGMENT

The authors wish to thank Ken Yamamoto of Sony Semiconductor Solutions in Japan, Martin Fritz, Gerd Spalink, and Ben Eitel of Sony Stuttgart Technology Center in Germany for many fruitful technical discussions and project management. They also wish to thank Atef Akhnoukh, Zu Yao Chang, and Dr. Juan Bueno Lopez of Delft University of Technology for technical support.

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