Autonomous Output Supply Scaling for Efficient Multichannel Electrical Stimulation

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***Abstract*—The development of neurostimulation devices for visual and somatosensory prostheses is rapidly gaining momentum, where scaling the number of stimulation channels is crucial to improve treatment efficacy. To this end, optimizing power efficiency is critical, particularly in wirelessly powered systems. Although current-mode stimulation is generally preferred for safety reasons, it is often associated with significant power overhead losses in the output driver. This challenge becomes even more pronounced in multichannel configurations, where the required load voltage varies unpredictably across channels and over time. Compliance monitor circuits have been used to scale the output driver voltage supply, which in turn reduces losses and improves power efficiency. However, existing implementations lead to increased area and power overhead while lacking the ability to adapt rapidly to dynamic load conditions. This work presents a stimulator architecture that enables autonomous output supply scaling per channel, minimizing power dissipation across a wide range of currents and impedances without requiring explicit compliance monitoring. A two-channel prototype fabricated in 0.18 μm CMOS was validated with both linear loads and electrodes. The proposed strategy achieves output-driver efficiencies above 80 % for stimulation currents of 30 kΩ to 95 μA and load impedances from 30 kΩ to 70 kΩ, showing up to 4.3 times improvement compared to a fixed-voltage supply. Furthermore, the circuit shows rapid adaptation to changes in the required output voltage, enabling 100 μs stimulation pulses with a 1 μs inter-pulse delay. This feature allows time-division multiplexing across electrodes with varying load conditions, which could be further explored to increase the number of electrodes served per stimulation channel and thereby enhance scalability.**

***Index Terms*—Electrical stimulation, neural interfaces, supply scaling, multichannel, power efficiency.**

I. Introduction

IMPLANTABLE neuromodulation devices have become integral to treating neurological disorders and advancing innovative applications like visual and somatosensory prostheses [2], [3], [4]. These applications require large-scale, multichannel stimulation systems capable of driving hundreds to thousands of channels [5], [6], [7]. Designing these systems necessitates addressing interdisciplinary challenges, including system-level electronics [8] and high-density, biocompatible electrodes [9].

One of the primary constraints in scaling these systems to large channel counts is efficient power management. Wireless power delivery is preferred for its reduced risk of infection compared to wired approaches. However, safety regulations severely limit the amount of power transferable to the implant [10]. For example, inductive power transfer at 13.56 MHz has a safe exposure limit of 544 μW/mm^2 [11], which translates to a maximum available power in millimeter-sized implants in the order of tens of mW. These limitations emphasize the need for power-efficient stimulator circuits to enable channel scaling.

Current-mode stimulation (CMS) stands out as the preferred method for neural tissue stimulation, primarily for its ability to precisely control the delivered amount of charge, a critical aspect of ensuring patient safety [12]. However, the inherent variability in electrode-tissue-interface impedance and the current amplitude requirements across channels and over time [13] pose significant challenges to the power efficiency of multichannel CMS, as illustrated in Fig. 1. In the conventional approach, a fixed voltage is used to supply all output drivers; hence, it needs to accommodate the channel with the highest tissue voltage requirements. Every channel for which the tissue voltage requirement is below the fixed voltage supply will contribute to an excessive voltage drop over the output driver, leading to increased power dissipation.

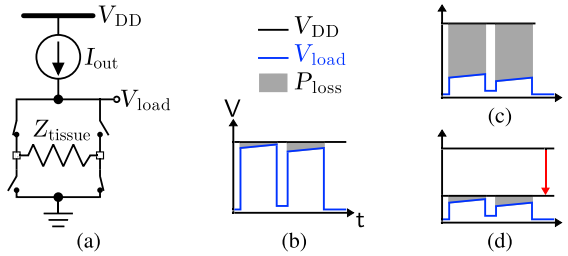

Fig. 1. Illustration of the power efficiency drawback of (multichannel) current-mode stimulation (CMS) in a bipolar configuration. (a) Conventional output stage for CMS with a fixed voltage supply V_{DD}; (b)Output voltage in the case of a good match between the load voltage V_{load} and voltage supply. The gray area indicates overhead losses in the output driver; (c) Output voltage in case of a mismatch between the load voltage and supply voltage, leading to high power dissipation in the output driver; (d) Scaled voltage supply reducing power dissipation in the output driver, and thus increasing the power efficiency for the example in (c). Figure modified from [1].

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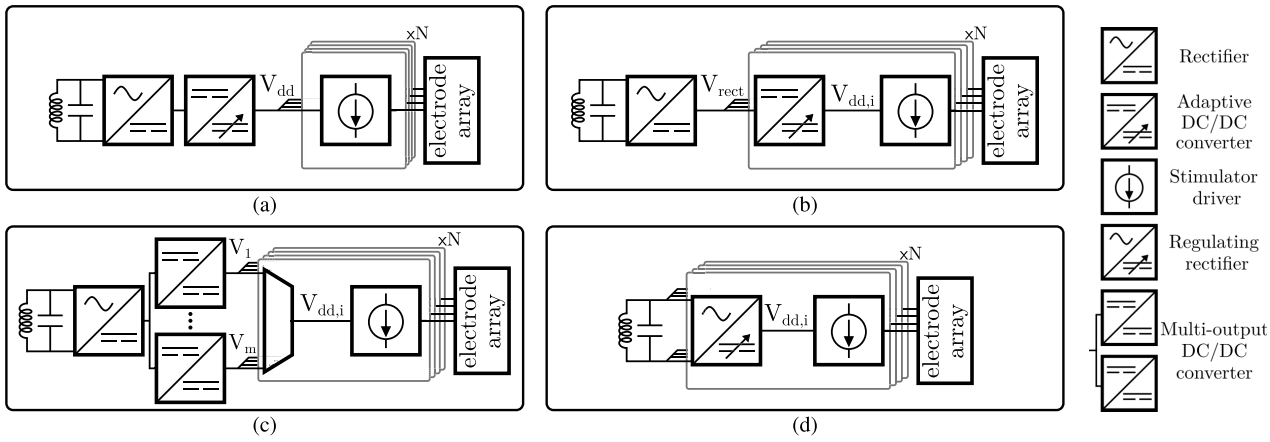

Fig. 2. Overview of power management strategies for adaptive voltage regulation in multichannel stimulator systems with a modular architecture. Each module contains at least an output driver that can connect to one or more electrodes and can have more local circuitry. (a) Global singular voltage regulation, using the same V_{dd} for all modules; (b) Parallel voltage regulation on a local scale, using local variable DC/DC converters in each module; (c) Parallel voltage regulation on a global scale, using a multi-output DC/DC converter on the system level and a multiplexer in each module to select the appropriate voltage level; (d) Proposed strategy using local regulating rectifiers in each module.

Given the limitations of the conventional fixed voltage supply, several approaches for scalable voltage supplies have been proposed in the literature to reduce the losses at the output driver. These approaches can be categorized into three groups: global singular voltage regulation, parallel voltage regulation on a local scale, and parallel voltage regulation on a global scale. The first group uses a single scalable voltage supply for the whole system (Fig. 2a), often implemented by reducing the transmitted power signal [14] or by an adaptive DC/DC converter [15], [16], [17], [18], [19], [20]. However, since all channels share the same supply, the output voltage must accommodate the worst-case channel. As a result, most channels still operate inefficiently, and the overall improvement compared to a fixed supply is minimal [21]. Consequently, channel-specific voltage scaling is required to improve the efficiency of large-scale multichannel systems. In the second group, the adaptive DC/DC converter is placed at the local scale of the output drivers (Fig. 2b). In [22], each stimulator output integrates a dedicated charge pump to dynamically adjust the supply voltage. However, the number of available voltage steps is typically limited, which restricts efficiency improvements [21]. Increasing the resolution requires additional capacitors per step, and because these converters are implemented per channel, this results in substantial area overhead and limits scalability. The third group reduces the area overhead by implementing a parallel DC/DC converter on a global scale (Fig. 2c) [23], [24], [25], [26], [27], [28], [29]. In [23], [24], [25], [26], [27], and [28], a multi-output DC/DC converter generates several voltage supply rails that are distributed to all channels, and each output driver selects a rail through a multiplexer (MUX). In this approach, the area of the DC/DC converter has less impact on the overall system area. However, the resolution of the voltage steps remains limited, which restricts the achievable efficiency improvement [21]. Increasing the number of rails requires larger MUX structures, which can add substantial area overhead depending on their implementation. For example, in [26] the six-level MUX accounts for about 25 % of the pixel area, while in [23] four 3:1 MUXes occupy nearly twice the area (2.5 mm^2) of the corresponding four-channel stimulation drivers (1.4 mm^2).

In addition to these trade-offs, most implementations also rely on multiple conversion stages to achieve the scaled output voltage. This leads to cascaded power losses and low overall power efficiency. To avoid cascaded losses, several single-stage regulating rectifier topologies have been proposed [30], [31], [32], [33]. This approach commonly uses a phase-controlled active rectifier to regulate the output voltage. A disadvantage of these implementations is that they are designed to scale the global voltage supply. As a result, a large output filter capacitor is used, limiting the design's scalability and the speed of the voltage regulation [31]. Moreover, the required output voltage is unknown since the channel impedance and current can vary widely. Therefore, an additional compliance monitor will be needed to select the appropriate reference voltage for each channel, which increases the power consumption and area of each channel.

To address these challenges, we present a channel-specific autonomous output supply scaling system. By distributing the received AC power signal across channels and performing on-channel regulated rectification, each stimulation channel automatically adapts its local supply voltage based on the instantaneous load conditions, without requiring explicit compliance monitoring or centralized voltage control. This single-step power conversion avoids cascaded losses associated with multi-stage regulation and continuously matches the output supply to the instantaneous requirements of the load impedance and stimulation current. As a result, the proposed architecture achieves high power efficiency at the output driver across a wide range of conditions. Compared to existing regulating rectifier approaches used in multichannel stimulation systems, the proposed design also eliminates the need for large output capacitors, external reference voltages, or compliance monitors, enabling fast, precise, and area-efficient voltage adaptation at the individual channel level.

This work expands on a previously presented conference paper [1] with an extension on the design methodology and the inclusion of experimental measurement results. The paper is organized as follows. Sections II and III describe the system architecture and circuit design of the proposed system. In Section IV, we present measurement results and in vitro validation of the presented ASIC. The results are discussed in Section V, and Section VI concludes the paper.

II. System Architecture

The proposed power management strategy is illustrated in Fig. 3 for a system comprising N stimulation modules. At the

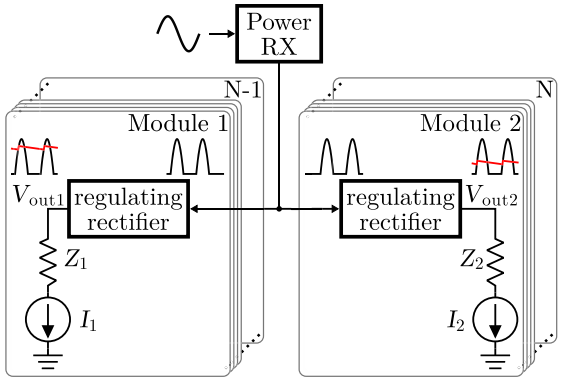

Fig. 3. The proposed power management strategy uses a modular architecture with N modules, each containing local regulating rectifier circuits. Both phases of the incoming AC signal are used by distributing them to the different modules.

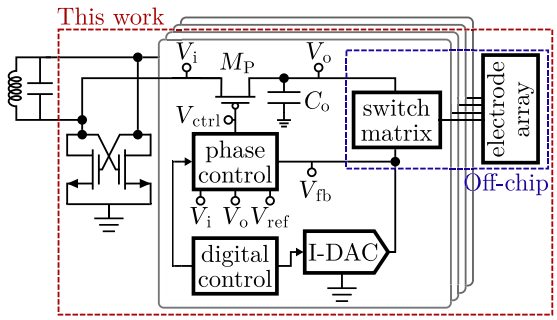

Fig. 4. Proposed system architecture. The regulating rectifier is implemented as a phase-controlled rectifier switch (M_p), in which the phase control is based on the headroom voltage of the current DAC (V_{fb}). An off-chip switch matrix connects the output current to an electrode array. Figure modified from [1].

global level, the incoming AC power signal is converted into two half-bridge rectified power signals, and distributed over the odd and even modules. Each module has a local regulating rectifier that regulates the channel-specific output voltage. The output voltage is automatically matched to the required level for the load, minimizing the energy losses at the output driver and improving the power efficiency.

To implement this automatic output voltage scaling, we propose the architecture of each module illustrated in Fig. 4. Each module contains a configurable current DAC (I-DAC), a switch matrix, digital control logic, and a local regulating rectifier consisting of a phase-controlled rectifier switch (M_p) and an output capacitor (C_o). A bipolar current output is generated between V_o and V_{fb}, and the switch matrix is used to direct this current to multiple electrodes. Furthermore, the switch matrix is used to create biphasic stimulation pulses.

On the system level, the incoming power is assumed to be received by means of an inductive link. However, the proposed approach would work with other (wireless) sources that produce an AC power signal (i.e., ultrasound, capacitive, or RF). The incoming AC power signal is split into two half-wave rectified sine waves using a cross-coupled NMOS pair at the input. Due to the variance in the output voltage requirements, the parallel regulating rectifiers will extract power from the input signal at different voltage levels. Moreover, although full-wave rectification would also be possible, using only half of the input signal at the input of the rectifiers omits copies of the control circuits that would be needed to rectify the other half of the input [31]. This simplifies the local control

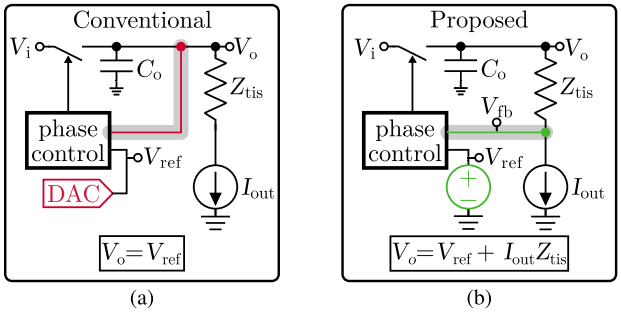

Fig. 5. Comparison of (a) the conventional regulating rectifier structure and (b) the proposed implementation.

and reduces the area of the rectifiers. Since multiple modules operate in parallel, the entire input signal will still be used.

Existing regulating rectifier designs, such as those in [30] and [31], have several drawbacks. In these designs, the output voltage V_o is used as the input of the controller. This approach typically requires an attenuator at the input of the controller, where a voltage divider with an impedance in the MΩ range is needed to minimize static power losses. However, this increases the overall circuit area. Additionally, in the conventional approach, the output voltage V_o is directly regulated by the reference voltage, resulting in discrete regulation steps. This can lead to overhead losses if $V_o > V_{load}$. Furthermore, due to the nonlinear and temporally variable nature of the load [13], the required output voltage at each channel is unknown, necessitating a compliance monitor to scale V_o as needed. Another drawback is that the conventional approach requires a separate DAC per channel to produce channel-specific output voltages, increasing the system's complexity and cost.

The proposed implementation addresses these limitations with a novel active phase controller. As shown in Fig. 5, the proposed design uses the headroom voltage of the current source, V_{fb}, as the control node in the active rectifier, which has several advantages. First, V_{fb} can be designed to be in the range of 100 to 200 mV, allowing direct detection by a low-voltage amplifier without requiring a high-impedance voltage divider, thereby reducing circuit area. Second, the proposed design regulates the output voltage to $V_o = V_{ref} + I_{out} Z_{tis}$, enabling the output to automatically track the required voltage. This minimizes overhead losses and removes the need for a compliance monitor. Finally, V_{ref} is the same for all modules in the system, allowing a single reference voltage to be used while producing separate output voltages at each channel. This significantly reduces the complexity compared to the conventional approach, which requires a separate DAC per channel. A comparison of the proposed implementation with conventional regulating rectifiers is shown in Fig. 5.

III. Circuit Design

A system with two parallel modules has been designed to demonstrate the proposed architecture (Fig. 4). In each module, a current is generated that flows from V_o to V_{fb}, corresponding to the nodes where the load impedance is connected. An off-chip switch matrix allows biphasic current pulses to be sent through an external electrode array. This section describes the design of the on-chip module, where system-level specifications are first derived, followed by the design of the sub-blocks. Regarding the system-level specifications, the circuit is designed to operate from a wirelessly received power signal with a central frequency of 13.56 MHz, commonly

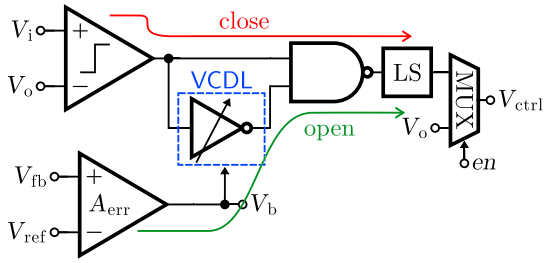

Fig. 6. Phase controller design. Figure modified from [1].

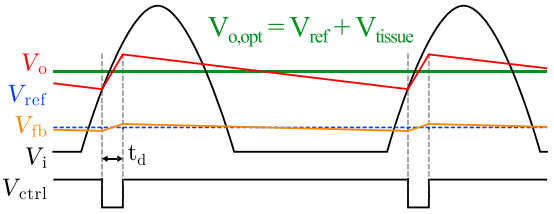

Fig. 7. Timing diagram of the signals in steady state. Figure modified from [1].

used in biomedical implants. Furthermore, the reconfigurable current DAC is specified with 4 bits of resolution between 20μA and 95μA, which corresponds to typical threshold values often reported in intracortical visual prostheses [2]. The DAC is binary coded with wide-swing cascode current sources in each branch, with the LSB branch sinking 5 μA. Additionally, there is a parallel branch of 20 μA to offset the current range. Moreover, C_o has a value of 40 pF, resulting in a ripple voltage ΔV_o of 175 mV at the maximum output current of 95 μA. Since the current is regulated by the I-DAC, the ripple voltage is allowed to be larger than for applications requiring a steady voltage supply. The size of C_o is a fundamental design trade-off with the allowed ripple voltage. Finally, the maximum voltage allowed at the output is 5 V such that 5 V transistors can be used, which allows for load impedances in the range of tens of kΩ, matching the impedances of Utah electrode arrays commonly used in cortical stimulation applications [2] [34]. A detailed description of the sub-blocks and their design considerations are given below.

A. Phase Controller

The design of the phase controller is depicted in Fig. 6. The rectifier switch (M_p in Fig. 4) is controlled by two loops. The first loop (indicated by the red arrow in Fig. 6), consisting of a comparator and a NAND gate, closes M_p at the cross-over point between V_o and V_i in each period. The conduction time of the pulse, t_d, is controlled by the second loop (indicated by the green arrow in Fig. 6), consisting of an error amplifier, a voltage-controlled delay line (VCDL) and the NAND gate. The error amplifier compares V_{fb} to the desired reference voltage V_{ref} and adjusts the delay time accordingly with the bias voltage of the VCDL, V_b. A timing diagram of the (ideal) signals in the controller at steady state is shown in Fig. 7. When the output driver is inactive (output current disabled), M_p is configured as a diode-connected transistor acting as a passive rectifier to ensure sufficient supply voltage at the start of a stimulation pulse. Most of the components in the phase controller are operating from a 1.8 V supply to reduce power consumption. Therefore, a level shifter (LS) is needed between the control logic and the rectifier switch. The LS and MUX are part of the rectifier switch driver described in Section III-E.

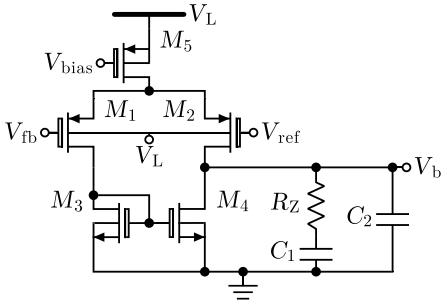

Fig. 8. Implementation of the error amplifier.

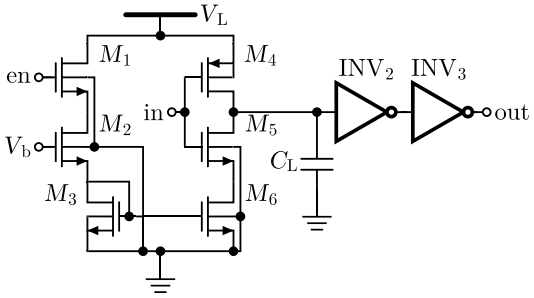

Fig. 9. Implementation of the voltage-controlled delay line.

B. Error Amplifier

The error amplifier is implemented as a 5T-OTA followed by a frequency compensation network with two poles and one zero, as depicted in Fig. 8. When the rectifier is disabled, the amplifier is also disabled. However, the input at V_{fb} can reach 5 V, and thus the amplifier is implemented using 5 V devices to avoid device breakdown. On the other hand, when the rectifier and the amplifier are enabled, the input at V_{fb} is in the range of V_{ref}, which is typically 200 mV. Therefore, the voltage supply of the amplifier is 1.8 V (V_L) to reduce its power consumption. The input pair is implemented using PMOS devices as the input voltage in active mode will be close to 0 V. At the start of a current pulse, the output of the amplifier will be saturated to V_L, which gives the shortest t_d. In turn, the filter capacitor (C_o in Fig. 4) is discharged by the DAC current, and V_{fb} drops until the amplifier gets out of saturation. At that point, the gain of the feedback loop restores to control the voltage to the desired level. Since the phase controller is a switched feedback loop, the output of the error amplifier needs frequency compensation to ensure loop stability. For stability, the frequency compensation has to dominate the overall loop gain. The design procedure of the compensation components is discussed in Section III-F.

C. Voltage-Controlled Delay Line

The VCDL is implemented as a single-sided current-starved inverter, depicted in Fig. 9. The delay of the element needs to be controlled only at the output transition from logic high to low. The element is reset at the output transition from low to high; hence, its transition time is irrelevant to the circuit's operation.

The output delay can be calculated using Eq. (1), assuming that C_L is charged to V_L at the beginning of the pulse and that the tipping point of INV$_2$ is at half the supply voltage, $V_L/2$. I_{M6} is regulated by V_b through M_2 and M_3.

$$t_d = \frac{V_L}{2}\frac{C_L}{I_{M6}} \tag{1}$$

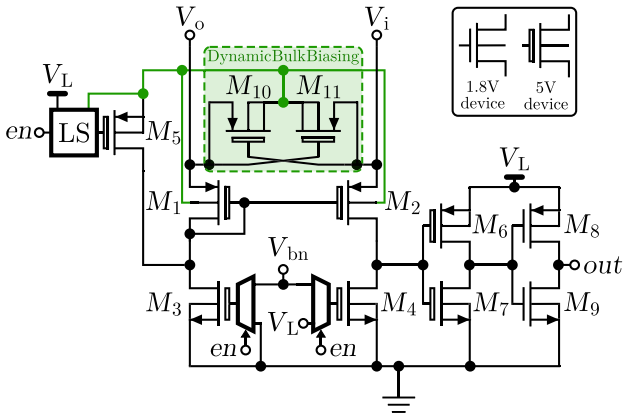

Fig. 10. Comparator design. Figure modified from [1].

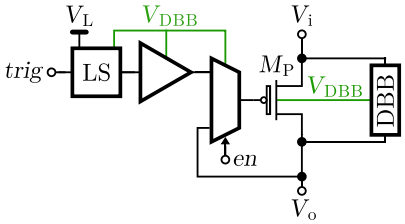

Fig. 11. Driver circuit for the rectifier switch.

In the implementation, C_L is created by sizing INV_2 to get a large input capacitance. This improves the drive strength of INV_2, minimizing the additional (overhead) delay. The simulated delay time of the VCDL is between 33 ns and 800 ps for $V_{th} \leq V_b \leq 1.8$ V. The circuit produces an infinite delay when $V_b < V_{th}$. However, in that case, the comparator turns the rectifier switch off when V_i drops below V_o.

D. Comparator

The design of the comparator is shown in Fig. 10. A common-gate input pair is used to allow for inputs above the supply rail of V_L. This omits the need for a steady, high-voltage supply for correct circuit operation. Using a dynamic bulk-biasing (DBB) circuit, the bulk terminals of the input pair are biased to the highest voltage of the two inputs. A single-bit multiplexer is used at the gates of M_3 and M_4, controlled by the enable signal. When the comparator is enabled, the gates are connected to the bias voltage V_{bn}, which is generated using an (external) bias current and a current mirror. When disabled, V_{gs} of M_3 is 0 V, and V_{gs} of M_4 is V_L. Furthermore, M_5 is used to pull up the gates of M_1 and M_2 when the comparator is disabled. This way, the comparator uses no static power when disabled. The buffer at the output ($M_6 - M_9$) is used to convert the output voltage of the comparator to the low-voltage domain for the following logic gates.

E. Rectifier Switch Driver

The rectifier switch, M_p, is a PMOS device with a size of 10 μm/500 nm (W/L). The driver circuit for this switch is shown in Fig. 11. The bulk of M_p is biased using a DBB circuit. A MUX controls the gate of M_p to select active or passive rectification mode. When the feedback loop is disabled, the MUX connects the gate of M_p to the output, creating a passive rectifier. Contrarily, when the rectifier is enabled, the gate of M_p is actively controlled by the feedback loop. The pulse signal *trig* is level-shifted to the appropriate voltage level and buffered to drive M_p. The driving voltage for the output of the level shifter, the buffer, and the MUX are also created using a (separate) DBB circuit, which selects the highest voltage between V_i and V_o.

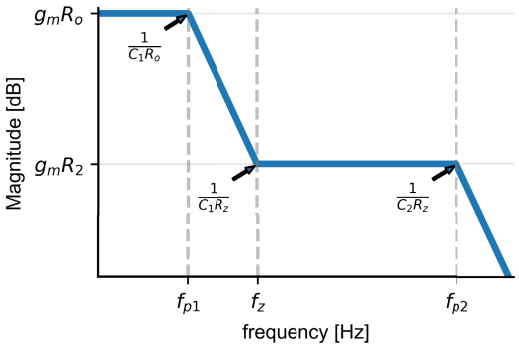

Fig. 12. Bode magnitude plot of the transfer function of the error amplifier with frequency compensation (Fig. 8). R_o and g_m are the output resistance and transconductance of the amplifier, respectively.

F. Design of the Feedback Loop

The loop gain of the phase controller is calculated by Eq. (2), where A_{err} is the gain of the error amplifier, A_{vcdl} the gain of the VCDL, A_{sw} the gain of the rectifier switch, and A_{out} the gain from V_o to V_{fb} (which will be <1). The frequency compensation components at the error amplifier are designed to be dominant in the total loop transfer.

$$A_L = A_{err}A_{vcdl}A_{sw}A_{out} \tag{2}$$

The magnitude of the transfer function of the error amplifier with frequency compensation is depicted in Fig. 12. It can be seen that the compensation adds two poles and one zero to the transfer function, where the dominant pole is created by the output resistance of the amplifier, R_o, and capacitor C_1. To boost the phase margin, resistor R_z is added to create a zero at $f_z = 1/(2\pi R_z C_1)$. The non-dominant pole at $f_{p2} = 1/(2\pi R_z C_2)$ filters out high-frequency signals. The phase controller is designed to operate at a switching frequency, f_{sw}, of 13.56 MHz. Since the cross-over frequency f_c of the open-loop gain (also known as the unity-gain frequency) should be lower than $f_{sw}/2$ to ensure stability, a design target of $f_c = f_{sw}/10$ is chosen to provide sufficient margin. Several design trade-offs can be derived from the Bode magnitude plot in Fig. 12. First, a high DC gain is desired to minimize the steady-state error. On the other hand, low power consumption is required, which limits the DC gain that can be achieved. Furthermore, the wide operating range of the circuit will cause variance in the (non-linear) input-output relations of the other sub-blocks. Separating the zero and the non-dominant pole makes the increase of the phase margin effective over broad operating conditions, which can be achieved by increasing C_1. However, the area of C_1 should be constrained for the scalability of the circuit. Taking into account the trade-offs above, the amplifier was designed to have low static power consumption and a small area for scalability. The implemented amplifier consumes 1 μA from a 1.8 V supply, with a DC open-loop gain of 33 dB. The compensation components are chosen as $C_1 = 3.2$ pF, $C_2 = 160$ fF, and $R_z = 100$ kΩ.

Regarding the VCDL, the transfer function is given by:

$$A_{\text{vcdl}} = \frac{\mathrm{d}t_{\text{d}}}{\mathrm{d}V_{\text{b}}}. \tag{3}$$

Since an increase in V_{b} will increase the discharge current and thus decrease t_{d}, A_{vcdl} is negative by design. Furthermore, A_{sw} and A_{out} are both positive. Therefore, A_{err} is designed to be positive to achieve an overall negative loop gain. The transfer function of the VCDL has two asymptotes since the delay goes to infinity when $V_{\text{b}} < V_{\text{th}}$, and approaches the minimum delay for V_{b} close to 1.8 V. Therefore, the gain of this block can vary over a wide range depending on the operating point of the overall circuit.

The next component in the architecture is the rectifier switch, for which the transfer function can be obtained from:

$$A_{\text{sw}} = \frac{\mathrm{d}V_{\text{o}}}{\mathrm{d}t_{\text{d}}}. \tag{4}$$

The output current I_{DAC} determines the discharge rate of the output capacitor and, thus, how much charge needs to be transferred in t_{d}. When conducting, the charging current can be calculated using

$$I_{\text{in}} = \frac{V_{\text{i}} - V_{\text{o}}}{R_{\text{sw,on}}}. \tag{5}$$

where $R_{\text{sw,on}}$ is the on-resistance of M_{p}. The DC gain of this stage depends on many variables, such as the slope of the input signal, the size of C_{o}, the output current I_{DAC}, and the on-resistance of the rectifier switch. Furthermore, a pole is introduced by the low-pass filter at $f_{\text{p,sw}} = D/(2\pi R_{\text{sw,on}} C_{\text{o}})$, where D is the duty cycle of the rectifier switch. To reduce conduction losses, the on-resistance of the rectifier switch should be low. However, this also reduces D and the location of p_{sw}. Therefore, the sizing of the rectifier switch should be done carefully to prevent p_{sw} from becoming dominant. Finally, the transfer function of the output stage is given by $A_{\text{out}} = V_{\text{ref}}/V_{\text{o}}$. Again, the attenuation depends on the impedance and current at the output. When V_{o} is close to V_{ref}, A_{out} approaches 1, and at the maximum output voltage $A_{\text{out}} = V_{\text{ref}}/5$.

The total loop gain of the designed circuit is simulated for all possible output current amplitudes (20 to 95μ A) and a load resistance ranging from 20kΩ to 70kΩ. The resulting loop gain magnitude and phase are shown in Fig. 13. The phase margin ranges between 52° and 74° for the simulated conditions. When the output is disabled, the loop gain is zero since the output of the OTA saturates. Therefore, the beginning of a current pulse causes a large step, and stability should be confirmed using transient simulations. The transient response to a 35μs current pulse at the output was simulated for the same range of output current amplitudes and load resistances. The results, shown in Fig. 14, show that all conditions result in a stable voltage at V_{fb}. For low output currents, the transient response is slower because the output current needs to discharge C_0, while a minimum amount of charge is deposited each cycle due to the minimum pulse width that the feedback loop can produce.

IV. Simulations and Experimental Validation

The circuit was implemented in a 180 nm CMOS TSMC process. The chip micrograph is shown in Fig. 15. The design has an active area of 800 $\mu m \times 126 \mu m$ (excluding pads) and a channel area of 368 $\mu m \times 126 \mu m$ (of which 52 % is occupied by C_{o}). The measurement setup is illustrated in Fig. 16. A 10 V_{pp},

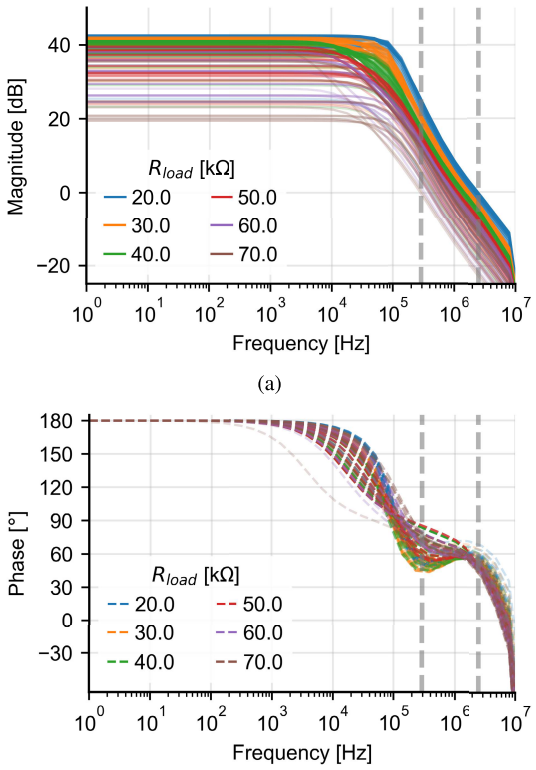

Fig. 13. Schematic simulations of loop gain magnitude (a) and phase (b) of the implemented regulator for a wide range of load conditions: R_{load} = 20 kΩ to 70 kΩ and I_{load} = 20 μA to 95 μA.[a] An increasing I_{load} is indicated as an increasing opacity of the traces.

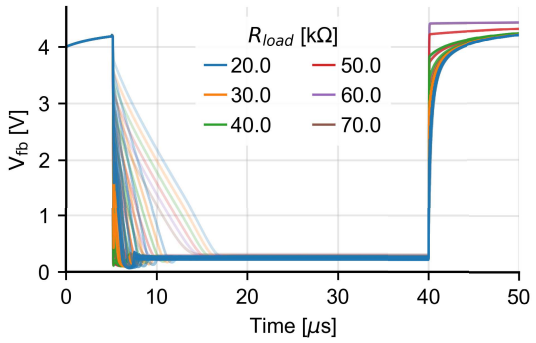

Fig. 14. Schematic simulation of the transient response for a stimulation pulse with a duration of 35 μs starting at t = 5 μs, while sweeping the conditions: R_{load} = 20 kΩ to 70 kΩ and I_{load} = 20 μA to 95 μA. The opacity of the traces indicates I_{load}, where high current equals high opacity.

13.56 MHz sine wave is generated using a signal generator (*Rigol dg4202*) and ac-coupled to the input of the chip using an RF 1:1 transformer (COILCRAFT SWB1010). The low-voltage supply V_{L} (1.8 V) is provided to the chip using a bench-top DC supply (*GW Instek GPP-4323*). For some measurements, an external H-bridge, created using analog switches (*ADG1211*), was used to generate biphasic current pulses. Furthermore, the necessary bias currents and reference voltage V_{ref} are generated on a PCB using commercially available ICs. In the final application, the low-voltage supply

[a]If the required output voltage, V_{o}, exceeds the maximum output voltage the circuit can provide, the output is no longer regulated, and the loop gain deteriorates. These output conditions are not included in the figure.

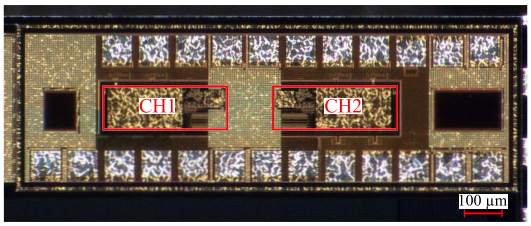

Fig. 15. Micrograph of the implemented chip with the two channels indicated by the red boxes.

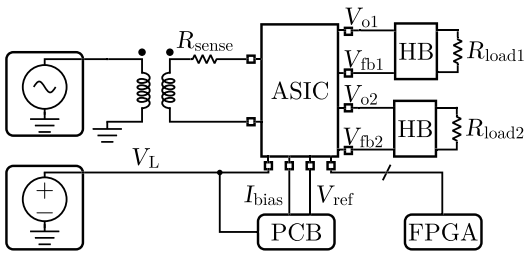

Fig. 16. Illustration of the measurement setup. The input signal is generated from a signal generator and ac-coupled to the chip using a 1:1 RF transformer. The 1.8 V voltage supply, bias currents, and reference voltage are supplied externally. The output nodes of both channels are connected to the loads using external H-bridges (HB). The ASIC is controlled using an FPGA module. R_{sense} is used to measure the input power.

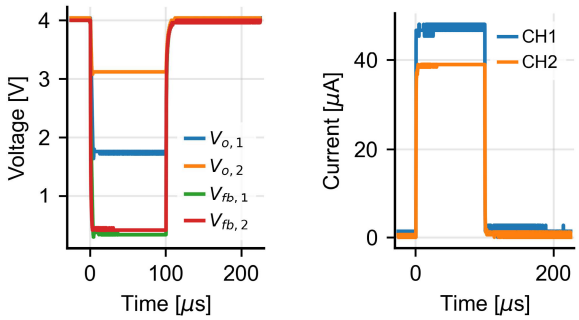

Fig. 17. Example of measured output voltages (a) for load impedances of 30kΩ and 70kΩ, and current amplitudes of 50μ A and 40μ A on Channels 1 and 2, respectively. (b) Effective measured load current.

could be generated from a separate rectifier in parallel with the proposed voltage regulators, and the bias currents should be generated on-chip. Finally, the control signals for the ASIC are created using an FPGA module (Digilent CMOD S7). In all presented measurements, V_{ref} is set to 250 mV.

A. Output Pulses

To demonstrate the operation of the circuit, the two channels are configured for different current amplitudes and load impedances. Both channels produce a current pulse with a duration of 100μ s. The amplitude is configured to 50μ A and 40μ A for Channels 1 and 2, respectively, and a resistive load of 30kΩ and 70kΩ is applied at the outputs. The resulting output voltages are shown in Fig. 17a. It can be seen that for both channels, V_{fb} is regulated to V_{ref}, while the output voltages $V_{o,1}$ and $V_{o,2}$, differ for both channels, depending on the output conditions. The effective output currents, shown in Fig. 17b, are found by subtracting these voltages and dividing them by the load impedance. For these output conditions, the error on the load current compared to the configured current is −2.8μ A(6%) for Channel 1 and −1.1μ A(3%) for Channel 2.

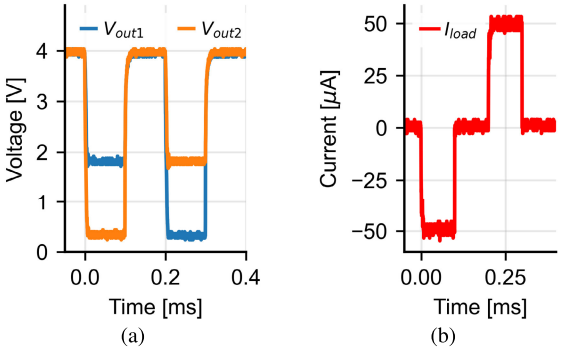

Fig. 18. (a) Measured voltages at the output of the H-bridge for a biphasic current pulse of 50μ A on a 30kΩ load. (b) Effective current as seen by the load.

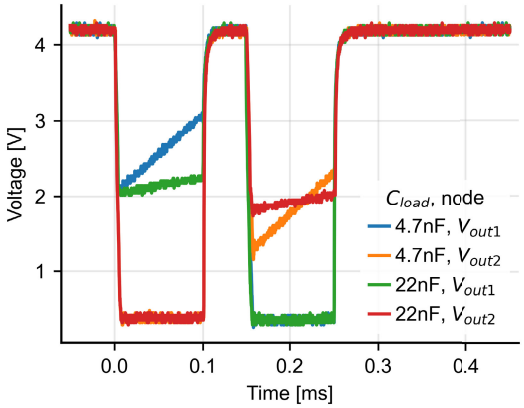

Fig. 19. Measured output voltages at the two H-bridge output nodes for a 50 μA biphasic stimulation pulse applied to a series RC load. Two load conditions are shown: R_{load}= 50 kΩ with C_{load}= 4.7 nF and C_{load} = 22 nF, respectively.

Next, an external H-bridge is used to create biphasic current pulses. Figure 18a shows the measured voltages at the two output nodes of the H-bridge for a biphasic current pulse of 50 μA on a 30 kΩ resistive load. The resulting load current is depicted in Fig. 18b. To further validate the behavior under more realistic load conditions, measurements were also performed using an RC load, modeling the electrode–electrolyte interface as a series resistor and capacitor. Figure 19 shows the measured output voltages for a 50 μA biphasic pulse applied to two RC loads: R_{load} = 50 kΩ with C_{load} = 4.7 nF and C_{load} = 22 nF, respectively. The resistor value was chosen within the typical impedance range of Utah electrode arrays [2], [34], while the capacitor values illustrate two representative capacitive behaviors observed in *in-vitro* measurements. The larger value (22 nF) reflects the slope observed in our electrode measurements (Fig. 29), whereas the smaller value (4.7 nF) represents a more demanding case with a steeper capacitive slope, demonstrating that the circuit maintains stable regulation even under such conditions. In both cases, the supply voltage adapts to the capacitive charging behavior of the load.

B. Varying Output Conditions

To characterize the output of the chip for varying load conditions, one of the channels is configured to produce a constant output current, as shown in Fig. 20. It can be seen that the maximum current is limited for larger load impedances,

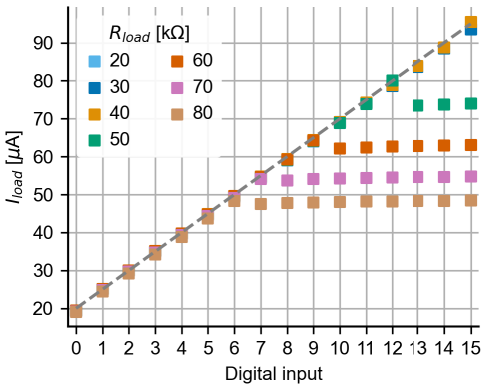

Fig. 20. Measured output current vs DAC configuration bits.

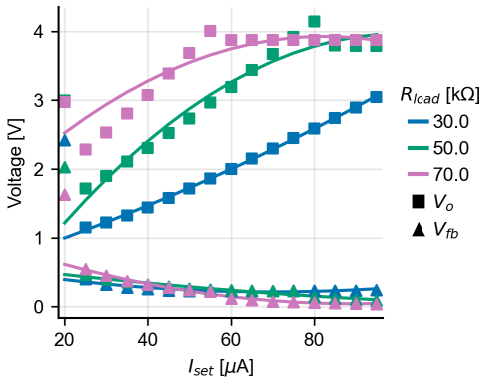

Fig. 21. Measured output voltages for varying load conditions. Markers indicate measured data; solid lines represent quadratic fits to the data.

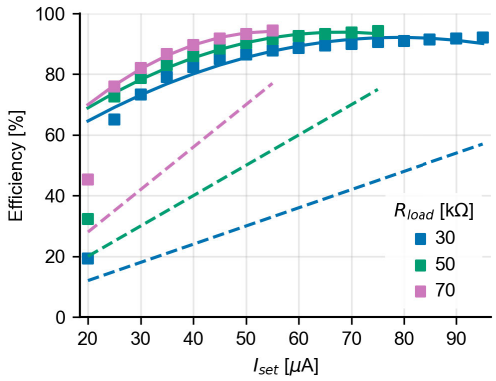

Fig. 22. Measured power efficiency (solid) at the output for three load impedances compared to the efficiency of a fixed 5 V voltage supply (dashed). Markers indicate measured data; solid lines represent quadratic fits to the data.

which is due to the maximum output voltage that the circuit can produce (around 4.2 V). The measured output voltages for three different load impedances are depicted in Fig. 21, where I_{set} is the configuration setting of the I-DAC. The measurements show a wide range of regulated output voltages, depending on the current and load impedance at the output. The broad operating conditions allow for accurate tracking of the required output voltage, resulting in a high power efficiency at the output. It is evident that V_{fb} is not regulated as desired for low-current output conditions, which is due to the minimum pulse width that the switch driver could produce. When the output current is small, the discharge rate of C_{o} is low, and the charge delivered to C_{o} for minimum t_{d} is too high to properly discharge the node to V_{ref}. As a result, V_{o} settles to about 3 V for all loads, and V_{fb} becomes $V_{\text{o}} - I_{\text{set}}R_{\text{load}}$. Consequently, V_{fb} is closer to its desired value for larger load impedances. This limitation could be mitigated by reducing the minimum t_{d} or by skipping pulses at low current conditions. Furthermore, it can also be seen that the maximum output voltage of the circuit is only around 4 V for a 5 V input signal. This is due to the large on-resistance of the implemented rectifier switch. The limitation on the maximum output voltage causes the deviation of I_{load} from its intended value in Fig. 20. To improve the maximum VCR of the circuit, the sizing of M_{p} should be improved.

For the following measurements, the results for load conditions where the circuit can not produce the required output voltage are discarded.

C. Power Efficiency

For the power measurements, the transformer in Fig. 16 is omitted, and a 5V half-sine signal is directly applied from the signal generator to the input of the chip. Each load condition is repeated 20 times in a random order, and the measured quantities are averaged. The efficiency at the output, calculated using Eq. (6), is shown in Fig. 22.

$$\eta_{\text{out}} = \frac{P_{\text{load}}}{P_{\text{out}}} \tag{6}$$

As a reference, the output efficiency for a fixed voltage supply of 5 V is also plotted in the same figure. It can be seen that the scaled voltage supply improves the efficiency at the output for all load conditions. The low efficiency for an output current of 20 μA is due to the effect that V_{fb} is not properly regulated, as explained in the previous section. This results in excessive voltage drop, and thus power dissipation, over the current source. A sense resistor of 47 Ω is used in series with the input to measure the input power. Parasitics on the PCB introduce a large offset in the measured power levels since the power to the load is small in this application. To compensate for this offset, the power at the input for all conditions is measured twice: once with the output of the chip enabled and once with the output disabled. The power measurements are obtained by subtracting P_{off} from P_{on} for a wide range of load conditions, with the measured results presented in Fig. 23. The total efficiency of the circuit is calculated using Eq. (7) and depicted in Fig. 24.

$$\eta_{\text{total}} = \frac{P_{\text{load}}}{P_{\text{in}}} \tag{7}$$

It can be seen that the overall efficiency is relatively low compared to the output efficiency shown in Fig. 22, which is mainly due to conduction losses in M_{p}. In Section V, we discuss several opportunities to improve the overall efficiency.

D. Efficiency in Multichannel Applications

To see how the measured efficiencies translate to a multichannel application (intracortical visual prosthesis), we apply the analysis presented in [21] to this system. For this analysis, we used the experimental data from [2] and [3] and compared the efficiencies for the conventional fixed-voltage supply, a stepped-voltage supply, and the proposed work. Details of the analysis are provided in Appendix I. The resulting efficiencies are shown in Fig. 25. The proposed work shows a median

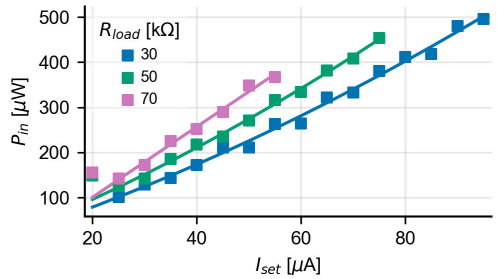

Fig. 23. Measured input power for a wide range of load impedances and output currents. Markers indicate measured data; solid lines represent quadratic fits to the data.

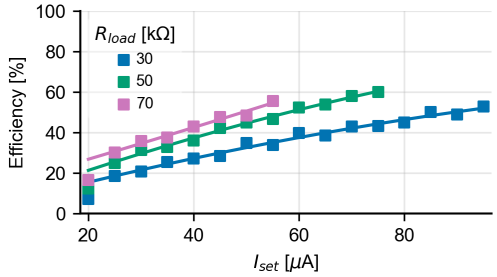

Fig. 24. Measured overall efficiency of the rectifier for three load impedances. Markers indicate measured data; solid lines represent quadratic fits to the data.

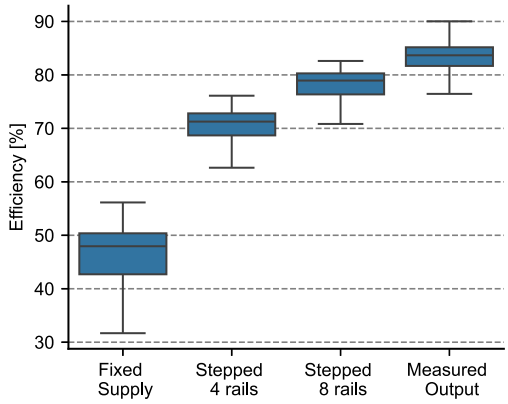

Fig. 25. Performance comparison of the (output) efficiency based on experimental data from intracortical visual prosthesis [2], [3], using the analysis method presented in [21].

efficiency of 84 % on this data, representing an improvement of 74 %, 17 %, and 6 % compared to a fixed supply and stepped voltage supplies with 4 and 8 steps, respectively.

E. Time Division Multiplexing

Time-division multiplexing (TDM) can be employed in electrical stimulation circuits to enable efficient resource sharing by utilizing a single stimulation driver across multiple channels [35]. However, existing multiplexed implementations overlook the need for precise voltage scaling for varying load conditions. Instead, they rely on fixed voltage supplies or regulating rectifiers with large output capacitors [35], [36], [37], [38], [39], [40]. Fixed supply implementations lead to low power efficiency (Fig. 25), while large output capacitors in regulating rectifiers limit the speed of voltage regulation, making them unsuitable for applications requiring rapid switching

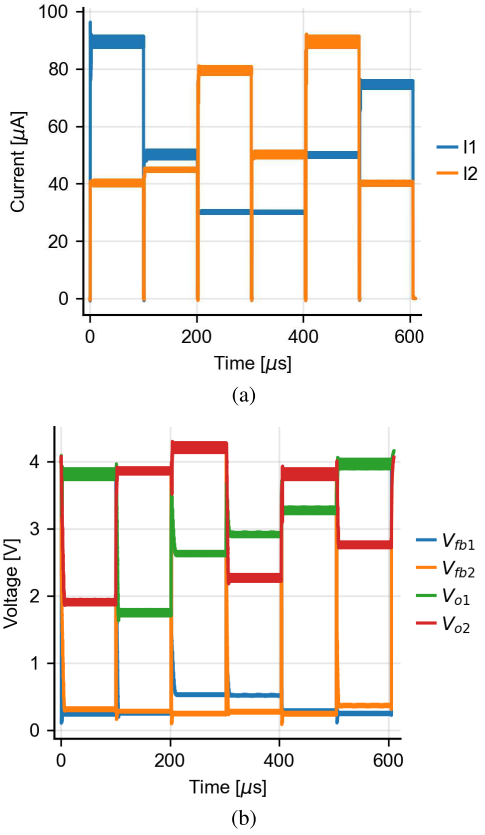

Fig. 26. Post-layout simulation of (a) output current and (b) output voltages during time-division multiplexing of the proposed circuit. Six current pulses of 100 μs each are applied consecutively with varying load impedance and current amplitude. An interpulse delay of 1 μs is used to configure the output conditions. For Channel 1, the current and load impedance sequences are $90, 50, 30, 30, 50,$ and 70 μA and $40, 30, 70, 80, 60,$ and 50 kΩ, respectively, while for Channel 2 they are $40, 45, 80, 50, 90,$ and 40 μA and $40, 80, 50, 40, 40,$ and 60 kΩ.

between channels with differing load impedances and current amplitudes. The proposed circuit overcomes these limitations by enabling scalable TDM for systems with a large number of electrodes, even when load conditions differ significantly between channels. The small output capacitor in this design allows for rapid voltage regulation and ensures seamless transitions between channels. Furthermore, the circuit automatically adjusts to changing load conditions, maintaining appropriate output voltage. In contrast, implementations with large output capacitors in regulating rectifiers exhibit slower response times, which hinder their ability to efficiently switch between channels. The flexibility of the proposed circuit for TDM is demonstrated via post-layout simulations of six consecutive current pulses, each lasting 100 μs, applied to two channels under varying output conditions (load impedance and current amplitude), as illustrated in Fig. 26. An interpulse delay of 1 μs is used to reconfigure the output current and to switch the load impedance. For channel one, the current and load impedance sequences are $90, 50, 30, 30, 50,$ and 70 μA and $40, 30, 70, 80, 60,$ and 50 kΩ, respectively. For channel two the corresponding sequences are $40, 45, 80, 50, 90,$ and 40 μA and $40, 80, 50, 40, 40,$ and 60 kΩ. These simulations highlight the circuit's ability to rapidly regulate the output voltage for each pulse, maintaining optimal power efficiency across diverse load conditions. The multiplexing frequency is limited by the duration of the stimulation pulses and the configuration

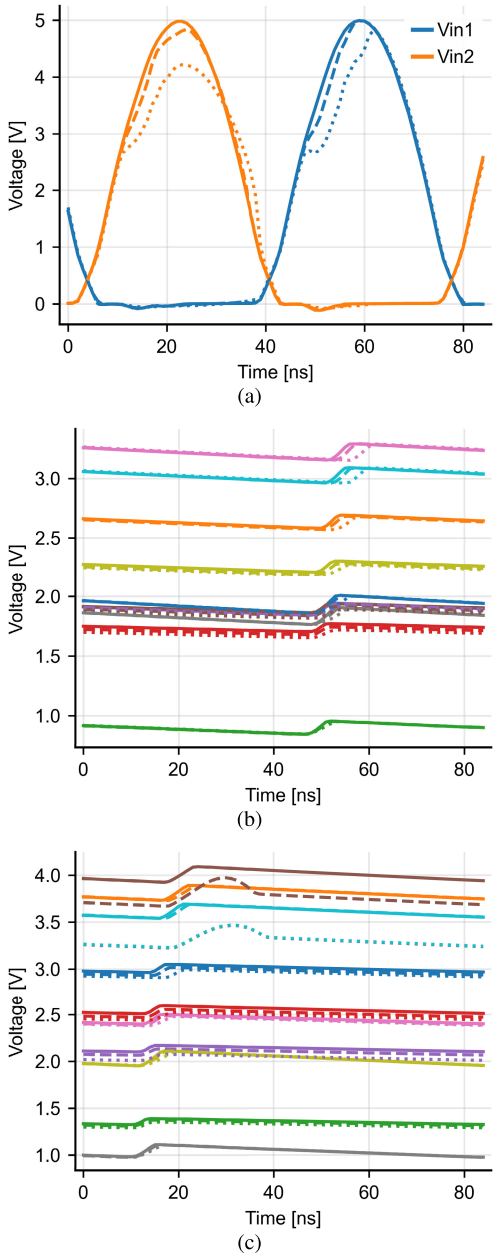

Fig. 27. Post-layout simulation results for a system with twenty parallel modules: (a) two half-wave rectified input voltages, each supplying ten modules; (b) regulated output voltages from modules powered by V_{in1}; (c) regulated output voltages from modules powered by V_{in2}. Linestyle indicates source resistance R_s (solid: 0 Ω, dashed: 50 Ω, dotted: 200 Ω), while color denotes the channel.

of the current source, of which the latter can be in the range of nanoseconds. Therefore, the TDM is effectively only limited by the pulse duration of each channel.

F. Scalability and Cross-Regulation Simulation

To evaluate potential interactions between multiple modules sharing the same input source, a system-level simulation was performed with twenty parallel modules. The input AC supply was modeled as an ideal sinusoidal source with an added series resistance R_s to emulate non-ideal source impedance. R_s was swept from 0 Ω to 200 Ω to investigate cross-regulation effects when multiple channels draw current simultaneously. For this simulation, the load impedance and stimulation current of each module were chosen randomly within the target operating range.

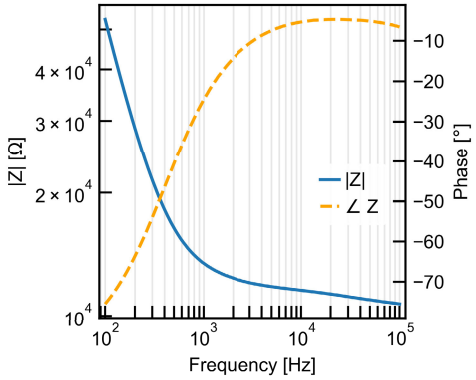

Fig. 28. Measured impedance magnitude and phase for the bipolar electrode pair in a PBS solution.

Figure 27 shows the post-layout simulated input waveform and representative regulated output voltages. As R_s increases, the input sinusoid exhibits increasing distortion due to the superposition of load currents from all modules. On the outputs supplied by V_{in1}, this distortion results primarily in a delay in the regulation response (Fig. 27b). In contrast, the outputs supplied by V_{in2} (Fig. 27c) show a limitation in the achievable regulated voltage when R_s becomes large.

The detailed design of the power-receiving LC tank was outside the scope of this work; however, this simulation provides important insight into the impact of source impedance on large-scale operation. It should be emphasized that distortion of the input signal would also occur in architectures with a single regulator driving all channels, and is therefore not a drawback specific to the proposed distributed rectifier implementation.

G. In Vitro Measurements

Finally, the chip is tested using custom-made flexible and conformable electrodes immersed in a phosphate-buffered saline (PBS) solution. The electrodes are Au-evaporated and functionalized with PEDOT:PSS. The contact pads have an area of 50 $\mu m \times 50\ \mu m$ with an inter-electrode distance of 950 μm. The output of the chip is connected to the electrodes in a bipolar configuration using the external H-bridge. First, the impedance of the electrodes is characterized using a Zurich Instruments MFIA digital impedance analyzer. The measured magnitude and phase of the impedance are shown in Fig. 28. The impedance at 1 kHz is approximately 15 kΩ. Next, biphasic current pulses of 50 μA and 95 μA are applied to the electrodes. The measured voltages at the output nodes are shown in Fig. 29a. The resulting load voltages, depicted in Fig. 29b, are obtained by subtracting these voltages. The measured load voltages are typical voltage transients for stimulation electrodes upon applying rectangular current pulses, where the ramp in the voltage is the effect of capacitance at the electrode-tissue interface that is charged by the stimulation current. These measurements show the capability of the circuit to follow a change in required output voltage.

H. Performance Comparison With Previous Work

Tables I and II summarize regulating-rectifier and multi-channel stimulator comparisons. Relative to prior regulating

TABLE I

COMPARISON AGAINST REGULATING RECTIFIER TOPOLOGIES

Work	2013 [30]	2017 [31]	2015 [33]	2024 [27]	This work
Technology (µm)	0.5	0.18 (SOI)	0.35	0.25	0.18
Resonant frequency (MHz)	2	144	13.56	2	13.56
Area/Channel (mm^2)	0.15	0.08	N/S	0.52	**0.046**
Max. output voltage (V)	4.6	0.8	3.6	4.5	5
Max. output current	2.48 mA	700 µA	N/S	22.5 mA	95uA
Output capacitor	N/S	1 nF	N/S	10 µF (off-chip)	**40 pF**
$PCE_{out,max}$	68 %	N/A	N/A	N/A	**95 %**
$PCE_{rect,max}$	87 %	65 %[1]	93 %	91 %[2]	64 %
Number of voltage steps	8	1 (fixed)	PWM-regulated	N/S	**Continuous**
Parallel output regulation	No	No	No	Yes	**Yes**
Scalability output channels	-	-	-	max. 6	**Unlimited**

[1] Simulated
[2] System with two regulating rectifiers and one fixed rectifier, PCE dominated by fixed rectifier that delivers 80 % of the power.

TABLE II

COMPARISON AGAINST (MULTICHANNEL) STIMULATOR IMPLEMENTATIONS WITH DYNAMIC VOLTAGE SCALING

Work	2023 [41]	2023 [24]	2023 [25]	2021 [26]	2022 [28]	2024 [42]	This work
Technology (µm)	0.18	0.25	0.18	0.18	0.18	0.18	0.18
Max. output voltage	12 V	5 V	12 V	−5.4 V/+3.6 V	12 V	±6 V	5 V
Max. output current	N/S	160 µA	2 mA	100 µA	1 mA[1]	2.5 mA	95 µA
Area/Channel (mm^2)	N/S	0.01	0.042	0.088	0.11	0.73	0.046
$EF_{CS,min}$	0.63[2]	N/S	N/S	N/S	0.6	0.51[3] 0.52[4]	0.23[3] 0.81[4]
Number of voltage steps	3	4	4	5	4	Continuous	**Continuous**
Parallel output regulation	Yes	Yes	Yes	Yes	Yes	No	**Yes**
Voltage regulation	Compliance monitor + MUX	Compliance monitor + MUX	Compliance monitor + MUX	Compliance monitor + MUX	External control	Current sensing fb loop	**Headroom voltage fb loop + regulating rectifier**
Tested load impedances							
R (kΩ)	-	-	-	-	10	2	30-70
RC (kΩ+nF)	8 + 30	20 + 50	2 + 24 & 15 + 100	8.72 + 22	1.2-2.5 + 80-16	2 + 2000	2 + 4.7-22
Electrodes	No	No	No	No	No	Yes	Yes

[1] External current sources [2] Simulated [3] Considering efficiency at output-driver [4] Considering overall efficiency

rectifiers (Table I), this work combines continuous regulation and parallel output capability with the smallest reported per-channel area ($368\mu m \times 126\mu m$) and a small C_o (40 pF), enabling fast adaptation and TDM. The measured maximum output-driver power conversion efficiency, $PCE_{out,max}$, is 95 %, while the maximum rectifier efficiency, $PCE_{rect,max}$, is 64 %. Unlike [27], the approach is not fundamentally limited in the number of parallel regulators.

When compared to other multichannel stimulator implementations employing dynamic voltage scaling (Table II), the proposed design offers a continuous output voltage while allowing parallel output regulation. Most prior works utilize compliance monitors or external control circuits to manage voltage regulation. In contrast, our design leverages a local regulating rectifier that autonomously adjusts the voltage supply based on the headroom voltage, eliminating the need for additional compliance monitoring circuits. Furthermore, the multichannel systems with dynamic voltage scaling are compared using EF_{CS}, an energy-based metric relative to a constant-supply current-source stimulator [17], [28]. We use the convention

$$EF_{CS} = \frac{E_{sup}}{E_{cs}}, \tag{8}$$

where E_{sup} is the energy consumed with the scaled supply and E_{cs} is the energy of an ideal fixed-supply current-source stimulator. Therefore, smaller EF_{CS} indicates lower energy relative to the fixed-supply baseline.

While prior works evaluate efficiency based on selected load conditions, Table II emphasizes that different designs target varying load scenarios, which may influence benchmarking results in favor of specific designs. In contrast, our approach addresses the challenges posed by variability and unpredictability in output conditions by generating a continuous output voltage, ensuring consistently high efficiency across a wide range of load scenarios. The objective of this work is not to optimize efficiency for a single load condition but to enable

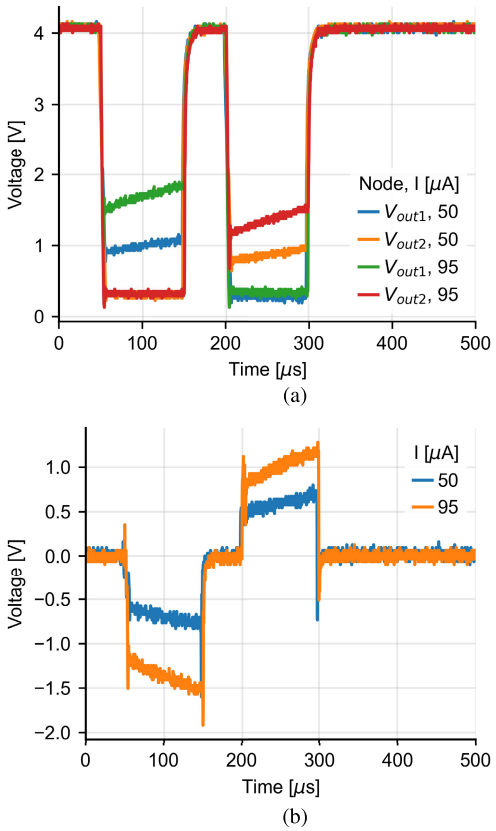

Fig. 29. In vitro measurements of the (a) output voltage and resulting (b) differential load voltage for current amplitudes of 50μ A and 95μ A.

power-efficient operation across diverse operating scenarios. In this respect, we have shown that the proposed circuit offers high efficiency at the output for realistic output conditions in the application of intracortical visual stimulation (Fig. 25), with an increase of 17 % compared to implementations with 4 voltage steps.

V. Discussion

The presented power management strategy of parallel regulating rectifiers that regulate the output voltage based on the headroom voltage of the current source offers high adaptability in the output voltage. Due to the implementation of the feedback circuit, the rectifier matches the output voltage without the need for a compliance monitor that is required for existing implementations [30]. This implementation reduces the complexity of the local controller associated with the other forms of local voltage regulation (Fig. 2b and 2c) [22], [24], [25], [26], [27]. The adaptability results in high power efficiency at the output driver, compared to the conventional fixed-voltage implementation (Fig. 22), achieving efficiency as high as 94 % for 50 kΩ, and > 80 % across almost all load conditions. Furthermore, the flexibility of the circuit results in a median efficiency at the output of 88 % when applied to experimental data from intracortical visual prostheses, doubling the efficiency compared to the conventional fixed supply.

The regulation speed of the output voltage allows the circuit to be used for efficient TDM between multiple electrodes, where the output requirements for each electrode will be different. The implemented design only occupies $368\mu\text{m}\times126\mu\text{m}$ per channel, achieving the lowest area among circuits employing continuous and parallel output regulation. The area could be further improved if part of the circuit is placed under the filter capacitor, C_o. Together, these features make the proposed implementation an attractive and power-efficient alternative for scaling stimulation systems to many channels.

Yet, there is room for further improvement, which is discussed here. The overall efficiency of the current design is not yet optimized and is mainly limited by conduction losses in M_p. There are several opportunities to improve the overall efficiency of the rectifier further. First, the size of M_p could be increased to reduce R_on and thereby the conduction losses. Additionally, the delay introduced by the comparator and switch driver leads to a voltage drop over the switch at the onset of the pulses, which leads to increased conduction losses. Offset compensation at the input of the comparator could improve the overall efficiency by minimizing the delays of the feedback [43], [44], [45], [46]. Reducing the voltage drop over M_p by sizing and offset compensation would also improve the maximum VCR of the rectifier. Furthermore, pulse frequency modulation (PFM) could improve the efficiency for small output currents [31]. Lastly, adaptive-biasing of the comparator could reduce the static power consumption of the feedback loop [31], [47].

Although the design is demonstrated here with two channels, it is designed to be scalable to many parallel channels. Other designs are fundamentally limited to provide only a few output rails. Scaling the number of output channels of the presented design is a matter of putting multiples of the same circuit in parallel. With the current dimensions, a system with 100 channels would take up less than 5 mm^2. Note that this includes an integrated output capacitor on-chip for each channel, whereas the output capacitance in some other works is off-chip [27]. As mentioned before, the area per channel could be reduced by placing circuits under C_o. Combined with time-division multiplexing, the number of channels could be increased to over 1000 for large-scale multichannel applications. Given that each rectifier only provides the output power for a single channel, the impact on the input signal from a wireless link from a single rectifier should be small. Furthermore, since the load conditions for each channel are different, the conduction periods of the different rectifiers will be spread in time. To spread the conduction periods even more, one could design the proposed circuit to operate at the falling phase of the input signal, similar to the peak right rectifier in [27], and distribute the designs over the system such that half of the channels rectify on the falling phase. Simulations with twenty parallel modules showed robustness to small distortions on the input signal. However, the source impedance of the power receiver plays an important role, and more investigation is needed to analyze the impact of many parallel modules.

Finally, the presented system only incorporated the proposed voltage regulators and output drivers. A complete stimulator system would require additional circuits (e.g., charge balancing, overvoltage protection) to ensure safe operation.

TABLE III

Summary of the Datasets Used in This Work. All Numerical Data Is Presented as Mean ± Sd

#	Source	Dataset	Electrode impedance [kΩ]	Current threshold [μA]
1	[2]	Human	47.0 ± 4.8	67 ± 37
2	[3]	Monkey A early	144.7 ± 72.6	65 ± 45
3	[3]	Monkey A late	71.1 ± 70.6	60 ± 58
4	[3]	Monkey L early	75.1 ± 36.3	19 ± 17
5	[3]	Monkey L late	74.9 ± 36.4	80 ± 71

VI. Conclusion

Variability in the load conditions between channels leads to low power efficiency in large-scale multichannel stimulator systems. This work introduces a novel power management strategy that offers adaptive regulation of the output voltage for each channel individually. The presented design implements a regulating rectifier for bipolar electrode configurations, where the headroom voltage on the current source is used as feedback voltage. In this way, the channel-specific output voltage is automatically scaled to the requirements of the load without the need to characterize the load impedance. The scaled voltage results in high power efficiency at the output driver over a wide range of load conditions. We demonstrated the scalability of the proposed circuit by showing the potential for time-division multiplexing of the output driver to many channels. Furthermore, the design was tested on realistic electrode impedances, where it could track the required output voltage. Lastly, we have listed recommendations to further improve the efficiency of the proposed power management strategy.

Appendix I

Appendix Efficiency Analysis Experimental Data

The efficiency analysis presented in Section IV-D is based on the analysis method presented in [21]. For this analysis, we used the experimental data from [2] and [3]. In total, we used five datasets, one from [2] (Human), and four from [3] (Monkey A early, Monkey A late, Monkey L early, Monkey L late). The current thresholds and electrode impedances for

these data sets are listed in Table III. Using these distributions, we created a new dataset with 10 000 entries for each of the subjects. In this dataset, all electrode impedances are rounded to a multiple of 10kΩ, and all current thresholds are rounded to a multiple of 5μ A. Furthermore, the current data is truncated over the range of 20μ A to 95μ A, and the impedance data is truncated to the range of 20kΩ to 80kΩ. The truncation and rounding of the entries are based on the measurement data obtained for the circuit. For the resulting dataset, efficiencies for each entry are calculated as described in [21] while taking into account a headroom voltage of 250 mV. Furthermore, the measured efficiency at the output of the proposed circuit is mapped to the data based on the current threshold and electrode impedance of each entry. As a result, we can compare the efficiency distributions for the different scenarios based on experimental data.

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