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# A 3V 15b 157 $\mu$ W Cryo-CMOS DAC for Multiplexed Spin-Qubit Biasing

Luc Enthoven, Job van Staveren, Jiang Gong, Masoud Babaie and Fabio Sebastiano

Delft University of Technology, Delft, The Netherlands; E-mail: L.A.Enthoven@tudelft.nl

## Abstract

This paper presents a 15b cryo-CMOS DAC for multiplexed spin-qubit biasing implemented in a 22-nm FinFET process. The integrating-DAC architecture and the robust digitally-assisted high-voltage output stage enable a low power dissipation (157 $\mu$ W) and small area (0.08mm<sup>2</sup>) independent of the number of biased qubits, and a 3V output range well beyond the nominal supply. This represents the first scalable solution for cryo-CMOS qubit biasing, which achieves a 1.8 $\times$  better voltage resolution with a lower DNL over a 3 $\times$  larger output range than the current state-of-the-art.

## Introduction

Semiconductor spin qubits present a promising, scalable platform for quantum computing. For each spin qubit, several gate electrodes electrostatically confine electrons (or holes) in quantum dots, which are cooled to sub-Kelvin temperatures. For the few (<10) spin qubits available today, all electrodes are wired to room-temperature electronics for the biasing, driving, and readout of the qubits. However, this approach is not scalable to future million-qubit quantum computers due to the unfeasibly large number of wires necessary. Thus, the control electronics should also operate at cryogenic temperature close to the qubits, ideally on the same chip [1]. The cryogenic electronics must dissipate low power to comply with the cooling budget of cryogenic refrigerators (<1mW at T<0.1K) while ensuring sufficient performance not to degrade the fidelity of qubits, thus calling for power-efficient solutions.

While prior cryo-CMOS controllers focused on qubit dynamic driving and readout [2,3], no scalable solution for the electrostatic biasing has been shown. Each electrode requires a low-noise high-accuracy bias voltage that is individually calibrated to compensate for fabrication and material variability (Fig. 1) [4]. Furthermore, such calibration routines also ask for the monotonicity of the biasing circuit. The bias generator can be multiplexed over multiple electrodes using sample-and-hold (S/H) circuits [5]. Although this reduces the power dissipated per electrode ( $\sim 3\mu$ W/electrode [6]), prior work can only support up to 400 electrodes due to the limited available cooling power. Since these circuits are designed using nanometer CMOS for future compatibility with spin-qubit fabrication, their output bias range is limited by the nominal supply (e.g., <1V), despite spin qubits requiring bias voltages up to 3V [7]. As an alternative, this paper describes a 22-nm FinFET bias DAC with a 3V output range and power dissipation independent of the number of electrodes thanks to an integrating-DAC architecture and a digitally-assisted high-voltage output stage.

## Circuit description

To maximize scalability, the presented DAC periodically generates a voltage ramp covering all the required bias voltages (Fig.1). By activating an analog demultiplexer (demux) at the right time, the bias voltage for each electrode is stored on a hold capacitor and periodically refreshed to counteract leakage.

Unlike prior DACs that generate a specific voltage for each electrode separately, the power dissipation and refresh rate of the presented DAC are largely independent of the number of biased electrodes and only limited by the total load capacitance. As the DAC only compensates for the hold-capacitor charge lost by leakage, requirements on the loading and settling are relaxed, potentially allowing the same voltage to be driven to multiple hold capacitors in parallel. The required refresh rate is expected to be <1Hz due to the very low leakage at cryogenic temperatures (<0.2 $\mu$ V/s [5]), thus relaxing the requirements on the minimum duration of the voltage ramp ( $t_{\text{bias}}$  in Fig.1) so that the circuit speed can be optimized for power consumption.

The integrating-DAC is implemented as a switched-capacitor integrator (Fig.2) supplied with a dc input voltage ( $V_{\text{ref}}$ ) to generate a ramp with discrete steps at the output, relaxing the synchronization with the demux in Fig.1 and achieving an inherently monotonic output. The integrator step size can be dynamically adjusted (“gear shifting”) by varying the input capacitance  $C_{\text{in}}$  (implemented by an 8b binary DAC). Gear shifting allows reaching the required bias voltages faster by increasing the step size to skip unused voltage codes (Fig.3). When fewer integration cycles are used, also the output noise improves since the noise accumulated in the integration capacitance  $C_{\text{int}}$  scales with the number of integration cycles.

Since the nominal supply voltage,  $V_{\text{DD}}$ , for the adopted thick-oxide devices is 1.8V, a two-stage thick-oxide Miller amplifier with a specifically devised high-voltage output stage is used to reach the target 3V output range (Fig.2). The input and output stages are supplied by the nominal  $V_{\text{DD}}$  and  $2 \cdot V_{\text{DD}}=3.6\text{V}$ , respectively. For reliability, all voltages across the output-stage devices are kept within the nominal operating region by adding cascodes  $M_{2,3}$ , whose gates are dynamically biased during the voltage ramp by two coarse DAC’s ( $\text{DAC}_{\text{H,L}}$ ) (Fig.2). The amplifier input is shielded from the high-voltage output by the MOM capacitor  $C_{\text{int}}$ , which has a higher compliance voltage, allowing for a  $V_{\text{DAC}}$  output range of 0.3-3.3V for a  $V_{\text{CM}}=0.3\text{V}$ . The high-voltage output stage has been designed for a 500pF output load. This would enable driving more than 10,000 electrodes ( $\sim 5,000$  qubits) based on parasitic capacitance estimations.

The coarse DACs are implemented by 2b thin-film resistive ladders (Fig.4). Only 4 levels for  $V_{\text{DAC,L,H}}$  are needed to ensure the voltage compliance due to a large margin in voltage headroom, which also makes the coarse DACs robust to timing errors. Diode-connected transistors  $M_{\text{H,L}}$  in series with each ladder shift the DAC voltage by replicating the  $V_{\text{GS}}$  of the output-stage cascodes. This ensures robustness to shifts in the threshold voltage, which increases significantly at cryogenic temperatures [8]. In the coarse-DAC’s branches, the voltages across transistors are kept below 1.8V by using cascode transistors with the gate connected to  $V_{\text{DD}}$  and diode-connected transistors. To drive the PMOS switches in  $\text{DAC}_{\text{H}}$ , a level shifter translates digital 0-1.8V signals to the 1.8-3.6V domain.

## Measurement results and conclusions

The performance of the proposed DAC fabricated in a 22-nm FinFET process (Fig.5) is reported in Tab.1. The total load at the DAC output (wiring, instruments) is measured to be above 480pF. Fig.3 demonstrates gear shifting ( $128C_u$  to  $2C_u$ ), showing how to reach a 3.3V output within only 20ms while offering a 15b resolution and minimizing the output noise. The DAC is monotonic (Fig.6) and dissipates  $157\mu\text{W}$  at 4.2K for a 62kHz clock, which allows for operation in a dilution refrigerator below 100mK since no significant changes in transistor characteristics are expected with respect to 4.2K [8].

Compared to prior work (Tab.1), the proposed DAC achieves a  $1.8\times$  better voltage resolution with a lower DNL

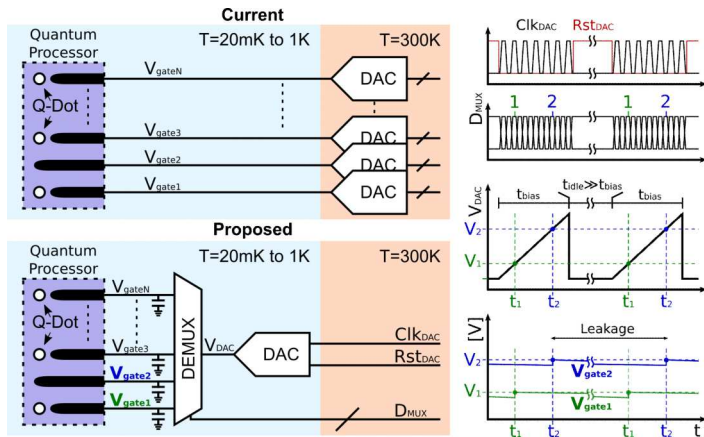


Fig. 1 Current method of biasing of spin-qubit electrodes (top), proposed cryo-CMOS DAC (bot) and corresponding voltage waveforms (right).

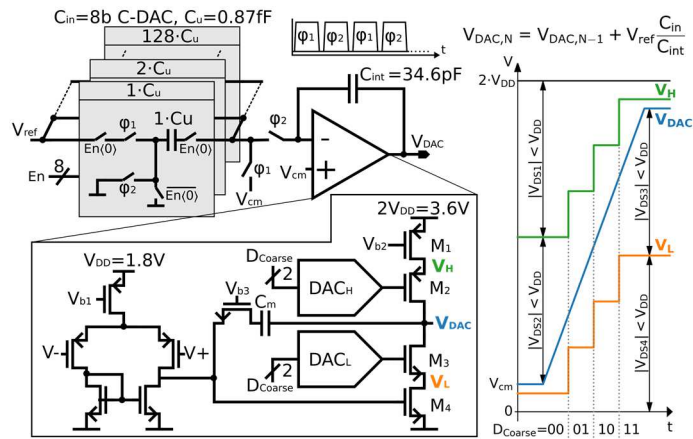


Fig. 2 Integrating-DAC with a low-voltage input-stage and a high-voltage output stage.  $V_L$  and  $V_H$  are dynamically biased via coarse  $\text{DAC}_H$ ,  $\text{DAC}_L$  depending on the output voltage  $V_{\text{DAC}}$  to ensure reliable operation.

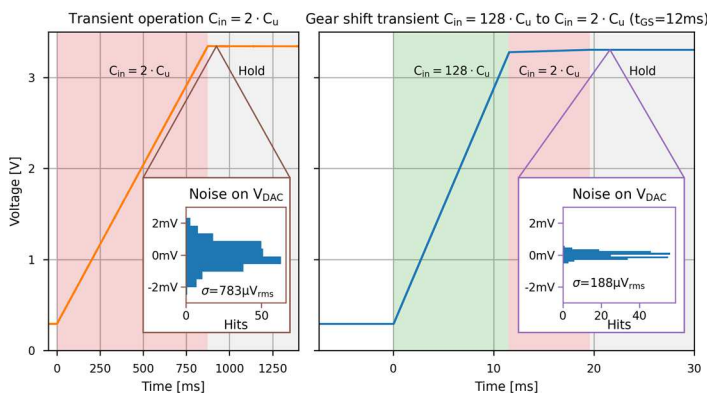


Fig. 3 Typical DAC output transient at 4.2K for regular and gear shift (GS) operation. The GS noise is limited by the noise floor of the acquisition card.

over a  $3\times$  larger output range. Thanks to the integrating-DAC architecture, the presented design offers power and area scalability to a very large number of electrodes, thus enabling the robust electrode biasing of large-scale quantum processors.

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Tab. 1 Performance summary and comparison table

	This Work	[6]	Off-the-shelf Qblox D5a†
<b>Technology [nm]</b>	22	65	Discrete
<b>Temperature [K]</b>	300	4.2	6
<b>Output Range [V]</b>	3	1	4
<b>V<sub>lsb</sub> [<math>\mu\text{V}</math>] (avg.)</b>	68.3	57.1	122.1
<b>Noise [<math>\mu\text{V}_{\text{rms}}</math>]</b>	192	188	N.A.
<b>INL [LSB]</b>	12.6	36.5	N.A.
<b>DNL [LSB]</b>	0.6	0.8	2.5†
<b>Refresh rate [Hz]</b>	> 1	3900	N.A.
<b>N<sub>electrode</sub></b>	10,000	8	1
<b>Power [<math>\mu\text{W}</math>]</b>	138	157	21.1
<b>Supply [V]</b>	1.8 & 3.6	1.1 & 2.5	$\pm 6$ V
<b>Core Area [mm<sup>2</sup>]</b>	0.076	0.14	N.A.

† Example of used lab equipment, available at <https://www.qblox.com/spi> † Estimated from figure

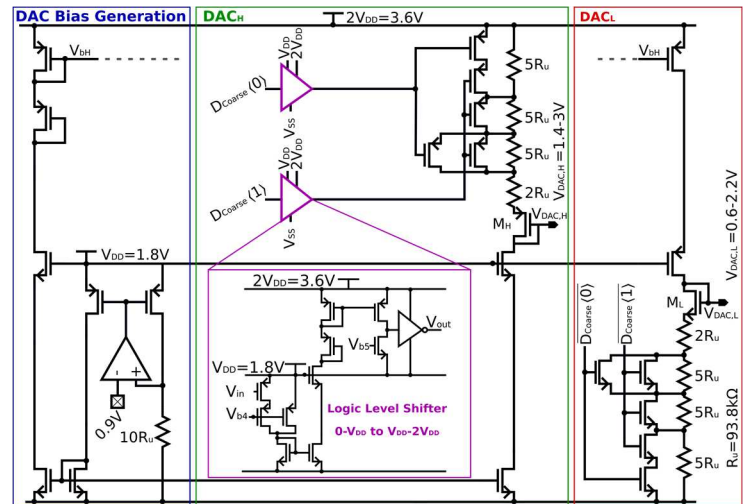


Fig. 4 Implementation of the coarse DACs ( $\text{DAC}_H$ ,  $\text{DAC}_L$ ), with PVT-robust bias generation and logic level shifters to drive the  $\text{DAC}_H$  switches.

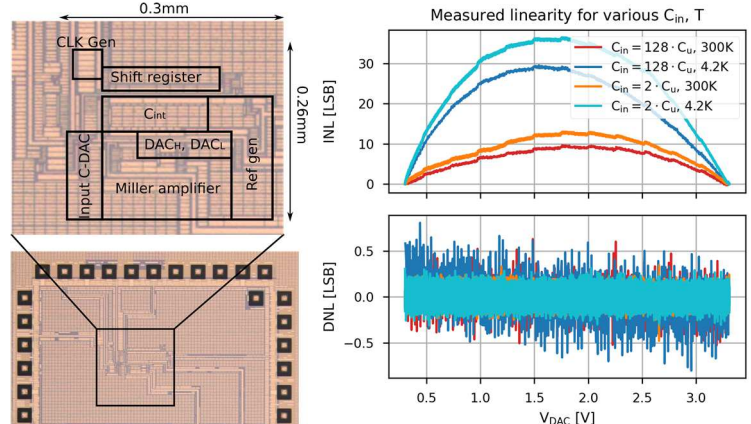


Fig. 6 Measured linearity at 4.2K and 300K for  $C_{in}=2C_u$  and  $C_{in}=128C_u$ .

Fig. 5 Die micrograph