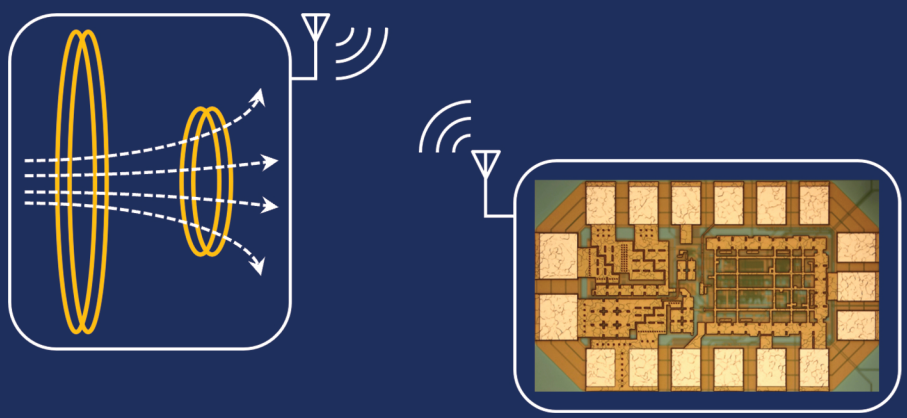
Integrated Interface Circuits for Wireless Power Transfer



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Integrated Interface Circuits for Wireless Power Transfer

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Dissertation

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Key words: Wireless power transfer, implantable medical devices, inductive resonant coupling, integrated interface circuits, power efficiency, output regulation, coupling adaptability, rectifier, global regulation, voltage mode, resonant current mode.

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Symbols

V_S	TX source voltage
I_S	TX source current
V_{IN}	Input voltage of a WPT system
V_{OUT}	Output voltage of a WPT or RX system
V_{O1}, V_{O2}	1st or 2nd output voltage of a multi-output WPT or RX system
V_{EA}	Error-amplifier output voltage
V_{REF}	Reference voltage
V_{REFH}	Upper regulation threshold voltage
V_{REFL}	Lower regulation threshold voltage
V_X	Switching-node voltage in a TX power amplifier
V_C	Capacitor voltage, typically across C_2
V_{AC1}, V_{AC2}	AC input node voltages at RX
V_{L1}, V_{L2}	Inductor voltage across L_1 or L_2 respectively
I_1	TX coil current
I_2	RX coil current
I_{OUT}	Output load current
I_{O1}, I_{O2}	1st or 2nd output load current
L_1	TX coil inductance
L_2	RX coil inductance
C_1	TX matching capacitance
C_2	RX matching capacitance
C_O / C_{OUT}	Output decoupling capacitor
C_{O1}, C_{O2}	1st or 2nd output decoupling capacitor
D_{COIL}	Separation distance between TX and RX coils
R_1	TX loop resistance
R_2	RX loop resistance
R_{OUT}	Output load resistance
R_{O1}, R_{O2}	1st or 2nd output load resistance
R_{ON} / R_{SW}	On resistance of a power transistor/switch
R_{CKT}	Equivalent circuit resistance
M	Mutual inductance between TX and RX coils
k	Magnetic coupling coefficient
ω	Angular frequency
f_C	Carrier frequency
Z_{EQ}	Equivalent RX reflected impedance at TX
Z_{RE}	Residual impedance
Z_{RX}	Equivalent RX impedance
P_{OUT}	Output power delivered to the load
P_{RX} / P_{MN}	Power delivered to the RX side
PTE / η_{LINK}	Link power-transfer efficiency
PCE	Power conversion efficiency
Q	Quality factor

Acronyms and Abbreviations

WPT	Wireless Power Transfer
WPDT	Wireless Power and Data Transfer
TX	Transmitter
RX	Receiver
IMD	Implantable Medical Device
BCI	Brain–Computer Interface
IoT	Internet of Things
RF	Radio Frequency
ISM	Industrial, Scientific and Medical
VM	Voltage-Mode
CM	Current-Mode
V/CM	Voltage-/Current-Mode
RCM	Resonant-Current-Mode
PTE	Power Transfer Efficiency
PCE	Power Conversion Efficiency
E2E	End-to-End
VCR	Voltage Conversion Ratio
DO	Dual-Output
PA	Power Amplifier
FBR	Full-Bridge Rectifier
VD	Voltage Doubler
DOVD	Dual-Output Voltage Doubler
DORCM	Dual-Output Resonant-Current-Mode
LC	Inductor–Capacitor
LDO	Low-Dropout Regulator
SMPC	Switching-Mode Power Converter
SCPC	Switched-Capacitor Power Converter
PWM	Pulse-Width Modulation
PFM	Pulse-Frequency Modulation
LSK	Load-Shift Keying
COT	Constant-Off-Time
DOT	Dynamic-Off-Time
ZVS	Zero-Voltage Switching
EMI	Electromagnetic Interference
PVT	Process, Voltage, Temperature
S&H	Sample-and-Hold
EA	Error Amplifier
VCDL	Voltage-Controlled Delay Line
MPPT	Maximum Power Point Tracking
MEPT	Maximum Efficiency Point Tracking
BOM	Bill of Materials

Chapter 1 Introduction

Modern society is increasingly reliant on electronic devices, each of which requires some kind of power supply. Wireless power transfer (WPT) eliminates the need for physically connected cables, resulting in electronic devices with greater spatial freedom, the ability to operate in harsh or sealed environments, and, in some cases, eliminates the need for batteries and/or periodic maintenance [1.1][1.2][1.3]. This enables a wide range of applications, and in the near future, may help reduce the use of wired infrastructure and batteries, contributing to a more sustainable world.

Although the basic concept of WPT was demonstrated by Nikola Tesla in the early 20th century [1.4], its practical realization has only become feasible in recent decades, driven by advances in semiconductor technology, high-frequency power devices, and the creation of wireless charging standards such as Qi [1.5]. These developments have reignited interest in WPT and enabled its integration into compact consumer and industrial products. Implementations based on integrated circuits are becoming increasingly popular owing to their low cost, small footprint, and compatibility with modern portable and wearable electronics.

This thesis presents the design of integrated interface circuits for WPT in biomedical applications, where high power efficiency, adaptability to wireless link variations, and system miniaturization are critical. By incorporating new circuit topologies and control strategies, the proposed designs achieve state-of-the-art power efficiency with enhanced link adaptability. They also achieve competitive output regulation performance and size reduction.

This chapter is an introduction to the thesis. It starts by discussing various real-world applications of WPT. Then, diverse WPT technologies are presented and compared, leading to the choice of WPT technologies tailored to the targeted biomedical applications. Next, challenges and general design specifications for interface circuits in the selected type of WPT systems are discussed. The chapter ends with an overview of the thesis goals and organization.

1.1 Wireless Power Transfer Applications

WPT can be applied in many domains, including consumer electronics, biomedical implants, internet of things (IoT), smart infrastructure, smart homes, electric vehicles, industrial automation, etc., as illustrated in Figure 1.1.

In consumer electronics, wireless charging pads are used to charge wearable devices such as smartwatches and wireless earbuds [1.5]. Wireless charging desks or docking stations are also emerging. These technologies eliminate the need for charging cables,

making portable electronics more convenient and sustainable. In biomedical implantable devices, such as retinal implants [1.6], pacemakers [1.7], and brain-computer interfaces [1.8], WPT is essential to avoid invasive wires and eliminate risky battery replacement surgery [1.9]. For IoT applications, such as wireless sensor nodes and radio-frequency identification (RFID) tags, large networks may include tens or hundreds of distributed devices, making battery-free and maintenance-free operations, and thus the use of WPT, highly desirable [1.10]. Furthermore, WPT can be used in industrial automation for powering rotating machinery and mobile robots, and in electric vehicles for enabling cable-free charging at parking spots or via embedded road coils.

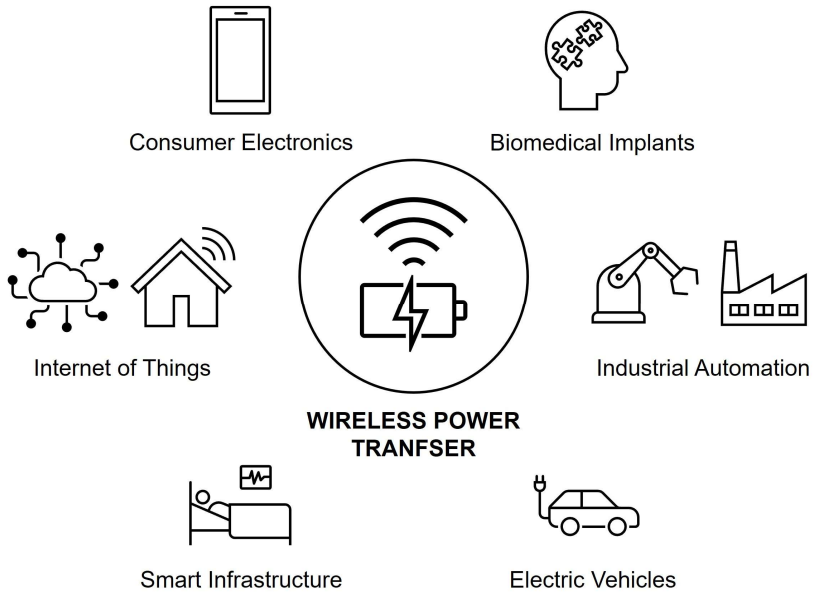

Figure 1.1 Wireless power transfer applications overview.

Different applications impose different requirements on WPT systems. For example, consumer electronics prioritize high output power and energy efficiency [1.5], whereas biomedical implants require miniaturized systems and robustness to coupling variations [1.2][1.9]. Electric vehicles demand kilowatt-level power delivery with resilient soft startup/switching and strong over-voltage/-current protection [1.11]. In contrast, wireless sensor nodes emphasize long-distance power transfer, low device fabrication cost, and compatibility with standard wireless communication protocols [1.10].

This thesis focuses on the use of WPT in biomedical applications. Unlike wireless charging, which is already widely adopted in consumer electronics, WPT for biomedical implants is still in its infancy and faces several scientific and technical challenges. Different types of implants impose different WPT specifications, which, in turn, requires different interface circuits. The discussions presented in the remainder of this thesis will be made in the context of biomedical applications.

1.2 Diverse Wireless Power Transfer Technologies

Wireless power transfer (WPT) can be realized via many different physical mechanisms. Each demands different circuit interfaces for power monitoring and control. This section discusses six promising WPT methods: (1) inductive coupling, (2) inductive resonant coupling, (3) capacitive coupling, (4) ultrasonic power transfer, (5) magnetoelectric power transfer, and (6) radio-frequency (RF) power transfer, as shown in Figure 1.2. Notably, emerging technologies such as optical WPT (near-infrared) [1.12] and body-coupled powering [1.13] are also promising solutions that deserve further investigation.

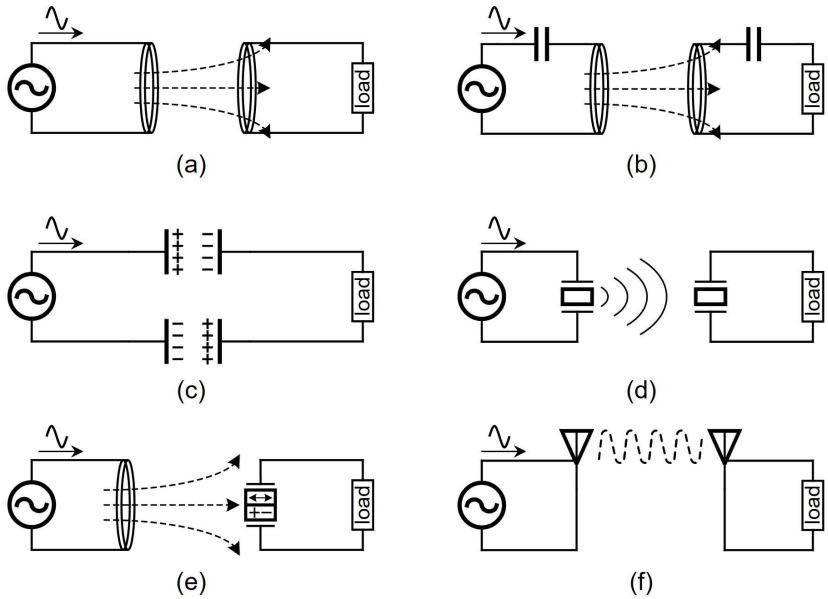

Figure 1.2 Diverse wireless power transfer modalities. (a) Inductive coupling. (b) Inductive resonant coupling. (c) Capacitive coupling. (d) Ultrasonic power transfer. (e) Magnetoelectric power transfer. (f) Radio-frequency (RF) power transfer.

1.2.1 Inductive Coupling

Inductive coupling relies on Faraday's law of electromagnetic induction, as shown in Figure 1.2(a). By driving an alternating current (AC) through a primary coil, a time-varying magnetic field is created, which induces a voltage in a nearby secondary coil [1.3][1.14][1.15]. Based on this principle, power can be wirelessly transferred from the primary coil to the secondary coil. When the coils are placed in close proximity, high power transfer efficiency (PTE) can be achieved. However, this degrades rapidly with increased separation distance or lateral misalignment between the coils.

1.2.2 Inductive Resonant Coupling

For more robustness to positional variations, which essentially corresponds to weaker coupling conditions, inductive resonant coupling can be employed by adding

capacitors to both the primary and secondary sides, forming inductor-capacitor (LC) resonant tanks [1.16], as shown in Figure 1.2(b). These resonators are tuned to the same frequency as the excitation source. At resonance, the power factor, defined as the ratio of real power to apparent power, is significantly improved on both sides. Specifically, series resonance on the primary side increases the power delivered from the excitation source, and series resonance on the secondary side improves PTE [1.14]. Together, these effects enable enough power to be transferred to the secondary side even under weak coupling conditions. A more detailed discussion is provided in Section 2.2.

1.2.3 Capacitive Coupling

Capacitive coupling relies on the electric field formed between two pairs of aligned conductive plates, as shown in Figure 1.2(c) [1.15]. When an AC voltage is applied to the plates on the primary side, an alternating electric field is generated, which induces a displacement current across the corresponding plates on the secondary side.

At short transfer distances, capacitive coupling can achieve high PTE. However, similar to non-resonant inductive links, its power and efficiency degrade rapidly with increased separation, as the coupling capacitance decreases. Moreover, such systems are highly sensitive to lateral misalignment, which further limits its practical robustness. As with inductive coupling, resonant LC networks can be used to reduce charge-sharing losses and improve the voltage conversion ratio [1.17].

1.2.4 Ultrasonic Power Transfer

As shown in Figure 1.2(d), ultrasonic power transfer operates via piezoelectric transducers, which convert electrical energy into mechanical vibrations on the transmitter side. These vibrations generate acoustic waves that propagate through a transmission medium and are received by a second piezoelectric transducer on the receiver side, where they are converted back into electrical energy [1.2][1.18].

Compared to electromagnetic waves, ultrasound exhibits lower attenuation in solid or fluid media, allowing for deeper penetration, and its shorter wavelength enables spatial focusability and supports the use of miniaturized receiver transducers. However, ultrasound is generally unsuitable for transmission through air due to high acoustic attenuation and poor coupling efficiency. Additionally, impedance mismatch at material interfaces, such as the air–tissue boundary, can result in substantial wave reflection, thereby reducing transmission power and efficiency [1.18].

1.2.5 Magnetoelectric Power Transfer

Magnetoelectric (ME) power transfer utilizes magnetoelectric materials composed of a magnetostrictive–piezoelectric heterostructure, as shown in Figure 1.2(e) [1.19]. When an AC current flows through a transmitter coil, it generates a time-varying magnetic field that excites the magnetostrictive layer within the ME composite at the

receiver. The resulting mechanical strain is transferred to the piezoelectric layer, which subsequently converts the mechanical energy into an AC voltage. As a result, the transmitted energy undergoes four transduction stages: electrical → magnetic → mechanical → electrical.

Unlike inductive coupling, ME power transfer depends on magnetic field strength rather than on magnetic flux linkage, thus enabling receiver miniaturization [1.20]. Moreover, unlike ultrasonic methods that require directional alignment, ME power transfer employs near-field magnetic coupling, rendering it largely insensitive to angular misalignment. It also avoids interface-related reflection losses. However, due to its near-field nature and inherently weak coupling, the output power achievable with ME systems is typically lower than that of ultrasonic power transfer under comparable size and implantation conditions.

1.2.6 Radio-Frequency (RF) Power Transfer

RF wireless power transfer uses propagating electromagnetic waves to deliver energy over long distances, as shown in Figure 1.2(f) [1.7][1.21]. When a high-frequency AC current (typically in the GHz range) flows through a transmitter antenna, it radiates electromagnetic waves into space, which are captured by a receiver antenna and converted back into electrical power.

Unlike near-field inductive coupling, RF power transfer operates in the far field, enabling energy transmission over distances ranging from meters to kilometers using compact antennas. It can also be readily combined with wireless data communication. However, due to free-space path losses, output power and efficiency decrease with distance. Furthermore, RF waves are strongly attenuated by biological tissues, limiting their effectiveness in powering deeply implanted biomedical devices [1.22].

1.3 Comparison of Wireless Power Transfer Technologies

As discussed in Section 1.2, different WPT modalities employ distinct physical mechanisms, each offering unique advantages and trade-offs. Table 1.1 provides a comparative summary of the key specifications of the major WPT modalities. Here, both inductive and capacitive methods are assumed to operate under resonant conditions. Note that SAR refers to the Specific Absorption Rate, which quantifies the rate at which electromagnetic or acoustic energy is absorbed by biological tissue.

In comparison, inductive and capacitive methods can achieve both high output power and power efficiency in short-medium scenarios. Ultrasonic and magnetoelectric methods enable deep penetration depths inside the human body and can support highly miniaturized RX designs. Notably, the delivered power by the ultrasonic link is typically higher than the magnetoelectric method in similar conditions (e.g., material dimensions) as the ultrasonic wave can efficiently be focused [1.23]. Due to their shorter wavelengths, ultrasonic and RF methods can be readily focused. The use of

acoustic waves allows ultrasonic systems to achieve a relatively high SAR safety threshold. RF WPT benefits from the ease of on-chip integration enabled by compact antenna structures. Similar integration is also feasible with near-field methods, including inductive and capacitive coupling, by operating at higher frequencies. Fabrication costs vary largely across modalities: while inductive and RF WPT systems are relatively low-cost, ultrasonic and magnetoelectric solutions are more expensive due to the use of specialized materials, such as piezoelectric and magnetostrictive composites.

Table 1.1 Specifications of diverse wireless power transfer technologies.

Specification	Inductive Resonant	Capacitive Resonant	Ultrasonic	Magnetoelectric	RF
Power Output (short range)	Very High (mW – W)	High (mW – W)	Moderate (μW – mW)	Low (μW – mW)	Low (μW – mW)
Efficiency (short range)	Very High (60 – 90%)	High (30 – 50%)	Moderate (10 – 30%)	Low (5 – 20%)	Very Low (<1 – 5%)
Tissue Penetration Depth	1 – 3cm	<1cm	5 – 10cm	3 – 5cm	1 – 2cm
Focusability	Low	Low	High	Low	Very High
Alignment Sensitivity	Medium	Very High	High	Low	High
SAR Limit Concern	Medium	High	Very Low	Low	Very High
Impedance Mismatch Sensitivity	Low	Low	Very High	Low	High
RX Miniaturization Capability	Medium	Low	Very High ($<1 – 5mm^3$)	High	High
CMOS Integration	Easy	Moderate	Difficult	Difficult	Easy
Fabrication Cost	Low	Medium	High	Very High	Low

From an application perspective, implantable medical devices (IMDs) span a wide range of clinical functions [1.24][1.25]. Neuro-electronic devices stimulate or record electrical activity in the nervous system, such as brain-computer interfaces (BCIs) [1.8], deep brain stimulators [1.26], spinal cord stimulators [1.27], cochlear implants [1.28], and retinal implants [1.6]. Cardiac electronic implants monitor and regulate heart activity, such as pacemakers [1.7] and implantable cardioverter defibrillators (ICDs) [1.29]. Wireless biosensors sense physiological parameters and integrate data telemetry, such as glucose monitors [1.30], intracranial pressure sensors [1.31], pH/oxygen/temperature sensors [1.31], and implantable ECG/EEG sensors [1.32]. Emerging IMD technologies also include closed-loop therapeutic systems (e.g., insulin pumps, programmable drug delivery systems) [1.33] and bioresorbable or flexible electronics [1.8].

Based on the above-mentioned references, the power requirements and implantation depths of diverse IMDs are summarized in Table 1.2. The diverse specifications demand tailored WPT strategies to ensure optimal performance and safety for each application.

Table 1.2 Power requirements and implantation depths of IMDs.

IMDs	Power Requirement	Implantation Depth
Brain-Computer Interfaces	20 – 100mW	3 – 15mm
Deep Brain Stimulators	50 – 100μW	2 – 10cm
Spinal Cord Stimulators	1 – 15mW	1 – 6cm
Cochlear Implants	10 – 40mW	4 – 10mm
Retinal Implants	40 – 150mW	4 – 30mm
Pacemakers	3 – 100μW	5 – 15cm
Cardioverter Defibrillators	50 – 500μW	5 – 15cm
Wireless Biosensors	500μW – 5mW	2mm – 10cm
Closed-Loop Therapeutic Systems	1 – 5mW	1 – 10cm
Drug Delivery Implants	1 – 3mW	1 – 10cm

From Table 1.2, IMDs can be broadly categorized into three power consumption ranges: high power (above tens of milliwatts), medium power (a few milliwatts), and low power (sub-milliwatt). Devices designed for high-resolution neural recording or large-array stimulation typically fall into the high-power category [1.8][1.34]. These include BCIs, cochlear implants, and retinal implants, which are often implanted at relatively shallow depths. In contrast, devices implanted deeper in the body, such as deep brain stimulators, spinal cord stimulators, pacemakers, etc., generally require medium to low power [1.35]. Wireless biosensors, such as subcutaneous sensors and those placed adjacent to internal organs, can be implanted at both shallow and deep locations with low power consumption [1.36]. Similarly, the implantation depths of closed-loop neuromodulators and drug delivery systems will depend on their specific application, but they typically require medium power levels [1.33].

Based on the above observations, ultrasonic and magnetoelectric methods are promising candidates for powering deep-implanted devices with low to medium power requirements, including deeply implanted biosensors, closed-loop neuromodulators, and drug delivery systems. RF methods are well suited for shallow-implanted biosensors and monitoring devices, owing to their inherent compatibility with wireless communication protocols. For deep, low-power cardiac implants such as pacemakers and implantable cardioverter defibrillators, two-stage or multi-stage WPT architectures may be adopted, for example, by cascading an inductive link with an ultrasonic link. Notably, renewable energy harvesting technologies offer a potential solution for powering low-power IMDs by harvesting energy from the ambient environment [1.37]. This, however, is out of scope of this thesis.

This thesis targets advanced, high-performance IMDs such as BCIs and retinal implants, which demand relatively high power levels and often involve complex system integration. For these applications, near-field WPT methods, inductive and capacitive coupling, are the best choices. Among them, inductive coupling is preferred due to its better tolerance to spatial misalignment and its greater penetration depth, while maintaining comparable power levels and PTE. Therefore, this thesis focuses on the

integrated interface circuit designs for inductive resonant WPT systems for high-power IMDs. Throughout the rest of this thesis, the term wireless power transfer (WPT) will explicitly refer to the inductive resonant method unless otherwise noted.

1.4 Design Specifications in WPT Interface Circuits

The design of WPT interfaces for IMDs entails the optimization of interrelated performance metrics and presents several challenges [1.9][1.38]. Four important design considerations can be identified: (1) power delivered to loads and power efficiency, (2) output regulation and multi-power-rail generation, (3) system compactness and bill-of-materials, and (4) robustness against wireless link variations.

1.4.1 Power Delivered to Loads and Power Efficiency

A WPT system must reliably deliver sufficient power to its loading circuits. The actual delivered power depends on multiple factors, including the TX input power level, power conversion efficiency (PCE) at both TX and RX, the wireless link coupling coefficient, and load impedance matching governed by the maximum power transfer theorem [1.9].

For IMD applications, the maximum deliverable power is further constrained by biological safety regulations. For instance, the Federal Communications Commission (FCC) limits the spatially averaged specific absorption rate (SAR) to 1.6 W/kg for 1 g of tissue over a 6-minute interval for head and torso exposure [1.39]. Such regulations establish the upper bound of transferable power, while the functional requirements of the IMD define the lower bound. Therefore, a successful WPT system must operate within this constrained power window.

Power efficiency is equally critical. A high RX PCE reduces energy loss and mitigates local tissue heating, addressing thermal safety concerns. High end-to-end (E2E) efficiency, measured from TX input to RX output, lowers overall energy consumption and extends the lifetime of battery-powered TX units (e.g., wearables). Maximizing efficiency also provides greater power headroom, enabling compliance with SAR limits. Achieving high efficiency requires careful co-optimization of circuit topologies and control strategies, remaining a central design challenge.

1.4.2 Output Regulation and Multi-Power-Rail Generation

As the primary power source for IMDs, the WPT system must satisfy stringent output performance requirements, including accurate voltage regulation under load and line variations, low steady-state ripple, and fast transient response.

Modern IMDs often require multiple supply voltages to support heterogeneous functional blocks, for example, 1.1 V for digital logic, 2.2 V for analog front-ends, and 3–10 V for neural stimulation drivers [1.40]. Each rail imposes distinct requirements. For WPT systems, generating multiple rails simultaneously without significant cross-

regulation remains a major challenge. Moreover, implementing multi-rail regulation must not come at the expense of power efficiency.

1.4.3 System Compactness and Bill-of-Materials

IMDs are subject to strict constraints on size, weight, and biocompatibility due to anatomical and surgical limitations. For example, retinal implants are typically limited to millimeter-scale system dimensions [1.41], and BCIs do not permit the widespread use of stiff, bulky electronic components [1.8]. In addition, cost is a critical factor, especially for IMDs intended for routine healthcare and commercial deployment.

These constraints motivate the development of highly compact and integrated WPT systems with minimal reliance on bulky off-chip components. However, system miniaturization must not compromise power efficiency and output regulation performance.

1.4.4 Robustness against Wireless Link Variations

Wireless links are one of the most critical variables in WPT systems. As will be elaborated in Chapter 2, the RX loads the TX through the link. Variations such as coil separation, lateral misalignment, or tissue-induced detuning alter the RX reflected impedance seen by the TX. These changes can cause fluctuations in both the power delivered to the RX and the effective voltage conversion ratio from TX to RX.

To ensure safe and reliable operation under such dynamic conditions, the WPT interface must employ robust and adaptive circuit and control strategies. These mechanisms should compensate for link variations in real time, maintaining stable power delivery and regulated output voltages.

1.5 Thesis Goals and Organization

The main goal of this thesis is to conduct a comprehensive investigation into the design of interface circuits for inductive resonant WPT systems targeting advanced IMD applications, and to improve performance beyond state-of-the-art designs.

The organization of this thesis is shown in Figure 1.3, which also shows the various sub-blocks present in a WPT system. Chapter 2 provides an overview of WPT system architectures, the underlying physics of coil coupling, and the evolution of WPT interface circuits. A thorough literature review is included.

Derived from the main goal, one key target of this thesis is to improve the coupling adaptability of the WPT interface circuits without sacrificing other performance metrics. To this end, three representative architectures, voltage-mode, hybrid voltage-/current-mode, and resonant-current-mode, have been designed, fabricated, and experimentally characterized.

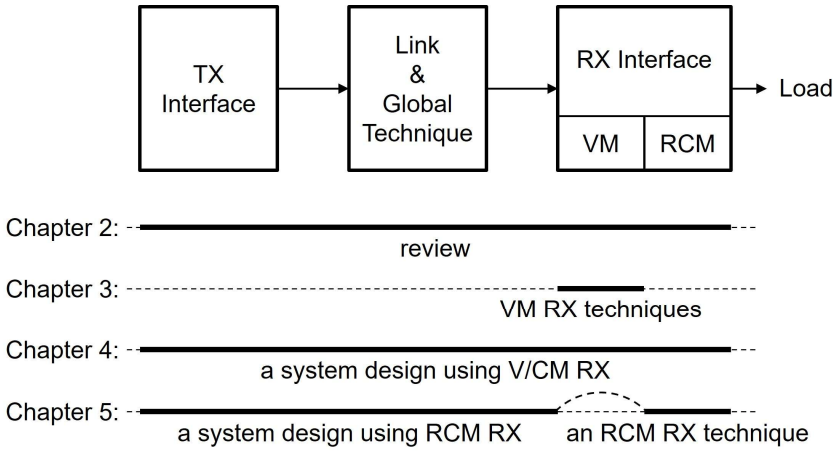

Figure 1.3 Sub-blocks of a wireless power transfer system and the organization of the thesis.

Chapter 3 focuses on voltage-mode (VM) RXs, which employ monophasic operation with high maximum power and peak efficiency, while exhibiting low voltage conversion ratios and narrow operable ranges. Two designs are presented: (1) a regulating voltage doubler, and (2) a dual-output extension. A compact single-stage dual-output RX is realized with 93% peak efficiency.

Chapter 4 presents a system design comprising a TX and an RX. It introduces a hybrid voltage-/current-mode (V/CM) RX, which extends the operational WPT range toward weaker coupling conditions by up to 50% compared with voltage-mode designs. Global power modulation is also investigated, resulting in a significant improvement in end-to-end efficiency compared with open-loop operation.

Chapter 5 studies resonant-current-mode (RCM) techniques, which are particularly well suited to weak-coupling and highly miniaturized scenarios. Two designs are presented: (1) a regulating three-phase RCM rectifier and (2) a compact 40.68-MHz WPT system based on the proposed three-phase RCM rectifier. Notably, an 8-mm-diameter RX coil is realized, achieving a sixfold reduction in form factor compared with state-of-the-art designs.

Finally, Chapter 6 concludes the thesis with main findings, a comparative analysis of the presented designs, and a discussion of future research directions.

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Chapter 2 Review of Wireless Power Transfer Systems

This chapter presents a system-level discussion of inductive resonant wireless power transfer (WPT) interface circuits. It begins with an overview of typical WPT system architectures, highlighting the key power management and signal processing components required at both transmitter (TX) and receiver (RX) sides. Next, the fundamental physics of magnetically coupled coils is examined, serving as a foundational framework for circuit design. This is followed by a comprehensive review of state-of-the-art RX and TX circuit designs. The chapter concludes with a discussion of global control loops for power regulation and an introduction to data telemetry techniques integrated within WPT systems.

2.1 System Design Overview

A typical inductive resonant WPT system comprises a TX and an RX connected via an inductive resonant link for energy transfer, as illustrated in Figure 2.1. It integrates several types of power conversion circuits, including DC–AC converters (inverters), AC–DC converters (rectifiers), DC–DC converters, and voltage regulators. In addition, a data channel may be further included for global power modulation or user data communication.

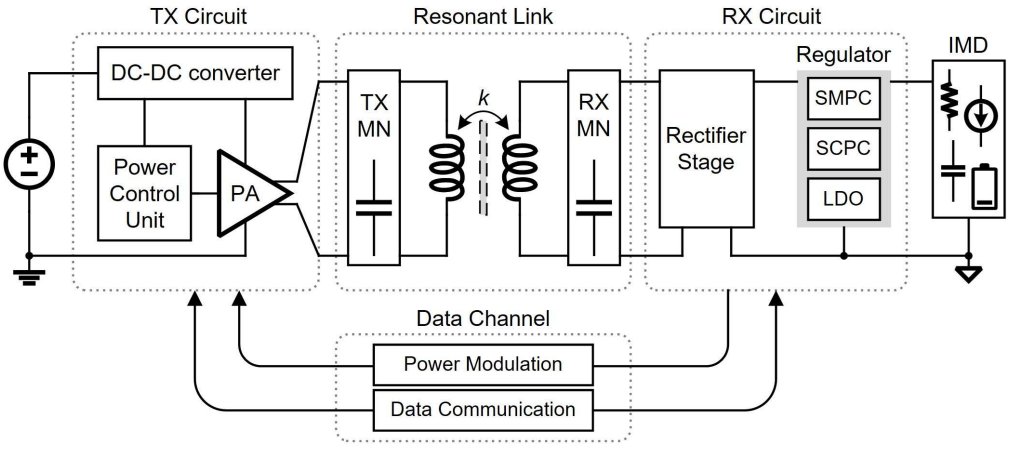

Figure 2.1 Block diagram of a generic WPT system.

In the TX circuit, a conventional implementation comprises a switching power amplifier (PA), which functions as an inverter, and a DC–DC converter modulating the PA's supply voltage to adjust the overall power transmitted across the link. A power control unit orchestrates the operation of both the PA and the DC–DC converter.

The resonant link consists of coupled TX and RX coils resonating at the same frequency, which is achieved by incorporating capacitive matching networks (MNs) connected either in series or parallel with the coils. Biomedical wireless systems commonly operate at industrial, scientific and medical (ISM) frequency bands, such as 6.78MHz, 13.56MHz, 40.68MHz, etc.

In the RX circuit, a typical architecture includes a rectifier that converts the received AC signal into DC, followed by a voltage regulator that ensures a stable output voltage for load circuits. The voltage regulator can be implemented using a switching-mode power converter (SMPC), a switched-capacitor power converter (SCPC), or a low-dropout regulator (LDO).

WPT systems may operate in either open or closed loop configurations. An open-loop WPT system operates the TX and RX circuits independently: the TX emits power at a certain level, and the RX executes AC-DC and voltage regulation locally. Closed-loop operation requires a data uplink channel that allows the RX to communicate load conditions back to the TX, enabling adaptive control of the transmitted power. Furthermore, the system may support simultaneous user data communication. In such cases, the data channel can be implemented either as a dedicated wireless link or as a through-power-link scheme embedded within the power channel.

2.2 Coupled Coils and Modeling

The resonant link bridges the TX and RX circuits, while it introduces variability and non-idealities that impact the WPT performance. Therefore, it is essential to consider different configurations, and their behavior in the presence of impedance mismatch and varying load and coupling conditions.

2.2.1 Resonant Link Configurations

The resonant link can be configured in four distinct ways, derived from the choice between series or parallel resonance at both TX and RX sides. They are: series–series (SS), series–parallel (SP), parallel–series (PS), and parallel–parallel (PP), as illustrated in Figure 2.2. Here, L_1 and L_2 represent the TX and RX coils, respectively, which are magnetically coupled with a coupling coefficient k; C_1 and C_2 denote the matching capacitors that form the resonant tanks at respective sides. The TX circuit is modeled as either a voltage source V_S or a current source I_S, while the "load" block represents the RX circuit and subsequent load circuitry.

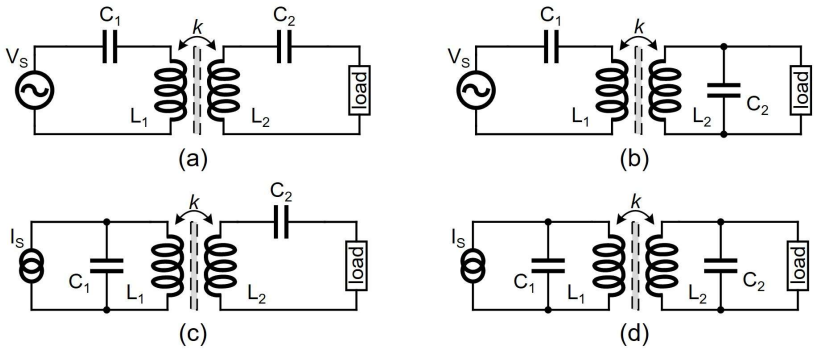

Figure 2.2 Resonant link configurations. (a) Series-series. (b) Series-parallel. (c) Parallel-series. (d) Parallel-parallel.

At TX, the combination of a voltage source and a series-resonant network [Figure 2.2(a) and (b)] is more widely adopted than the alternative architecture based on a current source and a parallel-resonant network [Figure 2.2(c) and (d)]. This preference arises from two main practical considerations. First, series resonance presents a relatively low and well-controlled input impedance at resonance, which naturally limits voltage stress on the TX circuit and simplifies device protection and integration. In contrast, parallel-resonant TX configurations exhibit high impedance at resonance, requiring large voltage swings to deliver comparable power. Second, parallel-resonant TX structures are inherently sensitive to load variations [2.1][2.2], resulting in resonance detuning and excessive voltage under light-load or open-circuit conditions, which degrades robustness and complicates system control. Hence, voltage-mode TX circuits (e.g., Class-D power amplifiers) with series-resonant matching are adopted as the primary TX architecture in this thesis.

At RX, the selection of resonant configurations depends on the load range. Intuitively, for heavy loads (i.e., low resistance), series resonance is preferred due to its ability to maintain a reasonable quality factor with small load resistances. Parallel resonance, in this case, leads to resonant detuning [2.3], as the load diverts excessive current from the resonant capacitor. Conversely, for light loads (i.e., high resistance), series resonance suffers from a degraded quality factor, while parallel resonance retains effective performance. A quantitative analysis of both configurations will be provided in Section 2.2.5.

2.2.2 Reflected Load Theory

The RX circuit loads the TX circuit through the resonant link. To design interface circuits, particularly at the RX, it is essential to understand how load impedance is transformed across the link. Figure 2.3(a) illustrates a link configuration using series resonance at the TX side.

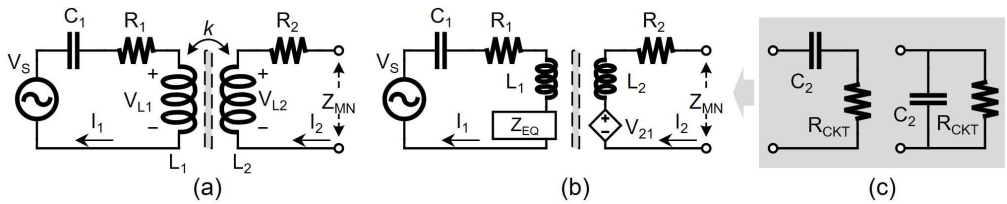

Figure 2.3 Reflected load modeling. (a) Link configuration. (b) Equivalent circuit model. (c) RX-side equivalent impedance circuits.

Based on Kirchhoff's voltage law and electromagnetic coupling theory, the time-domain voltage–current relationships for the TX and RX sides are expressed as

$$V_{L1}(t) = L_1 \frac{dI_1}{dt} - M \frac{dI_2}{dt}; \tag{2.1}$$

$$V_{L2}(t) = M \frac{dI_1}{dt} - L_2 \frac{dI_2}{dt} = I_2(R_2 + Z_{MN}); \tag{2.2}$$

Here, $M = k\sqrt{L_1 L_2}$ denotes the mutual inductance between the coupled L_1 and L_2 (k is the coupling coefficient), and R_1 and R_2 represent loop resistances on TX and RX sides, respectively. (2.1)–(2.2) can be transformed into the phasor domain, as given by

$$V_S = \left(R_1 + \frac{1}{j\omega C_1}\right) I_1 + j\omega L_1 I_1 - j\omega M I_2; \tag{2.3}$$

$$j\omega M I_1 - j\omega L_2 I_2 = (R_2 + Z_{MN}) I_2. \tag{2.4}$$

If the coupling is replaced by equivalent circuit representations at both sides, as shown in Figure 2.3(b), the reflected impedance observed at the TX side from the RX circuit, denoted Z_{EQ}, is given by

$$Z_{EQ} = \frac{\omega^2 M^2}{j\omega L_2 + R_2 + Z_{MN}}, \tag{2.5}$$

where Z_{MN} represents the equivalent impedance of the RX matching network and the RX circuit, which varies depending on whether series or parallel resonance is employed, as shown in Figure 2.3(c). Specifically,

- For series-resonance RX:

$$Z_{MN} = R_{CKT} + \frac{1}{j\omega C_2}. \tag{2.6}$$

- For parallel-resonance RX:

$$Z_{MN} = \frac{R_{CKT}}{1 + j\omega C_2 R_{CKT}} = \frac{R_{CKT}(1 - j\omega C_2 R_{CKT})}{1 + (\omega C_2 R_{CKT})^2}. \tag{2.7}$$

Here, R_{CKT} denotes the equivalent impedance of the RX rectifier and load circuitry. For series-resonance RX, the imaginary part of Z_{MN}, $Im\{Z_{MN}\}$, is determined by C_2. By setting $\frac{1}{\omega C_2} = \omega L_2$ ($\omega = \frac{1}{\sqrt{L_2 C_2}}$), or equivalently $\omega = \frac{1}{\sqrt{L_2 C_2}}$, the expression for Z_{EQ} shown in (2.5) simplifies to

$$Z_{EQ} = \frac{\omega^2 M^2}{R_2 + R_{CKT}}. \tag{2.8}$$

For parallel-resonance RX, the expression for Z_{MN} is more complex, and $Im\{Z_{MN}\}$ depends on both C_2 and R_{CKT}. If $(\omega C_2 R_{CKT})^2 \gg 1$ is assumed, (2.7) can be rewritten as

$$Z_{MN} \approx \frac{1}{R_{CKT}(\omega C_2)^2} + \frac{1}{j\omega C_2}. \tag{2.9}$$

In this regime, $Im\{Z_{MN}\}$ becomes largely insensitive to variations in R_{CKT}. Applying the same resonance condition $\omega = \frac{1}{\sqrt{L_2 C_2}}$, Z_{EQ} becomes

$$Z_{EQ} = \frac{\omega^2 M^2}{R_2 + \frac{1}{R_{CKT}(\omega C_2)^2}}. \tag{2.10}$$

The approximation condition, $(\omega C_2 R_{CKT})^2 \gg 1$, is generally required in practical parallel-resonance RX designs to ensure that the resonant behavior is not significantly disturbed by fluctuations in the load impedance.

By observing (2.8) and (2.10), it is evident that the reflected impedance Z_{EQ} decreases with increasing R_{CKT} in series-resonance RXs, while it increases with R_{CKT} in parallel-resonance RXs. Therefore, for a fixed TX configuration, series- and parallel-resonance RXs exhibit optimal performance at distinctly different load conditions.

2.2.3 Link Efficiency

Link efficiency is a key performance metric of the resonant link, determining the proportion of power successfully delivered to the load. It directly impacts the thermal safety and SAR compliance of WPT systems. The link efficiency, η_{LINK}, is defined as the ratio of the power delivered to $Re\{Z_{MN}\}$, P_{MN}, over the power extracted from the source V_S, P_1. Based on the reflected load theory, η_{LINK} can be derived by evaluating the TX and RX sides separately:

- At the RX side, the power transfer efficiency (η_{PTE_2}) is defined as the ratio between the power delivered to $Re\{Z_{MN}\}$ and the power dissipated in R_2 and $Re\{Z_{MN}\}$, which is given by

$$\eta_{PTE\_2} = \frac{Re\{Z_{MN}\}|I_2|^2/2}{Re\{Z_{MN}\}|I_2|^2/2 + R_2|I_2|^2/2} = \frac{Re\{Z_{MN}\}}{Re\{Z_{MN}\} + R_2}. \tag{2.11}$$

Here, $|I_2|$ represents the I_2 amplitude.

- At the TX side, the power transfer efficiency (η_{PTE_1}) is defined as the ratio between the power delivered to $Re\{Z_{EQ}\}$ and the power dissipated in R_1 and $Re\{Z_{EQ}\}$, which is given by

$$\eta_{PTE\_1} = \frac{Re\{Z_{EQ}\}|I_1|^2/2}{Re\{Z_{EQ}\}|I_1|^2/2 + R_1|I_1|^2/2} = \frac{Re\{Z_{EQ}\}}{Re\{Z_{EQ}\} + R_1}. \tag{2.12}$$

Here, $|I_1|$ represents the I_1 amplitude, and under resonant conditions, Z_{EQ} is purely real, as proved by (2.8) and (2.10). By combining (2.11) and (2.12), η_{LINK} can be derived as

$$\eta_{LINK} = \eta_{PTE\_2} \cdot \eta_{PTE\_1} = \frac{Re\{Z_{MN}\}}{Re\{Z_{MN}\} + R_2} \cdot \frac{Re\{Z_{EQ}\}}{Re\{Z_{EQ}\} + R_1}, \tag{2.13}$$

which is valid for both resonant and non-resonant situations. Furthermore, considering (2.6), (2.8), (2.9), and (2.10), the closed-form expressions for η_{LINK} for series- and parallel-resonance RXs are given by

- For series-resonance RX:

$$\eta_{LINK} = \frac{1}{1 + \frac{R_2}{R_{CKT}}} \cdot \frac{1}{1 + \frac{R_1(R_2 + R_{CKT})}{\omega^2 M^2}}. \tag{2.14}$$

- For parallel-resonance RX:

$$\eta_{LINK} = \frac{1}{1 + R_2 R_{CKT}(\omega C_2)^2} \cdot \frac{1}{1 + \frac{R_1\left(R_2 + \frac{1}{R_{CKT}(\omega C_2)^2}\right)}{\omega^2 M^2}}. \tag{2.15}$$

From (2.14) and (2.15), it is observed that η_{LINK} has a maximum point in both cases, due to its second-order relationship with R_{CKT}.

2.2.4 Power Delivered to RX

The power delivered to the RX side ($Re\{Z_{MN}\}$), P_{MN}, which is fully dissipated by R_{CKT}, can be expressed as

$$P_{MN} = P_1 \cdot \eta_{LINK} = \frac{|V_S|^2}{2(R_1 + Re\{Z_{EQ}\})} \cdot \eta_{LINK}. \tag{2.16}$$

Assuming a series-resonant TX configuration [Figure 2.3(a)], the expressions for P_{MN} for series- and parallel-resonance RXs become:

- For series-resonance RX:

$$P_{MN} = \frac{|V_S|^2}{2(R_1 + \frac{\omega^2 M^2}{R_2 + R_{CKT}})} \cdot \frac{1}{1 + \frac{R_2}{R_{CKT}}} \cdot \frac{1}{1 + \frac{R_1(R_2 + R_{CKT})}{\omega^2 M^2}}. \tag{2.17}$$

- For parallel-resonance RX:

$$P_{MN} = \frac{|V_S|^2}{2(R_1 + \frac{\omega^2 M^2}{R_2 + \frac{1}{R_{CKT}(\omega C_2)^2}})} \cdot \frac{1}{1 + R_2 R_{CKT}(\omega C_2)^2} \cdot \frac{1}{1 + \frac{R_1(R_2 + \frac{1}{R_{CKT}(\omega C_2)^2})}{\omega^2 M^2}}. \tag{2.18}$$

2.2.5 Effects of RX Resonance

The analytical forms of η_{LINK} and P_{MN} reveal that the RX resonance configuration has a significant impact on system performance. To evaluate these effects, both metrics are calculated and simulated using the parameters listed in Table 2.1. The theoretical calculation is based on (2.14), (2.15), (2.17), and (2.18).

Table 2.1 Circuit parameters used in the analysis.

Parameters		**Values**
Source voltage amplitude, $\|V_S\|$		5 V
Carrier frequency, f_C		6.78 MHz
TX coil	**Inductance, L_1**	1 µH
	Resistance, R_1	1 Ω
TX coil matching capacitance, C_1		551 pF
RX coil	**Inductance, L_2**	0.5 µH
	Resistance, R_2	1 Ω
RX coil matching capacitance, C_2		1.1 nF

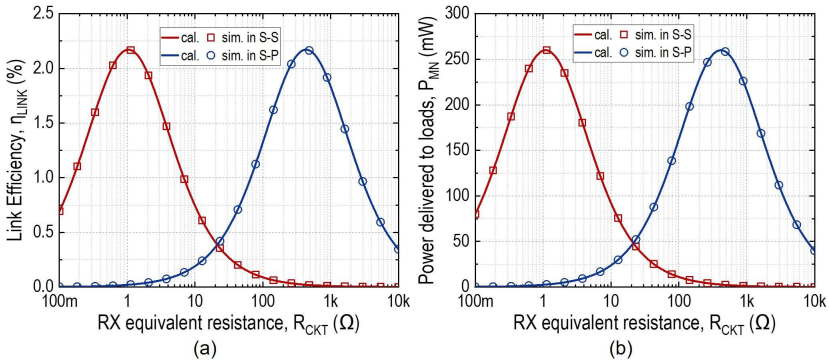

Figure 2.4 Effect of RX resonance at k=0.01. (a) η_{LINK} versus R_{CKT}. (b) P_{MN} versus R_{CKT}.

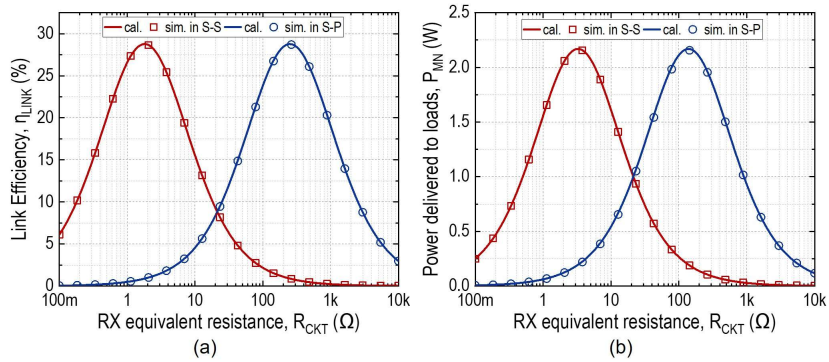

Figure 2.5 Effect of RX resonance at k=0.05. (a) η_{LINK} versus R_{CKT}. (b) P_{MN} versus R_{CKT}.

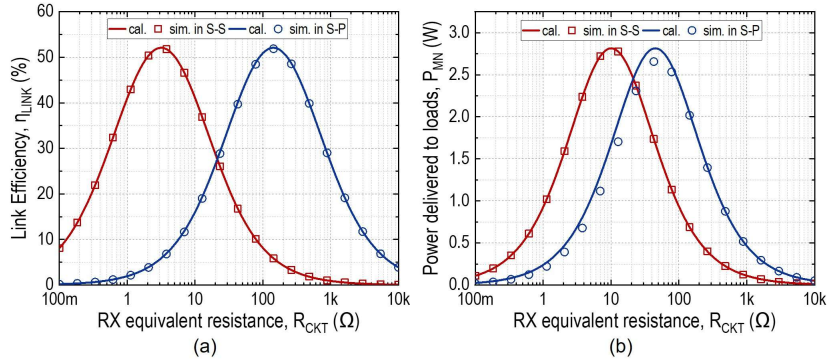

Figure 2.6 Effect of RX resonance at k=0.1. (a) η_{LINK} versus R_{CKT}. (b) P_{MN} versus R_{CKT}.

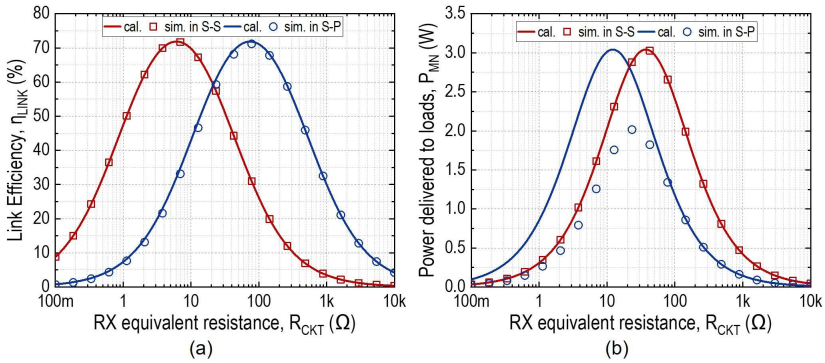

Figure 2.7 Effect of RX resonance at k=0.2. (a) η_{LINK} versus R_{CKT}. (b) P_{MN} versus R_{CKT}.

Figure 2.4, Figure 2.5, Figure 2.6, and Figure 2.7 show the calculated and simulated η_{LINK} and P_{MN} as functions of R_{CKT} for series–series (S–S) and series–parallel (S–P) TX–RX configurations under different coupling conditions. The results, especially under weaker coupling, confirm that the S–S configuration outperforms the S–P configuration under heavy load conditions (small R_{CKT}), offering higher link efficiency and power delivery. Conversely, the S–P configuration performs better under light load conditions (large R_{CKT}). These findings highlight the critical role of selecting appropriate matching network configurations based on anticipated loading conditions.

Moreover, in the S-S case, the calculated and simulated η_{LINK} and P_{MN} results show excellent agreement over the entire coupling range, owing to the straightforward modeling without mathematical approximations. In contrast, noticeable discrepancies appear in the S-P case, especially under stronger coupling, because of the approximation from (2.7) to (2.9), which becomes invalid as R_{CKT} decreases to the order of tens of ohms. For η_{LINK}, the mismatch between calculation and simulation remains limited because the approximated terms are partially normalized, as indicated in (2.13). In contrast, the calculation of P_{MN} exhibits larger errors, especially at k = 0.2, because the input power, P_1, is overestimated as the imaginary part of Z_{EQ} is neglected. However, since the targeted applications typically operate under weak coupling, i.e., $k \leq$ 0.1, the approximate model remains sufficiently accurate to provide meaningful insights and design intuition.

2.3 Receiver (RX) Design

A traditional RX interface circuit consists of two main stages: a rectifier that converts AC to DC and a voltage regulator that stabilizes the output supplied to the load circuits, as illustrated in Figure 2.1 [2.4][2.5][2.6][2.7]. While this architecture is functionally reliable, it suffers from cascaded power conversion efficiency (PCE) degradation and large form factor. This section provides a review of state-of-the-art RX circuit innovations that address these challenges in terms of active diode, delay compensation, output regulation, multi-output generation, and coupling adaptability.

2.3.1 Voltage-Mode (VM) Bridge Rectifiers

As the mainstream AC–DC converter topology, voltage-mode (VM) bridge rectifiers are widely employed in RX designs, such as the topologies shown in Figure 2.8(a). Driven by the requirements outlined in Section 1.4, their architecture and control techniques have evolved to improve efficiency and regulation performance, as discussed in the following subsections.

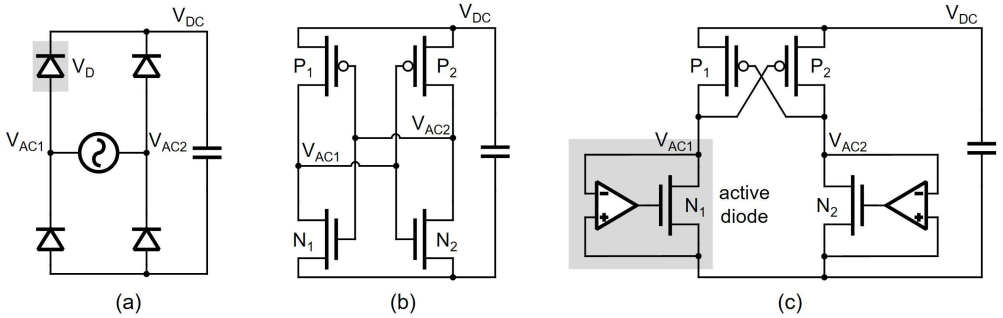

Figure 2.8 Rectifier topologies. (a) passive full-bridge rectifier. (b) cross-coupled rectifier. (c) active rectifier.

2.3.1.1 Active Diode and Delay Compensation

The conventional VM full-bridge rectifier uses passive diodes [Figure 2.8(a)] [2.8], enabling autonomous operation but incurring significant forward voltage drops (V_D), that degrade both PCE and voltage conversion ratio (VCR). For instance, assuming $V_{DC} = 5V$ and $V_D = 0.7V$, the theoretical PCE is limited to $\frac{V_{DC}}{V_{DC}+2V_D} \approx 78.1\%$.

To mitigate this limitation, cross-coupled rectifiers have been employed (Figure 2.8(b)) [2.9]. When V_{AC1} (or V_{AC}) exceeds V_{DC}, V_{AC2} (or V_{AC1}) is at ground, activating P_1 and N_2 (or P_2 and N_1) into the triode region without large voltage drops, provided that V_{DC} is higher than their threshold voltage, V_{TH}. However, if $V_{DC} > 2 \times V_{TH}$, conducting paths between V_{DC} and ground may arise, since both PMOS and NMOS devices will be turned on when V_{AC} (or V_{AC}) falls below $V_{DC} - V_{TH}$, leading to reverse current leakage.

To eliminate both forward voltage drops and reverse leakage, active rectifiers have been developed [2.10][2.11][2.12][2.13]. A common topology (Figure 2.8(c)) replaces the low-side diodes with comparator-controlled NMOS switches (active diodes), while retaining cross-coupled PMOS switches at the high side [2.10][2.11][2.14]. During the positive half-cycle of AC input, when V_{AC1} rises above V_{DC}, P_1 is already on if $V_{DC} > V_{TH}$. At this point, N_2 will be turned on as V_{AC} falls below ground by the comparator. Both P_1 and N_2 operate in the triode region. When $V_{AC1} - V_{AC}$ is smaller than V_{DC}, V_{AC} will surpass ground, and N_2 will be turned off accordingly by the comparator. In this positive half cycle, N_1 is always deactivated, so reverse conduction is prevented.

Notably, compared to the approach that replaces all four passive diodes with active diodes, the topology in Figure 2.8(c) is favored because it only requires two active-diode controllers, while the PMOS switches are autonomously driven and their gate capacitances are absorbed by the preceding resonance matching network [2.14].

Despite their advantages, active rectifiers introduce switching errors due to comparator delay and driver propagation delay, typically in the nanosecond range. Given that many biomedical WPT systems operate in Industrial, Scientific, and Medical (ISM) bands (e.g., 6.78 MHz, 13.56 MHz, 40.68 MHz), such delays can induce hard switching, body diode conduction, and reverse current, degrading PCE.

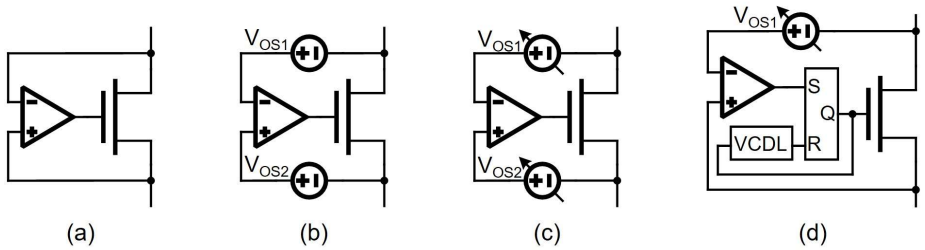

Figure 2.9 Active diode designs. (a) Basic. (b) Fixed delay compensation. (c) Adaptive delay compensation. (d) Hybrid delay compensation (VCDL: voltage-controlled delay line).

To address this, delay compensation techniques have been introduced. The idea is to intentionally add offset to the active-diode comparator, counteracting the error introduced by the delay, as shown in Figure 2.9 from (a) to (b). This can be implemented using switched bias-current branches [2.4][2.6][2.14][2.15][2.16] or static voltage offsets at the comparator input [2.17][2.18]. However, fixed delay compensation is sensitive to variations in coupling conditions, load impedance, and process, voltage, temperature (PVT) characteristics.

To overcome this, adaptive delay compensation has been proposed, as shown in Figure 2.9(c) [2.19][2.20]. This approach incorporates a feedback loop that dynamically adjusts the comparator offset based on the sampled voltages at the terminals of the power switch during switching edges. The loop often includes sample-and-hold (S&H) circuits, error amplifiers (EAs), voltage controlled current/voltage sources, etc. While feedback loops can adapt to coupling, loading, and PVT variations, their accuracy is bound by the intrinsic offset in the feedback loop components (e.g., EAs).

Both turn-on and turn-off of active diodes should have delay compensation, which is typically addressed by two switched branches in the comparator [2.19][2.20]. However, the alternation of delay compensation branches may induce multiple pulses at the output of the comparator when its input differential voltages are small [2.21]. To mitigate this, hybrid delay compensation schemes have been developed, which combine a comparator to determine turn-on timing, a voltage-controlled delay line (VCDL) to dictate turn-off timing, and a latch to hold the gate signal safely through one switching period, as shown in Figure 2.9(d) [2.22][2.23]. This ensures robust, glitch-free operation, at the cost of increased circuit complexity and potential startup concerns.

2.3.1.2 In-Situ Output Voltage Regulation

As the primary power source at RX, a WPT system must deliver high-quality DC output characterized by accurate voltage regulation under load and line variations, low output ripple, and fast transient response, while maintaining high efficiency and meeting size and cost constraints.

Instead of conventional two-stage architectures, state-of-the-art RX designs achieve in-situ output voltage regulation by directly modulating rectifier operation, eliminating the use of another DC-DC converter stage. Such designs are usually called single-stage RXs or regulating rectifiers. This approach not only reduces system form factor and fabrication cost by minimizing component count but also improves power conversion efficiency (PCE). Figure 2.10 illustrates four popular in-situ output voltage regulation methods: conduction-duty regulation, reverse-current regulation, multi-cycle pulse-width modulation (PWM) regulation, and hysteresis regulation.

In conduction-duty regulation [Figure 2.10 (b)] [2.24][2.25][2.26], the RX adjusts the conduction time of active diodes: under heavy load, conduction duration is extended; under light load, it is reduced. This method provides small steady-state voltage ripples because the rectifier operates continuously in every resonant period. However, it suffers from hard switching when turning off power switches, reducing PCE. Its load-transient response is also limited by the slow control loop.

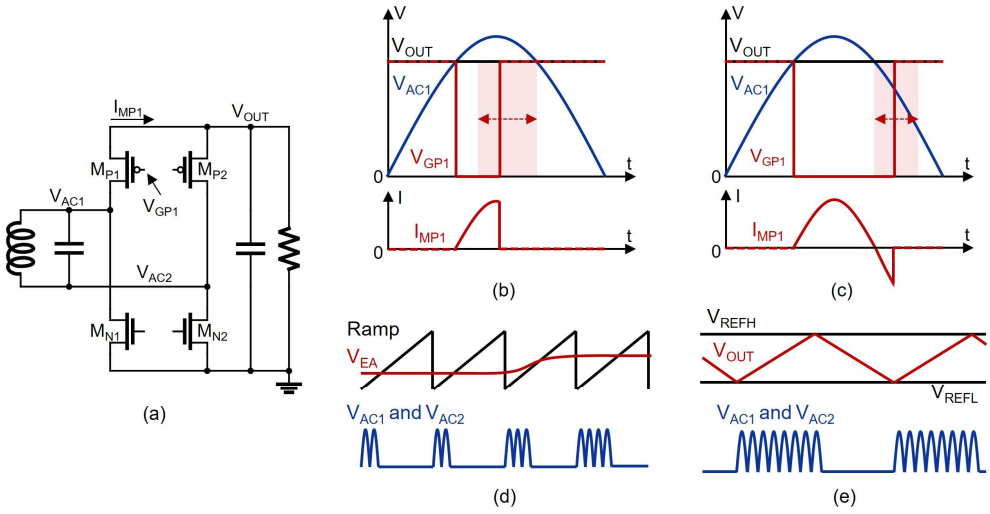

Figure 2.10 (a) A typical VM RX circuit, and in-situ output voltage regulation methods: (b) conduction-duty regulation, (c) reverse-current regulation, (d) multi-cycle PWM regulation, and (e) hysteresis regulation.

The reverse-current regulation method [Figure 2.10 (c)] [2.27] achieves regulation by intentionally introducing reverse conduction in active diodes during light load conditions and reducing it under heavier loads. Like conduction-duty regulation, it offers small steady-state voltage ripples but at the expense of lower PCE (due to reverse conduction) and limited transient performance.

In multi-cycle PWM regulation [Figure 2.10(d)], the output voltage, V_{OUT}, is compared to a reference voltage, generating an error signal, V_{EA}, which is further compared to a sawtooth ramp [2.8][2.28][2.29][2.30][2.31][2.32][2.33]. When V_{EA} > Ramp, the rectifier enters a freewheeling mode (0X mode) by turning on both M_{N1} and M_{N2}, interrupting power delivery during which V_{AC1} and V_{AC2} stay near zero. Otherwise, it normally conducts (1X mode). Under light loads, the 0X mode duty increases, while under heavy loads, it decreases. Compared with the first two methods, PWM regulation improves PCE by avoiding hard switching and reverse conduction. However, it introduces larger steady-state voltage ripples due to the 0X mode, and its analog control loop still limits transient speed due to loop stability constraints.

In hysteresis regulation [Figure 2.10(e)] [2.34][2.35][2.36][2.37][2.38][2.39], V_{OUT} is compared with two thresholds, V_{REFH} and V_{REFL}, forming a voltage window. When V_{OUT} surpasses V_{REFH}, the RX switches from 1X to 0X mode; when V_{OUT} falls below V_{REFL}, it switches back to 1X mode. This method avoids analog control loops, is usually unconditionally stable, and provides a fast transient response with minimal overshoot or undershoot. Its drawback is that the output ripple is determined by the hysteresis window, which is generally larger than in the other methods, constrained by practical issues such as noise, reference accuracy, and comparator metastability.

2.3.1.3 Single-Stage Multi-Output Generation

Implantable medical devices (IMDs) often require multiple power supplies to support different functional blocks at different voltage levels: for example, analog blocks typically demand higher voltages (e.g., 2.2 V) than digital blocks (e.g., 1.1 V), while neural stimulators may require compliance voltages ranging from 3 V to 10 V [2.40]. Hence, the WPT system must generate multiple regulated outputs at the RX side.

In a traditional two-stage RX architecture, this is achieved either by (1) employing multiple rectifier + DC–DC converter paths, or (2) using a single rectifier followed by a single-input multiple-output DC–DC converter [2.7]. While these methods stably isolate rectification and multi-output regulation, they suffer from large form factors, high fabrication costs, and reduced PCE.

To overcome these drawbacks, state-of-the-art RX designs employ in-situ multi-output voltage regulation, as illustrated in Figure 2.11. In [2.41], a path-selecting full-bridge rectifier is introduced, in which enabling either M_{P1} or M_{P2} directs power to V_{O1} or V_{O2}, respectively [Figure 2.11(a)]. However, this approach introduces extra conduction resistance from M_{P1} and M_{P2}. In [2.32][2.36][2.37][2.38][2.39][2.42][2.43], an upper-side-multiplexing full-bridge rectifier is proposed as a variation of the path-selecting scheme [Figure 2.11(b)]: V_{O1} is charged by enabling M_{P1} and M_{P2} as active diodes while disabling M_{P3} and M_{P4}; conversely, V_{O2} is charged by enabling M_{P3} and M_{P4} and disabling M_{P1} and M_{P2}. In [2.34], a parallel half-bridge rectifier is reported, in which one half-bridge charges V_{O1} while the other charges V_{O2} [Figure 2.11(c)]. Compared to the upper-side-multiplexing approach, this reduces the total number of

power switches and chip area but sacrifices the ability to deliver maximum output power to a single output owing to the lack of full-bridge operation.

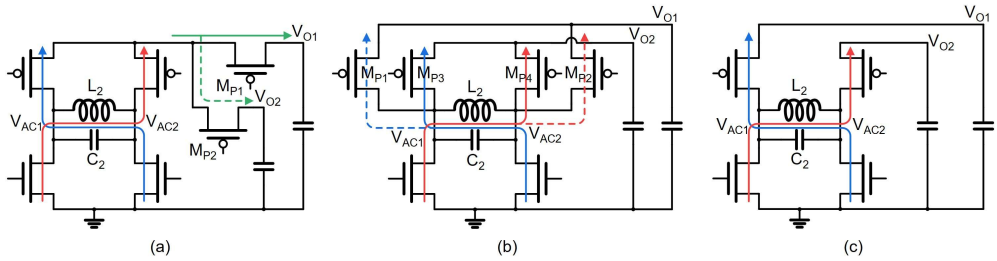

Figure 2.11 Single-stage dual-output VM RX structures. (a) Path-selecting full-bridge rectifier. (b) Upper-side-multiplexing full-bridge rectifier. (c) Parallel-half-bridge rectifier.

In summary, reported single-stage dual-output RX designs are predominantly based on full-bridge rectifiers. These architectures typically involve two to three resistive elements in the conduction loop, and both outputs tend to share similar optimal voltage domains due to their topological similarity.

2.3.2 Resonant-Current-Mode Rectifiers

Traditional RX designs are primarily based on voltage-mode (VM) rectifiers, such as full-bridge or half-bridge topologies. In 2016, the resonant-current-mode (RCM) rectifier was introduced [2.44][2.45], providing enhanced low-power receiving capability, also referred to as improved input sensitivity. This characteristic is particularly important for applications with highly variable coupling conditions, especially when coil miniaturization leads to reduced coupling strength.

Figure 2.12(a) and (b) illustrate the topology and operation of a VM full-bridge rectifier and an RCM rectifier [2.44][2.45], respectively. The operation of the RCM rectifier consists of two phases. In the resonance phase (Φ_1), M_N is turned on and M_P is turned off, allowing the L_2-C_2 tank to freely resonate and accumulate energy. Once sufficient energy has been stored (as determined by the RX controller), the rectifier switches to the charging phase (Φ_2), triggered when the RX coil current (I_2) reaches its peak. At this point, M_P is turned on and M_N is turned off, and L_2 acts as a current source to deliver the accumulated energy to the output. Upon I_2 becoming zero, the rectifier switches back to Φ_1.

Unlike VM rectifiers, which rely on a single-phase operation triggered by voltage thresholds, the RCM rectifier deals with the loop current (I_2) with a freely adjustable duty ratio between the two phases. In other words, it can operate without requiring a specific input-output voltage relationship. As a result, RCM rectifiers can cope better with the small input voltages that may arise under weak coupling conditions. Chapters 4 and 5 will further detail the differences between VM and RCM rectifiers and the associated design trade-offs.

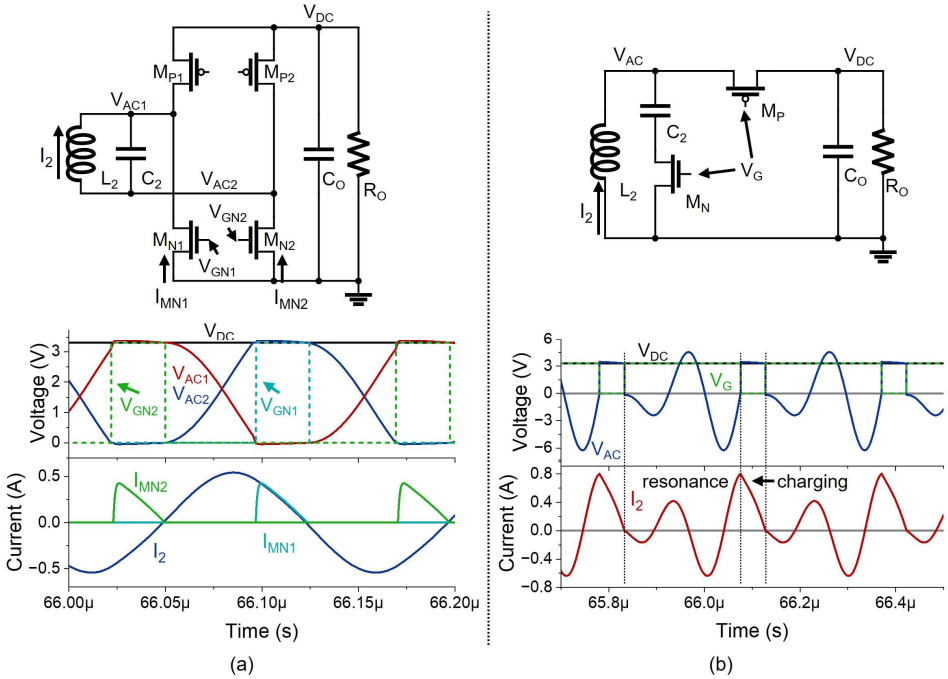

Figure 2.12 Topology and operation waveform of (a) voltage-mode full-bridge rectifier, and (b) resonant-current-mode rectifier.

2.4 Transmitter (TX) Design

The TX circuitry determines the overall WPT power level and plays a critical role in maximizing end-to-end efficiency. At the TX side, the most essential component is the power amplifier (PA). This section discusses the mainstream PA topologies, along with two key design considerations: soft switching and load matching.

2.4.1 Switching Power Amplifiers

For WPT applications, the PA must provide high output power with low output impedance and high power conversion efficiency (PCE), while linearity, crucial for audio and RF amplifiers, is not a concern. Consequently, the most adopted topologies are switching-mode PAs, particularly Class-D and Class-E [2.3].

Figure 2.13(a) illustrates the Class-D PA, which consists of a PMOS transistor (M_P) and an NMOS transistor (M_N), driving a series L_1-C_1 tank. In the first half cycle, M_P is on and M_N is off, allowing the tank to extract power from the supply, V_{IN}. In the second half cycle, M_N is on and M_P is off, enabling the tank to freewheel. In both cases, power is continuously transferred to the RX side. Ideally, the switching frequency matches the resonant frequency of the L_1-C_1 tank, resulting in a high power factor and efficient power delivery [2.1].

Figure 2.13(b) shows the Class-E PA, which comprises a large RF choke inductor

(L_C), an NMOS transistor (M_N), and a bypass capacitor (C_P), also driving a serial L_1-C_1 tank. L_C behaves as a near-DC current source. During the first half cycle, M_N is off, and the residual current from L_C and the tank ($I_{LC} - I_1$) flows through C_P. In the second half cycle, M_N is turned on, shorting C_P and redirecting the current. L_1, C_1, and C_P form a combined series-parallel resonance circuit, with a series-resonant frequency and a parallel-resonant frequency, also known as a multi-frequency network [2.3]. Given the topology and the multi-frequency load network, the Class-E PA can achieve not only zero-voltage switching (ZVS), which is also attainable in Class-D PAs, but additionally zero-voltage-derivative switching (ZVDS) under certain load conditions, resulting in high PCE.

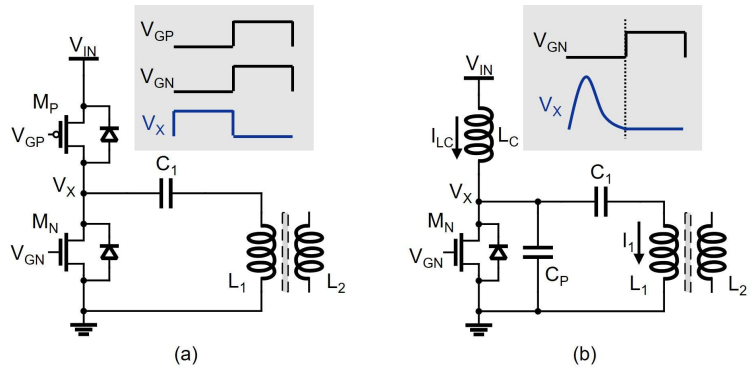

Figure 2.13 Power amplifier (PA) topologies. (a) Class-D PA. (b) Class-E PA.

Comparing the two, the Class-D PA employs two transistors, while the Class-E PA uses only one transistor but requires additional passive components. Class-D suffers from potential shoot-through between the transistors, necessitating dead-time control, whereas Class-E avoids this by relying on a single switch. On the other hand, given the same V_{IN}, the Class-E PA can achieve higher output power [2.46]. However, because Class-D does not adopt a multi-frequency network, it is more tolerant to load variations (both resistive and reactive) than Class-E [2.3].

For applications with variable load and coupling conditions, the Class-D PA offers superior reliability and a wider operating range compared to the Class-E PA. In contrast, the Class-E PA is more suitable for wireless fast-charging scenarios with relatively stable coupling and load conditions. Accordingly, the remainder of this thesis will focus on TX designs based on the Class-D PA.

2.4.2 Non-Ideal Switching

For high-power IMD applications, as discussed in Section 1.3, the TX-side PA may deliver a few Watts of output power. Minimizing losses in the PA stage is therefore essential to maximize efficiency. In a Class-D PA, the power transistors inherently exhibit non-zero on-resistance and parasitic capacitance, leading to unavoidable conduction and switching losses. Beyond these intrinsic factors, practical WPT scenarios further complicate matters, since the PA often drives a complex load network

with nonlinear RX behavior, imperfect resonance matching, etc. Such conditions alter the voltage–current relationship at the TX side and may introduce additional losses from hard switching and diode conduction during the Class-D switching deadtime.

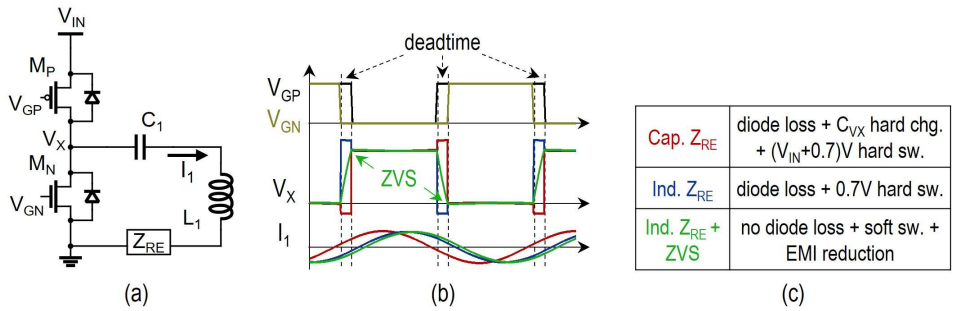

Figure 2.14 (a) Class-D PA structure with residual impedance (Z_{RE}) in the load network. (b) Voltage and current waveforms of the Class-D PA. (c) Loss characteristics under different Z_{RE} conditions.

Figure 2.14 shows the structure, waveform, and loss characteristics of a Class-D PA with different types of residual impedance (Z_{RE}) in its load network. Assuming M_P and M_N are driven with deadtime, L_1 and C_1 resonate perfectly at the switching frequency, and Z_{RE} is non-zero, three operating cases arise:

(1) **Capacitive Z_{RE}:** the TX loop current (I_1) leads the voltage (V_X). During the deadtime when V_X is initially low, both M_N and M_P are off. I_1 first discharges the parasitic capacitance at node V_X, making it negative, and then flows through M_N in diode mode once V_X drops below ground by one NMOS threshold voltage. This introduces additional diode conduction loss. When M_P turns on, V_X remains negative and must be rapidly charged up to V_{IN}, causing a hard turn-on of M_P with significant I×V loss. A similar mechanism occurs when deadtime begins with V_X initially high.

(2) **Largely inductive Z_{RE}:** I_1 lags V_X. During deadtime with V_X initially low, I_1 charges the parasitic capacitance at node V_X to V_{IN} + a PMOS threshold voltage before flowing through M_P in diode mode. When M_P turns on, V_X is rapidly discharged to V_{IN}. Compared with the capacitive case, this produces less energy loss, as the hard discharge only spans the PMOS threshold voltage drop. Similar behavior occurs when deadtime starts with V_X initially high.

(3) **Properly tuned inductive Z_{RE}:** in this favorable case, I_1 still lags V_X, but during deadtime with V_X initially low, it fully charges the parasitic capacitance at V_X to V_{IN} across the entire deadtime. Consequently, when M_P turns on, V_X equals V_{IN}, realizing zero-voltage turn-on of M_P. This eliminates diode conduction and hard-charging losses, and the energy used to charge V_X during one deadtime is recovered in the next, reflecting the lossless nature of L–C energy exchange. The same ZVS principle applies symmetrically when V_X is initially high.

From these observations, a practical and balanced design choice is to intentionally

add a small inductive Z_{RE} at the TX side to mitigate hard-charging and hard-switching losses, without adding complicated impedance compensation. Nevertheless, achieving full ZVS is always preferable. Without ZVS, diode conduction during deadtime can interact with parasitic inductance at V_X, causing ringing and high-voltage surges. These effects not only reduce efficiency but can also stress components and generate additional electromagnetic interference (EMI). Maintaining ZVS under varying load and coupling conditions therefore requires dedicated circuit techniques and adaptive control strategies [2.47][2.48][2.49][2.50].

2.4.3 Load Impedance Matching

As discussed in Section 2.4.1, the Class-D PA achieves maximum output power and near-unity power factor when operating at the resonant frequency of the L_1-C_1 tank. In practice, however, the resonant point can drift due to nonlinear RX behavior (e.g., discontinuous rectifier conduction), component distortion (e.g., coil shape change), aging effects, and other non-idealities. To align the load network's resonant frequency with the PA's switching frequency, load impedance matching techniques are employed. This is typically realized by introducing a tunable capacitor into the L_1-C_1 loop, which can be implemented in two ways: (1) a switched-capacitor branch with adjustable duty cycle [2.51][2.52][2.53], or (2) a MOS-capacitor with a voltage-controlled capacitance [2.54][2.55]. While these approaches ensure impedance matching at the TX side, they add extra components and additional power losses.

It is important to note that load impedance matching is fundamentally different from the ZVS condition discussed in Section 2.4.2. Impedance matching compensates for residual impedance (Z_{RE}) in the load network, where hard switching can still exist, while ZVS enables soft switching at node V_X under specific Z_{RE} conditions. Interestingly, certain circuit techniques can achieve both impedance matching and ZVS simultaneously [2.56][2.57][2.58].

2.5 System-Level Techniques

2.5.1 Global Control Loops

IMD applications often span a wide range of loads, from standby mode with μA-level load current to full-load operation with tens of mA. If the WPT system continuously operates in open loop at full power, as shown in Figure 2.15(a), the RX output can be regulated by a DC–DC converter, while the TX PA stage remains continuously active [2.59]. In this case, the end-to-end (E2E) efficiency drops significantly under light-load conditions.

To improve E2E efficiency, a global control loop can be introduced to adjust TX output power according to RX load conditions. Figure 2.15(b) shows such a closed-loop design [2.60]. Here, a regulating rectifier at the RX side monitors the output voltage and backscatters feedback data to the TX in real time. The data backscattering technique

will be detailed in Section 2.5.2. At the TX side, a DC–DC converter adjusts the supply voltage of the Class-D PA, thereby controlling the TX output power. With this scheme, the RX-side DC–DC converter can be eliminated. However, the added DC–DC stage at the TX introduces switching losses and off-chip components.

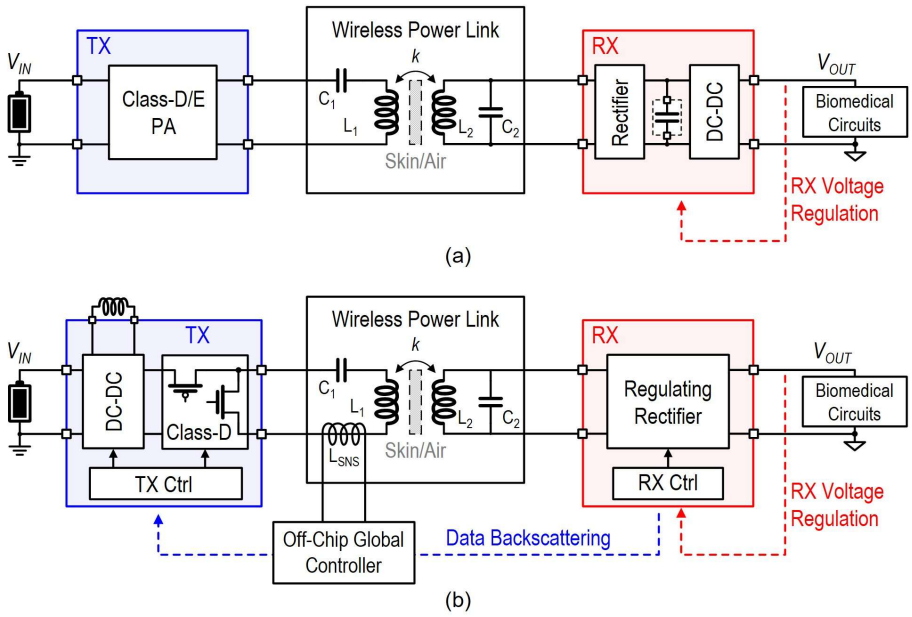

Figure 2.15 Multi-stage WPT systems. (a) Open-loop WPT system with output regulated by a DC–DC converter. (b) Closed-loop WPT system with TX power adjusted by a DC–DC converter.

To eliminate extra DC–DC stages, single-stage WPT systems have been developed, integrating both TX and RX into single-stage designs. Two representative implementations are shown in Figure 2.16, with their waveforms in Figure 2.17.

The first is a constant-off-time (COT) controlled WPT system [2.61][2.62]. When the output voltage (V_{OUT}) reaches its threshold (V_{REFH}), the RX sends a load-shift keying (LSK) signal (as 1-bit power-related data) to the TX. Upon demodulating this signal, the TX turns off its PA stage for a preset time, reducing the average TX output power without using a DC–DC converter. While this scheme provides simultaneous voltage regulation and TX power control, it requires a bulky sensing coil at the TX for demodulation, increasing system form factor and cost. Moreover, under heavy-load conditions, the constant off-time results in enlarged output voltage ripple and limits the maximum achievable output power.

The second is a hysteresis-controlled WPT system [2.63][2.64]. When V_{OUT} exceeds V_{REFH}, the RX sends an LSK signal that prompts the TX to switch from full-power to low-power mode by skipping three excitation pulses in every four switching periods, thereby lowering output power proportionally. During low-power mode, the RX receives minimal energy, and V_{OUT} is discharged by the load. Once V_{OUT} falls below the lower boundary V_{REFL}, the RX issues another LSK signal, prompting the TX

to return to full-power mode. Compared to the COT method, this scheme replaces the bulky sensing coil with an on-chip current sensor, improving integration and achieving better load regulation through hysteresis control. However, because the TX still leaks power during low-power mode, its E2E efficiency is expected to be lower than that of the COT system.

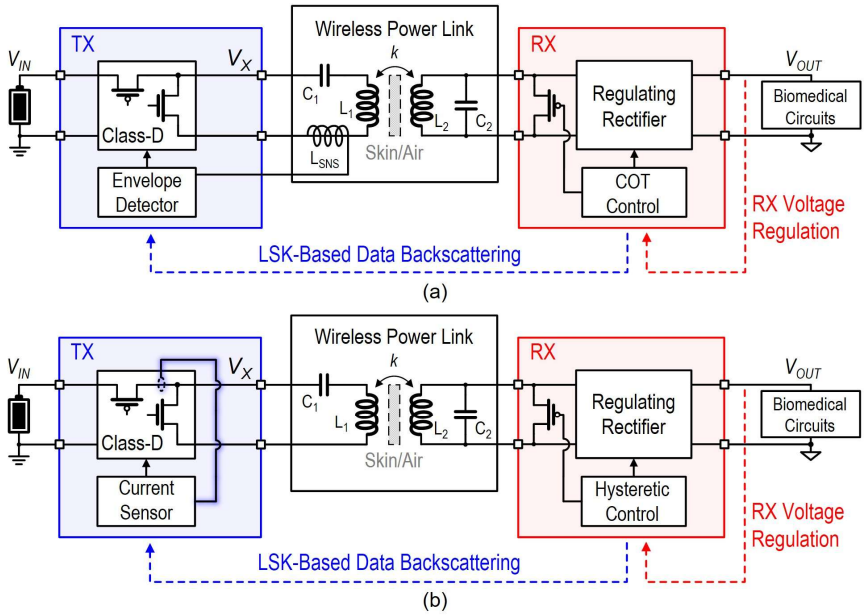

Figure 2.16 Single-stage WPT systems. (a) Constant-off-time (COT) controlled WPT system. (b) Hysteresis controlled WPT system. LSK: load-shift keying.

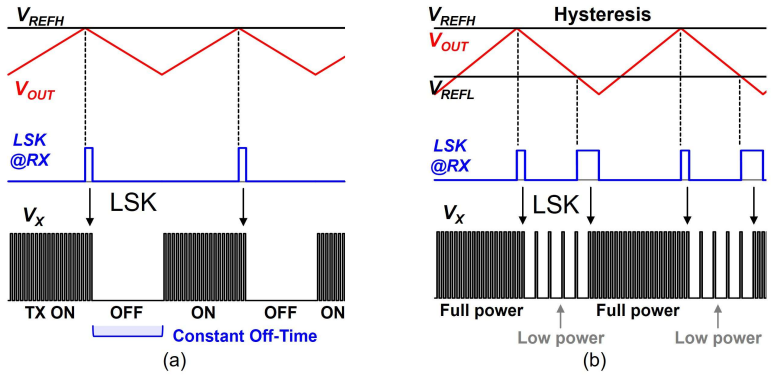

Figure 2.17 Operation waveform of (a) COT controlled WPT system and (b) hysteresis controlled WPT system.

In summary, global control methods for single-stage WPT systems enhance efficiency by coordinating TX power with RX load conditions. Nevertheless, existing schemes such as COT and hysteresis control face inherent trade-offs among E2E efficiency, output ripple, and load regulation, leaving room for further improvement.

Notably, under coupling variations, it is generally more robust to adopt nonlinear

control schemes (e.g., COT and hysteresis) that intentionally trade steady-state accuracy for transient response. In contrast, while linear (analog) control loops can achieve precise steady-state regulation, they must be slowed down to maintain stability as the coupling varies, resulting in suboptimal transient performance.

2.5.2 Data Backscattering

To accomplish closed-loop WPT systems, TX must acquire load information from the RX side. A straightforward solution is to use a dedicated data communication link, such as Bluetooth [2.65][2.66], but this requires additional hardware and increases power consumption at RX.

An alternative is through-power-link backscattering techniques, which transmit RX data using load-shift keying (LSK) [2.1]. This passive method modulates the RX reflected impedance observed at the TX by replacing the rectifier with a single low-resistance switch, as shown in Figure 2.18(a). Since the rectifier normally presents a relatively large equivalent input impedance, introducing a low-resistance switch creates a load-transient effect (with detailed expressions given in Section 2.2.2) [2.67].

Figure 2.18(b) illustrates the TX response when the RX toggles between normal conducting mode (1X mode, defined in Section 2.3.1) and LSK mode. In LSK mode, the switch shorts the RX coil (L_2), interrupting the L_2-C_2 resonance. Consequently, the reflected impedance at the TX is reduced compared to the 1X mode, and the TX loop current (I_1) increases significantly.

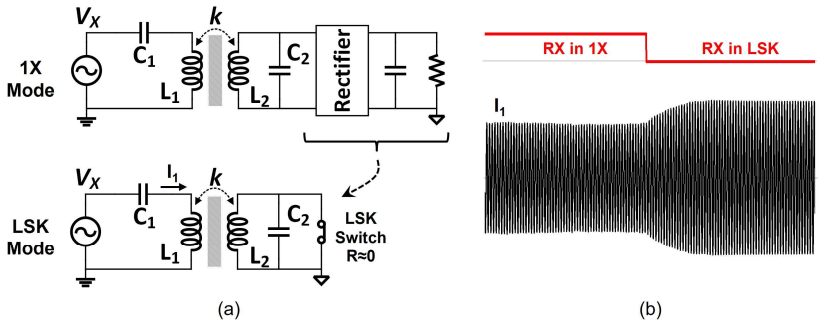

Figure 2.18 (a) circuit configuration and (b) waveform of typical LSK data backscattering.

At the TX side, RX data can be demodulated by detecting this current increase. Various implementations are possible, such as using a sensing coil [2.16], integrating an on-chip current sensor [2.64], or measuring the voltage amplitude across the resonant capacitor C_1, as will be introduced in Chapter 4.

It is worth noting that LSK is not limited to short-circuit modulation. Alternative approaches include adjusting the RX-side resonant matching [2.68] and using an open-circuit scheme [2.69].

2.6 Conclusion and Outlook

This chapter presents prior designs and discusses the key design considerations of wireless power transfer (WPT) systems, covering the inductive resonant link, receiver (RX) circuits, transmitter (TX) circuits, global power control methods, and through-power-link data backscattering. Clear development trends are observed: from multi-stage to single-stage RX/TX architectures, from open-loop to closed-loop control, and from reliance on numerous off-chip components to more highly integrated solutions. These advancements are driven by the need for higher power efficiency, improved output quality, smaller form factors, and reduced fabrication cost in implantable medical device (IMD) applications.

Despite this progress, critical challenges remain. First, coupling variation remains a largely unresolved problem. Most reported works propose circuit innovations under the assumption of constant coupling, which is unrealistic in practice. Whether state-of-the-art designs remain functional under varying coupling conditions, and if not, what new techniques are required, are central questions to be addressed. Second, current implementations are not sufficiently miniaturized for IMD use. Most still rely on centimeter-scale coils, whereas IMDs are mostly constrained to millimeter-scale dimensions. Bridging these gaps demands circuit innovations and more tailored design trade-offs.

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Chapter 3 Voltage-Mode Receivers

As discussed in Chapter 2, most reported wireless power transfer (WPT) systems employ voltage-mode (VM) receiver (RX) designs based on full-bridge rectifiers (FBRs). With active diodes and in-situ output voltage regulation, FBRs can achieve >90% power conversion efficiency (PCE) without needing a voltage regulator. However, their voltage conversion ratio (VCR), defined as the DC output voltage relative to the AC input voltage amplitude, is less than 1. This limits their operating range and output voltage in the presence of coupling variations or when miniature RX coils are used, as is typical in implantable medical device (IMD) applications, thereby making VCR a fundamental bottleneck for coupling-robust operation in FBR-based VM receivers.

To address this limitation, this chapter explores the voltage doubler (VD) topology, which theoretically offers twice the VCR of an FBR. A regulating VD is first introduced as a proof of concept. It is then extended to a dual-output VD that achieves independent regulation of its two outputs, enabling greater functionality without increasing hardware cost.

3.1 A Regulating Voltage Doubler[1]

3.1.1 Motivation

Figure 3.1 shows a biomedical WPT system and representative RX topologies. To overcome the low VCR of FBRs, [3.1] introduced a 1×/2× regulating rectifier, as shown in Figure 3.1(c). By reconfiguring it either as an FBR or a voltage doubler, this design improves the VCR from < 1 to between 1 and 2. However, it requires five power switches and two output capacitors, which increase its power losses, chip area and component count.

To improve VCR without these drawbacks, a regulating voltage doubler (VD) is proposed, as shown in Figure 3.1(d). It achieves a theoretical VCR of 2 using only two power switches and two output capacitors, thus reducing both losses and chip area.

The regulating VD operates in two modes for in-situ output regulation: a 2X mode

[1]based on: T. Lu and S. Du, "A Single-Stage Regulating Voltage-Doubling Rectifier for Wireless Power Transfer," in IEEE Solid-State Circuits Letters, vol. 6, pp. 29-32, 2023, doi: 10.1109/LSSC.2023.3239691.

and a 0X mode. When the output requires energy, it operates in 2X mode as a full-wave voltage doubler, charging C_{O1} when $V_{AC1} > V_{OUT}$ and C_{O2} when $V_{AC1} < 0$. When the output does not require energy, it transitions to 0X mode, lowering its input power to maintain high efficiency, as will be detailed in Section 3.1.3. Notably, V_{AC2} is predominantly a DC voltage at $V_{OUT}/2$, rather than an AC waveform as in the FBR, because it is clamped by the two output capacitors.

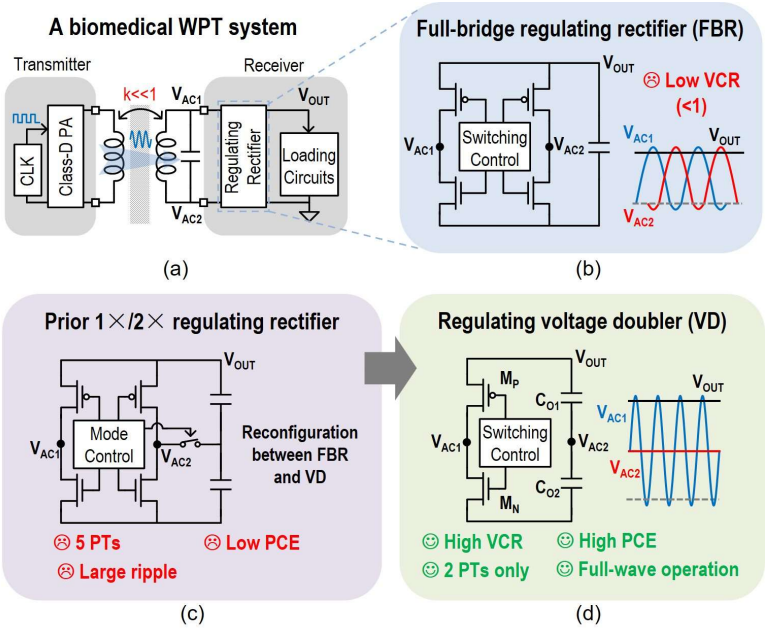


Figure 3.1 (a) Biomedical WPT system diagram. (b) FBR. (c) 1×/2× regulating rectifier. (d) Regulating VD.

3.1.2 System-Level Simulation

To highlight the differences between a VD and an FBR, system-level simulations were performed using the representative series–parallel resonance matching configuration shown in Figure 3.2. Depending on the RX topology, the equivalent input impedance seen from the resonant tank, R_{CKT}, differs: for the VD, it is $R_{OUT}/8$, while for the FBR it is $R_{OUT}/2$ [3.2]. This, combined with the difference in their VCRs, leads to different WPT performance.

Table 3.1 lists the simulation parameters. A power carrier frequency of 6.78MHz was selected, which is in the Industrial, Scientific and Medical (ISM) band. The coupling coefficient is chosen to represent a medium-to-weak coupling condition, which is commonly encountered in implantable systems due to tissue separation and misalignment between the external TX and the implantable RX [3.2]. The chosen TX and RX coil parameters reflect reported IMD implementations, in which centimeter-scale external coils are paired with significantly smaller and more resistive implantable coils [3.2][3.3][3.4][3.5][3.6][3.7]. The output voltage and load resistance are chosen to

be consistent with typical IMD supply rails and power consumption levels.

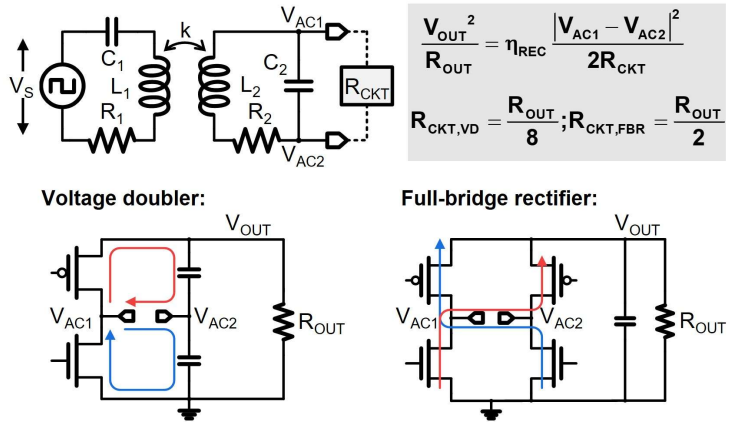


Figure 3.2 WPT system model with either a VD or an FBR.

Table 3.1 Parameter settings in the WPT system model.

Parameters		Values
Source peak-to-peak voltage, $\|V_S\|$		1.8 V
Carrier frequency, f_C		6.78 MHz
Coupling coefficient, k		0.05 (variable)
TX coil	**Inductance, L_1**	1 μH
	Resistance, R_1	0.3 Ω
RX coil	**Inductance, L_2**	0.2 μH (variable)
	Resistance, R_2	1 Ω
Output voltage, V_{OUT}		3.3V (variable)
Output resistance, R_{OUT}		Variable

Figure 3.3 shows the simulated results:

- P_{OUT} vs. V_{OUT}: The VD exhibits a wider operating range than the FBR while achieving comparable maximum power. The VD remains functional when the FBR cuts off (under high-V_{OUT} conditions).
- P_{OUT} vs. coupling factor k: The VD begins harvesting power at a coupling factor 2× lower than the FBR, thanks to its higher VCR, thereby improving weak-coupling performance.
- P_{OUT} vs. RX coil inductance L_2: With $L_2 < 100$ nH, the VD sustains significant power delivery, whereas the FBR's output drops sharply. This demonstrates the VD's suitability for coil miniaturization.
- Open-loop V_{OUT} vs. output resistance R_{OUT}: Under heavy-load conditions (small R_{OUT}), the FBR achieves slightly higher V_{OUT} than the VD [3.2]. However, under light-load conditions, more typical for IMDs, the VD produces much higher V_{OUT}, benefiting from its high-VCR nature.

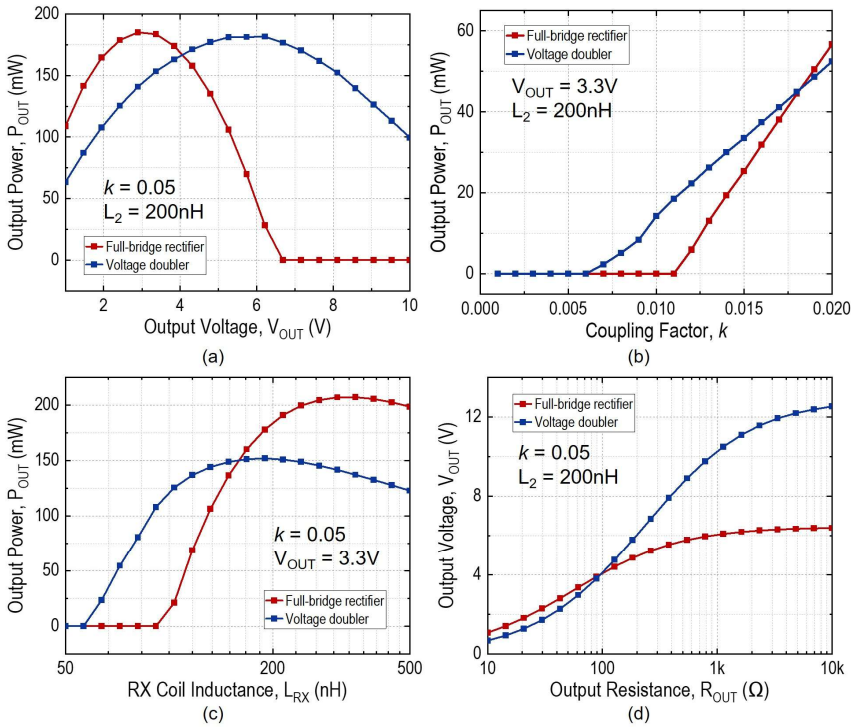


Figure 3.3 Simulated performance comparison between VD and FBR.

The simulation results confirm that the VD outperforms the FBR in terms of operational range, weak-coupling performance, and coil miniaturization, while maintaining comparable peak power delivery. These advantages make the regulating voltage doubler a promising candidate for practical IMD-oriented WPT systems.

3.1.3 Circuit Implementations

Figure 3.4 shows the system architecture of the proposed regulating voltage doubler, which consists of a power stage, a hysteresis output controller, and a self-start-up block. The use of hysteresis output control is for its simplicity, robustness, and fast transient response, compared to traditional pulse-width modulation schemes.

In the power stage, two power switches, M_P and M_N, are driven by the buffered outputs of two delay-compensated comparators, CMP_P and CMP_N, respectively. When the rectifier is enabled (2X mode), both switches operate as active diodes. The output capacitor C_{O1} is charged in the positive half-period of V_{AC}, and C_{O2} is charged in the negative half-period, forming a full-wave operation. C_{O1} and C_{O2} are stacked to achieve a doubled output voltage ($V_{OUT} = 2V_M$). A transmission-gate switch, S_{OVP}, is employed between the two AC input nodes to short the L_2-C_2 tank when the rectifier is disabled (0X mode). In this mode, the interrupted L_2-C_2 tank will turn down most of the power received from the TX, thus maintaining high RX efficiency.

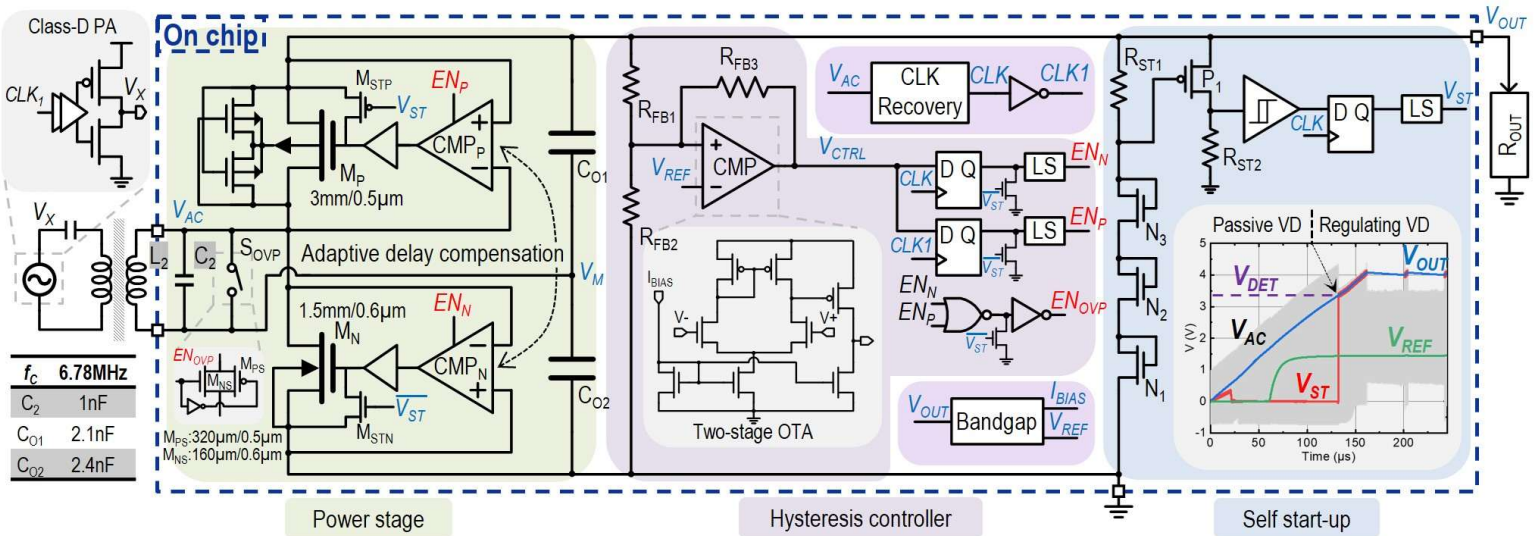


Figure 3.4 System architecture of the proposed regulating voltage doubler.

3.1.3.1 Hysteresis Output Controller

In this design, the output voltage, V_{OUT}, is regulated to 4 V by a hysteresis-based pulse-skipping controller. This voltage level can be adjusted upon application needs. The divided version of V_{OUT} is compared with a 1.45 V reference voltage V_{REF}, which is generated by an on-chip constant-current bandgap reference with an addition of a resistive output branch. The comparator, CMP, is a two-stage OTA with a positive feedback resistor, R_{FB3}. The hysteresis window is thus defined as

$$\mathrm{Hyst} = V_{REF}\left(\frac{R_{FB1} + R_{FB2}||R_{FB3}}{R_{FB2}||R_{FB3}} - \frac{R_{FB1}||R_{FB3} + R_{FB2}}{R_{FB2}}\right) \tag{3.1}$$

which is less than 50 mV in this work. Notably, the output ripple specification is application dependent. In practice, it must be designed by simultaneously considering load circuit requirement, filtering capacitance, load power range, and system power consumption budget.

When V_{OUT} reaches the upper hysteresis threshold, the output of CMP, V_{CTRL}, goes high. The rectifier will be disabled (0X mode) by setting M_P and M_N at V_{OUT} and V_{SS}, respectively, and S_{OVP} is turned on to limit the amplitude of V_{AC}. When V_{OUT} reaches the lower hysteresis threshold, V_{CTRL} goes low to enable the rectifier (2X mode); M_P and M_N work as active diodes, and S_{OVP} is turned off. In order to realize a smooth mode switch between 2X and 0X, a synchronized clock signal, CLK, is recovered from V_{AC} to synchronize EN_P, EN_N, and EN_{OVP} by the moment when V_{AC} equals V_M. Therefore, the mode switching happens when no conduction path exists between V_{AC} and V_{OUT}, so V_{AC} is not distorted and the resonance power can be saved.

3.1.3.2 Self-Startup Setting

The self-start-up of the rectifier is achieved by biasing M_P and M_N as diode-connected MOSFETs. As a result, the rectifier works as a passive VD until V_{OUT} attains a certain voltage V_{DET}. V_{DET} is designed around 3.4 V, which is sufficient for circuit operation but lower than the normal regulation level. It is defined by MOSFET's threshold voltages:

$$V_{DET} = V_{TH,N1} + V_{TH,N2} + V_{TH,N3} + V_{TH,P1} \tag{3.2}$$

where N_1 is a 2-V device, and N_2, N_3, and P_1 are 5-V devices. R_{ST1} and R_{ST2} are current-limiting resistors to reduce the quiescent power consumption of the start-up block. A Schmitt trigger is employed to avoid potential multi-startup issues caused by the slight drop in V_{OUT} when the rectifier just becomes active.

3.1.3.3 Adaptive Delay Compensation in Active Diodes

When the rectifier works at ISM band frequencies such as 6.78/13.56 MHz or higher, the propagation delay, typically several nanoseconds, of active diodes

(CMP_P/CMP_N and gate drivers) will induce significant delayed conduction and reverse currents in M_P and M_N. To compensate for this delay, various techniques such as current injection [3.8], [3.9], voltage offset [3.10], etc., have been reported. However, these usually operate the rectifier in open-loop without considering output regulation. In this work, an adaptive current injection technique is adopted with an offset locking technique, achieving regulation-compatible delay compensation. The circuit implementation of CMP_P is divided into three parts, as shown in Figure 3.5, Figure 3.6, and Figure 3.8, respectively.

Figure 3.5 shows the main comparator stage in CMP_P, comparing V_{AC} and V_{OUT}. It adopts a fully-differential push-pull common-gate comparator (on the left) for its fast, symmetric large-signal response and applicability around supply rails (V_{OUT}). Two pairs of switched current sources (ON-pair and OFF-pair) can be used to unbalance the common-gate stage. For example, when the ON-pair is enabled, branches b and c will have a stronger pull-down current (I_{BIAS} + $I_{ON\text{-}pair}$) than branches a and d (I_{BIAS}). Thus, seen from the comparator's output node V_{GP}, the pull-down current is larger than the pull-up current in equal-input condition (V_{AC} = V_{OUT}). This means that V_{GP} will switch when V_{AC} is a bit lower than V_{OUT}. This time-advanced edge compensates for the propagation delay of CMP_P and the gate driver and achieves M_P's zero-voltage turn-on. A current-based compensation scheme was chosen because it can achieve wider dynamic range compared to voltage-offset-based methods.

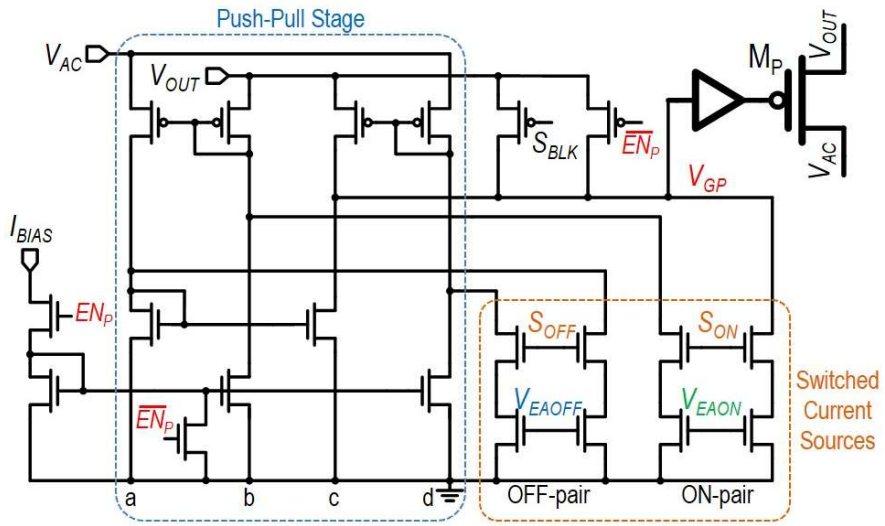


Figure 3.5 Circuit implementation of the push-pull comparator with switched biasing in CMP_P.

The next task is to control the delay compensation by appropriately driving the switched current sources. Given variable coupling and load conditions, this control should be adaptive [3.8][3.9]. The propagation delay is detected by a delay-to-voltage converter formed by sample-and-hold circuits and error amplifiers (EAs), as shown in Figure 3.6. The detailed waveforms of this process are shown in Figure 3.7. When the rectifier operates with insufficient delay compensation (Case 1 in Figure 3.7), M_P turns

on and off too late, and the delay-to-voltage converter yields a sampled V_{AC} voltage at turn-on, V_{HDON}, higher than V_{OUT} and a sampled V_{AC} voltage at turn-off, V_{HDOFF}, lower than V_{OUT}. Therefore, the EA drives its outputs, V_{EAON} and V_{EAOFF}, to increase the currents generated by the switched current sources. In steady-state, the delay can be near-optimally compensated regardless of coupling/loading/PVT variations [3.8], as reflected by Case 2 in Figure 3.7.

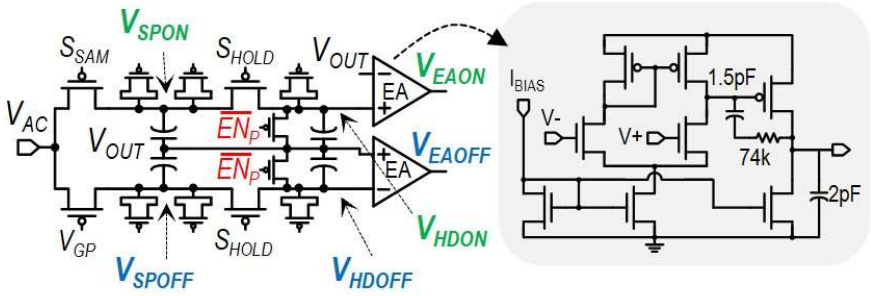


Figure 3.6 Circuit implementation of the delay-to-voltage converter in CMP_P.

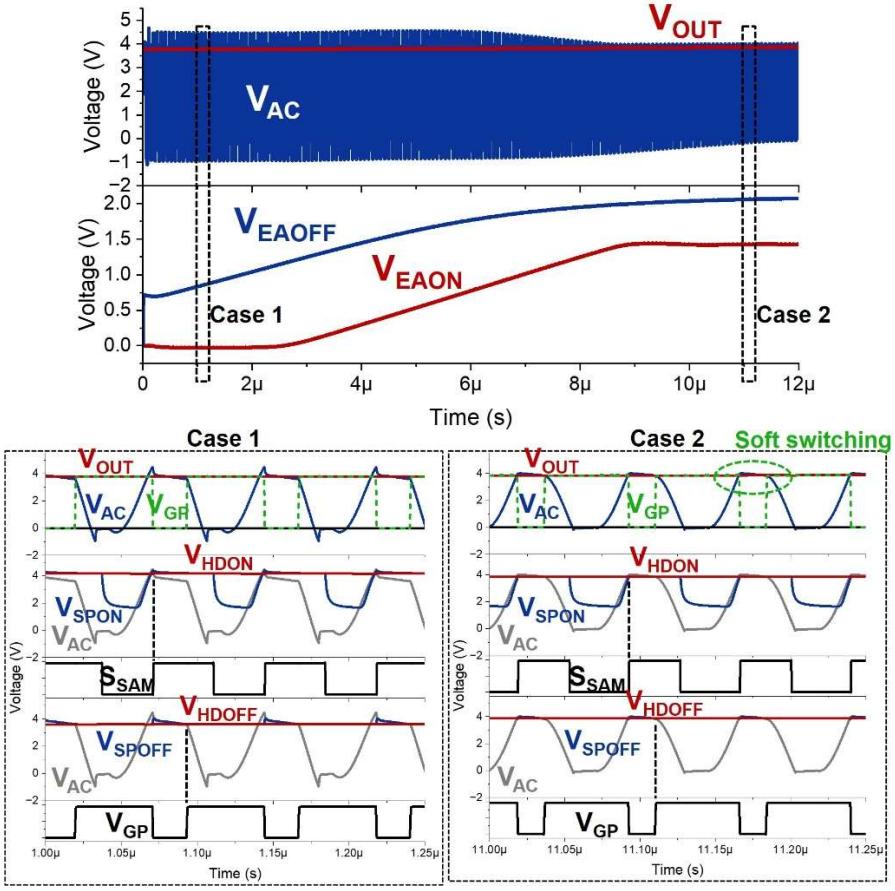


Figure 3.7 Detailed operation waveform of the adaptive delay compensation process in CMP_P.

Since the adaptive delay compensation forms a negative feedback loop, loop stability must be ensured. The switched current source, push–pull stage, and sample-and-hold circuit can be modeled as a voltage-to-current block, a current-to-delay block, and a delay-to-voltage block, respectively. Together, they can be approximated as a voltage-to-voltage gain stage whose overall gain is designed to be smaller than unity. As a result, the EA dominates the loop dynamics, and its Miller compensation capacitor establishes the dominant pole and ensures sufficient phase margin. This behavior was verified by making transient and Monte Carlo simulations across process corners and with varying load and coupling conditions.

In 0X mode, CMP_P and CMP_N are off, and their outputs are locked to turn off M_P and M_N. To prevent leakage-induced drift in V_{HDON} and V_{HDOFF}, which may cause a long settling time when returning to 2X mode, they are shorted to V_{OUT} and V_{SS} in CMP_P and CMP_N, respectively. The EA outputs therefore remain near their common-mode levels, close to the optimal compensation point. An alternative, maybe better, approach reported in the literature is the use of a dedicated voltage-holding circuit [3.11]. The input pair of EAs was implemented by large devices to reduce the effect of mismatch. Thus, when the rectifier enters 2X mode again, CMP_P and CMP_N can still provide mostly proper offset and have a short settle time.

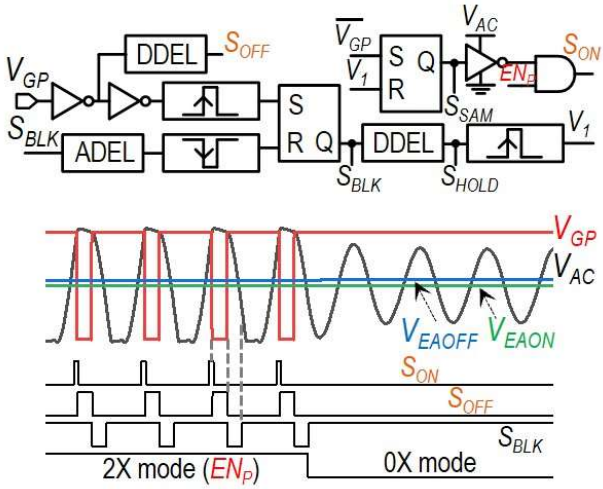


Figure 3.8 Circuit implementation of the logic timing generator in CMP_P (DDEL: digital delay cell) and corresponding waveforms.

The timing of the switched current sources is controlled by S_{ON} and S_{OFF} via a logic timing generator, as shown in Figure 3.8. To avoid energy waste by giving turn-on offset too early, S_{ON} is a short pulse which ensures that the current sources are only enabled when V_{AC} is rising (or falling) and is close to V_{OUT} (or V_{SS}) in CMP_P (or CMP_N). This is done by (1) designing the duration of S_{BLK} to be no shorter than 30 ns by an analog delay cell (ADEL) to freeze S_{ON}, when V_{AC} is in its falling (or rising) edge in CMP_P (or CMP_N) and (2) using the V_{AC}-supplied inverters [3.8].

3.1.4 Measurement Results

The proposed rectifier was fabricated in a 180-nm BCD process with standard 1.8-V/5-V devices, occupying a silicon area of 0.3/2.7mm^2 without/with on-chip capacitors, as shown in Figure 3.9(a). C_2 (1nF) was implemented using MIM capacitors, while C_{O1} (2.1nF) and C_{O2} (2.4 nF) were implemented using MOS capacitors stacked by MIM capacitors. Figure 3.9(b) shows the measurement setup when the rectifier is in the steady state. Figure 3.9(c) shows the measured coil sizes and parameters. The inductance, L_1 and L_2, and quality factors, Q_1 and Q_2, were measured by an impedance analyzer at 6.78MHz. To achieve cleaner signals and better high-frequency noise filtering, two additional off-chip capacitors (100nF and 2.2µF) were added at the DC output nodes in the test board.

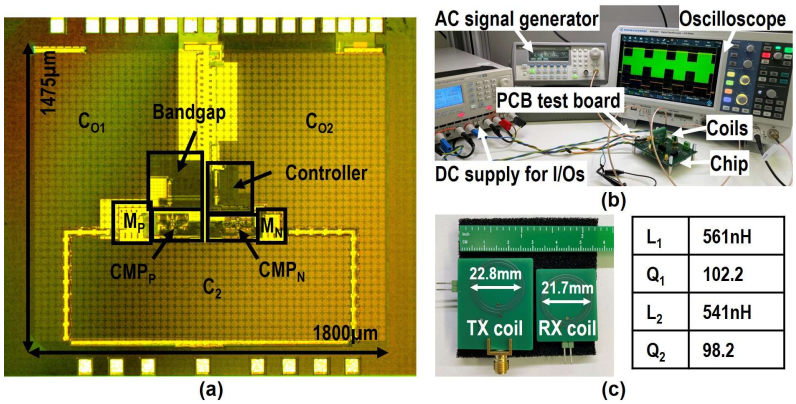


Figure 3.9 (a) Chip micrograph of the proposed rectifier. (b) Measurement setup during steady state. (c) Measured coil sizes and parameters.

Figure 3.10 shows the measured steady-state waveforms of the rectifier when R_{OUT} is 2 kΩ (equivalent to I_{OUT} = 2 mA). The rectifier regulates V_{OUT} at 4V by pulse-skipping control [Figure 3.10(a)]. When it is in 2X mode, the proper operation of CMP_P and CMP_N can be observed [Figure 3.10(b)], where V_{AC} has no obvious ringing/spark at the turn-on/off moments of M_P and M_N. As seen from Figure 3.10(c) and (d), V_{AC} is not distorted at the mode-changing moments and the previously generated offsets are maintained in CMP_P and CMP_N after 0X mode.

Figure 3.11 shows the measured load-transient waveforms of the rectifier when R_{OUT} changes between 1 kΩ (I_{OUT} = 4 mA) and 3 kΩ (I_{OUT} = 1.33 mA) in both directions. The duty ratio of 2X/0X mode changes, as seen from the signal EN_{OVP}; however, the hysteresis window of V_{OUT} is less than 50 mV in both transient cases, indicating that the output regulation is robust despite loading variations [3.12].

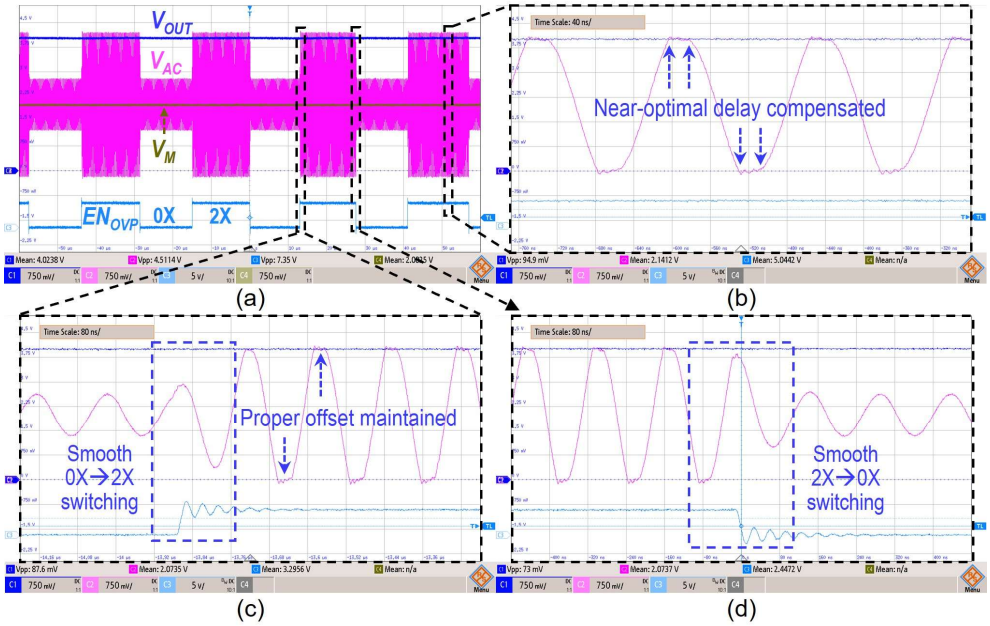


Figure 3.10 (a) Measured steady-state waveforms of the rectifier when R_{OUT} is 2 kΩ; zoomed-in waveforms (b) in 2X mode; (c) 0X to 2X; and (d) 2X to 0X.

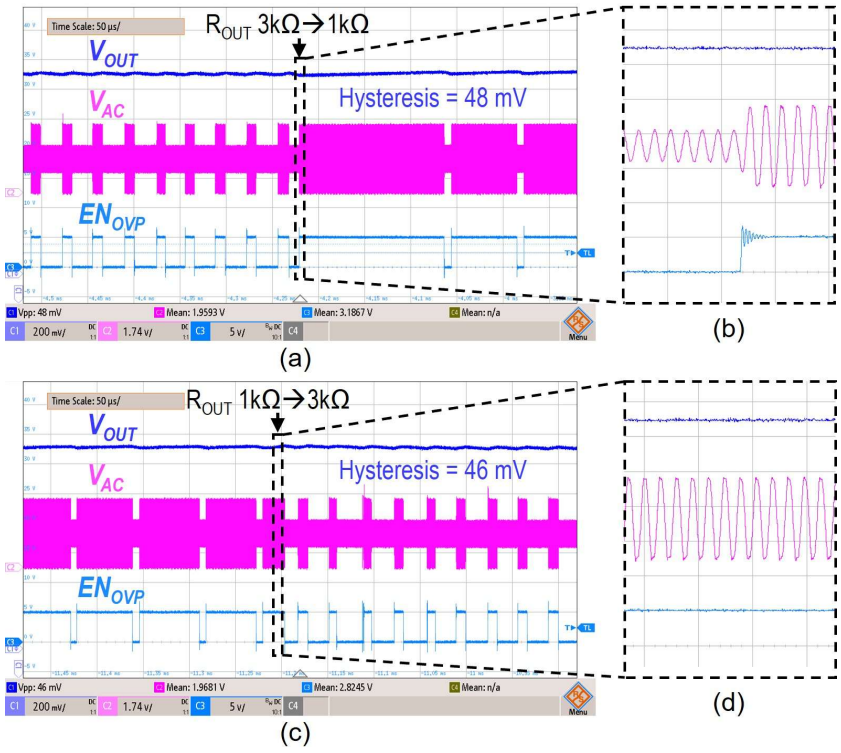


Figure 3.11 Measured load-transient waveforms of the rectifier when R_{OUT} changes (a-b) from 3 to 1 kΩ and (c-d) from 1 to 3 kΩ.

Figure 3.12 shows the measured cold-startup waveform of the rectifier. As described earlier, the rectifier first operates in the passive VD mode to charge up V_{OUT} until V_{ST} becomes logic high. Then, it switches to the normal regulating VD mode, where the V_{AC} envelope becomes smaller, indicating active diode operation.

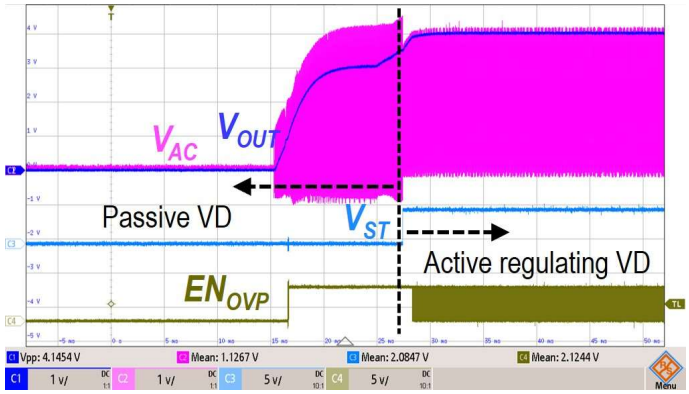


Figure 3.12 Measured cold-startup waveform of the rectifier.

Figure 3.13 shows the measured PCE, output power (P_{OUT}), and VCR of the rectifier under different loading conditions. The WPT transmitter is tuned to ensure that enough power can be provided. The peak PCE is achieved at 90.6% when P_{OUT} is 79.8 mW. The PCE keeps higher than 86.4% and the VCR keeps higher than 1.6 over the entire measured R_{OUT} range from 100Ω (I_{OUT} = 40 mA) to 4 kΩ (I_{OUT} = 1 mA). The maximum P_{OUT} reaches 159.2 mW.

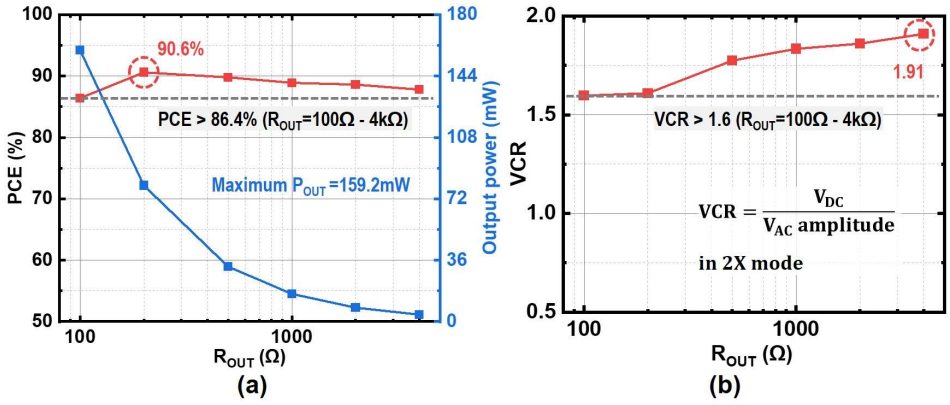


Figure 3.13 Measured (a) PCE, P_{OUT}, and (b) VCR of the rectifier versus R_{OUT}.

3.1.5 Conclusion

In Section 3.1, a 6.78-MHz regulating voltage doubler is proposed. Compared with state-of-the-art designs in Table 3.2, it achieves a VCR of up to 1.91, enhancing the overall WPT voltage gain. Using only two power transistors, adaptive delay-compensated comparators, a regulation-compatible offset-locking technique, and zero-

voltage mode switching, the design delivers high PCE across a wide load range, reaching a peak of 90.6%. The rectifier provides a maximum output power of 159.2 mW, sufficient for most bio-implant applications. In addition, the loading-insensitive hysteresis controller with a sub-50-mV window regulates V_{OUT} at 4 V and suppresses undershoot/overshoot during load transients.

Table 3.2 Comparison with state-of-the-art designs.

	This work	**TBCAS'20 [3.13]**	**SSCL'20 [3.10]**	**JSSC'19 [3.14]**	**JSSC'15 [3.3]**
Technology	180nm BCD	180nm CMOS	180nm CMOS	350nm CMOS	350nm CMOS
Working frequency	6.78MHz	1-10MHz	13.56MHz	1MHz	13.56MHz
Chip area	2.7mm^2	6mm^2	0.2mm^2	2.4mm^2	3.1mm^2
Topology	Full-wave VD	FBR	FBR	CM rectifier/HBR	1X/2X rectifier
Number of PTs	2	4	4	5	5
Active diode delay compensation	Adaptive switched biasing + offset locking	Adaptive switched biasing	Adaptive input voltage offset	No compensation	Fixed switched biasing
Output regulation	Hysteresis-based pulse skipping	PFM+PWM	No regulation	Conduction reverse current	1X/2X mode switching
Output voltage	4V	2.5V	1.9V*	3V	3.6V
Output ripple	48mV (Hyst. defined)	19.6mV	N/A	100mV*	150mV*
Load regulation	0.17%	0.46%	N/A	0.8%	3.1%
Line regulation	0.37%	0.48%	N/A	1.8%	N/A
ΔV in load-transient	Unobservable	80mV*	N/A	1V	112mV
Maximum P_{OUT}	159.2mW (R_{OUT}=100Ω)	65mW	7.2mW*	18mW	102mW
VCR	1.60-1.91 (R_{OUT}=100Ω-4kΩ)	0.86*	0.91	1.4*	1.3*
Peak PCE	90.6% @79.8mW	90.7% @32.5mW	90.7% @7.2mW	75% @18mW	92.6% @60mW

*Estimated from reference.

3.2 A Dual-Output Regulating Voltage Doubler[2]

Though the regulating voltage doubler (VD) effectively improves VCR, it only supports a single output while requiring two output capacitors, necessitating further power conditioning stages to meet multi-output requirements. This section introduces a dual-output VD derived from the regulating VD, extending its functionality without additional components and thereby improving component utilization.

3.2.1 Motivation

In single-stage RX structures, multiple outputs can be achieved by introducing additional power branches, as discussed in Section 2.3.1.3. While these circuits satisfy the multi-output requirement, they are all based on FBRs, limiting the VCR to < 1. Furthermore, they require at least six power transistors to maintain full-wave operation. Also, they always have at least two power transistors in the current path, resulting in high conduction losses.

To address these limitations, the dual-output regulating voltage doubler (DOVD) is proposed, as shown in Figure 3.14. It features only one conducting power transistor at a time, achieves a theoretical VCR of 2 at the output V_{O1}, and operates in a full-wave mode. With only two transistors in total, it also enables a compact chip area.

Interestingly, the DOVD concept arises from a straightforward design progression (Figure 3.14): (1) A traditional dual-output configuration employs two rectifiers. → (2) The simplest rectifier consists of a diode. → (3) To regulate both outputs, full-wave operation is preferable, assigning one polarity to each output. Following this reasoning, the DOVD was created, combining dual-output functionality with the high-VCR benefit of the voltage doubler.

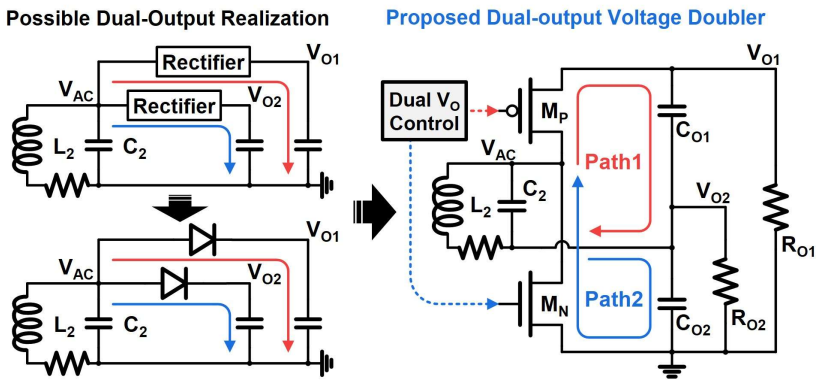


Figure 3.14 Proposed dual-output voltage doubler.

[2]based on: T. Lu, K. A. A. Makinwa and S. Du, "A Single-Stage Dual-Output Regulating Voltage Doubler for Wireless Power Transfer," in IEEE Journal of Solid-State Circuits, vol. 59, no. 9, pp. 2922-2933, Sept. 2024, doi: 10.1109/JSSC.2024.3378675.

3.2.2 Operation Principle

The power stage of the DOVD can be naturally divided into an upper path (Path 1) and a lower path (Path 2). It employs parallel pulse-frequency modulation (PPFM) with two independent hysteresis windows to regulate V_{O1} and V_{O2}. A lower-level hysteresis window regulates V_{O2}: when V_{O2} falls below the lower boundary, C_{O2} is charged via the lower path; when V_{O2} exceeds the upper boundary, the lower path is disabled. V_{O1} is regulated by a higher-level hysteresis window. Since V_{O1} equals the sum of the voltages across C_{O1} and C_{O2}, it can exceed its upper boundary during C_{O2} charging, meaning the effective hysteresis window for V_{O1} is slightly larger than that for V_{O2}.

To implement dual-output regulation, the DOVD operates in four distinct phases, as shown in Figure 3.15. Notably, a freewheeling switch, S_{FW}, is inserted in the topology to complete the regulation function. The four operation phases are:

Both-charging phase, Φ_1: When both outputs require energy, the DOVD acts as a full-wave voltage doubler with M_P and M_N operating as active diodes. Both C_{O1} and C_{O2} are charged.

C_{O1}-charging phase, Φ_2: When only V_{O1} requires charging, M_P operates as an active diode while M_N is disabled. Only C_{O1} is charged.

C_{O2}-charging phase, Φ_3: When only V_{O2} requires charging, M_P is disabled while M_N remains active, so only C_{O2} is charged.

Freewheeling phase, Φ_4: When neither output requires charging, S_{FW} shorts L_2, while M_P and M_N are disabled. C_{O1} and C_{O2} are then discharged only by their loads.

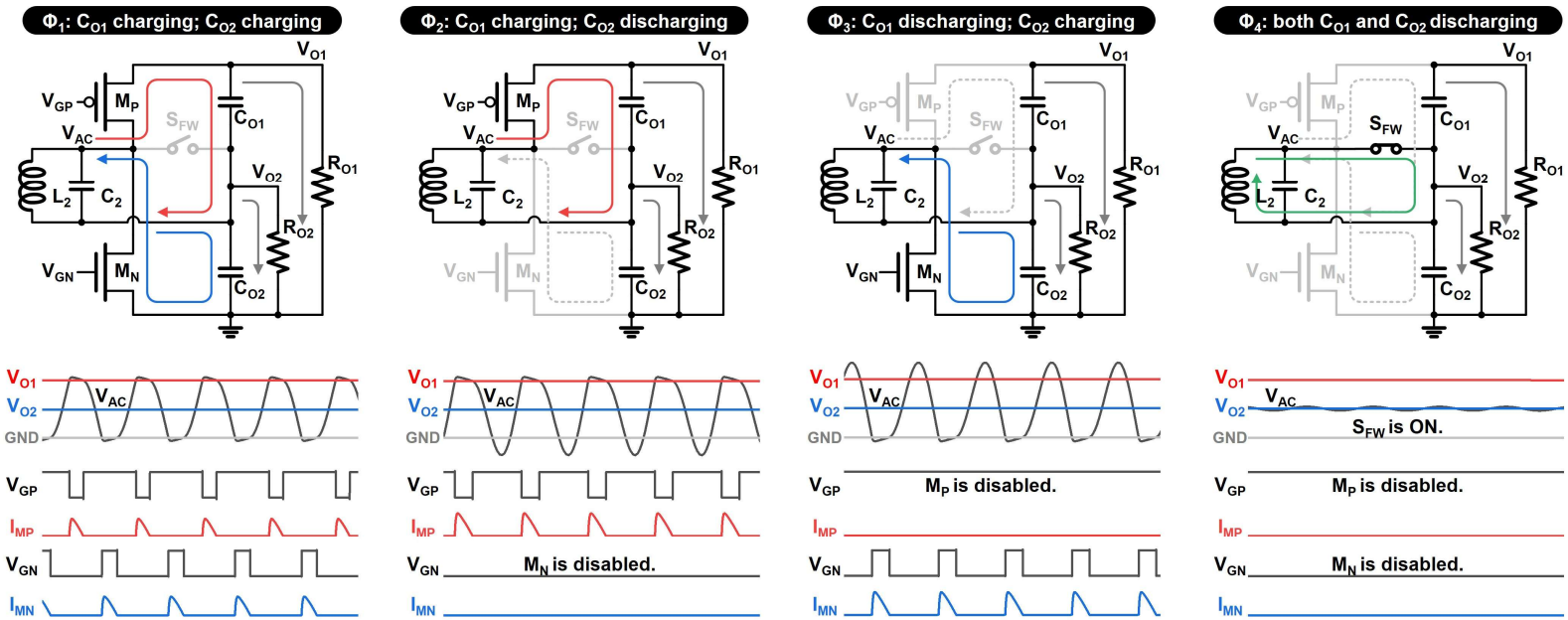


Figure 3.15 Four-phase operation principle of the proposed dual-output voltage doubler.

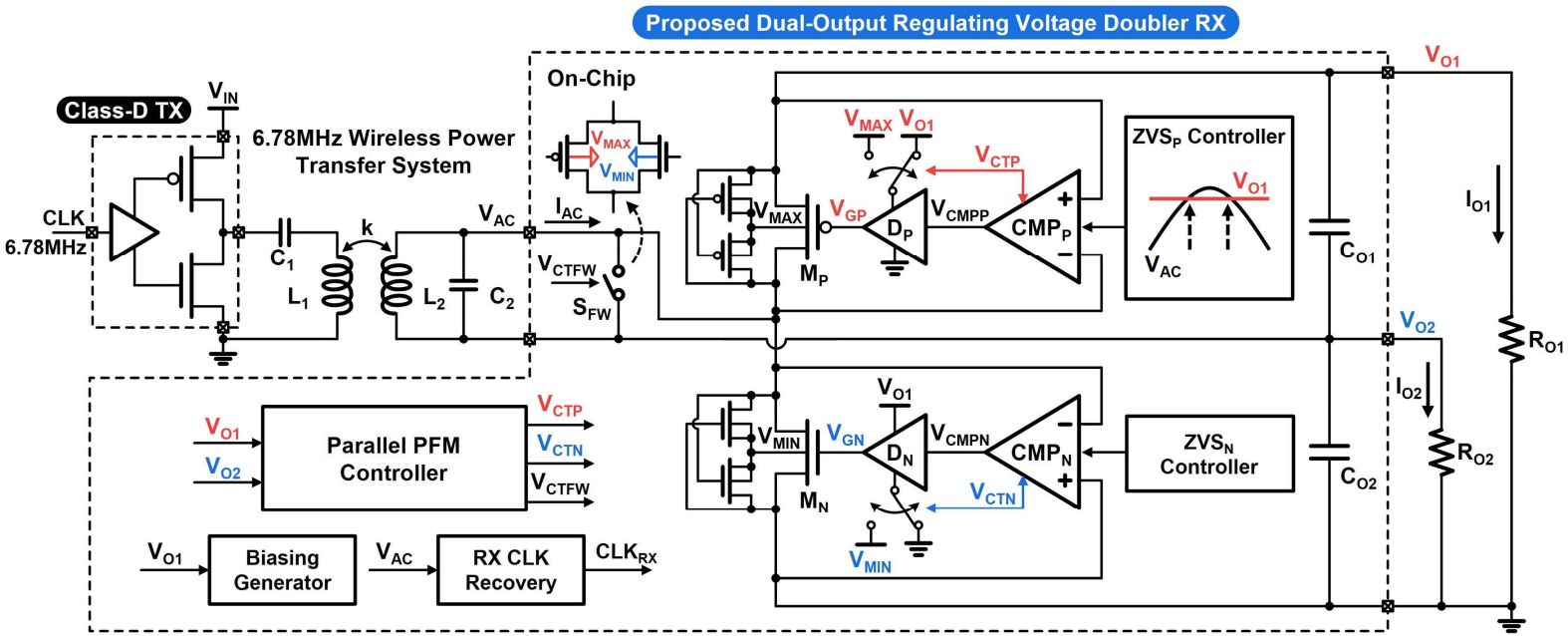


Figure 3.16 System diagram of the proposed dual-output voltage doubler.

3.2.3 Circuit Implementations

Figure 3.16 illustrates the system diagram of the proposed DOVD, used as the RX circuit in a 6.78-MHz series–parallel resonant WPT system. The power stage consists of M_P, M_N, C_{O1}, and C_{O2}. In the upper path, M_P is driven by CMP_P, which compares V_{AC} with V_{O1}. To ensure zero-voltage switching (ZVS), a digital-tuning ZVS_P controller compensates for the control loop delay between CMP_P and M_P. The gate driver D_P can switch its operation between a V_{CMPP} voltage buffer and a V_{MAX} voltage follower, supporting the four-phase operation. The lower path, comprising M_N, D_N, CMP_N, and the ZVS_N controller, is implemented in the same manner as the upper path. The PPFM controller regulates the two outputs by coordinating the four-phase operation, while a local clock (CLK_{RX}) recovered from V_{AC} synchronizes the control signals with the power flow to enable seamless phase transitions.

3.2.3.1 Parallel PFM Controller

Figure 3.17 shows the circuit diagram of the PPFM controller, which consists of three parts: the V_{O1} detector, the V_{O2} detector, and the output stage including logic buffers and level shifters. In the V_{O1} detector, V_{O1} is compared against the upper threshold voltage V_{REFH1} by a latched comparator. The comparison is synchronized with CLK_{RX} when V_{AC} is approximately equal to V_{O2}, ensuring that no conduction path exists when the DOVD samples V_{O1} and anticipates a possible phase transition. In contrast, V_{O1} is compared against the lower threshold voltage V_{REFL1} by a continuous-time comparator, since the DOVD may be in the freewheeling phase (Φ_4) without a valid CLK_{RX} edge. Following these stages, changes in V_{H1} and V_{L1} are identified by rising- and falling-edge detectors, respectively. The resulting voltage state of V_{O1} is stored in an SR latch, whose output is buffered, level-shifted, and then applied to the upper power path as the control signal V_{CTP} for V_{O1} regulation.

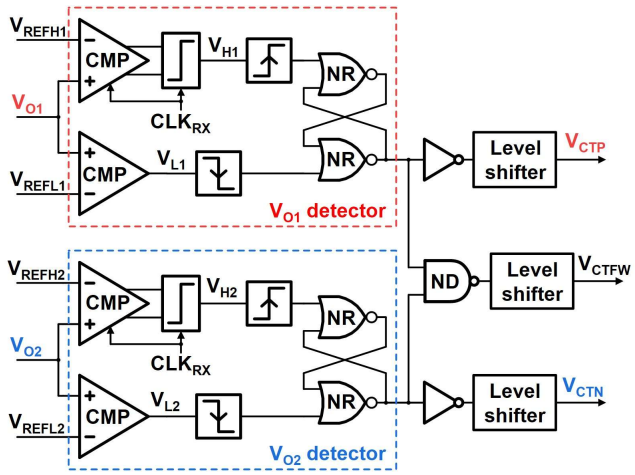


Figure 3.17 Circuit implementation of the PPFM controller.

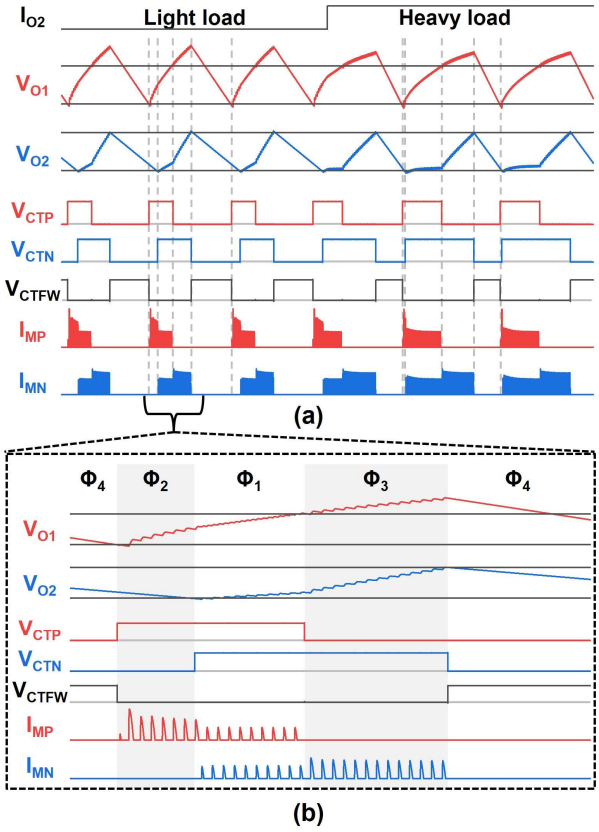


Figure 3.18 Simulated waveforms of the PPFM controller. (a) Waveforms during I_{O2} load transient. (b) Zoomed steady-state waveforms.

The V_{O2} detector operates in the same manner as the V_{O1} detector and directly generates the control signal V_{CTN} for the lower power path to regulate V_{O2}. The gate control signal for S_{FW}, V_{CTFW}, is derived from a NAND gate that takes the outputs of both detectors, ensuring that S_{FW} turns on only when both upper and lower power paths are idle. Figure 3.18(a) presents the simulated operational waveforms of the PPFM controller during an I_{O2} load transient, while Figure 3.18(b) shows zoomed-in steady-state waveforms.

3.2.3.2 Digital-Tuning Adaptive Delay Compensation

The control loop delay from CMP_P (or CMP_N) to M_P (or M_N) can cause significant turn-on and turn-off errors of M_P (or M_N). To mitigate this, delay compensation techniques must be applied. Furthermore, since the DOVD distributes power between the upper and lower paths through four-phase operation, the turn-on/off errors of M_P and M_N can vary across different phases. As a result, the delay compensation block must respond quickly enough to handle these variations.

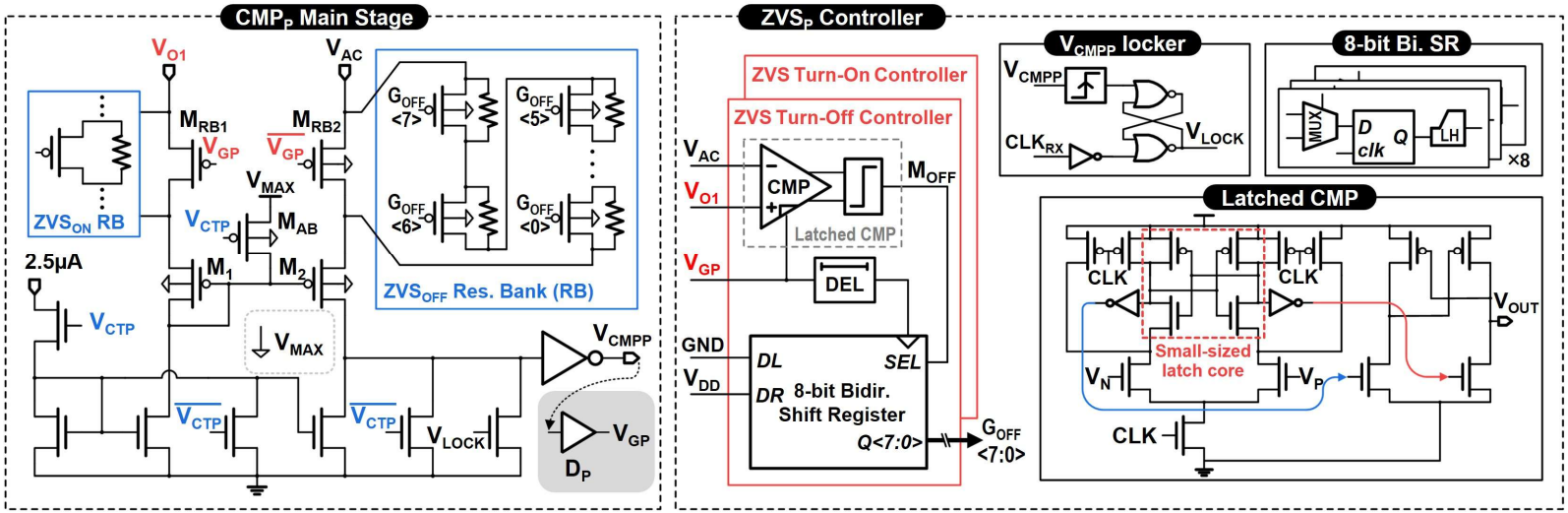


Figure 3.19 Circuit implementation of CMP_P with digital-tuning adaptive delay compensation (ZVS_P controller).

In [3.1], [3.3], [3.15], and [3.16], fixed delay compensation is implemented by adding switched biasing branches to a push–pull comparator. This approach is simple and reliable but sensitive to changes in input/load conditions and process, voltage, and temperature (PVT) variations. In [3.8] and [3.9], adaptive delay compensation is achieved by adding switched voltage-controlled biasing branches, while in [3.17] and [3.18], tunable voltage offsets are applied to comparator inputs. Although these methods can adaptively track delay variations, they rely on analog feedback loops, which are typically slow.

In this work, a digital adaptive delay compensation technique is proposed, offering fast response to both turn-on and turn-off delay variations. The circuit implementation of CMP_P and ZVS_P controller is shown in Figure 3.19. CMP_P uses a common-gate input pair (M_1 and M_2), with two resistor banks (RBs) placed at the inputs to provide voltage offsets for turn-on/off delay compensation. Each RB consists of eight identical unit resistors and eight bypass switches. Since V_{GP}, the final driving signal of M_P, is high when V_{AC} rises toward V_{O1}, the ZVS_{OFF} RB is shorted through M_{RB2}, while the ZVS_{ON} RB is inserted into the V_{O1} input path. The ZVS_{ON} RB then generates an offset voltage on V_{O1} to achieve ZVS turn-on of M_P. A similar mechanism applies to ZVS turn-off when V_{AC} falls below V_{O1}.

The ZVS_P controller tunes the voltage offsets by adjusting the number of engaged unit resistors in the RBs. In the ZVS_P turn-off controller, the polarity of the voltage error between V_{AC} and V_{O1} is detected by a latched comparator, synchronized with the rising edge of V_{GP} (the turn-off moment of M_P). Designed with a typical response time below 300 ps, the latched comparator eliminates the need for conventional sample-and-hold circuits. Its output determines the shift direction of an 8-bit bidirectional shift register (Bi. SR), which controls the number of engaged resistors in the ZVS_{OFF} RB. Through this feedback loop, an appropriate voltage offset is applied to enable ZVS turn-off of M_P. The ZVS_P turn-on controller operates in the same manner.

Since the delay compensation unbalances the comparator, switching RB may cause output oscillations around the equal-input condition, commonly referred to as the multiple-pulsing issue [3.19]. This behavior primarily occurs during turn-off, when the voltage difference between V_{AC} and V_{O1} is small as M_P is enabled. To prevent this, CMP_P uses a V_{CMPP} locker, as shown in Figure 3.19. After a rising edge, the locker forces V_{CMPP} to remain high until V_{AC} reverses polarity, ensuring that M_P is turned off only once per period. Similarly, a V_{CMPN} locker is also applied in CMP_N.

Figure 3.20 shows the operational waveforms of CMP_P and the ZVS_P controller. During phase transitions, CMP_P can recalibrate within a few cycles thanks to the proposed digital-tuning adaptive delay compensation. In steady state, M_P achieves near-optimal ZVS turn-on and turn-off, as further confirmed in the measurement results.

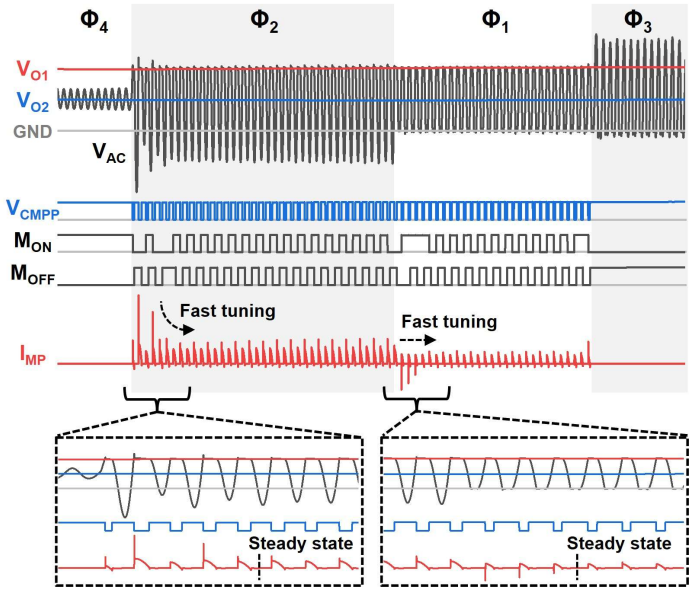


Figure 3.20 Simulated waveforms of CMP_P with digital-tuning adaptive delay compensation.

3.2.3.3 Adaptive-Biasing-Based V_{AC}-Swing Isolation

In the operational phases Φ_2 and Φ_3, the L_2–C_2 tank freewheels for half a period as the DOVD disengages one side of the power stage, leading to resonance energy accumulation. As a result, V_{AC} can fall below ground in Φ_2 or rise above V_{O1} in Φ_3. If M_N is simply disabled by tying V_{GN} to ground in Φ_2, it may unintentionally turn on once V_{AC} drops below $-V_{THN}$. A similar situation can occur for M_P during Φ_3. Therefore, proper biasing of M_P and M_N in these phases is essential to ensure reliable regulation of both outputs.

Figure 3.21 shows the adaptive-biasing gate driver circuits. When V_{CTP} is high, indicating that the upper power path should be active, the gate driver D_P functions as a four-stage inverter-based buffer powered by V_{O1}, producing V_{GP} as a buffered version of V_{CMPP}. When V_{CTP} goes low, the last stage of D_P is disconnected from the previous stages, and both transistors in the last stage are turned off. D_P then switches to voltage-follower mode, tying V_{GP} to V_{MAX}. This guarantees that V_{GP} follows V_{MAX} when the upper path is disabled, ensuring a robust open-circuit state for M_P when V_{AC} can exceed V_{O1}. The gate driver D_N is implemented in the same way.

The V_{AC} swing isolation concern also applies to CMP_P, CMP_N, and the S_{FW} driver, since they all interface with V_{AC} through non-isolated transistor terminals. For example, in CMP_P (Figure 3.19), the gates of the input pair M_1 and M_2 can be biased to V_{MAX} via M_{AB} when the upper power path is disabled. This prevents false switching at V_{CMPP}, thereby reducing unnecessary power loss and improving system reliability. The same design principles are used to implement V_{AC} swing isolation in other blocks.

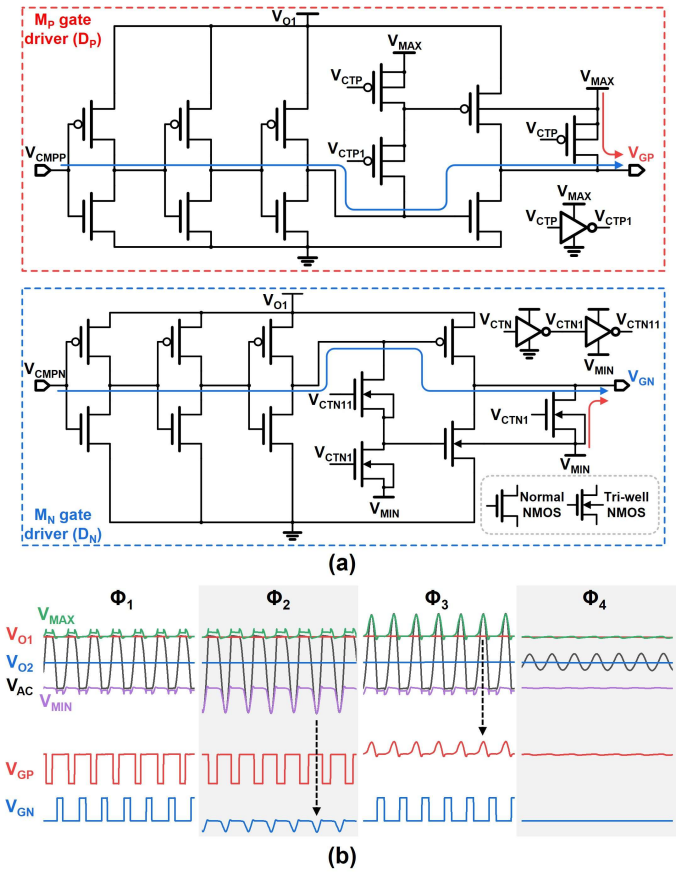


Figure 3.21 Adaptive-biasing gate drivers. (a) Circuit implementation. (b) Simulated waveforms.

3.2.4 Measurement Results

The proposed DOVD was fabricated in a 180-nm BCD process, occupying a silicon area of 0.34 mm² excluding pads, as shown in Figure 3.22. The power stage employs 5-V devices to support high-voltage power delivery, while 1.8-V devices are used in the control circuitry. Both C_{O1} and C_{O2} are implemented on chip, each with a capacitance of about 100 pF. Additional off-chip capacitors should be added for heavy-load applications.

Figure 3.23 shows the measurement setup. A Keysight 33600A waveform generator emulates the Class-D power amplifier at the TX side, generating a 6.78-MHz square wave. The wireless power link is implemented with a series–parallel resonant inductive topology. The TX and RX coils have inductances of 951 nH and 540 nH, respectively, with a fixed separation of 7 mm. For testing on the PCB, two 4.5-μF output capacitors were added externally to C_{O1} and C_{O2} as supplementary buffers.

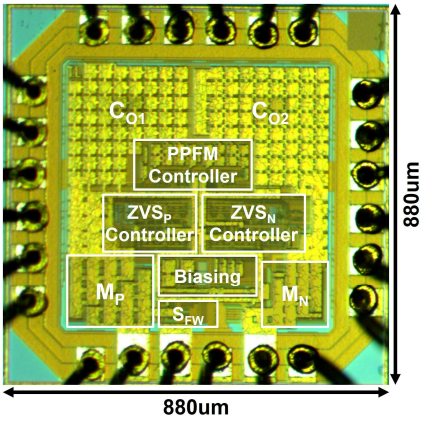
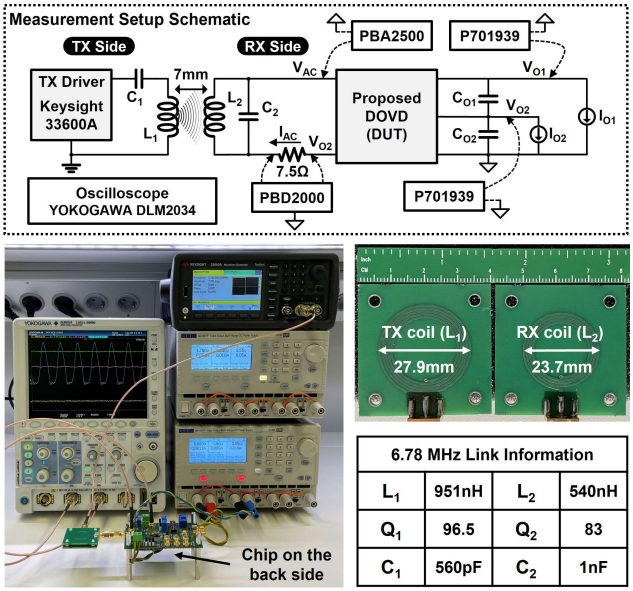


Figure 3.22 Die micrograph of the proposed dual-output voltage doubler.



6.78 MHz Link Information			
L_1	951nH	L_2	540nH
Q_1	96.5	Q_2	83
C_1	560pF	C_2	1nF

Figure 3.23 Measurement setup with link information.

Figure 3.24 shows the measured steady-state waveforms of the proposed DOVD under load conditions of I_{O1} = 1.65 mA (R_{O1} = 2 kΩ) and I_{O2} = 1.8 mA (R_{O2} = 1 kΩ). V_{O1} and V_{O2} are regulated at 3.3 V and 1.8 V, with voltage ripples of 125 mV and 75 mV. The control signals V_{CTP} and V_{CTN} confirm the four-phase operation managed by the PPFM controller.

Figure 3.25 presents the measured steady-state waveforms including the input voltage V_{AC}. The operational phases can be clearly distinguished from the V_{AC} amplitude. In Φ_2 and Φ_3, V_{AC} drops below ground and rises above V_{O1}, respectively, due to the freewheeling L_2–C_2 tank. In Φ_4, the V_{AC} amplitude decreases significantly as L_2 is short-circuited.

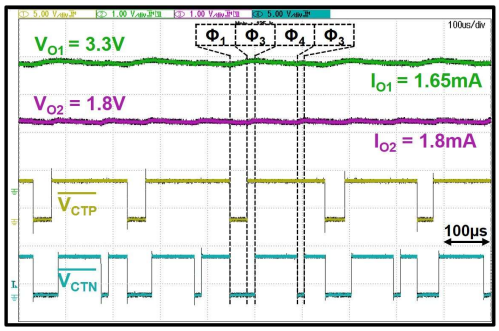


Figure 3.24 Measured steady-state waveforms showing PPFM output regulation.

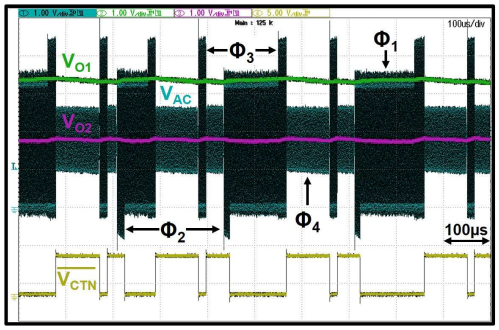


Figure 3.25 Measured steady-state waveforms with V_{AC} signals.

Figure 3.26 provides zoomed-in steady-state waveforms of the four operational phases. The input current, I_{AC}, was measured using a 2-GHz bandwidth differential probe across a 7.5-Ω sensing resistor inserted in the input path near V_{O2}. The results confirm that the proposed digital-tuning adaptive delay compensation enables the DOVD to achieve near-optimal ZVS turn-on and turn-off of both M_P and M_N across all charging phases.

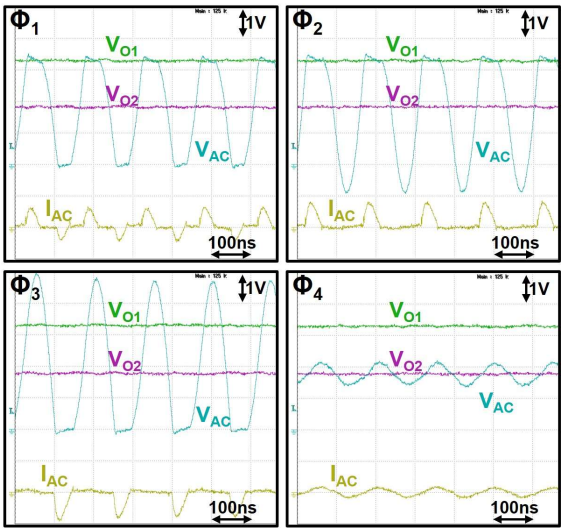


Figure 3.26 Measured zoomed steady-state waveforms in four phases.

Figure 3.27(a) shows the measured waveforms of the proposed DOVD during a load transient at V_{O1}. Owing to the fast hysteresis-based PFM controller, V_{O1} exhibits negligible undershoot or overshoot when I_{O1} varies between 0.66 mA (R_{O1} = 5 kΩ) and 16.5 mA (R_{O1} = 200 Ω), while I_{O2} is held constant at 1.8 mA (R_{O2} = 1 kΩ). Furthermore, because the proposed DOVD employs a PPFM control strategy, no cross-regulation is observed at V_{O2} during the I_{O1} load transient, confirming reliable dual-output regulation.

Similarly, Figure 3.27(b) shows the measured waveforms during a load transient at V_{O2}. When I_{O2} varies between 0.36 mA (R_{O2} = 5 kΩ) and 9 mA (R_{O2} = 200 Ω), while I_{O1} is fixed at 3.3 mA (R_{O1} = 1 kΩ), V_{O2} maintains stable regulation without undershoot or overshoot, and no cross-regulation is observed at V_{O1}.

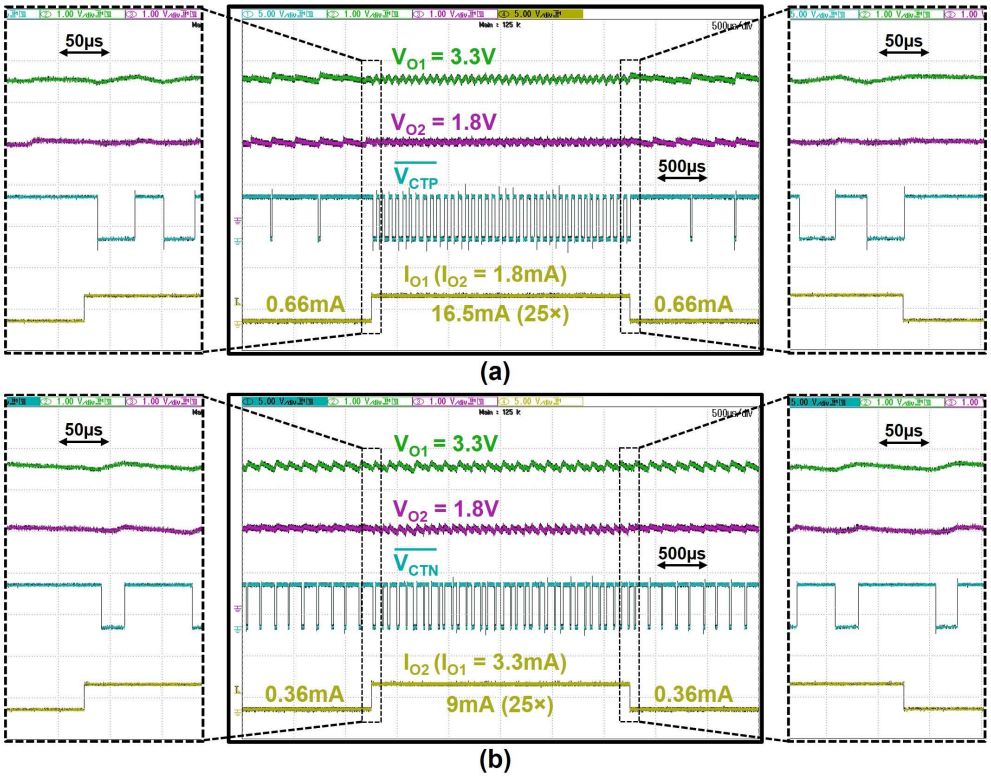


Figure 3.27 Load-transient waveforms (a) at I_{O1} with I_{O2} = 1.8 mA and (b) at I_{O2} with I_{O1} = 3.3 mA.

Figure 3.28 shows the measured PCE of the proposed DOVD under different load conditions. The PCE is defined as

$$PCE = \frac{\sqrt{\frac{{V_{O1}}^2}{R_{O1}} + \frac{{V_{O2}}^2}{R_{O2}}}}{(V_{AC} - V_{O2}) \times I_{AC}} \times 100\% \tag{3.3}$$

Because the oscilloscope has a fixed sampling rate, averaged instantaneous power is used for PCE calculation. From the 3-D color map in Figure 3.28(a), the DOVD

sustains a PCE above 85% across a wide load range. At very light loads (<5 mA for both outputs), the PCE drops as freewheeling conduction loss in Φ_4 becomes dominant. The peak PCE of 92.95% is achieved under heavy-load conditions (I_{O1} = 15 mA and I_{O2} = 20 mA), when the DOVD primarily operates in charging phases. With varying I_{O1} at fixed I_{O2} values [Figure 3.28(b)], the DOVD supports I_{O1} from 0 to 25 mA, maintaining >90% PCE across a wide range. With varying I_{O2} at fixed I_{O1} values [Figure 3.28(c)], the DOVD sustains I_{O2} from 0 to 30 mA. Compared with I_{O2}, the PCE shows stronger dependence on I_{O1}. The tested load ranges of I_{O1} and I_{O2} cover most practical requirements of biomedical implantable devices.

Figure 3.29 shows the measured VCR at V_{O1} across different load conditions. The VCR is defined as

$$VCR = \frac{2V_{O1}}{(V_{AC} - V_{O2})_{peak-to-peak}} \tag{3.4}$$

and is measured during Φ_1. As shown in Figure 3.29(a), the VCR remains above 1.72 over the full load range. The peak VCR of 1.875 is obtained when I_{O1} = 1.65 mA and I_{O2} = 5 mA. With varying I_{O1} under fixed I_{O2} [Figure 3.29(b)], VCR exhibits a clear negative correlation with I_{O1}. With varying I_{O2} under fixed I_{O1} [Figure 3.29(c)], VCR changes more gently, since I_{O2} does not directly load V_{O1}.

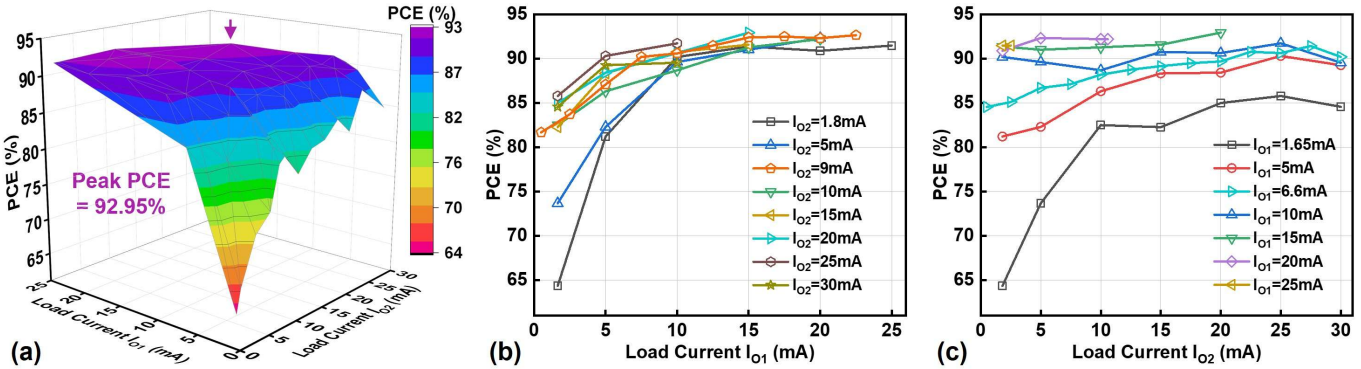


Figure 3.28 Measured PCE versus load currents. (a) 3-D colormap of PCE. (b) PCE versus I_{O1}. (c) PCE versus I_{O2}.

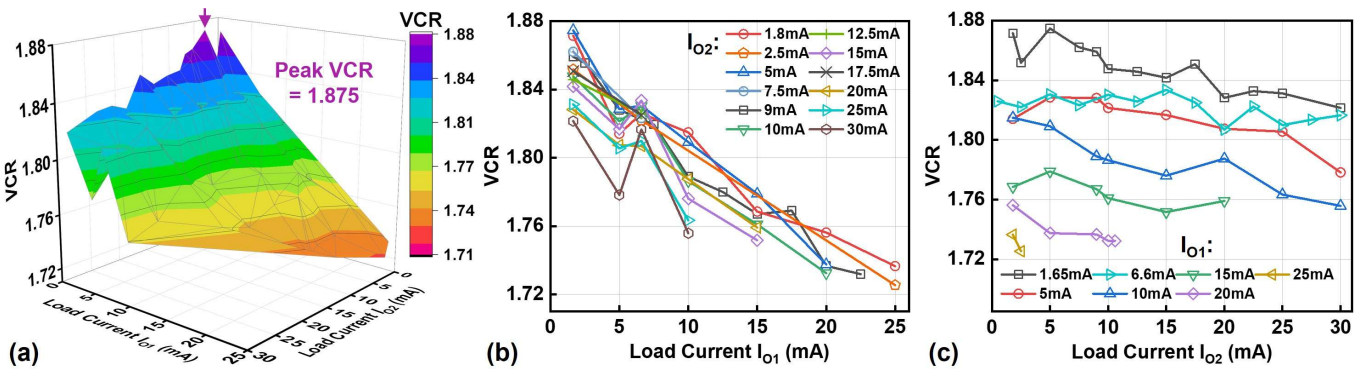


Figure 3.29 Measured VCR at V_{O1} versus load currents. (a) 3-D colormap of VCR. (b) VCR versus I_{O1}. (c) VCR versus I_{O2}.

Figure 3.30 presents the simulated power breakdown under the measured maximum output power condition, which reaches 90.5 mW (I_{O1} = 22.5 mA, I_{O2} = 9 mA). At this point, approximately 6.2% of the input power is consumed by DOVD, mainly due to conduction and switching losses of M_P and M_N ($P_{CDP/N}$ and $P_{SWP/N}$). P_{FW} denotes freewheeling loss.

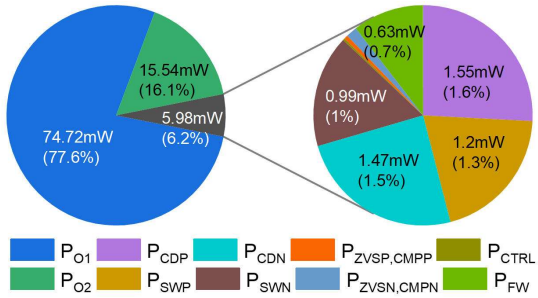


Figure 3.30 Simulated power breakdown under the measured maximum output power condition (I_{O1} = 22.5 mA, I_{O2} = 9 mA).

Table 3.3 compares the proposed DOVD with recently reported single-stage dual-output and high-VCR RX designs. The DOVD employs only two power transistors, which is the minimum device count among state-of-the-art designs, while achieving a VCR as high as 1.875, nearly twice that of conventional FBRs. With the proposed PPFM control strategy, it delivers instant load-transient response and negligible cross-regulation. In addition, the digital-tuning adaptive delay compensation enables near-optimal ZVS turn-on/off and provides fast responses to error variations. Leveraging both its simplified topology and advanced control circuitry, the proposed DOVD achieves the highest reported power efficiency in the table.

3.2.5 Discussions and Conclusion

3.2.5.1 End-to-End Efficiency

Regulating rectifiers have recently attracted significant interest in WPT integrated circuit design, driven by the stringent size and cost requirements of biomedical implants and portable electronics. However, their advantages come with trade-offs. Specifically, regulating rectifiers sacrifice the ability to perform impedance transformation, which is essential for achieving optimal end-to-end (E2E, TX-to-load) efficiency point tracking (OEPT) at the system level [3.20]. By contrast, a cascaded dc–dc converter reliably reflects the optimal impedance to the TX, thereby ensuring OEPT. This trade-off is an important consideration when designing a WPT system and must be carefully optimized according to application requirements. Without impedance transformation, E2E efficiency degrades when RX output voltages deviate from their optimal values. Although the RX may still maintain a decent PCE under such conditions, additional losses are likely to occur at the TX and within the inductive link.

These considerations also apply to the proposed DOVD. Since its optimal output voltages are determined by the topology, users can freely configure V_{O1} and V_{O2} but at a potential cost to E2E efficiency. To extend system lifetime and reduce local heating, future work should explore regulating rectifiers capable of OEPT.

3.2.5.2 Output Dependency in the DOVD

Because the DOVD employs two stacked output capacitors, it is important to examine its output dependencies. One concern is ripple dependency, arising from the PFM control scheme, which has limited pull-down capability. This issue can be mitigated through improved control techniques, such as incorporating linear current-sink stages [3.12] or adopting tighter regulation strategies like pulse-width modulation (PWM) [3.21].

Another concern is loading dependency (cross-regulation). In prior architectures (see Section 2.3.1.3), multiplexed power paths created unavoidable cross-regulation: a heavy load on one output reduced power availability to the other. This was mitigated in [3.22]. The proposed DOVD inherently avoids this problem by separating the power paths, ensuring that input power is accessible to both outputs simultaneously. Though V_{O1} and V_{O2} share C_{O2} and part of V_{O2}'s load originates from R_{O1}, the proposed parallel control strategy effectively manages this interaction. As confirmed by load-transient and PCE measurements, no cross-regulation is observed. If the two load currents differ significantly, the voltages across the two output capacitors still remain close to each other owing to the PPFM strategy.

3.2.5.3 Conclusion

Section 3.2 presents a dual-output regulating voltage doubler (DOVD). DOVD achieves AC-to-DC rectification with a VCR up to 1.875 and dual-output voltage regulation using only two power transistors. With PPFM-based output regulation, it demonstrates instant load-transient response and negligible cross-regulation. The digital-tuning adaptive delay compensation further enables near-optimal ZVS turn-on/off with fast response to error variations. Overall, the proposed DOVD achieves a competitive output power range of 2.6–90.5 mW and a high peak power efficiency of 92.95%.

Notably, a similar work published in 2025 demonstrated a regulating voltage doubler operating at 40.68 MHz [3.26], thereby further verifying the frequency scalability of the voltage-doubler topology.

Table 3.3 Comparison with state-of-the-art designs.

	JSSC'19 [3.14]	TBCAS'20 [3.13]	JSSC'21 [3.22]	ISSCC'23 [3.23]	JSSC'23 [3.24]	TCAS-I'23 [3.25]	This work
Technology	350 nm CMOS	180 nm CMOS	180 nm CMOS	65 nm CMOS	180 nm CMOS	180 nm CMOS	**180 nm BCD**
Chip Area	2.4 mm^2	6 mm^2	0.6 mm^2	0.74 mm^2	2.32 mm^2	2.7 mm^2	**0.34 mm^2**
Operation Frequency	1 MHz	2 MHz	6.78 MHz	40.68 MHz	6.78 MHz	6.78 MHz	**6.78 MHz**
LC Topology	Parallel	-	Series	Parallel	Parallel	Series	**Parallel**
Receiver Topology	VM/CM Rectifier	VM Full-Bridge Rectifier	VM Full-Bridge Rectifier	VM Full-Bridge Rectifier	VM Full-Bridge Rectifier	RCM Rectifier	**VM Voltage Doubler**
No. of Power Transistors	3	6	4	5	6	5	**2**
V_{OUT} (No. of V_{OUT})	3V (1)	1.5V, 2.5V (2)	1.8V, 3.3V (2)	1.1V, 2.2V (2)	3.7V, 5V (2)	1.8V, 3V (2)	**1.8V, 3.3V (2)**
Output Regulation	Reverse Conduction	PFM + PWM	PFM	PFM	PFM	PFM	**Parallel PFM**
Adaptive Delay Compensation	No	Analog-Based Turn-On/Off ZVS	No	Analog-Based Turn-On ZVS	Digital-Tuning Turn-On/Off ZVS	Digital-Controlled Delay Line	**Digital-Tuning Turn-On/Off ZVS**
Load-Transient Response	-	-	Instant	Instant	Instant	2 ms[#]	**Instant**
Cross Regulation	-	-	Unnoticeable	Unnoticeable	-	100 mV/mA[#]	**Unnoticeable**
Peak VCR	1.4	0.83*	0.92*	0.91*	0.85*	1.5	**1.875**
P_{OUT}	0.18mW – 18mW	7.3mW - 65mW	102mW - 1.02W	6mW – 60.5mW	0.5mW – 180mW	1mW – 7mW	**2.6mW - 90.5mW**
Peak PCE	75%	90.75%	91.9%	90.1%	91.8%	85.1%	**92.95%**

*Estimated from plotted data. [#]Related to the transmitter-side power regulation in [3.25].

3.3 Concluding Remarks

In this chapter, a new class of voltage-mode rectifiers, regulating voltage doublers, has been proposed, implemented, fabricated, and experimentally validated.

The first design, a regulating voltage doubler (VD), achieves a doubled voltage conversion ratio (VCR) compared to conventional full-bridge rectifiers (FBRs), extending the operable coupling and loading range with state-of-the-art power and efficiency. It also reduces the required number of power transistors from four to two, though it demands two output capacitors instead of one in FBR.

Building upon this, the second design, a dual-output regulating voltage doubler (DOVD), extends functionality by independently regulating voltages across both output capacitors. Compared to conventional FBR-based designs requiring at least six power switches, the DOVD realizes dual-output regulation using only two while preserving its high-VCR benefit. Nevertheless, the potential output dependency of the DOVD should be considered when powering PSRR-sensitive circuits.

3.4 References

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Chapter 4 A Coupling-Adaptive WPT System Using a Voltage-/Current-Mode Receiver[3]

In Chapter 3, voltage-mode (VM) receivers (RXs) based on voltage doublers were studied. The key improvement was a doubled voltage conversion ratio (VCR) compared with full-bridge rectifiers. However, voltage doublers still require a certain range of input voltage amplitudes to operate, limiting their input sensitivity and thus the operable coupling range.

To overcome this limitation, this chapter introduces a hybrid voltage-/current-mode (V/CM) RX. Building on this RX, a closed-loop WPT system is developed together with a wide-range global power modulation scheme at the transmitter (TX) to enhance the system-level coupling and load adaptability. The proposed system extends the WPT distance by up to 50% compared with VM-only systems, achieves a peak end-to-end (E2E) efficiency of 72.3% and up to 40% E2E-efficiency improvement compared with open-loop operation.

4.1 Motivation

As discussed in Chapter 2 and 3, VM rectifiers feature monophasic operation, periodic output charging and inherent voltage clamping, enabling safe and efficient operation despite their limited VCRs. In contrast, resonant current-mode (RCM) rectifiers operate without requiring a specific input-output voltage relationship, fundamentally improving input sensitivity, as discussed in Section 2.3.2 of Chapter 2 [4.1]. However, RCM operation typically yields a lower effective output charging frequency, resulting in larger steady-state output ripples. In addition, the resonance phase may introduce over-voltage risks under high-power conditions.

To combine the advantages of both topologies, a hybrid voltage-/current-mode

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(V/CM) rectifier is proposed. It operates in VM under strong coupling to maintain safe monophasic behavior and automatically switches to RCM under weak coupling to sustain power transfer at lower input levels.

In a WPT system, the TX also plays an important role in determining the delivered power and end-to-end (E2E) efficiency. Under weak coupling, the TX must maximize its output power to ensure sufficient energy transfer, whereas under strong coupling, it should reduce power to optimize E2E efficiency. Moreover, large load variations are often present in implantable medical device (IMD) applications, further requiring a wide power adjustment range.

Existing closed-loop WPT systems suffer from either limited power range or suboptimal trade-offs between efficiency and output regulation. This chapter also addresses these issues by introducing a three-mode TX with pulse-width-modulation-based global power control.

4.2 System-Level Design

Figure 4.1 presents the architecture of the coupling-adaptive WPT system. The RX is a V/CM rectifier involving M_P, M_N, S_{LC}, C_{O1}, and C_{O2}. Switch S_{LSK} is used for RX-to-TX data transfer via load-shift keying (LSK). The topology is designed based on a voltage doubler (VD) for its wider operating range than full-bridge rectifiers (see Section 3.1) and high component reusability in RCM, to be detailed in Section 4.2.1.

The TX employs a three-mode Class-D PA based on four power transistors, M_{P1}, M_{P2}, M_{N1}, and M_{N2}. The full-bridge structure improves maximum output power by 4× compared to half-bridges. Three operation modes are designed to serve global power control, which will be discussed in Section 4.2.2.

The wireless link incorporates a series-resonance L_1–C_1 tank at TX and a parallel-resonance L_2–C_2 tank at RX, ensuring both high power and high efficiency across the link [4.2].

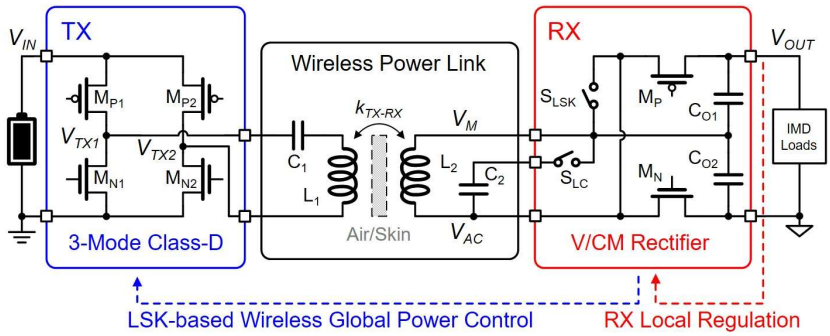


Figure 4.1 Proposed coupling-adaptive WPT system architecture.

4.2.1 Hybrid V/CM RX

4.2.1.1 V/CM RX Operation

The V/CM RX has six operation phases, as shown in Figure 4.2. The detailed operation is explained in the following.

1) VM Operation: Under strong coupling, the proposed RX works in VM as a full-wave VD with two phases. When V_{AC} is higher than V_{OUT}, it turns on M_P to enter the C_{O1}-charging phase, as shown in Figure 4.2(a). As V_{AC} is lower than ground, it switches to the C_{O2}-charging phase by turning on M_N, as shown in Figure 4.2(b). During the VM operation, S_{LC} is always turned on to form a parallel L_2–C_2 resonance tank.

2) Freewheeling (0X) Operation: To generate LSK signal for global power control and locally regulate V_{OUT}, the RX enters 0X phase, where S_{LSK} is turned on to short L_2, and M_P, M_N, and S_{LC} are all turned off, as shown in Figure 4.2(c).

3) Resonant CM Operation: Under weak coupling, the RX works as a resonant CM rectifier with three phases. Figure 4.2(d) shows the resonance phase, during which only S_{LC} is turned on, allowing resonance energy to accumulate in the L_2–C_2 tank. Once the accumulated energy reaches a sufficient level, the RX enters either the C_{O1}-charging phase or the C_{O2}-charging phase, as depicted in Figure 4.2(e) and (f), respectively. The CM charging phases are triggered only when V_{AC} equals V_M so that the entire resonance energy is stored in L_2. During the CM charging phases, L_2 performs as a current source, and C_2 is disconnected from the circuit.

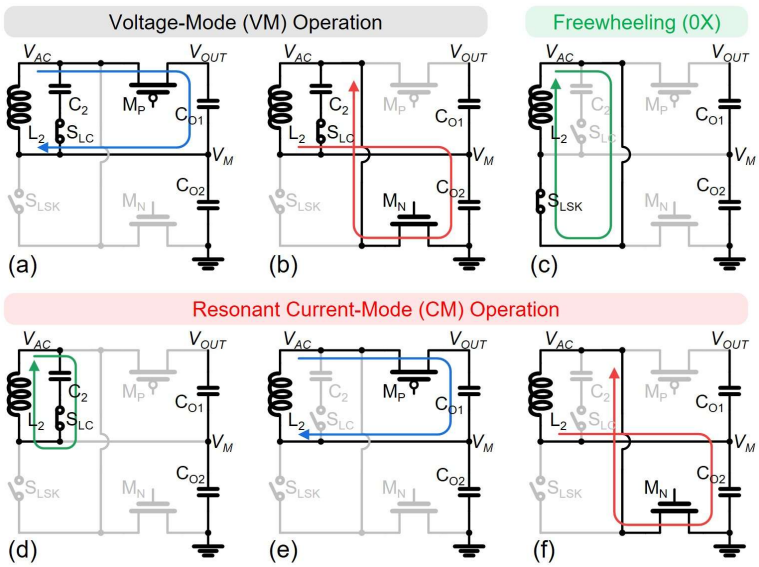


Figure 4.2 Operation principle of the proposed V/CM RX. (a) VM C_{O1}-charging phase. (b) VM C_{O2}-charging phase. (c) Freewheeling (0X) phase. (d) CM resonance phase. (e) CM C_{O1}-charging phase. (f) CM C_{O2}-charging phase.

Figure 4.3 shows the RX operation waveform. Under strong coupling, it works in VM. Upon V_{OUT} surpassing the upper threshold voltage, V_{REFH}, it enters 0X phase for 0.6 μs, generating an LSK signal that triggers global power control at TX for output regulation. In case the link coupling weakens, V_{OUT} decreases due to insufficient input power at RX. When V_{OUT} falls below the lower threshold voltage, V_{REFL}, a VM-to-CM transition detection will be initiated. The RX will seamlessly switch to CM operation to recover V_{OUT} if it is identified as weak coupling. The coupling identification process will be detailed in Section 4.3.1. Given that the wireless link can revert to strong coupling at any moment, the RX automatically backs to VM operation when V_{OUT} is recovered to V_{REFH}, eliminating the need for the CM-to-VM transition detection.

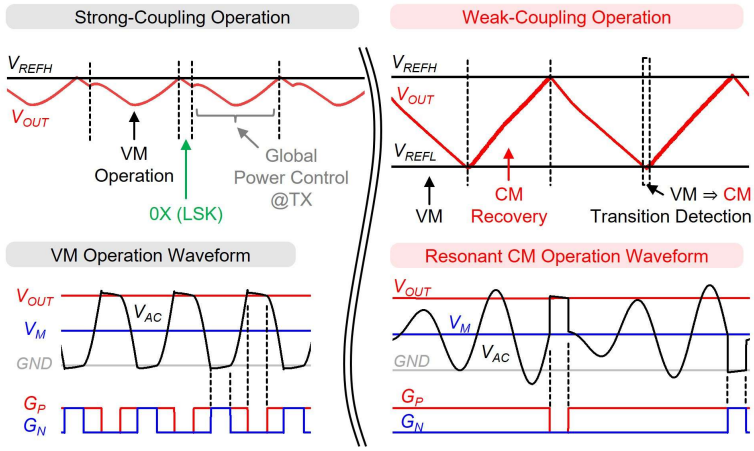


Figure 4.3 Operation waveform of the proposed V/CM RX.

4.2.1.2 V/CM Modeling and Analysis

The advantages of the hybrid mode can be investigated theoretically. As shown in Figure 4.4, the proposed RX in VM is modeled as a typical voltage doubler excluding output regulation. Derived from [4.2] and [4.3], the VM VCR, defined as the ratio between V_{OUT} and $|V_S|$, is given by

$$VCR_{VM} = \frac{\sqrt{P_1 \cdot \eta_{LINK} \cdot \eta_{VM} \cdot R_L}}{|V_S|} \tag{4.1}$$

where η_{VM} is the VM RX PCE. Assuming perfect impedance matching at both TX and RX by L_1-C_1 and L_2-C_2 networks, the TX power from V_S, P_1, and the link efficiency, η_{LINK}, can be respectively expressed as

$$P_1 = \frac{|V_S|^2}{2(R_1 + R_{EQVM})} \tag{4.2}$$

$$\eta_{LINK} = \frac{R_{EQVM}}{(R_{EQVM} + R_1) \cdot [R_2 R_{VM} (\omega C_2)^2 + 1]} \tag{4.3}$$

where the input resistance of the VM RX, R_{VM}, and the equivalent resistance of the VM RX reflected at TX, R_{EQVM}, are respectively given by

$$R_{VM} = \frac{\eta_{VM} \cdot R_{OUT}}{2 \cdot {VCR_{VD}}^2} = \frac{\eta_{VM} \cdot R_{OUT}}{8} \tag{4.4}$$

$$R_{EQVM} = \frac{\omega^2 M^2 R_{VM} (\omega C_2)^2}{R_2 R_{VM} (\omega C_2)^2 + 1} \tag{4.5}$$

where VCR_{VD} is the inherent VCR of voltage doubler; $\omega = 2\pi f_0$ is the angular frequency of the carrier (f_0 = 6.78 MHz); M is the mutual inductance between the TX and RX coils; R_{OUT} is the load resistance. Note that $(\omega C_2 R_L)^2 \gg 1$ is assumed to derive R_{EQVM} in (4.5). This neglects the effect of R_{OUT} on resonance shift, which should also be practically satisfied by a parallel-resonant RX (discussed in Section 2.2.2) [4.2].

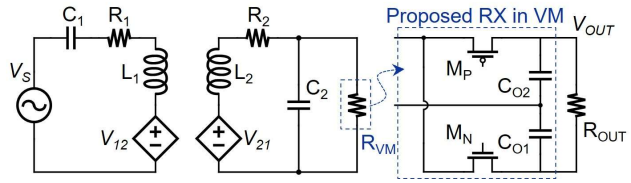


Figure 4.4 Modeling of the proposed RX VM operation.

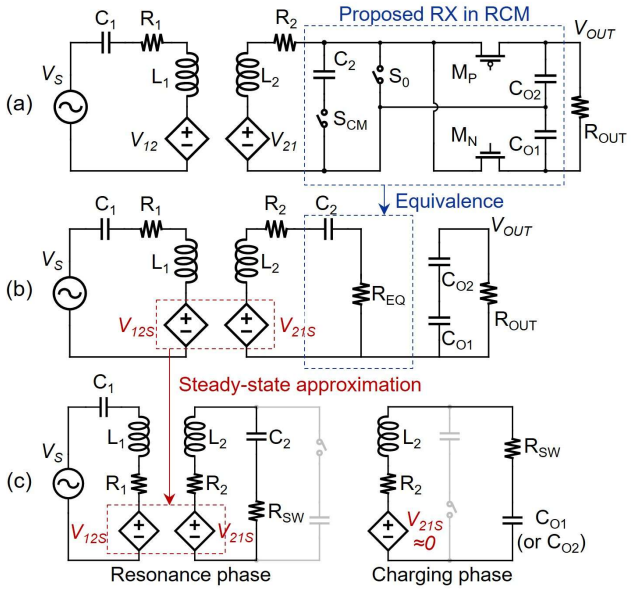


Figure 4.5 Modeling of the proposed RX RCM operation. (a) Schematic. (b) RX RCM operation equivalence. (c) TX steady-state approximation.

Figure 4.5 shows the modeling of the proposed RX in RCM. Briefly, the RCM RX has two operational phases: resonance phase and charging phase, excluding output

regulation. In the resonance phase, L_2-C_2 tank is freely resonating via S_{CM}; in the charging phase, L_2 becomes a current source delivering the resonance energy to one of the output capacitors, C_{O2} (or C_{O1}), via M_P (or M_N).

In previous RCM analysis [4.4], [4.5], and [4.6], the TX's steady state is approximated solely based on the impedance reflection during the resonance phase considering its much larger duty ratio. This may be valid under extremely weak coupling conditions with a low-quality TX resonance loop ($R_1 = 30\Omega$ in [4.4] and [4.6]), in which the RX transients are nearly invisible. However, it is not valid in practical WPT scenarios with higher power levels.

Here, energy conservation is used to approximate TX's steady state with a time-domain averaged RCM-equivalent resistance, R_{EQ}, as shown in Figure 4.5(b). Since the RCM operation only engages under weak coupling conditions, this approximation helps provide intuitive conclusions without solving time-dependent resonance transients at TX. Then, based on the approximated TX steady state, the two-phase RCM transient behavior can be solved at RX, regarded as a series-RLC resonant circuit. The final RCM model is displayed in Figure 4.5(c).

In the resonance phase of the RCM RX, if all the resonance energy in the previous cycle has been delivered to the output, the L_2-C_2 tank starts with mostly zero initial conditions. For high-quality WPT, which is usually the application case, the RX exhibits an underdamped response in this phase. Given $V_{21}(t) = |V_{21}|\sin(\omega t)$, the inductor current I_2 can be expressed as

$$I_2(t) = I_{MAX}(1 - e^{-\alpha t})\sin(\omega t) \tag{4.6}$$

where the damping factor α and the steady-state peak current I_{MAX} are respectively given by

$$\alpha = \frac{R_2 + R_{SW}}{2L_2};\ I_{MAX} = \frac{|V_{21}|}{R_2 + R_{SW}} \tag{4.7}$$

in which R_{SW} is the switch ON-resistance. At RX, the input power, $P_{IN,RX}$, can be separated into the output power of the resonance phase, P_{OUT}, and the loop power dissipation during both the resonance and charging phases, P_{LOSS}. In the charging phase it is assumed that the RX is far away from resonance and thus receives negligible power from the TX. If the resonance phase duration is set to $T_{RES} = (N - 0.5)/2f_C$ or $((N - 0.5)/2)P_C$, where N is integral and f_C is the carrier frequency, and the charging phase always starts at I_2-peak moments, P_{OUT} and P_{LOSS} can be respectively derived as

$$P_{OUT} = \frac{E_2}{T_{RES} + \frac{0.25}{f_C}} = \frac{L_2 {I_2}^2(T_{RES})}{2(T_{RES} + \frac{0.25}{f_C})} \tag{4.8}$$

$$P_{LOSS} = \frac{R_2 + R_{SW}}{T_{RES} + \frac{0.25}{f_C}} \int_0^{t_{RES}+\frac{0.25}{f_C}} I_2(t)^2 dt \tag{4.9}$$

where I_2 during the charging phase is approximated to keep a sinusoidal waveform and the charging phase duration is approximated to be $0.25/f_C$. To further calculate P_{OUT} for VCR, $V_{21}(t)$ needs to be solved to find $I_2(t)$. Applying Kirchhoff's voltage law (KVL) at the TX loop and RX loop in the resonance phase results in

$$\left(j\omega L_1 + R_1 + \frac{1}{j\omega C_1}\right) I_1(t) + V_{12}(t) = V_S(t) \tag{4.10}$$

$$\left(j\omega L_2 + R_2 + R_{SW} + \frac{1}{j\omega C_2}\right) I_2(t) = V_{21}(t) \tag{4.11}$$

At resonance where $\omega = 1/\sqrt{L_1 C_1} = 1/\sqrt{L_2 C_2}$, the amplitude of $V_{21}(t)$ can be given by

$$|V_{21}| = \omega M |I_1| = \omega M \frac{|V_S|}{R_1 + R_{EQCM}} \tag{4.12}$$

where the equivalent resistance of the RCM RX reflected at TX, R_{EQCM}, can be derived as

$$R_{EQCM} = \frac{\omega^2 M^2}{R_2 + R_{EQ}} \tag{4.13}$$

in which R_{EQ} is the proposed RCM-equivalent resistance. On the other hand, the input power of RX, $P_{IN,RX}$, can be expressed as

$$P_{IN,RX} = \frac{|V_S|^2}{2(R_1 + R_{EQCM})} \cdot \frac{R_{EQCM}}{R_1 + R_{EQCM}} \tag{4.14}$$

Based on the relationship that $P_{IN,RX} = P_{OUT} + P_{LOSS}$, R_{EQ} can be obtained by simultaneously solving (4.8), (4.9), and (4.14). Then, P_{OUT} can be calculated to reveal VCR by

$$VCR_{CM} = \frac{\sqrt{P_{OUT} \cdot \eta_{CM} \cdot R_{OUT}}}{|V_S|} \tag{4.15}$$

where η_{CM} is the RCM RX PCE excluding conduction losses, which are already considered in P_{LOSS}.

Table 4.1 Modeling and simulation circuit parameters.

Parameter		Value
Carrier frequency, f_C, $1/P_C$		6.78 MHz
Excitation amplitude, $\|V_S\|$		5 V
TX Coil	**Inductance, L_1**	1 μH
	Resistance, R_1	0.5 Ω
	Outer radius, r_1	13.5 mm
RX Coil	**Inductance, L_2**	0.3 μH
	Resistance, R_2	2 Ω
	Outer radius, r_2	10 mm
Switch on-resistance, R_{SW}		0.1 Ω
Output capacitance, C_{O1} and C_{O2}		10 nF

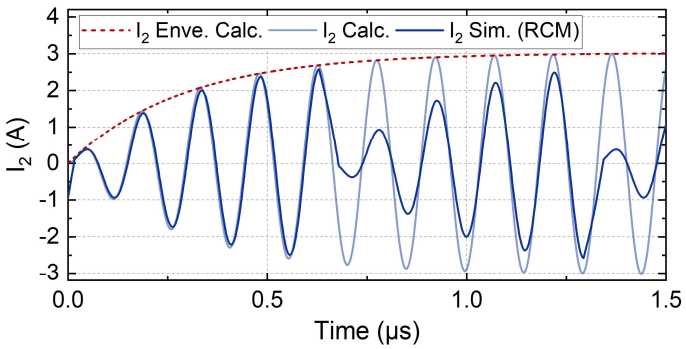


Figure 4.6 Modeled and simulated transient waveforms of I_2 in the RCM RX at coupling factor $k = 0.05$.

Cadence simulations were conducted to verify the efficacy of this RCM modeling. Table 4.1 shows the circuit parameters used in both modeling and simulations. Figure 4.6 presents both the simulated I_2 waveform using the proposed RCM RX topology and the modeled (calculated) I_2 transient waveform. It is observed that the RCM resonance phase can be accurately estimated by the series-RLC start-up transient, and the calculated envelope curve ($|I_2|$ in the modeling) tracks the peak I_2 values in the simulation.

Notably, this model involves several approximations that may lead to discrepancies from the actual behavior. It should therefore be used in conjunction with simulation verification. Moreover, the model can instruct, for example, the optimal number of cycles before switching from the resonant phase to the charging phase, as illustrated in the next two figures.

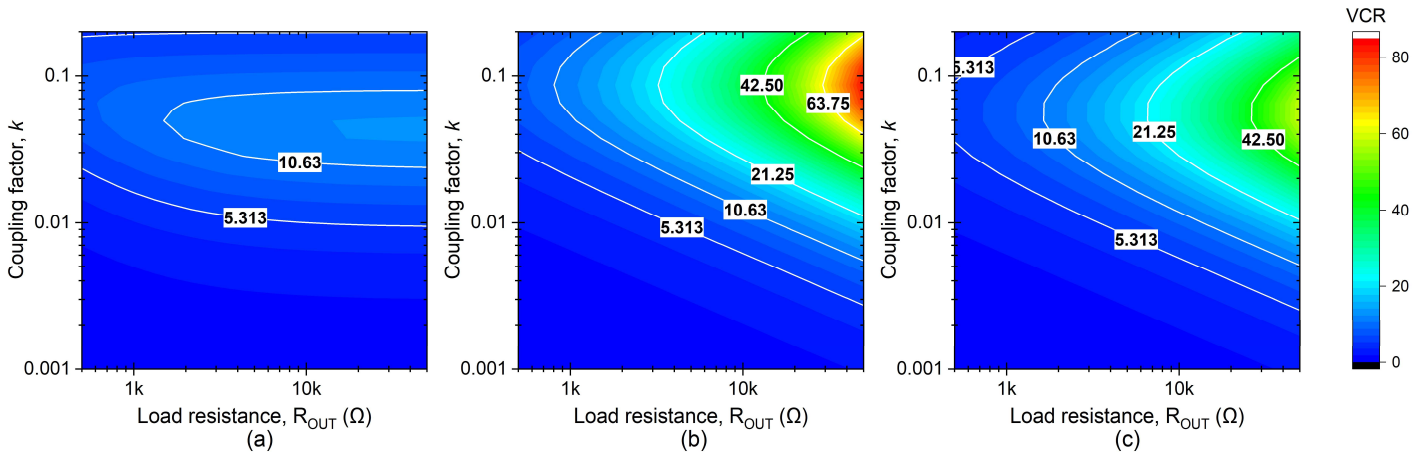


Figure 4.7 Modeled VCR colormaps versus load resistance, R_{OUT}, and coupling factor, k. (a) VM RX. (b) RCM RX with the resonance phase duration of $1.5 \times P_C$. (c) RCM RX with the resonance phase duration of $4.5 \times P_C$.

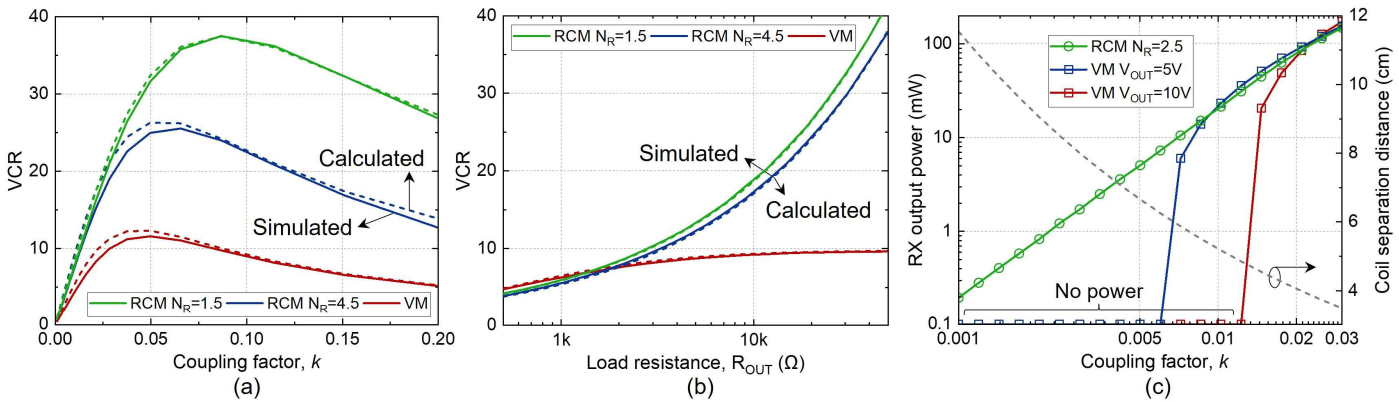


Figure 4.8 Modeled and simulated VCR comparisons between VM and RCM. (a) VCR versus k at R_{OUT} = 10kΩ. (b) VCR versus R_{OUT} at k = 0.025. (c) Simulated RX output power versus k at $|V_S| = 1.8\ V$ with constant-V_{OUT} loads.

Figure 4.7 shows the VCR performance of both VM and RCM RX based on the models, using the parameters from Table 4.1 and $\eta_{VM} = \eta_{CM} = 1$. As shown in Figure 4.7(a), the VM RX shows limited VCR (open loop) whose maximum only reaches around 10, at the critical coupling k = 0.05 (maximum power point), over the entire R_{OUT} range from 500Ω to 50kΩ. The VM VCR drops below 5 when k falls below 0.01. In comparison, the RCM RX shows a much higher VCR in general. Figure 4.7(b) shows the RCM RX performance when the resonance phase duration is $1.5 \times P_C$. The maximum VCR (open loop) exceeds 80 at the critical coupling k = 0.08, and the VCR remains higher than 5 even when k drops to 0.003 at R_L = 50kΩ. Figure 4.7(c) shows the RCM RX with a $4.5 \times P_C$ resonance phase duration and a critical coupling k = 0.055 similar to the VM RX. Due to higher P_{LOSS} in the resonance phase, it shows lower VCR under strong coupling conditions; its weak-coupling VCR is comparable to the $1.5 \times P_C$ RCM case. Note that with a higher-quality RX coil, the RCM operation with a longer resonance phase can potentially show a higher weak-coupling VCR.

Figure 4.8 compares the VCR of VM and RCM RX using both the models and simulations. From Figure 4.8(a) it can be seen that the RCM VCR outperforms the VM VCR over the entire k range from 0.001 to 0.02 at R_{OUT} = 10kΩ. In the weaker coupling region, the RCM RX still has a VCR that is at least double that of the VM RX. The calculated results from models show good fits with the simulated results; the small remaining error is mainly caused by the impedance matching approximation during the modeling process. Figure 4.8(b) shows the relationship between VCR and R_{OUT} at k = 0.025. Under this coupling condition, the VM RX slightly outperforms the RCM RX when a heavy load condition applies (R_{OUT} < 2kΩ). However, the RCM RX rapidly boosts the VCR when R_{OUT} increases. The maximum achievable RCM VCR is primarily determined by the load condition instead of the circuit topology, as is the case for VM RXs. As a result, the proposed RX can sustain the output voltage by switching to RCM operation and, in case of a very weak inductive link, simultaneously lightening its load condition (e.g., putting some loads into sleep).

Besides the open-loop VCR analyses, Figure 4.8(c) displays the relationship between the RX output power and k when the RX has a constant-output-voltage load, mimicking a regulating rectifier. The amplitude of the source voltage, $|V_S|$, is set to 1.8 V, determined by the required power level. Since the constant output voltage, V_{OUT}, sets a conducting threshold for the VM rectifier, the VM RX cannot harvest power from TX until k exceeds 0.007 (or 0.012) at V_{OUT} = 5 V (or 10 V). In contrast, the RCM RX can always harvest power from TX insensitive to k, thanks to its current-mode nature, thus achieving an extended operable coupling range. Based on the coil sizes in Table 4.1, the coil separation distance, D_{12}, can be approximated using the equation [4.2]

$$D_{12} = \sqrt{\left(\frac{{r_1}^2 \cdot {r_2}^2}{k \cdot \sqrt{r_1 \cdot r_2}}\right)^{\frac{2}{3}} - {r_1}^2} \tag{4.16}$$

to provide a more intuitive feeling of the extension feature. For miniaturized IMD applications with a smaller or higher resistance RX coil, the RCM operation promises an even more significant extension of the WPT range.

In summary, RCM RX provide significantly higher VCR and a much wider operable coupling range than VM RX, especially under weak coupling. Unlike VM operation, RCM can harvest power without a coupling threshold, making it well suited for miniaturized IMDs with variable and weak inductive links.

4.2.2 Three-Mode TX

The Class-D PA adopted at the TX side is shown in Figure 4.9. It has three operation modes. The detailed operation is explained in the following. The corresponding waveforms are shown in Figure 4.10.

1) Full-Bridge (2X) Mode: The Class-D PA works as a full bridge by activating all four power transistors to attain high output power. The two phases in the 2X mode are shown in Figure 4.9(a) and (b). The switching node swing, $V_{TX1} - V_{TX2}$, equals $2\times V_{IN}$.

2) Half-Bridge (1X) Mode: The PA works as a half-bridge by only activating M_{P1} and M_{N1}. M_{P2} keeps off and M_{N2} keeps on. Figure 4.9(c) and (d) show the two phases in the 1X mode. Since V_{TX2} is on the ground, the swing of $V_{TX1} - V_{TX2}$ is only V_{IN}.

3) Freewheeling (0X) Mode: By turning on M_{N1} and M_{N2} and turning off M_{P1} and M_{P2}, the PA is freewheeling with the residual energy in the L_1–C_1 tank. In the 0X mode, no power is drained from V_{IN}, and the swing of $V_{TX1} - V_{TX2}$ becomes near zero.

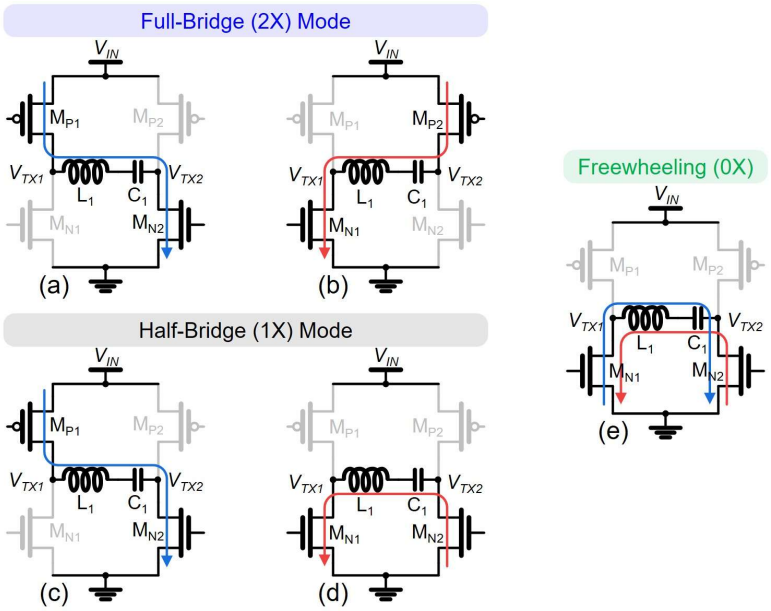


Figure 4.9 Operation principle of the three-mode TX. (a-b) Full-bridge (2X) operation mode. (c-d) Half-bridge (1X) operation mode. (e) Freewheeling (0X) mode.

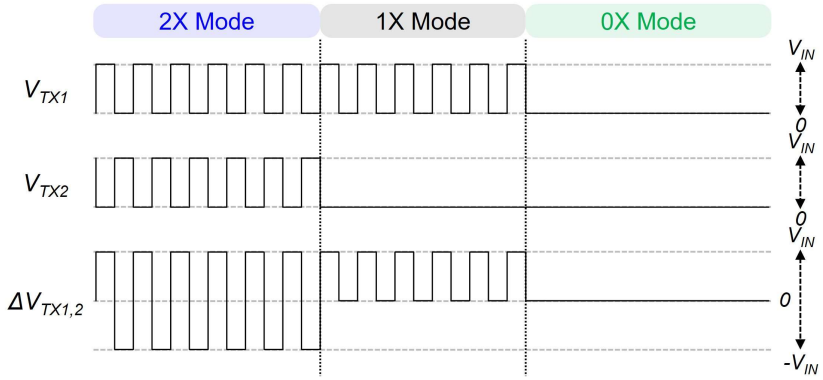


Figure 4.10 Operation waveform of the three-mode TX across different modes.

To achieve global power control, the TX alternates the operation between an active (2X or 1X) mode and the 0X mode. In the 2X mode, the TX emits 4× power of the 1X mode [4.7], [4.8], thus enhancing its heavy-load or weak-coupling performance. In contrast, the 1X-mode TX shows higher power efficiency by saving switching losses and reducing loop current, which also results in smaller V_{OUT} ripples. Therefore, the tradeoff between the output power and the power efficiency is optimized at TX by properly selecting the active mode, which will be further detailed in Section 4.3.2.

4.2.3 Global PWM Regulation

In a closed-loop WPT system, global power control should be tailored to meet the application requirements. Continuous control methods, such as supply modulation, are preferred for high-power (>1 W) applications [4.7], [4.9], [4.10], while discontinuous control methods are widely applied in sub-100-mW low-power applications. In [4.11], a global constant-idle-time control was reported, which deactivates the TX power stage for a certain period when the RX output voltage exceeds a threshold. Though this non-linear approach results in a stable loop and fast transient responses, it suffers from large voltage ripple in heavy-load conditions and limited light-load E2E efficiency. To address this, a global hysteretic control method was reported in [4.12], as shown in Figure 4.11(a). It improves light-load efficiency by incorporating longer idle periods; however, it necessitates additional power consumption at TX for LSK demodulation during the low-power mode. Furthermore, the low-power mode restricts the adjustable power range, thereby limiting its efficacy in accommodating varying coupling conditions [4.13].

Figure 4.11(b) depicts the proposed global PWM control. It adjusts the on/off duty ratio of the TX power stage by monitoring the PWM period. If the PWM period exceeds the predetermined reference duration, the TX will decrease the off time, and vice versa. Therefore, the heavy (or light) load condition corresponds to a short (or long) off period. Compared to the constant-idle-time control, the proposed PWM control achieves a better tradeoff between power efficiency and output ripple. Compared to the

hysteretic control, it only requires one LSK modem in each regulation cycle, allowing the TX power stage to have a reliable fully on/off operation without extra LSK-demanded power dissipation.

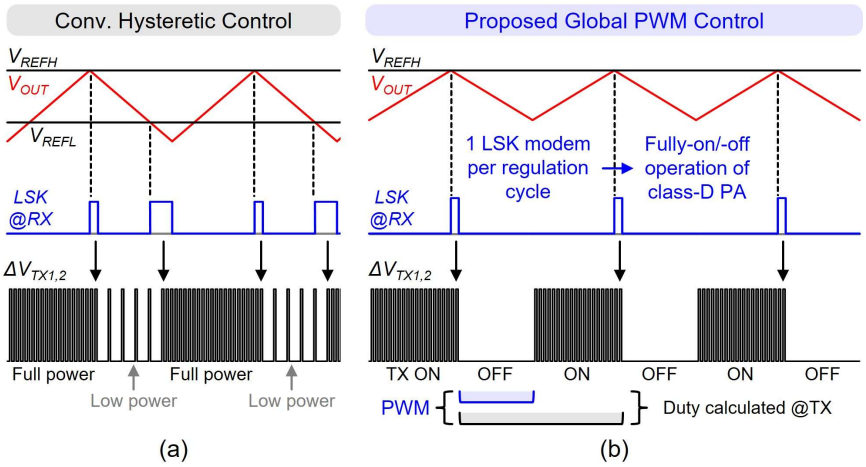


Figure 4.11 (a) Conventional hysteretic control. (b) Proposed global PWM control.

4.3 Circuit Implementations

Figure 4.12 shows the overall architecture of the proposed 13.56-MHz coupling-adaptive WPT system with in-band uplink data transfer. On the RX chip, S_{LC} and S_{LSK} are implemented by transmission gates. The three power switches, M_P, M_N, and S_{LC}, are each implemented using two switch segments with different sizes, as shown in Table 4.2. In CM operation, only one segment is enabled, while in VM operation both segments are turned on to support higher power levels. The sizes of M_P, M_N, and S_{LC} in CM are designed to balance switching loss and conduction loss under mid-range load conditions. In addition, S_{LC} is intentionally oversized in VM to act as a low-resistance conduction path with negligible switching activity. In this design, S_{LC} in VM has an on-resistance of approximately 50 mΩ.

Table 4.2 Aspect ratios of the power switches in the V/CM RX.

Switch	Width/Length in VM	Width/Length in CM
M_P	10.2mm/180nm (3mm/180nm + 7.2mm/180nm)	3mm/180nm
M_N	5mm/180nm (1.5mm/180nm + 3.5mm/180nm)	1.5mm/180nm
S_{LC} PMOS	20mm/180nm (6mm/180nm + 14mm/180nm)	6mm/180nm
S_{LC} NMOS	10mm/180nm (3mm/180nm + 7mm/180nm)	3mm/180nm

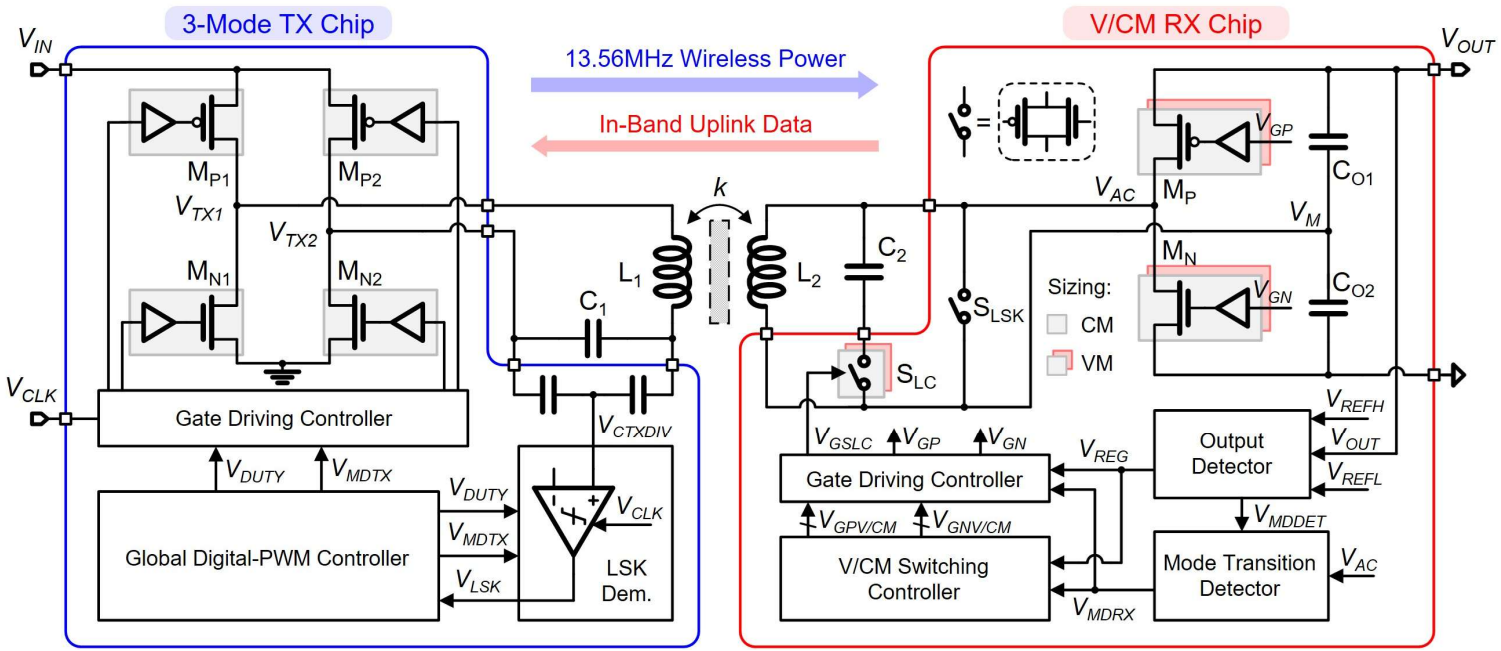


Figure 4.12 Overall architecture of the proposed coupling-adaptive WPT system.

The output voltage, V_{OUT}, is monitored by the output detector, which generates a regulation signal V_{REG} directly controlling S_{LSK} and a mode-transition detection trigger signal V_{MDDET}. Enabled by V_{MDDET}, the mode-transition detector performs open-circuit V_{AC} detection to commence mode transition between VM and CM. The switching controller determines the accurate turn-on/-off moments of M_P and M_N using an adaptive delay compensation technique. The gate driving controller at RX finalizes the gate voltages V_{GSLC}, V_{GP}, and V_{GN}. On the TX chip, the gate driving signals for the Class-D PA have been designed with dead time to avoid short circuits between V_{IN} and ground [4.14]. The global digital-PWM controller generates a regulation signal V_{DUTY}, reflecting the on/off duty ratio of TX, and chooses an active mode between 1X and 2X modes. The voltage-sensing LSK demodulator interfaces a divided voltage swing on C_1, using an on-chip capacitive divider, and sends the demodulated data, V_{LSK}, to the global digital-PWM controller.

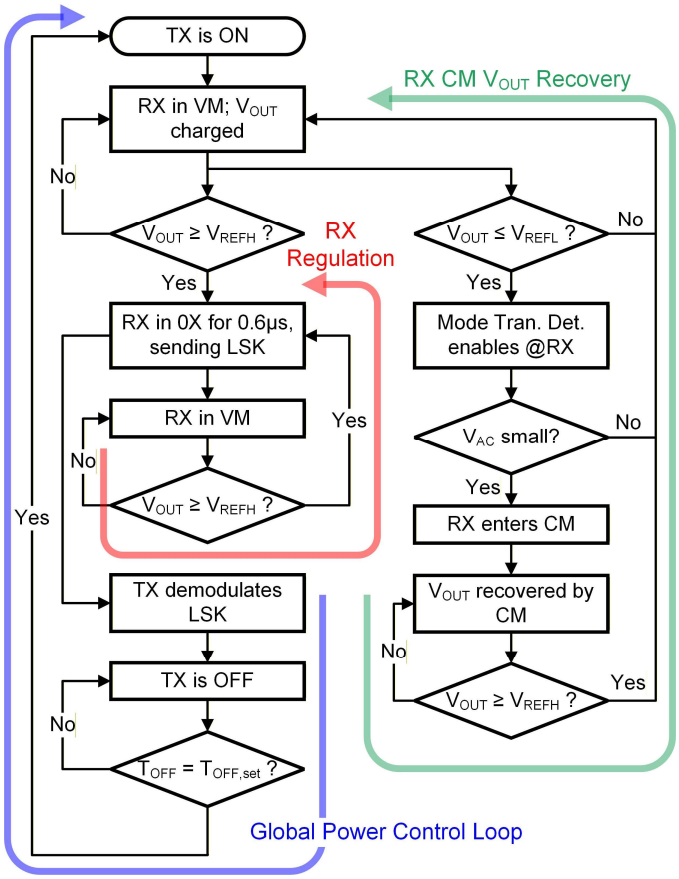


Figure 4.13 Operation flowchart of the proposed coupling-adaptive WPT system.

Figure 4.13 summarizes the operation flow of the proposed WPT system. It involves three main control loops: the global power control loop, the RX local V_{OUT} regulation loop, and the RX CM V_{OUT} recovery loop. The engagement of the loops depends on the coupling and loading conditions, which will be elucidated shortly.

4.3.1 Hybrid V/CM RX Implementation

Figure 4.14 shows the output detector and the mode transition detector at RX. V_{OUT} is compared to V_{REFH} using a StrongARM comparator clocked by inverted V_{GN}. Once V_{OUT} exceeds V_{REFH}, V_{REG} will present a 0.6-μs pulse, switching RX to 0X phase. If V_{OUT} continuously exceeds V_{REFH} after the 0X pulse, another 0X pulse will be immediately generated. The multi-pulse LSK signal can result in a more pronounced impedance change reflected at TX, enhancing the robustness of data transfer. Moreover, it inherently operates as constant-off-time control, serving as the RX local V_{OUT} regulation method, as will be demonstrated in the measurement section.

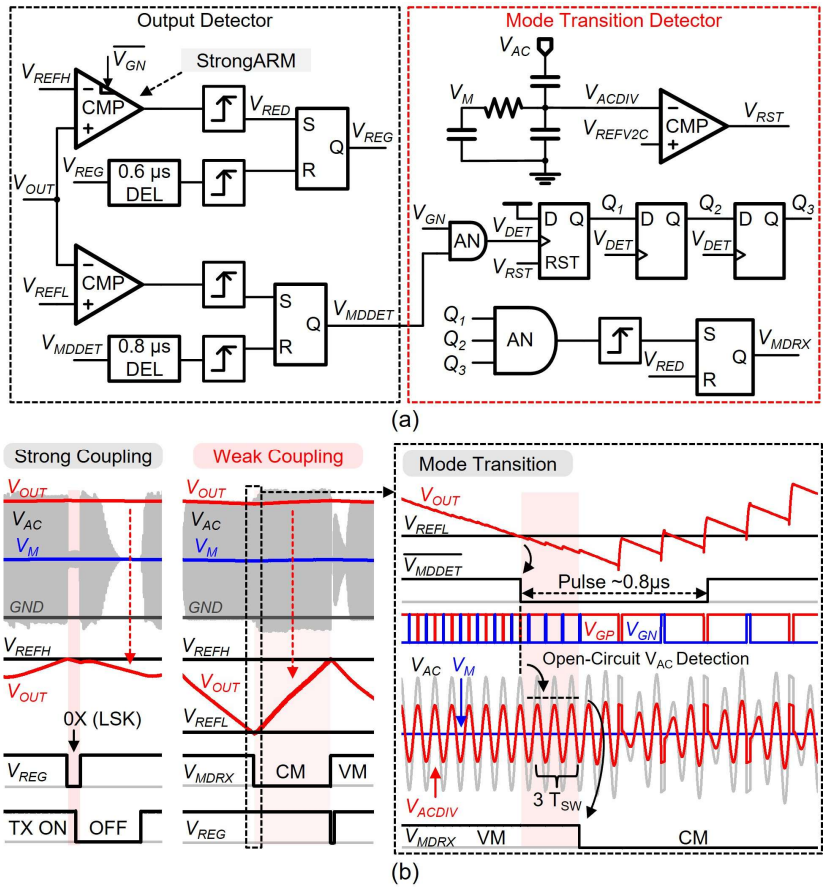


Figure 4.14 Output detector and mode transition detector at RX. (a) Implementation. (b) Operation waveform.

As shown in Figure 4.14, V_{MDDET} can generate a 0.8-μs pulse when V_{OUT} falls below V_{REFL}, initiating the mode transition detection (event driven). Instead of immediately switching to CM, an additional verification step is introduced to mitigate false triggers caused by unpredictable V_{OUT} undershoots. During the pulse, M_P is turned off, while M_N continues to operate as an active diode. This scenario indicates that the

RX alternates between the resonance phase and the VM C_{O2}-charging phase, as depicted in Fig. 4.2(d) and (b), respectively. In this configuration, the open-circuit V_{AC} can be detected because the L_2–C_2 tank is able to resonate freely during positive half cycles without being clamped by V_{OUT}. For reliable VM-to-CM transition, the divided version of V_{AC}, V_{ACDIV}, must remain below the threshold voltage V_{REFV2C} for three consecutive switching periods (T_{SW}) to reflect the weak-coupling condition. The CM-to-VM transition happens automatically upon V_{OUT} touching the upper boundary V_{REFH}.

Figure 4.15 shows the switching controller of M_P. Operating at 13.56 MHz, even a small control loop delay can result in significant switching errors in the power path [4.15], [4.16]. Therefore, a fast-responding adaptive delay compensation technique is adopted [4.17]. In the VM switching controller, the M_P turn-on moment is determined by a comparator with a delay-compensating input offset; the M_P turn-off moment is governed by a voltage-controlled delay line (VCDL). In the CM switching controller, the timing determination mechanism is similar to the VM loop, while an additional energy detector is added to monitor V_{AC} during the CM resonance phase. The CM switching controller generates gate signals for both M_P and S_{LC}. To prevent a short circuit from V_{OUT} to RX ground during the switching moment of both switches, a dead time is designed to slightly lag $V_{GPCMNOV}$ behind V_{GSLC}. A multiplexer selects V_{GP} from V_{GPVM} or $V_{GPCMNOV}$ based on V_{MDRX}. Thanks to the adaptive delay compensation, the complex control loop does not introduce additional power loss in the power path. The switching controller of M_N is implemented similarly, while M_P and M_N are enabled alternately for a balanced energy distribution between C_{O1} and C_{O2}.

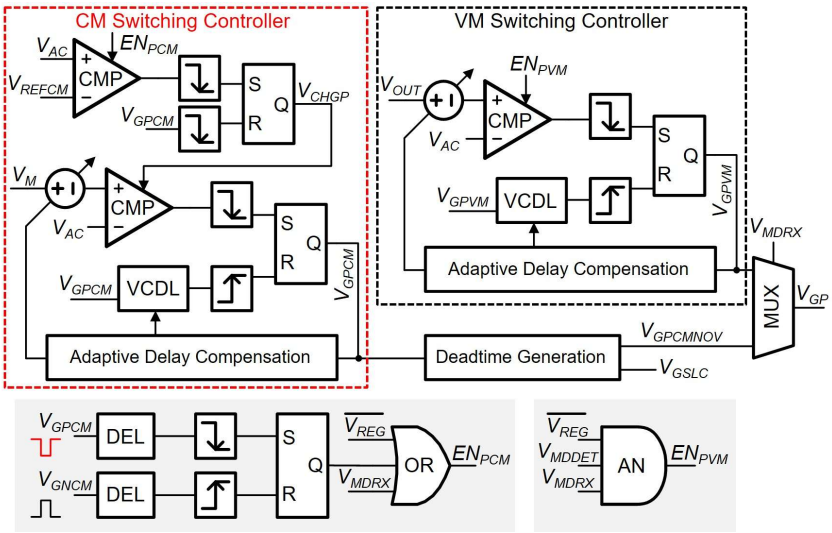


Figure 4.15 Switching controller of MP at RX.

4.3.2 Global Digital-PWM Controller

Using the global PWM control in WPT scenarios, the reference PWM duration should be selected to optimize the tradeoff between E2E efficiency and V_{OUT} ripple. A shorter PWM period helps achieve a smaller V_{OUT} ripple; however, this implies more frequent turn-on/-off of the PA at TX. In practice, the resonant wireless link requires start-up phases to build energy before commencing power transfer; moreover, considerable residual energy can remain in the L_1–C_1 tank after turning off the PA, only a small portion of which can be further transferred to RX. Thus, frequent turn-on/-off of the PA at TX often results in limited TX power efficiency and, thus, degraded E2E efficiency [4.13]. In this work, the reference PWM duration is set to 64 × T_{SW}, given the above tradeoff.

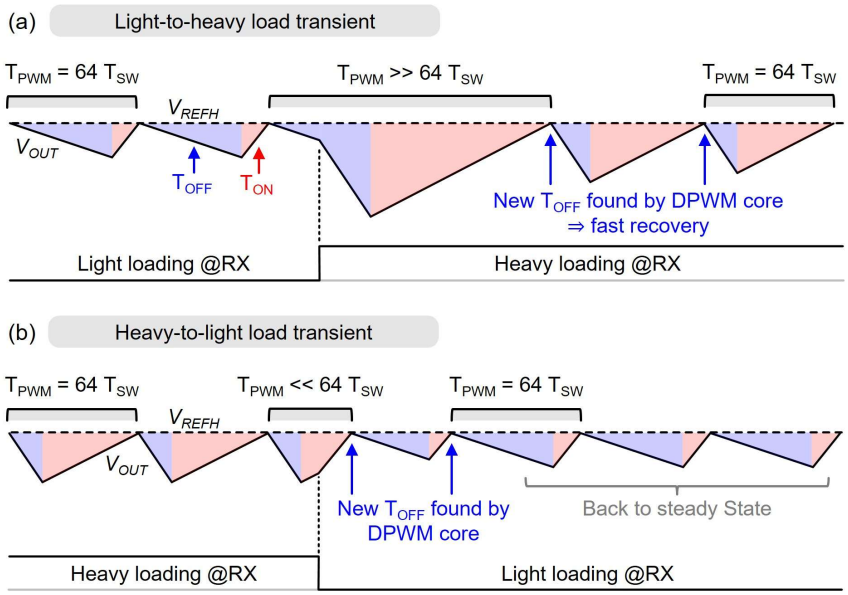


Figure 4.16 Operation principle of the proposed digital-PWM control. (a) Light-to-heavy load transient. (b) Heavy-to-light load transient.

Typically, a PWM control can be realized by comparing a sawtooth wave to a DC reference voltage, with frequency compensation ensuring loop stability. However, it suffers from slow load-transient responses and long settling times, resulting in large voltage ripples during light-to-heavy load transients and degraded E2E efficiency after heavy-to-light load transients [4.14]. To solve this, a digital PWM algorithm is proposed in this work, whose operation principle is shown in Figure 4.16. When one PWM period (T_{PWM}) ends by demodulating the LSK signal from RX, the TX directly calculates the next off time (T_{OFF}) based on the T_{PWM} and the last T_{OFF}. The relation can be expressed as follows:

$$\frac{T_{OFF}}{T_{PWM}} = \frac{T_{OFF,next}}{T_{PWM,set}} \tag{4.17}$$

where $T_{PWM,set}$ is 64 × T_{SW}. Therefore, in the steady state, T_{PWM} is regulated around 64 × T_{SW}. When light-to-heavy load transient happens, as shown in Figure 4.16(a), the TX requires a longer on time (T_{ON}) to charge up V_{OUT}. In the next PWM period, a distinct T_{OFF} will be calculated to accommodate the new on/off duty. Given that the transient can happen at any moment in a PWM period, the TX may also need another calculation to accurately track the new load condition at full scale. Benefiting from the non-linear digital-PWM algorithm, the system can achieve an up to 2 × T_{PWM} transient recovery within tens of microseconds, instead of several milliseconds using an analog loop [4.14]. A similar fashion applies to heavy-to-light load transients, as shown in Figure 4.16(b).

Based on (4.17), the TX needs calculations to find the next T_{OFF}. Compared to digital multipliers, using a lookup table (LUT) is a more efficient solution, given that T_{OFF} is limited in (0, 64). However, an LUT covering all T_{OFF}–T_{PWM} combinations still requires a large memory occupying an impractical silicon area. To solve this, a coarse-fine searching technique is proposed, as shown in Figure 4.17. In the coarse loop, T_{OFF} and T_{PWM} are counted by every 8 × T_{SW}, both of which are then mapped in an LUT. Hence, the LUT size can be reduced by 64×. If the coarse loop returns the same results for two consecutive T_{PWM}, the TX will switch to the fine loop, where the T_{OFF} will be incrementally adjusted by every single T_{SW} till T_{PWM} equals 64 × T_{SW}.

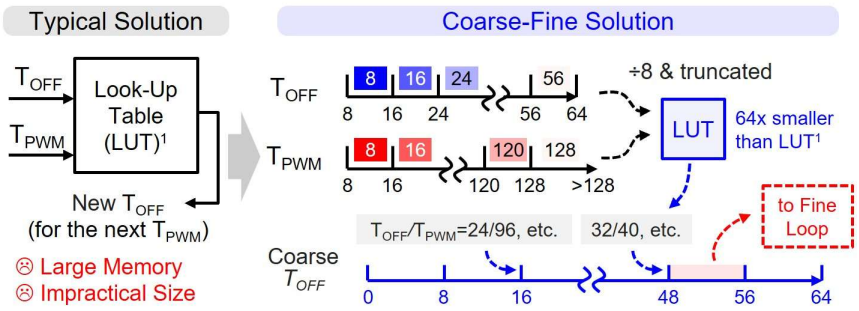


Figure 4.17 Proposed coarse-fine searching technique in the global digital-PWM controller.

Figure 4.18 shows the circuit implementation of the proposed global digital-PWM controller, with the operation waveform depicted in Figure 4.19. Besides T_{OFF}, the coarse loop also determines the active mode of TX. To optimize the tradeoff between output power and power efficiency, the 2X-mode of TX is activated only when the 1X-mode TX cannot supply sufficient power. This is detected by two conditions: 1) T_{OFF} equals 1 × T_{SW} with 1X-mode TX and 2) counted T_{PWM} exceeds 128 × T_{SW}. Condition 1) addresses steadily heavy-load cases. When the TX switches to 2X mode under condition 1), T_{OFF} is set to 8 × T_{SW}. Condition 2) handles unpredictable load transients, performing immediate 1X-to-2X mode transition without waiting for the end of the PWM period. The TX 2X-to-1X mode transition occurs when T_{OFF} exceeds 56 × T_{SW} in 2X mode, ensuring that the concurrent load condition can be easily handled by the 1X mode. When TX backs to the 1X mode, T_{OFF} is set to 32 × T_{SW}. A power overlap should

be applied between the prior 2X mode and the next 1X mode operation to avoid mode jumping back. Besides both loops, a logic clock generator, derived from the 13.56-MHz system clock V_{CLK}, is applied, generating distributed clock signals for blocks to prevent race hazard issues.

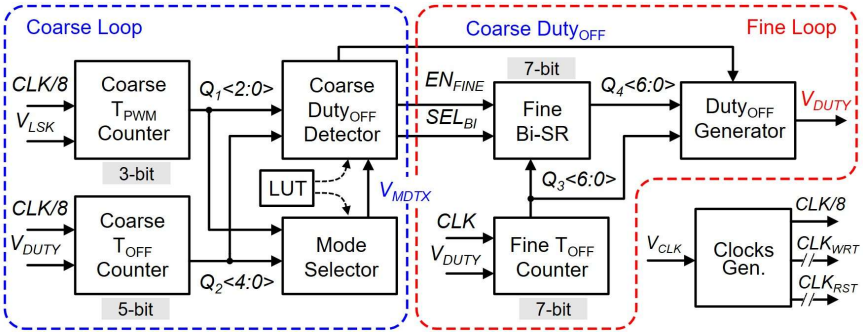


Figure 4.18 Global digital-PWM controller at TX.

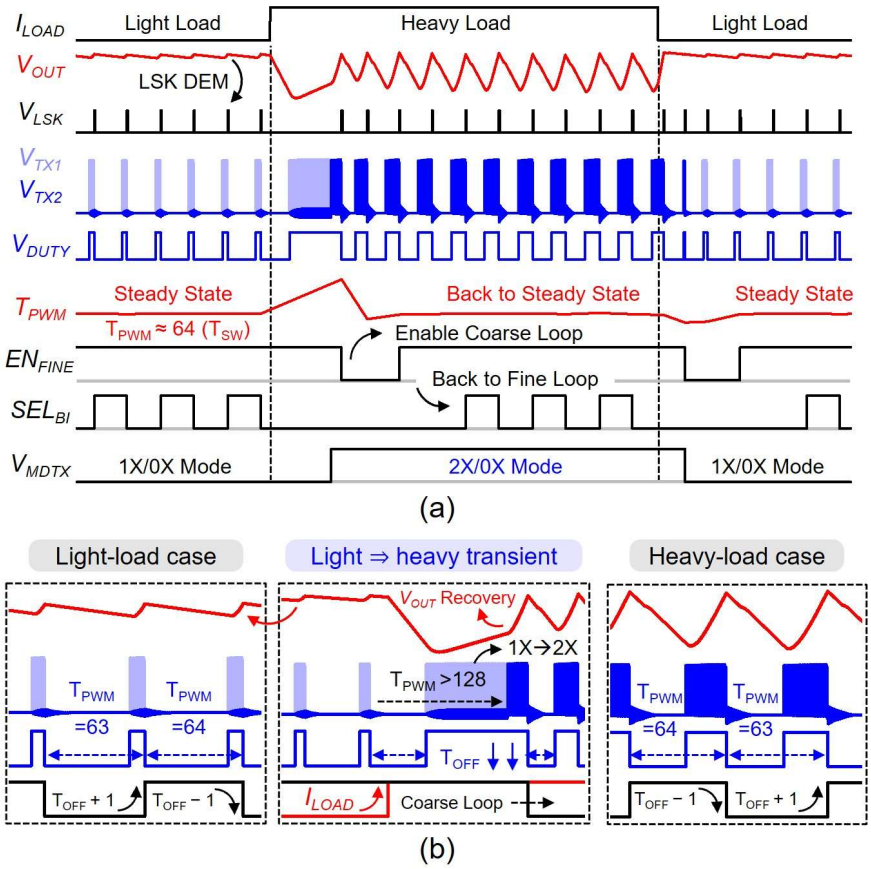


Figure 4.19 Operation waveform of the global digital-PWM controller at TX. (a) Load-transient waveform. (b) Zoomed-in waveform.

4.3.3 Voltage-Sensing LSK Demodulator

The data transfer between RX and TX is essential to achieve global power control. Traditionally, this is accomplished through wireless communication techniques such as Bluetooth or a dedicated data transfer link [4.18]. Since these solutions inevitably increase system cost and volume, in-band techniques have been recently developed to transfer data directly through the power link [4.19], [4.20], [4.21]. For RX-to-TX data transfer, LSK and frequency-shift-keying (FSK) are two appealing options [4.2]. However, many biomedical WPT systems require a fixed switching frequency to reduce electromagnetic interference (EMI) in adjacent signal processing units, making LSK the only viable solution.

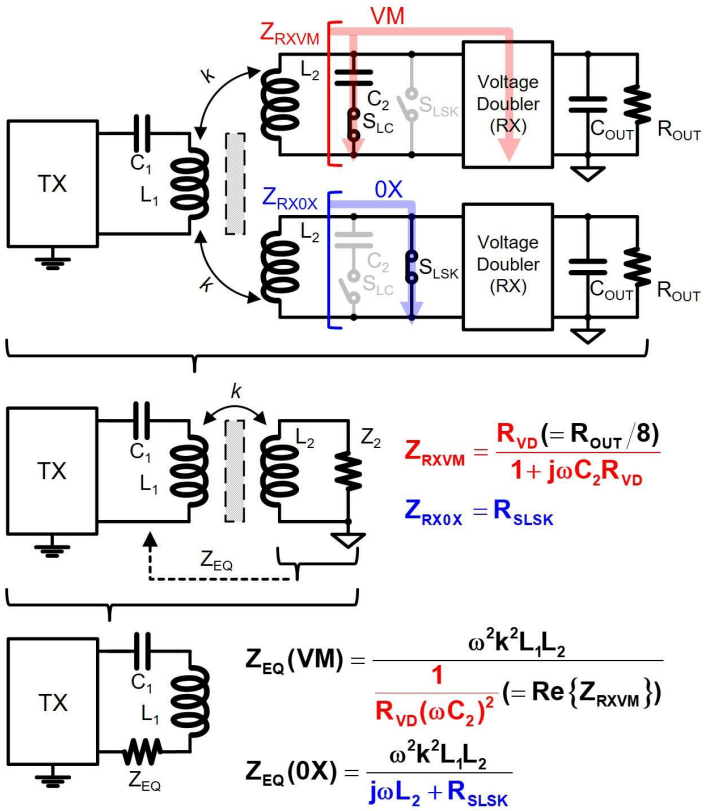


Figure 4.20 Principle of the in-band LSK-based RX-to-TX data transfer in the proposed system.

Figure 4.20 shows the principle of the LSK-based RX-to-TX data transfer in the proposed system. By changing the equivalent impedance of RX, Z_{RX}, the impedance difference will be reflected to TX, resulting in a loop current/voltage change at TX. When RX works in VM, Z_{RXVM} is regarded as the C_2 in-parallel connected with the VD. The input impedance of the VD can be approximated as (R_{OUT}/8) [4.22]. In contrast, Z_{RX0X} equals R_{SLSK} when RX is in the 0X phase. The reflected equivalent impedance of RX at the TX side, Z_{EQ}, can be expressed as [4.2]

$$Z_{EQ} = \frac{\omega^2 k^2 L_1 L_2}{j\omega L_2 + R_2 + Z_{RX}} \tag{4.18}$$

where k is the L_1–L_2 coupling coefficient and R_2 is the internal resistance of L_2. The Z_{EQ} expressions in different modes are shown in Figure 4.20.

Conventionally, the in-band LSK demodulation is performed using an off-chip sensing coil or an on-chip current sensor to detect the changes in the L_1–C_1 loop current at TX. This work proposes an LSK demodulation method that senses the voltage on C_1 (V_{C1}), as shown in Figure 4.21. Given that L_1 and C_1 resonate at the switching frequency, the rising edge of V_{CLK} aligns with the positive peak of V_{C1}. Hence, the TX simply utilizes a clocked comparator to detect the amplitude changes in V_{C1}, eliminating the need for envelope detectors and continuous-time amplifiers in conventional solutions. Figure 4.22 illustrates the implementation of the proposed LSK demodulator. To ensure safe voltage detection, V_{C1} is divided using an on-chip capacitive divider. Considering that V_{C1} can reach amplitudes of tens of volts, C_{DIV1} and C_{DIV2} were implemented using high-voltage metal–oxide–metal capacitors. In addition, the input pairs of the post comparators were designed with 5-V MOSFETs instead of 1.8-V ones, providing sufficient margin for V_{C1DIV} swing. The distorted V_{C1DIV} waveform in 2X-mode TX, caused by the level shift of V_{TX2}, will not affect the amplitude detection because V_{TX2} is at the ground during the V_{CLK} (also CLK_D) rising edge.

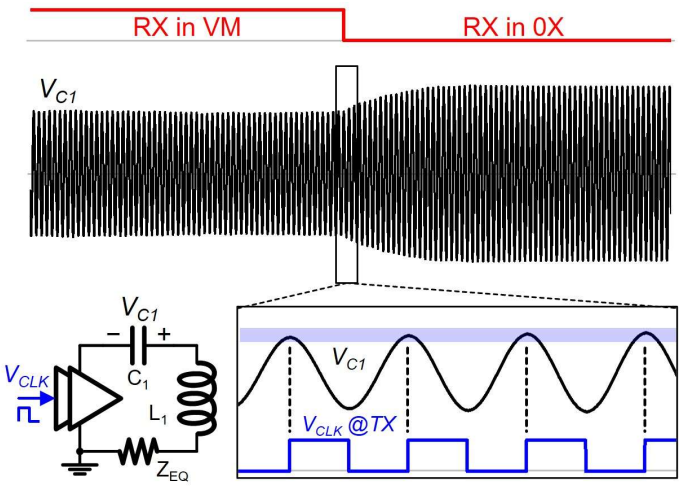


Figure 4.21 Operation principle of the voltage-sensing LSK demodulation at TX.

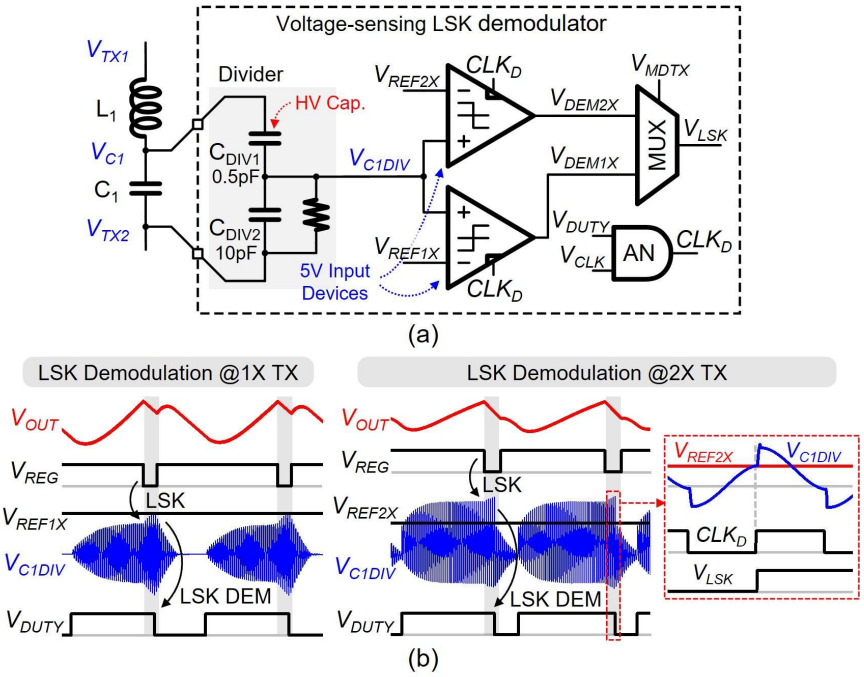


Figure 4.22 Voltage-sensing LSK demodulator at TX. (a) Implementation. (b) Operation waveform.

4.4 Measurement Results

The prototype TX and RX chips were fabricated in a 180-nm CMOS process, mostly using 1.8-V MOSFET devices. As shown in Figure 4.23, the TX and RX chips occupy 0.8- and 0.9-mm^2 silicon area, respectively, excluding pads. Both chip areas are dominated by input and output decoupling capacitors, which can be removed if off-chip capacitors are used.

In the experimental measurement setup, as shown in Figure 4.24, off-chip buffer capacitors of 330 nF were added for each of C_{O1} and C_{O2} at RX. The TX chip is powered by a 1.8-V DC supply. Measured by an impedance analyzer, the PCB coil L_1 has an inductance of 1.39 µH at 13.56 MHz with a 30-mm outer diameter, while L_2 is 295 nH with a 20-mm outer diameter. Both single-layer coils have a 0.7-mm trace width and 60-µm copper thickness. C_1 and C_2 have capacitance of 100 and 470 pF, respectively. The coil distance between L_1 and L_2 can be adjusted to mimic the varying coupling conditions in real-world applications.

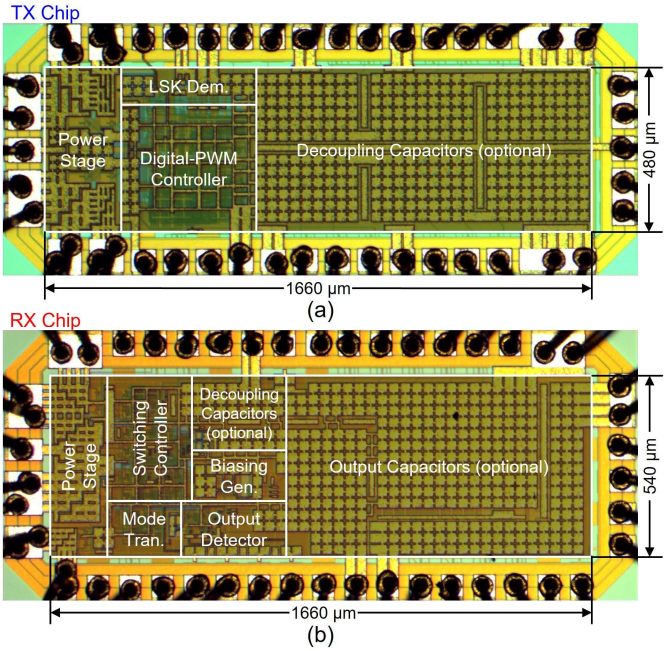
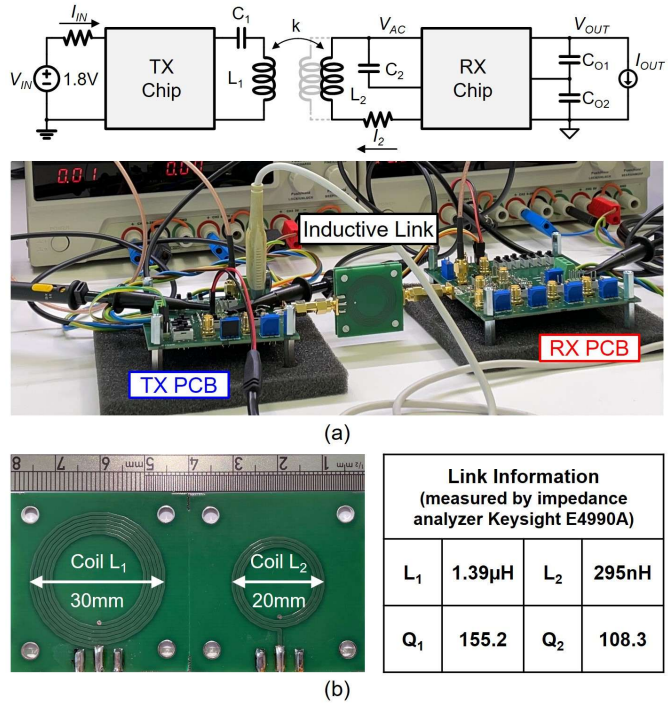


Figure 4.23 Chip micrograph. (a) TX chip. (b) RX chip.



Link Information (measured by impedance analyzer Keysight E4990A)			
L_1	1.39µH	L_2	295nH
Q_1	155.2	Q_2	108.3

Figure 4.24 Measurement setup. (a) Testbench schematic and photograph. (b) Inductive link information.

Figure 4.25 shows the measured steady-state operation when the coil distance is 1.25 cm, and the load current, I_{OUT}, is 30 mA. In this strong-coupling and heavy-load

condition, the RX switches its operation between VM and 0X, regulating V_{OUT} at 1.8 V with the help of the global PWM control. The measured V_{OUT} exhibits ripples around 100 mV. The TX operates in 2X/0X mode to accommodate the heavy load. Through global PWM control, T_{PWM} is stabilized at 64 × T_{SW}, with a constant on/off duty ratio.

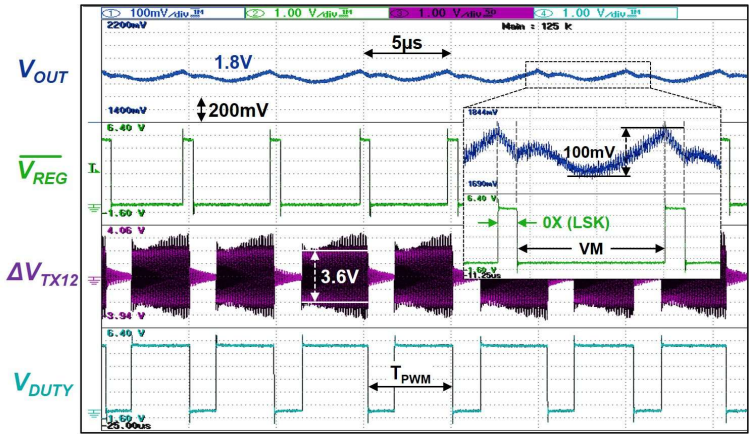


Figure 4.25 Measured steady-state operation with 30-mA I_{OUT} at 1.25-cm coil distance.

With the same coil distance, Figure 4.26 shows the measured steady state when I_{OUT} decreases to 1.8 mA. Due to this light load, V_{OUT} can increase after turning off the TX by harvesting the residual energy in the L_1–C_1 tank. Hence, it is observed that the RX uses a second 0X pulse to achieve local V_{OUT} regulation. In this state, V_{OUT} shows a 25-mV ripple, while the TX operates in 1X/0X mode.

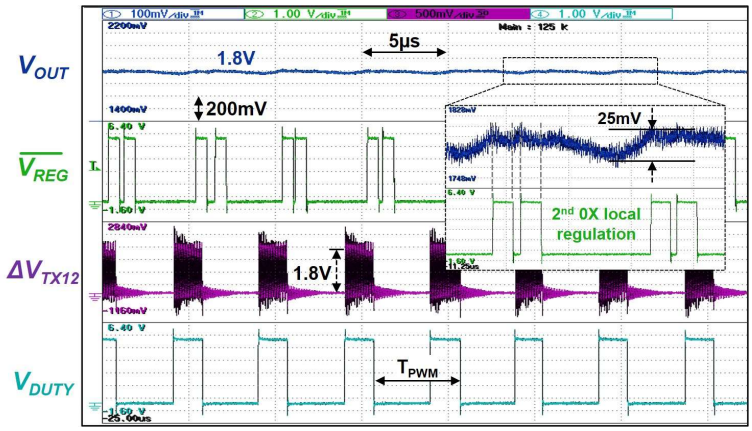


Figure 4.26 Measured steady-state operation with 1.8-mA I_{OUT} at 1.25-cm coil distance.

Figure 4.27 illuminates the LSK modem process for RX-to-TX data transfer in the proposed WPT system. It is observed that V_{C1DIV} presents a clear increase in amplitude when the RX enters the 0X phase. By detecting the amplitude increase using the proposed voltage-sensing LSK demodulator, the RX data is recovered at TX, facilitating global power control.

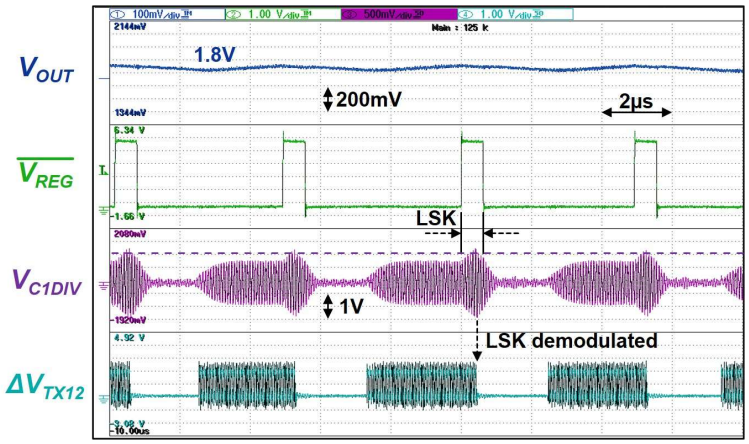


Figure 4.27 Measured LSK-based RX-to-TX data transfer with the proposed voltage-sensing LSK demodulation.

Figure 4.28 exhibits the measured coupling-transient response as the coil distance increases when TX continuously operates in 2X mode. It is observed that by moving apart the TX and RX coils, it becomes increasingly challenging for VM operation to regulate V_{OUT} at 1.8 V. To compensate, CM operation is engaged more frequently to stabilize and recover V_{OUT}.

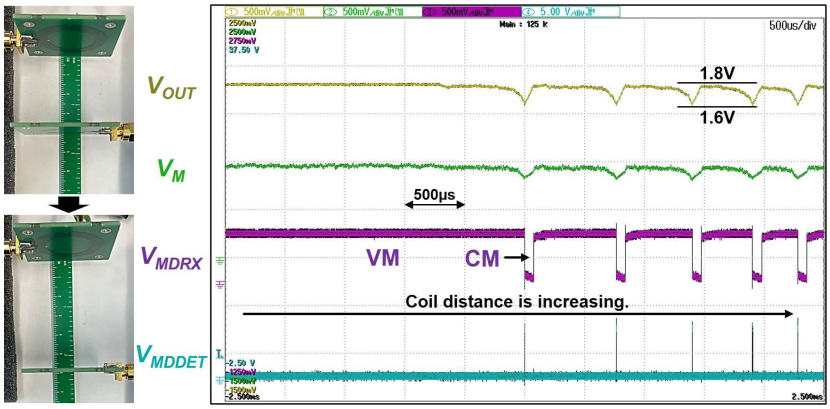


Figure 4.28 Measured coupling-transient response with an increasing coil distance with the proposed V/CM RX.

Figure 4.29 illustrates the measured steady-state operation when the coil distance is increased to 5.5 cm. Given the weak-coupling condition, the RX cannot maintain V_{OUT} at 1.8 V through the VM operation. When V_{OUT} drops below 1.6 V, V_{MDDET} goes high to enable the VM-to-CM transition detection, and the RX switches to CM after detecting the open-circuit V_{AC}. It is observed that V_{OUT} is recovered during the CM operation. In this steady state, the RX alternates between VM and CM, regulating V_{OUT} in a 200-mV hysteretic window. Once the coupling condition strengthens sufficiently for the VM RX to charge up V_{OUT}, the RX will not go back to CM, and the global power control will be resumed.

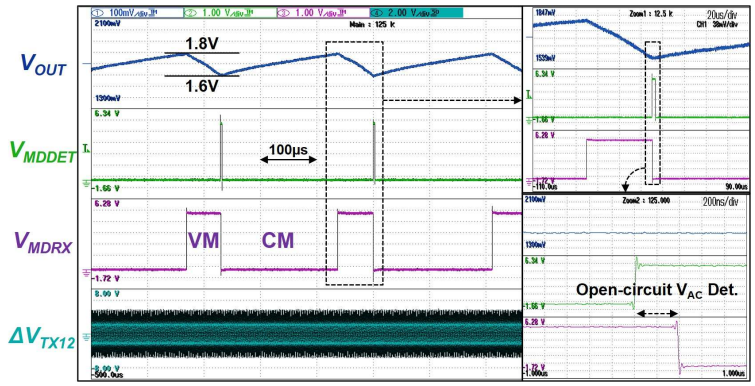


Figure 4.29 Measured steady-state operation with 0.5-mA I_{OUT} at 5.5-cm coil distance.

The measured zoomed-in operation waveform at RX is depicted in Figure 4.30. The VM operation is shown in Figure 4.30(a), where the RX operates as a full-wave VD. It is observed that adaptive delay compensation calibrates the turn-on/-off moment of M_P and M_N, achieving zero-voltage switching (ZVS). In the CM operation shown in Figure 4.30(b), the energy accumulation behavior is observable during the resonance phase, given an increasingly larger V_{AC} amplitude. The charging phases for C_{O1} and C_{O2} happen alternately. Benefiting from the adaptive delay compensation, it is observed that ZVS is achieved at both the start and end moments of the charging phases.

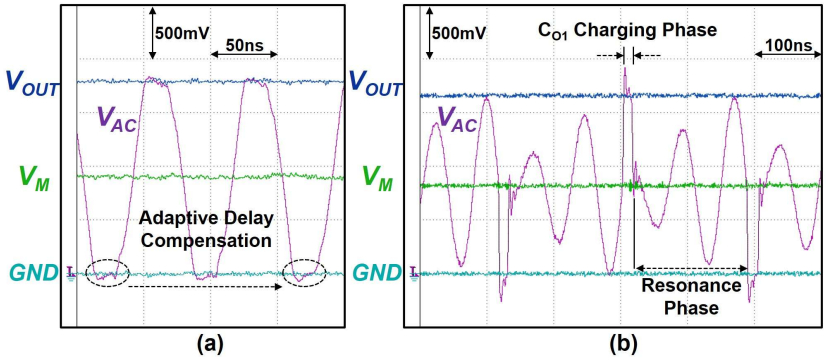


Figure 4.30 Measured zoomed-in RX waveform. (a) VM operation. (b) Resonant CM operation.

The load-transient operation was measured when I_{OUT} changes between 0.18 and 5.3 mA, with a 10-ns rise/fall time and a coil distance of 0.5 cm. The waveform is shown in Figure 4.31. During the light-to-heavy transient, a 75-mV undershoot is observed, and V_{OUT} is recovered within 8 µs. Once the transient T_{PWM} is over, the digital-PWM controller at TX calculates the on/off duty ratio and generates a new T_{OFF} in the next T_{PWM}, as verified in Figure 4.31. Thus, the system backs to the steady state after the 8-µs recovery time, showing a fast transient response. During the heavy-to-light transient, no overshoot is observed, thanks to the instant LSK-based RX-to-TX communication and the RX local V_{OUT} regulation, and the system backs to the steady state in 2 × T_{PWM}.

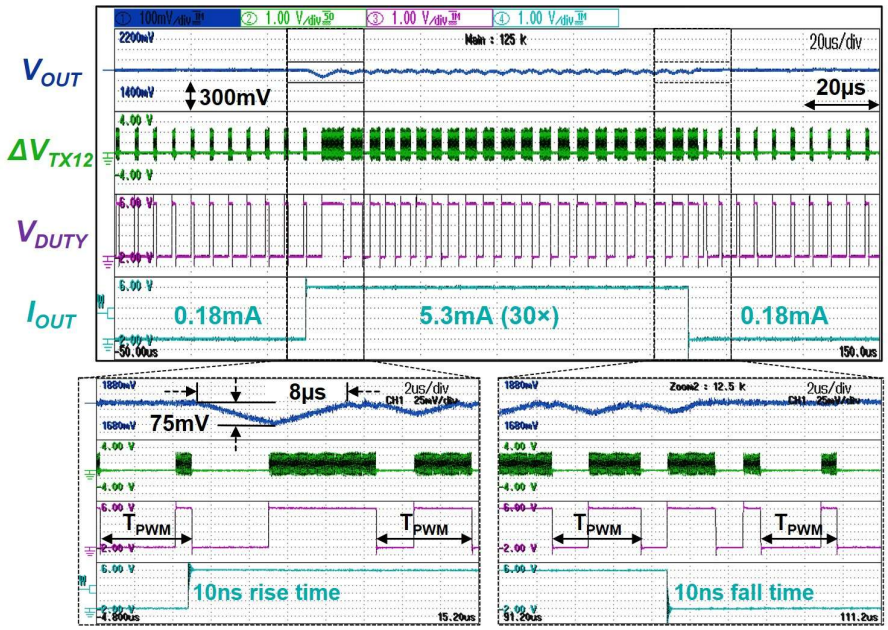


Figure 4.31 Measured load-transient operation with I_{OUT} between 0.18 and 5.3 mA at 0.5-cm coil distance.

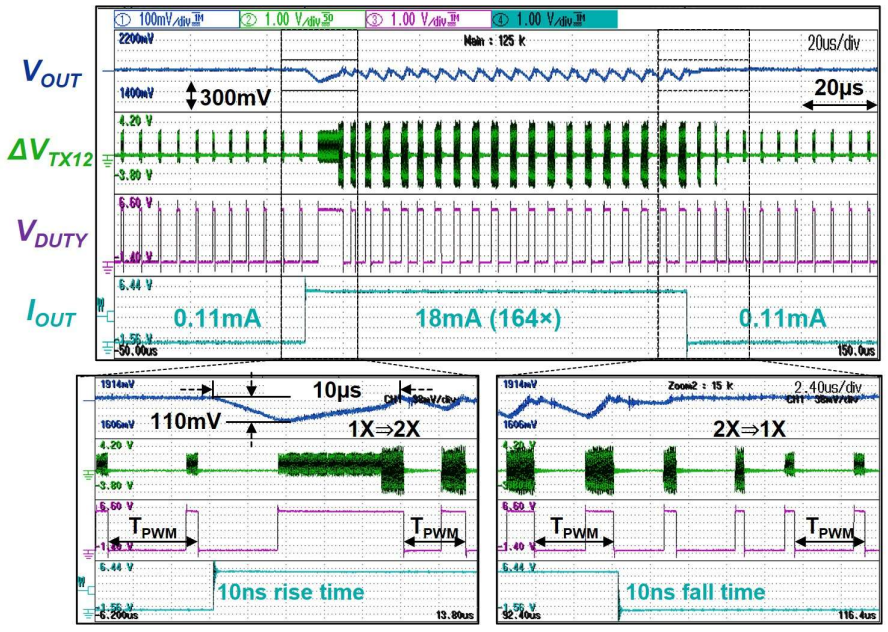


Figure 4.32 Measured load-transient operation with I_{OUT} between 0.11 and 18 mA at 0.5-cm coil distance.

Figure 4.32 shows the measured load-transient operation when I_{OUT} changes between 0.11 and 18 mA. During the light-to-heavy transient, V_{OUT} depicts a 110-mV undershoot, which is then recovered within 10 µs. To accommodate the resulting 18-mA heavy load, the TX switches from 1X/0X to 2X/0X operation. The heavy-to-light

transient happens with unnoticeable overshoots, and the TX reverts to 1X/0X operation afterward, catering to the light load. Fast transient recovery is also observable during this load transient, thanks to the digital-PWM control strategy.

By integrating the CM operation at RX, the system survives in weaker coupling conditions with longer coil distances between L_1 and L_2, namely, the WPT range. The measured results are shown in Figure 4.33. With the 1X-mode TX, it is observed that the proposed V/CM RX achieves 1.5× wider WPT range compared to the VM operation at I_{OUT} of 0.18 mA. The widest WPT range reaches 6 cm when the TX operates in 1X/0X-mode. Furthermore, employing the 2X/0X-mode TX extends the WPT range to 7 cm at the same I_{OUT}, showing a 1.4× extension compared to VM operation. Figure 4.33(c) shows the relationship between the maximum operable coil distance and I_{OUT} for various operational configurations. It is observed that the V/CM RX significantly improves V_{OUT} regulation at 1.8 V compared to merely increasing the TX power from 1X to 2X mode. By utilizing both V/CM RX and 2X-mode TX, the maximum operable coil distance is further extended beyond the baseline performance achieved with 1X-mode TX and VM-only RX. The system attains its widest WPT range of 7.2 cm at I_{OUT} of 0.1 mA.

The power efficiency was measured at $V_{IN} = V_{OUT} = 1.8$ V, as shown in Figure 4.34(a)–(e). Figure 4.34(a) shows the measured E2E efficiency at 0.5-cm coil distance utilizing different regulation methods. It is observed that the peak E2E efficiency of the proposed system achieves 72.3% at $I_{OUT} = 12$ mA, with TX in 1X/0X mode. When the TX operates in 2X/0X mode, the E2E efficiency reaches the peak of 71.4% at $I_{OUT} = 39$ mA. With the global PWM power regulation, up to 40.5% and 30.4% enhancements in E2E efficiency are achieved compared to the scenarios where the output regulation solely relies on RX while the TX stays operating in the 1X- and 2X-only modes, respectively. The maximum output power is achieved at 81 mW. Figure 4.34(b) and (c) shows the measured E2E efficiency at various coil distances. The E2E efficiency is the product of the TX efficiency, the wireless link efficiency [or power transfer efficiency (PTE)], and the PCE at RX. As the coil distance increases, the link efficiency decreases, leading to both reduced E2E efficiency and lower output power. When the coil distance reaches 5 cm, the V/CM operation takes over at RX, accommodating the low input power at RX. Moreover, Figure 4.34(d) and (e) presents the measured PCE at RX. The peak PCE of 92.7% is obtained when I_{OUT} is 12 mA at 1.27-cm coil distance. When the distance is set to 5 and 6 cm, the RX operates in V/CM. Figure 4.34(f) shows the measured coupling coefficient versus coil distance using an impedance analyzer.

Table 4.3 benchmarks this work against recently reported WPT systems. The proposed system achieves a wide WPT range, improving the weak-coupling performance, thanks to the hybrid-mode RX. Benefiting from the global digital-PWM power modulation, it also realizes high E2E efficiency, fast load-transient recovery, small output voltage ripple with sub-μF output decoupling capacitors, and a high integration level.

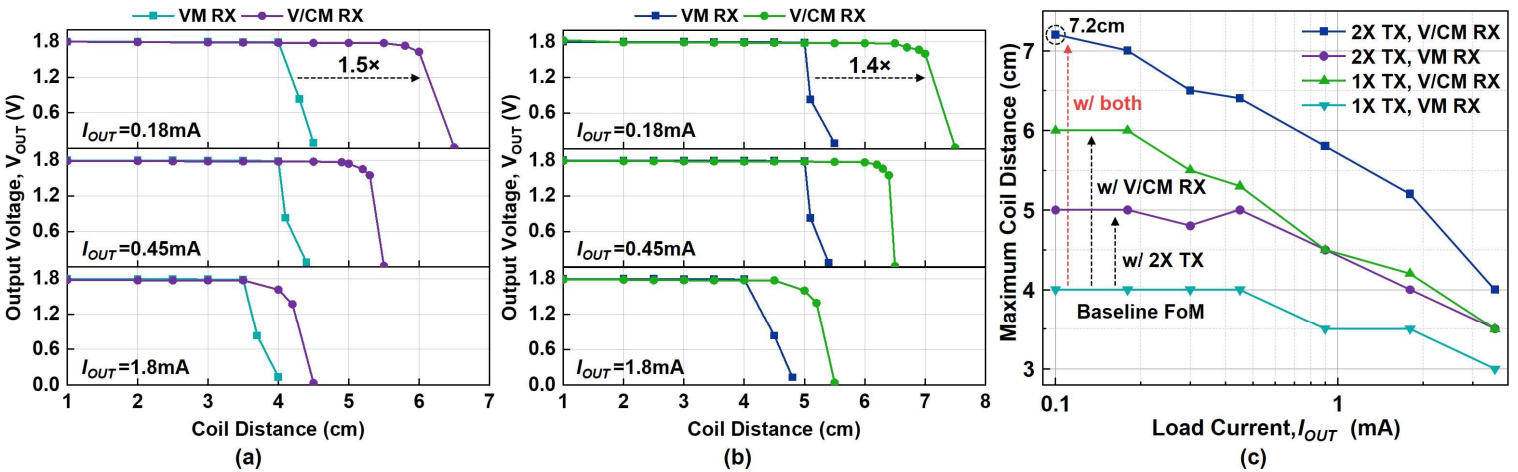


Figure 4.33 Measured WPT range in different I_{OUT} conditions. (a) With 1X-mode TX. (b) With 2X-mode TX. (c) Measured maximum coil distance versus I_{OUT}.

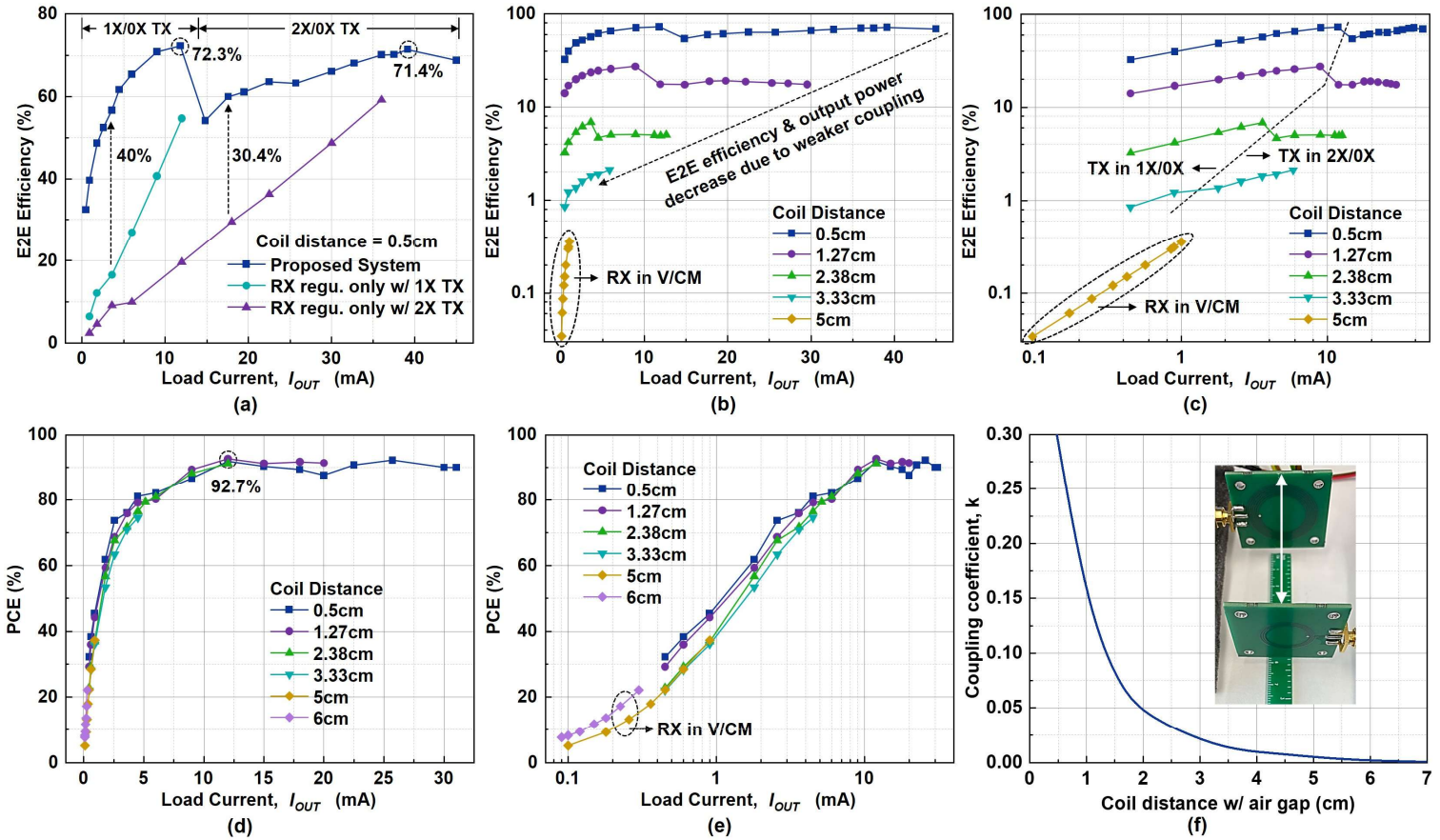


Figure 4.34 Measured power efficiency. (a) E2E efficiency versus I_{OUT} with different regulation methods. (b) and (c) E2E efficiency versus I_{OUT} under different coupling conditions. (d) and (e) PCE versus I_{OUT} at RX under different coupling conditions. (f) Measured coupling coefficient versus coil distance with air gap.

Table 4.3 Comparison to state-of-the-art designs.

	TBCAS' 15 [4.9]	**JSSC' 18 [4.11]**	**JSSC' 21 [4.7]**	**JSSC' 22 [4.12]**	**TBCAS' 22 [4.14]**	**JSSC' 23 [4.23]**	**This Work**
Technology	350nm CMOS	65nm CMOS	250nm CMOS	180nm CMOS	180nm CMOS	180nm CMOS	**180nm CMOS**
WPT Architecture	Series-Parallel	Series-Parallel	Series-Series	Series-Parallel	Series-Parallel	Series-Series	**Series-Parallel**
TX Topology	Buck + Class-D	Class-D	Diff. Class-D	Class-D	3-Mode Class-D	Diff. Class-D	**3-Mode Class-D**
RX Topology	1X/2X FBR	FBR	FBR	FBR	FBR	FBR	**V/CM VD**
Frequency (MHz)	13.56	13.56	6.78	6.78	13.56	6.78	**13.56**
Coil Diameter (cm)	TX 5; RX 1	TX 3.5; RX 2	TX 4.5; RX 4.5	TX 3.2; RX 2.5	TX 4; RX 2.2	TX 5; RX 5	**TX 3; RX 2**
Off-Chip Components (exclude WPT link)	1 coil, 2 C_{OUT}, 1 global controller	1 coil, 1 C_{OUT}	1 coil, 1 C_{OUT}, 1 data demodulator	1 C_{OUT} (8μF)	1 coil, 1 C_{OUT} (2.2μF)	1 C_{OUT} (10μF)	**2 C_{OUT} (330nF each)**
Global Regulation Method	Supply modulation	Constant off-time	PWM (CCM)	Hysteretic	PWM (DCM)	PWM (CCM)	**Digital-PWM (DCM)**
Global Data Link (Fully integrated ?)	Wireless LSK (No)	Wireless LSK (No)	Wireless LSK (No)	Wireless LSK (Yes)	Wireless LSK (No)	Wireless Phase Shift (Yes)	**Wireless LSK (Yes)**
Data Demodulation @TX (Implementation)	I_1 Sensing (3^{rd} coil)	I_1 Sensing (3^{rd} coil)	I_1 Sensing (3^{rd} coil)	I_1 Sensing (Current Sensor)	I_1 Sensing (3^{rd} coil)	Phase Shift Detector	**V_{C1} Sensing (Comparator)**
V_{IN} @TX / V_{OUT} @RX (V)	(N/R) / 3.8	2.5 / (1.2-2.5)	5 / 5	1.8 / (1.1-1.8)	(N/R) / 3.3	3.3 / 3.3	**1.8 / 1.8**
V_{OUT} ripple (mV) @I_{OUT}	N/R	100 @10mA	200 @50mA	75 (Hysteretic)	100 @16.5mA	N/R	**25 @ 1.8mA; 100 @30mA**
Max. Output Power (mW) (@D_{coil})	234 (@0.3cm)	49.4 (@0.6cm)	400 (@0.3cm)	63 (@0.65cm)	162 (@0.3cm)	900 (@2cm)	**81 (@0.5cm)**
Load Tran. Recovery (μs) (@Step Ratio)	2000 (@1:10)	0 (@1:10)	820 (@1:3)	0 (@1:3)	1100 (@1:10)	70 (@1:4)	**10 (@1:164)**
Max. WPT Range (cm) (@I_{OUT})	1.8 (@13.5mA)	1.15 (@4mA)	0.3 (@50mA)	1.15 (@22mA)	1 (@21mA)	2 (@273mA)	**7.2 (@0.1mA); 5.2 (@1.8mA)**
Peak E2E Efficiency (@D_{coil})	62.4% (@0.3cm)	70.6% (@0.6cm)	71.5% (@0.3cm)	68.9% (@0.7cm)	70.1% (@0.1cm)	77% (@1.5cm)	**72.3% @1X TX; 71.4% @2X TX (@0.5cm)**

N/R: not reported; CCM: continuous conduction mode; DCM: discontinuous conduction mode.

4.5 Concluding Remarks

In this chapter, a new class of rectifier, hybrid voltage-/current-mode (V/CM) rectifier, has been proposed, combining the strengths of voltage-mode (VM) rectifiers and resonant-current-mode (RCM) rectifiers. A closed-loop WPT system using the V/CM RX has been implemented, fabricated, and experimentally validated.

The V/CM rectifier extends the voltage doubler by adding a power switch in the resonant-capacitor branch to enable RCM operation. Autonomous mode-transition is achieved using an event-driven quasi-open-circuit V_{AC} detection scheme. In addition, the hybrid-mode principle is theoretically modeled and analyzed.

By employing the V/CM RX, the WPT system demonstrates an up to 50% wider transfer range compared with the VM-only approach. With global digital-PWM control, it yields 72.3% peak end-to-end efficiency and fast load-transient recovery. Joint adaptability at both the RX and TX enables robust operation across wide coupling and load variations, making the system well suited for reliable and resilient IMD applications.

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Chapter 5 Resonant-Current-Mode Techniques

In Chapter 4, a voltage-/current-mode (V/CM) receiver (RX) was investigated, demonstrating improved input sensitivity compared with voltage-mode (VM) RXs. In this circuit, resonant-current-mode (RCM) operation is employed to recover the output voltage that cannot be sustained by VM and is therefore primarily activated under weak coupling. This approach relies on the prerequisite that VM operation can provide a sufficient voltage conversion ratio (VCR) under normal coupling.

However, the VCR of VM rectifiers is inversely proportional to the RX coil inductance [5.1]. Consequently, as RX coils are miniaturized, their reduced inductance progressively narrows the operable range of VM topologies, particularly in high-voltage (HV) applications such as neural stimulation. In contrast, RX coil miniaturization also mitigates over-voltage risks in RCM. As a result, pure RCM topologies emerge as a compelling solution for highly miniature implantable medical devices (IMDs).

Driven by this need, this chapter investigates two RCM-based designs. The first is a regulating three-phase RCM rectifier that overcomes key limitations of prior RCM topologies, achieving high power conversion efficiency (PCE) and in-situ output regulation. The second is a 40.68-MHz WPT system built upon the proposed three-phase RCM RX, leveraging RCM's adaptive VCR to facilitate RX coil miniaturization. The system enables an 8-mm-diameter RX coil, achieving an approximately sixfold reduction in form factor compared with state-of-the-art designs.

5.1 A Regulating Three-Phase Resonant-Current-Mode Rectifier[4]

5.1.1 Motivation

As shown in Chapters 3 and 4, state-of-the-art VM designs can readily achieve over 90% PCE and output power exceeding 100 mW, benefiting from mature rectifier topologies and advanced delay-compensation techniques. In addition, in-situ output regulation can be integrated with minimal performance degradation.

[4]based on: T. Lu and S. Du, "A Three-Phase Regulating Resonant-Current-Mode Rectifier With Bypass-Capacitor Residual-Free Charging for Wireless Power Transfer," in IEEE Journal of Solid-State Circuits, doi: 10.1109/JSSC.2025.3597069.

In contrast, most reported RCM rectifiers operate mainly in weak-coupling, unregulated conditions, exhibiting peak output power of only a few tens of milliwatts and PCE below 90%, which will be detailed in this section. This performance gap highlights the challenge of replacing VM RXs with existing RCM solutions.

The limitations of prior RCM topologies stem from either excessive voltage swing during the resonance phase or residual energy during the charging phase, as well as the absence of in-situ output regulation. To address these issues, Section 5.1 proposes a three-phase RCM topology, incorporating a bypass-capacitor-based residual-free charging mechanism and a freewheeling phase. The proposed design achieves over-200-mW maximum output power with a peak PCE of 94.5%.

5.1.2 Rectifier Topology Analysis

In Chapter 4, the open-loop VCR in both VM and RCM was modeled and analyzed, which is helpful to understand the RCM nature and motivate V/CM mode switching under weak coupling. In this section, to provide a more complete view of rectifier design, the trade-offs between VM and RCM topologies in terms of output power and PCE are evaluated.

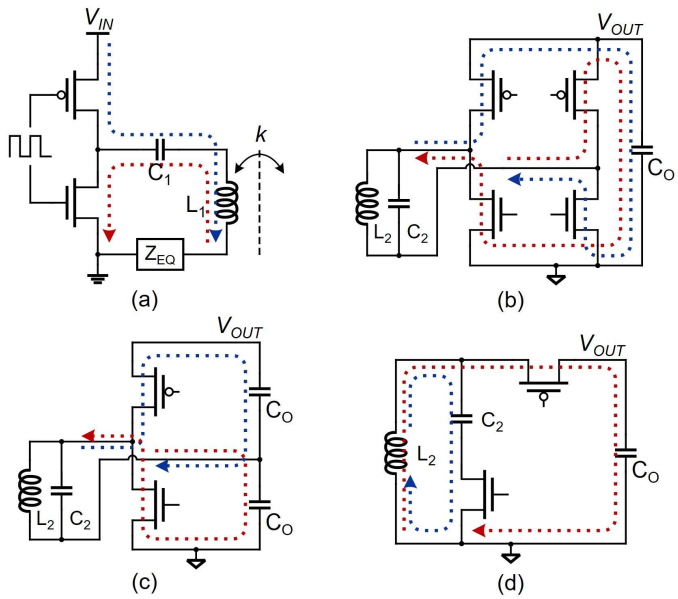


Figure 5.1 WPT interfacing circuits in analysis. (a) TX Class-D power amplifier. (b) RX VM full-bridge rectifier. (c) RX VM voltage doubler. (d) RX RCM rectifier.

Figure 5.1 shows the WPT interfacing circuits used in the analysis. A Class-D power amplifier drives the L_1–C_1 resonant tank at the TX side, as shown in Figure 5.1(a), while the RX can be configured as a full-bridge rectifier (FBR), voltage doubler (VD), or RCM rectifier, as shown in Figure 5.1(b)–(d), respectively. Dotted lines indicate current flows during operation. For the FBR and VD, the blue and red current

paths become conductive to charge the output capacitor(s) in the positive and negative half-periods, respectively, in every resonant period. As discussed in Chapter 2 and Chapter 4, the RCM rectifier typical consists of two phases: resonance phase (Φ_1) and charging phase (Φ_2), where the resonance phase (blue path) can span multiple resonant periods to build up energy in the resonant tank. The number of resonant periods per RCM operation cycle ($\Phi_1 + \Phi_2$) is denoted as N_R. Key circuit parameters used in the analysis are summarized in Table 5.1. C_1 (or C_2) matches L_1 (or L_2) at f_C for proper resonance. L_2 is set smaller with lower quality than L_1, considering coil miniaturization and biocompatible materials' high resistivity. The supply voltage, V_{IN}, is set to 1.8 V. All switches are assumed to have identical ON-resistance, R_{SW}. The switches in the FBR and VD are modeled as ideal diodes, assuming zero forward voltage drops and zero reverse currents.

Table 5.1 Circuit parameters in analysis.

Parameter		Value
Carrier frequency, f_C		6.78 MHz
Excitation supply voltage, V_{IN}		1.8 V
TX Coil	**Inductance, L_1**	1 μH
	Resistance, R_1	1 Ω
TX coil matching capacitance, C_1		551 pF
RX Coil	**Inductance, L_2**	200 nH
	Resistance, R_2	1 Ω
RX coil matching capacitance, C_2		2.76 nF
Switch on-resistance, R_{SW}		0.2 Ω

As the load of the TX, the RX behavior is characterized by its reflected impedance at the TX side, as discussed in Chapter 2. Based on the inductive link analysis, the reflected impedance from a VM RX at the TX side is given by

$$Z_{EQ,VM} = \frac{\omega^4 M^2 {C_2}^2 R_{VM}}{\omega^2 {C_2}^2 R_2 R_{VM} + 1} \tag{5.1}$$

where $\omega = 2\pi f_C$ is the angular carrier frequency, $M = k\sqrt{L_1 L_2}$ denotes the mutual inductance between the coupled L_1 and L_2 (k is the coupling coefficient), and R_{VM} is the equivalent input resistance of the VM RX. The reflected impedance from an RCM RX at the TX side is given by

$$Z_{EQ,RCM} = \begin{cases} \dfrac{\omega^2 M^2}{R_2}, (in\ \Phi_1) \\ \dfrac{\omega^2 M^2}{R_2 + j\omega L_2 + R_{SW}}, (in\ \Phi_2) \end{cases} \tag{5.2}$$

assuming a suffciently large C_O. From (5.1) and (5.2), it can be observed that $Z_{EQ,VM}$ is influenced by R_{VM}, which depends on the output voltage V_{OUT} or the load condition

[5.1], [5.2]. In contrast, $Z_{EQ,RCM}$ is independent of any output-side parameters of the RX, regardless of whether it is in Φ_1 or Φ_2. It is solely determined by the duty ratio between both phases, as discussed in Chapter 4. Therefore, the RCM rectifier exhibits a load-insensitive behavior, leading to distinct performance from its VM counterparts. It is also worth noting that both $Z_{EQ,VM}$ and $Z_{EQ,RCM}$ decrease with increasing WPT distance, due to the corresponding reduction in k.

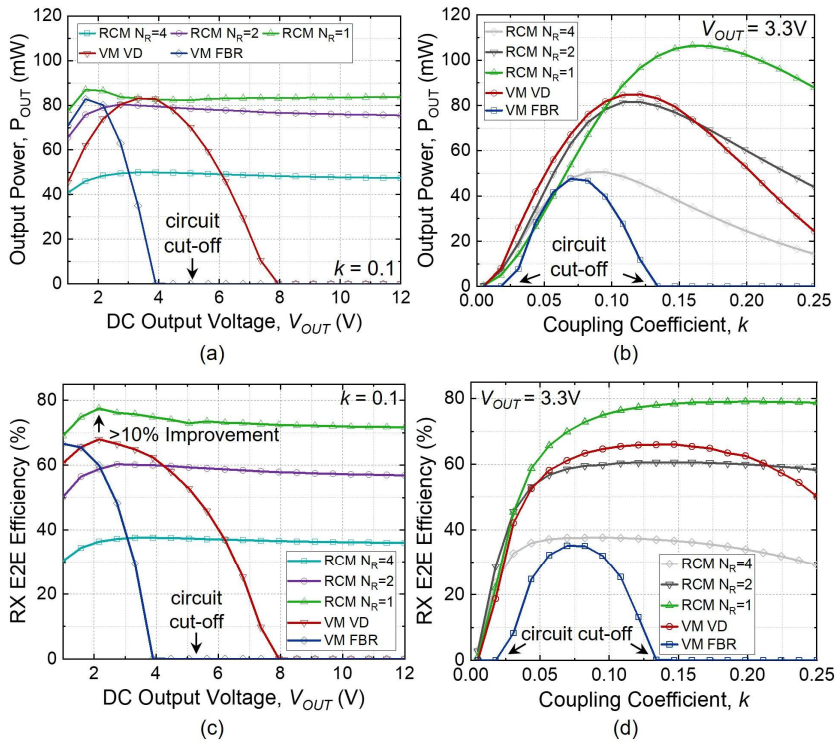


Figure 5.2 Simulated RX output power, P_{OUT}, and RX E2E efficiency. (a) P_{OUT} versus V_{OUT} at k = 0.1. (b) P_{OUT} versus k at V_{OUT} = 3.3 V. (c) Efficiency versus V_{OUT} at k = 0.1. (d) Efficiency versus k at V_{OUT} = 3.3 V.

Figure 5.2 shows the simulated RX output power, P_{OUT}, and RX E2E efficiency versus output voltage, V_{OUT}, and k for different rectifier topologies. The RCM rectifier operates in three cases, N_R = 1, 2, and 4. Figure 5.2(a) presents P_{OUT} versus V_{OUT} from 1 to 12 V, where k is fixed at 0.1. A certain V_{OUT} specifies the load condition of the rectifier while mimicking a regulating rectifier situation. It can be observed that P_{OUT} of FBR and VD reaches a peak value only at a specific V_{OUT}, and they stop conducting when V_{OUT} is too high due to their limited VCR. In contrast, the RCM rectifier maintains relatively constant P_{OUT} across the entire V_{OUT} range, demonstrating a wide operating range and high VCR. Given the strong coupling at k = 0.1, the RCM rectifier with N_R = 1 achieves higher P_{OUT} than the cases with N_R = 2 and N_R = 4.

Figure 5.2(b) presents P_{OUT} versus k varying from 0.005 to 0.25 at V_{OUT} = 3.3 V. The VM rectifiers exhibit a limited high-P_{OUT} coupling range due to their small VCR,

the small RX coil, and the frequency-splitting effect in resonant WPT systems [5.1]. In comparison, the RCM rectifier can dynamically select the optimal N_R, enabling a high-P_{OUT} envelope across varying coupling conditions. For instance, to maximize P_{OUT}, the RCM rectifier operates with $N_R = 2$ when k is in the range of [0:005; 0:09], whereas for $k > 0.09$, it transitions to $N_R = 1$.

Figure 5.2(c) illustrates the RX E2E power efficiency, η_{E2E}, versus V_{OUT} at $k = 0.1$. Distinct from PCE, η_{E2E} is defined as the ratio of P_{OUT} to the RX input power, capturing losses in both the RX coil and the rectifier. It thus reflects the overall power transfer efficiency at the implanted RX side. The VM rectifiers exhibit narrow high-η_{E2E} regions, with η_{E2E} dropping sharply as V_{OUT} increases, mainly due to reduced P_{OUT} and increased RMS current in L_2 charging/discharging C_2 with larger voltage swing. In contrast, the RCM rectifier shows flat η_{E2E} curves, due to per-cycle resonant energy nulling by RCM operation and thus a V_{OUT}-insensitive RMS current level in L_2.

Figure 5.2(d) shows η_{E2E} versus k at $V_{OUT} = 3.3$ V. The RCM rectifier with $N_R = 2$ and the VD exhibit similar η_{E2E} performance, while the RCM rectifier with $N_R = 1$ demonstrates a noticeably higher η_{E2E} curve, especially under strong coupling. This is primarily attributed to the lower RMS current in L_2 and the higher P_{OUT}.

The simulation results show that the VM rectifiers can deliver superior performance under specific loading conditions with robust monophasic operation. However, they operate with relatively limited VCRs and narrow optimal operating ranges. In contrast, the RCM rectifier significantly extends the operable VCR range while maintaining comparable performance, benefiting from its load-insensitive behavior [see Figure 5.2(a) and (c)].

On the other hand, the RCM rectifier better adapts to coupling variations by adjusting N_R. Though the RCM rectifier was initially recognized for its energy harvesting capability under extremely weak coupling, it is now shown to be able to outperform VM rectifiers in both power and efficiency under strong coupling conditions [see Figure 5.2(b) and (d)]. Hence, the RCM rectifier presents a compelling choice for biomedical WPT applications and is especially well-suited for miniature implants that require HV functionality and operate under wireless link fluctuations.

5.1.3 Proposed Topology

Conventional RCM rectifiers can be categorized into two types: parallel-LC [5.3][5.4] and series-LC [5.5][5.6][5.7][5.8][5.9][5.10][5.11], as shown in Figure 5.3 and Figure 5.4, respectively. Both have the two typical phases: resonance phase (Φ_1) and charging phase (Φ_2). In Φ_1, the power switch M_N is turned on and M_P is off, allowing the L_2–C_2 tank to resonate freely. In Φ_2, M_P is turned on and M_N is off, enabling the output capacitor C_O to be charged by the RX coil current I_2.

The two topologies are distinguished by the placement of the resonant capacitor C_2. The parallel-LC topology connects C_2 in series with M_N, which is capable of

interrupting the L_2–C_2 resonant loop but exposing the high-swing node V_{AC} to M_P. Hence, the resonant charge accumulated in Φ_1 can be completely delivered to C_O if Φ_2 begins when I_2 reaches its peak. However, in Φ_1, M_P must withstand a high drain-to-source voltage (V_{DS}) of $|V_{AC}| + V_{OUT}$, which may necessitate an HV-rated device or a stack of multiple low-voltage (LV) devices.

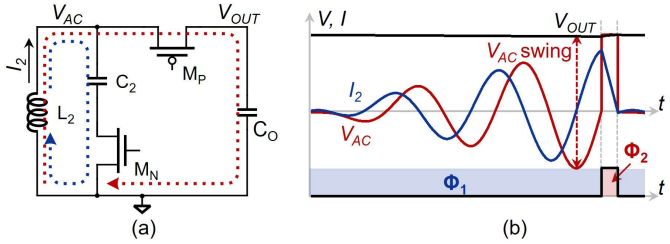


Figure 5.3 (a) Topology and (b) operation waveform of parallel-LC RCM rectifier.

In the series-LC topology, C_2 is connected in series with L_2, which constrains the voltage swing across both M_P and M_N to V_{OUT}. Nonetheless, since C_2 remains in the circuit in Φ_2, residual energy may persist if Φ_2 begins at the peak of I_2. To avoid the additional conduction losses caused by the residual energy, the designs [5.6][5.8][5.11] initiate Φ_2 earlier (before the I_2 peak), allowing C_2 to act as a voltage source that charges C_O via L_2. With precise timing, this method enables both $I_2 = 0$ and $V_C = 0$ at the end of Φ_2. However, it requires sophisticated feedback control with slow convergence to recognize the imperceptible switching instant, limiting its practicality, especially under fluctuating wireless link conditions.

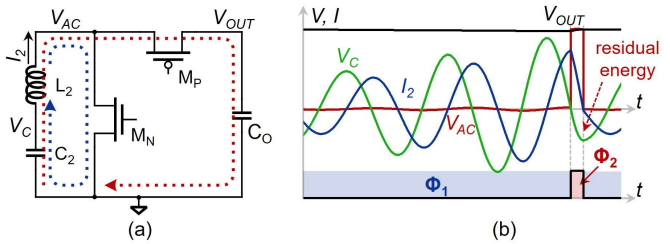


Figure 5.4 (a) Topology and (b) operation waveform of series-LC RCM rectifier.

The parallel-LC and series-LC RCM topologies present complementary trade-offs in rectifier operation; however, to regulate V_{OUT}, both must rely either on a separate DC–DC stage or on adjusting the duty ratio between Φ_1 and Φ_2 [5.7][5.10], as they consist of only two operational phases. Under light-load conditions, the duration of Φ_1 is prolonged in the duty-control method, resulting in a significantly large I_2, which in turn causes excessive conduction losses in both the RX coil and the rectifier circuit.

5.1.3.1 Proposed RCM Rectifier

Figure 5.5(a) shows the proposed RCM rectifier topology. C_2 is connected in series with L_2, while a power switch M_{N2} is connected in parallel with C_2. The proposed rectifier consists of three operational phases: the resonance phase (Φ_1), the charging phase (Φ_2), and the freewheeling phase (Φ_3), as shown in Figure 5.5(b)–(d), respectively. In Φ_1, only M_{N1} is turned on, enabling freely resonating L_2–C_2 tank. In Φ_2, both M_P and M_{N2} are turned on, and M_{N1} is off; L_2 charges C_O as a current source and C_2 is disconnected. In Φ_3, both M_{N1} and M_{N2} are turned on, and M_P is off; the L_2–C_2 resonance is interrupted.

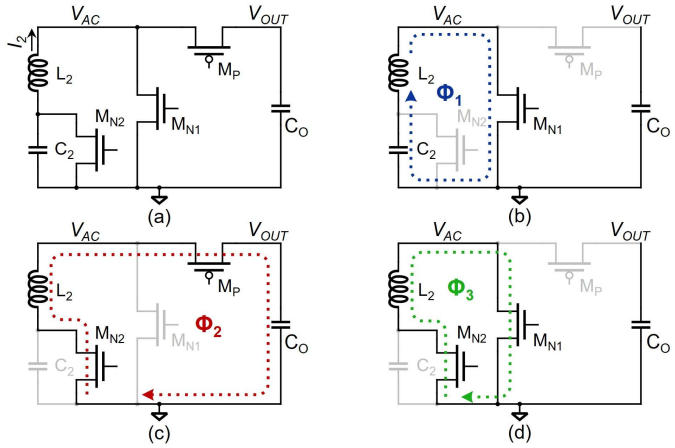


Figure 5.5 (a) Topology and (b)–(d) operation phases of the proposed three-phase regulating RCM rectifier. (b) Resonance phase, Φ_1. (c) Charging phase, Φ_2. (d) Freewheeling phase, Φ_3.

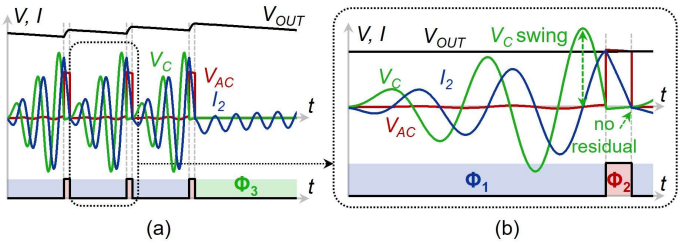


Figure 5.6 (a) Three-phase regulating rectifier operation and (b) zoomed-in RCM operation (Φ_1 and Φ_2) of the proposed three-phase regulating RCM rectifier.

Leveraging the three phases, the proposed rectifier achieves power-efficient output regulation, residual-free charge delivery, and releases voltage stress on each power switch. Figure 5.6 shows its operation waveform. First, unlike Φ_1, Φ_3 disables the L_2–C_2 resonance, significantly lowering the link efficiency from TX to RX [5.1]. When C_O holds sufficient energy, the rectifier can lower the RX input power by entering Φ_3 [as reflected by the reduced I_2 in Φ_3 in Figure 5.6(a)], thus maintaining high PCE. Second, Φ_2 involves a bypass-capacitor-based operation through the activation of M_{N2}. Since the large M_{N2}, operating in the deep-triode region, presents low ON-resistance, the energy

remaining in C_2 becomes negligible by the end of Φ_2 that begins at the I_2 peak [see Fig. 5.6(b)]. Last, Φ_1 in the proposed topology is similar to that of the series-LC topology, which limits the voltage swing across both M_P and M_{N1} to V_{OUT}. Meanwhile, M_{N2} only experiences the voltage across C_2, V_C, independent of V_{OUT}.

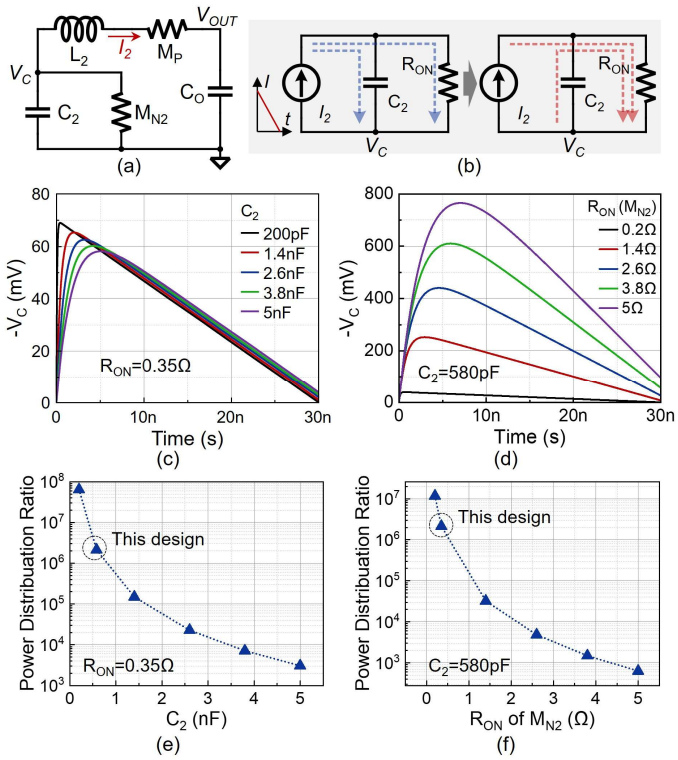


Figure 5.7 Bypass-capacitor operation analysis. (a) Circuit and (b) equivalent model in charging phases (Φ_2). Simulated transient waveform of V_C under (c) various C_2 and (d) various R_{ON} of M_{N2}. Simulated power distribution ratio under (e) various C_2 and (f) various R_{ON} of M_{N2}.

It is essential to validate the efficacy of the proposed bypass-capacitor operation under varying values of C_2 and the ON-resistance (R_{ON}) of M_{N2}. Figure 5.7(a) recalls the circuit configuration in Φ_2. In this phase, L_2 first charges C_2, building up V_C from zero, which then conducts the M_{N2} branch to share I_2. As energy in L_2 gradually depletes at a fixed V_{OUT}, I_2 becomes insufficient to sustain both the C_2 and M_{N2} branches, causing C_2 to discharge. This amount of energy from C_2 is eventually redistributed among M_{N2}, M_P, and C_O. Figure 5.7(b) presents the equivalent model by replacing L_2 with a current source exhibiting a linear deenergizing profile (I_2 = 200 mA at t = 0; I_2 = 0 mA at t = 30 ns), while neglecting the remaining components in the L_2 branch. In this design, M_{N2} is implemented as a 6-mm 5-V NMOS device with R_{ON} of 0.35 Ω under a 3.3-V bias, and C_2 is 580 pF as used in measurement. Simulated transient waveforms of V_C applying various C_2 and R_{ON} values are shown in Figure 5.7(c) and (d), confirming the expected hump-shaped profiles. Figure 5.7(e) and (f) plot the power distribution ratio (PDR), defined as P_{RON}/P_{C2}, across a wide range of C_2 and

R_{ON} values. In all cases, the M_{N2} branch handles the majority of power from L_2; the PDR is 633 in the worst case (R_{ON} = 5 Ω and C_2 = 580 pF), while in this design (R_{ON} = 0.35 Ω and C_2 = 580 pF) it exceeds 2 × 10^6. These results confirm that the proposed bypass-capacitor operation effectively eliminates the residual energy after charging phases.

Notably, this experiment considers only the charging phase while assuming normal operation during the resonance phase. If a different value of C_2 is used, L_2 can be adjusted accordingly to maintain a resonant frequency of 6.78 MHz. However, in the present analysis, the value of L_2 is not critical, as it does not affect the power distribution between C_2 and R_{ON}.

5.1.3.2 RCM Topology Comparison

To validate the effectiveness of the proposed three-phase RCM rectifier, it is necessary to benchmark its performance against existing RCM topologies. The analysis reuses the specifications listed in Table 5.1, with results shown in Figure 5.8. V_{OUT} is fixed at 3.3 V, and N_R is set to 2. The analysis omits output regulation (which will be detailed shortly) by applying constant-voltage loads, allowing a focused evaluation of conducting operations. Therefore, the proposed rectifier always operates in Φ_1 and Φ_2.

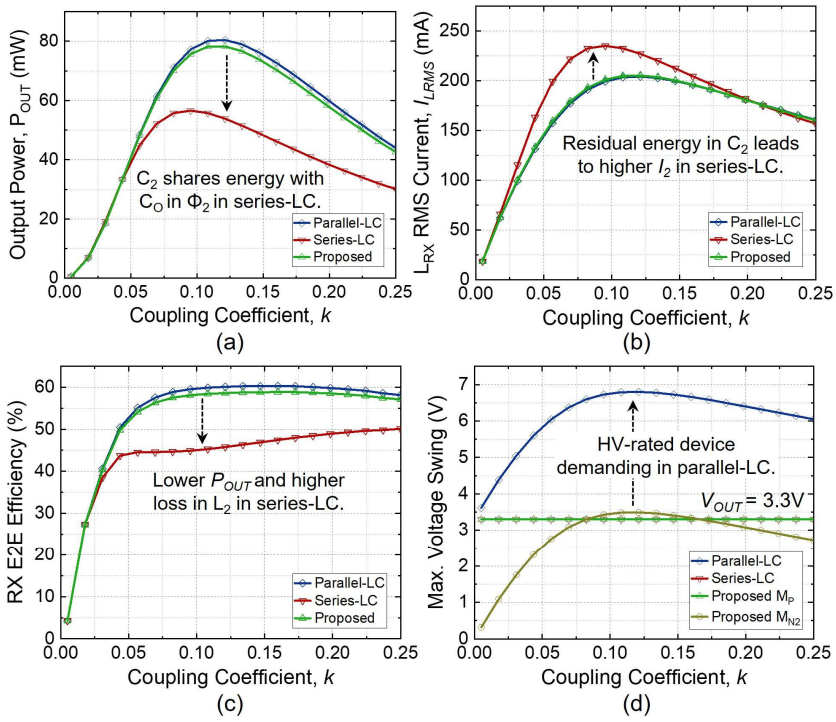


Figure 5.8 Simulated performance of the parallel-LC, series-LC, and proposed RCM rectifiers versus k with N_R = 2 and V_{OUT} = 3.3 V. (a) P_{OUT}. (b) RMS current in L_2. (c) η_{E2E}. (d) Maximum voltage swing.

Figure 5.8(a) shows the simulated RX output power, P_{OUT}. The series-LC RCM rectifier [typical implementation with residual energy after charging (see Figure 5.4)] delivers lower P_{OUT} because C_2 shares the charging energy with C_O in Φ_2. This residual energy in C_2 also leads to higher I_2, as shown in Figure 5.8(b). Under stronger coupling, the RMS I_2 for all three topologies tends to converge, because the parallel-LC and the proposed rectifiers present higher RX input power due to their reflected impedance being closer to the TX-side maximum power point [5.1][5.12]. The combination of lower P_{OUT} and higher I_2 in the series-LC topology results in a notable drop in RX E2E efficiency, η_{E2E}, as shown in Figure 5.8(c). Though the parallel-LC topology demonstrates higher P_{OUT} and η_{E2E}, these values are based on an idealized scenario where a single switch (M_P) must withstand nearly 7-V V_{DS} [see Figure 5.8(d)]. When accounting for the increased ON-resistance of an HV-rated device or stacked LV devices, the proposed rectifier and the parallel-LC rectifier should exhibit similar conducting performance. However, the proposed rectifier offers the added advantage of a low-power freewheeling phase. Furthermore, the use of an NMOS device provides inherently less power loss compared with PMOS, and the stand-alone M_{N2} eliminates the need for complex gate-driving circuitry typically required for stacked device configurations.

On the other hand, compared qualitatively to the residual-free series-LC RCM rectifier reported in [5.8], the proposed rectifier realizes inherent residual-free charging with simplified and robust control, despite requiring two switches to conduct during the charging phase. While the design in [5.8] is well-suited for open-loop rectifier designs, the proposed rectifier provides enhanced utility and reliability for batteryless implants under variable coupling conditions, particularly when in situ output regulation is required.

5.1.3.3 In-Situ Output Regulation and Inherent LSK

The series-LC and the proposed rectifiers are compared with hysteresis-based output regulation, as shown in Figure 5.9. The parallel-LC rectifier is excluded because a long-term Φ_1 easily induces an over-breakdown V_{AC} swing across M_P. When the rectifier is "off", the series-LC rectifier switches to Φ_1 [see Figure 5.9(a)], as implemented in prior work [5.7] and [5.10], while the proposed rectifier transitions to Φ_3 [see Figure 5.9(b)]. A noticeable I_2 decrease is observed in the proposed waveform, leading to significant PCE enhancements, especially under light-load conditions [see Fig. 5.9(c)]. In addition, the proposed Φ_3 inherently introduces a downward transient in the RX-reflected impedance at the TX by interrupting the L_2–C_2 resonance [5.13], [5.14]. This results in an increase in the amplitude of the TX loop current, I_1, as shown in Figure 5.9(b), when a typical VM TX is used. By demodulating the resulting upward transient in I_1 amplitude, 1-bit uplink data transfer can be enabled, facilitating simultaneous power and data transfer. Importantly, the amplitude modulation (AM) effect on I_1 using the proposed three-phase operation is dependent on the coupling condition (k), as shown in Figure 5.10. The simulation reuses the specifications listed in

Table 5.1. The resulting modulation index (MI) increases with stronger coupling, i.e., larger k. It is also worth noting that the increased I_1 amplitude in Φ_3 implies higher TX power consumption, potentially reducing the E2E efficiency from TX to RX. However, the proposed operation ensures a low thermal burden on the implant side, which is typically more critical, and enhances compatibility with single-TX multi-RX configurations (e.g., for neural interface applications) by avoiding unnecessary energy draw from the TX. Moreover, the E2E efficiency can be further improved with closed-loop TX power modulation techniques.

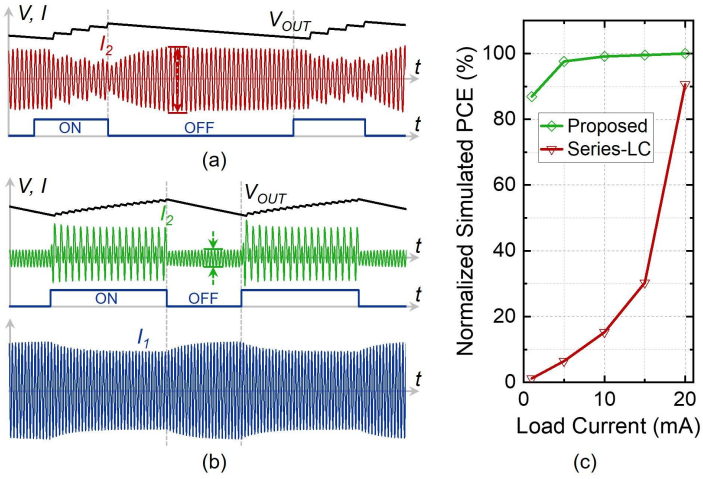


Figure 5.9 Hysteresis-based output regulation waveform of (a) series-LC rectifier and (b) proposed rectifier. (c) Normalized simulated PCE of both rectifiers with regulation.

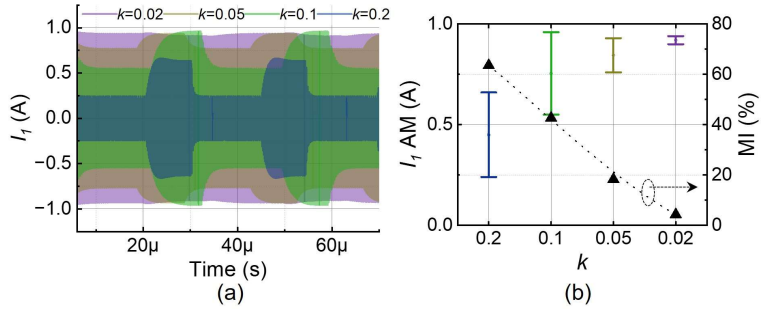


Figure 5.10 (a) Simulated waveform and (b) amplitude modulation index of I_1 with the proposed three-phase operation at various k.

Remarkably, VM regulating rectifiers often adopt similar freewheeling phases for output regulation [5.15][5.16]. While such a freewheeling operation effectively reduces link efficiency to conserve RX input power, it does not fully interrupt power transfer. The resulting power leakage can continue to degrade the PCE, especially under light-load conditions, as reflected in Figure 5.9(c).

5.1.4 Circuit Implementations

Figure 5.11 shows the system architecture. The proposed rectifier power stage comprises three power transistors, M_P, M_{N1}, and M_{N2}. M_{N2} is driven by an adaptive-biasing gate driver D_3, which will be detailed later. The regulation controller maintains the DC output voltage, V_{OUT}, within a hysteresis window defined by two programmable reference voltages, V_{RH} and V_{RL}, which can be set according to application requirements. When V_{OUT} drops below V_{RL}, the rectifier is activated and alternates between Φ_1 and Φ_2 to charge V_{OUT} (on-duty). As V_{OUT} surpasses V_{RH}, it transitions to Φ_3, idling the power stage and lowering the RX input power (off-duty).

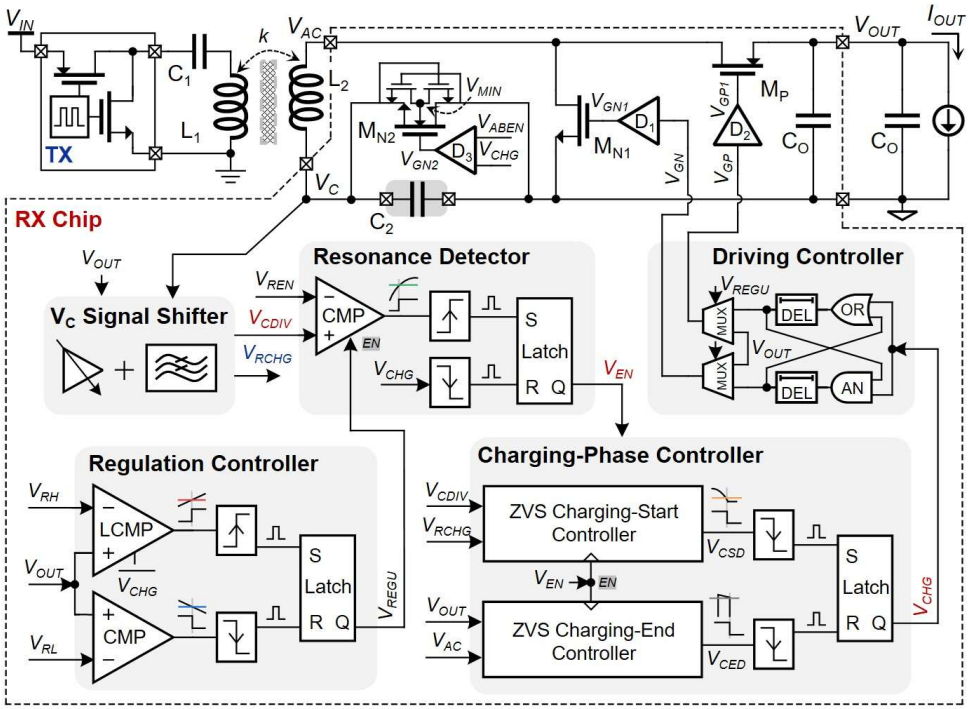


Figure 5.11 System architecture of the proposed three-phase regulating RCM rectifier.

During the on-duty, the output of the regulation controller, V_{REGU}, is logic-high, enabling the resonance detector to compare a divided and level-shifted version of V_C (V_{CDIV}), generated by the V_C signal shifter, against a reference voltage, V_{REN}. This comparison monitors the accumulated resonant energy level in the L_2–C_2 tank in Φ_1, as shown in Figure 5.12. Once the resonant energy reaches the threshold defined by V_{REN}, the charging-phase enable signal, V_{EN}, transitions high to activate the charging-phase controller. The resonance detector also protects M_{N2} from overvoltage stress during operation. The ZVS charging-start controller and the ZVS charging-end controller determine the initiation and termination of the charging phase, respectively. To achieve ZVS at both edges, digital-assisted delay-compensation tuning loops are employed in both controllers, which will be described later. The output of the charging-phase

controller, V_{CHG}, determines the power-stage gate-drive signals V_{GP} and V_{GN}, via the driving controller that also inserts appropriate deadtime between switching events. During the off-duty, the power stage remains idle with no switching activity, and all control circuits, except for the regulation controller, are disabled to conserve power.

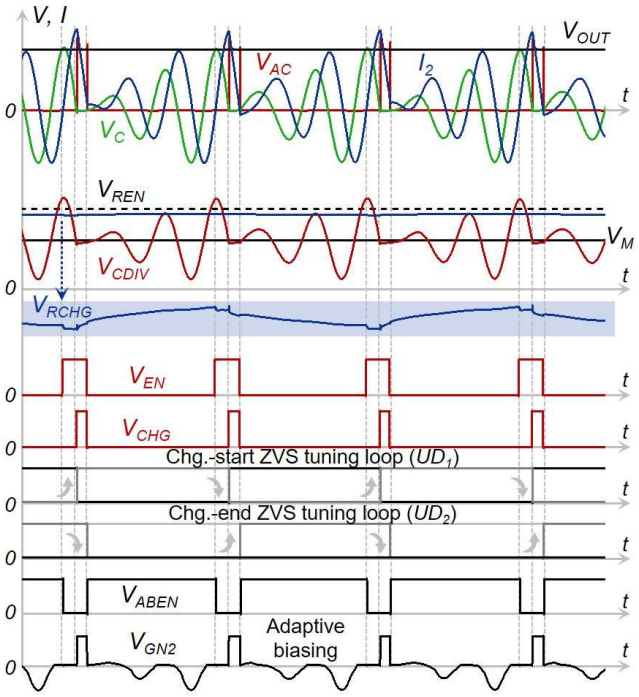


Figure 5.12 Operation waveform of the proposed three-phase regulating RCM rectifier.

Figure 5.13 shows the circuit implementation and simulated operation waveform of the V_C signal shifter. As the midpoint of the L_2–C_2 tank, V_C can exceed V_{OUT}, the system supply voltage, or drop significantly below ground. To prevent this high voltage from control blocks, the V_C signal shifter generates a scaled version, V_{CDIV}, by dividing V_C by 3× using a capacitive divider. The DC component of V_{CDIV} is defined as V_M, set to half of V_{OUT} via a resistive divider. High-frequency isolation between V_{CDIV} and V_M is provided by a low-pass filter formed by R_{LP} and the capacitive divider. To better adapt to various N_R cases, R_{LP} can be replaced with an active switch that performs time-domain disconnection, controlled by V_{CHG}. This can ensure V_{CDIV} equals V_M at the end of Φ_2, when V_C is nearly indistinguishable from ground. In addition, the V_{OUT} divider includes a resistor ladder that generates a tunable reference voltage, V_{RCHG}, for use in the ZVS charging-start controller.

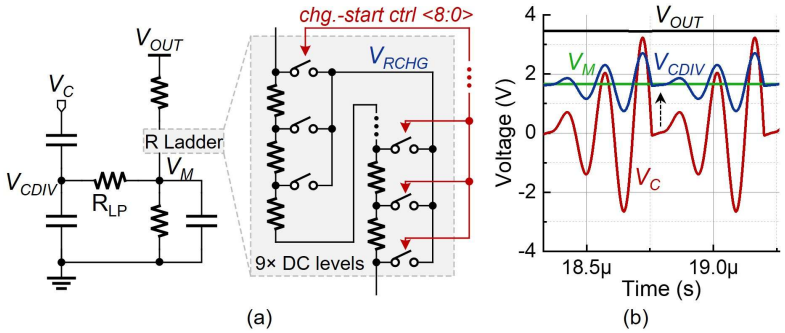


Figure 5.13 (a) Circuit implementation and (b) operation waveform of the V_C signal shifter.

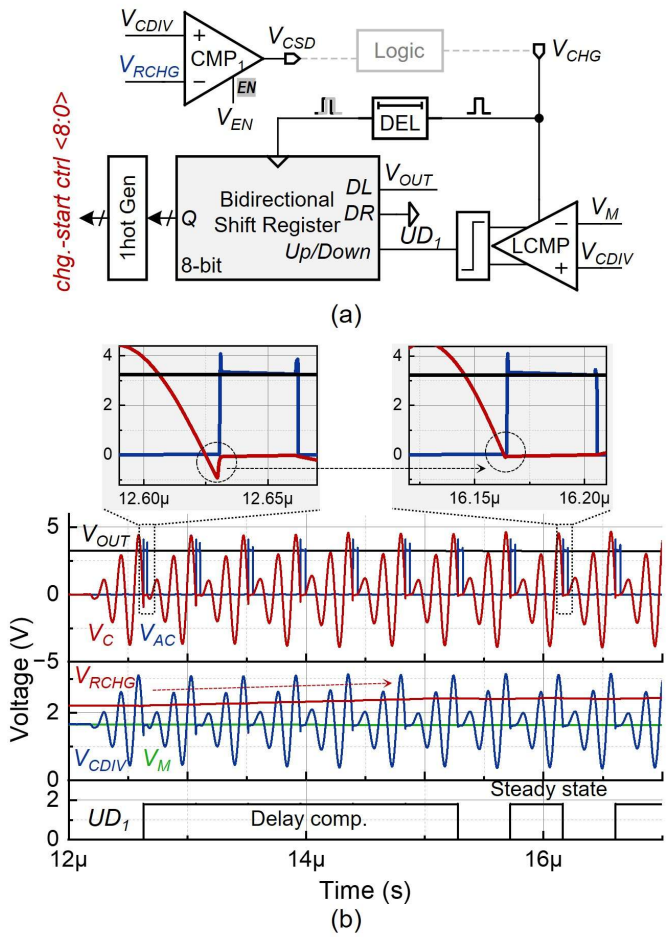


Figure 5.14 (a) Circuit implementation and (b) operation waveform of the ZVS charging-start controller.

Figure 5.14 shows the circuit implementation and simulated operation waveform of the ZVS charging-start controller, which detects the I_2 peak to trigger the transition from Φ_1 to Φ_2. At this moment, V_{CDIV} should equal V_M, indicating that V_C is tied to

ground, allowing M_{N2} to turn on with negligible V_{DS}, thereby achieving ZVS [see Figure 5.14(b)]. Ideally, this transition could be determined by a comparator (CMP_1); however, the propagation delay in the control loop, including the comparator, logic gates, and the gate driver, can introduce significant switching errors in the 6.78-MHz power stage. To address this, a digital-assisted ZVS technique is proposed. It comprises a fast latched clocked comparator (LCMP), an 8-bit bidirectional shift register (Bi-SR) with a one-hot generator, and the V_{RCHG} generator integrated within the V_C signal shifter. The LCMP senses the control delay by comparing V_{CDIV} and V_M at the rising edge of V_{CHG}. Designed with a typical response time under 1 ns, the LCMP can counterbalance the slight lead of the V_{CHG} edge relative to the actual gate-driving signal of M_{N2}, V_{GN2}, allowing removal of a separate sampling circuit for V_{CDIV}. The LCMP output determines the shift direction of the Bi-SR (UD_1), which then adjusts the V_{RCHG} level accordingly. By using the calibrated V_{RCHG} instead of V_M as the reference input to CMP_1, the charging phase Φ_2 can be precisely initiated at the I_2 peak.

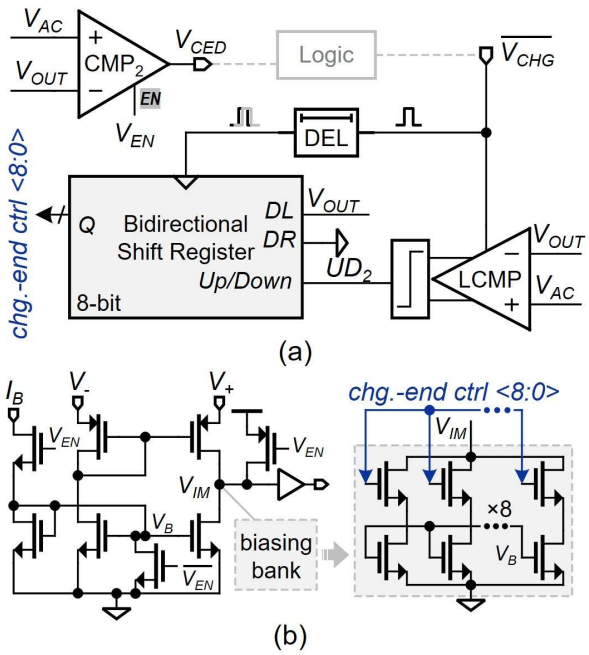


Figure 5.15 Circuit implementation of (a) ZVS charging-end controller and (b) CMP_2.

Figure 5.15 shows the circuit implementation of the ZVS charging-end controller. Its goal is to achieve zero-voltage turn-off of M_P, ensuring complete charge delivery to C_O while preventing reverse current flow. The comparator CMP_2 monitors V_{AC} relative to V_{OUT}, and a similar digital-assisted ZVS tuning loop is employed to compensate for control delay. This is accomplished by adjusting the current bias of CMP_2 through an 8-bit biasing bank, as illustrated in Figure 5.15(b). Noting that both ZVS controllers use uniform-step tuning, while binary-weighted tuning is also feasible to extend the tuning range or achieve finer resolution, albeit at the cost of slower convergence.

Figure 5.16(a) shows the deadtime control between M_{N1} and M_P gate driving signals to prevent a direct short from V_{OUT} to ground. This concern does not apply to M_{N2}, as it resides in the L_2 branch without abrupt current transients. During Φ_1 to Φ_2 transition, V_{GN1} and V_{GN2} switch first, derived from V_{CHG}, while V_{AC} rises due to the disconnection of M_{N1}. After a deadtime, V_{GP1} switches. This deadtime can align with the V_{AC} rising time to further realize zero-voltage turn-on of M_P. During Φ_2 to Φ_1 transition, M_P is turned off first, followed by the switching of V_{GN1} and V_{GN2} after a deadtime.

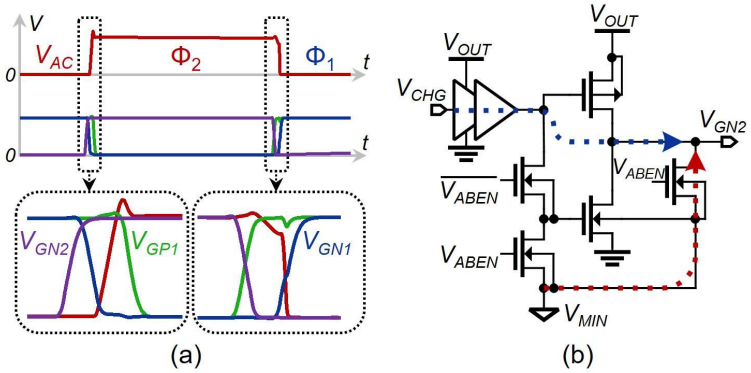


Figure 5.16 (a) Switching deadtime waveform. (b) Circuit implementation of gate driver D_3.

Figure 5.16(b) shows the implementation of the adaptive-biasing gate driver D_3. As described in Figure 5.12 and Figure 5.13, V_C can fall significantly below ground in Φ_1, during which D_3 pulls V_{GN2} down to V_{MIN}, which is defined as the lower of V_C and ground, to maintain M_{N2} is off. V_{MIN} is generated by an NMOS-based cross connector, as shown in Figure 5.11. In Φ_2, D_3 fast drives M_{N2} as a normal driver. Its mode transition is governed by V_{ABEN}, which is synchronized with V_{EN}.

5.1.5 Measurement Results

The proposed three-phase RCM regulating rectifier has been fabricated in a 180-nm CMOS process, occupying a silicon area of 0.4 mm^2 including optional on-chip output capacitors, as shown in Figure 5.17. The power switches M_P, M_{N1}, and M_{N2} are implemented using 5-V devices. Figure 5.18 shows the measurement setup. C_O is implemented off-chip with capacitance of 4.7 µF. The TX is realized by a waveform generator generating a 6.78-MHz square wave with an amplitude of $V_{IN}/2$. It drives a series-resonant L_1–C_1 tank. The TX and RX coils, L_1 and L_2, have inductances of 951 and 950 nH, respectively, with identical diameters of 27 mm. Matching capacitors C_1 and C_2 are used to tune L_1 and L_2 to resonance at 6.78 MHz. Notably, the chosen L_1 and L_2 values do not impact the effectiveness of the proposed rectifier; smaller RX coils can be readily adopted when required. The coaxial separation distance between L_1 and L_2, D_{COIL}, is adjustable, mimicking coupling variations in practice.

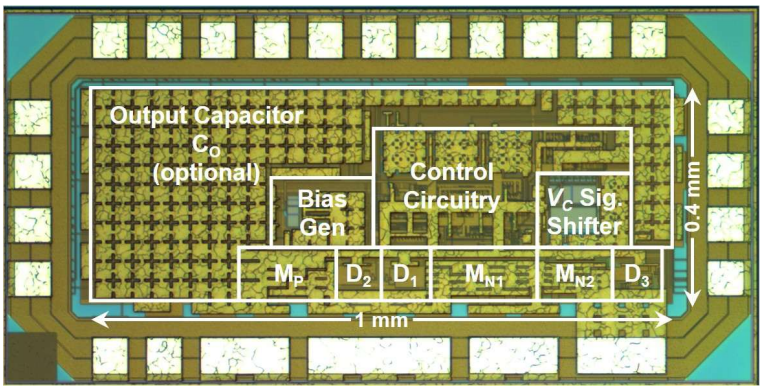


Figure 5.17 Chip micrograph.

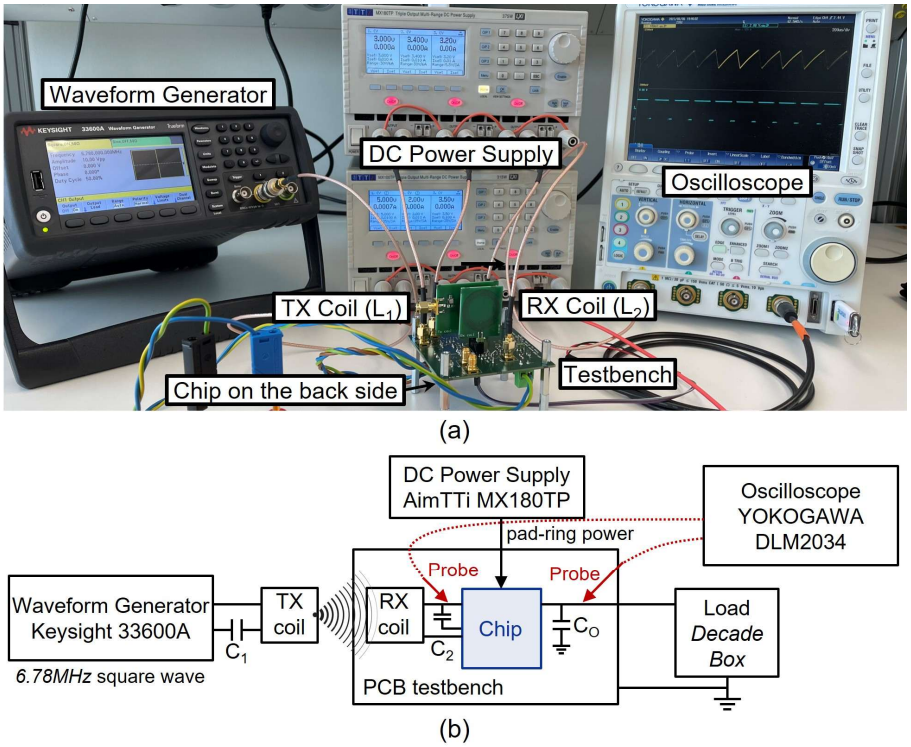


Figure 5.18 (a) Photograph and (b) schematic of measurement setup.

Figure 5.19 shows the measured steady-state waveform of the rectifier when it regulates the DC output voltage, V_{OUT}, at 3.3 V. Under the heavy-load condition in Figure 5.19(a), V_{OUT} is regulated within a 60-mV hysteresis window. The ON/OFF duty ratio of the rectifier, indicated by V_{REGU}, is large, while it becomes small under the light-load condition [see Figure 5.19(b)]. During the off-duty, V_C presents nearly unnoticeable amplitude because of the low-power freewheeling phase.

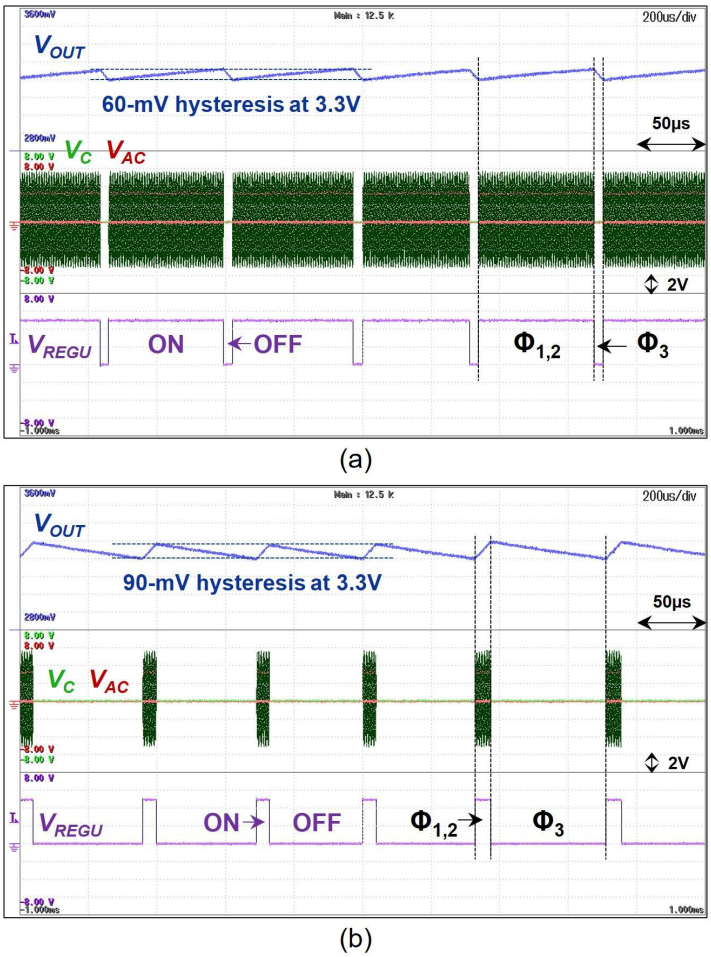


Figure 5.19 Measured steady-state waveform with three-phase regulation (a) under heavy-load conditions and (b) under light-load conditions.

Figure 5.20 presents the measured zoomed-in steady-state waveform of the rectifier. At low RX input power, it operates with longer resonance phases, as shown in Figure 5.20(a), where N_R = 4. As the RX input power increases, due to tighter coupling or higher TX power, it dynamically adjusts to operate with N_R = 3, 2, and 1, as shown in Figure 5.20(b)–(d). Due to the inherent residual-free operation and the digital-assisted ZVS tuning, the rectifier exhibits smooth switching behaviors between phases, with no observable energy remaining in the L_2–C_2 tank after Φ_2 (the charging phase). Figure 5.21 shows the measured I_2 waveform at N_R = 4 when V_{OUT} is 3.3, 2.2, and 4.4 V, respectively. At 3.3 V, the charging phases are observed to end with near-zero I_2, clearly validating the residual-free operation. The limit-cycle oscillation observed at 2.2 V, as well as the slight residual energy after charging phases at 4.4 V, can be further mitigated by enhancing the resolution and tuning range of the ZVS control loops. Notably, these implementation non-idealities do not compromise the load-insensitive nature of the proposed RCM rectifier.

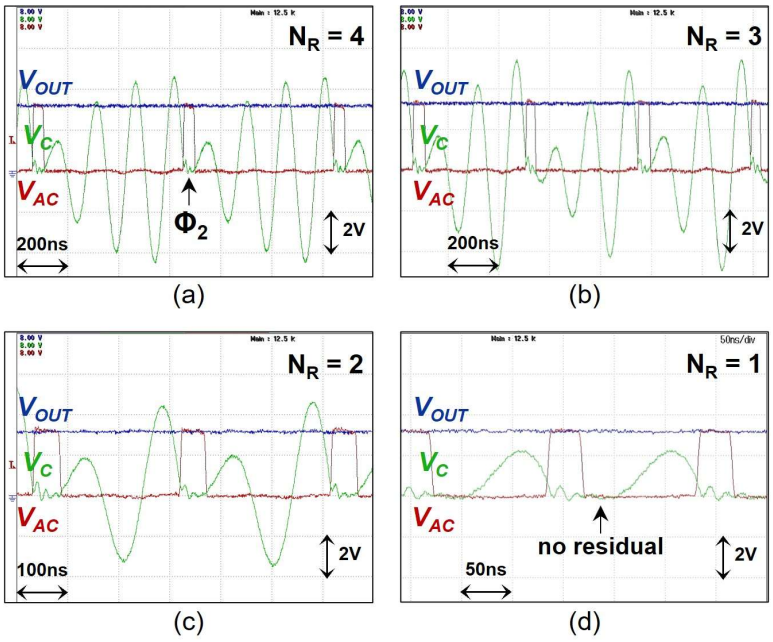


Figure 5.20 Measured zoomed-in steady-state waveform under different N_R conditions. (a) N_R = 4. (b) N_R = 3. (c) N_R = 2. (d) N_R = 1.

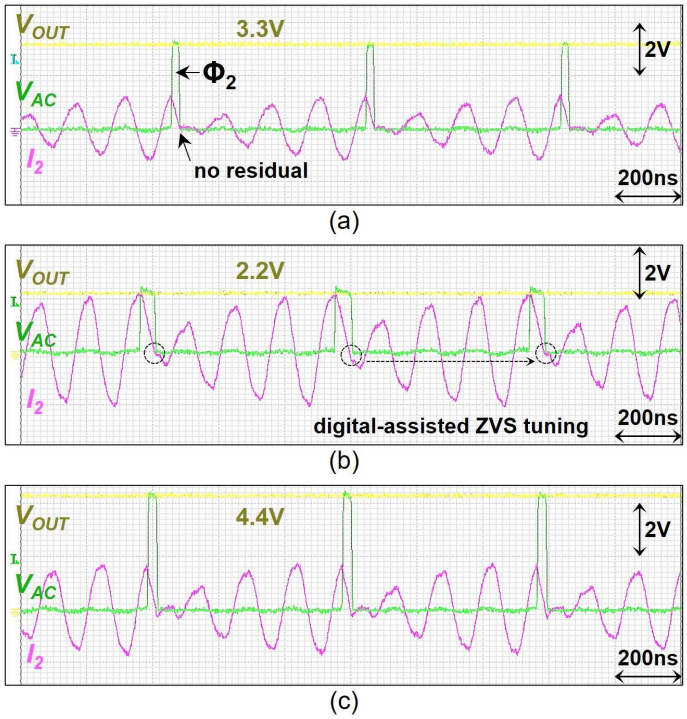


Figure 5.21 Measured steady-state waveform of I_2 at N_R = 4 under different V_{OUT} conditions. (a) V_{OUT} = 3.3 V. (b) V_{OUT} = 2.2 V. (c) V_{OUT} = 4.4 V.

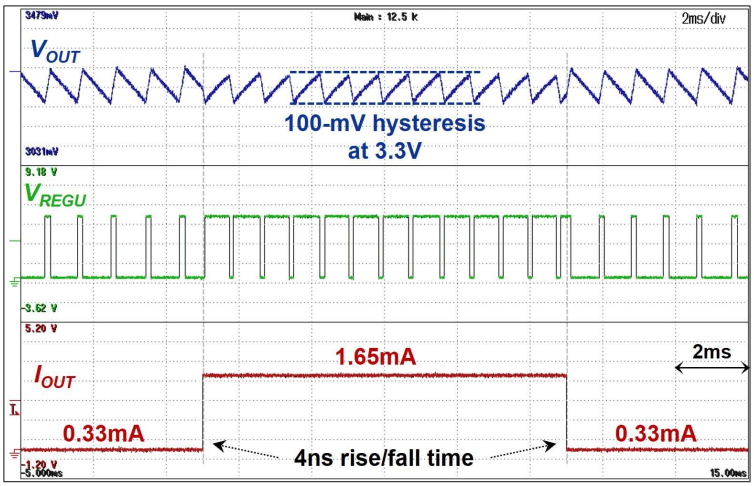


Figure 5.22 Measured load-transient waveform at D_{COIL} = 1 cm and V_{IN} = 1.8 V.

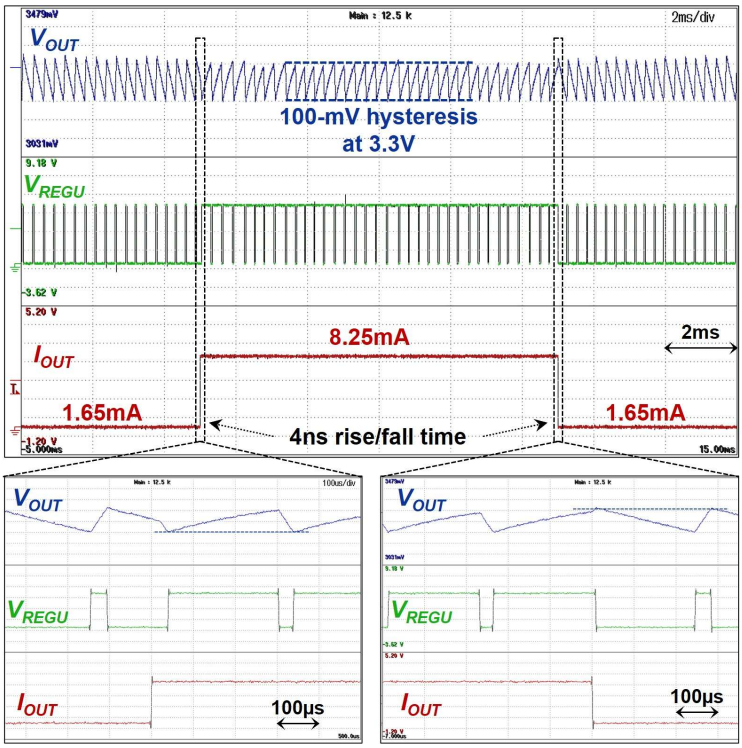


Figure 5.23 Measured load-transient waveform at D_{COIL} = 0.5 cm and V_{IN} = 3.9 V.

Figure 5.22 shows the measured load-transient waveform at D_{COIL} = 1 cm and V_{IN} = 1.8 V. During the load transients, the rectifier load current, I_{OUT}, steps between 0.33 and 1.65 mA (5× load change) with a rise/fall time of approximately 4 ns. Though the rectifier's ON/OFF duty ratio shifts significantly during these transitions, it consistently regulates V_{OUT} within the hysteresis window at 3.3 V. Figure 5.23 shows the measured load-transient waveform at D_{COIL} = 0.5 cm and V_{IN} = 3.9 V, where I_{OUT} transitions

between 1.65 and 8.25 mA (5× load steps). The results confirm that higher input power and heavier load conditions do not compromise the rectifier's ability to maintain proper V_{OUT} regulation.

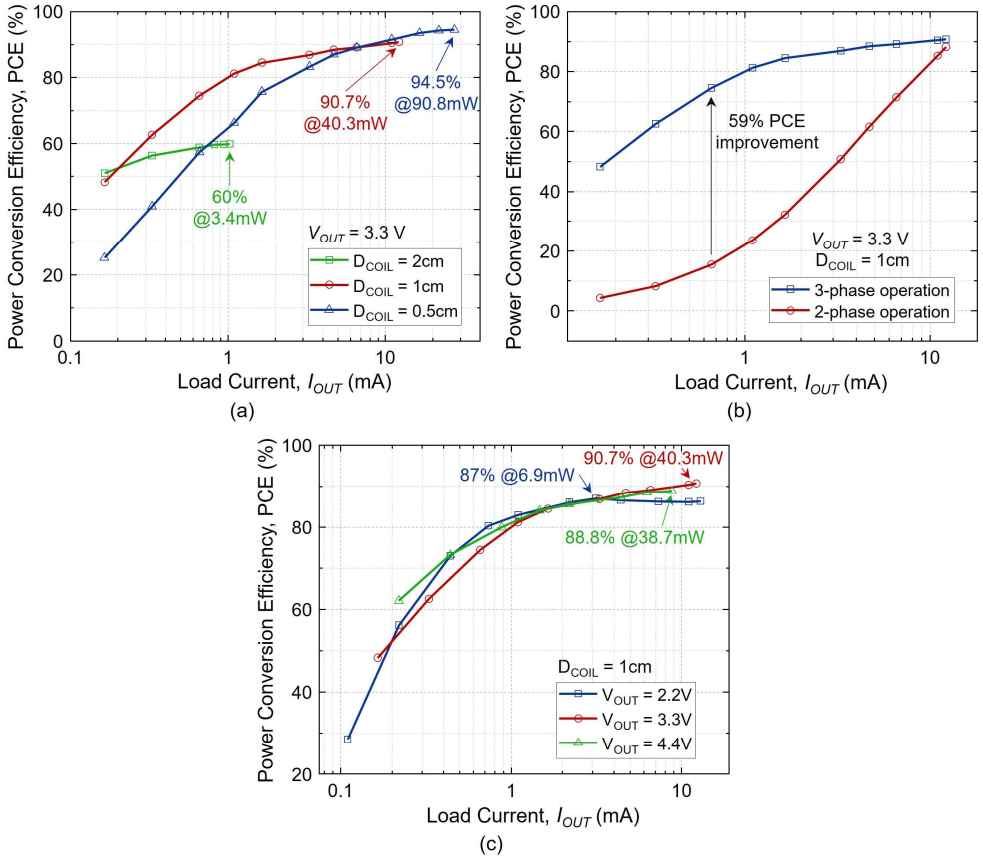


Figure 5.24 Measured PCE at V_{IN} = 10 V (a) under different D_{COIL} conditions at V_{OUT} = 3.3 V, (b) with different phase operations at V_{OUT} = 3.3 V and D_{COIL} = 1 cm, and (c) under different V_{OUT} conditions at D_{COIL} = 1 cm.

Figure 5.24 shows the measured PCE of the rectifier, defined as

$$PCE = \frac{\overline{V_{OUT} \cdot I_{OUT}}}{\frac{1}{T}\int_{t_0}^{t_0+T} V_{AC}(t) \cdot I_2(t)dt} \times 100\% \tag{5.3}$$

where T spans three complete hysteresis regulation cycles, ensuring that V_{OUT} remains constant and P_{OUT} accurately equals $V_{OUT} \cdot I_{OUT}$. The L_2 current, I_2, is measured using shunt-based sensing. A 5.1-Ω resistor (R_{SNS}) is placed in series with L_2 near V_C, and a 2-GHz bandwidth differential probe (PBD2000) monitors the voltage across it via a four-wire Kelvin connection.

Figure 5.24(a) shows the PCE under various D_{COIL} at V_{OUT} = 3.3 V. When D_{COIL} = 2 cm, the peak PCE reaches 60% at P_{OUT} = 3.4 mW, limited by the low-power level and

long resonance phase. As D_{COIL} decreases, both the achievable P_{OUT} and peak PCE improve. Though PCE decreases under light-load conditions due to unavoidable power loss in the freewheeling phase, the peak PCE reaches 90.7% and 94.5% for D_{COIL} = 1 and 0.5 cm, respectively, corresponding to P_{OUT} of 40.3 and 90.8 mW.

Figure 5.24(b) compares the PCE under three-phase and two-phase operation modes. In the two-phase operation, Φ_1 is activated during the rectifier's off-duty instead of Φ_3, mimicking the approach in [5.7] and [5.10] as described in Section 5.1.2. The proposed three-phase operation yields a higher PCE curve, achieving up to 59% improvement, attributed to the inclusion of the low-power freewheeling phase (Φ_3).

Figure 5.24(c) shows the PCE under various V_{OUT} levels at D_{COIL} = 1 cm. This prototype is optimized for V_{OUT} = 3.3 V, in terms of switching deadtime, transistor sizing, etc., so the cases with V_{OUT} = 2.2 and 4.4 V present slightly lower peak PCE and shifted peak-PCE points. Nonetheless, all PCE curves remain at a comparable level, confirming the RCM rectifier's load-insensitive behavior. Overall, the proposed rectifier maintains a broad high-PCE region, exceeding 80% or 85% starting from I_{OUT} = 1 or 2 mA, respectively, demonstrating its effectiveness for efficient power management in high-power miniature biomedical implants.

5.1.6 Comparison and Conclusion

Table 5.2 benchmarks the proposed three-phase regulating RCM rectifier against state-of-the-art RCM designs. It achieves a maximum P_{OUT} of 209.4 mW, measured at V_{IN} = 10 V and D_{COIL} = 0.25 cm without using R_{SNS}. It should be noted that the measured coil distance range does not reflect the maximum achievable WPT distance, as a high-output-impedance waveform generator was used to emulate the TX side, which exhibits a rapid drop in output power with increasing coil separation.

Compared to state-of-the-art, the proposed rectifier maintains reliable residual-free charging over a wide power range, particularly in high-power (strong-coupling) conditions. Combined with dedicated ZVS control, this enables high maximum output power, high peak power efficiency, and a broad high-efficiency load range. Moreover, a freewheeling phase is introduced, pioneering in RCM designs, to support power-efficient in situ output regulation.

With the implemented switching control, the effective charging frequency in RCM can be increased to the carrier frequency in high-power conditions, narrowing the gap between RCM and VM rectifiers. In addition, the resonance-phase input voltage is actively monitored, effectively mitigating over-voltage risks and improving circuit robustness.

Table 5.2 Comparison to state-of-the-art RCM rectifiers.

	JSSC'16 [5.3]	JSSC'20 [5.6]	TPEL'23 [5.7]	TPEL'22 [5.8]	JSSC'24 [5.10]	ISSCC'25 [5.11]	This Work
Technology (nm)	180	180	65	180	65	180	**180**
Active Area (mm^2)	0.544	0.21	0.14	0.54	0.2	1.311	**0.4**
Excitation Frequency (MHz)	0.05	13.56	13.56	5	13.56	6.78	**6.78**
RCM Rectifier Topology	Parallel-LC	Series-LC	Series-LC	Series-LC	Series-LC	Series-LC	**3-Phase**
Residual-Free Charging Phase	Yes	Yes	No	Yes	No	Yes	**Yes**
Maximum Voltage Stress across Switch	$V_{IN}+V_{OUT}$	V_{OUT}	V_{OUT}	V_{OUT}	V_{OUT}	V_{OUT}	**V_{IN} or V_{OUT}**
Freewheeling Phase	No	No	No	No	No	No	**Yes**
Output Regulation Method	Separate DC-DC Stage	Separate DC-DC Stage	Duty Control of Charging Phase	Separate DC-DC Stage	Duty Control of Charging Phase	Separate DC-DC Stage	**Hysteresis Control using Freewheeling Phase**
TX/RX Coil Diameter (mm)	37/2.6[#]	6	150/55×86[##]	28/21	30/30	(N/R)/12	**27/27**
TX Input Voltage (V)	N/R	N/R	40**	40	40**	80**	**1.8 – 10**
TX Topology	N/R	N/R	ADA4870	Half-Bridge[$]	ADA4870	EPC90123	**Half-Bridge[$$]**
Rectifier Output Voltage (V)	3.3*	1.8*	3	1.8*	1; 3 (2 outputs)	N/R	**2.2 – 4.4**
Load-Transient Recovery Time (µs)	N/A	N/A	22	N/A	100	N/A	**Instantaneous**
Measured Coil Distance (cm)	8.5	1.5 – 2	3 – 18.5	1 – 3.2	1 – 4.2	5	**0.25 – 2**
Maximum P_{OUT} (mW) (@ Coil Distance, cm)	0.0017 (8.5)	15.4 (1.5)	150 (18.5)	169 (1)	108 (4.2)	23.7 (5)	**209.4 (0.25)**
Peak PCE (@ Output Power, mW)	61.2% (@0.0017)	92.6% (@10.1)	N/R	84.9% (@16.8)	89%** (@90)	75.1% (@8.559)	**94.5% (@90.8)**

N/A: not applied. N/R: not reported. *unregulated. **estimated from papers or datasheets. [#]Coilcraft coil. [##]rectangular shape. [$]function generator AFG3011. [$$]waveform generator Keysight 33600A.

5.2 A 40.68-MHz WPT System Using a Three-Phase RCM RX Achieving an 8-mm RX Coil[5]

5.2.1 Motivation

In Chapter 4, a closed-loop WPT system was demonstrated with high end-to-end (E2E) efficiency. However, it still relies on RX coils with large inductance and centimeter-scale dimensions, a limitation shared by most reported system designs. This constraint primarily arises from the use of relatively low carrier frequencies, such as 6.78 MHz or 13.56 MHz, within the industrial, scientific, and medical (ISM) bands.

To overcome this limitation, a 40.68-MHz WPT system is proposed to allow millimeter-scale RX coils. The choice of 40.68 MHz within the ISM bands strikes a favorable balance: it allows RX coil miniaturization to millimeter scale without incurring excessive frequency-dependent losses. Though higher-frequency circuits can realize further size reduction, they rely more on passive components and experience sharply increased frequency-dependent losses.

In addition, reducing the RX coil size inevitably weakens the coupling strength for a given coil separation distance, which motivates the adoption of a resonant-current-mode (RCM) topology at RX to maintain robust power delivery under variable weak-coupling conditions. Accordingly, this section introduces a 40.68-MHz WPT system using the three-phase RCM RX.

5.2.1.1 Influence of Carrier Frequency on WPT Links

The use of bulky coils in previous works can be understood by examining the relationship among link efficiency η_{LINK}, RX coil inductance L_2, and carrier frequency f_C. Figure 5.25(a) shows a WPT link model with series resonances at both TX and RX, where R_1 and R_2 are the resistances in TX and RX loops, respectively. Based on electromagnetic theory and Kirchhoff's current law applied to both TX and RX sides [5.1][5.17], the link efficiency, η_{LINK}, defined as the ratio of the power delivered to the load resistance R_{OUT} over the power drawn from the voltage source V_S, is given by

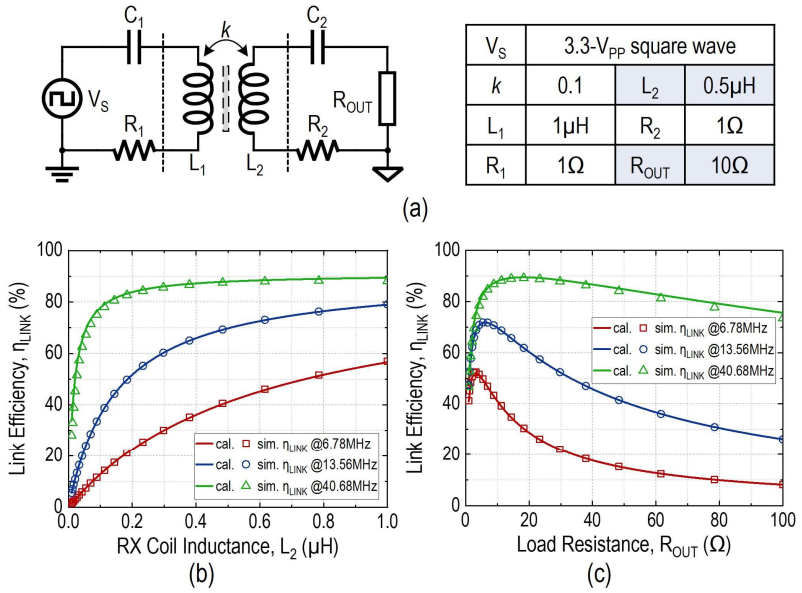
$$\eta_{LINK} = \frac{R_{OUT}}{R_2 + R_{OUT}} \cdot \frac{1}{1 + \frac{R_1(R_2 + R_{OUT})}{k^2\omega^2 L_1 L_2}} \tag{5.4}$$

where k is the coupling factor, and $\omega = 2\pi f_C$. From (5.4), η_{LINK} increases with f_C for a given coil set, implying that higher carrier frequencies allow smaller coils without

[5]based on: T. Lu and S. Du, "A 40.68-MHz Dual-Output Wireless Power Transfer System for Millimeter-Scale Biomedical Implants," in IEEE Journal of Solid-State Circuits, doi: 10.1109/JSSC.2025.3617375.

degrading efficiency.

This trend is verified in Figure 5.25(b), which plots η_{LINK} versus L_2 at R_{OUT} = 10Ω. The solid curves represent analytical predictions from (5.4), and the discrete points are Cadence Virtuoso simulation results using identical parameters. The calculated and simulated results show close agreement. They confirm that achieving the same η_{LINK} at lower operating frequencies, such as 6.78MHz and 13.56MHz, requires significantly larger L_2, which implies physically larger RX coils if R_2 remains constant. Figure 5.25(c) further explores the dependence of η_{LINK} on R_{OUT} at L_2 = 0.5μH. Except under extremely heavy load conditions, which are uncommon in biomedical applications, a higher f_C consistently yields higher η_{LINK}. Hence, prior WPT systems rely on centimetric coils to sustain adequate link efficiency and thus sufficient output power; however, this design choice limits their practical applicability in highly miniaturized biomedical implants.



V_S	3.3-V_{PP} square wave		
k	0.1	L_2	0.5μH
L_1	1μH	R_2	1Ω
R_1	1Ω	R_{OUT}	10Ω

Figure 5.25 WPT link efficiency analysis. (a) WPT link configuration. (b) η_{LINK} versus L_2. (c) η_{LINK} versus R_{OUT}.

5.2.1.2 Limitations of Existing 40.68-MHz WPT Circuits

Driven by practical application needs, 40.68-MHz WPT solutions have been investigated in advanced biomedical systems [5.18][5.19]. Figure 5.26(a) presents a WPT system used for a neural interface, reported in 2024 [5.18]. To support diverse bioelectronic functions, the system provides dual output voltages in different domains. However, the TX operates continuously without global power modulation, reducing the E2E efficiency under light-load conditions. In addition, the RX design employs a conventional 2-stage architecture with passive diode conduction followed by a linear

regulator, resulting in poor PCE and potential thermal safety concerns.

Recent power management research at this frequency has primarily focused on improving RX performance [5.20][5.21][5.22]. For example, dedicated switching control, instead of delay compensation, has been developed for open-loop active rectifiers to mitigate substantial switching delays relative to the short resonant period (<25 ns) at 40.68MHz [5.22]. In 2023, the first regulating rectifier at this frequency was reported, which achieves single-stage dual-output regulation, as shown in Figure 5.26(b) [5.20]. This design uses constant-on-time (5 ns) active diodes to simplify switching control, but incurs reverse currents and hard switching when coupling or load conditions vary. Moreover, it still omits global power modulation, and its full-bridge rectifier (FBR) topology yields a low voltage conversion ratio (VCR), making it unsuitable for loose-coupling scenarios with small RX coils.

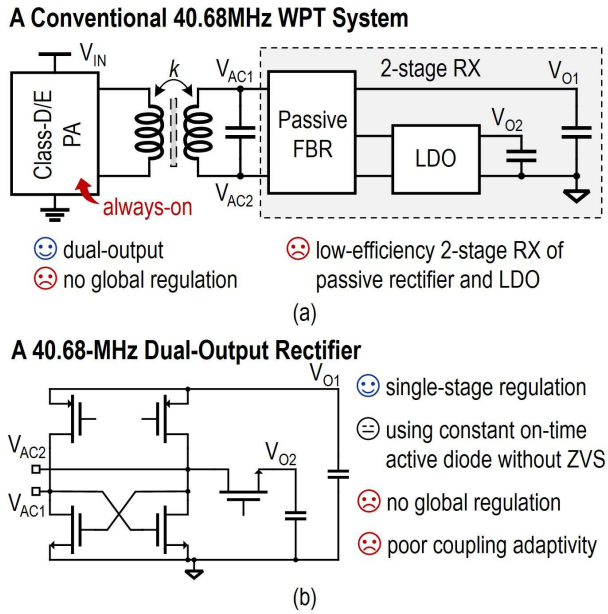


Figure 5.26 Reported WPT designs at 40.68MHz. (a) A system design [5.18]. (b) A rectifier design [5.20].

So far, while existing 40.68-MHz designs address specific application needs, they lack several key circuit advancements, leaving a gap between application requirements and practical implementation. This section presents a 40.68-MHz WPT system that achieves a millimeter-scale RX coil while delivering state-of-the-art (including low-frequency designs) power and efficiency. The system incorporates: 1) global power modulation via a dynamic offtime (DOT) algorithm with an in-band LSK uplink; 2) a single-stage, dual-output resonant-current-mode (DORCM) rectifier at the RX that achieves soft switching and robust adaptability to varying coupling; and 3) an adaptive zero-voltage-switching (AZVS) Class-D PA at the TX that minimizes switching losses and electromagnetic interference.

5.2.2 System-Level Design

The proposed WPT system topology is shown in Figure 5.27, comprising three main stages: AZVS TX, DORCM RX, and the wireless link. The AZVS TX employs a Class-D power amplifier (PA), composed of M_{PTX} and M_{NTX}, to drive a series-resonant L_1–C_1 tank. The DORCM RX consists of four power transistors, M_{P1}, M_{P2}, M_{N1}, and M_{N2}, and two output capacitors, C_{O1} and C_{O2}. M_{P2} and M_{N2} employ dynamic body biasing to prevent unintentional conduction under high V_{AC} or negative V_{C2} conditions. Considering applied voltage stress, M_{PTX}, M_{NTX}, and M_{N2} are implemented by 5-V MOSFET devices, while M_{P1}, M_{P2}, and M_{N1} are 2-V devices. The system adopts DOT-based power modulation, leveraging RX feedback from an in-band LSK uplink. To regulate the two DC output voltages and trigger the uplink signal, the RX operates in three distinct modes that collectively involve four operation phases.

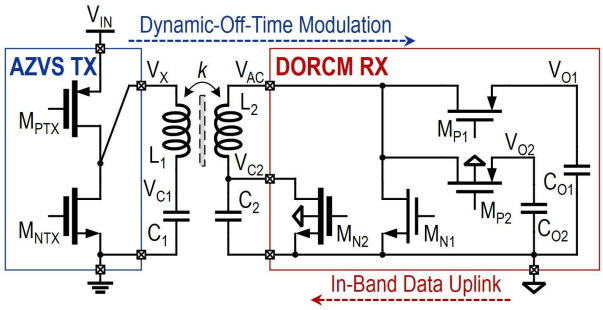


Figure 5.27 Proposed 40.68-MHz WPT system topology.

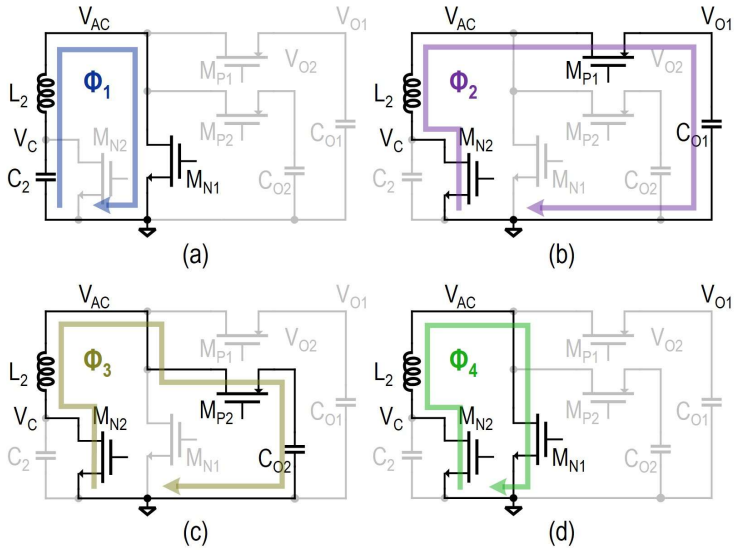


Figure 5.28 Operation phases of the DORCM RX. (a) Resonance phase Φ_1. (b) V_{O1}-charging phase Φ_2. (c) V_{O2}-charging phase Φ_3. (d) Freewheeling phase Φ_4.

5.2.2.1 Dual-Output RCM Rectifier

Though operating at 40.68MHz, a smaller RX coil weakens the wireless link coupling condition and increases its sensitivity to misalignment and separation distance variations, thereby requiring a high-VCR RX. The three-phase regulating RCM topology is an excellent candidate compared to VM and prior RCM counterparts, and this work utilizes the topology with a dual-output configuration.

The RX has four RX operation phases: the resonance phase (Φ_1), V_{O1}-charging phase (Φ_2), V_{O2}-charging phase (Φ_3), and the freewheeling phase (Φ_4), as shown in Figure 5.28(a)-(d). In Φ_1, only M_{N1} is turned on, allowing the L_2–C_2 tank to freely resonate and accumulate energy. In Φ_2, M_{P1} and M_{N2} are turned on, enabling L_2, as a current source, to deliver the accumulated charge to C_{O1}. In Φ_3, M_{P2}, instead of M_{P1}, is turned on to direct charge to C_{O2} in a similar fashion. In Φ_4, M_{N1} and M_{N2} are turned on, shorting L_2 and thus interrupting the L_2-C_2 resonance.

Table 5.3 RX mode-phase mapping.

Mode @RX	**MD_1**	**MD_2**	**MD_{LSK}**
Phase operation	$\Phi_1 \leftrightarrow \Phi_2$	$\Phi_1 \leftrightarrow \Phi_3$	Φ_4

Based on the four phases, the RX operates in three distinct modes to fulfill its functionality: V_{O1}-charging mode (M_{D1}), V_{O2}-charging mode (M_{D2}), and power-data uplink mode using LSK (MD_{LSK}). The mapping between RX modes and phases is summarized in Table 5.3. In MD_1, the RX alternates between Φ_1 and Φ_2 to charge V_{O1}, while in MD_2, it alternates between Φ_1 and Φ_3 to charge V_{O2}. In MD_{LSK}, the RX enters Φ_4, during which it presents a distinct reflected impedance at the TX than the normal charging modes MD_1 and MD_2. The equivalent reflected impedance, Z_{REF}, in both cases is expressed as

$$Z_{EQ} = \begin{cases} \dfrac{\omega^2 M^2}{R_2 + R_{ON}} \cdot \lambda, (in\ \mathrm{MD}_1, \mathrm{MD}_2) \\ \dfrac{\omega^2 M^2}{R_2 + R_{ON} + j\omega L_2}, (in\ \mathrm{MD}_{LSK}) \end{cases} \tag{5.5}$$

where $M = k\sqrt{L_1 L_2}$ denotes the mutual inductance between the coupled L_1 and L_2 (k is the coupling coefficient), R_2 is the loop resistance in the L_2-C_2 tank, R_{ON} denotes the on-resistance of a power transistor, and λ is a near-unity factor representing the time-averaged impedance transformation of the RCM operation, as discussed in Chapter 4. From (5.5), Z_{EQ} is largely reduced in MD_{LSK}, resulting in an increased current amplitude in the L_1–C_1 tank. This result matches the analysis in Section 5.1.2, enabling the in-band data backscattering.

5.2.2.2 Global Dynamic-Off-Time Modulation

As discussed in Chapters 2 and 4, global power modulation is an effective approach to improve E2E efficiency by adapting the TX power to varying RX load conditions. In [5.23], constant-off-time (COT) modulation was proposed, which disables the TX power stage for a fixed duration once the RX output voltage reaches its target level. This enables fully on/off TX operation and provides a wide power adjustment range. However, it suffers from poor load regulation and can induce large output voltage ripples under heavy-load conditions. Hysteresis control (Hyst), proposed in [5.24] and demonstrated in Chapter 3, maintains the RX output voltage within a hysteresis window, resulting in nearly load-independent output ripples. Nonetheless, it requires the TX to remain in a power-leaking standby mode while the RX is off to detect the lower-threshold trigger, thereby narrowing the TX power adjustment range and reducing E2E efficiency under light-load conditions. In Chapter 4, pulse-width modulation (PWM) has been introduced to balance the trade-off between output voltage ripple and E2E efficiency by adjusting TX's on/off duty ratio while keeping the total modulation period constant. It can be implemented using phase-locked-loop (PLL)-based analog methods [5.25][5.26] or look-up table (LUT)-based digital methods (see Chapter 4). The analog approach offers tight voltage regulation but suffers from slow transient responses, whereas the digital method responds quickly to load transients but requires complex, areaconsuming hardware implementations. In addition, the LUT size increases rapidly if the total modulation period is lengthened.

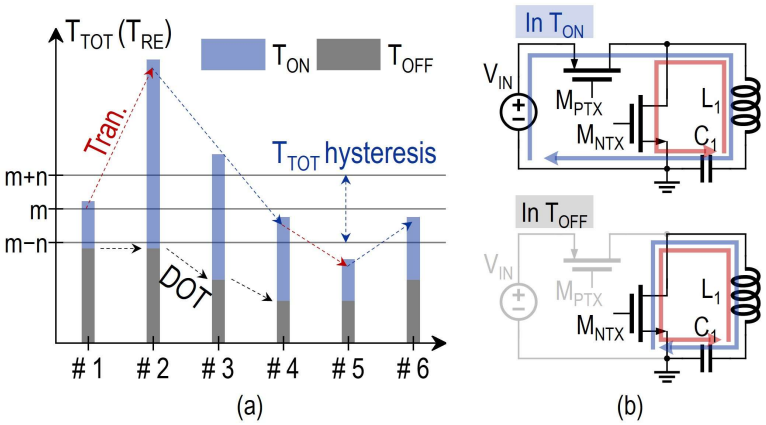


Figure 5.29 Dynamic-off-time (DOT) modulation. (a) Operation principle. (b) Corresponding TX operation phases.

To overcome the limitations of prior approaches, dynamic-off-time (DOT) modulation is proposed. As shown in Figure 5.29(a), the proposed DOT algorithm regulates the total modulation period (T_{TOT}), comprising a TX-on period (T_{ON}) and a TX-off period (T_{OFF}), within a hysteresis window centered at m × T_{RE} and bounded by a width of 2n × T_{RE}, where $T_{RE} = 1/f_C$ is the resonant period. When T_{TOT} exceeds the hysteresis boundaries (#1→#2 or #4→#5), the TX adjusts T_{OFF} stepwise (#2→#3→#4

or #5→#6). To avoid oscillatory toggling in T_{TOT}, the adjustment step α should be set smaller than the hysteresis window width, which is given by

$$\frac{T_{OFF,i}}{T_{OFF,i\pm1}} = \frac{T_{TOT,i}}{T_{TOT,i\pm1}} = \alpha < \frac{m+n}{m-n} \tag{5.6}$$

where the ± sign accounts for both increasing and decreasing T_{OFF} cases. Figure 5.29(b) illustrates the two operation phases of the Class-D PA TX: during T_{ON}, the Class-D PA drives the L_1–C_1 tank with symmetric pulsing (active state); during T_{OFF}, only M_{NTX} remains closed, allowing the L_1–C_1 tank to freewheel without drawing power from V_{IN} (idle state).

From (5.6), a larger α yields a wider hysteresis window. A wide window can degrade load regulation (as in constant-off-time control), whereas a small adjustment step can slow the transient response (as in analog PWM). In practice, α should be chosen to balance regulation accuracy and response speed based on application requirements. In this prototype, m = 128×T_{RE} and n = 32×T_{RE} are selected, resulting in α = 1.5. The corresponding available T_{OFF} values are 0, 8, 12, 18, 27, 40, 60, and 90 (×T_{RE}), where the value "0" is intentionally included to support extremely heavy-load conditions.

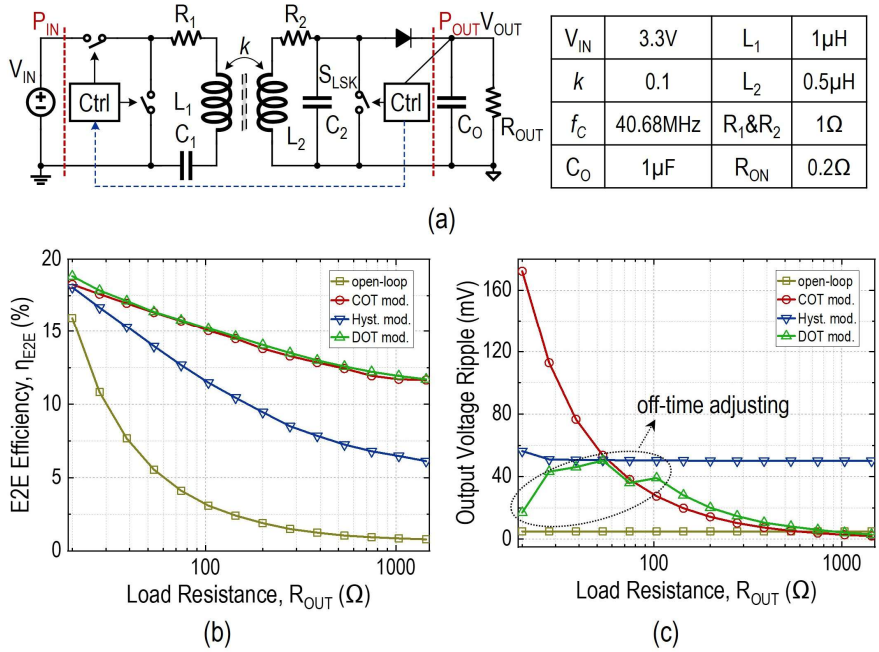
It is worth noting that the proposed global modulation method exhibits integral-like behavior without derivative action, which can result in slower load regulation. An additional local regulator can be used at the RX if faster output regulation is required. In addition, the DOT modulation operates as a discrete-time digital feedback loop. Though the uplink latency can introduce extra loop delay, stability is ensured by: 1) the hysteresis window that bounds T_{TOT} and 2) the fixed adjustment step α = 1.5 that limits loop gain.

Compared to prior methods, the proposed DOT modulation enables fully on/off TX operation under regulation for improved E2E efficiency than Hyst, while achieving smaller ripple by adjusting T_{OFF} than COT. Unlike analog PWM methods, the proposed scheme allows faster load transients without complex compensation. Compared to digital PWM methods, it offers slightly slower regulation but greatly simplifies the digital implementation by eliminating large LUTs, and permits longer T_{TOT} settings to flexibly balance ripple and efficiency for different applications.

The proposed DOT method is further quantitatively compared against COT, Hyst, and open-loop control, as shown in Figure 5.30. A Class-D PA is adopted at the TX, and a half-bridge rectifier (HBR) is used at the RX [Figure 5.30(a)]. When the RX output voltage V_{OUT} reaches 1.8V, the backscattering switch S_{LSK} turns on, idling the HBR and switching the TX to "OFF" state. For DOT and COT, the TX in the "OFF" state is fully disabled, as shown in Figure 5.29(b). The DOT method employs the α = 1.5 configuration, while COT applies a fixed TX-off period of 64 × T_{RE}. For Hyst, the TX in the "OFF" state periodically skips three positive drive pulses, resulting in 1/4× output power. It resumes "ON" state when V_{OUT} drops below 1.75V. For the open-loop

method, the TX remains on, as shown in Figure 5.29(a). All switches and the HBR diode are assumed to have identical on-resistance, R_{ON}. The E2E efficiency, η_{E2E}, is defined as the ratio of P_{OUT} to P_{IN}.

Figure 5.30(b) and (c) show η_{E2E} and output voltage ripple, respectively, as functions of load resistance R_{OUT} ranging from 20Ω to 1.5kΩ. The DOT method presents a rough ripple profile because of the 1.5×T_{OFF} adjustment step. The results confirm that DOT and COT modulation achieve high η_{E2E}, thanks to fully on/off TX operation. Meanwhile, DOT and Hyst exhibit small output voltage ripples, owing to their adjustable TX-off periods.



V_{IN}	3.3V	L_1	1μH
k	0.1	L_2	0.5μH
f_C	40.68MHz	R_1&R_2	1Ω
C_O	1μF	R_{ON}	0.2Ω

Figure 5.30 Comparison of global modulation methods. (a) WPT system implementation. (b) η_{E2E} versus R_{OUT}. (c) Output voltage ripple versus R_{OUT}.

5.2.2.3 System-Level Operation

Figure 5.31 presents the system-level operation waveforms. During a light-to-heavy load transient at V_{O2}, as shown in Figure 5.31(a), T_{TOT} can exceed the upper hysteresis bound, and the DOT algorithm correspondingly shortens T_{OFF}, thereby suppressing the ripple on V_{O2}. Since T_{TOT} remains within the hysteresis window both before and after the transient, the charging/discharging duty ratio of V_{O1} may vary only slightly or remain unchanged, resulting in negligible ripple variation on V_{O1} across the transient. Notably, cross regulation (undershoots) at V_{O1} may still occur during transients due to the temporarily extended T_{OFF}.

During each T_{ON}, the RX follows the sequence $MD_1 \Rightarrow MD_2 \Rightarrow MD_{LSK}$. Upon

detecting the RX LSK, the TX evaluates whether T_{TOT} exceeds the hysteresis bounds and adjusts T_{OFF} accordingly.

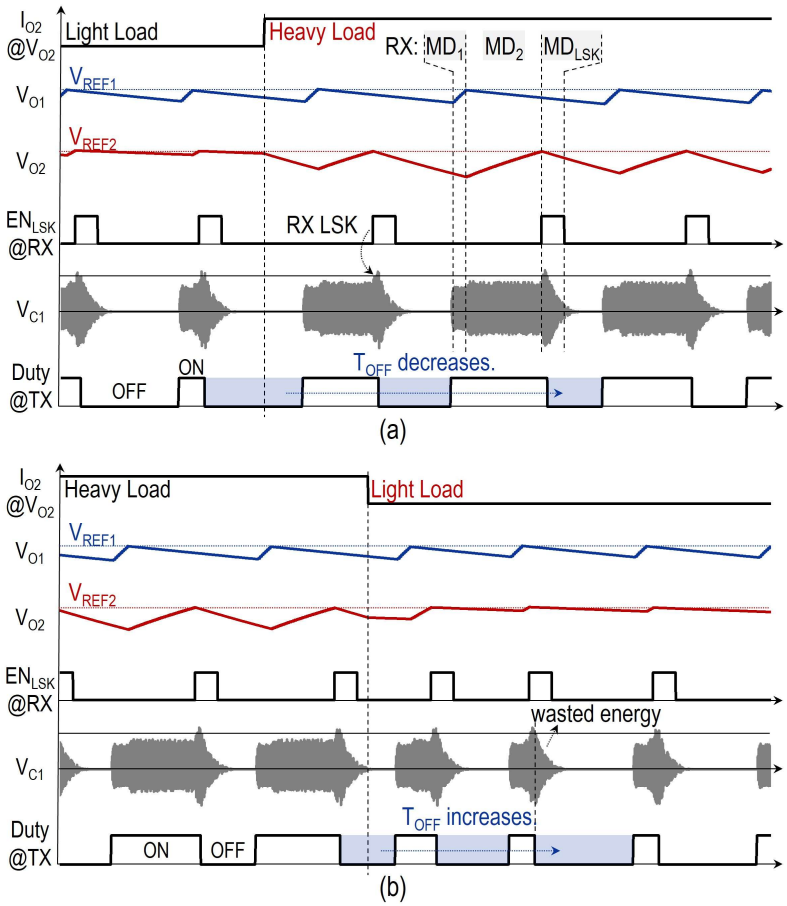


Figure 5.31 System-level operation waveforms. (a) During a light-to-heavy load transient. (b) During a heavy-to-light load transient.

Figure 5.31(b) shows the waveforms during a heavy-to-light load transient at V_{O2}. In this case, T_{OFF} is increased if T_{TOT} falls below the lower hysteresis bound. Owing to instantaneous mode switching at the RX, no overshoots are observed at either V_{O2} or V_{O1}. In principle, when the RX is in MD_{LSK}, it stops receiving power from the TX, and the residual resonant energy in the L_1–C_1 tank is likely wasted during T_{OFF}. Unlike COT, DOT modulation can extend T_{OFF} under light-load conditions, mitigating this negative impact on E2E efficiency.

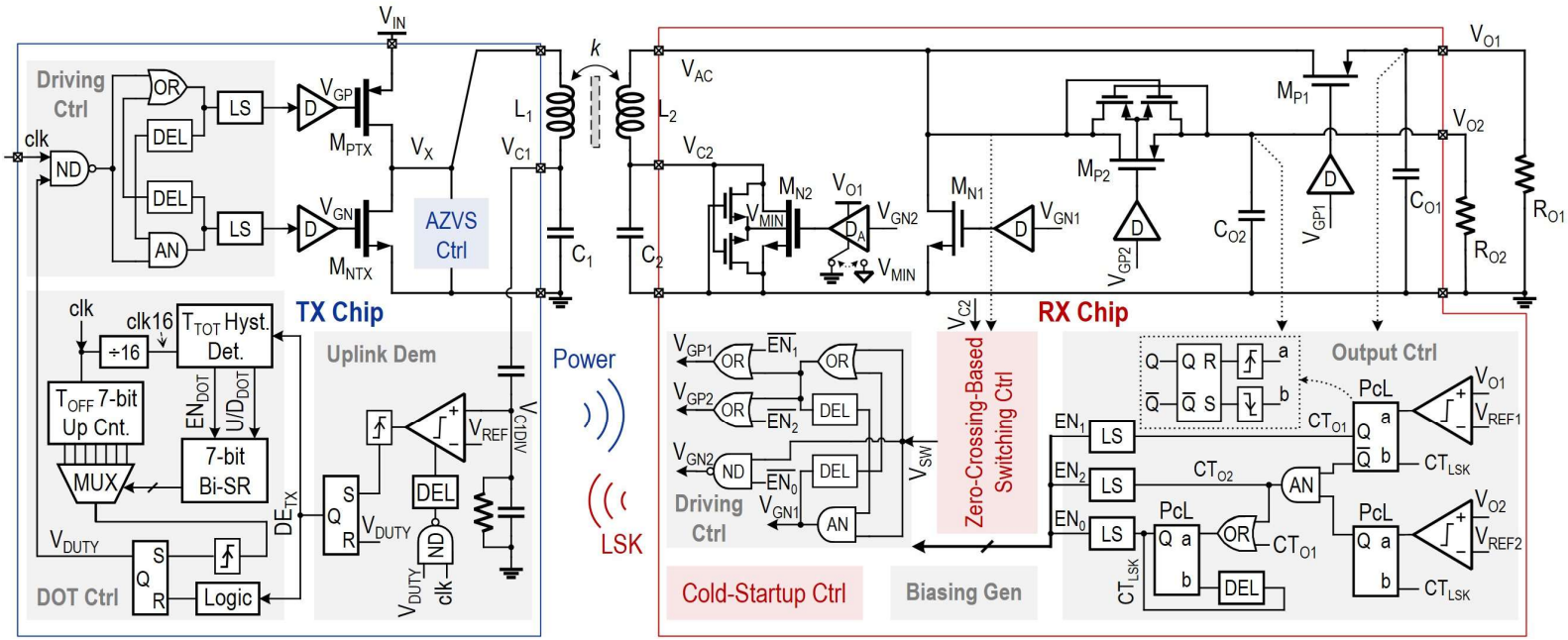


Figure 5.32 System architecture of the proposed 40.68-MHz single-link dual-output WPT system.

5.2.3 Circuit Implementations

Figure 5.32 shows the proposed WPT system architecture. At the TX, a 40.68-MHz clock signal, clk, drives the Class-D PA and establishes the dead time between the gate driving signals V_{GP} and V_{GN}. Zero-voltage switching at node V_X is enabled by the AZVS control block (AZVS Ctrl). The uplink demodulation block (Uplink Dem) monitors the voltage amplitude across C_1 to detect the uplink signal from the RX [5.13]. Upon receiving an uplink pulse, the output of Uplink Dem, DE_{TX}, asserts high to initiate T_{TOT} hysteresis evaluation and pull down the latched signal V_{DUTY} within the DOT control block (DOT Ctrl). This transitions the Class-D PA into the idle state via the driving control block (Driving Ctrl). If T_{TOT} exceeds its hysteresis window [96 × T_{RE}, 160 × T_{RE}], the DOT Control block updates the multiplexer selection to modify the subsequent T_{OFF}. When T_{OFF} ends, a logic-high output from the T_{OFF} counter sets V_{DUTY} high again, triggering the Class-D PA back to the active state.

At the RX, M_{N2} is driven by an adaptive gate driver that can clamp its gate voltage to the lower of V_{C2} and ground, ensuring reliable turn-off during the resonance phase (Φ_1) [5.27][5.28]. The DC output voltages V_{O1} and V_{O2} are compared with reference voltages V_{REF1} and V_{REF2}, respectively, within the output control block (Output Ctrl). The comparison results are latched by pulse-controlled latches (PcL) to generate three time-multiplexed enable signals, EN_1, EN_2, and EN_0, only one of which is asserted high at any given time to indicate the RX operation mode. The RX switching behavior is governed by the zero-crossing-based switching control block (Switching Ctrl), which outputs the control signal V_{SW} to the driving control block (Driving Ctrl); Driving Ctrl then generates the gate-driving signals V_{GP1}, V_{GP2}, V_{GN1}, and V_{GN2}, conditioned upon the state of the enable signals. In addition, the RX supports cold-startup, to be discussed shortly.

Figure 5.33 shows the simulated waveform of the DOT control block with detailed logic timing. Case 1 represents steady-state operation. At the rising edge of DE_{TX}, EN_{DOT} remains low, indicating that T_{TOT} stays within the hysteresis window; therefore, T_{OFF} remains constant. At the next falling edge of clk, DOT Ctrl will lower V_{DUTY} to turn off the TX power stage and reset the logic. Case 2 represents a load-transient condition. At the rising edge of DE_{TX}, EN_{DOT} is already high, meaning T_{TOT} exceeds the hysteresis bounds. DOT Ctrl then checks U/D_{DOT}: if it is logic low, the next T_{OFF} will be decreased. At the next falling edge of clk, DOT Ctrl lowers V_{DUTY} to turn off the TX power stage, reset the logic, and start counting the new T_{OFF}, whose duration is set according to the updated T_{OFF} option. Figure 5.34 shows the circuit implementation of T_{TOT} hysteresis detector (T_{TOT} Hyst. Det.), explaining the generation of EN_{DOT} and U/D_{DOT}.

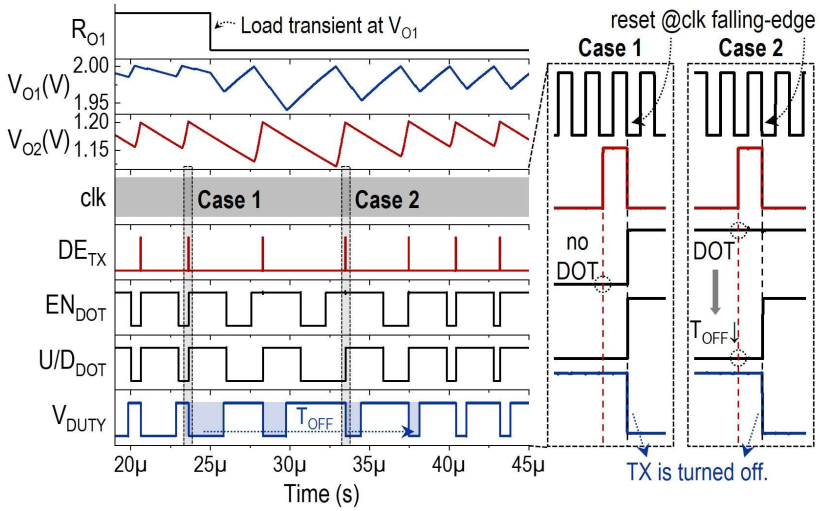
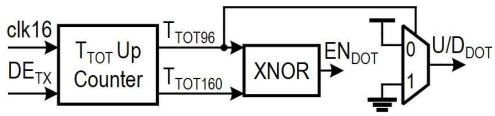


Figure 5.33 Simulated waveform of the DOT control block.



T_{TOT}	<96	[96,160)	≥160
T_{TOT96}	"0"	"1"	"1"
T_{TOT160}	"0"	"0"	"1"

Figure 5.34 Circuit implementation of T_{TOT} hysteresis detector.

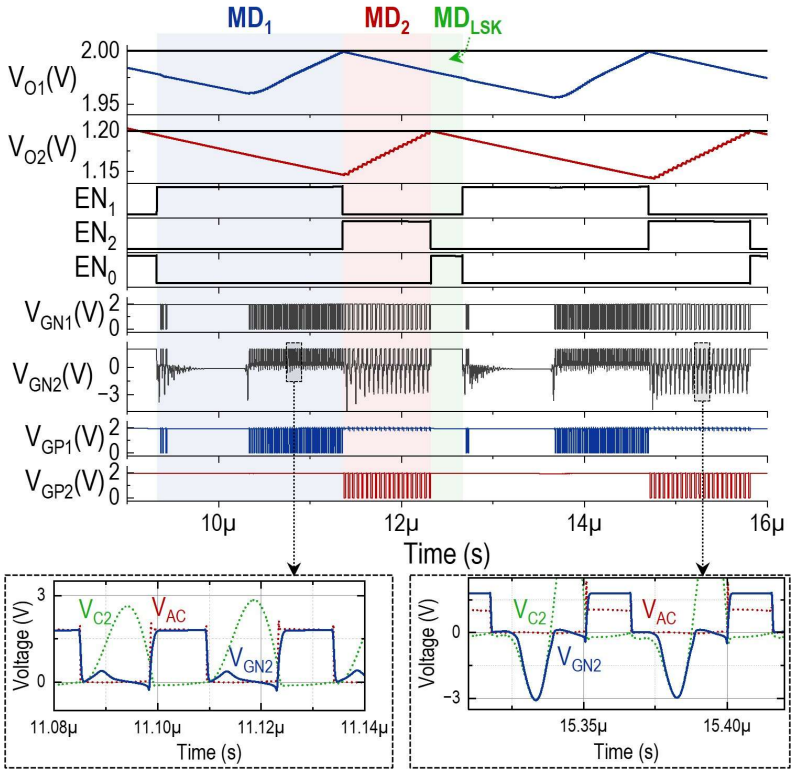


Figure 5.35 Simulated waveform of the DORCM RX.

Figure 5.35 shows the detailed simulated waveform of the DORCM RX. Notably, after the RX switches from MD_{LSK} to MD_1, it can still enable a few additional charging phases to V_{O1} even after the TX has turned off its power stage. This occurs because the L_1–C_1 tank retains residual resonant energy (see Figure 5.31). This residual reception helps reduce TX energy waste during T_{OFF}. In addition, V_{GN2} follows V_{C2} during resonance phases when V_{C2} is lower than ground, allowing L_2–C_2 resonance without interference from M_{N2}.

5.2.3.1 RX Zero-Crossing-Based Switching Control

Interfacing a variable link, the RCM rectifier can stay in the resonance phase (Φ_1) for either a single resonant period (T_{RE}), referred to as single-period Φ_1 (SP-Φ_1) case, or multiple periods, referred to as multi-period Φ_1 (MP-Φ_1) case. This requires the RX to detect the resonance energy level during each T_{RE}. If sufficient energy is detected, the RX transitions from Φ_1 to Φ_2, or Φ_3, to deliver energy to the outputs. Prior RCM designs operating at 6.78MHz or 13.56MHz typically employ continuous-time comparators to detect peak resonance voltage across C_2, while using delay-compensation techniques in comparators for accurate phase switching control [5.6][5.8][5.28]. However, these approaches do not scale well to 40.68MHz: continuous-time comparators may fail to capture sharp voltage peaks due to limited bandwidth, and comparator-based delay compensation schemes demand impractically large voltage offsets as T_{RE} shortens at 40.68MHz. This further requires comparators with wide dynamic range and sufficient input voltage swing. Though increasing bias current can ease these requirements, it sharply increases power consumption. Some designs mitigate the switching-control challenges by performing resonance energy detection and phase switching over two adjacent resonance periods [5.6]. Nonetheless, it precludes SP-Φ_1 operation, compromising system performance under high-power conditions.

Figure 5.36 shows the proposed single-mode zero-crossing based switching controller, which seamlessly supports both SP-Φ_1 and MP-Φ_1 operations. In the resonant L_2-C_2 tank, a zero-crossing of V_{AC} coincides with a peak in V_{C2}. Hence, to detect the energy level during Φ_1, a zero-crossing detector (ZCD) is used to identify the V_{AC}-zero events, which in turn trigger a clocked comparator. This comparator evaluates a DC-shifted, scaled version of V_{C2} (V_{C2DIV}), generated by the V_{C2} Shifter block, against a reference voltage V_{REN}. Unlike continuous-time comparators, this combination of a ZCD and a clocked comparator outcomes the ”resonance-good” signal V_{CHG} (on its rising edge) with a well-defined delay, mainly from the ZCD. To trigger the RX transition from Φ_1 to Φ_2 (or Φ_3), an additional delay, t_{DL1}, is introduced from V_{CHG} by Digital-Controlled Delay Line 1 (DCDL1) to align with the I_2 peak, which corresponds to the V_{C2} zero. DCDL2 subsequently determines the charging duration (t_{DL2}) and initiates the RX transition back to Φ_1 when I_2 reaches zero. Notably, the resonance detection with a properly set V_{REN} also protects M_{N2} from overvoltage stress by triggering the charging phase before V_{C2} approaches the device breakdown limit. In

addition, V_{REN} influences the RX power capability by defining the resonance phase duration [5.4]. In this work, V_{REN} is externally set and held constant during operation to meet only the safety-operation requirement.

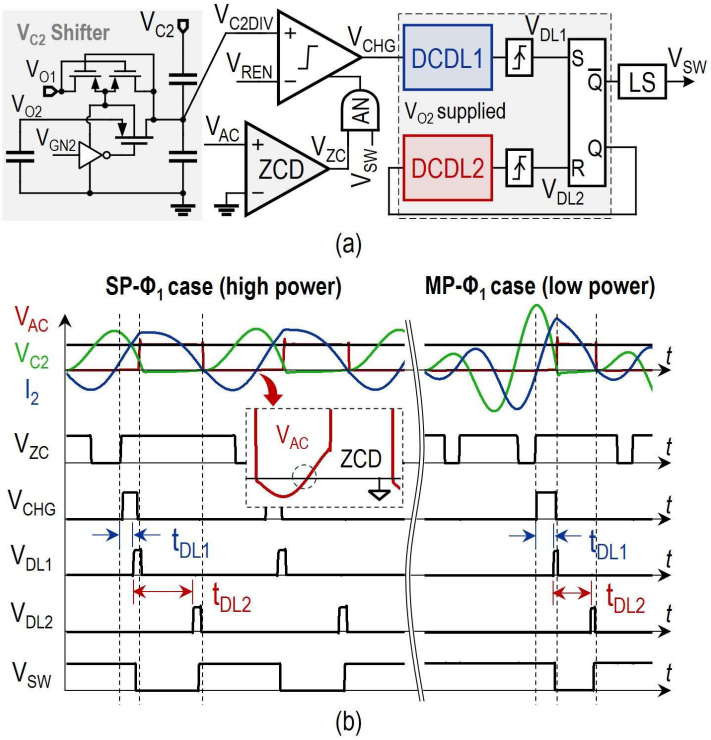


Figure 5.36 RX zero-crossing-based switching controller. (a) Circuit implementation. (b) Operation waveform.

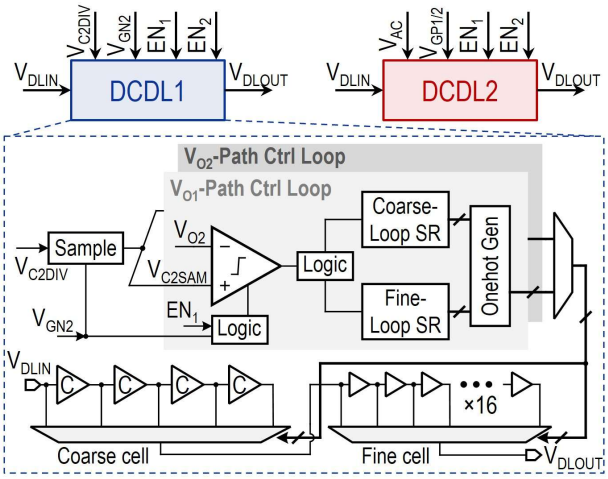


Figure 5.37 Circuit implementation of the digital-controlled delay line (DCDL) in the RX switching controller.

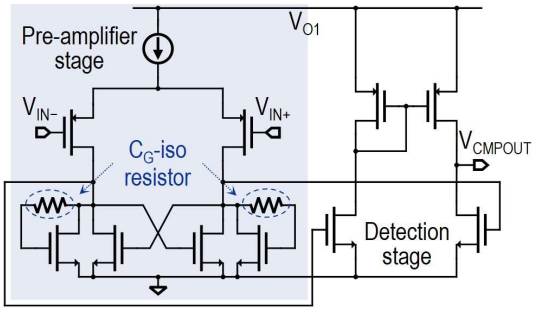


Figure 5.38 Circuit implementation of the zero-crossing detector (ZCD) in the RX switching controller.

Figure 5.37 shows the circuit implementation of DCDL1, while DCDL2 employs a similar structure. DCDL1 samples V_{C2DIV} at the rising edge of V_{GN2} and then compares the sampled value V_{C2SAM} with the DC component of V_{C2DIV}, V_{O2}. Under ideal zero-voltage switching of M_{N2}, V_{C2} is grounded, making V_{C2DIV} equal to V_{O2}. If a switching error is present, DCDL1 adjusts its delay line stepwise, guided by the comparison result. The delay line includes a 2-bit coarse cell and a 4-bit fine cell, offering a practical balance between tuning range, resolution, and hardware consumption. The unit delays of the coarse and fine cells are 3.1 ns and 290 ps, respectively. DCDL2 achieves zero-voltage turn-off of M_{P1} (or M_{P2}) at the end of Φ_2 (or Φ_3) by monitoring V_{AC} at the rising edge of V_{GP1} (or V_{GP2}). Both DCDL integrate two separate control loops for V_{O1}-charging mode (MD_1) and V_{O2}-charging mode (MD_2), enabling seamless mode transitions from MD_1 to MD_2. To ensure accurate peak-V_{C2} detection, the ZCD adopts a continuous-time two-stage structure that provides low offset and high speed, as shown in Figure 5.38 [5.29]. It has a typical power consumption of 38 μW.

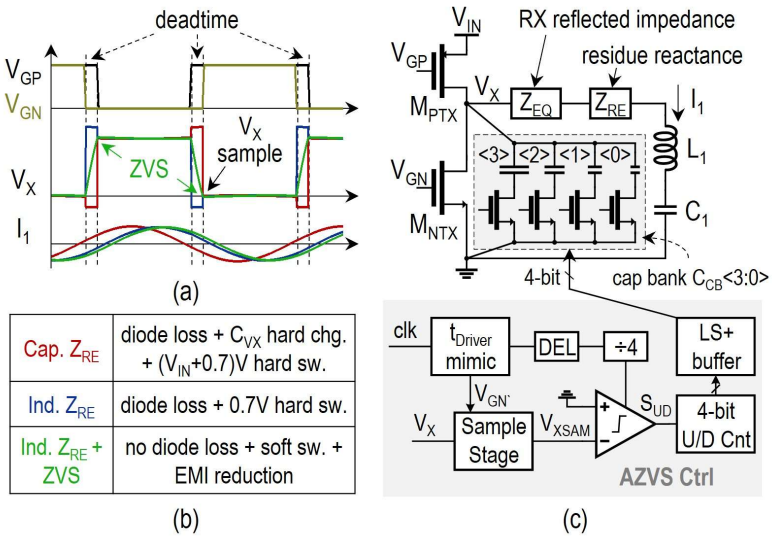
It is worth noting that the proposed ZCD + DCDL method differs from conventional comparator-based delay compensation methods by directly adjusting delay elements to compensate for the control loop delay, thereby avoiding voltage-to-time conversion in comparators. As a result, it eliminates the trade-off among dynamic range, input swing, and power consumption inherent in conventional methods.

5.2.3.2 TX Adaptive-ZVS Control

In Class-D PAs, to prevent shoot-through currents between the supply and ground, a dead time is usually inserted between the conduction periods of high-side and low-side switches. However, beyond inherent gate-driving and conduction losses, load conditions and parasitics at the mid-node can introduce additional power loss during this interval. This issue becomes more pronounced at 40.68MHz, where the dead time occupies a larger fraction of the switching cycle.

In practical WPT scenarios, the Class-D PA may experience either inductive or capacitive loading due to the residual reactance of the L_1–C_1 tank (Z_{RE}) and the equivalent reflected impedance from the RX (Z_{EQ}). Under ideal resonance at the RX, Z_{EQ} is mostly real, and the nature of Z_{RE} determines whether the PA exhibits capacitive

or inductive switching behavior, each associated with different power loss characteristics, as shown in Figure 5.39(a)–(b). Prior works have favored inductive Z_{RE} to alleviate hard switch turn-on and mitigate the charging/discharging of the parasitic capacitance at V_X (C_{VX}) [5.30]. However, body-diode conduction and hard switching persist.

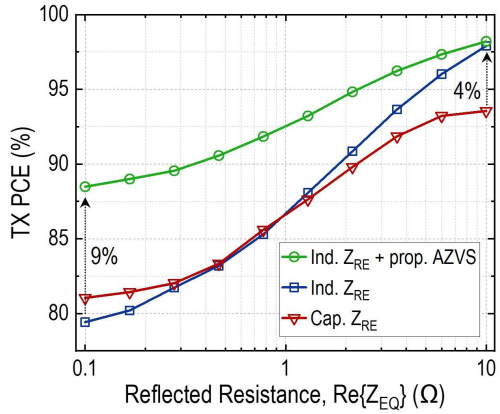


Cap. Z_{RE}	diode loss + C_{VX} hard chg. + (V_{IN}+0.7)V hard sw.
Ind. Z_{RE}	diode loss + 0.7V hard sw.
Ind. Z_{RE} + ZVS	no diode loss + soft sw. + EMI reduction

(b)

Figure 5.39 (a) Switching waveforms and (b) loss characteristics of a Class-D PA under different load impedance conditions. (c) TX adaptive zero-voltage switching Class-D PA implementation.

To address the abovementioned issues, this work applies an adaptive zero-voltage switching (AZVS) strategy, as shown in Figure 5.39(c). It introduces programmable capacitance at V_X to compensate the lagging current (I_1) under inductive Z_{RE}, enabling zero-voltage switch turn-on at the end of the dead time and eliminating diode losses. In addition, the softened V_X waveform helps reduce electromagnetic interference. A 4-bit capacitor bank connected to V_X with binary-weighted capacitance values, C_{CB}<3:0>, is controlled by an AZVS control block (AZVS Ctrl). At each rising edge of V_{GN}, V_X is sampled as V_{XSAM}. V_{XSAM} is then compared with the TX ground once every four periods. The lower adjustment speed helps ensure a stable loop. If V_X drops below ground when M_{NTX} turns on, AZVS Ctrl increases the total capacitance at V_X to reduce its slew rate; otherwise, it decreases C_{VX}, as indicated by signal S_{UD}. Notably, charging or discharging the added capacitance does not incur charge-sharing losses, as I_1 is regulated by L_1. It is worth mentioning that the proposed AZVS method operates only when Z_{RE} in the L_1–C_1 loop is inductive. This can be intentionally achieved by slightly increasing either L_1 or C_1 at the TX. If a capacitive Z_{RE} arises due to coil shape distortion, aging effects, or other factors, the AZVS method can only disable the entire capacitor bank to minimize hard-switching loss but cannot maintain ZVS. Achieving ZVS with a capacitive Z_{RE} requires impedance matching techniques [5.31].



f_C	40.68MHz
L_1	510nH
C_1	29pF/31pF (ideal 30pF)
C_{VX}	A few pF
$C_{CB<3:0>}$	40, 20, 10, 5pF
R_1	1Ω
R_{ONTX}	0.2Ω
R_{ONCB}	0.05Ω
t_{DDT}	1ns

Figure 5.40 Simulated TX power conversion efficiency (PCE) under different C_1 and ZVS conditions.

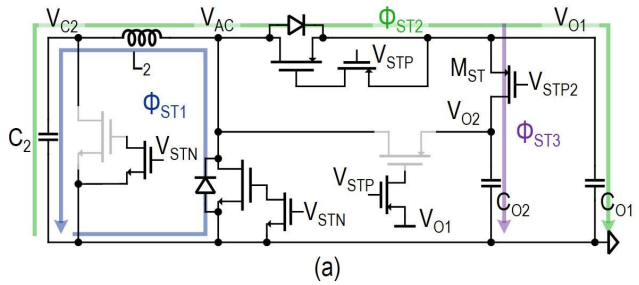
Figure 5.40 shows simulated TX power conversion efficiency (PCE) under various C_1 and ZVS conditions. The purely real Z_{EQ} is swept from 0.1Ω to 10Ω, and simulation parameters are listed on the right. In simulation, C_1 is set to either 29 pF or 31 pF, corresponding to capacitive or inductive Z_{RE} conditions, respectively; perfect resonance occurs near C_1 = 30 pF. A few picofarads of parasitic capacitance are assumed at V_X, attributed to M_{PTX}, M_{NTX}, and off-chip interconnections. R_1 represents the resistance in the TX loop. The on-resistances of M_{PTX}/M_{NTX} and the capacitor bank switches are denoted as R_{ONTX} and R_{ONCB}, respectively. The dead time is fixed at 1 ns, matching the near1 ns slew rates of V_{GP} and V_{GN}. Simulation results confirm that the proposed AZVS control enhances TX PCE across the entire load range, with improvements of up to 9% than either inductive or capacitive Z_{RE} cases.

It is important to note that the capacitance values in the capacitor bank should be designed by simultaneously considering several parameters: (1) the residual inductance in the L_1-C_1 tank, (2) the load resistance range of the Class-D PA, and (3) the switching deadtime of the Class-D PA. The first two parameters influence the current phase and amplitude in the L_1-C_1 loop, respectively, and the third determines the voltage integration time across the capacitance at node V_X. In addition, though the added capacitance from the capacitor bank always connects to V_X, it only affects the slew rate of V_X during deadtime and does not impact the L_1-C_1 resonance and normal conducting phases of the Class-D PA. For example, when M_{PTX} is on, the added capacitance is effectively merged with the input voltage source, whereas when M_{NTX} is on, it is shorted by the low on-resistance of M_{NTX}.

5.2.3.3 RX Cold-Startup Configuration

As the supply for an implanted device, the RX must be capable of starting up from the cold state. Figure 5.41 shows the proposed RX startup configuration. In the cold state, the RX cannot operate in active RCM mode and instead relies solely on passive diode connections. Therefore, M_{P2} and M_{N2} are not usable due to their dynamic body

biasing considering body effect. On the other hand, the diode connections of M_{P1} and M_{N1} form a half-bridge rectifier (HBR), enabling V_{O1} to charge up. To charge V_{O2}, a P-type startup switch, M_{ST}, connects V_{O1} and V_{O2}. To ensure its robust turn-off in normal operation, the body of M_{ST} is tied to the higher potential V_{O1}. At the beginning of the startup, its gate (V_{STP2}) is grounded. As a result, M_{ST} turns on when V_{O1} exceeds the PMOS threshold, allowing V_{O2} to charge. This phase is referred to as State 1. Once V_{O2} reaches a sufficient level while V_{O1} is only higher by the conduction drop across M_{ST}, M_{ST} will be turned off by pulling V_{STP2} up to V_{O1}. Thereafter, the HBR continues charging V_{O1} until it reaches its target level. This phase is defined as State 2.



	State 1	State 2
Φ_{ST}	1+2+3	1+2
V_{STP}	gnd	gnd
V_{STN}	V_{O1}	V_{O1}
V_{STP2}	gnd	V_{O1}

(b)

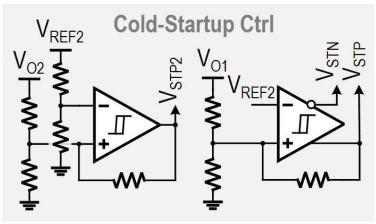


Figure 5.41 RX cold-startup setting. (a) Topology configuration. (b) Operation state table. (c) Circuit implementation of the cold-startup controller.

During startup, all four power transistors are switched off via control signals V_{STP} and V_{STN}. The cold-startup controller (Cold-Startup Ctrl) generates the three control signals V_{STP}, V_{STN}, and V_{STP2}, as shown in Figure 5.41(c). At the beginning of cold startup, circuit blocks are inoperable due to the low supply voltage; however, V_{STP} and V_{STP2} are pulled low through resistive paths to ground. Once the supply voltage V_{O1} rises sufficiently, the comparators begin to function and produce the appropriate outputs. Specifically, V_{STP2} transitions high when the divided V_{O2} exceeds the divided V_{REF2}, while V_{STP} and V_{STN} swap polarities once the divided V_{O1} surpasses V_{REF2}, indicating the completion of cold startup. The resistor divider ratios are designed to match the target levels of V_{O1}, V_{O2}, and the reference V_{REF2}.

To enable correct operation, a self-startup reference generator, e.g., a threshold-based voltage reference or a self-startup bandgap reference, is required to ensure V_{REF2} settles before any polarity transitions of the control signals occur.

5.2.4 Measurement Results

The proposed TX and RX chips are fabricated in a 180nm BCD technology, occupying silicon areas of 1.2mm^2 and 1.4mm^2, respectively, as shown in Figure 5.42. The measurement setup is illustrated in Figure 5.43. The spiral RX coil (L_2) is realized using a single-layer PCB with an 8-mm diameter and an inductance of 92.7nH. Its dimension is possible to be designed further smaller with the same inductance; however, that will result in a smaller k under the same coil separation condition. The output capacitors C_{O1} and C_{O2} are mainly implemented off-chip, each with a capacitance of 100 nF. The coaxial coil separation distance D_{COIL} is adjustable to emulate varying coupling conditions in practical applications. For efficiency measurements, a current probe is used to sample the TX input power with minimal disturbance to the high-energy power path. Meanwhile, the RX input power is measured via a shunt-based method combining R_{SNS} with a high-bandwidth differential probe.

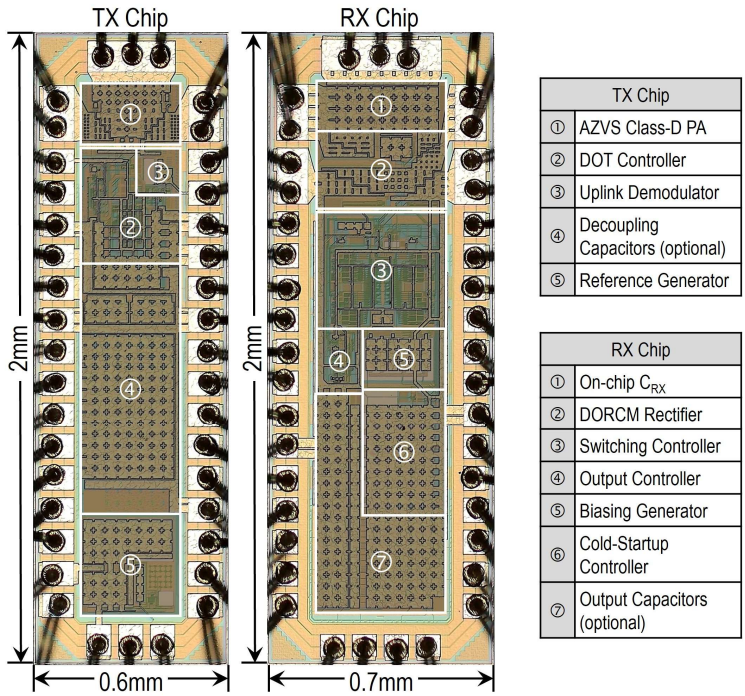
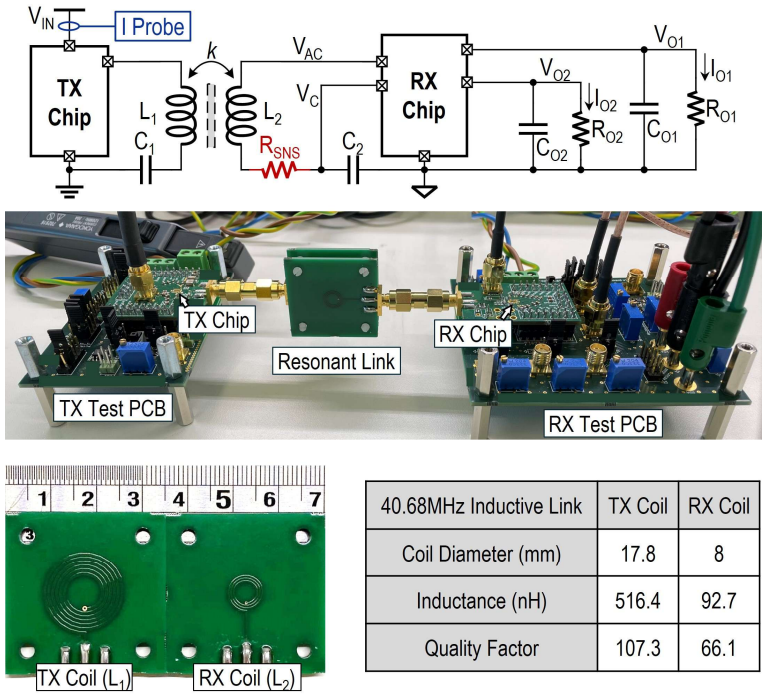


Figure 5.42 Chip micrographs.



40.68MHz Inductive Link	TX Coil	RX Coil
Coil Diameter (mm)	17.8	8
Inductance (nH)	516.4	92.7
Quality Factor	107.3	66.1

Figure 5.43 Measurement setup.

Figure 5.44 shows the measured steady-state waveform under RX load currents I_{O1} = 8mA, I_{O2} = 12mA, with a TX supply voltage of V_{IN} = 3.3V. D_{COIL} is set at 5.2mm, approximately corresponding to a coupling factor of k = 0.1. The output voltages V_{O1} and V_{O2} are regulated at 2V and 1.2V, respectively. The RX alternates between V_{O1}-charging mode (MD_1), V_{O2}-charging mode (MD_2), and LSK uplink mode (MD_{LSK}). Upon demodulating each LSK uplink, the TX transitions from the active (”ON”) state to the idle (”OFF”) state, establishing a stable on/off duty ratio over each complete DOT modulation period (T_{TOT}). The measured result confirms that T_{TOT} stabilizes around 3.6 µs, with the TX-off period (T_{OFF}) equal to 27×T_{RE}.

Figure 5.45 shows the measured steady-state waveform of the V_{AC} signal, which verifies mode transitions at the RX. Notably, immediately after exiting MD_{LSK} and entering MD_1, the RX enables a few additional charging phases to transfer the residual resonant energy in the L_1–C_1 tank to V_{O1}, even after the TX has turned off.

Figure 5.46 shows the measured RX steady-state waveform with key voltage signals in the power path. As shown in Figure 5.46(a), the RX exhibits smooth switching behavior when the TX turns on, owing to the RCM nature in which charging phases occur only when the resonant energy reaches a certain threshold. Figure 5.46(b) further confirms a seamless RX mode transition from MD_1 to MD_2, enabled by the separated V_{O1}-path and V_{O2}-path control loops in the DCDLs. The small ripples on the V_{C2} amplitudes indicate that the DCDLs are dynamically adjusting to track the optimal switching timing.

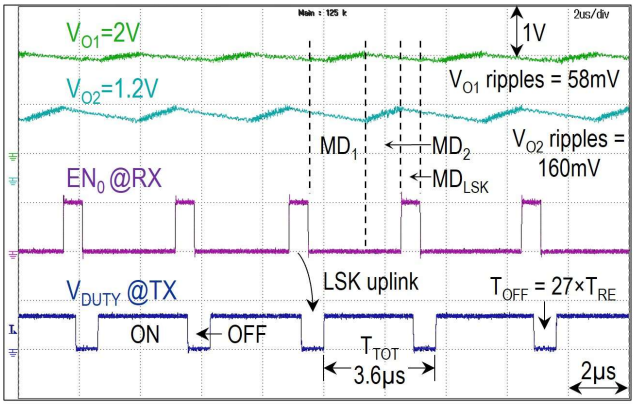


Figure 5.44 Measured steady-state waveform at I_{O1} = 8mA, I_{O2} = 12mA, V_{IN} = 3.3V, and D_{COIL} = 5.2mm.

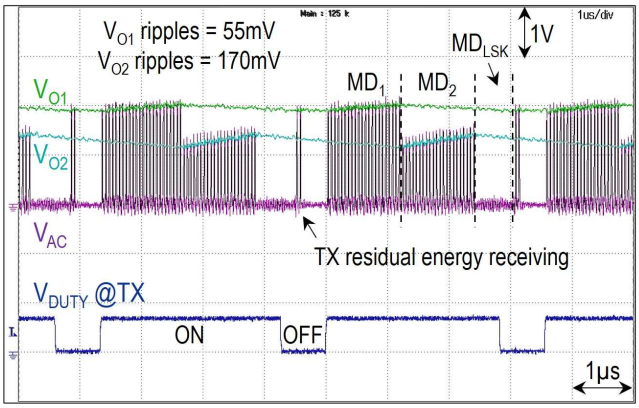


Figure 5.45 Measured steady-state V_{AC} waveform at I_{O1} = 8mA, I_{O2} = 12mA, V_{IN} = 3.3V, and D_{COIL} = 5.2mm.

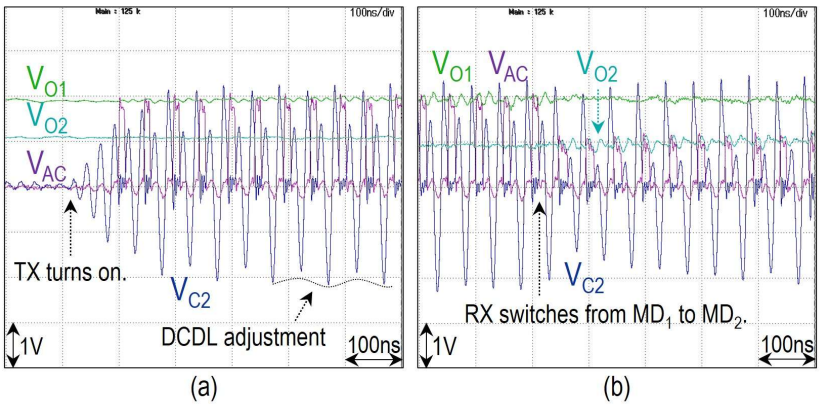


Figure 5.46 Measured steady-state waveforms at the RX. (a) In MD_1. (b) Switching from MD_1 to MD_2.

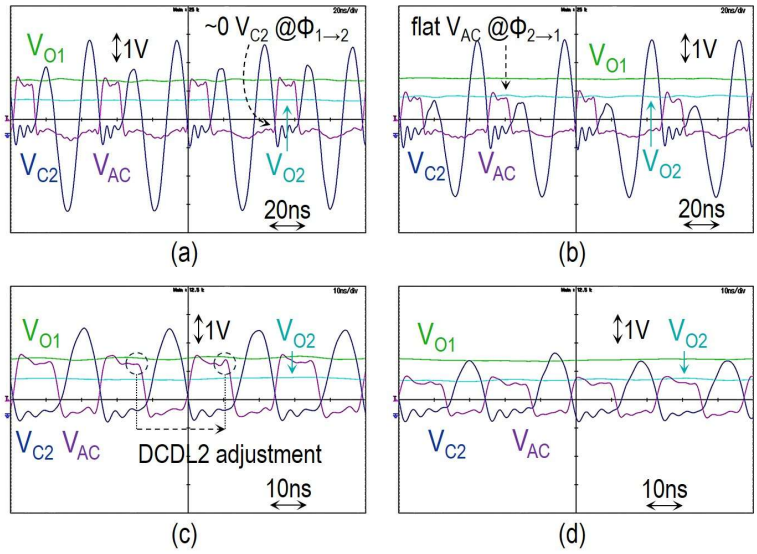


Figure 5.47 Measured zoom-in steady-state waveforms at the RX. (a) MP-Φ_1 case in MD_1. (b) MP-Φ_1 case in MD_2. (c) SP-Φ_1 case in MD_1. (d) SP-Φ_1 case in MD_2.

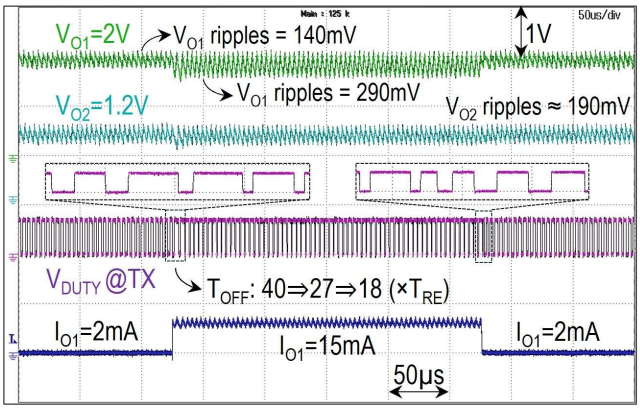


Figure 5.48 Measured load-transient waveform at I_{O2} = 8mA, V_{IN} = 3.3V, and D_{COIL} = 5.2mm.

Figure 5.47(a) and (b) present the measured zoom-in steady-state waveforms during V_{O1} and V_{O2} charging, respectively, at D_{COIL} = 5.2mm, where the RX operates in MP-Φ_1 mode. Figure 5.47(c) and (d) show corresponding measurements at D_{COIL} = 2.5mm (approximately k = 0.2), where the RX operates in SP-Φ_1 mode. In both MP-Φ_1 and SP-Φ_1 scenarios, the phase transition from Φ_1 to Φ_2 (or Φ_3) occurs when V_{C2} is near zero, indicating near zero-voltage turn-on of M_{N2}. Likewise, V_{AC} exhibits only minor voltage surges during the Φ_2 (or Φ_3) to Φ_1 transition, demonstrating near zero-voltage turn-off of M_{P1} (or M_{P2}), thanks to the proposed switching control strategy.

Figure 5.48 shows the measured load-transient waveform at V_{O1} with I_{O2} = 8mA, V_{IN} = 3.3V, and D_{COIL} = 5.2mm. When I_{O1} transitions from 2mA to 15mA (a 7.5× step), the ripple on V_{O1} increases due to the heavier load. T_{OFF} decreases from 40×T_{RE} to 18×T_{RE} to maintain a constant T_{TOT} and mitigate the load regulation performance.

Larger output capacitors can be used to further suppress the voltage ripple. Though V_{O2} shows a slight undershoot caused by the momentarily prolonged T_{TOT} during the transient, it maintains nearly constant ripple before and after the event, owing to the relatively constant T_{TOT} enabled by the DOT modulation. Upon a heavy-to-light load transition, T_{OFF} increases back from $18\times T_{RE}$ to $40\times T_{RE}$. Due to immediate mode switching at the RX, cross-regulation on V_{O2} is unnoticeable. The load-transient behavior observed at V_{O2} is similarly well-regulated.

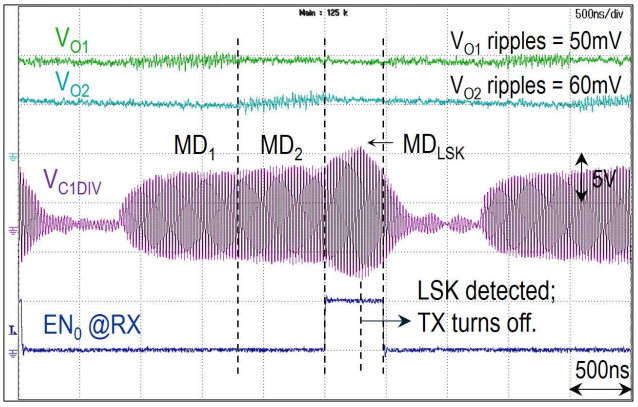


Figure 5.49 Measured LSK modem waveform at D_{COIL} = 5.2mm.

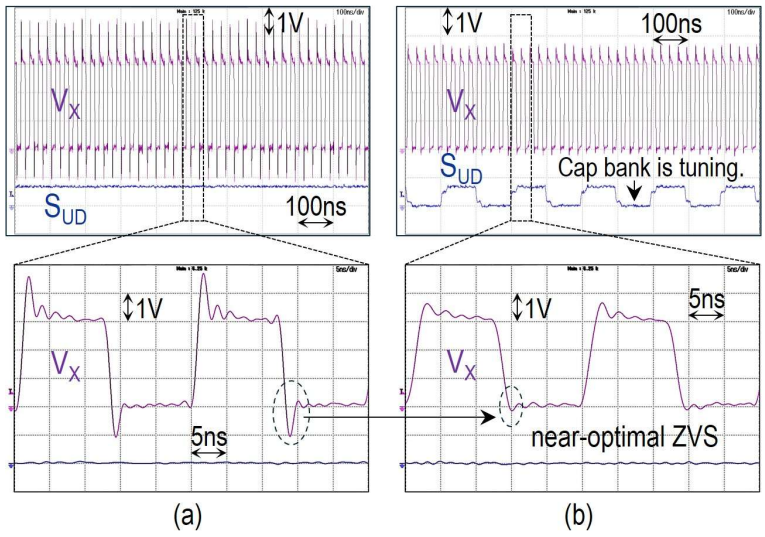


Figure 5.50 Measured TX switching waveforms with the capacitor bank and AZVS controller (a) disabled and (b) enabled.

Figure 5.49 shows the measured LSK uplink modem waveform at D_{COIL} = 5.2mm. When the RX enters MD_{LSK}, the TX observes an increase in the amplitude of V_{C1} as well as V_{C1DIV}, enabling successful demodulation of the uplink signal.

The measured TX switching waveforms with the capacitor bank and AZVS

controller disabled and enabled are shown in Figure 5.50(a) and (b), respectively. When the capacitor bank and AZVS control are enabled, the capacitance at node V_X is finely tuned, enabling nearly zero-voltage switching of both M_{PTX} and M_{NTX} without noticeable body-diode conduction and voltage spikes.

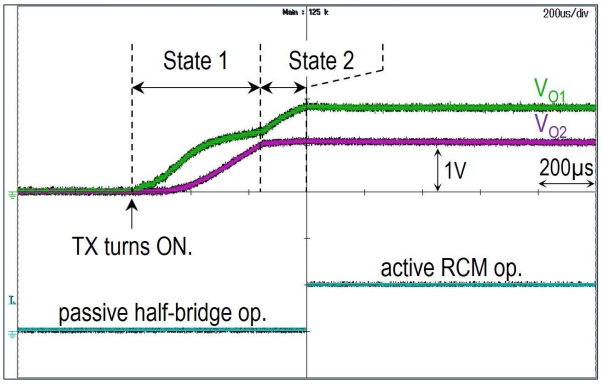


Figure 5.51 Measured RX cold-startup waveform.

Figure 5.51 shows the measured RX cold-startup waveform. During the half-bridge operation based on diode connection, the two subsequent states are observed. Once State 2 concludes, the RX transitions into active RCM operation.

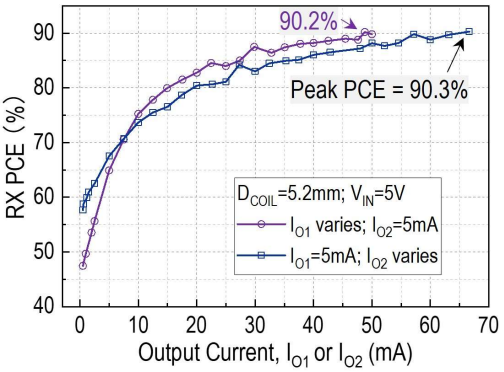


Figure 5.52 Measured power conversion efficiency at the RX.

Figure 5.52 shows the measured power conversion efficiency (PCE) at the RX, with D_{COIL} = 5.2mm and V_{IN} = 5V. The RX input power was measured using the shunt resistor R_{SNS} with a resistance of 3.5Ω. A 2-GHz bandwidth differential probe (PBD2000) monitors the voltage across R_{SNS} using a 4-wire Kelvin connection on the test PCB. In both I_{O1} = 5mA and I_{O2} = 5mA cases, the RX demonstrates similar PCE profiles, confirming soft-switching behavior in both the V_{O1} and V_{O2} charging paths. A peak PCE of 90.3% is achieved at I_{O1} = 5mA and I_{O2} = 67mA, corresponding to a total output power of 90.4mW.

Figure 5.53 presents the measured end-to-end (E2E) power efficiency from the TX input to the RX outputs, in which R_{SNS} is short-circuited. To reflect practical coupling

scenarios in biomedical implants, the E2E efficiency was measured under three representative D_{COIL}: 2.5mm, 5.2mm, and 10mm, corresponding to k of 0.2, 0.1, and 0.04, respectively. Measurements are performed under two operating modes: global-DOT-modulation mode and RX-regulation-only mode. The global-DOT-modulation mode represents the normal operation where the TX is dynamically modulated based on feedback. In contrast, the RX-regulation-only mode keeps the TX continuously on, with the RX periodically entering MD_{LSK} to regulate V_{O1} and V_{O2}.

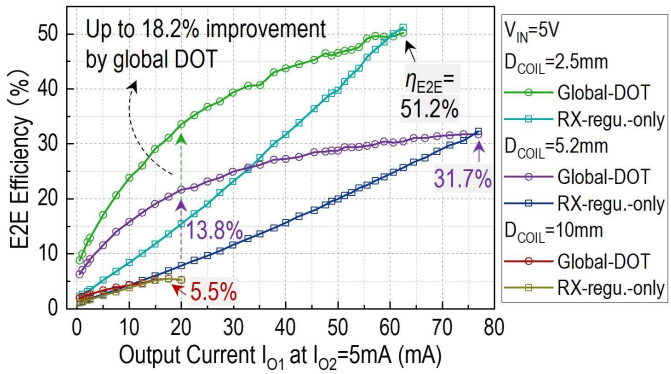


Figure 5.53 Measured end-to-end (E2E) power efficiency.

In D_{COIL} = 10mm case, the peak E2E efficiency is limited to 5.5%, and the maximum output power reaches only 46mW due to the low link efficiency. As D_{COIL} decreases to 5.2mm, the operable load range significantly expands, and the system achieves a peak PCE of 31.7% at a maximum output power of 149.7mW. Under this condition, enabling global DOT modulation yields up to a 13.8% improvement in E2E efficiency. When D_{COIL} becomes 2.5mm, the system achieves a peak E2E efficiency of 51.2% at 130mW output power. With global DOT modulation, the E2E efficiency improves by up to 18.2%, which, at I_{O1} = 20mA, translates to a 2.2× reduction in TX input power.

It is worth noting that the power results were measured *ex vivo* using PCB-based coils in air. For practical *in vivo* applications, compliance with applicable specific absorption rate (SAR) limits must be ensured. Standardized tissue-equivalent measurements are recommended to validate the power results before deployment. In addition, angular misalignment between the TX and RX coils has a similar impact on the coupling coefficient as increasing coil separation.

5.2.5 Comparison

Table 5.4 benchmarks this work against state-of-the-art biomedical WPT system designs. By operating at a power carrier frequency of 40.68MHz, the proposed system achieves an 8-mm diameter RX coil without significantly sacrificing output power and RX PCE. This corresponds to an approximately six-fold reduction in form factor (planar area) compared with typical RX coil diameters of 20 mm.

The higher maximum output power in this work is attributed to two factors: (1) the TX is driven with a relatively higher input voltage, and (2) the RCM rectifier at the RX, when configured to operate the charging phase in every resonant period, can deliver power comparable to that of FBR and VD rectifiers under strong coupling, as discussed in Section 5.1.

Though small output capacitors are used, the proposed global DOT modulation regulates the output voltage ripple. Increasing the output capacitance can further reduce the ripple.

Compared with low-frequency designs, the proposed system exhibits a lower peak E2E efficiency due to: (1) the smaller coupling factor at which the peak was measured, dictated by the small RX coil, (2) increased TX and RX coil losses from the skin effect at higher switching frequencies, and (3) additional losses from the power switches in the Class-D PA.

Compared with other 40.68-MHz designs, though [5.20] employs a smaller 4mm diameter RX coil, its coil separation is limited to 2mm; in contrast, the proposed system demonstrates strong coupling adaptability, enabled by the RX RCM topology. The proposed system also optimizes switching operation at both TX and RX. Furthermore, it achieves a high level of integration, with global power modulation realized through a fully integrated data uplink channel.

Table 5.4 Comparison to state-of-the-art RCM rectifiers.

	JSSC'18[5.23]	JSSC'22[5.24]	TCAS-I'23[5.9]	JSSC'24[5.32]	JSSC'24[5.13]	JSSC'24[5.20]	ISSCC'24[5.18]	**This work**
Carrier Frequency	13.56MHz	6.78MHz	6.78MHz	13.56MHz	13.56MHz	40.68MHz	40.68MHz	**40.68MHz**
Coil Diameter	RX 20mm TX 25.2mm	RX 25mm TX 32mm	RX 23mm TX 41mm	RX 30mm TX 35mm	RX 20mm TX 30mm	RX 4mm TX 16.5mm	RX 24mm TX 32mm	**RX 8mm** **TX 17.8mm**
Chip Integration	TX & RX	TX & RX	TX & RX	TX & RX	TX & RX	RX only	RX only	**TX & RX**
Technology	65nm CMOS	180nm CMOS	180nm CMOS	65nm CMOS	180nm CMOS	65nm CMOS	180nm BCD	**180nm BCD**
Chip Area	RX 1.44mm^2 TX 1.44mm^2	RX 1.3mm^2 TX 0.98mm^2	RX 2.7mm^2 TX 0.98mm^2	RX 0.15mm$^{2\#}$ TX 0.15mm$^{2\#}$	RX 1.65mm^2 TX 1.53mm^2	RX 0.74mm^2 TX external	RX 1.6mm^2 TX external	**RX 1.4mm^2** **TX 1.2mm^2**
Off-Chip Components	C_O (1μF), and a LSK sensing coil	C_O (8μF)	2 C_O	C_{O1} (1μF), C_{O2} (1μF), a LSK coil and a detector	2 C_O (330nF each)	C_{O1} (220nF), C_{O2} (470nF)	C_{O1} (1μF), C_{O2} (1μF)	**C_{O1} (100nF), C_{O2} (100nF)**
TX Topology	Class-D PA	Class-D PA	Class-D PA	Reconfigurable Class-D PA	Reconfigurable Class-D PA	OPA 2677	Class-E PA	**Adaptive-ZVS Class-D PA**
RX Topology	Full-Bridge Regulating Rectifier	Full-Bridge Regulating Rectifier	DO RCM Regulating Rectifier	DO Full-Bridge Regulating Rectifier	VM/RCM Regulating Rectifier	DO Full-Bridge Regulating Rectifier	Full-Bridge Rectifiers + LDOs	**DO RCM Regulating Rectifier**
Global Regulation	Constant Off-Time Control	Hysteretic Control	"Record & Replay" Control	PWM Control	Digital PWM Control	No	No	**Dynamic Off-Time Control**
TX Input Voltage	2.5V	1.8V	1.8V	1.2V	1.8V	N/R	N/R	**3.3V – 5V**

Table 5.4 (continued)

	JSSC'18[5.23]	JSSC'22[5.24]	TCAS-I'23[5.9]	JSSC'24[5.32]	JSSC'24[5.13]	JSSC'24[5.20]	ISSCC'24[5.18]	**This work**
RX Output Voltages (# of outputs)	1.2 – 2.5V (1)	1.2 – 1.8V (1)	3V; 1.8V (2)	2.5V; 1.2V (2)	1.8V (1)	2.2V; 1.1V (2)	4V; 2V (2)	**2V; 1.2V (2)**
Output Voltage Ripple (I_{OUT})	50mV (10mA)	75mV (hysteretic)	50mV@V_{O1}(1mA); 50mV@V_{O2}(1mA)	N/R	100mV (30mA)	190mV@V_{O1}(25mA); 90mV@V_{O2}(5mA)	N/R	**58mV@V_{O1}(8mA); 160mV@V_{O2}(12mA)**
RX Cold-Startup	No	No	Yes	Yes	No	Yes	Yes	**Yes**
Coil Separation Distance (D)	0.2 – 1.1cm	0.65cm	1 – 2cm	0.6 – 1.5cm	0.5 – 7cm	0.2cm	1.2cm (k=0.115)	**0.25 – 1cm (k=0.04 – 0.2)**
Peak E2E Efficiency	70.6% (@D=0.6cm)	61.9% (@D=0.65cm)	31.3% (@D=1cm)	62.7% (@D=0.6cm)	72.3% (@D=0.5cm)	N/R	31.4% (@D=1.2cm)	**51.2% (@D=0.25cm)**
Peak RX PCE	N/R	N/R	85.1%	88%	92.7%	90.1%	87.4%**	**90.3%**
Maximum P_{OUT}	49.4mW	32mW	7mW	20mW	80.5mW	60.5mW	110mW	**149.7mW**

N/R: Not reported; [#]area excluding pads; **simulation result.

5.3 Concluding Remarks

This chapter investigated resonant-current-mode (RCM) techniques through comparative analysis, circuit design, implementation, fabrication, and experimental validation.

The first contribution is a three-phase regulating RCM rectifier that overcomes key limitations of conventional parallel-LC and series-LC RCM topologies, including excessive voltage swing and residual charging, by introducing a bypass-capacitor-based residual-free charging mechanism. The design further enables power-efficient in-situ output regulation through a dedicated freewheeling phase. It achieves over-200-mW maximum output power and a peak PCE of 94.5%.

The second contribution is a dual-output WPT system built upon the proposed three-phase RCM RX. Operating at 40.68 MHz, the system enables an 8-mm-diameter RX coil while delivering state-of-the-art output power and RX efficiency. It integrates circuit techniques including global dynamic-off-time power modulation, adaptive ZVS Class-D transmitter, and zero-crossing-based RX switching control, optimized for high-frequency operations.

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Chapter 6 Conclusions and Outlook

This thesis has described the development of interface integrated circuits for inductive resonant wireless power transfer (WPT). This chapter summarizes the main findings, provides a comprehensive comparison between the proposed and state-of-the-art designs, and concludes with a discussion of future research directions.

6.1 Main Findings

The main findings of this thesis are:

- Among various WPT technologies, inductive resonant coupling is best suited to short-to-medium-range implantable medical devices (IMDs) because of its high efficiency and robustness to spatial misalignment and distance variations. (Chapter 1)
- The resonance configuration at the receiver (RX) side, series or parallel, strongly affects the link efficiency and the power delivered to the RX under specific load conditions. As a rule of thumb, series resonance performs better for heavy loads, whereas parallel resonance is more suitable for light loads. (Chapter 2)
- In the presence of coupling variations, non-linear control schemes (e.g., hysteresis-based), either locally at the receiver (RX) or globally across the WPT system, provide robust output regulation while balancing steady-state accuracy and transient response. In contrast, to maintain stability, analog linear control loops must slow down as the coupling varies, leading to suboptimal performance. (Chapter 2)
- The voltage-doubler topology largely extends the operating coupling range compared with the conventional full-bridge rectifier, relaxing design constraints on other design parameters such as the RX coil size for comparable performance. (Chapter 3)
- The dual-output voltage doubler (DOVD) further exploits the voltage-doubler topology by regulating two independent outputs using only two power transistors. This enables the co-optimization of power efficiency, voltage conversion ratio (VCR), on-chip power density, and multi-output regulation. (Chapter 3)
- Combining voltage-mode (VM) and resonant-current-mode (RCM) operation improves RX input sensitivity and increases the transfer distance by up to 50%. This requires only one additional on-chip power switch with negligible extra

efficiency loss, at the cost of higher control complexity. (Chapter 4)

- Global digital pulse-width modulation (PWM) improves end-to-end efficiency compared to hysteretic control by enabling full on/off TX operation, though its load regulation is suboptimal. A lookup-table-based digital implementation improves load-transient response relative to conventional analog PWM, at the expense of larger silicon area. (Chapter 4)
- VM rectifiers excel under stable coupling, large coils, and low-VCR conditions, offering robust monophasic operation and high output quality. In contrast, RCM rectifiers perform reliably over a wider VCR range, especially at high VCR, thanks to their load-insensitive two-phase behavior, making them ideal for variable coupling and miniaturized coils. (Chapter 5)
- Increasing the power carrier frequency from 6.78/13.56 MHz to 40.68 MHz enables either improved link efficiency or significant coil miniaturization. Although additional high-frequency losses (e.g., skin effect) occur, they are outweighed by the fundamental performance gains offered by higher-frequency operation. (Chapter 5)
- Global dynamic-off-time modulation trades off output regulation against design complexity, chip area, and power consumption compared to digital-PWM. (Chapter 5)

6.2 Comparison with State-of-the-Art

6.2.1 RX Designs

Figure 6.1 compares the peak power conversion efficiency (PCE) and maximum output power of state-of-the-art RX designs with the RX designs presented in this thesis for IMD-oriented WPT [6.1]–[6.13]. In general, the RX in a WPT system should deliver sufficient power to loads while maintaining the highest possible PCE. Notably, no clear trade-off is observed between PCE and output power for RX designs.

The proposed VM RX designs (Chapter 3) and the hybrid voltage-/current-mode (V/CM) RX design (Chapter 4) achieve comparable peak PCE and maximum output power to the best VM designs reported in the literature. This performance is achieved through simplified power stages with a minimal number of power transistors and advanced switching control techniques, such as adaptive delay compensation. The proposed RCM RX design (Chapter 5) achieves the highest peak PCE and maximum output power among all VM, V/CM, and RCM rectifiers, benefiting from its three-phase topology that effectively overcomes the limitations of prior RCM architectures.

It should be noted that the achievable output power level also depends on TX topology, TX input voltage, and coupling conditions; a more comprehensive system-level benchmarking will be discussed in Section 6.2.2.

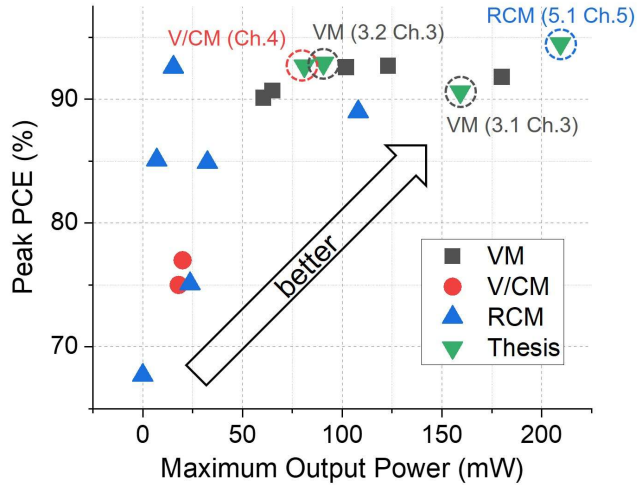

Figure 6.1 Peak PCE vs. maximum output power of RX designs [6.1]-[6.13].

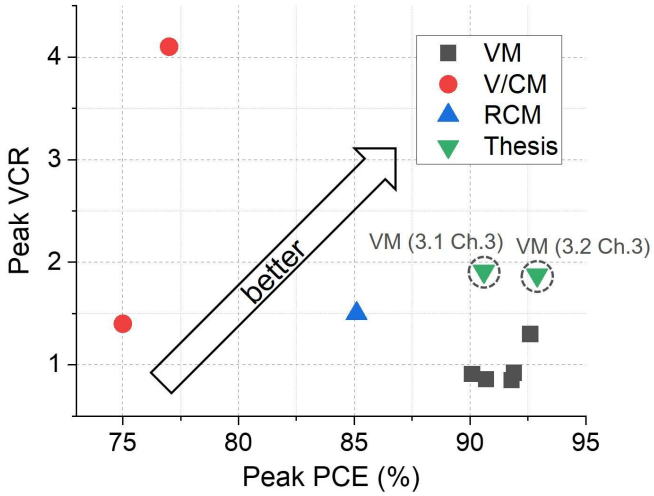

Figure 6.2 Peak VCR vs. peak PCE of RX designs. The VCR represents the voltage conversion ratio provided by the circuit topology [6.1][6.3][6.4][6.5][6.8][6.9][6.12][6.14].

Figure 6.2 compares the peak VCR and peak PCE among various RX designs [6.1][6.3][6.4][6.5][6.8][6.9][6.12][6.14]. For the proposed designs, only two VM designs (Chapter 3) are plotted, as their VCRs are explicitly defined by the circuit topologies. In contrast, the hybrid V/CM and RCM designs prioritize in-situ output regulation, and their RCM operation does not report a quantitative VCR. The proposed VM designs retain the inherently high PCE characteristic of the VM class while improving the VCR to nearly 2.

6.2.2 WPT System Designs

Figure 6.3 benchmarks WPT system designs [6.15]–[6.23] that report both TX and RX chip designs, using two key performance metrics: the power-efficiency figure of merit (FoM) [6.24] and the normalized maximum distance between TX and RX coils [6.25], which are defined respectively as

$$FoM = \frac{{\eta_{E2E}}^2 \cdot PDL}{{V_{IN}}^2} \tag{6.1}$$

$$\text{normalized maximum coil distance} = \frac{D_{MAX}}{\sqrt{D_{TX} \cdot D_{RX}}} \tag{6.2}$$

where η_{E2E} represents the peak end-to-end (E2E) efficiency, PDL is the maximum delivered output power, V_{IN} denotes the DC input voltage at the TX side, D_{MAX} is the maximum measured operable coil distance, D_{TX} and D_{RX} are the TX and RX coil outer diameters, respectively.

The proposed hybrid V/CM system (Chapter 4) achieves both the highest FoM and normalized maximum coil distance among the compared designs, owing to the use of the V/CM RX technique and the global PWM power control scheme.

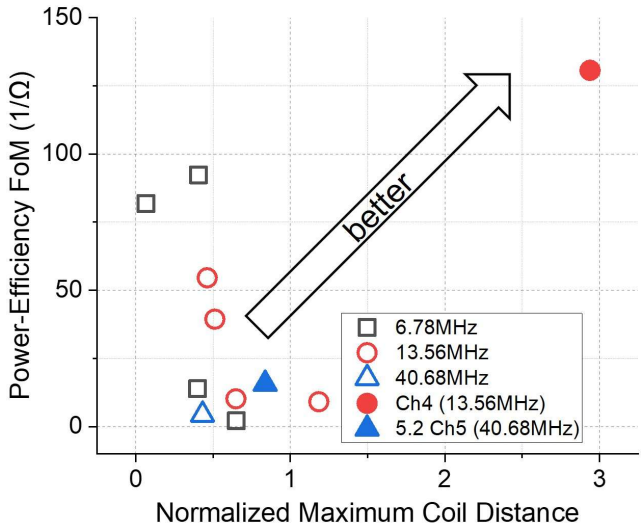

Figure 6.3 Power-efficiency FoM vs. normalized maximum coil distance of system designs [6.15]-[6.23].

Figure 6.4 compares the power-efficiency FoM and RX coil diameter across different WPT system designs [6.15]–[6.23]. The proposed RCM system (Chapter 5) features the smallest RX coil of all compared designs. Its relatively lower FoM results from a reduced η_{E2E} caused by high-frequency losses, primarily occurring at the TX side. Nevertheless, the system maintains a high peak PCE over 90% at the RX side and

can deliver up to 150-mW output power, meeting the requirements of high-power IMD applications.

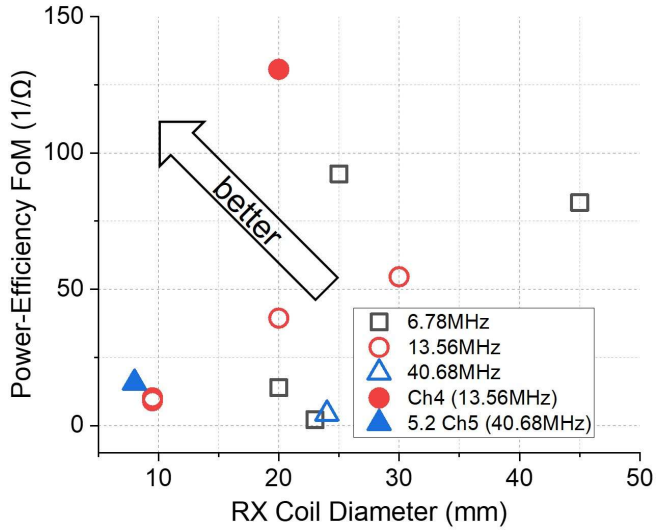

Figure 6.4 Power-efficiency FoM vs. RX coil diameter of system designs [6.15]-[6.23].

Notably, as function-driven power management units, the proposed RX and WPT systems distinguish themselves not only through performance metrics but also by offering unique or enhanced functionalities, for example, the dual-output voltage doubler presented in Chapter 3.

6.3 Future Research Directions

IMDs are rapidly evolving, driving increasing demand for advanced WPT technologies. Accordingly, several research directions related to this thesis remain open for further exploration, as outlined below.

6.3.1 Simultaneous Wireless Power and Data Transfer (WPDT)

IMDs require not only efficient wireless power delivery but also reliable wireless data communication. Conventional wireless communication technologies, such as Bluetooth and ultra-wideband (UWB), offer high data rates ranging from tens of megabits per second (Mb/s) to sub-gigabit per second (Gb/s). However, they demand considerable power consumption and additional hardware components, which increase the IMD's form factor and power burden.

Transmitting data through the existing wireless power link presents a promising alternative, as it reduces component count and minimizes system size. Nevertheless, current simultaneous wireless power and data transfer (WPDT) systems still struggle to meet both the stringent power and data requirements of IMDs simultaneously. Thus, a

key open challenge lies in developing methods to efficiently transmit data through the power link without compromising power delivery performance.

6.3.2 WPT Network Powering Multiple IMDs

Looking ahead, as IMD applications evolve toward deeper implantation depths, the use of large, monolithic implants is expected to give way to distributed networks of miniature implants. Designing a dedicated TX for each RX is impractical in such scenarios, highlighting a key open challenge: developing single-TX, multi-RX WPT systems. A critical question arises: how can the TX dynamically allocate and regulate power delivery among multiple RX nodes while maintaining high overall efficiency?

Moreover, simultaneous WPDT in these single-TX, multi-RX configurations is particularly promising, as it would enable coordinated power distribution and real-time communication among distributed implants.

6.3.3 Maximum Efficiency/Power Point Tracking (MEPT/MPPT)

In a WPT system, the TX serves as the power source, while the RX acts as the power load, as discussed in Chapter 2. This source-load relationship influences both the power delivered to the load and the end-to-end (E2E) efficiency [6.26]. Therefore, if a WPT system can achieve maximum power point tracking (MPPT) and/or maximum efficiency point tracking (MEPT), the design constraints on other parameters can be relaxed and overall system performance can be enhanced. For instance, with effective MPPT, a lower TX input voltage or smaller RX coil could still transfer sufficient power, while MEPT can extend the lifetime of battery-powered TX devices by minimizing the energy extraction from source.

However, conventional MPPT/MEPT implementations, mostly discrete circuit implementations, typically require complex control strategies, additional circuit components, and cascaded power stages (e.g., DC-DC), which hinder their applicability in compact IMDs. This raises an important open question: how can MPPT/MEPT be achieved in IMD-oriented WPT systems, based on integrated circuits, using minimal additional circuitry while preserving high efficiency and stability?

6.3.4 From Miniaturization to Full Integration

Based on this thesis, it is observed that most state-of-the-art WPT systems still rely on bulky off-chip components to build the wireless link. Although the work presented in Chapter 5 successfully scales the RX coil size down to the millimeter range, it remains unsuitable for many IMD applications that demand even smaller form factors. To further reduce the size of RXs without fundamental performance loss, it may be necessary to increase the operating frequency into the gigahertz (GHz) range. The key

challenge lies in developing high-frequency WPT interface circuits that can maintain strong figures of merit despite frequency-dependent losses and parasitic effects.

Moreover, the inductive resonant coupling method offers a distinct advantage: its coils can be monolithically integrated on chip. Fully integrated WPT RXs would drastically reduce the IMD footprint. Advancing such fully integrated RX solutions, particularly those compatible with the aforementioned research directions (e.g., multi-RX networks, simultaneous power and data transfer, and MPPT/MEPT), represents a highly promising avenue for future exploration.

6.4 Concluding Remarks

This thesis has presented the development of inductive resonant wireless power transfer (WPT) interface circuits for implantable medical devices (IMDs). The research introduced several receiver (RX) architectures optimized for high efficiency, coupling adaptability, output regulation, etc. Voltage-mode (VM) RX designs based on the voltage doubler structure achieved improved voltage conversion ratios and multi-output regulation. A voltage-/current-mode (V/CM) RX further enhanced low-power receiving capability under weak coupling conditions, while a resonant-current-mode (RCM) RX was developed for miniaturized coils. At the system level, global power modulation techniques were also advanced to improve end-to-end efficiency without significantly compromising output regulation performance, which includes digital pulse-width modulation control and dynamic-off-time control.

Despite these advancements, several research directions remain open for IMD-oriented WPT interface circuits, and further refinement is needed before the proposed designs can be fully translated into practical healthcare applications. For example, specific absorption rate (SAR) limits must be ensured through standardized tissue-equivalent measurements. Beyond their immediate scope, the analog and mixed-signal circuit techniques presented in this thesis, such as high-speed continuous-time comparators, controllable delay lines, and signal shifters, may also find applications in energy harvesting systems, battery management systems, and AC–DC/DC–DC power converter implementations.

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Summary

This thesis presents the design of integrated interface circuits for inductive resonant wireless power transfer (WPT) systems, targeting implantable medical devices (IMDs). IMDs require compact, high-efficiency, and robust wireless power solutions capable of adapting to link and load variations. This thesis systematically develops three receiver and system architectures: voltage-mode (VM), hybrid voltage-/current-mode (V/CM), and resonant-current-mode (RCM), to improve power conversion efficiency (PCE), voltage conversion ratio (VCR), and adaptability over state-of-the-art designs.

Chapter 1 introduces the motivation and background of WPT for biomedical applications. Various WPT modalities are compared in terms of power level, efficiency, penetration depth, integration feasibility, etc. Among them, inductive resonant coupling is identified as the most suitable for short-to-medium-range high-power IMDs, owing to its high efficiency and near-field property. The chapter also outlines major design challenges in integrated inductive resonant WPT interfaces, including high-efficiency power delivery, multi-rail regulation, miniaturization, and adaptability under varying coupling conditions.

Chapter 2 establishes comprehensive review of inductive-resonant WPT systems, which includes inductive link foundations, transmitter (TX) and receiver (RX) interface circuit designs, and system-level techniques. The chapter begins with a reflected load theory bridging the RX and TX circuits, where link efficiency and power delivered to RX are also analyzed. The design considerations of RX circuits are then discussed in depth. The RX circuits are categorized into two types: voltage-mode (VM) bridge rectifiers and resonant-current-mode (RCM) rectifiers. In VM designs, the following techniques are analyzed: 1) active diode and delay compensation, 2) in-situ output voltage regulation, and 3) single-stage multi-output generation. On the TX side, switching-mode power amplifiers (PAs) such as Class-D and Class-E are examined. Impedance-matching and zero-voltage switching (ZVS) techniques are introduced. The chapter also introduces through-power-link data backscattering based on load-shift keying (LSK) and global modulation techniques such as constant-off-time and hysteresis control for end-to-end (E2E) efficiency enhancement.

Chapter 3 presents VM RX designs based on voltage doubler. The first design demonstrates the concept of a single-stage regulating voltage doubler, achieving doubled VCR compared with full-bridge rectifiers. The second extends this concept to a dual-output voltage doubler (DOVD), realizing two independently regulated outputs using only two power transistors and achieving 93% peak power conversion efficiency (PCE).

Chapter 4 introduces a coupling-adaptive closed-loop WPT system design using a

voltage-/current-mode (V/CM) RX. The V/CM RX combines the advantages of VM and RCM operations. Under weak coupling conditions, it autonomously switches from VM to RCM to maintain output regulation. The mode-switching behavior is also theoretically analyzed. On the TX side, the presented system integrates a global digital pulse-width modulation (PWM) scheme with a three-mode Class-D power amplifier to improve end-to-end (E2E) power efficiency and widen power adjustment range. It achieves up to 50% WPT range extension compared with VM-only systems, 72.3% peak E2E efficiency, and up to 40% E2E efficiency improvement compared with open-loop systems.

Chapter 5 presents RX and system designs based on RCM techniques for highly miniaturized IMDs. The first design introduces a three-phase regulating RCM rectifier employing a bypass-capacitor-based residual-free charging mechanism to eliminate resonant energy residual loss, achieving 94.5% peak PCE. The second integrates this topology into a 40.68-MHz dual-output WPT system, achieving an 8-mm-diameter RX coil, representing a 6× miniaturization improvement over prior art while sustaining >90% peak PCE on RX. A dynamic-off-time global modulation and adaptive-ZVS Class-D TX further enhance E2E efficiency.

Chapter 6 summarizes the main findings and benchmarks the proposed designs against state-of-the-art RX and WPT systems. It shows that the proposed topologies achieve superior performance across multiple dimensions: efficiency, output regulation, coupling/loading adaptability, and form factor. Finally, several promising research directions are outlined, including simultaneous wireless power and data transfer (WPDT), single-TX multi-RX power distribution, maximum efficiency/power point tracking (MEPT/MPPT), and fully integrated WPT interfaces for millimeter-scale IMDs.

Samenvatting

Dit proefschrift presenteert het ontwerp van geïntegreerde interfacecircuits voor inductief-resonante draadloze energieoverdrachtsystemen (wireless power transfer, WPT), gericht op implanteerbare medische apparaten (implantable medical devices, IMDs). IMDs vereisen compacte, efficiënte en robuuste oplossingen voor draadloze energieoverdracht, die zich kunnen aanpassen aan variaties in koppeling en belasting. In dit proefschrift worden drie ontvanger- en systeemarchitecturen systematisch ontwikkeld: spanningsmodus (voltage-mode, VM), hybride spannings-/stroommodus (voltage-/current-mode, V/CM) en resonante-stroommodus (resonant-current-mode, RCM), met als doel de vermogensconversie-efficiëntie (power conversion efficiency, PCE), spanningsconversieverhouding (voltage conversion ratio, VCR) en aanpasbaarheid te verbeteren ten opzichte van de stand van de techniek.

Hoofdstuk 1 introduceert de motivatie en achtergrond van WPT voor biomedische toepassingen. Verschillende WPT-modaliteiten worden vergeleken op basis van onder meer vermogensniveau, efficiëntie, penetratiediepte en integratiemogelijkheden. Hieruit blijkt dat inductief-resonante koppeling het meest geschikt is voor IMDs met een hoog vermogensniveau en een korte tot middellange overdrachtsafstand, vanwege de hoge efficiëntie en het near-field karakter. Daarnaast worden in dit hoofdstuk de belangrijkste ontwerpuitdagingen van geïntegreerde inductief-resonante WPT-interfaces uiteengezet, waaronder hoogefficiënte vermogensoverdracht, multi-rail spanningsregeling, miniaturisatie en robuuste werking onder variërende koppelingscondities.

Hoofdstuk 2 geeft een uitgebreid overzicht van inductief-resonante WPT-systemen, inclusief de fundamenten van inductieve koppeling, interfacecircuits aan de zenderzijde (transmitter, TX) en ontvangerzijde (receiver, RX), en systeemniveau-technieken. Het hoofdstuk begint met een theorie van gereflecteerde belasting, die de RX- en TX-circuits met elkaar verbindt, waarbij ook de linkefficiëntie en het aan de RX geleverde vermogen worden geanalyseerd. Vervolgens worden de ontwerpoverwegingen van RX-circuits diepgaand besproken. De RX-circuits worden ingedeeld in twee categorieën: spanningsmodus (VM) brugrectifiers en resonante-stroommodus (RCM) rectifiers. Voor VM-ontwerpen worden de volgende technieken geanalyseerd: (1) actieve diode en delay-compensatie, (2) in-situ uitgangsspanningsregeling en (3) single-stage multi-output generatie. Aan de TX-zijde worden schakelende vermogensversterkers (power amplifiers, PAs), zoals Class-D en Class-E, besproken. Daarnaast worden impedantiematching en zero-voltage switching (ZVS)-technieken geïntroduceerd. Ook behandelt dit hoofdstuk dataterugkoppeling via het vermogenskanaal op basis van load-shift keying (LSK), evenals globale modulatiestrategieën zoals constant-off-time en hysteresisregeling ter verbetering van de end-to-end (E2E) efficiëntie.

Hoofdstuk 3 presenteert VM-RX-ontwerpen gebaseerd op een spanningsverdubbelaar. Het eerste ontwerp demonstreert het concept van een single-stage regelende spanningsverdubbelaar, waarmee een tweemaal hogere VCR wordt bereikt in vergelijking met full-bridge rectifiers. Het tweede ontwerp breidt dit concept uit naar een dual-output spanningsverdubbelaar (dual-output voltage doubler, DOVD), waarmee twee onafhankelijk geregelde uitgangen worden gerealiseerd met slechts twee vermogensschakelaars en een piek-vermogensconversie-efficiëntie van 93%.

Hoofdstuk 4 introduceert een koppeling-adaptief closed-loop WPT-systeem op basis van een spannings-/stroommodusontvanger (V/CM RX). De V/CM RX combineert de voordelen van VM- en RCM-werking. Onder zwakke koppelingscondities schakelt het systeem autonoom van VM naar RCM om de uitgangsspanning gereguleerd te houden. Dit modusschakelgedrag wordt ook theoretisch geanalyseerd. Aan de TX-zijde integreert het gepresenteerde systeem een globaal digitaal pulsbreedtemodulatie (PWM)-schema met een driefasige Class-D vermogensversterker om de E2E-efficiëntie te verbeteren en het vermogensregelbereik te vergroten. Het systeem bereikt een uitbreiding van het WPT-bereik tot 50% ten opzichte van systemen die uitsluitend op VM zijn gebaseerd, een piek-E2E-efficiëntie van 72,3%, en tot 40% verbetering van de E2E-efficiëntie vergeleken met open-loop systemen.

Hoofdstuk 5 presenteert RX- en systeemontwerpen op basis van RCM-technieken voor sterk geminiaturiseerde IMDs. Het eerste ontwerp introduceert een driefasige regelende RCM-rectifier die gebruikmaakt van een bypass-condensator-gebaseerd residual-free charging-mechanisme om restverliezen van resonantie-energie te elimineren, en bereikt een piek-PCE van 94,5%. Het tweede ontwerp integreert deze topologie in een 40,68-MHz dual-output WPT-systeem met een RX-spoel met een diameter van 8 mm, wat neerkomt op een miniaturisatieverbetering van 6× ten opzichte van eerdere ontwerpen, terwijl een piek-PCE van meer dan 90% aan de RX-zijde behouden blijft. Een dynamic-off-time globale modulatie en een adaptieve-ZVS Class-D TX verbeteren de E2E-efficiëntie verder.

Hoofdstuk 6 vat de belangrijkste bevindingen samen en vergelijkt de voorgestelde ontwerpen met de stand van de techniek op het gebied van RX- en WPT-systemen. Hieruit blijkt dat de voorgestelde topologieën superieure prestaties leveren op meerdere dimensies, waaronder efficiëntie, uitgangsregeling, aanpasbaarheid aan koppeling en belasting, en form factor. Tot slot worden verschillende veelbelovende richtingen voor toekomstig onderzoek geschetst, waaronder gelijktijdige draadloze energie- en dataoverdracht (wireless power and data transfer, WPDT), energieverdeling van één TX naar meerdere RX'en, maximum efficiency/power point tracking (MEPT/MPPT), en volledig geïntegreerde WPT-interfaces voor millimeterschaal IMDs.

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List of Publications

Journal Papers

1. **T. Lu**, B. Zhao and S. Du, “A Bipolar Quad-Output Regulating Rectifier with Coil-Reused DC-DC Power Enhancement for Wireless Power Transfer,” invited for publication in *IEEE Journal of Solid-State Circuits* (Special Issue – ISSCC 2026).
2. **T. Lu** and S. Du, "A Three-Phase Regulating Resonant-Current-Mode Rectifier With Bypass-Capacitor Residual-Free Charging for Wireless Power Transfer," in *IEEE Journal of Solid-State Circuits*, vol. 61, no. 5, pp. 2203-2214, May 2026.
3. **T. Lu** and S. Du, "A 40.68-MHz Dual-Output Wireless Power Transfer System for Millimeter-Scale Biomedical Implants," in *IEEE Journal of Solid-State Circuits*, vol. 61, no. 3, pp. 963-976, March 2026.
4. Y. -h. Ou-yang, R. Wijermars, P. Yeon, **T. Lu**, A. Arbabian, W. A. Serdijn, S. Du, and D. G. Muratore, "A 40.68-MHz Fully-Integrated Voltage/Current-Mode Dual-Output PMU for Wireless Neural Implants," in *IEEE Transactions on Biomedical Circuits and Systems*, vol. 20, no. 1, pp. 41-56, Feb. 2026.
5. Y. Wei, X. Yue, **T. Lu**, Z. Chen and S. Du, "A Synchronous Piezoelectric–Electromagnetic Hybrid Energy Harvesting Platform With Coil-Sharing Scheme," in *IEEE Journal of Solid-State Circuits*, vol. 60, no. 12, pp. 4407-4420, Dec. 2025.
6. **T. Lu** and S. Du, "A 92.3%-Efficiency Switching-Mode Dual-Output Regulating Rectifier With Improved Link Adaptability for Wireless Power Transfer," in *IEEE Journal of Solid-State Circuits*, vol. 60, no. 7, pp. 2354-2366, July 2025.
7. **T. Lu** and S. Du, "A Coupling-Adaptive Wireless Power Transfer System With Voltage-/Current-Mode Receiver and Global Digital-PWM Regulation," in *IEEE Journal of Solid-State Circuits*, vol. 59, no. 12, pp. 4175-4187, Dec. 2024.
8. **T. Lu**, K. A. A. Makinwa and S. Du, "A Single-Stage Dual-Output Regulating Voltage Doubler for Wireless Power Transfer," in *IEEE Journal of Solid-State Circuits*, vol. 59, no. 9, pp. 2922-2933, Sept. 2024.
9. **T. Lu**, R. Wang, Z. Tang, Y. Zou, X. Yue, Y. Liang, H. Gong, S. Liu, Z. Chen, X. Liu, J. Jiang, B. Zhao, and S. Du, "A Thermoelectric Energy Harvesting System Assisted by a Piezoelectric Transducer Achieving 10-mV Cold-Startup and 82.7% Peak Efficiency," in *IEEE Transactions on Power Electronics*, vol. 39, no. 5, pp. 6352-6363, May 2024.
10. S. Liu, **T. Lu**, Z. Tang, Z. Chen, J. Jiang, B. Zhao, and S. Du, "A Single-Stage

Three-Mode Reconfigurable Regulating Rectifier for Wireless Power Transfer," in *IEEE Transactions on Power Electronics*, vol. 38, no. 7, pp. 9195-9205, July 2023.

11. **T. Lu** and S. Du, "A Single-Stage Regulating Voltage-Doubling Rectifier for Wireless Power Transfer," in *IEEE Solid-State Circuits Letters*, vol. 6, pp. 29-32, 2023.

Conference Papers

12. **T. Lu**, B. Zhao and S. Du, "9.2 A 91%-Efficiency Single-Stage Bipolar Quad-Output Regulating Rectifier with Event-Driven Output Power Enhancement via Coil-Reused DC-DC for Wireless Power Transfer," *IEEE International Solid-State Circuits Conference (ISSCC)*, 2026, pp. 160-162.
13. **T. Lu** and S. Du, "A Simultaneous Wireless Power and Full-Duplex Data Transfer System Over a Single Inductive Link Achieving 17/3.4Mb/s and 61.1% Efficiency for Miniature Biomedical Implants," *IEEE International Solid-State Circuits Conference (ISSCC)*, 2026, pp. 72-74.
14. **T. Lu** and S. Du, "A 200.2-mW Wireless Power Transfer System with Hybrid SC-/RC-LSK and Triple Regulated Outputs Achieving 66.1% E2E Efficiency," *IEEE European Solid-State Electronics Research Conference (ESSERC)*, 2025, pp. 77-80.
15. **T. Lu**, X. Li, W. Peng and S. Du, "A 0.49W 120.230VRMS to 8.12VDC Power Converter with Switched-Capacitor Regulation and Rectifier Short Flipping Achieving Maximized Bridge Conduction Time," *IEEE Custom Integrated Circuits Conference (CICC)*, 2025.
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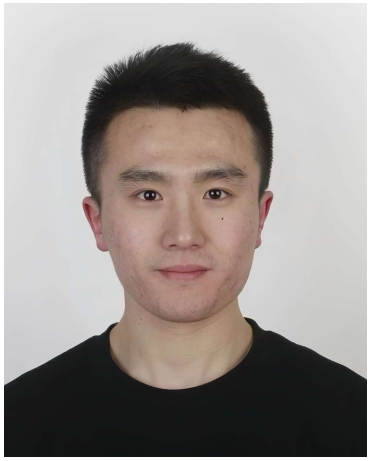
17. **T. Lu** and S. Du, "A Switching-Mode Single-Stage Dual-Output Regulating Rectifier Achieving 92.33% Efficiency and Extended Range for Wireless Power Transfer," *IEEE European Solid-State Electronics Research Conference (ESSERC)*, 2024, pp. 169-172.
18. S. Li, **T. Lu**, J. Jiang and S. Du, "A Fully Integrated Recursive Switched-Capacitor DC-DC Converter with Hybrid Hysteresis-CFM Control," *IEEE European Solid-State Electronics Research Conference (ESSERC)*, 2024, pp. 57-60.
19. **T. Lu** and S. Du, "A 3-Phase Resonant Current-Mode Wireless Power Receiver with Residual-Free Energy Delivery and Digital-Assisted ZVS Achieving 94.5% Efficiency," *IEEE Custom Integrated Circuits Conference (CICC)*, 2024, pp. 1-2.

20. **T. Lu** and S. Du, "27.4 A 13.56MHz Wireless Power Transfer System with Hybrid Voltage-/Current-Mode Receiver and Global Digital-PWM Regulation Achieving 150% Transfer Range Extension and 72.3% End-to-End Efficiency," *IEEE International Solid-State Circuits Conference (ISSCC)*, 2024, pp. 450-452.

21. **T. Lu**, Z. -Y. Chang, J. Jiang, K. Makinwa and S. Du, "A 13.56MHz Fully Integrated 91.8% Efficiency Single-Stage Dual-Output Regulating Voltage Doubler for Biomedical Wireless Power Transfer," *IEEE Custom Integrated Circuits Conference (CICC)*, 2023.

22. **T. Lu** and S. Du, "A 6.78 MHz Dual-output Reconfigurable Rectifier with Hysteretic Output Regulation for Wireless Power Transfer Systems," *IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, 2022.

About the Author



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