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ABSTRACT

By its very nature, Spin Wave (SW) interference provides intrinsic support for Majority logic function evaluation. Due to this and the fact that the 3-input Majority (MAJ3) gate and the inverter constitute a universal Boolean logic gate set, different MAJ3 gate implementations have been proposed. However, they cannot be directly utilized for the construction of larger SW logic circuits as they lack a key cascading mechanism, i.e., fanout capability. In this paper, we introduce a novel ladder-shaped SW MAJ3 gate design able to provide a maximum fanout of 2 (FO2). The proper gate functionality is validated by means of micromagnetic simulations, which also demonstrate that the amplitude mismatch between the two outputs is negligible, proving that an FO2 is properly achieved. Additionally, we evaluate the gate area and compare it with SW state-of-the-art and 15 nm CMOS counterparts working under the same conditions. Our results indicate that the proposed structure requires a 12× less area than the 15 nm CMOS MAJ3 gate and that at the gate level, the fanout capability results in 16% area savings, when compared to the state-of-the-art SW majority gate counterparts.

The rapid increase in available row data led to an abrupt downscaling of the CMOS technology in order to meet the continuously increasing application demand for high performance computation platforms.[1] However, CMOS scaling became more and more difficult due to various technological hurdles, such as (i) quantum mechanics related phenomena and physical limitations, such as leakage;[2] (ii) high failure rate and short lifetime of devices;[3] and (iii) steep fabrication cost increase not justifiable by scaling economical benefits.[2] As a result, different emerging technologies are now explored as potential candidates for future partial/total CMOS replacement.[4,5] One of them relies on Spin Wave (SW) interference within magnetic waveguides.[4,5] Preliminary investigations suggest that SW based computing potentially enables ultra low power consumption at acceptable delay and has great scalability potential.[4,5] SW computing is based on wave interference, which can be either constructive or destructive depending on the interfering SW phases. This principle is used to build SW logic gates. A spin wave interferometer, e.g., Mach–Zhender interferometer, was used to investigate this phenomenon.[6–10] To this end, different logic and Majority gate designs were introduced;[11–21] they all, with the exception of Refs. 16 and 17, make use of bent waveguides through which weak signals as SWs do not properly propagate and attenuate very fast.

As the 3-input Majority gate (MAJ3) together with an inverter forms a universal Boolean logic gate set, it provides the foundation for the potential implementation of complex SW circuits.[11] However, building larger circuits requires gates with fan-out capability, which none of the previously mentioned designs possesses. Thus, if a certain Majority gate has to provide its output to more than one gate input, it has to be replicated. For example, if a gate output has a fan-out $f > 1$, all the gates on its cone of influence starting for the circuit primary inputs have to be replicated f times. Given that practical circuits include many such gates, the lack of fan-out capability results in substantial area and energy consumption overheads. The SW circuit fan-out issue has been addressed, and magnonic splitter[22–25] or caustic beam[22] based solutions have been proposed. However, the presented designs require large frequency bands and are not scalable. If the magnetic field is applied in plane, the T-shape magnonic splitter[23] relies on the SW mode (backward volume and surface) conversion. Given that the dispersion relation is magnetic field direction dependent, such an approach results in complex SW interference patterns, which precludes the utilization

of T-shape magnonic splitters in the design of large SW circuits. The possibility to implement a magnonic splitter by voltage controlled reconfigurable nano-channels was discussed in Ref. 24; however, no detailed analysis of the spin wave quality after splitting has been provided. Additionally, a nonlinear directional coupler that allows SW transmission from a waveguide to another was investigated[25] and demonstrated the SW power dependency of this phenomenon. However, this concept splits the SW energy and cannot provide SW replication, which is crucial for gate fan-out achievement.

In view of the above, it can be concluded that SW based computing with potential ultra low energy consumption cannot become reality without gate intrinsic fan-out capabilities. Here, we overcome this challenge and introduce a generic SW Majority gate structure that provides natural fan-out support. Our structure is based on an area efficient 3-input Majority ladder-shaped SW gate structure that is able to provide a maximum fan-out of 2. This concept has been validated by means of micromagnetic simulations with the Object Oriented Micromagnetic Framework (OOMMF).

Generally speaking, the proposed gate can operate with any SW type; however, each SW type has its proper dispersion relation, which plays a crucial role in the actual gate design. Magnetostatic Spin Waves (MSWs) can be classified into three limiting cases: Magnetostatic Surface Spin Wave (MSSW), Backward Volume Magnetostatic Spin Wave (BVMSW), and Forward Volume Magnetostatic Spin Wave (FVMSW).[26] Depending on the wave propagation direction, BVMSW and MSSW exhibit different dispersion relations. This complicates the circuit design because similar SW propagation in both horizontal and vertical directions is required. For FVMSWs, which propagate in a plane perpendicular to the static magnetization orientation, SW exhibits the same dispersion relation regardless of the wave vector orientation. In this view, we rely on them in the gate design introduced in the following lines.

Different SW excitation (and detection) methods exist, e.g., microstrip antennas,[27,28] magnetoelectric cells,[29–31] spin–orbit torque.[32,33] A spin wave propagates through the waveguide with a wavelength λ, frequency f, amplitude A, and phase ϕ. Information can be encoded in its amplitude, phase, or both of them. If multiple SWs coexist in a waveguide, the computation can be performed using wave interference. Two waves with the same λ, A, and f can interfere constructively or destructively depending on their relative phase difference: (i) in-phase SWs interfere constructively and the resulting wave has a doubled amplitude and (ii) out-of-phase SWs interfere destructively, and therefore cancel each other. If more than two equal λ and f SWs interfere, the result reflects a Majority decision, i.e., if more SWs have $\phi = \pi$ (logic "1") than $\phi = 0$ (logic "0"), the resultant SW has $\phi = \pi$, and $\phi = 0$ otherwise. This means that the SW interference provides natural support for direct (no Boolean gates are required) Majority gate implementations. For example, a CMOS implementation of a 3-input Majority gate requires 18 transistors, whereas a single magnetic waveguide is enough for the SW counterpart.[11,16] In the linear regime, it is possible to have simultaneous propagation of spin waves with different frequencies. The information can be encoded in the phase of the spin wave at each and every frequency, and therefore, SW gates inherently enable parallel computation on shared hardware resources. Additionally, if the involved waves have different amplitudes, they still interfere constructively or destructively depending on the phase difference. However, this generates multiple SWs with different amplitude values, which could be beneficial for the realization of multi-valued logic gates. In the most general case, SWs with different amplitudes, phases, wavelengths, and frequencies can be excited and intricately interfere in the same waveguide. This provides promising alternative avenues toward novel, yet to be discovered, SW based computing paradigms and systems.

In this paper, we propose a 3-input Majority gate (MAJ3) that has a ladder-shape structure, as depicted in Fig. 1. The inputs are excited at (I_1, I_2, I_3, and I_4) and the outputs are read from (O_1, O_2).

To obtain a proper interference pattern at the crosspoints, the waveguide width w has to be less than or equal to the wavelength λ. Also, the excited SWs should have the same amplitude A. In addition, all excited SWs are required to have the same frequency to achieve the desired interference pattern. We propose a generic device layout, its dimensions, and some critical distances d_i (where i = 1, 2, . . ., 7) expressed in terms of spin wave wavelengths, as indicated in Fig. 1. For example, if λ wavelength SWs have to constructively interfere when they have the same phase and destructively otherwise, d_1, d_2, d_3, d_4, and d_5 must be equal with $n\lambda (n = 1, 2, 3, \ldots)$. If the opposite behavior is targeted, d_1, d_2, d_3, d_4, and d_5 must be equal with $\frac{n}{2}\lambda (n = 1, 3, 5, \ldots)$. Moreover, to obtain a proper fan-out of 2, i.e., outputs with the same energy levels, the structure has to be symmetric, and thus d_1 to d_5 must have the same value.

In contrast with CMOS gates, SW gates can provide both direct and inverted output by properly adjusting the output transducer position vs the output interference point. In this way, the direct and inverted result can be read at a distance of $n\lambda (n = 1, 2, 3, \ldots)$ and $\frac{n}{2}\lambda (n = 1, 2, 3, \ldots)$ from the last interference, respectively. In our case, MAJ (a, b, c) and $\overline{MAJ}(a, b, c)$ are obtained at $d_6 = d_7 = n\lambda (n = 1, 2, 3, \ldots)$ and $d_6 = d_7 = \frac{n}{2}\lambda (n$

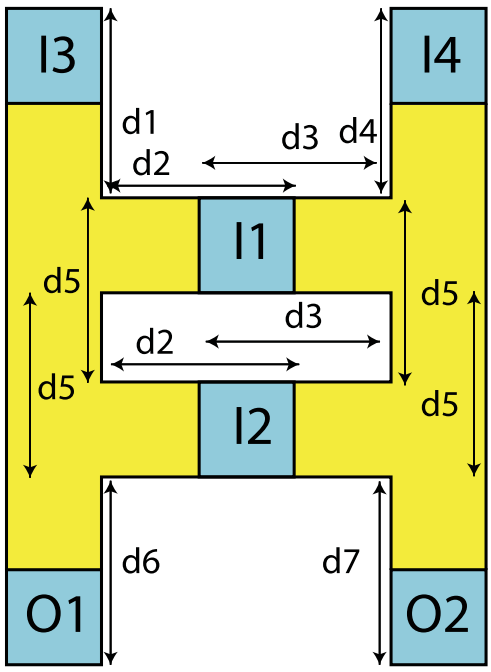

FIG. 1. 3-input Majority gate with fan-out capability.

TABLE I. MAJ3 truth table.

I_1	I_2	I_3	O_1	I_1	I_2	I_4	O_2	Indication in Fig. 2
0	0	0	0	0	0	0	0	(i)
0	0	1	0	0	0	1	0	(ii)
0	1	0	0	0	1	0	0	(iii)
0	1	1	1	0	1	1	1	(iv)
1	0	0	0	1	0	0	0	(v)
1	0	1	0	1	0	1	0	(vi)
1	1	1	1	1	1	0	1	(vii)
1	1	1	1	1	1	1	1	(viii)

= 1, 3, 5, . . .), respectively, and both outputs exhibit the same energy because of the structure symmetry.

Intuitively speaking, the Majority gate operates as follows: (i) SWs with appropriate phases are initiated at I_1, I_2, I_3, and I_4 to the targeted logic value (0 or 1). (ii) The excited SWs propagate (in both directions in the horizontal and vertical waveguides) and interfere when meeting each other. The resulting wave propagates toward the outputs O_1 and O_2. Thanks to the symmetry of the device and the isotropic behavior of the spin waves in this configuration, the waves arriving at the gate outputs are identical, and thus, the 3-input Majority gate exhibits a fan-out of 2. It is worth mentioning that I_3 has an effect on O_2 as the spin wave signal excited at I_3 propagates through I_1 and I_2. Also, I_4 has an effect on O_1 as the spin wave signal excited at I_4 propagates through I_1 and I_2. In addition, spin wave excited at I_1 and I_2 face edges, while its propagation to the output, in contrast to I_3 and I_4, which have a straight path to the outputs. Therefore, I_3 and I_4 are excited at lower energy than I_1 and I_2 as will be discussed further later in this paper.

It is worth mentioning that I_3 has an effect on O_2 as the SW excited at I_3 propagates through I_1 and I_1. Similarly, I_4 has an effect on O_1 as the spin wave signal excited at I_4 propagates through I_1 and I_2. In addition, SWs excited at I_1 and I_2 face edges, while they propagate toward the outputs, while I_3 and I_4 generated SWs have a straight path to O_1 and O_2, respectively. Therefore, I_3 and I_4 are excited at lower energy than I_1 and I_2 as will be discussed further in this paper.

We validate the proposed majority gate by means of micromagnetic simulations while making use of $Fe_{60}Co_{20}B_{20}$ waveguides, with a Perpendicular Magnetic Anisotropy (PMA) field greater than the magnetic saturation, which means that no external magnetic field is required for proper gate operation. We instantiated a MAJ3 gate for waveguide width $w = 75$ nm, and to simplify the interference pattern, we selected a larger wavelength than w, SW wavelength $\lambda = 165$ nm, which implies that $d_1 = d_2 = d_3 = d_4 = d_5 = d_6 = d_7 = 165$ nm. Furthermore, we assume the following values of the relevant parameters:[34] magnetic saturation $M_s = 1.1 \times 10^6$ A/m, exchange stiffness $A_{exch} = 18.5$ pJ/m, damping constant $\alpha = 0.004$, perpendicular anisotropy constant $k_{ani} = 8.3177 \times 10^5$ J/m^3, and waveguide thickness $t = 1$ nm. We calculated the FVMSW dispersion relation for these parameters,

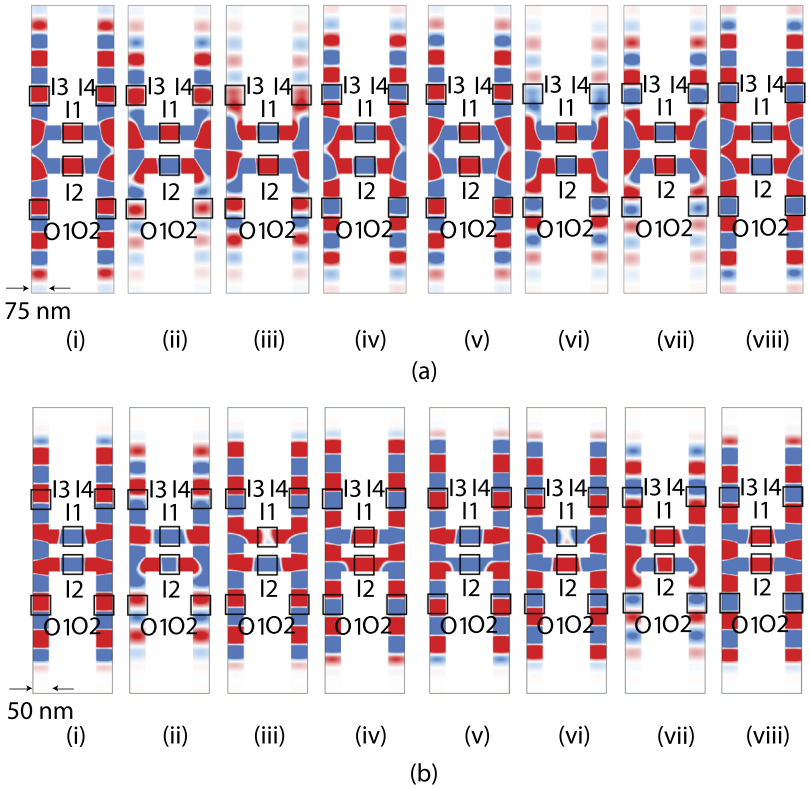

FIG. 2. Color coded snapshots of the magnetization state demonstrating all majority functions for two widths of SW waveguide: (a) 75 nm and (b) 50 nm. Blue represents logic 1, which presents a phase of π, red presents logic 0, which presents phase 0, the input order is (I_3 I_2 I_1) and (I_4 I_2 I_1), and (i), (ii), (iii), (iv), (v), (vi), (vii), and (viii) present the gate reaction to (0 0 0), (0 0 1), (0 1 0), (0 1 1), (1 0 0), (1 0 1), (1 1 0), and (1 1 1) input patterns, respectively.

and for λ = 165 nm, and $k = 2\pi/\lambda$ = 38 rad/μm, the SW frequency is determined to be f = 6.5 GHz. To get some indication of the MAJ3 scaling implications, we also designed smaller structures, e.g., w = 50 nm, with λ = 110 nm and f = 9 GHz. This makes the distances $d_1 = d_2 = d_3 = d_4 = d_5 = d_6 = d_7$ = 110 nm.

The proposed design combines two Majority gates operating in parallel on the same input set as can be observed in Table I. I_1, I_2, and I_3 constitute the first Majority gate with its output being detected at O_1, whereas I_1, I_2, and I_4 constitute the second Majority gate with O_2 as the output. Figure 2 presents OOMMF simulation results for the proposed w = 75 nm and w = 50 nm MAJ3 gates, under all possible input combinations. Note that in the figure, blue presents logic "1" (i.e., phase of π), red presents logic "0" (i.e., phase 0), the input order is (I_3 I_2 I_1) and (I_4 I_2 I_1), and (i), (ii), (iii), (iv), (v), (vi), (vii), and (viii) capture the gate reaction to (0 0 0), (0 0 1), (0 1 0), (0 1 1), (1 0 0), (1 0 1), (1 1 0), and (1 1 1) input patterns, respectively. As can be observed from Fig. 2, the results are in agreement with the MAJ3 truth table in Table I. If $I_1 = I_2 = I_3 = 0$ or the majority of the inputs are 0, then $O_1 = O_2 = 0$ (red), whereas if the majority of the inputs are 1, then the outputs O_1 and O_2 are 1 (blue), as expected. In addition, it can be noticed in Fig. 2 that the scaling does not affect the functionality of the Majority gate.

Figure 3 presents the possibility of having the inverted and non-inverted outputs by adjusting the reading position. As one can observe in Fig. 3, the inverted output (O'_1 and O'_2) of the Majority gates can be obtained by just shifting the reading position to a $\frac{n}{2}\lambda$ position.

By post-processing the OOMMF simulations, we estimated the MAJ3 gate delay, i.e., the maximum time it takes for the inputs to propagate to the output, as 1.5 ns and 1 ns for the w = 75 nm and w = 50 nm structures, respectively. To investigate the waveguide width reduction influence on the SW group velocity Vg, we calculated the group velocities from micromagnetic simulation and obtained Vg_{50nm} = 1.15 μm/ns and Vg_{75nm} = 1 μm/ns for w = 50 nm and w = 75 nm structures, respectively. We also note that SWs are traveling shorter distances for the smaller structure, e.g., distance I_3 to O_1 is 380 nm for w = 50 nm and 570 nm for w = 75 nm. This implies that the I_3 to O_1 propagation takes 330 ps for w = 50 nm and 570 ps w = 75 nm. Therefore, the gate performance increase is a consequence of both shorter traveling distance and increased group velocity. Thus, the gate delay can be further reduced by scaling down w, but also by making use of other waveguide materials.

We note that if only one MAJ3 output is required, then the structure can be simplified: (i) physically, by removing one of its vertical waveguides (arms) or (ii) logically, by not providing an input signal to I_4. Moreover, the gate fan-out capabilities can be extended beyond two by vertically lengthening its arms. For example, if the outputs in Figs. 2 and 3 are shifted downward to the end of the arms and two outputs are placed upward (at the upper-end of the arms), four outputs can be accommodated and if properly designed, the gate can provide a fan-out of 4 as indicated in Fig. 4. However, the detailed design of such a structure constitutes future work and is out of the scope of the current paper.

To get inside on the quality of the achieved fan-out, i.e., the similarity between the two SWs obtained at the gate outputs, we make use of Magnetization Spinning Angle (MSA) as metric. The input and output spinning angles are calculated as

$$MSA = \arctan\left(\frac{\sqrt{(\overline{m_x})^2 + (\overline{m_y})^2}}{M_s}\right), \quad (1)$$

where $\overline{m_x}$ and $\overline{m_y}$ are the x and y components of the magnetization, respectively.

Table II presents the contribution percentage of each input to the outputs O_1 and O_2 when each of them is separately activated, for the 50 nm waveguide width design. The output MSAs in the table are normalized values with respect to the activated input MSA. Thus, when only I_1 is activated, O_1 and O_2 MSAs are normalized by I_1 MSA. The same holds true for the other three situations presented in the table. As it can be noticed, I_3, I_2, I_1, and I_4 contributions to O_1 and O_2 are quite different. Due to the symmetry, I_1 equally contributes to both gate outputs O_1 and O_2 and the same holds true for I_2 also. However, due to its proximity, I_2 has a larger contribution to

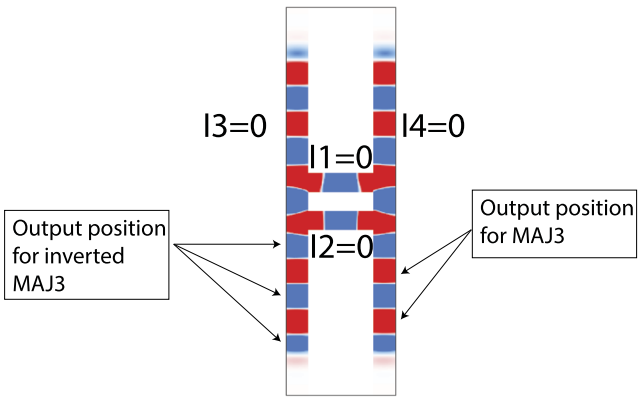

FIG. 3. Inverted outputs O'_1 and O'_2 and non-inverted outputs O_1 and O_2.

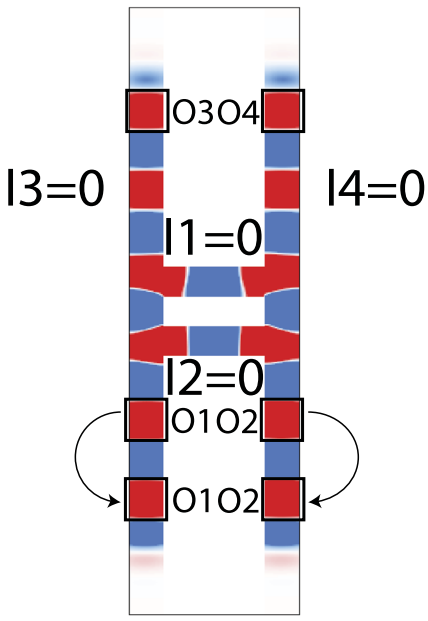

FIG. 4. FO4 MAJ3 gate.

TABLE II. Input contribution percentage on the outputs—separately activated inputs.

Inputs	O_1/I (%)	O_2/I (%)
I_1	54	54
I_2	57	57
I_3	96	35
I_4	35	96

the outputs than I_1 and as such their strengths have to be properly balanced. Input I_3 SW is the strongest contributor to O_1 as it has a direct path to O_1, while spin waves from I_2 and I_1 are facing edges and reflect back and forth. Moreover, I_3 mostly affects O_1 and to a lower extent O_2, while the I_4 effect is stronger on O_2 and weaker on O_1. Thus, as the inputs on the vertical and horizontal waveguides differently contribute to the outputs, I_3 and I_4 SWs must be excited at lower energy than I_1 and I_2 SWs to enable the correct gate behavior.

Table III presents the normalized (with respect to I_1) MSA of the outputs when all inputs are activated together for the same w = 50 nm design. As it can be noticed from Table III, the normalized O_1 and O_2 MSA is the same in all cases, which means that the proposed MAJ3 gate can successfully achieve a fan-out of 2. One can also observe in the table that different input combinations are producing different normalized MSA values. When all gate inputs have the same value ($I_1 = I_2 = I_3$), the output MSA is reaching the highest value because of the constructive interference. When inputs have different values, the destructive interference diminishes the spin wave energy, which results in lower MSA values. Moreover, when the horizontal inputs (I_1 and I_2) are different, the position of the asserted input affects the MSA output. For example, when (I_3 = 1, I_2 = 0, and I_1 = 1) or (I_3 = 0, I_2 = 1, and I_1 = 0), the normalized output MSA is higher than when (I_3 = 1, I_2 = 1, and I_1 = 0) or (I_3 = 0, I_2 = 0, and I_1 = 1) because I_2 is located further than I_1 and I_3 from the interference location. As a result, when I_1 and I_3 have the same state, they interfere constructively and then destructively with I_2, which results in a larger magnetization angle.

An accurate evaluation of the proposed structure is not possible at this stage of development, especially for the energy and delay. That is mostly due to the missing excitation and detection cell figure of merit data. Thus, as the transducers are the dominant source for energy and delay, we chose to use the area as a metric to position our proposal vs the existing state of the art.

TABLE III. Normalized outputs (O_1 and O_2) by I_1—simultaneously activated inputs.

Inputs				
I_1	I_2	I_3 AND I_4	O_1/I_1 (%)	O_2/I_1 (%)
0	0	0	1	1
0	0	1	0.28	0.28
0	1	0	0.37	0.37
0	1	1	0.45	0.45
1	0	0	0.45	0.45
1	0	1	0.37	0.37
1	1	0	0.28	0.28
1	1	1	1	1

In order to make a fair comparison with Ref. 12, we scaled down the MAJ3 design for $w = \lambda = 48$ nm and validate it by means of OOMMF simulations. In addition, the outputs are captured directly at the last interference point. The proposed scaled FO2 MAJ3 gate requires a real estate of 0.0576 μm^2. As the gate in Ref. 12 cannot provide fan-out, we have to consider two such gates working in parallel on the same input set to evaluate both gates in similar utilization conditions, which results in a required area of 0.0691 μm^2, i.e., our proposal provides a 16% area reduction at the gate level. We note, however, that at the circuit level the area savings are significantly more substantial, as, in order to deal with a fan-out of 2 gate output O, the approach in Ref. 12 requires the replications of all the gates on O's cone of influence starting from the circuit primary inputs, and that for efficient logic synthesis of practical circuits, gates with >1 fan-out are frequently necessary.

In order to compare with CMOS, we evaluated a 3-input Majority gate implemented in 15 nm technology with two NAND gates and one OR-AND-Invert (OAI) gate, at V_{dd} = 0.8 V, 25 °C, and an output load capacitance of 20 fF. Our evaluation indicates that the 15 nm CMOS MAJ3 area is 0.688 μm^2, thus a 12× larger area than the proposed SW MAJ3 gate.

In summary, we presented a novel fan-out of 2 area efficient 3-input spin wave Majority gate (MAJ3). We validated two instances of our proposal by means of OOMMF simulations and evaluated the fan-out quality by making use of the Magnetization Spinning Angle (MSA) as the metric. We calculated the normalized MSA values for the gate outputs and obtained negligible mismatch between them under all possible input combinations, i.e., a high quality fan-out. We compared our proposal with MAJ3 SW, under the same material assumptions and utilization conditions, and 15 nm CMOS state-of-the-art counterparts in terms of area and demonstrated a 16% and 12× less area, respectively. As a closing remark, we note that achieving >1 fan-out is an enabling factor for the realization of SW circuits as it eliminates the otherwise required circuit replication associated with fan-out nodes intrinsic to SW circuits produced by means of logic synthesis. Thus, the implications of our proposal at the circuit level are a lot more substantial than at the gate level, both in terms of area and energy consumption.

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DATA AVAILABILITY

The data that support the findings of this study are available within the article.

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