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On the Electron Transport in Simplified IBC-SHJ Solar Cells With MoO_x Blanket Layer

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ABSTRACT

Interdigitated-back-contacted silicon heterojunction (IBC-SHJ) solar cells with molybdenum oxide (MoO_x) as a hole transport layer and a novel (*n*)-type hydrogenated nanocrystalline silicon (nc-Si:H)/MoO_x electron transport stack use ultra-thin MoO_x as a full-area blanket layer. This solar cell architecture is realized with a simplified fabrication process and ensures high shunt resistances, attributed to the low lateral conductivity of the MoO_x layer. Here we investigate the electron transport mechanisms through the electron collection contact to improve the understanding and performance of the IBC-SHJ solar cells. For this evaluation, we first introduce plasma treatments between (*n*)nc-Si:H and MoO_x and assess their role in passivation, charge carrier transport and MoO_x growth. Temperature-dependent current–voltage (*I–V*) measurements of front/back-contacted (FBC) solar cells with (*n*)nc-Si:H/MoO_x stack, supported by high-resolution transmission electron microscopy (HR-TEM) and energy dispersive X-ray spectroscopy (EDX) imaging and numerical simulations, reveal that plasma treatment (PT) and plasma treatment with boron (PTB) enable electron transport based on direct energy transitions. Next, we perform thickness sensitivity analysis to find the optimal layer thicknesses of (*n*)nc-Si:H and MoO_x. While FBC-SHJ devices exhibit stable performance across a broad range of (*n*)nc-Si:H thicknesses (10–50 nm), IBC-SHJ devices are more sensitive to such a thickness variation, with thinner (*n*)-layers limiting final device efficiency. The combination of 50-nm thick (*n*)nc-Si:H, PTB, and 1.7-nm thick MoO_x enables the best performance of IBC-SHJ solar cells. When metallized with electroplated Cu, our champion IBC-SHJ solar cell with MoO_x blanket layer reaches an efficiency of 23.59%. Further advancements in (*n*)nc-Si:H properties, passivation, transparent conductive oxide selection, and front-side light management are expected to drive efficiencies well above 24%.

1 | Introduction

Interdigitated-back-contacted silicon heterojunction (IBC-SHJ) solar cells combine the advantages of SHJ technology with IBC architecture, enabling both high open-circuit voltage (V_{OC}) [1] and short-circuit current density (J_{SC}) [2] and offering the potential for achieving the ultimate single-junction photoconversion efficiency [3]. Namely, SHJ solar cells ensure high passivation quality and efficient transport of charge carriers by implementing intrinsic hydrogenated amorphous (a-Si:H) [4–8] and doped hydrogenated nanocrystalline silicon (nc-Si:H)-based layers [9–15]. In IBC architecture, both electrodes are placed on the rear side of the solar cell, ensuring efficient light in-coupling and avoiding metal grid shading losses as well as parasitic absorption in a-Si:H, nc-Si:H, and transparent conductive oxide (TCO) layers [16]. Specifically, a record single-junction solar cell efficiency of 27.3% has been reported for IBC-SHJ solar cells [2], exhibiting $J_{SC} = 42.62\,mA/cm^2$ [2]. On the other hand, the processing of back-contact solar cell architecture commonly introduces additional complexity to the fabrication process as it requires accurate patterning of contacts on the rear side [17].

Tomasi et al. [18] presented the so-called tunnel-IBC architecture to simplify the fabrication process of IBC-SHJ solar cells by introducing a simplified self-aligned approach and reducing the total number of processing steps. Such an approach includes

the patterned deposition of a (*n*)nc-Si:H via hard mask, followed by full-area deposition of (*p*)nc-Si:H. Hole collection takes place through the (*p*)nc-Si:H layer, whereas electron collection occurs through the tunneling recombination junction formed by (*n*)nc-Si:H and (*p*)nc-Si:H stack [18]. A tunnel-IBC solar cell demonstrating an efficiency of 25.4% has been reported [19]. However, implementing a highly conductive (*p*)nc-Si:H layer that contacts both electrodes potentially leads to lower shunt resistance, limiting the attainable *FF* and, thus, the final performance of tunnel-IBC solar cells [20].

As an alternative to tunnel-IBC solar cells, in our previous work, we presented an IBC-SHJ solar cell architecture with a molybdenum oxide (MoO_x, $x<3$) blanket layer replacing the (*p*)nc-Si:H [21]. MoO_x is selected as a suitable candidate due to its low lateral conductivity compared with (*p*)nc-Si:H [22–24] and successful implementation in SHJ solar cells as a hole transport layer (HTL) [24–34]. Moreover, thin MoO_x layers can be processed faster compared with typical (*p*)nc-Si:H layers [22, 24, 32], via a simpler deposition process such as thermal evaporation, giving this approach a potential advantage from the industrial point of view. In Figure 1A, we present a sketch of the IBC solar cell with a thin (<2 nm) MoO_x blanket layer. In this structure, MoO_x is deposited over a pre-patterned (*n*)nc-Si:H and requires no patterning or intentional gap formation due to its thin thickness and low conductivity. Metal fingers can be used to mask TCO and isolate electron and hole collecting regions [35]. This ultimately means that only one patterning step (patterning of (*n*)nc-Si:H) followed by only one alignment step (alignment of metal fingers with (*n*)nc-Si:H) is necessary for the fabrication of our IBC solar cells. The patterning can be done by photolithography or with more industrially appealing methods such as laser patterning [2] or shadow masking [18].

In the proposed structure, holes are collected through the (*i*)a-Si:H/MoO_x/TCO stack, whereas electron collection occurs through the novel electron transport layer (ETL) stack consisting of (*i*)a-Si:H/(*n*)nc-Si:H/MoO_x/TCO [21]. In our previous work, we described the basic working principle of this novel ETL stack. Carrier dynamics in this layer stack occur in the conduction band [36, 37]. Hence, unlike in the case of (*n*)nc-Si:H/(*p*)nc-Si:H stack of tunnel-IBC solar cells, no recombination junction forms in the MoO_x-based ETL stack. However, the deposited layers build a potential barrier for carrier collection. To control such a barrier, we previously proposed the use of (*n*)nc-Si:H layers featuring low activation energy (E_a) [10, 13, 37–40]. In the initial stages of developing IBC-SHJ solar cells with MoO_x blanket layer and (*n*)nc-Si:H, we reported efficiencies up to 21.14% with *FF* of 78.61% and high shunt resistances [21].

In this work, we further explore the potential of MoO_x-based IBC solar cells focusing on the understanding and optimization of the electron collection stack with the final aim to achieve an efficiency boost. This study builds on our initial proof-of-concept [21], combining theoretical modeling and experimental analysis to investigate electron transport mechanisms within the novel (*n*)nc-Si:H/MoO_x ETL stack. By developing a comprehensive understanding of this stack and device structure, we provide a foundation for targeted optimization efforts aimed at maximizing the performance of MoO_x-based IBC solar cells. First, to decouple the behavior of the ETL stack from the IBC solar cells' performance, we fabricated front/back-contacted (FBC) SHJ solar cells featuring such a stack. We evaluated the influence of plasma treatments (PTs) as well as (*n*)nc-Si:H and MoO_x thicknesses on the performance of the solar cells. Moreover, temperature-dependent current–voltage (*I–V*) measurements, supported by high-resolution transmission electron microscope (HR-TEM) with energy-dispersive X-ray spectroscopy (EDX) imaging, were performed to understand the role of the PTs in electron transport. Lastly, we fabricated IBC-SHJ solar cells with the optimized layer stack and electroplated Cu electrodes reaching an efficiency of 23.59%.

2 | Experimental Details

Figure 1 shows a schematic representation of fabricated FBC and IBC solar cells. FBC solar cells (Figure 1B) were manufactured to independently evaluate the novel ETL stack before integration into IBC solar cells (Figure 1A). For the fabrication of all solar cells, we used (*n*)-type Topsil float-zone (FZ) <100> c-Si wafers with thicknesses of 280 ± 20 µm and resistivities of 3 ± 2 Ωcm. The wafers were textured to achieve a random distribution of pyramids using a diluted tetra-methylammonium hydroxide (TMAH) solution with monoTEX additive (RENA Technologies) [41]. Subsequently, the wafers were cleaned using room-temperature 99% nitric acid (HNO_3), 110°C 69.5% HNO_3, and finally, 0.55% hydrofluoric acid (HF) [42].

This was followed by the deposition of silicon-based thin-film layers in a multi-chamber plasma-enhanced chemical vapor deposition (PECVD) tool (Elettrorava S.r.l.). In the case of FBC

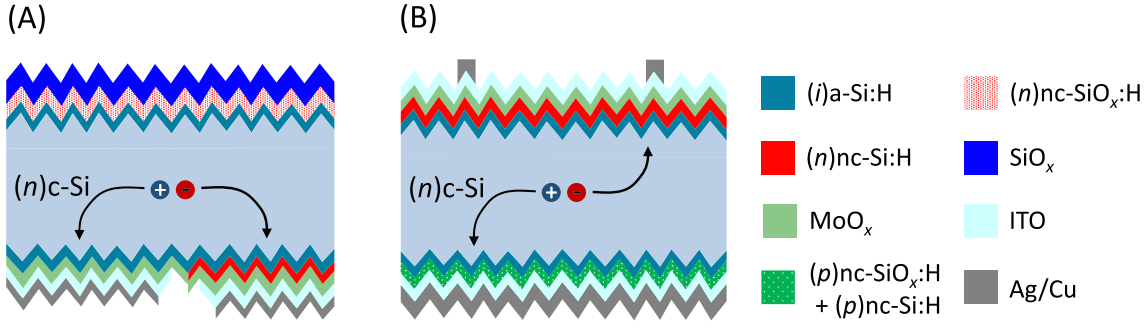

FIGURE 1 | Schematic representation of (A) IBC-SHJ solar cell with full area MoO_x on the rear side and (B) FBC-SHJ solar cell with MoO_x as a part of electron collection contact stack on the front side.

solar cells, (*i*)a-Si:H/(*n*)nc-Si:H layer stack was deposited first, followed by a brief vacuum break and, after reloading the samples, the deposition of (*p*)-contact layer stack. The deposition conditions of intrinsic and doped silicon-based thin films were reported in our previous works [4, 22, 38, 43]. During the PECVD process, optional PTs were incorporated into the ETL layer stack before the deposition of MoO_x as described in [25, 28, 44]. We applied two treatment conditions: PT, which involves a precursor gas mixture consisting of SiH_4, H_2, and CO_2, and PT with boron (PTB), which additionally includes B_2H_6 [25, 28, 44]. Following the PECVD steps, MoO_x layers were deposited through thermal evaporation at a base pressure of 5.0×10^{-6} mbar using a stoichiometric MoO_3 powder (Sigma Aldrich) as the source material at a deposition rate of about 0.1 nm/s. Next, the wafers were loaded into a magnetron sputtering tool to deposit tin-doped indium oxide (ITO) at room temperature. 75- and 150-nm thick ITO layers were deposited for the front and rear sides, respectively. The cell precursors with ITO were annealed at 180°C and metallized with screen-printed Ag paste cured in an air environment at 170°C for 40 min. The active cell area of FBC-SHJ solar cells is 3.86 cm^2.

IBC-SHJ solar cells feature (*i*)a-Si:H/(*n*)nc-Si:H/SiO_x layer stack at the front side deposited via PECVD processes. Unlike the rest of the PECVD depositions, the SiO_x was deposited using Plasmalab 80 Plus PECVD (Oxford Instruments plc) tool. Silicon-based layers, PTs, and MoO_x introduced on the rear side were deposited as described above for FBC-SHJ solar cells. All IBC solar cells feature a 150-nm thick ITO layer and were metallized with either 2-μm thick evaporated Ag or 25-μm thick electroplated Cu [45]. Additional photolithography and etching steps were introduced for patterning of (*n*)nc-Si:H, ITO, and metallization. A comprehensive flowchart for IBC solar cell fabrication has been reported in our previous publication [21], describing the deposition and patterning steps in detail. Solar cells metallized with evaporated Ag follow the same fabrication process as presented in our previous publication [21]. Devices with Cu electroplated contacts follow the same process flow up to and including ITO deposition and annealing. After this step, metallization is done with electroplating as described in our previous work [45], followed by ITO etching as the final step of the process with Cu fingers acting as etching mask [35]. Each wafer consists of seven solar cells—three with an area and pitch size of 4.05 cm^2 and 300 μm, respectively; two with area and pitch size of 4.09 cm^2 and 650 μm, respectively; and two with area and pitch size of 4.19 cm^2 and 1200 μm, respectively. We define the area of a solar cell by a measurement mask on the front side of the wafer corresponding to the cell area on the back side excluding busbars.

To monitor the fabrication process of solar cells, we measured the effective carrier lifetime (τ_{eff}) of the cell precursors after every deposition, patterning, or annealing step. These measurements were performed using a Sinton WCT-120 instrument with either transient photoconductance decay mode or quasi-steady-state photoconductance mode [46, 47]. The *I–V* characteristics of the completed solar cells were evaluated using a AAA class Wacom WSX-90S-L2 solar simulator under standard test conditions and calibrated with reference solar cells validated at Fraunhofer ISE CalLab. The same solar simulator was used for temperature-dependent *I–V* measurements. For room temperature *I–V* measurements, solar cells were not cut into single cells but measured as a part of a wafer and contacted with point probes. For temperature-dependent measurements, we cut individual cells from the wafer as we use a conductive, temperature-controlled chuck. To determine the series resistance of the solar cells, we obtained the pseudo-fill factor (p*FF*) using a Sinton Instruments Suns-V_{OC}-150 Illumination-Voltage Tester and used the p*FF* to extract the $R_{s,SunsVoc}$ of solar cells [46, 48, 49]. The same Suns-V_{OC} setup was used to measure the shunt resistance of solar cells. An HR-TEM (FEI cubed Cs-corrected Titan operating at 300 kV) with EDX was utilized to image the structure and composition of the ETL layer stack. The thickness and etching rate of a-Si:H, nc-Si:H, and TCO layers have been determined using J. A. Woollam spectroscopic ellipsometry setup (M-2000DI system). The thickness of MoO_x has been determined by the same setup and confirmed by HR-TEM images, and the thickness of metal contacts has been determined by Dektak stylus profiler by Bruker Corporation and confirmed by Hitachi Regulus SU8230 scanning electron microscope (SEM) [45].

3 | Front/Back-Contacted Solar Cells

3.1 | Effect of PTs

To evaluate the performance of the proposed ETL stack in solar cells, we fabricated rear junction FBC-SHJ solar cells (see Figure 1B), which feature (*n*)nc-Si:H/MoO_x stack and varied PTs on the front side. We kept the thickness of MoO_x at 1.7 nm, as suggested in [25], and the thickness of (*n*)nc-Si:H at 50 nm, as proposed by our previous study [21]. Moreover, we compare the solar cells with the novel ETL stack to a reference SHJ solar cell with a 50-nm thick (*n*)nc-Si:H without MoO_x. On the rear side of the devices, our laboratory standard (*p*)-type contact stack [22] was applied to independently evaluate the performance of the front contact stack. To analyze solar cell performance and compare different contact stacks, we present in Figure 3A the V_{OC}, *FF*, p*FF*, and $R_{s,SunsVoc}$ of (i) solar cells with three different treatment conditions included during fabrication and (ii) reference SHJ solar cells. Moreover, the external parameters of the best solar cell for each set of conditions are summarized in Table S1. We discuss these parameters as relevant indicators of passivation and charge carrier transport in solar cells, as well as parameters that can serve as guidelines when extending the analysis from proof-of-concept FBC solar cells to final IBC devices.

Overall, comparable V_{OC} is observed among solar cells with MoO_x-based ETL ranging between 710 and 715 mV, showing that the additional treatment step has little impact on the passivation quality of the devices. This is possibly linked to the thick (*n*)nc-Si:H layer protecting (*i*)a-Si:H during the treatment step from any potential plasma-induced damage. Unlike V_{OC}, the treatment choice significantly influences *FF* with an increase from 76% without PT to 81% with PT and, finally, above 82% with PTB. This can be explained by significantly lower $R_{s,SunsVoc}$ of solar cells with PTB and lower contact resistivity of samples with PTB compared with the ones without PT, as reported in our previous work [21]. Namely, devices without PT exhibit $R_{s,SunsVoc}$ above 2300 mΩcm^2 on average, with the highest values reaching above 3500 mΩcm^2. This drops to 750 mΩcm^2 for devices with PT and 500 mΩcm^2 for the ones with PTB. All layers and treatments in the fabricated devices were

processed under the same conditions apart from the difference in PTs. Hence, the difference in performance can be ascribed to the PTs and interfaces that are influenced by the treatment choice. Moreover, all solar cells with (*n*)nc-Si:H/MoO_x ETL show comparable p*FF* from 83% to 85%, indicating good junction quality at c-Si interfaces for all samples [50] and confirming that the differences in *FF* originate from fine-tuning the ETL stack. Compared with the reference SHJ solar cell, devices with MoO_x-based ETL and PTB show a higher average V_{OC} and *FF* gain of $2\%_{abs}$ on average related to 1000 $m\Omega cm^2$ lower $R_{s,SunsVoc}$. The differences in V_{OC} and *FF* between solar cells with a MoO_x-based stack and reference SHJ devices are potentially related to a larger energy barrier for holes that is established by the introduction of MoO_x in the stack and, therefore, larger asymmetry for electrons and holes, ensuring better selective transport of electrons [37].

3.2 | Temperature-Dependent *I–V* Measurements and Evaluation of Transport Mechanisms

To investigate the electron transport through the (*n*)nc-Si:H/MoO_x-based stack and the influence of PTs, we analyzed the illuminated *I–V* characteristics of selected solar cells as a function of temperature [28, 34, 51]. We measured solar cells from all sample groups presented in Figure 2A (no PT, PT, PTB, and reference) in the temperature range from 15°C to 55°C. Figure 3 presents V_{OC} and *FF* of a representative device from each group across this temperature range. Moreover, in Figure S1, we present *J–V* curves at different temperatures of the representative solar cells.

All measured solar cells exhibit a decrease in V_{OC} as the cell temperature increases, attributed to increased recombination within

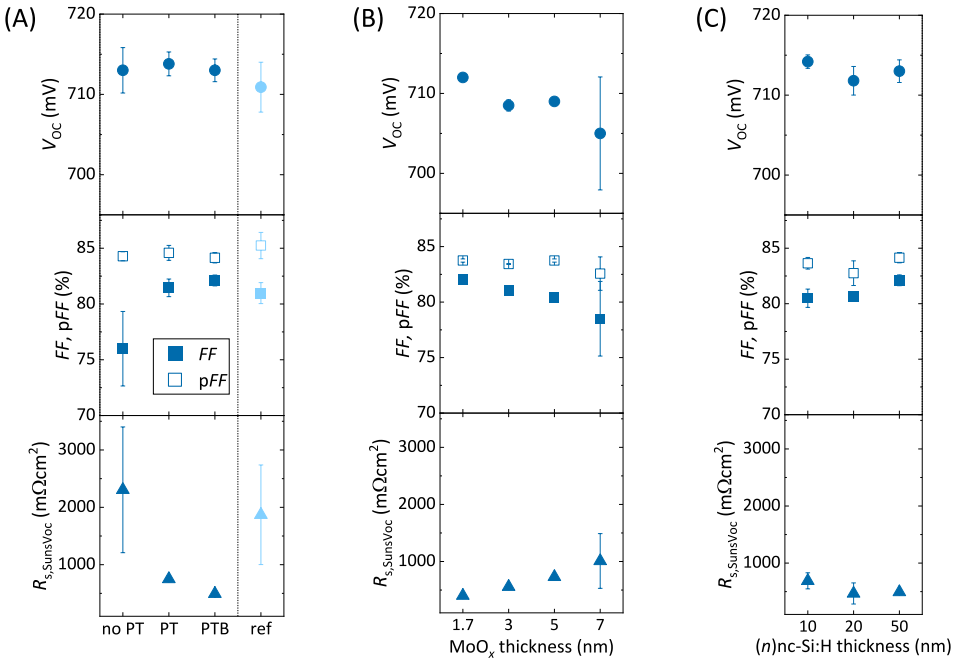

FIGURE 2 | From top to bottom, V_{OC}, *FF* and p*FF*, and $R_{s,SunsVoc}$ of FBC-SHJ solar cells with (*n*)nc-Si:H/MoO_x ETL stack with (A) varied plasma treatment conditions, 1.7-nm thick MoO_x and 50-nm thick (*n*)nc-Si:H, (B) with PTB, 1.7-, 3-, 5- or 7-nm thick MoO_x and 50-nm thick (*n*)nc-Si:H and (C) with PTB, 1.7-nm thick MoO_x and 10-, 20- or 50-nm thick (*n*)nc-Si:H. The average values and error bars are based on 2 cells from one wafer for PTB and 50-nm thick (*n*)nc-Si:H data points and for 5 cells from one wafer for other data points in (A) and (C) and on 2 cells from one wafer for each data point in (B).

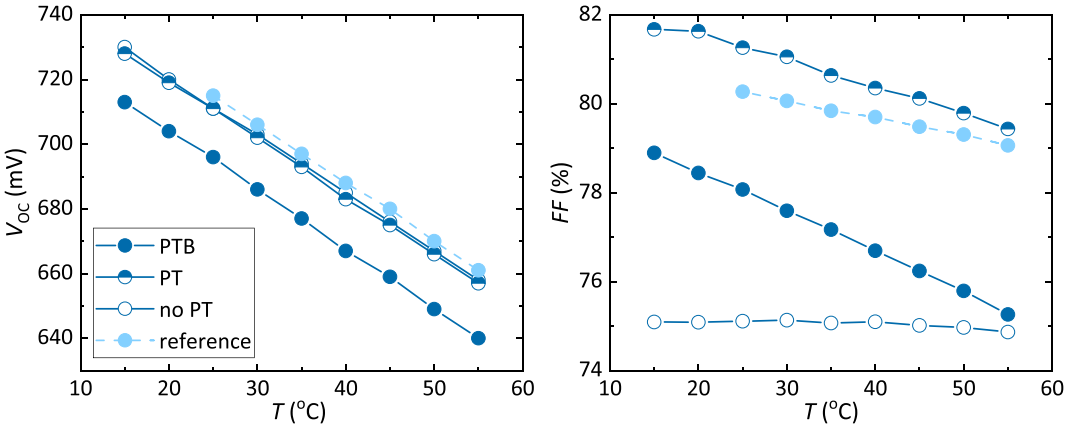

FIGURE 3 | V_{OC} (left) and *FF* (right) evolution as a function of temperature of a representative reference FBC-SHJ solar cell (light blue data set) and representative FBC-SHJ solar cells with (*n*)nc-Si:H/MoO_x contact stack with varied plasma treatment conditions (dark blue data sets).

c-Si at higher operating temperatures [52–54]. In the case of solar cells with PT, PTB, and reference SHJ device, we observe a decrease in *FF* at higher temperatures, which is likely also related to increased recombination as the operating temperature increases. This is commonly observed for SHJ solar cells [51, 55]. However, the temperature-dependent behavior of solar cells is both recombination and transport related [51]. We observe the counterposed interplay of the two effects in the measured *FF* of a solar cell without PT, where no *FF* drop is observed at higher cell temperatures. Instead, *FF* remains constant throughout the temperature range. We suspect that the electron transport in this solar cell is based on indirect energy transitions via energy states within the energy bandgap, leading to significantly improved transport at higher temperatures as reflected in *FF* values. This possibly indicates that transport is predominantly based on trap-assisted tunneling (TAT) associated with recombination processes [28]. In the case of other measured devices (PT, PTB, and reference), due to better energy band alignment, transport is likely based on direct energy transitions dominated by thermionic emission (TE) and direct tunneling (DT) transport mechanisms [28]. In these samples, for higher temperatures, both V_{OC} and *FF* are affected negatively by recombination mechanisms as the transport is not based on TAT.

To better understand the origin of these trends, we performed HR-TEM analysis combined with EDX elemental mapping on representative samples of each treatment group. We present the results in Figures S2 and S3. The analysis shows that the introduction of treatments, especially PTB, reduces oxygen diffusion from MoO_x into the underlying nc-Si:H layer and results in a well-confined MoO_x layer. These two characteristics seem to be crucial for the efficient transport of electrons through this stack, also likely supporting the desired transport mechanisms discussed above.

Insights from TEM and EDX analyses, combined with findings from our previous work [21, 25], served as the basis for numerical simulations performed using the TCAD Sentaurus software by Synopsys Inc [56]. Figure 4 presents the resulting energy band diagrams for stacks without PT and with PTB. Note that we extracted the SiO_x thickness from EDX analysis, whereas the oxygen content in the MoO_x film is based on our previous work [25], and it was used to calculate the work function [25]. In the absence of PT, we observe a thicker oxygen-rich interfacial layer between (*n*)nc-Si:H and MoO_x, which can act as a barrier for carrier transport. In fact, thicker SiO_x hinders the transport of electrons, and trap states within the SiO_x film contribute to the charge dynamics in TAT processes (see Figure 4). It is worth noting that TAT mechanisms are facilitated by phonon interactions, which are temperature dependent. As the device temperature increases, phonon activity rises, therefore enhancing the contribution of TAT to the overall charge transport. This, together with the observed *FF* trend of no PT samples, which remains almost unaffected with temperature, supports the hypothesis that TAT is the dominant transport mechanism. Note that for no PT samples, TAT compensates for the expected *FF* decrease as observed for the reference sample. In contrast, the device with PTB exhibits a more favorable band alignment, enabling carrier transport dominated by DT and TE (see Figure 4), also reflected in decreasing *FF*. Additional experiments and simulations are being conducted to further confirm these findings.

3.3 | Effect of MoO_x and (*n*)nc-Si:H Thickness

Next, we look at the effect of MoO_x thickness on passivation and transport in rear junction FBC solar cells with MoO_x-based ETL stack. Figure 2B shows the V_{OC}, *FF*, p*FF*, and $R_{s,SunsVoc}$ of solar cells 50-nm thick (*n*)nc-Si:H, PTB, and varying thicknesses of MoO_x from 1.7 to 7 nm. Solar cells with 1.7-nm thick MoO_x achieve the highest V_{OC} of 712 mV. The V_{OC} of the solar cells decreases as the thickness of MoO_x increases to an average of 705 mV for a 7-nm thick layer. Similarly, the highest average *FF*

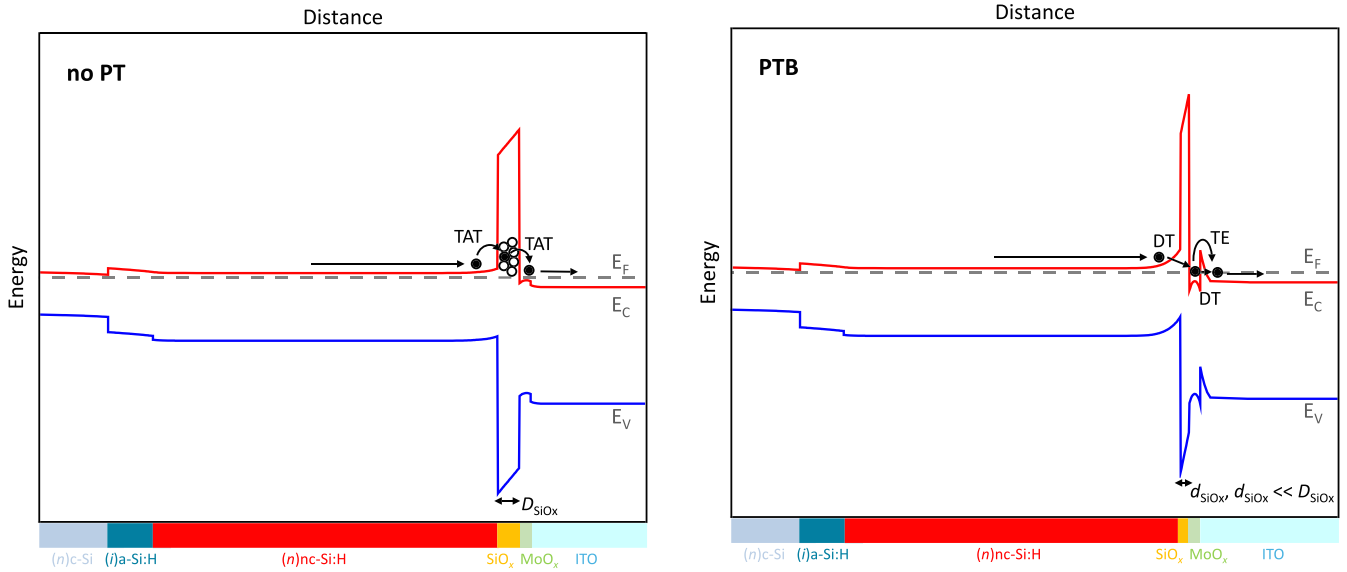

FIGURE 4 | Band diagram illustrating electron transport through layer stack featuring (*n*)nc-Si:H/MoO_x contact without PT (left) and with PTB (right). Conduction and valence bands are shown in solid red and blue lines, respectively, and Fermi level is shown in grey dashed line. Full and hollow circles represent electrons and traps, respectively. Black arrows represent transport of electrons. The corresponding transport mechanisms of charge carriers are thermionic emission (TE), direct tunneling (DT), and trap-assisted-tunneling (TAT).

of 82% is measured in a device with the thinnest MoO_x layer, which then drops to 78.5% on average for the thickest, while the p*FF* remains comparable among the devices. $R_{s,SunsVoc}$ increases as the thickness of MoO_x increases. As the electron transport occurs from (*n*)nc-Si:H through MoO_x to TCO [21], we assume that a thin MoO_x layer is necessary to enable electrons to cross through it and be collected efficiently. The same thickness is previously reported as the optimum for the HTL stack [25]; hence, no compromise has to be made when implementing it as a blanket layer in IBC solar cells.

Aiming to reduce the PECVD processing time of our device, we also evaluate the influence of (*n*)nc-Si:H thickness on solar cell performance. For this evaluation, we fabricated rear junction FBC-SHJ solar cells (see Figure 1B), which feature (*n*)nc-Si:H/MoO_x stack with PTB. We keep the thickness of MoO_x at the optimal thickness of 1.7 nm (see Figure 2B). We compare the V_{OC}, *FF*, p*FF*, and $R_{s,SunsVoc}$ of solar cells with 10-, 20-, and 50-nm thick (*n*)nc-Si:H in Figure 2C. Among the presented devices, the thinnest (*n*)nc-Si:H enables the best average V_{OC} of 714.2 mV, a gain of 2.4 mV compared with solar cells with 20-nm thick (*n*)nc-Si:H and 1.2 mV compared with the ones with 50-nm thick (*n*)nc-Si:H. This is potentially related to shorter plasma processing that can cause damage to thin (*i*)a-Si:H underneath. With a 50-nm thick layer, field effect passivation plays a more significant role compared with a 20-nm thick layer without additional damage to (*i*)a-Si:H, hence enabling better V_{OC}. However, the specific cause is still under investigation. On the other hand, solar cells with the thickest (*n*)nc-Si:H show the highest *FF* of 82.1% on average, which is related to the lowest $R_{s,SunsVoc}$ enabled by thicker and more conductive (*n*)nc-Si:H [21]. The gain in *FF* is only around $+1.5\%_{abs}$ compared with the devices with 10- and 20-nm thick (*n*)nc-Si:H. Overall, solar cells with three different thicknesses of (*n*)nc-Si:H exhibit relatively similar performance when integrated into the FBC architecture. Considering the potential reduction in PECVD processing time by using thinner layers, we further explore the impact of (*n*)nc-Si:H thickness in IBC solar cells in the following section.

4 | Interdigitated-Back-Contacted Solar Cells

Next, we fabricated IBC-SHJ solar cells with three (*n*)nc-Si:H thicknesses to verify that the device performance is not strongly affected by (*n*)nc-Si:H thickness also in an IBC configuration. All devices feature PTB and a 1.7-nm thick MoO_x layer as optimal for both HTL [25] and ETL stacks. Figure 5 shows the results of IBC-SHJ solar cells with 10-, 20-, and 50-nm thick (*n*)nc-Si:H. Additionally, a summary of the external parameters corresponding to the best solar cell for each condition is provided in Table S1. For all external parameters, devices with thinner (*n*)nc-Si:H exhibit significantly lower performance and greater spreading of the results among fabricated devices. Moreover, *J*–*V* curves of many solar cells with 10-nm thick (*n*)nc-Si:H show an S-shape indicating non-efficient carrier collection (see Figure S4). In the case of solar cells with a 10-nm thick layer, the average V_{OC} is 635.7 mV, which rises to 678.6 mV for cells with a 50-nm thick (*n*)-layer, an absolute gain of above 40 mV. Similarly, J_{SC} increased from 27.3 to 32.5 mA/cm^2 for 20-nm thick (*n*)nc-Si:H and finally to 38.1 mA/cm^2 for the thickest layer. The most significant gain is observed in *FF*, which

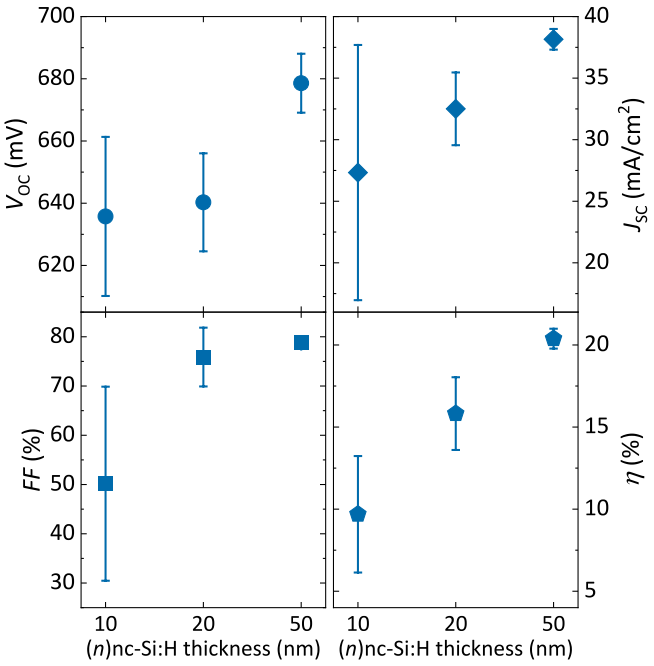

FIGURE 5 | *J*–*V* parameters of IBC-SHJ solar cells with MoO_x blanket layer with different thicknesses of (*n*)nc-Si:H layer. The average values and error bars are based on 21 cells from three wafers for 10-nm thick (*n*)nc-Si:H, 7 cells from one wafer for 20-nm thick (*n*)nc-Si:H, and 7 cells from one wafer for 50-nm thick (*n*)nc-Si:H.

improves by above $15\%_{abs}$ when increasing the thickness from 10 to 20 nm and for an additional $3\%_{abs}$ when implementing 50-nm thick (*n*)nc-Si:H, reaching 78.8% on average. The final average efficiency improves from 9.7% for devices with the thinnest (*n*)-layer up to 20.4% for the ones with the thickest (*n*)-layer, owing to enhancements in all external parameters.

Unlike in the case of FBC-SHJ solar cells, thinner (*n*)nc-Si:H does not ensure optimal cell performance. This limitation cannot be attributed to shunting losses due to the low conductivity of MoO_x [23, 24] and measured shunt resistances reaching 200 kΩcm^2, also for the devices with thin (*n*)nc-Si:H layers. Instead, the likely cause is the low conductivity (i.e., high E_a) of the thin (*n*)-layers [21], which leads to inefficient collection of electrons. The electrons that cannot be efficiently collected are prone to recombination with holes in the gap region, significantly reducing device performance. Overall, these results point to the additional complexity that IBC architecture introduces and the influence of this more complex system on the behavior of independent layers and layer stacks.

In addition to optimizing the ETL stack, we also evaluate two metallization methods in our laboratory. Thus far, all IBC-SHJ cells presented in this work (see Figure 5), as well as the ones in our previous publication [21] have been metallized with a 2-μm thick layer of evaporated Ag. To reduce the resistance of the metal fingers and ensure efficient extraction of the charge carriers, we metallize our devices with a 25-μm thick electroplated Cu [45]. Figure 6 shows the *J*–*V* curves of the best solar cells fabricated with evaporated Ag (in black) and electroplated Cu (in orange). The dash-dotted orange *J*–*V* curve refers to the best solar cell metallized with electroplated Cu manufactured in the same run as the best Ag-based device. It reaches a J_{SC} of 40.59 mA/cm^2, a V_{OC} of 712 mV, a *FF* of 79.87%,

and a conversion efficiency of 23.10%. In Figure S5, we present external quantum efficiency and reflectance curves of this device. Additionally, we measure p*FF* up to 81% and shunt resistance of 200 kΩcm^2. The overall absolute improvement in J_{SC} of 1.31 mA/cm^2, V_{OC} of 25 mV, and 1.77%$_{abs}$ *FF* ultimately led to a 2%$_{abs}$ gain in efficiency. Both solar cells have an area of 4.05 cm^2, feature a pitch size of 300 μm, and follow the same fabrication process with the same layers. Hence, this improvement is solely related to the better extraction of carriers thanks to the thicker and, therefore, less resistive metal electrodes ensuring lower series resistance. This is especially important in IBC architecture as electron and hole collection regions are positioned in close proximity. Namely, in that case, more resistive metal electrodes not only significantly influence the extraction of charge carriers (hence impacting J_{SC} and *FF*) but also potentially increase recombination at the rear side of the solar cells (and limiting V_{OC}) due to the large presence of charges close to electrodes that cannot be extracted [57]. The performance of the Cu-plated IBC solar cells was further improved following the establishment of more stable PECVD conditions and, therefore, improved surface passivation. During such a run, we obtained a 1-ms gain in τ_{eff} corresponding to a 12-mV gain in iV_{OC}, measured after the deposition of (*i*)a-Si:H stack. The *J*–*V* curve of the best solar cell from this run (featuring an area of 4.09 cm^2 and a pitch size of 650 μm) is also reported in Figure 6 (solid orange line). This solar cell showcases a further V_{OC} increase of 12 mV and a 1.17%$_{abs}$ gain in *FF* with respect to the previous best Cu-plated device, achieving a conversion efficiency of 23.59%. The performance of the champion solar cell is, however, slightly impacted by the lower J_{SC} compared with the previous run. This reduction could be attributed to a different pitch size of the two cells. Namely, champion cell design with a larger pitch leads to a larger rear cell area covered by thick (*n*)nc-Si:H (35.3% for 300-μm pitch design versus 37.8% for 650-μm pitch design), possibly causing higher parasitic absorption of long wavelength light. Additionally, any further discrepancy can potentially be related to an unintentionally thinner front SiO_x layer caused by longer exposure to HF during native oxide removal, which can vary across samples [21]. Further investigations are ongoing to better understand the efficiency gain and the reasons behind the reduced J_{SC}.

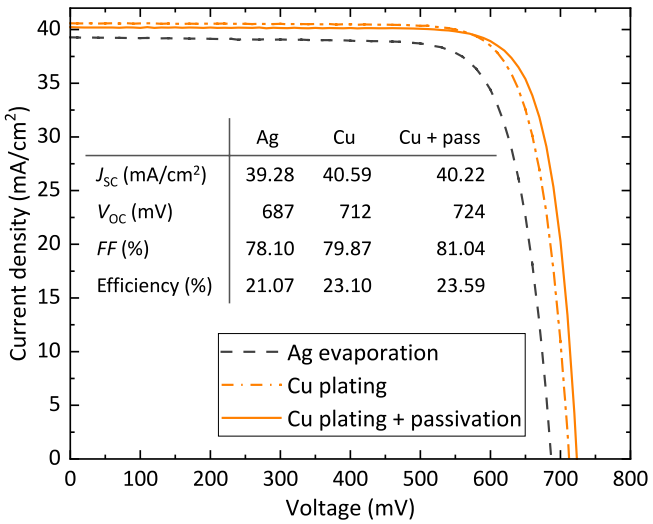

FIGURE 6 | *J*–*V* curves and solar cell parameters of best IBC-SHJ solar cells metallized with evaporated Ag (dashed black line) and electroplated Cu (dash-dotted orange and solid orange lines).

After understanding the collection of charges and addressing the limitation of unoptimized metallization in our devices, we explore opportunities for further improvements of IBC-SHJ solar cells with MoO_x blanket layer. With the improvements in metallization, the remaining J_{SC} discrepancy compared with values reported for high-efficiency IBC solar cells can be attributed to optical losses from the unoptimized front layer stack (consisting of approximately 800-nm thick SiO_x on top of 8-nm thick (*n*)nc-SiO_x:H front surface field in current devices). Removing the (*n*)nc-SiO_x:H window layer and introducing a modulated surface texture [41] or an optimized (double-layer) antireflection coating stack [2, 58–61] is expected to boost J_{SC}. To further improve V_{OC}, we shall follow two main routes. First, we aim to keep fine-tuning the passivation layer stack on the rear side, ensuring compatibility with the more extensive process flowchart required for IBC-SHJ solar cells compared with that of FBC-SHJ solar cells. Meanwhile, we aim to improve the front-side passivation layer stack. Second, we investigate ways to realize the target electrical properties of the (*n*)nc-Si:H layer that concurrently enable a thickness reduction for decreasing processing time and improving charge collection. Finally, by exploring other TCOs with more favorable band alignment with MoO_x and higher mobilities, such as IWO [62], we can further reduce resistive and optical losses. With the proposed improvements, we expect J_{SC} and V_{OC} to increase beyond 41 mA/cm^2 and 725 mV [4, 63], respectively, and *FF* to exceed 82%, anticipating efficiencies close to 24.5% in the short term.

5 | Conclusion

This study presents a comprehensive analysis of electron transport through a novel (*n*)nc-Si:H/MoO_x stack aimed at improving the understanding and performance of IBC-SHJ solar cells with a MoO_x blanket layer.

The initial investigation focuses on the role of PTs (PT and PTB) on the effectiveness of electron transport through this stack. We first evaluated FBC-SHJ solar cells featuring the (*n*)nc-Si:H/MoO_x stack with different treatments applied before MoO_x. V_{OC}, *FF*, and $R_{s,SunsVoc}$ reveal that devices with PTB outperform the ones with PT or without any treatment. Temperature-dependent illuminated *I*–*V* measurements indicate that transport through the stack with PT or PTB is based on direct energy transitions, which result in more efficient electron transport compared with devices without treatments. Supporting HR-TEM and EDX imaging further confirms that PTB treatment leads to a well-confined Mo-rich layer and a thinner oxidic interfacial layer with (*n*)nc-Si:H. Additionally, our investigation into the impact of MoO_x and (*n*)nc-Si:H thickness reveals that a thin MoO_x layer (1.7 nm) delivers optimal performance, while thicker layers increase $R_{s,SunsVoc}$. FBC-SHJ solar cells show little sensitivity to the thickness of (*n*)nc-Si:H, showing comparable results for a thickness range from 10 to 50 nm. However, thinner (*n*)nc-Si:H layers in IBC-SHJ solar cells significantly reduce device performance due to inefficient electron collection and recombination in the gap region. The champion solar cell fabricated with the optimized contact stack, electroplated Cu contacts, and optimized surface passivation achieves a conversion efficiency of 23.59%. Future work targeting (i) enhanced front side optical and passivation scheme, (ii) more conductive (*n*)nc-Si:H and improved passivation, and (iii) choice of a more suitable TCO is

expected to bring the efficiency of such solar cells up to 24.5% in the short term.

Author Contributions

Katarina Kovačević: conceptualization, data curation, investigation, methodology, writing – original draft preparation, visualization, validation. **Yifeng Zhao:** conceptualization, methodology, writing – review and editing, supervision. **Paul Procel:** conceptualization, data curation, investigation, methodology, writing – review and editing, software. **Liqi Cao:** conceptualization, methodology, writing – review and editing. **Miro Zeman:** supervision. **Luana Mazzarella:** conceptualization, methodology, writing – review and editing, supervision. **Olindo Isabella:** conceptualization, writing – review and editing, supervision, funding acquisition, project administration, resources.

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Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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Supporting Information

Additional supporting information can be found online in the Supporting Information section. **Figure S1:** Temperature-dependent illuminated *J-V* characteristics of FBC-SHJ solar cells with (*n*)nc-Si:H/MoO_x stack with (A) PTB, (B) PT, and (C) no PT, and (D) of a reference FBC-SHJ solar cell. **Figure S2:** HAADF and EDX elemental maps of no PT sample (top), PT sample (middle), and PTB sample (bottom). **Figure S3:** Cross-sectional HR-TEM image of ETL stack with PTB showing nc-Si:H, SiO_x, MoO_x and ITO. A 2- to 2.5-nm thick MoO_x layer is highlighted green in the image. **Figure S4:** *J-V* curves of three IBC-SHJ solar cells with 10- (dotted line), 20- (dashed line), and 50-nm (solid line) thick (*n*)nc-Si:H, PTB, and 1.7-nm thick MoO_x. **Table S1:** External parameters of the best solar cells for each variation of the experimental conditions. **Figure S5:** External quantum efficiency (EQE) and reflectance (R) curves of an IBC-SHJ solar cell with Cu electroplated contacts before optimized passivation.