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15.5 Cryo-CMOS Circuits and Systems for Scalable Quantum Computing

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Quantum computing holds the promise to achieve unprecedented computation power and to solve problems today intractable. State-of-the-art quantum processors consist of arrays of quantum bits (qubits) operating at a very low base temperature, typically a few tens of mK, as shown in Fig. 15.5.1 The qubit states degrade naturally after a certain time, upon loss of quantum coherence. For proper operation, an error-correcting loop must be implemented by a classical controller, which, in addition of handling execution of a quantum algorithm, reads the qubit state and performs the required corrections. However, while few qubits (~10) in today's quantum processors can be easily connected to a room-temperature controller, it appears extremely challenging, if not impossible, to manage the thousands of qubits required in practical quantum algorithms [1].

In this paper we propose an integrated controller for quantum processors that can enable such massive interconnections by operating at cryogenic temperatures next to the base temperature (Fig. 15.5.2). We advocate the use of CMOS operating at cryogenic temperatures (cryo-CMOS), thanks to its scalability, reliability, and compactness, properties required for the next generation scalable quantum computers. Moreover, cryo-CMOS circuits and systems could prove to be useful in other domains, wherever low noise is essential, such as metrology, imaging, instrumentation, etc.

Although cryogenic CMOS circuits have been proposed in the past [2,3], extremely demanding performance is required for quantum-processor control. Ultra-low noise and extremely high accuracy are needed to read weak signals from the qubits (few μV or nA over bandwidths of several MHz) and to generate analog control signals that minimize quantum decoherence. We demonstrate three sub-blocks of the controller in Fig.15.5.2: a low-noise amplifier (LNA), an RF oscillator, and a single-photon avalanche diode (SPAD), that have been optimized for cryogenic operation, while ensuring such performance.

The first problem to solve when designing cryo-CMOS circuits is transistor modeling. Fig. 15.5.3 shows the 4K and 300K I_{DS}-V_{DS} characteristics of N- and P-MOS transistors fabricated in 0.16μm and 40nm CMOS. While mobility increases at 4K when compared with 300K, the expected current increase is mitigated by partial substrate freeze-out and other effects. A kink may be observed at higher V_{DS} for older processes (>100nm) and for particular devices such as thick-oxide transistors (Fig. 15.5.3), due to impact ionization at the drain and the ensuing substrate current coupled with substrate resistivity increase leading to a lower threshold voltage [4]. The cryogenic behavior of other devices such as N-well resistors and substrate BJTs also deviates from 300K (Fig. 15.5.3). Although the physical phenomena affecting CMOS devices at cryogenic temperatures have been explained and models proposed for older technologies (> 0.16μm), no standard cryogenic compact model exists in a commercial SPICE simulator. A modified PSP/MOS11 model was developed for the design of the circuit blocks presented here.

CMOS logic cells have been implemented and demonstrated to operate at cryogenic temperatures as demonstrated by a 0.16μm CMOS ring oscillator (Fig 15.5.7) operating from 4K to 300K within a supply range of 0.8-to-1.8V. At 4K the inverter delay is 30ps at 1.8V and increases to 400ps at 0.8V.

A spin qubit can be read out via a charge-sensitive resistive sensor, such as a quantum-point contact at base temperature near the qubit [1]. Its resistance can be remotely monitored by measuring the reflection coefficient at a 50Ω line connected to the sensor. Multiple qubits can be multiplexed by adding frequency-selective matching networks to the sensors. However, due to limited sensor sensitivity (ΔR/R~1%) and because a large power can alter the qubit state, the reflected power is extremely weak (-135dBm in a 1MHz bandwidth per qubit), thus requiring ultra-low-noise read-out. We thus propose a CMOS LNA (Fig.15.5.4), achieving both 50Ω input matching and low noise thanks to the low thermal noise at 4K and to a noise-canceling topology [5]. Simulations using the developed cryogenic CMOS models predict a 0.6K noise temperature (NF=0.009dB) at 4K. While reliable characterization of full performance is currently limited by the cryogenic setup and is still ongoing, a gain above 28dB over a 1.2GHz bandwidth was measured at 4K (Fig.15.5.4). The 0.16μm CMOS LNA (Fig.15.5.7) dissipates 97mW, thus allowing more than 500 qubit channels with power efficiency better than 200μW/qubit.

Logic quantum operations on spin qubits are driven by microwave signals tuned to the qubit resonant frequency (QRF). Nuclear spin in the substrate induces frequency noise in the QRF (~1.9kHz$_{rms}$ for a purified ^{28}Si substrate) that degrades the quantum coherence. To avoid additional degradation, the noise in the CMOS oscillator should be <1.9kHz$_{rms}$, resulting in a phase noise (PN) of <-145dBc/Hz at 10MHz offset from a 6GHz carrier (f_0). We propose to achieve such PN with a class-F oscillator [6] optimized for cryogenic temperatures (Fig. 15.5.5). The PN of an LC oscillator is at minimum when the tank has auxiliary resonance at $3f_0$ while simultaneously its common-mode resonates at $2f_0$. As a result, both 1/f noise up-conversion and thermal-to-phase noise sensitivity of core devices (thick-oxide MOS $M_{1,2}$) significantly decrease. To avoid $M_{1,2}$ entering a possible kink region and thus loading the tank, the oscillation swing is limited at $M_{1,2}$ drains. However, a 1:2 step-up transformer is used to boost the swing at $M_{1,2}$ gates, thus improving the oscillator's PN. The 12mW 40nm CMOS oscillator (Fig.15.5.7) shows a 7% shift in its 25% tuning range at 4K. Although its 1/f^3 PN corner increases at cryogenic temperatures, the PN in the 20dB/dec region improves almost linearly with decreasing temperature, thus meeting the required specifications.

The SPAD is a p-n junction biased above breakdown by voltage V_{ex}, so as to operate in Geiger mode, yielding infinite optical gain and thus generating a digital signal upon detection of a single photon. The 0.18μm CMOS SPAD (Fig. 15.5.7) has a sensitivity range of 350-to-800nm, thus covering the needs for qubits implemented as NV centers in diamond, that are interfaced with waveguides operating from 500nm to 1550nm. The SPAD was designed and tested for use at 77K. The SPAD dark count rate (DCR) and breakdown voltage are shown in Fig. 15.5.6. The device reaches a photon detection probability of 28% at 500nm and an excess bias of 4V, and it is amenable to integration in large arrays with variable aspect ratio, thus well adapting to the needs of optical interfaces of 1D and 2D qubit arrays.

The demonstrated performance shows that cryo-CMOS is a viable technology for the implementation of the proposed cryogenic multi-channel classical interface for quantum processors, thus paving the way to the realization of very large scale qubit arrays for viable quantum computing applications.

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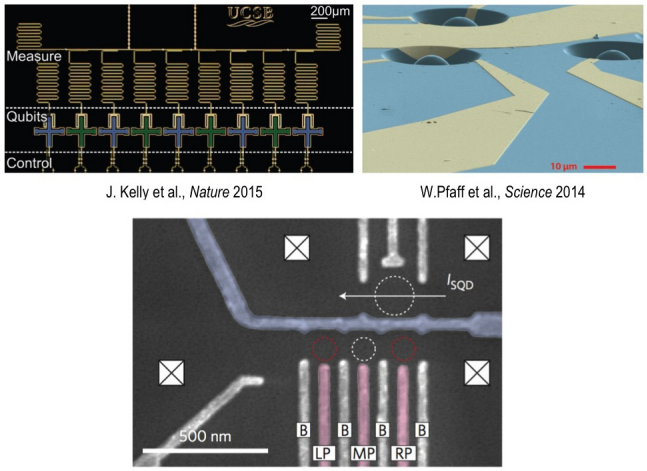


Figure 15.5.1: State-of-the-art quantum processors: 9-qubits transmon array (top left); 3 NV-center qubits (top right); 3-quantum-dot array for spin qubits (bottom).

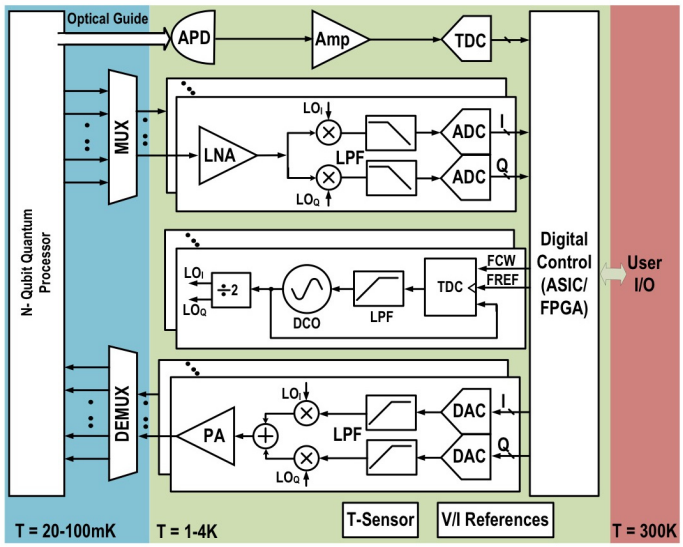


Figure 15.5.2: Multi-channel classical interface to a quantum processor.

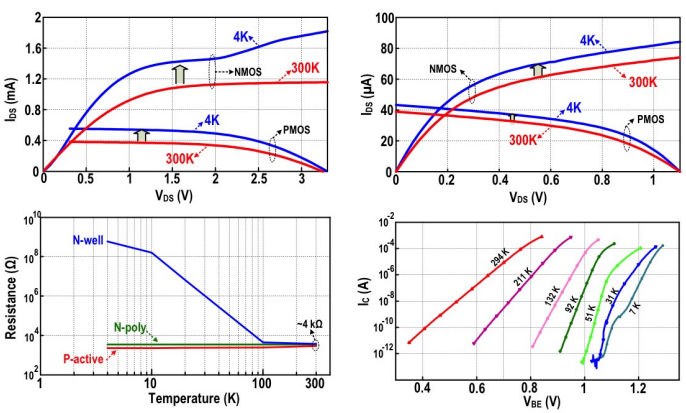


Figure 15.5.3: I-V vs. T: thick-oxide 0.16μm CMOS transistors (top left); thin-oxide 40nm CMOS transistors (top right); resistors (bottom left) and parasitic substrate NPN (bottom right) in 0.16μm CMOS.

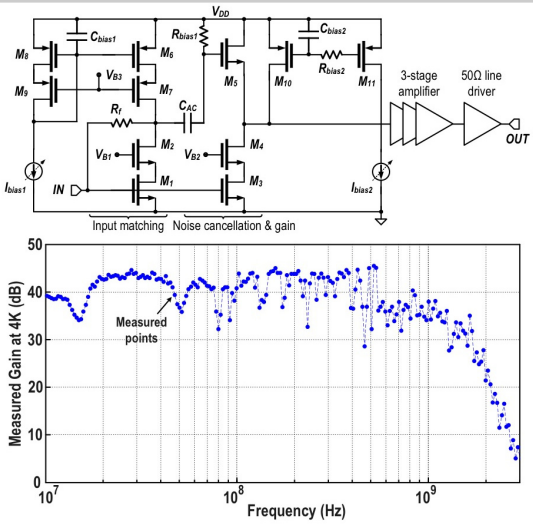


Figure 15.5.4: Low-noise-amplifier schematic (top). Measured gain at 4K (bottom).

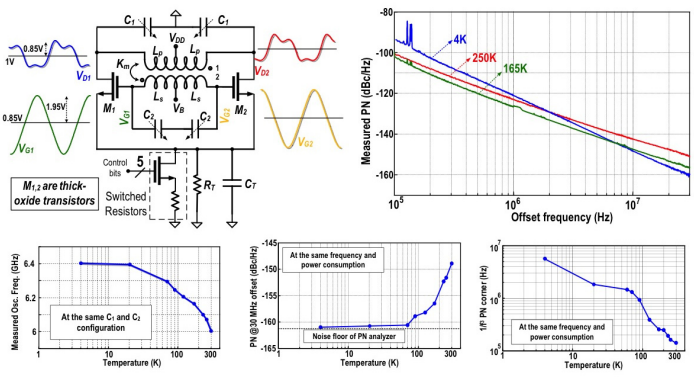
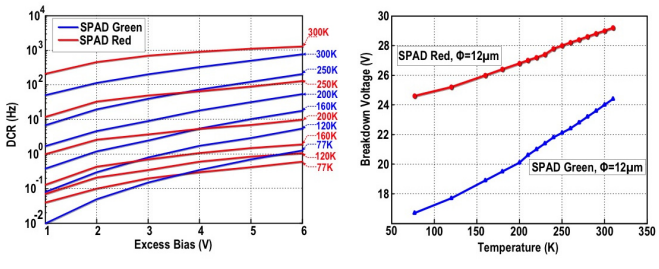


Figure 15.5.5: Class-F oscillator with simulated waveforms (top left). Measured PN at 6.2GHz (top right). Measured oscillation frequency, PN at 30MHz offset, and oscillator 1/f³ PN corner vs. T (bottom).



Parameter	This work (SPAD green)	Cova et al. 1981	Webster et al. 2012	Mandai et al. 2012	Unit
Active diameter	12	8	10	12	μm
Breakdown voltage @ 300K	24	20	19.7	35.7	V
DCR density @V_{ex}=2V @ 300K	0.88	3.98	3.2-64.5	0.15	Hz/μm²
DCR density @V_{ex}=2V @ 77K	0.00035	-	-	-	Hz/μm²
PDP peak @V_{ex}=4V (@ λ)	28 (500nm)	38 (550nm)	36 (600nm)	47.6 (480nm)	%
FWHM Time Jitter (@laser λ)	115.79 (785nm) (V_{ex}=6V)	< 60 (654nm)	165 (790nm)	86 (637nm)	ps
Afterpulsing probability	< 1.5	< 4	50	0.3	%

Figure 15.5.6: Measured data for two cryo-SPADs (blue for higher green sensitivity, red for higher red sensitivity): dark count rate (top left) and breakdown voltage (top right) vs. T. Summary (bottom).

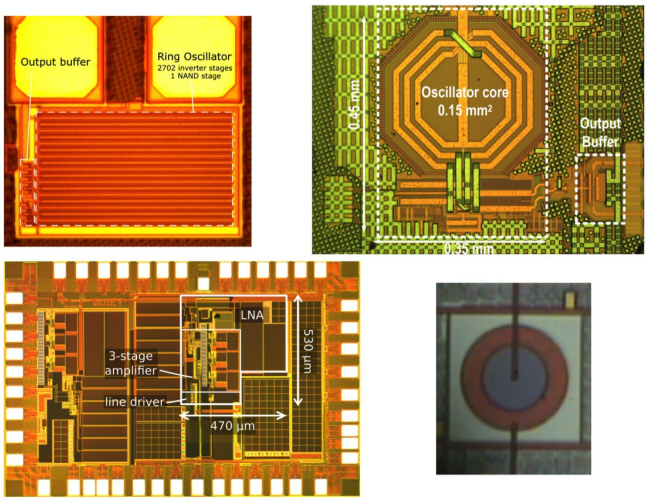


Figure 15.5.7: Micrographs: 0.16µm CMOS ring oscillator for process characterization (top left); 40nm CMOS class-F oscillator (top right); 0.16µm CMOS LNA (bottom left); 0.18µm CMOS 12µm SPAD (bottom right).

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