A Sub-1-V Capacitively-Biased Voltage Reference with an Auto-Zeroed Buffer and a TC of 18-ppm/° C

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A Sub-1-V Capacitively-Biased Voltage Reference With an Auto-Zeroed Buffer and a TC of 18-ppm/°C

Heungsik Eum, *Student Member, IEEE*, Kofi A. A. Makinwa, *Fellow, IEEE*, Inhee Lee, *Senior Member, IEEE*, and Youngcheol Chae, *Senior Member, IEEE*

***Abstract*—This brief presents a capacitively-biased CMOS voltage reference, which can operate from a sub-1V supply while achieving a low temperature coefficient (TC) and a competitive power-supply rejection ratio (PSRR). The reference voltage is generated by a capacitive bias circuit that provides a well-defined proportional-to-absolute-temperature (PTAT) bias current for a ΔV_{th} type reference that consists of two stacked MOSFETs with different threshold voltages. The generated output voltage is sampled by an auto-zeroed (AZ) buffer, which can drive capacitive loads up to 2 nF. Fabricated in a 65 nm CMOS process, the prototype voltage reference occupies 0.058 mm^2, including the AZ buffer and an on-chip timing generator. It outputs a reference voltage of 204.1 mV with a minimum supply voltage of 0.7 V. It achieves a TC of 18 ppm/°C from −40 °C to 85 °C and a PSRR of −75 dB at 100 Hz with only 200 μV ripple.**

***Index Terms*—CMOS voltage reference, capacitively-bias circuit, sub-threshold voltage reference, CMOS analog design, sub-1-V, high-precision circuits.**

I. Introduction

MOST electronic systems require voltage references that must be stable over process, voltage, and temperatures (PVT) variations [1], [2], [3]. The increasing interest in battery-operated portable applications has led to a demand for low-power and low-voltage references. As CMOS processes have scaled down, however, their supply voltage has scaled accordingly. Therefore, a key challenge in scaled CMOS processes is the design of accurate voltage references that can operate at low supply voltages.

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Heungsik Eum and Youngcheol Chae are with the Department of Electrical and Electronics Engineering, Yonsei University, Seoul 03722, South Korea (e-mail: ychae@yonsei.ac.kr).

Kofi A. A. Makinwa is with the Microelectronics Department, Delft University of Technology, 2628 Delft, The Netherlands.

Inhee Lee is with the Department of Electrical and Computer Engineering, University of Pittsburgh, Pittsburgh, PA 15260 USA.

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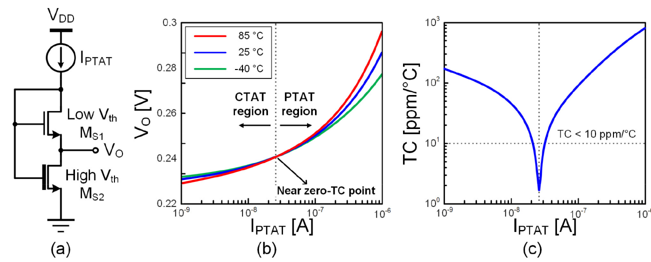

Fig. 1. (a) ΔV_{th} voltage reference using I_{PTAT} bias current and (b) simulated output voltage V_O and (c) TC versus I_{PTAT}.

Bandgap references (BGRs) based on BJTs or diodes are well-known for their robustness to PVT variations [4]. They accomplish this by summing proportional-to-absolute-temperature (PTAT) voltages and complementary-to-absolute-temperature (CTAT) voltages generated with the help of precisely biased BJTs [5]. However, despite their accuracy, conventional BGRs require a high supply voltage, making them difficult to use in advanced CMOS processes. Switched-capacitor (SC) techniques can then be employed to realize low-voltage BGRs, which only consume a few tens of nW [6], [7], [8], [9]. Compared to traditional BGRs, however, such references exhibit quite high temperature coefficients (TCs >30 ppm/°C). Recently, a curvature correction scheme improves TCs even at a low supply voltage, along with the SC techniques [10]. However, the numerous switches in the scheme increase its complexity. Furthermore, high-quality BJTs are not always available in advanced CMOS processes. Alternatively, as shown in Fig. 1(a), so-called ΔVth voltage references can also be made, which output the threshold voltage difference of two different MOSFETs. They are also quite PVT robust and can operate from low supply voltages while consuming low power, ranging from a few pW to tens of nW [11], [12], [13], [14], [15], [16]. However, their biasing schemes are not defined well, which causes relatively high TCs (>50 ppm/°C).

This brief presents a sub-1-V ΔVth voltage reference that is biased by a PTAT current generated by a SC bias circuit. It allows the generation of a well-defined PTAT current, which enables the proposed voltage reference core to achieve a precise voltage with a low TC and competitive PSRR. The reference voltage is subsequently sampled by an auto-zeroed (AZ) buffer that has two output stages, which can then drive

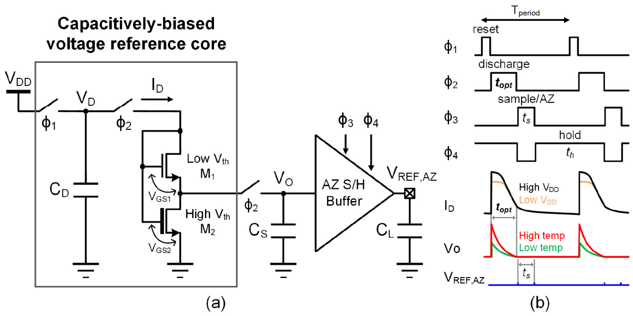

Fig. 2. (a) The proposed capacitively-biased voltage reference and (b) its timing diagram.

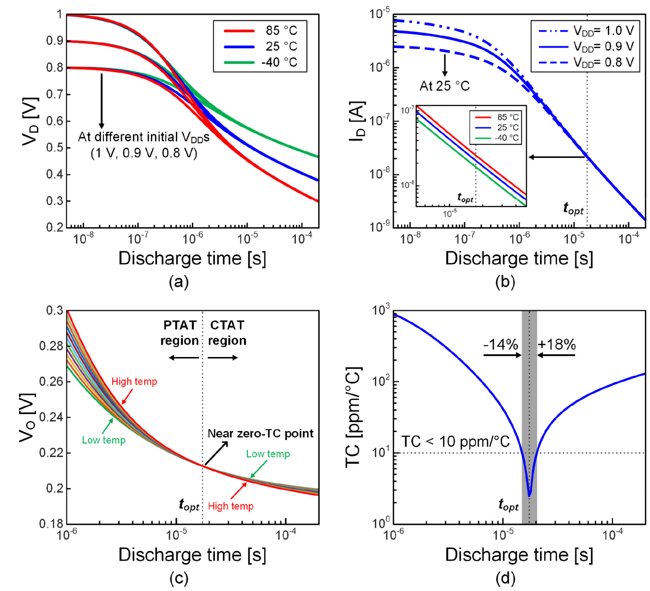

Fig. 3. Simulation results of the core of the proposed reference: (a) Diode voltage V_D, (b) discharge current I_D, (c) output voltage V_O, and (d) TC versus discharge time.

significant capacitive loads with minimal ripples, such as the reference buffers of ADCs. Fabricated in a 65 nm CMOS process, the proposed voltage reference generates an output of 204.1 mV from a minimum supply voltage of 0.7 V. It achieves a TC of 18 ppm/°C from −45 to 85 °C and a power supply rejection ratio (PSRR) of −75 dB at 100 Hz.

II. Proposed Voltage Reference

A. Principle of PTAT-Biased ΔVth Voltage Reference

Fig. 1(a) illustrates the simplified schematic of the proposed voltage reference, which relies on the ΔV_{th} between a thin-oxide (low V_{th}) transistor M_{S1} and a thick-oxide (high V_{th}) transistor M_{S2}. Biased by a PTAT current (I_{PTAT}), the stacked combination of M_{S1} and M_{S2} generates an output voltage V_O $=V_{GS2}$-V_{GS1}, whose temperature dependence is determined by I_{PTAT} and by the characteristics of the two transistors. Fig. 1(b)∼(c) shows the simulated V_O at three different temperatures as a function of I_{PTAT}. It can be seen that the temperature dependence of V_O changes from CTAT to PTAT depending on the magnitude of I_{PTAT}. At a certain I_{PTAT}, V_O exhibits a near zero-TC, as can be seen in Fig. 1(c). However, in the chosen 65 nm CMOS process, this current is typically in the order of a few tens of nA, making its precise generation challenging. To address this problem, inspired by [17], [18], a SC- biasing scheme is proposed in this brief.

B. Proposed Capacitively-Biased Voltage Reference

Fig. 2 shows the proposed capacitively-biased voltage reference and its timing diagram. One operation period T_{Period} (=80 μs) and a capacitor C_D (=1.9 pF) are selected to make the leakage on C_S (=0.75 pF) negligible. During a reset phase (ϕ_1), C_D is initially charged to the supply voltage V_{DD}. In the subsequent discharge phase (ϕ_2), C_D is discharged via the stacked diode-connected MOSFETs, resulting in a time-varying V_O (=V_{GS2}-V_{GS1}). After an initial transient, the stacked MOSFETs will enter the weak inversion region, and the voltage V_D, along with its discharging bias current I_D, will be solely determined by their exponential I-V characteristic, regardless of the initial V_{DD}. Fig. 3(a) shows that after a brief (here, after 1 μs), V_D decreases logarithmically as a function of CTAT. As depicted in Fig. 3(b), I_D becomes an approximately PTAT current, given by mC_DV_T/t, where m is the slope factor of M_2, V_T is the thermal voltage, and t is the discharge time. The simulation results of V_O versus the discharge time are shown in Fig. 3(c)∼(d). As I_D decreases, the temperature dependency of V_O changes from PTAT to CTAT, and a near zero-TC point exists at t_{opt} in the middle. And then the resulting V_O can then be sampled by disconnecting C_S. As shown in Fig. 2, an AZ S/H buffer with high input impedance and low offset is employed to drive an external load. The AZ S/H buffer samples V_O during a sample/AZ phase (ϕ_3) and generates a low-offset copy $V_{REF,AZ}$ during a hold phase (ϕ_4). All the pulses are generated by an on-chip timing generator, enabling the voltage reference from an external clock.

The two different transistors in Fig. 2, M_1 and M_2, are used to generate ΔV_{th}. The sizes of M_1 (W/L_1=10/1 μm/μm) and M_2 (W/L_2=4.2/8.4 μm/μm) are selected to minimize the leakage of M_1 and optimize the TC of V_O. In simulation, the lowest TC of ∼2.7 ppm/°C is achieved at t_{opt} (=17.5 μs) generating V_O of about 0.2 V. The TC remains below 10 ppm/°C even when the discharge time varies over a wide range (−14% to +18%) around t_{opt}. Monte-Carlo simulations show that the corresponding variation of V_O is approximately ±3.6 mV (±1.8%). As shown in Fig. 3(b), at t_{opt}, the required I_D is in the order of a few tens of nA (17.5, 21.4, and 25.1 nA at −40, 25, and 85 °C, respectively) even with a V_{DD} variation from 0.8 to 1 V. These results indicate that the reference core can be operated at a sub-1-V supply, and that the TC of V_O is robust to variations in the discharge time.

C. Auto-Zeroed Sample-and-Hold Buffer

As shown in Fig. 4, the output node (O_1) of the buffer with a single output stage switches between V_O and V_O+V_{OS}, causing large ripples at the boundary of two phases. To suppress the ripples, splitting it into two output stages is more effective, where the output stages maintain each output

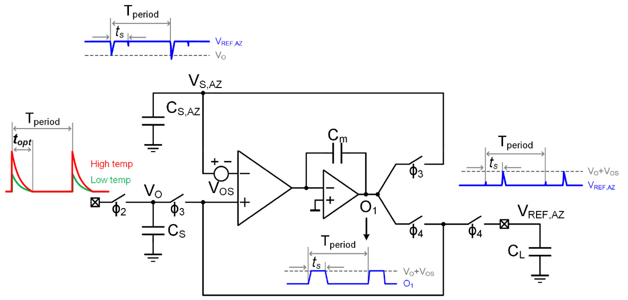

Fig. 4. Schematic of the auto-zeroed sample-and-hold buffer with single output stage.

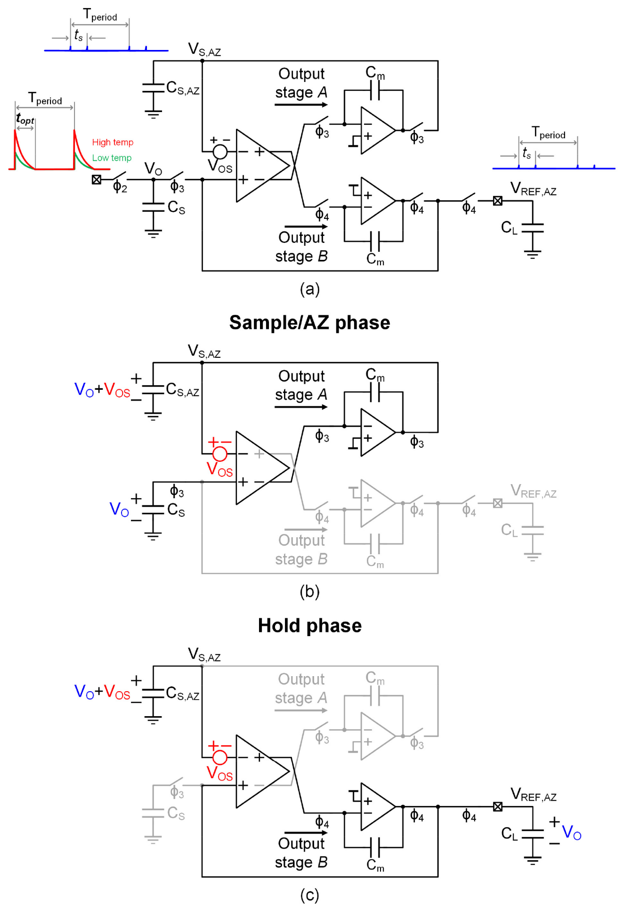

Fig. 5. (a) Schematic of the proposed auto-zeroed sample-and-hold buffer, and operation in (b) sample/AZ phase and (c) hold phase.

voltage. Fig. 5 shows the proposed buffer that consists of a single input stage that alternately drives two output stages. While one output stage (*A*) drives an on-chip sample/AZ capacitor $C_{S,AZ}$ (=3.8 pF), which copies V_O during the sample/AZ phase, the other output stage (*B*) drives the load capacitor (C_L). During the sample/AZ phase (ϕ_3), the buffer is configured for unity gain via the first output stage (*A*), and thus stores V_O+V_{OS} on $C_{S,AZ}$, where V_{OS} is the buffer's offset voltage. In the subsequent hold phase (ϕ_4), the buffer is configured to unity gain via the second output stage (*B*), canceling its offset and transferring V_O to the output capacitive load up to 2 nF. To achieve low-offset, the input stage has a

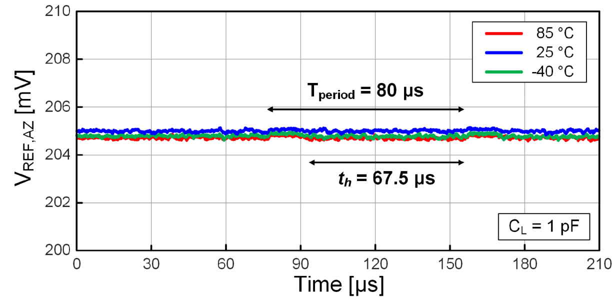

Fig. 6. Measured $V_{REF,AZ}$ at −40, 25, and 85 °C.

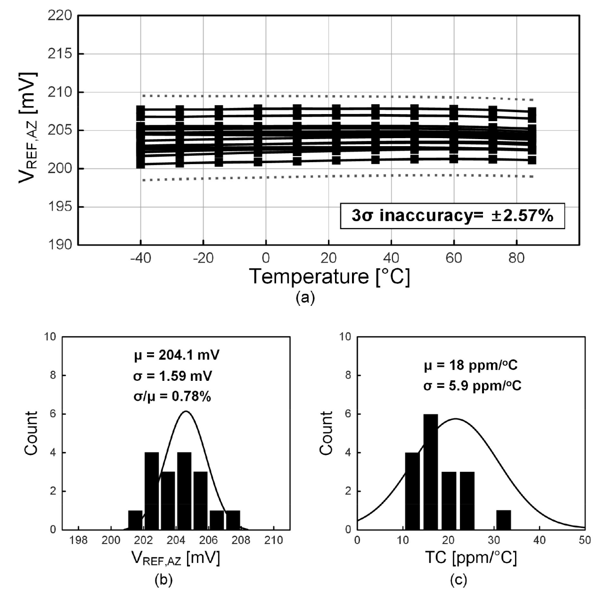

Fig. 7. (a) Measured inaccuracy, and distribution of (b) $V_{REF,AZ}$ and (c) TC at t_{opt}.

gain of >53 dB over PVT. The amplifier's open-loop gain is >85 dB, ensuring that its initial offset can be suppressed to the micro-volt level. The buffer's simulated offset voltage remains within 10 μV over PVT, which is negligible compared to the expected spread in V_O. At room temperature, the integrated noise of the buffer is 50 μV_{rms}.

III. Measurement Results

The prototype reference is fabricated in a 65 nm CMOS process. An external reference clock is employed for testing. The measurements were carried out on 17 samples in ceramic DIL packages. As shown in Fig. 6, using a load capacitor C_L of 1 pF and a hold time t_h of 67.5 μs, the measured $V_{REF,AZ}$ has an output ripple of 200 μV caused by the residual charge injection of switches in the S/H buffer. The distribution of $V_{REF,AZ}$ is depicted in Fig. 7. The measured 3σ-inaccuracy is ±2.57% at t_{opt}=17.5 μs. The measured mean (μ) and standard deviation (σ) of $V_{REF,AZ}$ are 204.1 mV and 1.59 mV, respectively, corresponding to a σ/μ ratio of 0.78%. The measured TC is 18 ppm/°C with a spread of 5.9 ppm/°C. To assess its robustness to timing errors, the distribution of $V_{REF,AZ}$ is also measured at 0.9t_{opt} and 1.1t_{opt}, as shown in Fig. 8. The 3σ-inaccuracy and the σ/μ ratio remain consistent

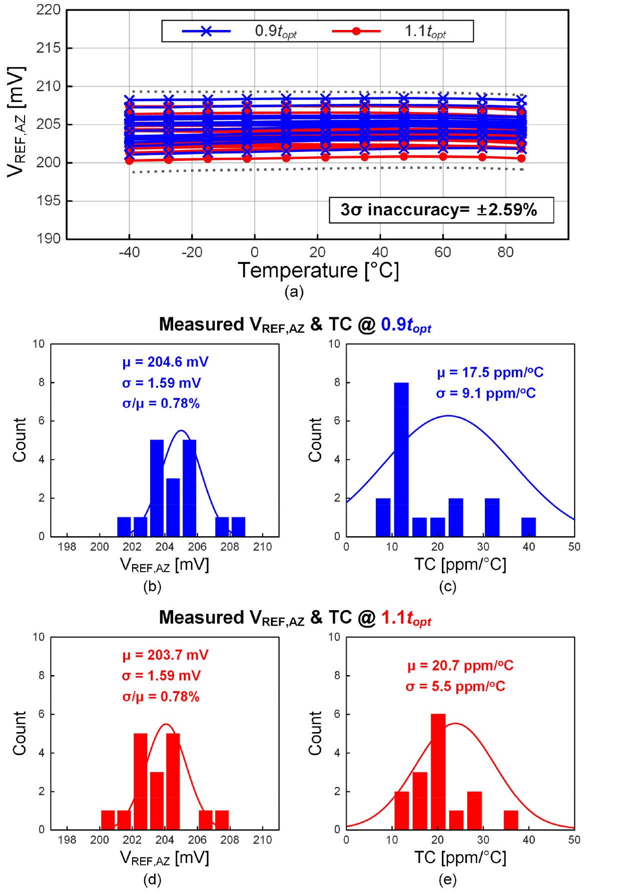

Fig. 8. (a) Measured inaccuracy, distribution of (b) $V_{REF,AZ}$ and (c) TC at 0.9t_{opt}, and distribution of (d) $V_{REF,AZ}$ and (e) TC at 1.1 t_{opt}.

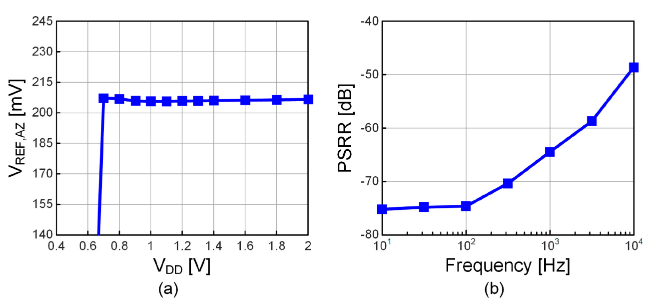

Fig. 9. (a) Measured $V_{REF,AZ}$ versus V_{DD} and (b) PSRR.

at ±2.59% and 0.78%, respectively. Although the TC and $V_{REF,AZ}$ vary slightly by 3.2 ppm/°C and 0.9 mV, respectively, these results confirm the reference's robustness to timing variations.

As shown in Fig. 9(a), the reference can be operated from supply voltages ranging from 0.7 to 2 V. In Fig. 9(b), a measured PSRR of −75 dB is attained at 100 Hz. Fig. 10 presents the measured noise spectrum, which shows that the total integrated noise from 1 Hz to 6.25 kHz is 85.6 μV_{rms} mainly limited by the sampling noise of C_S (=0.75 pF). Under a 0.8 V supply at 25 °C, the power consumption including the buffer and the timing generator is 10 μW, chosen to drive external loads and accommodate AC performance assessment of the reference core precisely under a wide range of test

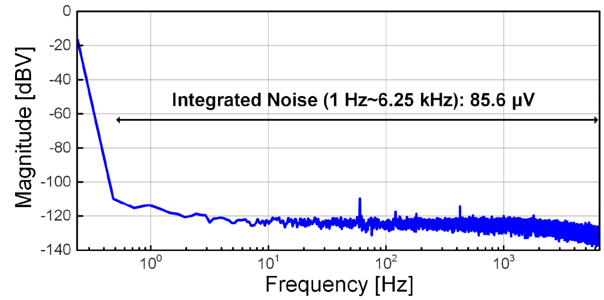

Fig. 10. Measured output noise spectrum.

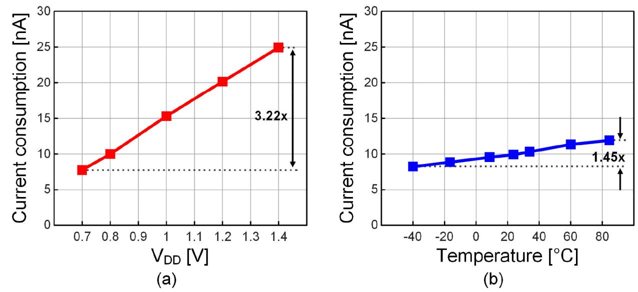

Fig. 11. Current consumption of the reference core at different (a) supply voltages and (b) temperatures.

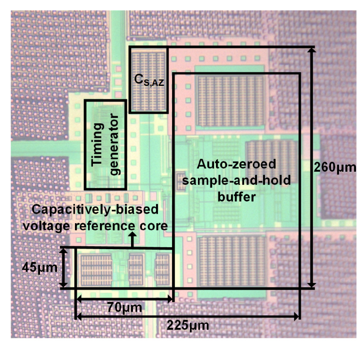

Fig. 12. Chip micrograph.

conditions. Fig. 11 shows that the reference core's current consumption increases by a factor of 3.22 as the supply voltage ranges from 0.7 to 1.4 V. Also, the current consumption varies by a factor of 1.45 from −40 °C to 85 °C, which is significantly smaller than leakage-based voltage reference (300× in [12]). Fig. 12 shows the chip micrograph that occupies a core area of 3,150 μm^2 and a total area of 0.058 mm^2.

Table I provides performance summary and comparison to previous sub-1-V SC-based references. This brief provides the lowest TC and a competitive PSRR with small ripples compared to prior sub-1-V references based on BJT [6], [7], [9], ΔVth [13], and diode [18]. Furthermore, due to the SC technique and its simplicity, it is also suitable for IoT applications, similar to [9].

IV. Conclusion

This brief presents a sub-1V CMOS voltage reference. Thanks to its capacitively-biased ΔV_{th} reference architecture, compared with prior sub-1-V SC-based voltage references,

TABLE I
PERFORMANCE SUMMARY AND COMPARISON TO PREVIOUS SC-BASED REFERENCES

Publication	**This Work**	[6]	[7]	[13]	[9]	[18]
Technology	**65nm**	130nm	130nm	65nm	65nm	16nm
Reference Core	**ΔV_{th}**	BJT	BJT	ΔV_{th}	BJT	Diode
Including buffer	**Yes**	Yes	No	No	No	No
Min. V_{DD} [V]	**0.7**	0.75	0.5	0.62	0.5	0.85
Temp. range [°C]	**-40 to 85**	-20 to 85	0 to 80	-25 to 110	-40 to 120	-20 to 110
TC (μ) [ppm/°C]	**18**	40	75†	108	38	< 52
V_{REF} [mV]	**204.1**	256	500	389.9	503	370
σ/μ [%]	**0.78**	1	0.67	1	0.46	0.24
Output ripple	**200μV**	20mV	50μV	100μV††	200μV††	-
# of chips	**17**	180	6	15	10	10
PSRR @low [dB]	**-75**	-86	-40	-62	-50	-49
Core power [nW]	**8**	15 - 20	19.7	25	24	18
Total power [nW]	**10,000**	170	32			388
Core area [μm²]	**3,150**	20,000†††	26,400	77,000	42,500	1,680
Total area [μm²]	**58,500**	70,000				

† Best TC ††Simulated †††Estimated

the proposed voltage reference achieves the lowest TC of 18 ppm/°C, which is also robust to its t_{opt} variations. It also provides 204.1 mV at a minimal supply voltage of 0.7 V and features a PSRR of −75 dB at 100 Hz, while maintaining a core power of 8 nW and occupying only a core area of 3,150 μm^2. An AZ S/H buffer is used to drive external (capacitive) loads with low-offset and only 200 μV of output ripple.

APPENDIX

THEORETICAL ANALYSIS OF THE PROPOSED VOLTAGE REFERENCE CORE

In this section, the proposed voltage reference during the discharge phase is theoretically analyzed. To simplify the expression, the derivation with partial differentiation is omitted. Assuming $V_{DS} >> V_T$, its drain current is expressed by

$$I_D = \mu C_{DEP}\left(\frac{W}{L}\right)V_T^2 exp\left(\frac{V_{GS}-V_{TH}}{mV_T}\right) = I_O exp\left(\frac{V_{GS}-V_{TH}}{mV_T}\right), \quad (1)$$

where μ is the carrier mobility, C_{DEP} is the depletion capacitance, W and L are the width and length of the NMOS respectively, V_T is the thermal voltage, V_{GS} and V_{TH} are the gate-source voltage and threshold voltage of the NMOS respectively, and m is the slope factor of the transistor. The capacitor discharge with diode-connected NMOS (M_2) in Fig. 2 is approximately expressed by

$$V_{GS2}(t) = -m_2 V_T ln\left(\frac{I_{O2}t}{C_D m_2 V_T}\right) + V_{TH2}. \quad (2)$$

Applying (2) to (1), the capacitive bias circuit generates a V_{DD}-insensitive current after a short time and is expressed as

$$I_D = \frac{C_D m_2 V_T}{t}. \quad (3)$$

Finally, considering V_O=V_{GS2}-V_{GS1} with the same I_D, the output voltage V_O can be given by

$$V_O(t) = (m_1 - m_2)V_T \ln\left(\frac{I_{O2}t}{C_D m_2 V_T}\right) + m_1 V_T \ln\left(\frac{I_{O1}}{I_{O2}}\right) + \Delta V_{TH}. \quad (4)$$

The first term has CTAT characteristics that vary with the discharge time t, while the other terms have time-invariant PTAT characteristics. With the discharge time, the thermal property of V_O changes from PTAT to CTAT, and there is a zero-TC point of V_O at t_{opt} in the middle. As a result, V_O can be expressed as

$$V_O(t_{opt}) = V_{TH2} - V_{TH1}. \quad (5)$$

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