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Fully Integrated Ultrasound Power Receiver for Multi-Piezo Implants with Random Phase Offset

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***Abstract*— A single transmitter source can power multiple ultrasound piezoelectric transducers to enhance the harvested power; however, the received ultrasonic signals vary in phase and amplitude across each element. This paper introduces a fully integrated, high-frequency SSHC rectifier tailored for miniaturized multi-piezo implants to efficiently harvest power at variable phase offsets with a compact form factor. The design incorporates a novel phase-splicing flipping capacitor-sharing technique between all four ultrasound piezoelectric transducers to improve area efficiency. The proposed 4-stage SSHC rectifier can harvest 5.94x more power than a full bridge rectifier operating at a high ultrasonic excitation frequency of 780 kHz. The proposed system was designed using 180-nm BCD process technology for a 2x2 piezoelectric transducer array, with each element featuring an internal capacitor (C_P) of 63.7pF.**

***Index Terms*— Implantable Medical Devices (IMDs), Multi-Piezo implants, Synchronized switch harvesting on Capacitors (SSHC), Ultrasound piezoelectric transducers (US-PT).**

I. Introduction

Implantable medical devices (IMDs) enable key advancements in medical care, yet their invasiveness remains a major limitation. Wireless power transfer enables safer, smaller, and less invasive IMDs. Specifically, ultrasound (US) power transfer has the potential to allow miniaturized deep implants (Fig. 1(a)) since US suffers less tissue attenuation than electromagnetic waves. However, US waves are also attenuated as they propagate through biological tissues reducing power density collected at the receiver when attempting to reach deep-seated targets within the body.

One approach to address this issue is to increase the area of the receiver transducer either by increasing the dimension of the transducer or incorporating an array of multiple transducers. Composite array configurations, commonly employed in medical ultrasound imaging, have demonstrated higher coupling factors than single PTs, making them ideal candidates for energy harvesting applications [1-2]. Additionally, flexible transducer arrays offer improved directional sensitivity, which is particularly beneficial when the embedded implants are subject to movement due to tissue displacement. Notably, the amplitude and phase of the received ultrasound signals may vary across each element based on the sonication angle and element spacing (Fig. 1(b)).

The voltage produced by the PT harvester needs to be rectified before it can be used to power other circuits. A full-bridge rectifier (FBR) is commonly employed in US-based power harvesting systems due to its simplicity and reliability

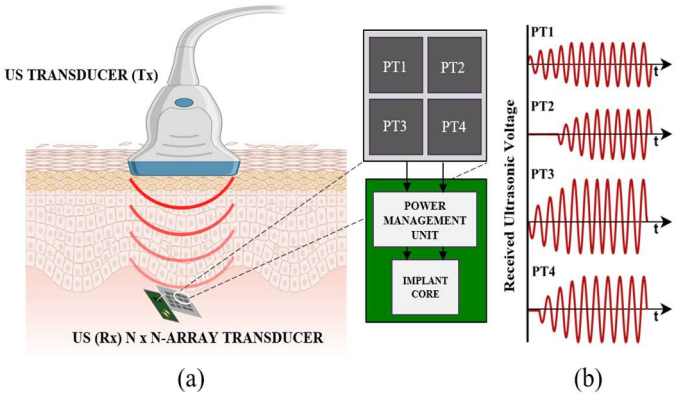

Fig. 1. (a) Conceptual schematic of a US WPT link for powering multi-PT (Rx) implants with a zoomed-in view of 4 elements; (b) Received ultrasound voltage varying in amplitude and phase across each element

[3-6]. However, its power output is limited by charge loss during the charging and discharging of the intrinsic capacitor of the PT (C_P).

To enhance output efficiency, certain inductor-based active bias-flip rectifiers were examined at low vibrational frequencies, typically in the range of a few hundred Hz, to aid in flipping the voltage across C_P by forming an RLC loop [7-8]. However, inductors are not preferred in biomedical applications due to their electromagnetic interference (EMI), and restrictions in miniaturization. The inductorless synchronized switch harvesting on capacitors (SSHC) rectifier designs presented in [9-12] address this issue but necessitate either multiple flying capacitor stages or capacitors larger than C_P to effectively substitute inductors.

In multi-piezo US applications, the superposition of the harvested signals can lead to a destructive interference effect and reduce the output power. Very few low-frequency interface circuits have been developed to convert the multiple AC inputs from a multi-piezo array configuration addressing the random phase offsets across elements, and these are all inductor-based [13-15]. Directly employing one SSHC rectifier for each PT element results in designs whose area is predominantly occupied by an extensive array of flying capacitors making it hard to integrate them on-chip.

This paper proposes a high-frequency SSHC rectifier designed for multi-piezo arrays that aim to share the flying capacitors across all elements within the array. The design introduces a novel phase-splicing (PS) technique that enables shared capacitor access while minimizing the total on-chip

capacitance, effectively resolving conflicts arising from unpredictable phase offsets. This modular design is also readily scalable to accommodate larger-scale US-PT arrays.

The organization of this paper is as follows: Section II outlines the proposed rectifier design and the PS technique. Section III details the circuit implementation. Section IV presents the analysis of the simulation results for the proposed system. Finally, Section V concludes the paper.

II. Multi-Input SSHC Rectifier With Phase-Splicing Technique

A. Traditional SSHC rectifier used for a single-element

Theoretically, the flipping efficiency in typical k-stage SSHC rectifiers for a single element, assuming that all flying capacitors are equal ($C_1 = C_2 = \cdots = C_k$), is given by [11-12],

$$\eta_f = \frac{kC_k}{C_P + (k+1)C_k} \quad (1)$$

where k is the number of flying capacitors used in an SSHC rectifier, C_k is the capacitance of each flying capacitor, and C_P is the capacitor of the PT. When $C_k = C_P$, the corresponding η_f of a four-stage SSHC rectifier is 66.7%.

In a 4-piezo array, achieving an overall efficiency of 66.7% requires 16 flying capacitors. Furthermore, it can be inferred that the same efficiency can be achieved with a 2-stage flipping rectifier if $C_k \sim 100C_P$, which is considerably larger for on-chip integration, even considering the small inherent capacitance of US-PTs [12].

A typical 4-stage SSHC rectifier requires 9 switching signal phases for a single PT (Fig. 2(a)) [11]. Each phase needs to be large enough to ensure the complete charging and discharging of C_P, while also being constrained to ensure that the overall flipping time remains within 10% of the vibration period, to avoid excessive energy wasting.

The flipping process consists of three essential stages:

i) Dumping stage, where the charge is transferred from C_P to C_{fly1}, C_{fly2}, C_{fly3} and C_{fly4} across 4 distinct phases.

ii) Clearing stage, where any residual charge in C_P is discharged in a single phase.

iii) Recharging stage, where C_P is replenished by receiving charge from C_{fly4}, C_{fly3}, C_{fly2} and C_{fly1} in reverse order and with reversed polarity, completing the flipping sequence over 4 phases. This means that, in this 9-phase flipping sequence a single flying capacitor is accessed twice. C_{fly1} is accessed in phase-1 and phase-9, C_{fly2} is accessed in phase-2 and phase-8, and so on. Phase-5 corresponds to the clearing stage that requires no capacitors.

B. Proposed design with phase-splicing technique

To optimize the performance of multiple PT elements, it is essential to address the phase offsets between them. One straightforward approach is to rectify the piezo voltage of each element individually, followed by integrating the power from each channel, which also offers greater versatility. The same approach is used in this design due to its simplicity (Fig.2(b)).

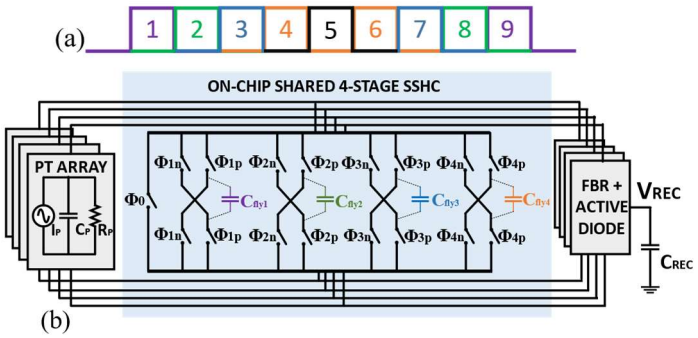

Fig. 2. (a) 9-phase flipping sequence for 4-stage SSHC (b) System overview of the proposed design

The proposed system utilizes just four flying capacitors, with $C_k = C_P$ for all four elements in the array to achieve an overall efficiency of 66.7%. In a multi-piezo array with arbitrary phase offsets, the flipping time is uncertain, posing a significant challenge, especially when the flying capacitors need to be shared among the elements. More than one element may require simultaneous access to a shared capacitor during overlapping phases, leading to potential contention for capacitor access. If the flying capacitors are not sufficiently large, such simultaneous access can reduce flipping efficiency; however, increasing the capacitor size compromises miniaturization. To ensure a compact area and avoid efficiency degradation, it is imperative to implement a conflict resolution mechanism that effectively manages access to shared capacitors among multiple elements.

A phase-splicing (PS) technique is designed to resolve such access conflicts optimally. To elaborate, we consider a scenario where all four elements require simultaneous flipping as illustrated in Fig. 3(a). In this case, the flipping efficiency can diminish due to the decreasing effective C_k/C_P (Eq. (1)). Since flipping occurs across nine non-interleaved phases, the sequence can be segmented at points of conflict to grant access to only one element at a time. A dedicated request handler is developed to prioritize access for a single element, while the remaining are queued. The request handler operates on a first-come, first-served basis to manage these conflicts efficiently. It continuously monitors the current flipping phases of all elements to anticipate and avert any potential conflicts in the upcoming phase, thereby eliminating the need for a separate evaluation cycle. If all PTs require flipping simultaneously, the request handler assigns dedicated priorities, ensuring sequential service: the first PT is addressed first, followed by the second, third, and fourth in order. With the highest priority assigned to PT1 for accessing the shared flying capacitor, C_{fly1}, PT2 initiates its flipping sequence only after PT1 completes its Phase-1. PT3 and PT4, meanwhile, remain in the queue to commence their respective Phase-1 operations. Upon completion of Phase-1, PT1 can immediately proceed to Phase-2 without interference, while PT2 begins its sequence, delayed by one phase, and PT3 starts two phases later. However, a conflict arises when PT3 needs to begin Phase-4, as PT1 simultaneously requires access to start Phase-6. Due to PT1's higher priority, Phase 4 of PT3 is deferred until Phase-6 of PT1

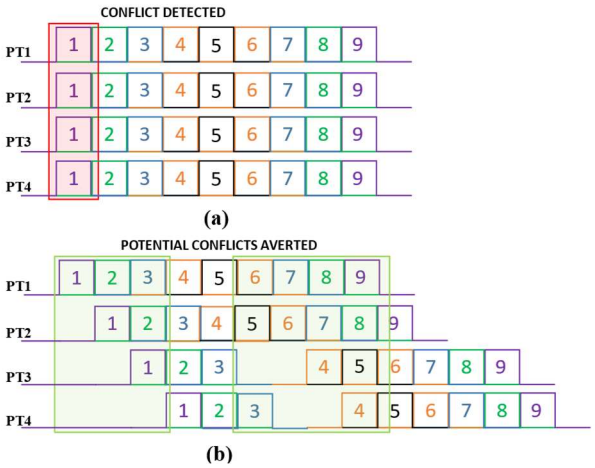

Fig. 3. (a) Conflicts for shared capacitor access among elements (b) Access conflicts averted by Request Handler

concludes. Once completed, PT3 is still unable to proceed, as Phase-6 of PT2 is now due. This process of prioritization continues until PT3 can resume its sequence. Similarly, PT4 experiences a three-phase delay in starting its flipping sequence, and subsequent conflicts are resolved similarly. Fig. 3(b) demonstrates the spliced flipping sequence, enabling optimal sharing of the flying capacitors. In cases where a phase request is initiated while the capacitor is already being accessed by another PT, the request is automatically queued. The period during which the capacitor is in use is designated as a "red zone," during which no new phase requests are accepted, ensuring that conflicts are avoided and the capacitor access is properly managed without interruption. Furthermore, the proposed algorithm operates in real-time, enabling continuous tracking of any changes in the request signals during subsequent flipping periods.

III. Circuit Implementation

The top-level architecture of the design is depicted in Fig. 4. The system comprises the request handler block with pulse generators, four pulse sequencing blocks with level shifters, four on-chip SSHC rectifiers, and four FBRs. In this configuration, the four on-chip flying capacitors require 9x4 pulses for the four PTs. The generated pulses are sequenced in the pulse sequencing block according to the current-voltage polarity and then level-shifted to the appropriate voltage levels to drive the switch arrays for voltage flipping.

A. Request handler block

This digital logic circuit block comprises four request handlers with pulse generators responsible for generating 8x4 capacitor access phases, along with a separate priority assignment block dedicated to producing the four C_P-clearing, phase-5 pulses. The first request handler generates a total of eight pulses for Phase-1 and Phase-9 (Fig.5), the second for Phase-2 and Phase-8, the third for Phase-3 and Phase-7, and the fourth for Phase-4 and Phase-6. SYN1-4 signals are fed into the first request handler, initiating Phase-1 pulses for all four PTs based on priority. These Phase-1 pulses act as requests to the next handler

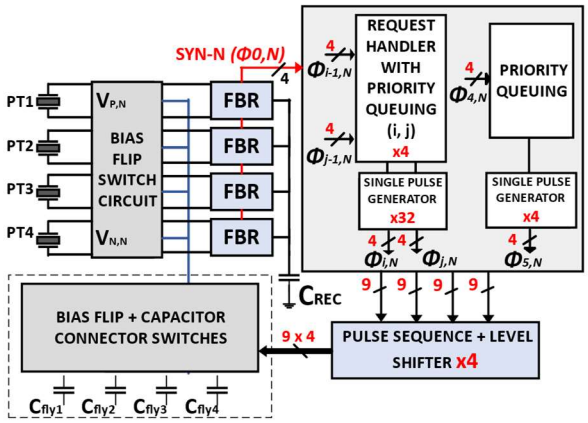

Fig. 4. The top-level block diagram of the proposed system

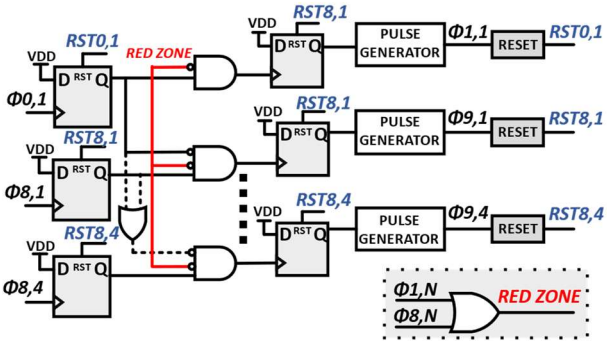

Fig. 5. Request handler-1

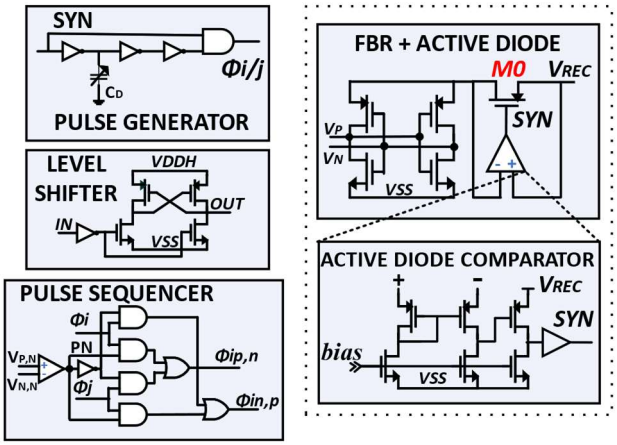

Fig. 6. Circuit implementations of top-level blocks

for Phase-2 pulses, which then sequentially trigger the following phases up to Phase-5. Subsequently, Phase-5 pulses prompt Phase-6 generation from the fourth handler, cascading in reverse until Phase-8 pulses prompt the first handler to generate the final Phase-9 pulse.

B. Full-bridge rectifier with active diode comparator

The FBRs rectify the received AC voltage to DC while generating four synchronized signals (SYN-N), which denote the FBR conduction status and trigger the voltage-flipping process. When the PT voltage requires flipping, the PMOS M0 turns OFF, stopping FBR conduction and generating a rising edge in SYN_N (Fig.6). These signals are then fed into the request handler-1 to initiate pulse generation based on priority.

TABLE I: Comparison with the state-of-the-art

	JSSC'17 [9]	ISSCC'18 [16]	ISCAS'22 [10]	**This work**
Technique	SSHC	SSHC	SSHC	**SSHC**
V_{OC}	2.5V	2.5V	2V	**2V**
F(Hz)	92	219	100k	**780k**
$C_{P,total}$	45nF	1.94nF	100pF	**255pF**
$C_{fly,total}$	360nF	15.5nF	800pF	**256pF**
$C_{fly,total}$ / $C_{P,total}$	8	8	8	**1**
Off-chip component	9 caps	9 caps	1 cap	**0**
Number of PTs	1	1	1	**4**
P_{MAX}(mW)	0.162	0.016	0.197	**3.03**
P_{SSHC}/P_{FBR}	9.68	5.2-8.2	5.69	**5.94**

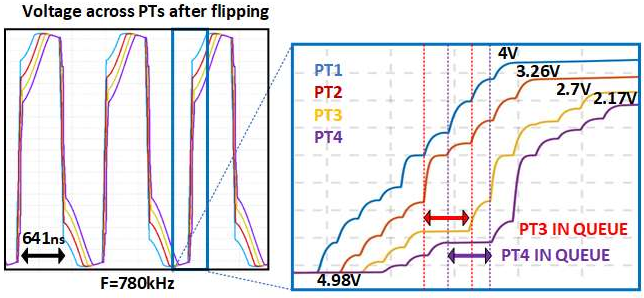

Fig. 7. Case 1-Voltage across PTs after flipping with wait time

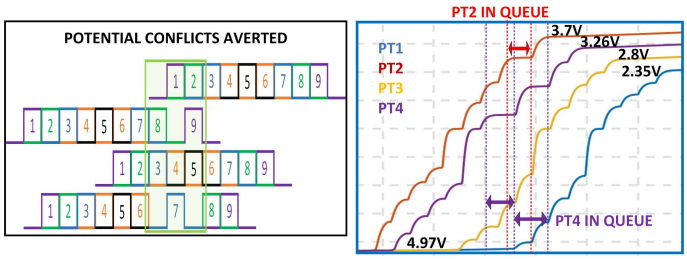

Fig. 8. Case 2-Voltage across PTs after flipping with wait time

IV. Simulation Results

The system is designed using a 180-nm BCD process. In the simulations, the transducer array comprised of four elements, each characterized by an inherent capacitance of C_P = 63.7pF, with an excitation frequency of 780 kHz, aligning with the transducer's natural resonance frequency. The capacitance of the four flying capacitors is set to 64pF each, which is equivalent to that of C_P. The open circuit voltage amplitude across the PTs ($V_{oc,N}$) is set to 2V. To assess the robustness and confirm the versatility of the designed circuit, simulations were conducted for special cases including i) near or equal to 0/π phase difference and ii) arbitrary arrival times and partial overlap cases.

A. Analysis of zero phase difference condition

Fig.7 illustrates the voltage across all four PTs, highlighting the wait times in the flipping sequence (see Fig. 4(b)). Notably, PT1 achieves a flipping efficiency of 80%, which degrades

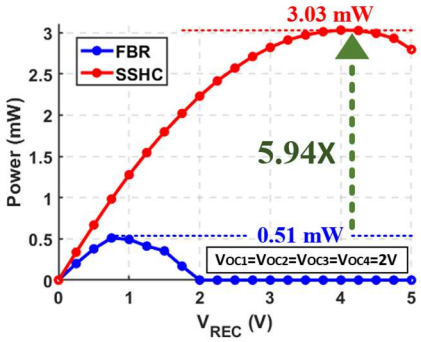

Fig. 9. The extracted power versus rectified voltage

sequentially to 65.4%, 54%, and 43.6% for the remaining PTs. This efficiency reduction results from charge-sharing during the flipping sequence: initially, C_{fly1} charges from $C_{P,PT1}$, but in subsequent phases, it shares charge with each subsequent PT, leading to reduced voltage increments. At the onset of Phase-6 of PT1, C_{fly1} maintains a higher voltage due to the initial dumping of all 4 PTs, thus benefiting its flipping efficiency. Overall, the average efficiency across the PTs is approximately 60.68%, slightly below theoretical expectations due to longer flipping time and current leakage at such high frequencies. Notably, the theoretical efficiency of a non-shared system with the same area (i.e., 16 capacitors $C_k = C_P/4$) is only 44.4%.

B. Analysis of arbitrary arrival times and partial overlap case

In this scenario, as depicted in Fig. 8, PT2 arrives first, followed by PT4, PT3, and PT1. The request handler assigns priorities based on arrival times while resolving conflicts according to the established priorities of PT1, PT2, PT3, and PT4. A conflict between Phase-9 of PT2 and Phase-1 of PT1 is successfully avoided by prioritizing PT1. Consistent with this prioritization scheme, PT4 is assigned the lowest priority and remains in the queue before the initiation of Phase-7 and Phase-8. The average efficiency across the PTs, in this case, is 60.8%.

Table I compares the proposed design with state-of-the-art piezoelectric energy harvesting interfaces. This is the first fully integrated SSHC rectifier proposed for a multi-piezo array, achieving a 5.94x enhancement in energy extraction compared to an FBR at a high ultrasonic frequency of 780 kHz (Fig. 9). The capacitor-sharing technique reduces the $C_{fly,total}/C_{P,total}$ by eight times compared to a typical SSHC rectifier, significantly decreasing the capacitor area. The C_{REC} size is set at 500 pF, which can be integrated on-chip in this technology, achieving a fully on-chip design—unlike state-of-the-art solutions that require at least C_{REC} to be off-chip.

V. Conclusion

This paper presents a fully integrated, high-frequency, scalable SSHC rectifier optimized for multi-PT arrays. The novel phase-splicing (PS) technique enables efficient capacitor sharing among all elements, mitigating conflicts arising from variable phase offsets. The proposed design reduces the overall form factor suitable for implantable medical devices and still achieves 5.94 times more power than an FBR.

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