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Dynamic Analysis of Photovoltaic to Virtual Bus Parallel Differential Power Processing Architecture

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***Abstract*—Photovoltaic (PV) to virtual bus parallel differential power processing (PDPP) architecture can mitigate mismatch losses among PV strings. This article presents a comprehensive dynamic analysis by deriving a small-signal model of the PDPP architecture based on its state space model. Subsequently, the corresponding transfer functions and frequency response are obtained, offering valuable insights into the dynamic behavior of the architecture. To validate the accuracy of the derived model, the frequency response has also been achieved by observed data from both PLECS simulation and experiment through system identification. Besides, this article discusses the design considerations of the discrete controllers' parameters for both virtual and intermediate bus voltages and studies the stability of the architecture. Experimental measurements confirm the ability of the central controller to stabilize the virtual bus voltage to the desired level within 0.6 seconds, while the intermediate bus voltages settle within 15 ms, enabling proper maximum power point tracking of each PV string.**

***Index Terms*—Differential power processing, photovoltatronics, photovoltaic (PV) system, small signal modelling, system identification.**

NOMENCLATURE

A. List of Acronyms

BL	Bridgeless
CCM	Continuous conduction mode
CPSD	Cross power spectral density
DAB	Dual active bridge
DMPPT	Distributed MPPT
DPP	Differential power processing
GUI	Graphical user interface
KCL	Kirchhoff's Current Law
LCOE	Levelized cost of electricity
MPPT	MPP tracking
MPP	Maximum power point
P&O	Perturbation and observation
PDPP	Parallel differential power processing
PI	Proportional-integral
PRBS	Pseudo-random binary sequence
PSD	Power spectral density
PV	Photovoltaic
PV2B	Photovoltaic-to-bus
PV2PV	Photovoltaic-to-photovoltaic
PV2VB	Photovoltaic-to-virtual bus
PWM	Pulse width modulation
SDPP	Series differential power processing
SLC	String-level converter
SPDPP	Series-parallel differential power processing
SPS	Single phase shift

B. List of Symbols

$\boldsymbol{A}$	State matrix
$\boldsymbol{B}$	Input matrix
$\boldsymbol{C}$	Output matrix
C_{BL}	BL converter output LC filter capacitor
C_S	Main bus capacitor
$\boldsymbol{D}$	Feedthrough matrix
$d_{\mathrm{BL}}(t)$	BL converter switch status
$d_S(t)$	Central switch status
f_{clock}	PRBS clock frequency
f_{PRBS}	Frequency range of the generated PRBS
f_{sw}	SLCs and central converter switching frequency
$f_{\mathrm{PV}}(v_{\mathrm{PV}})$	PV current–voltage (I–V) characteristic equation
$i_{\mathrm{BL}_L}(t)$	BL converter inductor current
$i_{\mathrm{DAB}_L}(t)$	DAB converter's load current
i_{L_s}	Boost inductor current
$i_{\mathrm{PV}}(t)$	PV string current
$i_{\mathrm{pri}}(t)$	Primary side current of the DAB converter
$i_{\mathrm{sec}}(t)$	Secondary side current of the DAB converter
L_{BL}	BL converter output LC filter inductor
L_{DAB}	DAB converter leakage inductor
L_S	Boost inductor
N_{PV}	Total number of PV strings
N_{PRBS}	PRBS length
N_{T}	Transformer turn ratio of the DAB converter
$p_{\mathrm{DAB}}(t)$	Output power of DAB converter
$p_{\mathrm{in}}(t)$	Total power generated by the PV strings
$p_{\mathrm{out}}(t)$	Output power of the system
$p_{\mathrm{VB}}(t)$	Virtual bus power
r_{PV}	Small-signal resistance of a PV element
$S_v(\omega)$	PSD of noise (v)
$S_u(\omega)$	PSD of input (u)
$S_{yu}(\omega)$	CPSD of input (u) and output (y)
T_{IB}	Intermediate bus voltage PI controller sampling time
T_{MPPT}	Perturbation period of MPPT algorithm
T_{VB}	Virtual bus PI controller sampling time
$v_{\mathrm{BL}_L}(t)$	BL converter inductor voltage
$v_{\mathrm{IB}}(t)$	Intermediate Bus Voltage

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V_{out}	Output voltage of boost converter
$v_{\text{PV}}(t)$	PV string voltage
$v_S(t)$	Main bus voltage
$v_{\text{SLC}_{\text{BF}}}(t)$	SLC's output voltage before LC filter
$v_{\text{SLC}_i}(t)$	SLC's output voltage
$v_{\text{VB}}(t)$	Virtual bus voltage
$z(t)$	A generic instantaneous Variable
$\overline{z}(t)$	Moving average of $z(t)$ over one switching period
$\tilde{z}(t)$	Small-signal term of $\overline{z}(t)$
Z	Constant equilibrium value
$Z(s)$	Variable in Laplace domain
$\varphi(t)$	Phase shift between the primary side and secondary side of the DAB converter

I. Introduction

OVER the past few decades, there has been a remarkable progression in the field of PV technology, semiconductors, circuits, and system architectures. These advancements have played a key role in substantially reducing the LCOE associated with PV systems, rendering them increasingly competitive in the ever-evolving landscape of energy generation [1]. A promising innovative concept contributing to the reduction of LCOE is the DPP architectures which brings significant advantage of mitigating mismatch-related losses attributed to factors such as partial shading, PV module tilt angles, dust accumulation, PV cell degradation, and more [2], [3]. What distinguishes DPP architectures from other DMPPT approaches is their ability to efficiently handle mismatch conditions. In such scenarios, converters are adept at processing only a portion of the generated power, allowing the bulk of the power produced by PV elements to pass through to the output without undergoing local processing. This feature brings: (i) a reduction in the overall cost of converters and an enhancement of system efficiency [4], [5], and (ii) a reduction in stress on system components, ultimately resulting in improved reliability and extended operational lifespan [6].

As shown in Fig. 1, DPPs are categorized into two main types: SDPP [7], [8], [9] and PDPP [10], [11]. The SDPP architecture (Fig. 1(a)) regulates the differential current (i_{MIC_i}) between individual PV modules $(i_{\text{PV}_{M_i}})$ and the overall PV string current (i_{PV}), effectively mitigating mismatch-related losses among series-connected PV modules. However, they cannot address mismatch losses among parallel-connected PV strings. To facilitate parallel connection of PV strings, PDPP architectures are engineered to provide the required differential voltage (v_{SLC_i}) between the voltage of PV strings (v_{PV}) and a main bus (v_S) (Fig. 1(b)). This operation effectively addresses mismatch-related losses among PV elements connected in parallel [12]. The literature has introduced two PDPP architectures: PV2B PDPP architectures [10], [13] and PV2VB PDPP architectures [11] (Fig. 2).

In PV2VB PDPP architectures, the virtual bus voltage, which defines the voltage rating of components, can be set lower than the main bus or PV string voltage. This allows for a reduction in the voltage rating of components, resulting in less electromagnetic interference (EMI) and radio-frequency interference [11], [14], [15]. Besides, the proposed PV2VB architecture provides superior scalability compared to conventional designs. Specifically, the SLC input voltage aligns with the virtual bus voltage, rather than the PV string or main bus voltage. This design allows

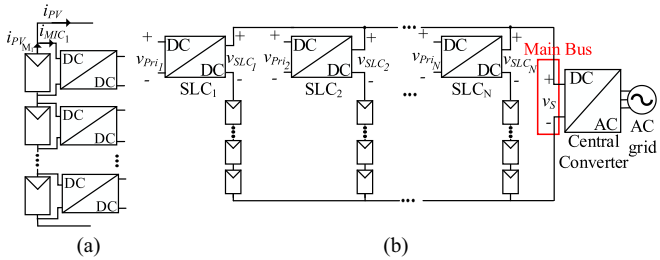

Fig. 1. PV systems using DPP architectures: (a) SDPP; (b) PDPP.

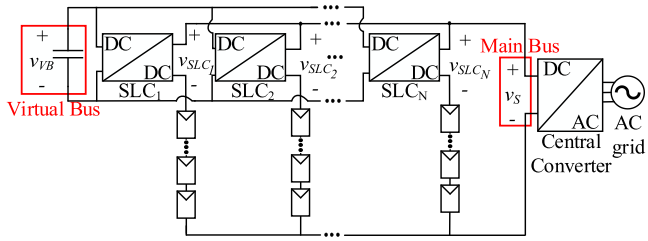

Fig. 2. PV systems using proposed PV2VB PDPP.

for greater flexibility in integrating new PV modules into each PV string, making it a more adaptable and versatile solution.

In [11], [15], an analysis of the steady-state operation of both the central converter and SLCs is provided, along with a description of their control objectives, duties, power ratings, and the design of the virtual bus voltage under steady-state conditions. However, in power electronic systems, the ability to deal with and control the consequences of unavoidable disturbances or errors that may drive circuits beyond their design specifications is crucial [16]. These perturbations encompass variations and uncertainties in source, load, or circuit parameters, disruptions in switching times, and—especially in PV systems—the MPPT algorithm. Hence, in the PV2VB PDPP architecture depicted in Fig. 2, precise control of both the SLCs and the central converter is crucial to maintain system robustness against disturbances and parameter variations and ensure optimal performance. Therefore, understanding the system's dynamic behavior through accurate modeling is essential for effective integration with other systems, proper component selection, and the exploration and development of new control methods [16], [17].

This article provides comprehensive system modeling and control design guidelines for the PV2VB PDPP architecture. Initially, a mathematical model of the architecture is derived using the state-space method and small-signal modeling in Section II. This section details the process, starting with the large-signal model equations, followed by their linearization, and concluding with the development of the architecture's state-space model. System identification [18], [19], [20] is then performed using data from both PLECS simulations and experiments to verify the accuracy of the mathematical model in representing the system's behavior, as described in Section III. The PV2VB PDPP architecture features two types of controllers: (i) the central controller, which adjusts the virtual bus voltage, and (ii) distributed controllers, which ensure the effective performance of the SLCs. Section IV covers the requirements and guidelines for these controllers. Based on these requirements and the validated mathematical model, PI

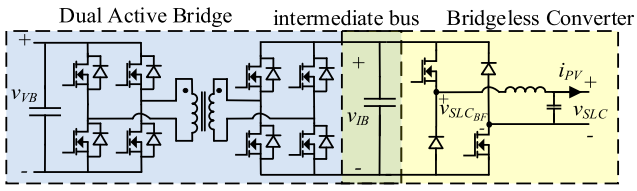

Fig. 3. Proposed SLCs topology for PV2VB PDPP architecture: A DAB converter followed by a BL converter.

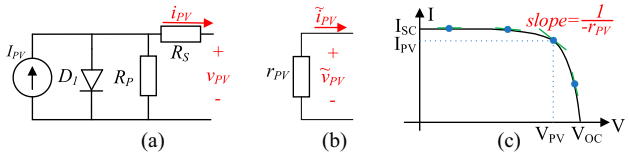

Fig. 4. A PV element: (a) large signal model; (b) small signal equivalent circuit; and (c) exemplary I–V curve.

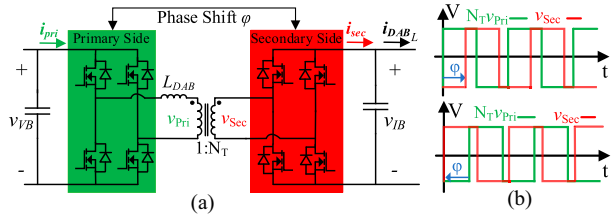

Fig. 5. DAB converter. (a) Topology. (b) Waveforms using SPS modulation. Top: The primary side leads the secondary side, and the energy is transferred from the virtual bus to the intermediate bus. Bottom: The secondary side leads the primary side, and the energy transfer direction is reversed.

controllers are designed as examples. The design process focuses on critical parameters such as phase margin, bandwidth, and settling time. Section V presents experiments conducted on a prototype with two SLCs connected to separate PV strings, each rated at 2 kW, 400 V, and 5 A, to validate the controller designs.

II. State Space Model of the PV2VB PDPP Architecture

In a PV2VB PDPP architecture, SLCs are connected to a shared isolated dc bus called the virtual bus (Fig. 2). Preserving power equilibrium within this virtual bus is of utmost importance, as it serves to ensure stable operation and mitigate voltage fluctuations. This equilibrium is achieved by letting some PV strings inject energy into the virtual bus through their SLCs while the other PV strings draw energy from it. In this architecture, each SLC not only serves as MPP tracker for the connected PV string but also provides a path for the efficient transfer of power to and from the virtual bus, while a central converter maintains the virtual bus voltage at a constant level. In [15], a DAB converter followed by a BL converter was proposed (Fig. 3). BL converters facilitate a path for PV strings current and generate necessary negative and positive voltages, while DAB converters facilitate power transfer between the intermediate bus and the virtual bus, regulating the intermediate bus voltage. A detailed analysis of the steady-state operation of the PV2VB DPP architecture can be found in [15]. Here, the focus is on deriving the equations governing the operation of the PV strings, the SLCs and the central converter, and to create a state-space model of the PV2VB PDPP architecture.

A. PV String Model

When addressing PV cells, a range of equivalent circuits of varying complexity and accuracy have been proposed in the existing literature. Among these, the single-diode model depicted in Fig. 4(a) is widely recognized as the prevalent large signal model for PV cells [21]. A PV string consists of several PV cells connected in series, so it is possible to extend the model to PV strings. This model inherently yields a nonlinear current–voltage equation for the PV string, which can be linearized around a specific operating point

$$i_{\mathrm{PV}}(t) = f_{\mathrm{PV}}(v_{\mathrm{PV}}(t)) \rightarrow \tilde{i}_{\mathrm{PV}}(t) = \frac{-1}{r_{\mathrm{PV}}} \cdot \tilde{v}_{\mathrm{PV}}(t)$$
$$r_{\mathrm{PV}} = \frac{-1}{\frac{\partial f_{\mathrm{PV}_i}}{\partial \tilde{v}_{\mathrm{PV}}(t)}|_{\tilde{v}_{\mathrm{PV}}(t)=V_{\mathrm{PV}}}}. \quad (1)$$

This linearized model is depicted in Fig. 4(b). Besides, as shown in Fig. 4(c), $-1/r_{\mathrm{PV}}$ is the slope of the PV string I–V curve at a given operating dc point $(I_{\mathrm{PV}}, V_{\mathrm{PV}})$, and it is assumed to be frequency-independent at sufficiently low frequencies [22].

B. Averaged Large Signal Model of the Power Converters

Given that SLCs and the central converter operate as PWM converters, averaging over a switching period is performed to derive the models of the power converters.

1) SLCs Model: In the PV2VB PDPP architecture in this study, the SLCs consist of a DAB converter followed by a BL converter (Fig. 3). The DAB converter's primary side connects to the virtual bus, while its secondary side is connected to the BL converter. An *Intermediate Bus* between the two converters decouples their operation. The second stage of the SLC topology is the BL converter, located between the PV string and the main bus. It provides both positive and negative output voltages necessary for PV strings to operate at MPP and ensures a current path for the PV string [15].

For DAB converters, an averaged equivalent circuit and the respective mathematical model are introduced in [23] considering an SPS modulation (see Fig. 5). The average output power of a DAB converter can be expressed as [23]

$$\overline{p}_{\mathrm{DAB}}(t) = \frac{\overline{v}_{\mathrm{VB}}(t) \cdot \overline{v}_{\mathrm{IB}}(t) \cdot \varphi(t) \cdot (1 - 2 \cdot \varphi(t))}{N_{\mathrm{T}} \cdot f_{\mathrm{sw}} \cdot L_{\mathrm{DAB}}}. \quad (2)$$

The average values of input and output currents over one switching period are used to describe the characteristics of the current. In a lossless DAB converter, the primary and secondary side power are equal and obtained by

$$\overline{p}_{\mathrm{DAB}}(t) = \overline{i}_{\mathrm{pri}}(t) \cdot \overline{v}_{\mathrm{VB}}(t) = \overline{i}_{\mathrm{sec}}(t) \cdot \overline{v}_{\mathrm{IB}}(t). \quad (3)$$

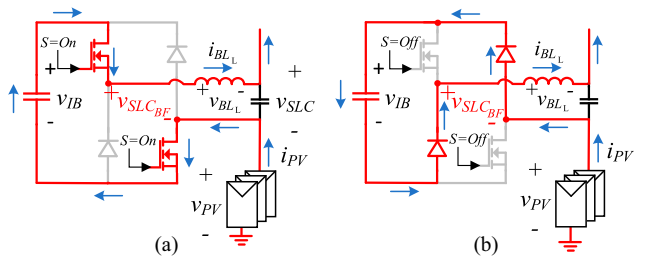

Fig. 6. BL converter operation during: (a) the ON-state; (b) the OFF-state.

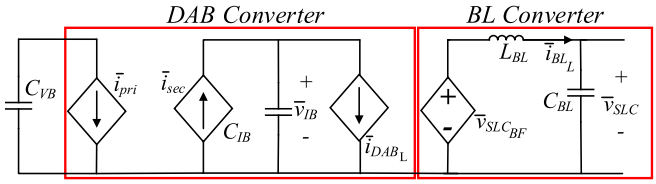

Fig. 7. Averaged large signal model of an SLC (a DAB followed by a BL converter).

So, the average currents for both the primary and secondary sides will be

$$\bar{i}_{\mathrm{pri}}(t)=\frac{\bar{v}_{\mathrm{IB}}(t)\cdot\varphi(t)\cdot(1-2\cdot\varphi(t))}{N_{\mathrm{T}}\cdot f_{\mathrm{sw}}\cdot L_{\mathrm{DAB}}} \tag{4}$$

$$\bar{i}_{\mathrm{sec}}(t)=\frac{\bar{v}_{\mathrm{VB}}(t)\cdot\varphi(t)\cdot(1-2\cdot\varphi(t))}{N_{\mathrm{T}}\cdot f_{\mathrm{sw}}\cdot L_{\mathrm{DAB}}}. \tag{5}$$

The average load current of the DAB converter ($\bar{i}_{\mathrm{DAB}_L}$) is determined by the behavior of the BL converter. When the BL converter operates in CCM, during the ON state of the BL converter switches, the current in the intermediate bus flows upwards [Fig. 6(a)], drawing energy from the intermediate bus. Conversely, during the switch's OFF state, the current direction reverses, with energy being returned to the intermediate bus [Fig. 6(b)]. Consequently, the average current over a complete switching cycle can be calculated by

$$\bar{i}_{\mathrm{DAB}_L}(t)=\left(2\cdot\bar{d}_{\mathrm{BL}}(t)-1\right)\cdot\bar{i}_{\mathrm{BL}_L}(t). \tag{6}$$

By using (4)–(6), it is possible to establish a large signal average model for the DAB converter, as illustrated in Fig. 7. To complete the SLC model, the BL converter must also be analyzed.

As far as the output voltage of the SLCs before the LC filter ($\bar{v}_{\mathrm{SLC_{BF}}}$) is concerned, no significant transients are present, except for the negligible effects during the switching period. Therefore, the BL converter can be modelled by its LC filter and a voltage source with an average voltage value equal to

$$\bar{v}_{\mathrm{SLC_{BF}}}(t)=\left(2\cdot\bar{d}_{\mathrm{BL}}(t)-1\right)\cdot\bar{v}_{\mathrm{IB}}(t). \tag{7}$$

Equations (6) and (7) show that to let average power flow from the intermediate bus to the PV string, the BL converter's duty cycle must be above 0.5. If the duty cycle drops below this threshold, the power flow reverses, moving from the PV string to the intermediate bus. Since the direction of power flow is determined by the duty cycle (d_{BL}) and not by any structural change in the SLCs, the mathematical models remain consistent throughout both power flow directions [15]. The ultimate step in obtaining an average large-signal equivalent circuit of SLCs involves combining the DAB and BL converters models, resulting in the circuit depicted in Fig. 7.

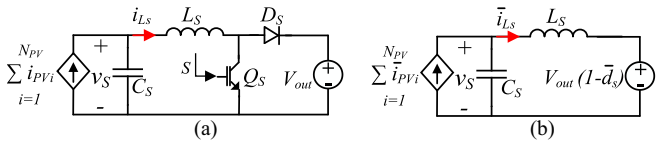

Fig. 8. Boost converter: (a) schematic; (b) averaged large signal model.

The equivalent circuit of Fig. 7 can be used to obtain a state-space representation of the SLCs, with the state variables being $\bar{v}_{\mathrm{SLC}}(t)$, $\bar{v}_{\mathrm{IB}}(t)$, and $\bar{i}_{\mathrm{BL}_L}(t)$, and the inputs being $\bar{d}_{\mathrm{BL}}$ and $\varphi(t)$, which control the operation of the switches in both DAB and BL converters. Noting that the average voltage of the i^{th} PV string $\bar{v}_{\mathrm{PV}_i}(t)$ is equal to

$$\bar{v}_{\mathrm{PV}_i}(t)=\bar{v}_S(t)-\bar{v}_{\mathrm{SLC}_i}(t) \tag{8}$$

the state equations of the state-space model for the i^{th} SLC are

$$\frac{\partial\bar{v}_{\mathrm{SLC}_i}(t)}{\partial t}=\frac{\bar{i}_{\mathrm{BL}_{L_i}}(t)-\bar{i}_{\mathrm{PV}_i}(t)}{C_{\mathrm{BL}}}=\frac{\bar{i}_{\mathrm{BL}_{L_i}}(t)-f_{\mathrm{PV}_i}\left(\bar{v}_S(t)-\bar{v}_{\mathrm{SLC}_i}(t)\right)}{C_{\mathrm{BL}}}$$
$$=g_{1_i}\left(\bar{i}_{\mathrm{BL}_{L_i}}(t),\bar{v}_S(t),\bar{v}_{\mathrm{SLC}_i}(t)\right) \tag{9}$$

$$\frac{\partial\bar{v}_{\mathrm{IB}_i}(t)}{\partial t}=\frac{\bar{v}_{\mathrm{VB}}(t)\cdot\varphi_i(t)\cdot(1-2\cdot\varphi_i(t))}{N_{\mathrm{T}}\cdot f_{\mathrm{sw}}\cdot L_{\mathrm{DAB}}\cdot C_{\mathrm{IB}}}-\frac{\left(2\cdot\bar{d}_{\mathrm{BL}_i}(t)-1\right)\cdot\bar{i}_{\mathrm{BL}_{L_i}}(t)}{C_{\mathrm{IB}}}$$
$$=g_{2_i}\left(\bar{i}_{\mathrm{BL}_{L_i}}(t),\bar{v}_{\mathrm{VB}}(t),\varphi_i(t),\bar{d}_{\mathrm{BL}_i}(t)\right) \tag{10}$$

$$\frac{\partial\bar{i}_{\mathrm{BL}_{L_i}}(t)}{\partial t}=\frac{\bar{v}_{\mathrm{IB}_i}(t)\cdot\left(2\cdot\bar{d}_{\mathrm{BL}_i}(t)-1\right)-\bar{v}_{\mathrm{SLC}_i}(t)}{L_{\mathrm{BL}}}$$
$$=g_{3_i}\left(\bar{v}_{\mathrm{SLC}_i}(t),\bar{v}_{\mathrm{IB}_i}(t),\bar{d}_{\mathrm{BL}_i}(t)\right). \tag{11}$$

2) Central Converter Model: To establish a complete model for the architecture, it is necessary to consider the central converter equations in the state-space form. As a representative topology, a boost converter has been selected, whose state variables are $\bar{i}_{L_s}(t)$ and $\bar{v}_S(t)$, whereas $\bar{d}_s(t)$ is the input variable. It should be noted that the input current of the boost converter is the summation of the PV strings currents (Fig. 8). Ultimately, by formulating the relevant equations for both the switch-ON and switch-OFF states and subsequently averaging them over a switching cycle, we can successfully derive the boost converter equations for the state-space model

$$\frac{\partial\bar{v}_S(t)}{\partial t}=\frac{\left(\sum_{i=1}^{N_{\mathrm{PV}}}\bar{i}_{\mathrm{PV}}(t)\right)-\bar{i}_{L_s}(t)}{C_s}$$
$$=\frac{\left(\sum_{i=1}^{N_{\mathrm{PV}}}f_{\mathrm{PV}_i}\left(\bar{v}_S(t)-\bar{v}_{\mathrm{SLC}_i}(t)\right)\right)-\bar{i}_{L_s}(t)}{C_s}$$
$$=g_4\left(\bar{v}_{\mathrm{SLC}_i}(t)|i=\{1\ldots N_{\mathrm{PV}}\},\bar{v}_S(t),\bar{i}_{L_s}(t)\right) \tag{12}$$

$$\frac{\partial \overline{i}_{L_s}(t)}{\partial t} = \frac{\overline{v}_S(t) - V_{\text{out}} \cdot \left(1 - \overline{d}_s(t)\right)}{L_s} = g_5\left(\overline{v}_S(t), \overline{d}_s(t)\right). \quad (13)$$

Here, it is assumed that the dynamic behavior of V_{out} is negligible and does not exert a significant influence on the overall architecture dynamics. Therefore, for the purposes of analysis in this article, it is considered a constant value.

3) Virtual Bus: The architecture has one more state variable: $\overline{v}_{\text{VB}}$. To determine the related state equation, a KCL must be applied at the virtual bus node

$$\frac{d\overline{v}_{\text{VB}}(t)}{dt} = \frac{\sum_{i=1}^{N_{\text{PV}}} \overline{v}_{\text{IB}_i}(t) \cdot \varphi_i(t) \cdot (1 - 2.\varphi_i(t))}{N_{\text{T}} \cdot f_{\text{sw}} \cdot L_{\text{DAB}} \cdot C_{\text{VB}}} = g_6\left(\overline{v}_{\text{IB}_i}(t) | i = \{1 \ldots N_{\text{PV}}\}, \varphi_i(t) | i = \{1 \ldots N_{\text{PV}}\}\right). \quad (14)$$

C. Steady-State Solution

In small-signal analysis, the equations are linearized around an operating point, and constant equilibrium values of the state or input variables do appear in the model. Thus, when considering a desired operating point defined by parameters such as $V_{\text{PV}_{\text{MPP}_i}}$, $I_{\text{PV}_{\text{MPP}_i}}$, V_{out}, and V_{IB_i}, where $V_{\text{PV}_{\text{MPP}_i}}$ and $I_{\text{PV}_{\text{MPP}_i}}$ represent MPP voltage and current of i^{th} PV string, determining the equilibrium values for both state and input variables is crucial to finalize the model. These are achieved by

$$V_S = \frac{\sum_{i=1}^{N_{\text{PV}}} V_{\text{PV}_{\text{MPP}_i}} \cdot I_{\text{PV}_{\text{MPP}_i}}}{\sum_{j=1}^{N_{\text{PV}}} I_{\text{PV}_{\text{MPP}_i}}} \quad (15)$$

$$V_{\text{SLC}_i} = V_S - V_{\text{PV}_{\text{MPP}_i}},\ I_{\text{BL}_{L_i}} = I_{\text{PV}_{\text{MPP}_i}} \quad (16)$$

$$D_{\text{BL}_i} = \frac{V_{\text{SLC}_i}}{2 \cdot V_{\text{IB}}} + 0.5 \quad (17)$$

$$\Phi_i \cdot (1 - 2 \cdot \Phi_i) = \frac{V_{\text{SLC}_i} \cdot I_{\text{PV}_{\text{MPP}_i}} \cdot N_{\text{T}} \cdot f_{\text{sw}} \cdot L_{\text{DAB}}}{V_{\text{VB}} \cdot V_{\text{IB}_i}} \quad (18)$$

$$D_S = \frac{V_{\text{out}} - V_S}{V_{\text{out}}}. \quad (19)$$

The averaged large-signal model developed in Section II allows to calculate these equations by imposing all the derivatives equal to zero.

D. Linearization and Small Signal Model

The large-signal model derived in Section II can be linearized around an operating point to derive a small signal model of the PV2VB PDPP architecture. The process of linearization involves expanding (9)–(14) through a Taylor series expansion, focusing on linear terms

$$\frac{\partial \tilde{v}_{\text{SLC}_i}(t)}{\partial t} = \frac{\partial g_{1_i}}{\partial \overline{v}_{\text{SLC}_i}(t)} \tilde{v}_{\text{SLC}_i}(t) + \frac{\partial g_{1_i}}{\partial \overline{i}_{\text{BL}_{L_i}}(t)} \tilde{i}_{\text{BL}_{L_i}}(t) + \frac{\partial g_{1_i}}{\partial \overline{v}_S(t)} \tilde{v}_S(t) \quad (20)$$

$$\frac{\partial \tilde{v}_{\text{IB}_i}(t)}{\partial t} = \frac{\partial g_{2_i}}{\partial \overline{i}_{\text{BL}_{L_i}}(t)} \tilde{i}_{\text{BL}_{L_i}}(t) + \frac{\partial g_{2_i}}{\partial \overline{v}_{\text{VB}}(t)} \tilde{v}_{\text{VB}}(t) + \frac{\partial g_{2_i}}{\partial \varphi_i(t)} \tilde{\varphi}_i(t) + \frac{\partial g_{2_i}}{\partial \overline{d}_{\text{BL}_i}(t)} \tilde{d}_{\text{BL}_i}(t) \quad (21)$$

$$\frac{\partial \tilde{i}_{\text{BL}_{L_i}}(t)}{\partial t} = \frac{\partial g_{3_i}}{\partial \overline{v}_{\text{SLC}_i}(t)} \tilde{v}_{\text{SLC}_i}(t) + \frac{\partial g_{3_i}}{\partial \overline{v}_{\text{IB}_i}(t)} \tilde{v}_{\text{IB}_i}(t) + \frac{\partial g_{3_i}}{\partial \overline{d}_{\text{BL}_i}(t)} \tilde{d}_{\text{BL}_i}(t) \quad (22)$$

$$\frac{\partial \tilde{v}_S(t)}{\partial t} = \sum_{i=1}^{N_{\text{PV}}} \frac{\partial g_4}{\partial \overline{v}_{\text{SLC}_i}(t)} \tilde{v}_{\text{SLC}_i}(t) + \frac{\partial g_4}{\partial \overline{v}_S(t)} \tilde{v}_S(t) + \frac{\partial g_4}{\partial \overline{i}_{L_s}(t)} \tilde{i}_{L_s}(t) \quad (23)$$

$$\frac{\partial \tilde{i}_{L_s}(t)}{\partial t} = \frac{\partial g_5}{\partial \overline{v}_S(t)} \tilde{v}_S(t) + \frac{\partial g_5}{\partial \overline{d}_s(t)} \tilde{d}_S(t) \quad (24)$$

$$\frac{\partial \tilde{v}_{\text{VB}}(t)}{\partial t} = \sum_{i=1}^{N_{\text{PV}}} \frac{\partial g_{6_i}}{\partial \overline{v}_{\text{IB}_i}(t)} \tilde{v}_{\text{IB}_i}(t) + \sum_{i=1}^{N_{\text{PV}}} \frac{\partial g_{6_i}}{\partial \varphi_i(t)} \tilde{\varphi}_i(t). \quad (25)$$

The coefficients of (20)–(25) are obtained by taking the corresponding derivatives from (9)–(14). The generalized form of a linearized state space model, designed to extract the desired transfer function, can be expressed as follows:

$$\begin{cases} \dfrac{\partial \tilde{x}(t)}{\partial t} = \boldsymbol{A}\tilde{x}(t) + \boldsymbol{B}\tilde{u}(t) \\ \tilde{y}(t) = \boldsymbol{C}\tilde{x}(t) + \boldsymbol{D}\tilde{u}(t). \end{cases} \quad (26)$$

In PV2VB PDPP architectures, each SLC contributes three state variables ($\tilde{v}_{\text{SLC}}$, $\tilde{v}_{\text{IB}}(t)$, $\tilde{i}_{\text{BL}_L}$), the central converter adds two state variables ($\tilde{v}_S(t)$, $\tilde{i}_{L_S}(t)$), and the last state variable is the virtual bus voltage ($\tilde{v}_{\text{VB}}$). Thus, the system comprises a total of $(3N_{\text{PV}}+3)$ state variables. Regarding input and output variables, each SLC encompasses two input variables ($\tilde{d}_{\text{BL}}$ and $\tilde{\varphi}$) and the central converter introduces one input variable $(\tilde{d}_S)$. Thus, the total number of input variables amounts to $(2N_{\text{PV}} + 1)$. The main control goal revolves around regulating the intermediate bus voltage of each SLC and virtual bus voltage, meaning there will be $(N_{\text{PV}} + 1)$ output variables. Therefore, the state, input, and output vectors are respectively defined as follows:

$$\tilde{x}(t) = [\tilde{v}_{\text{SLC}_1}(t)\ \tilde{v}_{\text{IB}_1}(t)\ \tilde{i}_{\text{BL}_{L_1}}(t)\ \ldots\ \tilde{v}_{\text{SLC}_{N_{\text{PV}}}}(t)\ \tilde{v}_{\text{IB}_{N_{\text{PV}}}}(t)\ \tilde{i}_{\text{BL}_{L_{N_{\text{PV}}}}}(t)\ \tilde{v}_S(t)\ \tilde{i}_{L_S}(t)\ \tilde{v}_{\text{VB}}(t)]^T \quad (27)$$

$$\tilde{u}(t) = \left[\tilde{\varphi}_1(t)\ \tilde{d}_{\text{BL}_1}(t) \ldots \tilde{\varphi}_{N_{\text{PV}}}(t)\ \tilde{d}_{\text{BL}_{N_{\text{PV}}}}(t)\ \tilde{d}_{\text{BL}_{N_{\text{PV}}}}(t)\ \tilde{d}_{\text{S}}(t)\right]^T \quad (28)$$

$$\tilde{y}(t) = \left[\tilde{v}_{\text{IB}_1}(t)\ \ldots\ \tilde{v}_{\text{IB}_{N_{\text{PV}}}}(t)\ \tilde{v}_{\text{VB}}(t)\right]^T \quad (29)$$

Matrix $\boldsymbol{A}$, $\boldsymbol{B}$, $\boldsymbol{C}$, and $\boldsymbol{D}$ can be obtained from (20)–(25). Eventually, based on the linearized (20)–(25), the small signal equivalent circuit of the architecture is shown in Fig. 9.

III. System Identification Based on Observed Data

The actual transfer function of the PV2VB PDPP architecture has been evaluated through system identification, aiming at validating the mathematical model developed in the previous section. System identification methods are usually divided into parametric [24] and nonparametric methods [25]. Here, the latter are preferable since for a fair validation the system must be

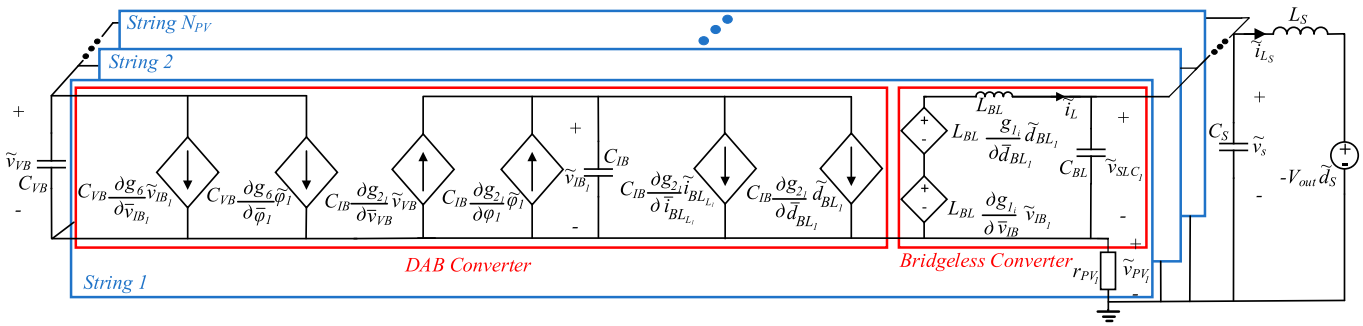

Fig. 9. Averaged small signal model of the PV2VB PDPP architecture.

considered as a black box with the dynamics totally unknown. Nonparametric method includes: correlation analysis [18], [26], transient-response analysis [27], and frequency response, Fourier, or spectral analysis [25]. To obtain frequency insights—crucial for understanding system behavior and designing an effective controller—off-line spectral analysis [28] is utilized.

A. Nonparametric System Identification Procedure

For system identification, after the system reaches steady-state, it is perturbed by an ad-hoc informative small-signal. An informative input should be persistently exciting, i.e., it contains sufficiently diverse frequencies and excites desired modes and dynamics of the system [18], [19]. PRBS is a proper input for system identification, since it contains a wide range of frequencies and is easy to implement. The PRBS is a periodic, deterministic, binary signal with white noise-like properties and is generated by a difference equation [19]. After PRBS is generated, it is possible to change it to two desired levels $\{-a, +a\}$, and the sequence is periodic with a length of

$$N_{\text{PRBS}} = 2^n - 1. \tag{30}$$

A standard PRBS has a maximum frequency determined by its clock frequency and a bandwidth determined by its length, so its frequency range is as follows:

$$\frac{f_{\text{Clock}}}{N_{\text{PRBS}}} < f_{\text{PRBS}} < \frac{f_{\text{Clock}}}{2}. \tag{31}$$

Therefore, the clock frequency should be selected so that the PRBS signal can effectively excite the desired system dynamics. Additionally, the PRBS length must be long enough to provide reliable results, but overly long sequences can lead to challenges such as increased data complexity and extended test durations. For the PRBS magnitude $\{-a, +a\}$, a larger amplitude is beneficial to improve the signal-to-noise ratio when injected into the duty cycle of the central converter. However, to ensure linear system behavior, the PRBS amplitude must remain low. Once the excitation input is applied to the system, the input/output data are collected and pre-processed to deal with drift, trends, offset, outliers, missing data, and so on. Afterwards, power spectral analysis is performed to identify the frequency response of the system.

For small-signal disturbances, a power converter can be regarded as a linear time-invariant discrete-time system, where the following relationships among the input PSD, output PSD, and CSPD exist [19], [26], [29]

$$S_y(\omega) = \left|H(e^{i\omega})\right|^2 \cdot S_u(\omega) + S_v(\omega) \tag{32}$$

$$S_{yu}(\omega) = H(e^{i\omega}) \cdot S_u(\omega) \tag{33}$$

where $H(e^{i\omega})$ is the input-to-output frequency response and for discrete input and output signals, the CPSD and the cross-covariance R_{yu} between input and output are

$$S_{yu}(\omega) = \sum_{m=-\infty}^{\infty} R_{yu}(m)e^{-i2\pi m},\ R_{yu}(m) = \sum_{m=1}^{\infty} \tilde{u}(m)\tilde{y}(n+m). \tag{34}$$

Whereas the PSDs and auto-covariance R_u and R_y of the two signals can be calculated as

$$S_z(\omega) = \sum_{m=-\infty}^{\infty} R_z(m)e^{-i2\pi m},\ R_z(m) = \sum_{m=1}^{\infty} \tilde{z}(m)\tilde{z}(n+m) \tag{35}$$

where z is either the input signal u or the output signal y. The estimates are then formed as

$$H(e^{i\omega}) = \frac{S_{yu}(\omega)}{S_u(\omega)},\ S_v(\omega) = S_y(\omega) - \frac{\left|S_{yu}(\omega)\right|^2}{S_u(\omega)}. \tag{36}$$

Thus, in the spectral analysis, by using post-processed measured samples of both input and output, input and output PSDs and their CPSD are calculated by (32)–(35). Afterwards, the transfer function of the system is estimated using (36).

Note that here: 1) system identification is performed in open loop; 2) the PRBS signal is generated by the *idinput()* function in MATLAB; and 3) the nonparametric identification procedure presented above is applied through the *spafdr()* function in MATLAB.

B. Validation Through Circuit Simulations

A first validation of the model has been performed through PLECS simulations. A PV2VB PDPP architecture with specification shown in Table I has been simulated in PLECS. The system initially operates in a closed-loop mode until it achieves steady-state conditions with both PV strings at their MPPs (Table II). Then, the architecture transitions to an open-loop mode. During this phase, a PRBS signal is added to the duty cycle of the central converter, and the virtual bus voltage is measured. The PRBS signal parameters are presented in

TABLE I
ARCHITECTURE PARAMETERS OF THE SYSTEM FOR SYSTEM IDENTIFICATION

Symbol	Value	Symbol	Value	Symbol	Value
N_{PV}	2	C_{BL}	3 μF	L_{BL}	660 μH
C_{VB}	1.2 mF	L_{DAB_L}	22 μH	C_S	6.6 μF
L_S	510 μH	f_{sw}	100 kHz		

TABLE II
OPERATING POINT FOR SYSTEM IDENTIFICATION

Symbol	Value	Symbol	Value	Symbol	Value
$V_{PV_{MPP_1}}$	267 V	$I_{PV_{MPP_1}}$	5.3A	V_{IB_1}	200 V
$V_{PV_{MPP_2}}$	400 V	$I_{PV_{MPP_2}}$	5.3 A	V_{IB_2}	200 V
V_{out}	450 V	V_{VB}	200 V		

TABLE III
PRBS SIGNAL PARAMETERS

Parameter	Symbol	Value	
		PLECS simulation	Experiment
Clock frequency	f_{Clock}	50 kHz	100 Hz
Length	N_{PRBS}	131 071	2047
Amplitude (central converter)	a_{d_S}	$\{-0.01, 0.01\}$	$\{-0.015, 0.015\}$
Amplitude (DAB converter)	$a_{\varphi_{DAB}}$	$\{0.004, 0.004\}$	$\{-0.001, 0.001\}$

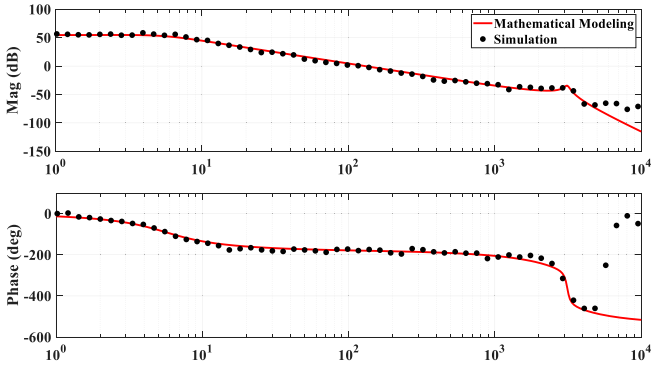

Fig. 10. $D_S(s)$ to $V_{VB}(s)$ transfer function. The input used for system identification is a two-period 17-bit PRBS with clock frequency of 50 kHz.

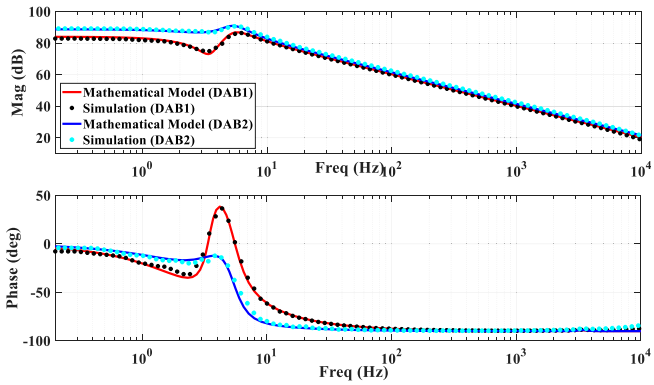

Fig. 11. $\Phi_i(s)$ to $V_{IB_i}(s)$ transfer functions. The input used for system identification is a two-period 17-bit PRBS with clock frequency of 50 kHz.

Table III and have been chosen based on the considerations discussed in the previous section. The $D_S(s)$ to $V_{VB}(s)$ transfer function has been evaluated using the nonparametric identification procedure presented above, and the Bode plots are shown in Fig. 10. Using the same procedure, a PRBS signal is applied to the phase shift of each DAB converter, one at a time. The $\Phi_i(s)$ to $V_{IB_i}(s)$ transfer function is then evaluated and the Bode plots are shown in Fig. 11.

The architecture with two PV stings has nine state variables, which lead to nine poles. As shown in Fig. 10, the $D_S(s)$ to $V_{VB}(s)$ transfer function has three zeros and nine poles; moreover, it is possible to identify on the Bode plot two dominant poles defining the dynamic of the system. On the other hand, Fig. 11 shows that $\Phi_i(s)$ to $V_{IB_i}(s)$ transfer functions at high frequencies resemble those of independent DAB converters [30], with the zeros located very close to the poles, effectively canceling each other out. This indicates that the virtual bus and intermediate bus capacitors are sufficiently large to decouple the performance of the DAB converters from other parts of the architecture. The differences between the Bode plots of DAB1 and DAB2 arise from their different operating points: while DAB1 transfers power from the virtual bus to the intermediate bus, DAB2 transfers power from the intermediate bus to the virtual bus.

Figs. 10 and 11 provide a validation of the mathematical model presented in Section II. Indeed, the Bode plot estimated from PLECS simulations through system identification (dots) and the one calculated from the mathematical model (solid lines). Discrepancies between the mathematical model and simulation results for the $D_S(s)$ to $V_{VB}(s)$ transfer function appear at frequencies above $0.05 \times f_{sw}$. This is due to the strong low-pass characteristic of this transfer function (resulting in more than -70 dB attenuation), combined with the limited duty cycle variation $\{-0.01, 0.01\}$. As a result, the simulation struggles to capture high-frequency dynamics above $0.05 \times f_{sw}$. Nevertheless, all system poles and zeros, and consequently the system's overall dynamic behavior, are accurately captured within this frequency range of $0.05 \times f_{sw}$.

C. Experimental Validation

Fig. 12 shows two SLCs prototypes connected to two PV emulators as PV strings, a 6210H-600S Programmable dc power supply as one of the PV strings and a SM1500-CP-30 Bi-directional dc Power Supplies as the other PV string. Then, the output of the boost converter was connected to a SM1500-CP-30 Bi-directional dc Power Supplies emulating the constant voltage output dc bus (V_{out}). The digital controller was

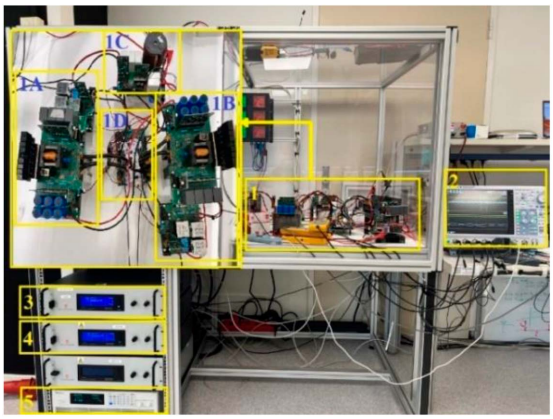

Fig. 12. Photograph of the PV2VB PDPP architecture prototype. 1A: SLC_1, 1B: SLC_2, 1C: central converter, 1D: micro controller, 2: YOKOGAWA DLM5038 Oscilloscope, 3 and 4: SM1500-CP-30 bi-directional dc power supplies, 5: 6210H-600S programmable dc power supply.

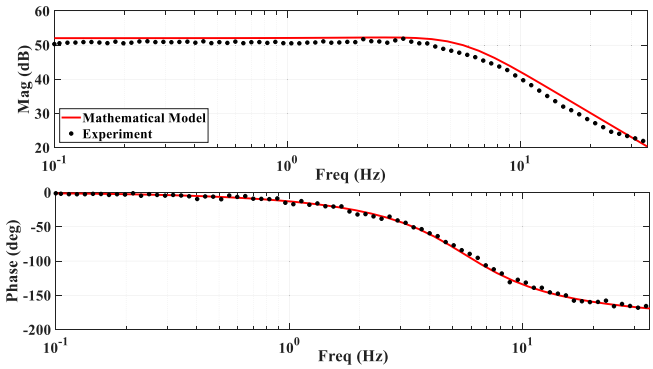

Fig. 13. $D_S(s)$ to $V_{VB}(s)$ transfer function. The input used for system identification is a two-period 11-bit PRBS with clock frequency of 100 Hz.

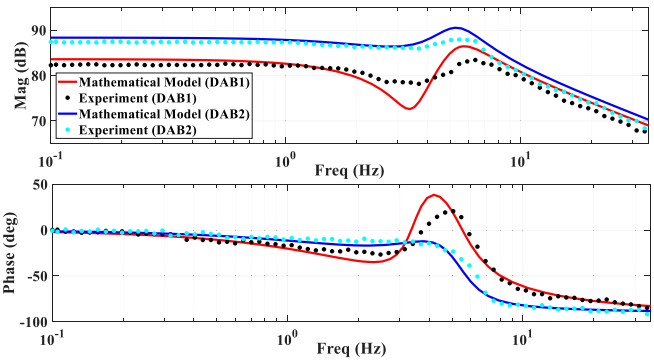

Fig. 14. $\Phi_i(s)$ to $V_{IB_i}(s)$ transfer functions. The input used for system identification is a two-period 11-bit PRBS with clock frequency of 100 Hz.

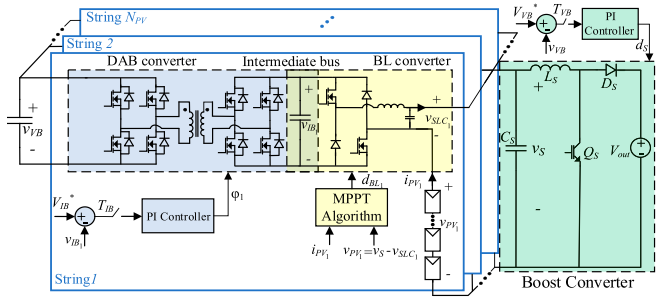

Fig. 15. PV2VB PDPP architecture with its control loop block diagrams.

implemented using an STM32H723 advanced Arm®-based 32-bit MCU. PRBS signal is applied by the microcontroller and was injected to the boost duty cycle. Then, the virtual bus voltage was divided by high precision resistors and measured using a TA041 differential oscilloscope probe (10:1) and then collected by a YOKOGAWA DLM5038 oscilloscope.

Although the microcontroller includes PI controllers for closed-loop output voltage regulation, the experiments for system identification were conducted in open loop. The input and the output data collected by the oscilloscope were transmitted to a computer for offline processing in the MATLAB/Simulink environment. The architecture parameters and system's operating point remain the same as in the PLECS simulation example in Section III (Tables I and II), but the PRBS parameters are different (Table III).

The spectral analysis method described in Section III-A is used to identify the $D_S(s)$ to $V_{VB}(s)$ transfer function of the architecture. The PRBS was stored in the microcontroller and injected onto the duty cycle of central converter. Using the same procedure, the Bode plots of the $\Phi_i(s)$ to $V_{IB_i}(s)$ transfer functions were obtained experimentally. Figs. 13 and 14 illustrate a comparison between the frequency response obtained from the mathematical model and the one obtained experimentally through system identification. The analysis demonstrates a good alignment between responses across the tested frequency range, thereby validating the proposed mathematical model of the PV2VB PDPP architecture. Note that, due to their slow transient response, PV emulators cannot accurately represent PV strings at high frequencies, limiting the experimental results to less than 50 Hz. However, for DAB converters, the experimental results (Fig. 14) effectively capture the transition band, which is the critical part of the Bode plot. Additionally, as discussed in Section IV-A, for the $D_S(s)$ to $V_{VB}(s)$ transfer function (Fig. 13), the low-frequency band is the most important for controller design.

In the PV2VB PDPP architecture's normal operation, tracking the MPP of PV strings is crucial and achieved via MPPT algorithms. The widely used P&O algorithm adjusts the duty cycle of BL converters, causing periodic perturbations in the PV string's operating point at regular interval, known as the perturbation period. These perturbations induce oscillations on the virtual bus, which can be mitigated in the proposed prototype by an 11.2 mF virtual bus capacitor. However, this capacitor attenuates frequency content in its voltage response to the PRBS signal and decreases the signal-to-noise ratio.

Thus, although for system identification a 1.2 mF capacitor has been utilized at the virtual bus, in Section IV the controllers are designed for a virtual bus capacitance of 11.2 mF.

IV. Controllers Design Considerations

Fig. 15 illustrates the PV2VB PDPP architecture alongside its control structures. In this architecture, the central converter regulates the virtual bus voltage by adjusting the main bus voltage, while the primary responsibility of the SLCs is to track the MPP of the PV strings. Although the BL converter handles MPP tracking, fluctuations in the intermediate bus voltages can adversely affect the performance of MPP tracking. Thus, the DAB converter must effectively regulate these intermediate bus voltages to ensure stable and efficient operation. Considering a search-based MPPT algorithm like P&O, the system inherently has two categories of feedback (error-based) control loops: one central converter controller and N_{PV} DAB converter controllers (Fig. 15).

The first control loop is the central converter controller aiming to maintain the voltage of the virtual bus at the desired level by controlling the duty cycle of the boost converter. The second controller governs the DAB converters, focusing on regulating intermediate bus voltages through the DAB converters phase shifts. Thus, two types of transfer functions are our interest: (i) $D_S(s)$ to $V_{\mathrm{VB}}(s)$ and (ii) $\Phi_i(s)$ to $V_{\mathrm{IB}_i}(s)$:

$$G_{\frac{V_{\mathrm{VB}}}{D_S}}(s)=\frac{V_{\mathrm{VB}}(s)}{D_S(s)}\left|\begin{array}{l}\Phi_j(s)=0,\ j=1,\ldots,N_{\mathrm{PV}}\\ D_{\mathrm{BL}_j}(s)=0,\ j=1,\ldots,N_{\mathrm{PV}}\end{array}\right. \tag{37}$$

$$G_{i\,\frac{V_{\mathrm{IB}_i}}{\Phi_i}}(s)=\frac{V_{\mathrm{IB}_i}(s)}{\Phi_i(s)}\left|\begin{array}{l}\Phi_j(s)=0,\ j=1,\ldots,N_{\mathrm{PV}},\ j\neq i\\ D_{\mathrm{BL}_j}(s)=0,\ j=1,\ldots,N_{\mathrm{PV}}\\ D_S(s)=0\end{array}\right. . \tag{38}$$

Both voltage control loops are essential for maintaining the voltages within specified limits, ensuring system stability, and improving system performance. Here an indirect technique has been used for designing discrete PI controllers; so initially, the continuous-time controllers are designed in the s-domain by using MATLAB SISOtool. Then, based on the continuous-time controller, the discrete-time controller is calculated by Tustin transformation.

A. Central Converter Controller

To prevent interference between the central controller and to enable the MPPT algorithms to autonomously seek the MPP of the PV string, it is preferable to increase the sampling time of the central PI controller to minimize its interference with the MPPT algorithm as follows:

$$T_{\mathrm{VB}}=4\cdot m\cdot T_{\mathrm{MPPT}}|_{m=1,2,\ldots}. \tag{39}$$

However, if the sampling period is too long, the discrete-time PI controller may not yield satisfactory results. In practical terms, for a broad range of systems, the sampling period is typically chosen to be at most half of the slowest time constant [31]. The slowest time constant in the architecture is 300 ms with parameters outlined in Table I (except for C_{VB} which is 11.2 mF) and a 15 ms for the perturbation period of the MPPT algorithm (T_{MPPT}) has been chosen. Therefore, a sampling time of 60 ms, which is equal to 4 times T_{MPPT}, is selected for the central controller. In this article, the criteria for designing the PI controller parameters of the central converter are phase margin and bandwidth. A phase margin of approximately 60 degrees is considered for compensated system to ensure a reasonable stability margin and mitigate the effects of uncertainties and variations—such as dynamic resistance of PV strings r_{PV}—in the system. Additionally, to achieve satisfactory accuracy, the sampling time of the discrete-time PI controller must be 20 times faster than the highest bandwidth frequency [31]. Hence, a bandwidth of 1 Hz is chosen for designing the central converter's PI controller.

TABLE IV
Controllers Parameters

	Parameter	Symbol	Value
Central controller	Sampling time	T_{VB}	60 ms
	Proportional coefficient*	$K_{p_{\mathrm{VB}}}$	0.003
	Integral coefficient	$K_{I_{\mathrm{VB}}}$	0.015
DAB controllers	Sampling time	T_{IB}	10 μs
	Proportional coefficient	$K_{p_{\mathrm{IB}}}$	0.0005
	Integral coefficient	$K_{I_{\mathrm{IB}}}$	0.01

Note: $^{*}K_p+K_I/s$, K_p is Proportional Coefficient, K_I is Integral Coefficient.

B. DAB Converters Controllers

In contrast to the central converter controller, there is no specific lower limit for the sampling time of DAB converters. Hence, the sampling frequency of the PI controller can be set as fast as the switching frequency of the DAB converter, which is 100 kHz, to enhance response time and reduce phase lag in the system. The criteria for designing the DAB converters PI controllers are phase margin and settling time. It is preferable for the settling time of the intermediate bus voltages to be lower than the perturbation period of the MPPT algorithm ($T_{\mathrm{IB}}<T_{\mathrm{MPPT}}$) to minimize interference. As for the central converters PI controller, a phase margin of approximately 60 degrees is considered. Lastly, the parameters of the controllers are designed for the architecture with the parameters outlined in Table I (except for C_{VB}, which is 11.2 mF) and the operating point specified in Table II. The controllers' parameters are shown in Table IV.

C. Stability Analysis

Fig. 16 presents the Bode plot for the open-loop $D_S(s)$ to $V_{\mathrm{VB}}(s)$ transfer function, both compensated and uncompensated, at three different PV String 1 voltages (V_{PV1}). The remaining operating point variables are detailed in Table II. As illustrated in Fig. 16, when the PV String 1 voltage is equal to 267 V, the phase margin of the compensated $D_S(s)$ to $V_{\mathrm{VB}}(s)$ transfer function is approximately 60 degrees (indicated by the red dashed line). When the voltage of PV String 1 decreases from 267 to 160 V, a slight increase in the phase margin is observed, suggesting improved stability with greater mismatches between PV strings. Conversely, when the voltage increases from 267 to 375 V, the phase margin decreases, leading to reduced system stability. This poor stability occurs

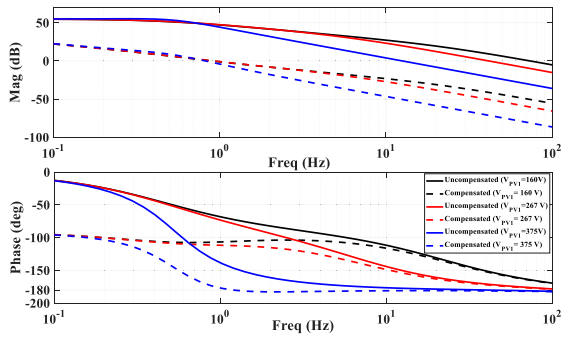

Fig. 16. Bode plot of the compensated and uncompensated open-loop $D_S(s)$ to $V_{VB}(s)$ transfer function at different operating points.

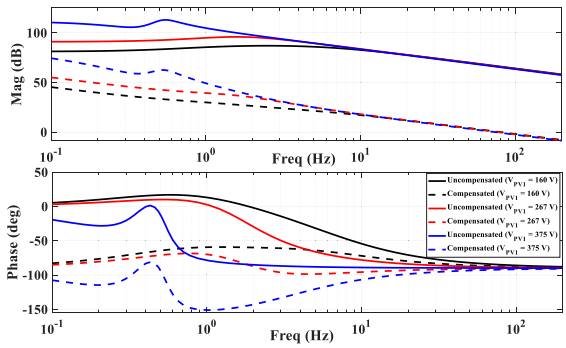

Fig. 17. Bode plot of the compensated and uncompensated open-loop $\Phi_1(s)$ to $V_{IB_1}(s)$ transfer function at different operating points.

because, at a PV string voltage of 375 V, the phase of the uncompensated transfer function (blue solid line) drops sharply near the selected bandwidth frequency. This behavior arises as increased voltage in PV String 1 reduces mismatch among PV strings, lowering the power processed by the SLCs. Note that low power operation of SLCs can also result from reduced PV string current. While lowering the bandwidth could mitigate this issue, it would also result in a slower transient response at other operating points. Therefore, for central converters, gain scheduling or other advanced control strategies such as model predictive control (MPC) and sliding mode control (SMC) are recommended to enhance performance, stability, and adaptability [32].

Fig. 17 shows the bode plot for the open-loop $\Phi_1(s)$ to $V_{IB_1}(s)$ transfer function, both compensated and uncompensated, evaluated at the same operating points as in Fig. 16. The phase margin of uncompensated transfer function remains at 90 degrees across all three operating points, and the bandwidth, which defines the speed of the transient response, stays around 70 Hz. Thus, a simple PI controller can be sufficient for DAB converters across different operating points.

V. Experimental Results

To evaluate the performance of the PI controllers and their capability to manage disturbances, two different PV string curves, as shown in Fig. 18, are utilized. The operating point of PV string 1 experiences a significant and abrupt drop from 390 to 300 V as it transitions from generating I–V curve 1 to I–V curve 2 at 0.07 s (highlighted with a vertical green line in Fig. 19), whereas PV string 2 continues generating I–V curve 1.

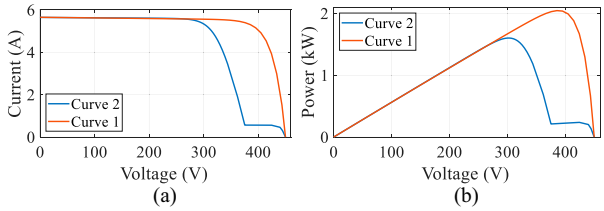

Fig. 18. PV string's (a) I–V curves. (b) P–V curves used in the experiments.

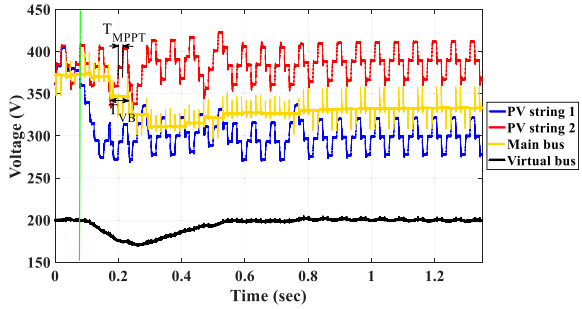

Fig. 19. Voltage waveforms in the PV2VB PDPP architecture. PV string 2 stays at I–V curve 1, whereas PV string 1 transitions from I–V curve 1 to I–V curve 2 after 0.07 s, highlighted with the green line.

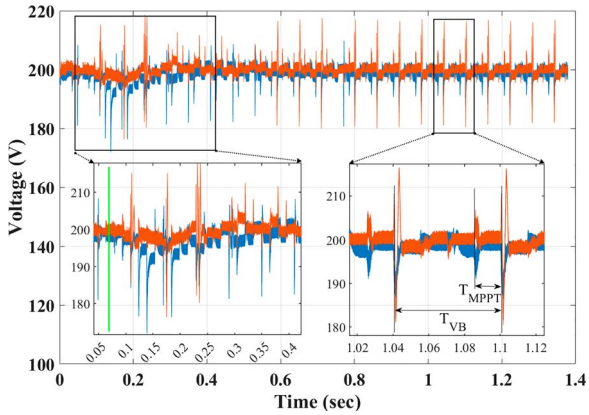

Fig. 20. Transition of intermediate bus voltages in the PV2VB PDPP architecture (blue: V_{IB_1}, red: V_{IB_2}).

Fig. 19 illustrates that the central controller with a sampling time of 60 ms can effectively handle the disturbances, restoring the virtual bus to its initial state within less than 600 ms by determining a new operating voltage for the main bus. Simultaneously, the MPPT algorithm ensures that PV strings operate at their MPP. Fig. 19 proves the system's ability to independently find the MPP of both PV strings with the typical behaviour of P&O algorithm, with a perturbation period of 15 ms and a perturbation step size of 5% applied to the duty cycle.

Fig. 20 depicts the intermediate bus voltages of the architecture. The PI controllers of the DAB converters demonstrate their effectiveness in managing disturbances, successfully bringing back the intermediate bus voltages to 200 V after the abrupt change in the operating conditions of PV string 1. Additionally, the PI controller is capable of handling disturbances caused by the MPPT algorithm and central converter within 15 ms. It

ensures that disturbances on intermediate bus voltages do not interfere with the operation of the MPPT and central controller.

VI. Conclusion

This article provided a thorough analysis of the dynamic behavior of the PV2VB PDPP architecture and its mathematical model, crucial for designing and tuning controllers. The mathematical model was validated through system identification based on the data acquired from both PLECS simulation and experiments, ensuring its applicability in real-world scenarios. Considering the control requirements, the controller parameters were designed with a settling time of 15 ms, which corresponds to the MPPT perturbation period, for the DAB controllers, a bandwidth of 1 Hz for the central converter's PI controller, and a phase margin of 60 degrees for both. The transient response and system stability were validated through experimental tests. These tests confirmed the system's stability, demonstrating the central controller's ability to stabilize the virtual bus voltage to the desired level within 0.6 s, while the intermediate bus voltages settled within 15 ms.

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