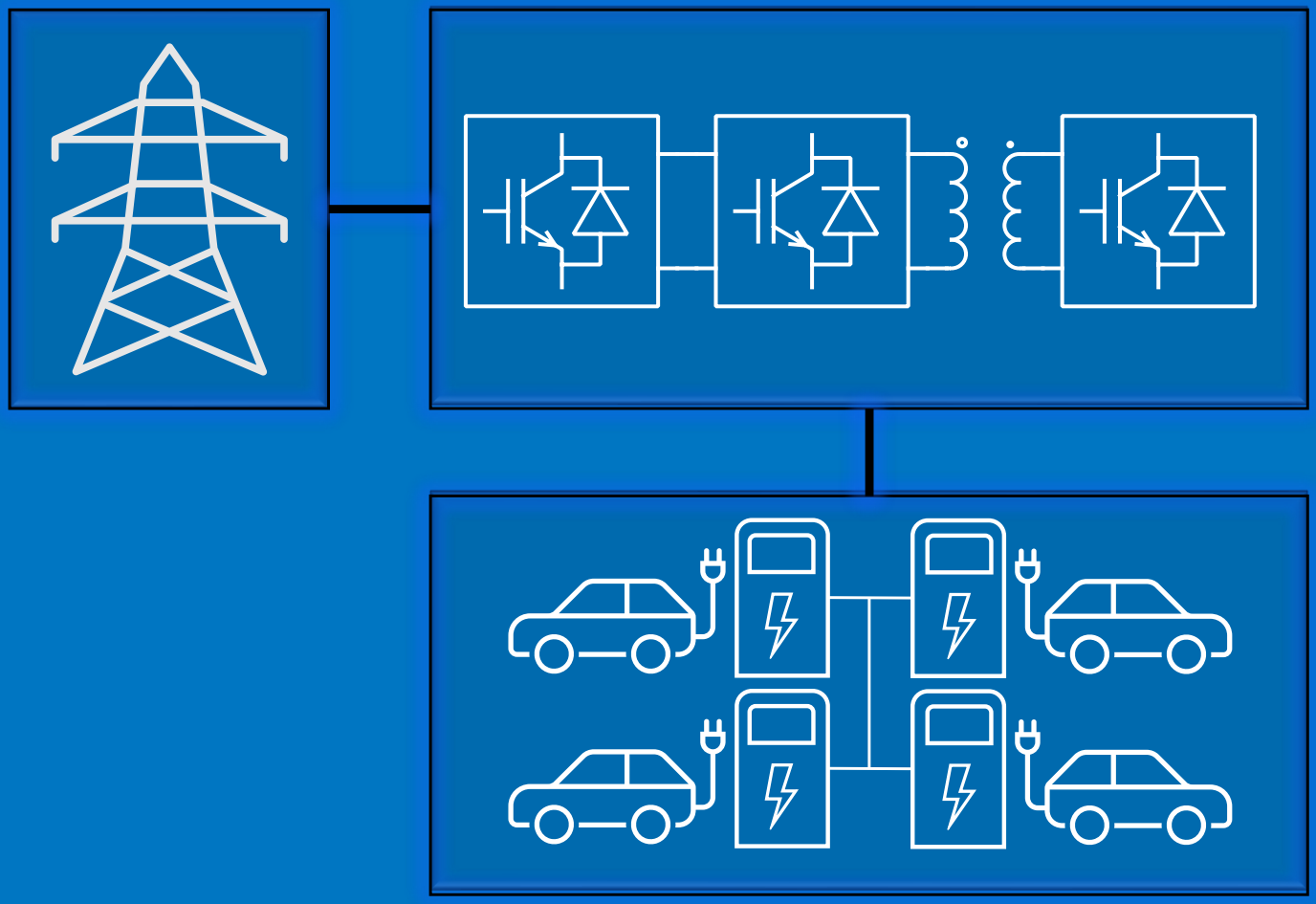
# Modelling, Control System Design and Comparison of Star and Delta Connected Solid-State Transformers

## A study of three MVAC to LVDC Modular Multilevel Converter based Solid State Transformers for Ultra-Fast EV Charging Applications

Casper Grootes

Delft University of Technology



TU Delft

# Modelling, Control System Design and Comparison of Star and Delta Connected Solid-State Transformers

## A study of three MVAC to LVDC Modular Multilevel Converter based Solid State Transformers for Ultra-Fast EV Charging Applications

by

Casper Grootes

to obtain the degree of Master of Science
at the Delft University of Technology,
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| | |
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Cover: EV Charging Station Connected to the MVAC grid through an SST

TU Delft

# Abstract

With an increase in higher power (ultra) fast EV charging stations and a new EU law for mandatory deployments of EV charging stations, an optimal MVAC grid connection for these charging stations is desired. Considering this connection, the use of a solid-state transformer (SST) performs better in terms of weight, size and efficiency with a similar cost, compared to the conventional low-frequency transformer (LFT) for MVAC to LVDC conversions. This study compares three MMC-based SST topologies where a DAB is connected to each submodule: Double-Star, Single-Star and Single-Delta. The cost of an MMC mainly depends upon the required energy storage and the switch stress. The topologies are therefore mainly compared based on these parameters, but other parameters are considered as well. With the goal of minimising the required energy storage, an 80% MMC energy storage reduction compared to the theoretical minimum requirement has been achieved by control.

A novel mathematical model has been proposed for each SST; this uses an MMC model based on the switching function and a DAB model based on the single phase-shift control. The model has been implemented in simulation and proven to accurately determine the average behaviour of the SST while significantly reducing the simulation complexity and time. This model helps to understand the SST's behaviour and furthermore allows for control system tuning both manually and automatically using the Genetic Algorithm.

Three different control systems have been designed. Control system A, where the MMC current is controlled by the average submodule voltage and the DAB controls the LVDC bus voltage. Control system B, where the DAB controls each individual submodule voltage and the MMC current is controlled by the LVDC bus voltage. Control system C, which is similar to control system B, but uses a stable DC voltage source on the LVDC bus and a set MMC current. An improved DAB control has been designed for control systems B and C, resulting in control systems B* and C*. This control is based on the use of a current feedforward and a PI controller combined with the inverted equations of the DAB model. The three topologies have been successfully simulated with this improved DAB control system using an 80% MMC energy storage reduction compared to the theoretical minimum requirement. This improves the general behaviour and significantly reduces the cost of the SST. The improved DAB control system has been tested using a hardware DAB with a current step input, which has shown that the new control system performs better in voltage peak reduction compared to PI control.

Out of the three topologies, the Single-Star topology performs the best. It has the lowest energy storage requirement and switch stress. Furthermore, its behaviour lies the closest to the ideal model. The best result for the Single-Star SST is achieved with the proposed improved DAB control, which leads to the lowest energy storage requirement, switch stress, THD, submodule voltage deviations and settling time. Out of these two control systems, C* performs the best.

# Acknowledgement

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I would like to thank Adnan Ahmad for his support during the start of the thesis and the initial draft of the 1MVA MMC.

# Contents

# Nomenclature

## Abbreviations

| Abbreviation | Definition |
|---|---|
| AC | Alternating Current |
| APOD | Alternating Phase Opposition Disposition |
| BESS | Battery Energy Storage System |
| CHB | Cascaded H-Bridge |
| DAB | Dual Active Bridge |
| DC | Direct Current |
| EU | European Union |
| ESR | Equivalent Series Resistance |
| EV | Electric Vehicle |
| FB | Full Bridge |
| FFT | Fast Fourier Transform |
| FFW | Feedforward |
| FI | Full Insertion |
| HB | Half Bridge |
| HFT | High Frequency Transformer |
| HI | Half Insertion |
| LFT | Low Frequency Transformer |
| LPF | Low Pass Filter |
| LSC | Level Shifted Carrier |
| LV | Low Voltage |
| MMC | Modular Multilevel Converter |
| MV | Medium Voltage |
| NLC | Nearest Level Control |
| PD | Phase Disposition |
| PSC | Phase Shifted Carrier |
| PSCLAS | Phase SHifted Carrier Lower Arm Shifted |
| POD | Phase Opposition Disposition |
| PWM | Pulse Width Modulation |
| RMS | Root Mean Square |
| SM | Submodule |
| SSE | Sum Square Error |
| SST | Solid State Transformer |
| TEN-T | trans-European transport |
| THD | Total Harmonic Distortion |

# Symbols

| Symbol | Definition | Unit |
|---|---|---|
| $C$ | Capacitance | [F] |
| $E$ | Energy | [J] |
| $f$ | Frequency | [Hz] |
| $I$ | Current | [A] |
| $L$ | Inductance | [L] |
| $m$ | Modulus | [pu] |
| $N$ | Amount of Submodules per arm | - |
| $n$ | Transformer Turn Ration | - |
| $P$ | Active Power | [W] |
| $R$ | Resistance | [Ω] |
| $S$ | Apparent Power | [VA] |
| $t$ | Time | [s] |
| $V$ | Voltage | [V] |
| $\alpha$ | DAB Power Scale | [pu] |
| $\theta$ | Phase Shift | [rad] |
| $\tau$ | Time Constant | [s] |
| $\phi$ | Relative DAB Phase Shift | [pu] |
| $\omega$ | Radial Frequency | [rad/s] |

# Introduction

On the 11th of December 2019, the European Union first presented the European Green Deal, a plan to reduce the emission of greenhouse gasses by 55% by 2030 and completely by 2050 [1]. As part of the green deal, the European Union will end the sale of new $CO_2$ emitting cars by 2035 [2]. Therefore, there will be an increase in zero-emission cars such as the electric vehicle (EV), which in turn will result in an increased need for a good EV charging infrastructure across the European Union. In March 2023, the European Union passed a new law as part of the Green Deal: The new Regulation for the deployment of alternative fuels infrastructure (AFIR). This law sets mandatory deployment targets for electric recharging infrastructure for the road sector. From 2025 onward, the core trans-European transport (TEN-T) network will require a fast charging station for EVs of at least 150kW, and a heavy-duty charging station of 350kW every 60 km. [3]. On July 13th 2023, a new law was passed with mandatory deployment targets up to 2035 [4]. The full overview of the mandatory deployment targets is presented in [5], including total charging pool requirements of up to 3.6MW by 2030 for heavy-duty electric vehicles. Tables 1.1 and 1.2 present the full overview of the targets. A 3.6MW charging pool connected to the conventional low voltage three-phase 400V alternating current (LVAC) grid, would result in an undesirably high phase current of approximately 5.2kA. High-power EV charging can have undesired impacts on the grid [6, 7].

Connecting such a charging station to the medium voltage alternating current (MVAC) grid of 10kV might be a better alternative. For this, a solid-state transformer (SST) can be considered, directly connecting an 800V low voltage direct current (LVDC) bus to the 10kV MVAC grid. [8]

## Project Objective

This project will consider the use of a modular multilevel converter (MMC) based 3.5MVA solid-state transformer (SST) to connect the 10kV MVAC grid to an 800V LVDC EV charging station. Both star- and delta-connected SSTs, including their control systems, will be considered and compared. The main costs of an MMC are determined by the submodule costs, consisting of the switch cost (dependant on $V$, considering a single current rating) and the capacitor cost (dependent on $V^2$ for electrolytic capacitors) [9]. Therefore, the different topologies will be compared on the total switch stress of the MMC and the total stored energy ($CV^2$) in the MMC. Furthermore, a control system will be developed for the SST while investigating the potential of using the control system to reduce the stored energy.

## Used Methodology

To obtain the desired results of the project objective, the following steps and methodology will be used:

1. **Literature Evaluation:** Existing literature will be reviewed, considering MMCs and SSTs, on the design choice possibilities and potential configurations to be considered.
2. **Modeling of the MMC/SST:** Mathematical modelling of the converter will be done in order to understand its behaviour, and potentially help with the control system tuning.
3. **Control System Design:** Various control systems for the SST will be designed. This includes their potential for reducing the stored energy in the MMC and their tuning.
4. **Simulation:** Simulations of the different topologies and their control system will be built in PLECS [10]. The simulation results will be used for the comparison.
5. **Hardware test:** A hardware test is done to validate the improved DAB control system.
6. **Conclusion:** The gathered results of the simulations and hardware test will be summarised and used to draw a conclusion about the different topologies and control systems.

This thesis report is divided into chapters according to the methodology used. A publication draft about the developed mathematical SST model and its ability to help with the control system tuning using the genetic algorithm is given in appendix A.

# 1

# Background Information and Literature Evaluation

## 1.1. EV Charging

On July 13th 2023, the European Union passed the law which includes the mandatory targets for EV Charging stations across the EU. Tables 1.1 and 1.2 represent these targets for electric cars, vans and heavy-duty vehicles, across the trans-European transport (TENT-T) Road Network.

| Target Date | EV Recharging Type | TENT-T Core Road Network | TENT-T Comprehensive Road Network |
|---|---|---|---|
| 31-12-2025 | Individual Charger | 150kW | - |
| | Charging Pool | 400kW | - |
| 31-12-2027 | Individual Charger | 150kW | 150kW along 50% |
| | Charging Pool | 600kW | 300kW along 50% |
| 31-12-2030 | Individual Charger | - | 150kW |
| | Charging Pool | - | 300kW |
| 31-12-2035 | Individual Charger | - | 150kW |
| | Charging Pool | - | 600kW |

**Table 1.1:** EU EV-Charging infrastructure targets for cars and vans, to be placed at least every 60 km [5]

| Target Date | EV Recharging Type | TENT-T Core Road Network | TENT-T Comprehensive Road Network |
|---|---|---|---|
| 31-12-2025 | Individual Charger | 350kW along 15% | |
| | Charging Pool | 1.4MW along 15% | |
| 31-12-2027 | Individual Charger | 350kW along 50% | 350kW along 50% |
| | Charging Pool | 2.8MW along 50% | 1.4MW along 50% |
| 31-12-2030 | Individual Charger | 350kW | 350kW every 100 km |
| | Charging Pool | 3.6MW | 1.5MW every 100 km |

**Table 1.2:** EU EV-Charging infrastructure targets for heavy-duty vehicles, to be placed at least every 60 km[1] [5]

An overview of extra fast electric vehicle charging technologies is given in [11], including EV charging up to 350kW where a 200-mile driving range can be added within 10 minutes of charging. Furthermore, the usage of 800V batteries has already been reported to allow these charging power rates due to cable weight limitations [8]. Cable weight limitations allow charging of 400V DC up to 200kW and 800V DC up to 350kW, as 800V DC charging requires a less heavy cable due to the lowered cable current [11]. Due to the requirements set by the European Union of table 1.2, 800V DC will be required to allow these charging rates. Even higher power ratings can be considered using multilevel medium voltage connected charging topologies [12]. An overview of the impact on the grid of EV-Charging is given in [7].

With these trends, it is clear that DC EV-Chargers operating on at least 800VDC are required to meet the mandatory charging infrastructure targets set by the European Union [5]. To allow for the total charging pool power ratings, a SST-based connection of DC charging station of at least 800V to the MVAC grid is to be considered [8, 12].

[1] With the exception of the target heavy-duty vehicle charging stations along the TENT-T Comprehensive Road Network, which need to be placed at least every 100 km

## 1.2. The Modular Multilevel Converter

The modular multilevel converter (MMC) is the most fundamental building block of the considered solid-state transformer (SST). This chapter will briefly describe the background of the MMC as this information is essential for understanding MMC-based SSTs.

With a need for a DC to AC conversion at higher voltage the typical two-level voltage source inverter (VSI) will not suffice due to the limited blocking voltage of the available switches. By using a multilevel topology the DC-link voltage can be divided across multiple switches allowing for higher DC-link voltages and therefore higher power [13]. The Double-Star Modular Multilevel converter is presented in [14].

A MMC consists of multiple armss, each consisting of N number of submodules (SMs) and an inductor. Figure 1.1 shows the configuration of such an arm as well as the equivalent symbol for an MMC arm, which is used in other figures.

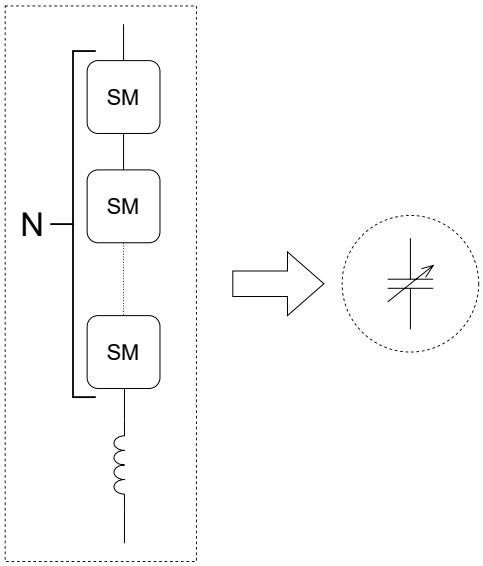
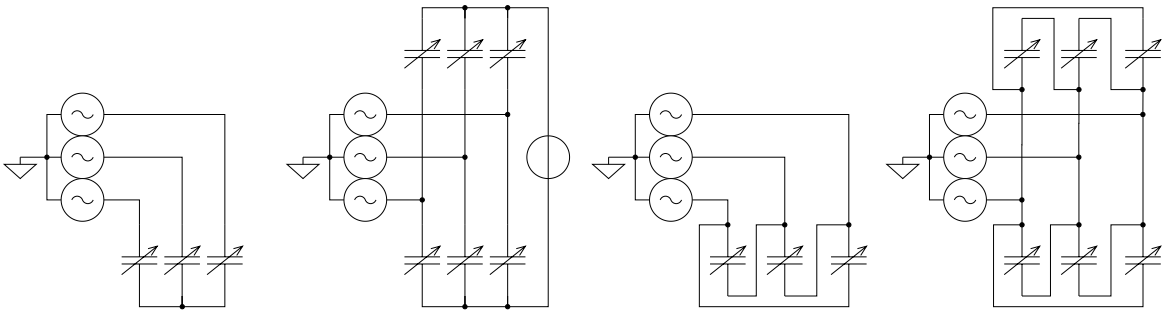



**Figure 1.1:** Single MMC Arm

A review of MMCs for stationary applications is presented in [15]. Neglecting AC-AC conversion topologies gives four topologies: Single- and Dual-Star, and Single- and Dual Delta. Figure 1.2 shows these four topologies of which the Double-Star (Figure 1.2b) is the most commonly used as it provides a DC-Link. The Double-Star, Single-Star and Single-Delta topologies are the considered MMC topologies to be compared. The initial MMC analysis is done for the Double-Star MMC topology as this is the most-used and most-complex.

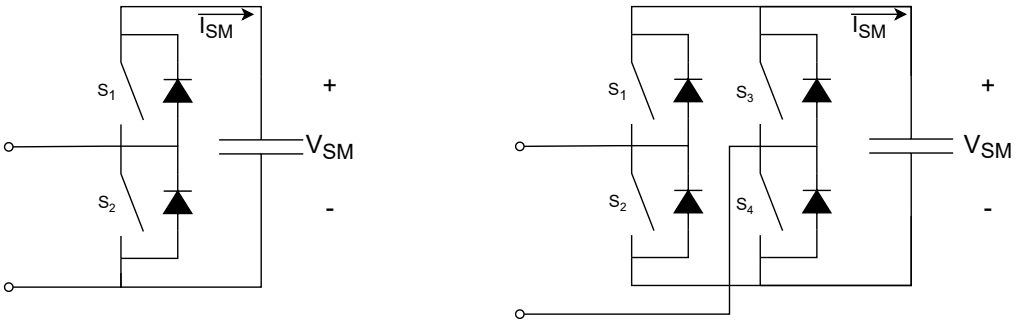


**(a)** Single-Star Configuration **(b)** Double-Star Configuration **(c)** Single-Delta Configuration **(d)** Double-Delta Configuration

**Figure 1.2:** Different MMC Topologies

## 1.3. The MMC Submodule

The submodule of a MMC usually consists of a capacitor and switches. The half-bridge submodule is presented in [14]. Many other submodule types exist some of which are presented in [15–17]; this includes multilevel, current source, and other topologies. The second most commonly used and considered submodule is the full-bridge, sometimes referred to as H-bridge, submodule. The full bride submodule can insert the positive and negative submodule voltage, while being more robust towards DC-faults [18]. The half-bridge SM can only insert the positive submodule voltage and is less tolerant towards DC faults; however, it is easier to implement due to its simplicity. Figure 1.3 shows the half-bridge submodule (figure 1.3a) and the full-bridge submodule (figure 1.3b).




**(a)** Half Bridge Submodule (HBSM)

**(b)** Full Bridge Submodule (FBSM)

**Figure 1.3:** Most commonly used MMC SM's

The Half-Bridge Submodule (HBSM) and the Full-Bridge Submodule (FBSM) will be the two considered submodules in this report, as these are the most commonly used. The HBSM can be used for the double-star configuration (Figure 1.2b) as the upper legs provide only the positive voltage and the lower the negative. For the single-star (Figure 1.2a) and delta (Figure 1.2c) configurations, a FBSM is required due to the need to insert both positive and negative voltages in each arm.

## 1.4. MMC Modulation Techniques

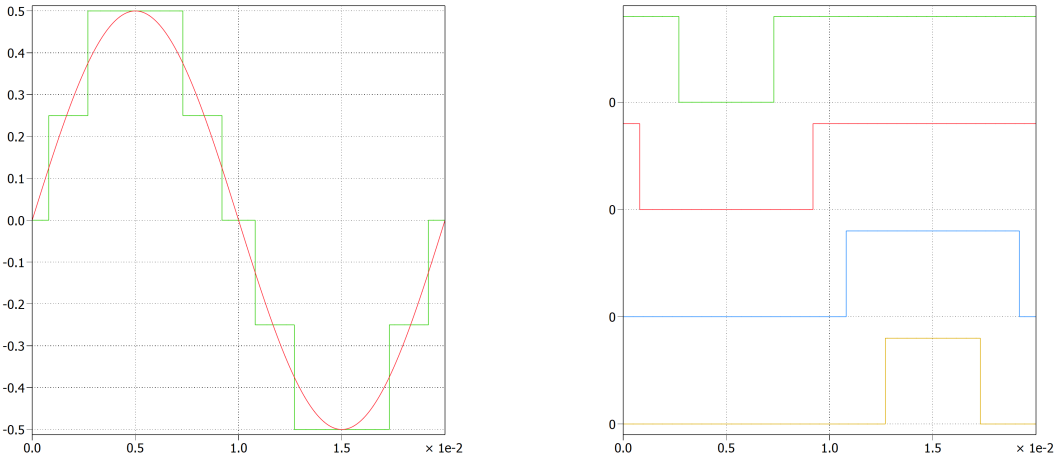
To control the submodules with an AC reference signal, a modulation technique is required to create the desired switching signals. These switching signals then control the gate of the switches in order to insert or bypass the submodule (HBSM), or to insert a positive or negative voltage (FBSM). These modulation techniques can be divided into three categories:

- Nearest Level Control (NLC)
- Level Shifted Carrier (LSC)
- Phase Shifted Carrier (PSC)

A preliminary research has been done comparing various modulation techniques and their effects on Harmonics, Total Harmonic Distortion (THD), complexity, internal voltage and circulating current. NLC, the three most common LSC methods and the two most common PSC methods will be briefly summarised. The results of which have been obtained in this preliminary research. [19]

### 1.4.1. Nearest Level Control (NLC)

Nearest Level Control is the most simple form of modulation for MMCs. The amplitude of the AC reference signal is rounded to the nearest level and the required amount of submodules are inserted. The generated voltage is now a stepped version of the reference voltage with N+1 levels. Figure 1.4 shows the control signals of the MMC.




**(a)** Sinusoidal reference and its nearest levels

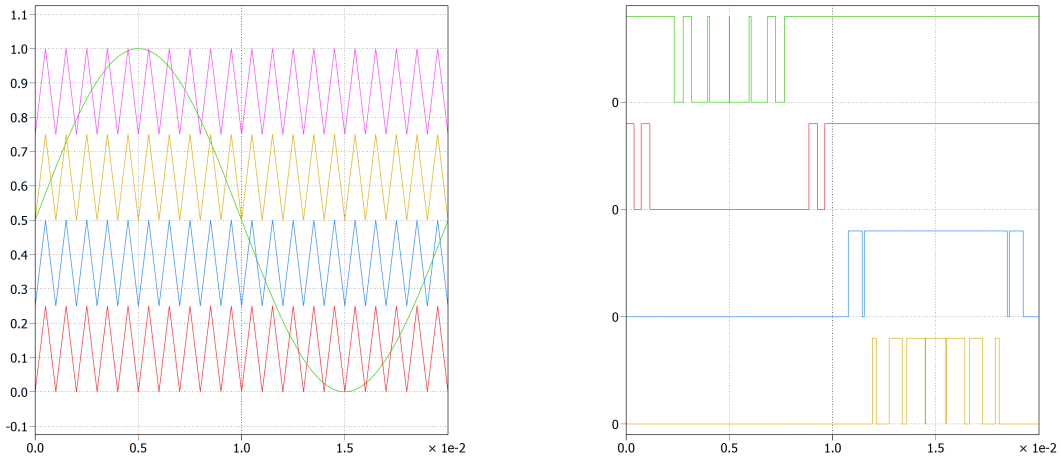
**(b)** Generated PWM signals

**Figure 1.4:** Nearest Level Control (NLC) width N=4

The higher the number of submodules used, the less the THD will be, therefore this technique is mostly applied with higher numbers of submodules (e.g. N>10). With NLC the total energy drawn or given to each submodule will not be equal and therefore a sorting algorithm for voltage balancing will be required.

### 1.4.2. LSC: Phase Disposition (PD)

Phase Disposition (PD) is the simplest Pulse Width Modulation (PWM) using N-level shifted carriers. The N amount of carriers are equally distributed between 0 and 1 and compared to the AC reference, which is also between 0 and 1. The outputs of the comparators give the control signals for the submodules. Figure 1.5 shows this.




**(a)** Sinusoidal reference and the carriers

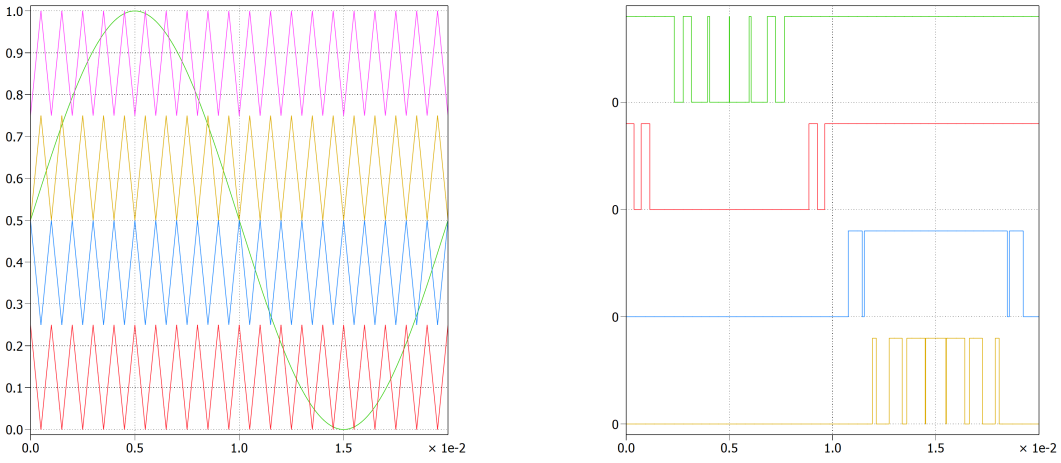
**(b)** Generated PWM signals

**Figure 1.5:** Phase Disposition (PD) with N=4

PD similarly to NLC will not give an equal energy distribution between the submodules and will therefore require voltage balancing. Furthermore, the THD will be lower than NLC for a low N and higher for a high N. The main downside of PD is the undesired voltage spikes introduced on the internal voltage.

### 1.4.3. LSC: Phase Opposition Disposition (POD)

Phase Opposition Disposition (POD) is similar to PD but with the phase of the lower half carriers being inverted. Figure 1.6 shows these carriers.




**(a)** Sinusoidal reference and the carriers

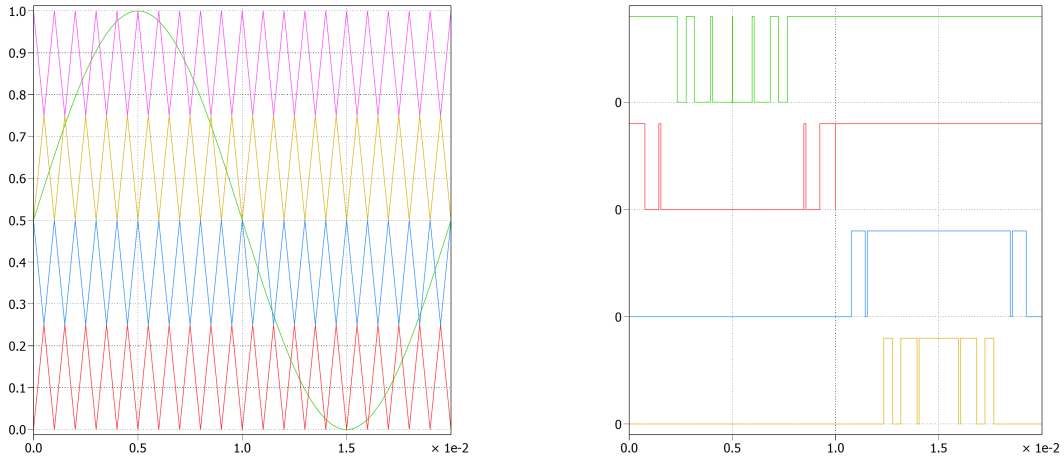
**(b)** Generated PWM signals

**Figure 1.6:** Phase Opposition Disposition (POD) with N=4

The advantage of the inverted phase is the removal of the undesired voltage spikes, this comes at the cost of increased THD compared to PD. POD, like PD, has an uneven energy distribution between the submodules and requires voltage balancing.

### 1.4.4. LSC: Alternating Phase Opposition Disposition (APOD)

Alternating Phase Opposition Disposition (APOD) is similar to PD, but with each odd harmonic being inverted. Figure 1.7 shows these carriers.




**(a)** Sinusoidal reference and the carriers

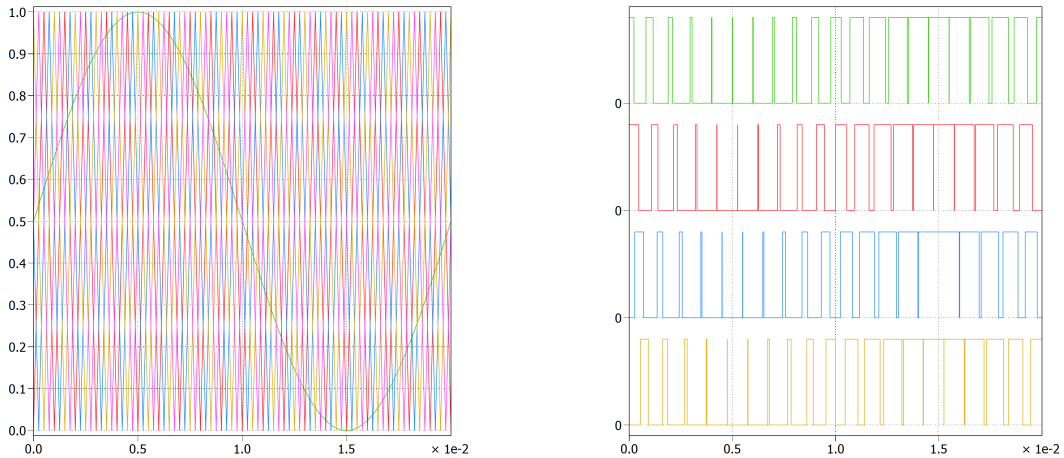
**(b)** Generated PWM signals

**Figure 1.7:** Alternating Phase Opposition Disposition (APOD) with N=4

The properties of APOD are comparable to POD. According to most literature, the THD of APOD is reduced compared to POD. The preliminary research has shown cases where this is not true. APOD, like all LSC modulations, will have an uneven energy distribution between the submodules and requires voltage balancing.

### 1.4.5. PSC: Phase Shifted Carrier

The Phase Shifted Carrier (PSC) modulation consists of N carriers which are shifted in phase by $\frac{2\pi}{N}$ rad. The reference AC waveform is then compared to these carriers to create the desired switching signals for the submodules. Figure 1.8 shows the phase-shifted carrier.




**(a)** Sinusoidal reference and the carriers

**(b)** Generated PWM signals

**Figure 1.8:** Phase Shifted Carrier (PS) with N=4

Phase-shifted carrier modulation presents an equal energy distribution between the submodules, eliminating the need for voltage balancing by sorting. Furthermore, it has reduced THD compared to POD, APOD, and NLC with low N. It is the technique with the most switching commutations per submodule and will therefore most likely result in the highest switching losses compared to LSC and NLC.

### 1.4.6. PSC: Phase Shifted Carrier with Lower Arm Shifted

When using a phase-shifted carrier modulation, it is also possible to shift the carriers of the lower arm by $\frac{\pi}{N}$ rad compared to the upper arm (PSCLAS). Figure 1.9 shows this shift.

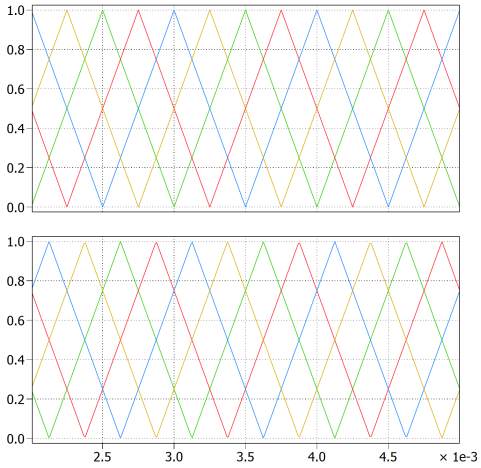



**Figure 1.9:** Upper and Lower arm Carriers of Phase Shifted Carrier Lower Arm Shifted (PSCLAS)

Compared to PSC, PSCLAS eliminates the Nth harmonic of the switching frequency which can result in a reduction of the THD. However, the preliminary research has shown that this can also introduce the earlier mentioned voltage spikes.

For the solid-state transformer equal power flow per submodule is desired. The reasoning behind this is explained in section 1.5. Because of this, PSC is required. To avoid voltage spikes the regular PSC method without shifting the lower arm will be used.

## 1.5. The Solid State Transformer

A solid-state transformer (SST) topology which generates a LVDC bus from the MVAC grid is desired. Concepts of the SST date back to the 1960s with five main types: Matrix type, isolated front end, isolated back end, isolated modular multilevel converter, and single-cell approach [20], where the isolated modular multilevel converter is the considered SST type in this research. Multiple SST topologies are presented and compared in literature [20–31]. Note that in some of this literature, a Single-Star or Single-Delta MMC configuration is referred to as a Cascaded H-bridge (CHB) Converter. In SST development projects, the MMC-based SST is the main choice [26] considering projects by Siemens [32], Bombardier [33], Alstom [34], GE Global Research [35], ABB [36, 37] and the FREEDM System Center [38–40]. Specifically for an MVAC to LVDC conversion, a solid state transformer (SST) performs better than a conventional low-frequency transformer (LFT) in terms of volume, weight and efficiency while maintaining a similar cost [25]. Figure 1.10 [8] presents this comparison.

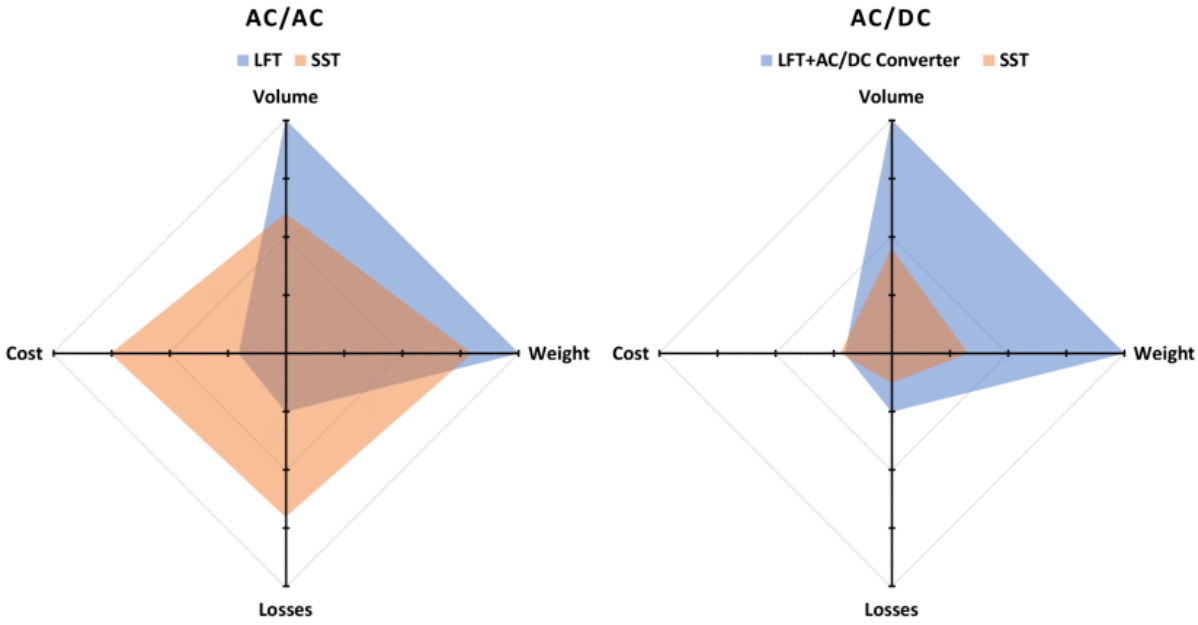
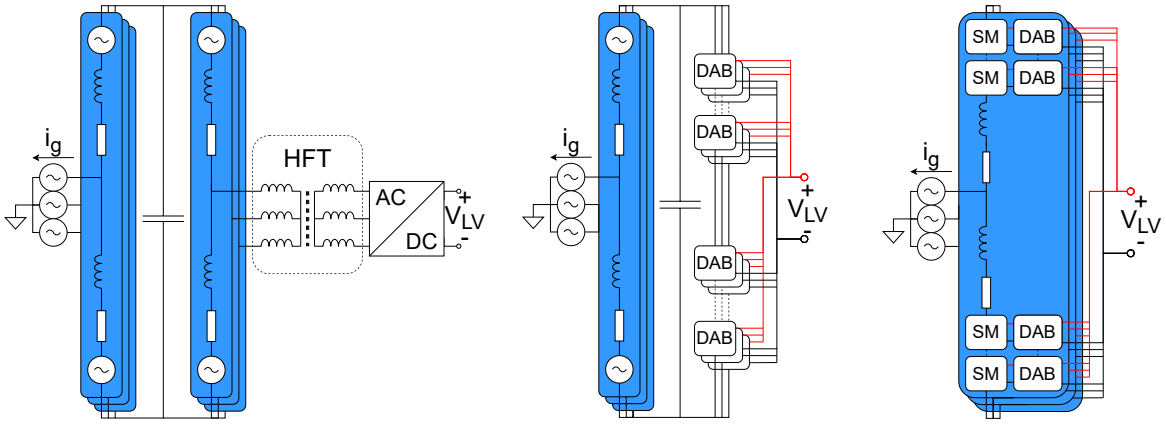



**Figure 1.10:** Comparison of an SST to an LFT in AC/AC and AC/DC applications [8, 25]

Figure 1.11 shows three MMC-based alternatives which will be briefly discussed based on literature to confirm the choice of the use of the configuration as shown in figure 1.11c. Figure 1.11a shows an SST where an MVDC link is created using an MMC. A second MMC is used to drive a high-frequency transformer (HFT), which with an active rectifier generates DC. The use of an MMC to drive a single HFT is suggested in [27, 28, 32]. However, the use of series to parallel isolated converters, such as the Dual Active Bridge (DAB), might be a better alternative. Series to parallel DAB configurations are suggested in [21, 29–31]. Figure 1.11b shows the implementation of a series to parallel DAB connection to generate the LVDC from the MVDC. [31] compares this topology to one where each DAB is connected straight to a submodule. The use of a DAB connected straight to each submodule is presented in [20, 22, 23, 25, 26, 31]. The direct coupling of the DAB removes the MVDC-link and therefore the MVDC-link capacitance, saving costs. Furthermore, this allows for potential control of the MMC submodule voltages through the DAB, and it is the only topology which allows for Single-Star and Single-Delta topologies. This makes the direct coupling of the DAB to each submodule the clear choice of design.




**(a)** Back-to-back MMCs with single HFT

**(b)** MMC providing MVDC for series-parallel DAB connection

**(c)** DABs connected directly to each SM

**Figure 1.11:** Different MVAC-LVDC MMC-based SST Configurations

When considering the options for a direct submodule coupled DAB, [22] uses DAB connections between the submodules of the different phases for submodule voltage balancing. [23] uses the DAB similarly as the here intended objective: To create an LVDC bus for ultra-fast charging applications. In [23] one DC bus is generated per phase and the MMC circulating current is controlled to generate power flow between the various LVDC busses. Due to the circulating current control, this connection is only a viable solution for a Double-Star connection.

Alternatively, a single LVDC bus can be generated as suggested in [8], where the AC power components of the three phases will cancel each other out, resulting in constant power on the DC bus. Figure 1.11c shows this SST configuration with a directly coupled DAB per SM with a parallel connection on the secondary side to generate the desired LVDC bus. Due to the removal of the MVDC-Link capacitance, the potential submodule voltage control and the option to use Single-Star or Delta topologies, this will be the most efficient solution in terms of hardware usage compared to the alternatives of Figure 1.11a, Figure 1.11b and the proposed solution in [23].

With the use of a directly coupled DAB, even power distribution per submodule is desired for design simplicity purposes. Therefore the phase-shifted modulation as described in section 1.4 has to be used.

# 2

# Mathematical Modeling

## 2.1. MMC Model with insertion indices

In order to analyse and model the behaviour of the MMC, a mathematical model is desired. By approximating the voltage across the submodules as an AC voltage source and neglecting the grid inductance, an equivalent circuit for mathematical modelling can be obtained. Figure 2.1 shows the used circuit for a single phase.

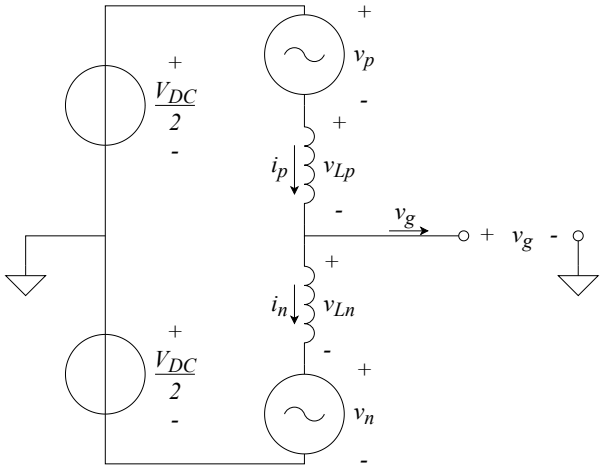



**Figure 2.1:** Single Phase MMC Model

Applying Kirchoff's voltage law to the upper arm results in equation 2.1.

$$v_p + v_{Lp} + v_g - \frac{V_{DC}}{2} = 0 \tag{2.1}$$

By taking the inductor series resistance into account, equations 2.2 and 2.3 can be obtained.

$$v_{Lp} = L\frac{di_p}{dt} + R_L i_p \tag{2.2}$$

$$v_p + L\frac{di_p}{dt} + R_L i_p + v_g = \frac{V_{DC}}{2} \tag{2.3}$$

Similarly, for the lower arm, equations 2.2 and 2.3 can be obtained.

$$v_{Ln} = L\frac{di_n}{dt} + R_L i_n \tag{2.4}$$

$$v_n + L\frac{di_n}{dt} + R_L i_n - v_g = \frac{V_{DC}}{2} \tag{2.5}$$

The grid current $i_g$ is then given by equation 2.6.

$$i_g = i_p - i_n \tag{2.6}$$

The circulating current $i_c$ is defined in [17] according to equation 2.7.

$$i_c = \frac{i_p + i_n}{2} \tag{2.7}$$

[17] describes the following: Define the internal voltage $v_c$ and the output voltage $v_o$ according to equations 2.8 and 2.9.

$$v_c = \frac{v_p + v_n}{2} \tag{2.8}$$

$$v_o = \frac{-v_n + v_n}{2} \tag{2.9}$$

Figure 2.2 shows the equivalent circuit using these definitions.

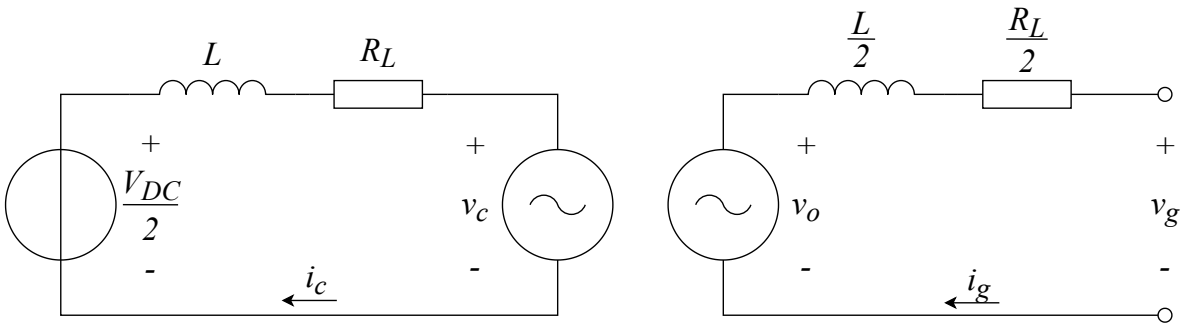



**Figure 2.2:** Equivalent MMC model based on internal voltage $v_c$ and output voltage $v_o$

Applying kirchoffs voltage law to figure 2.2 results in equations 2.10 and 2.11

$$L\frac{di_c}{dt} + R_L i_c = \frac{V_{DC}}{2} - v_c \tag{2.10}$$

$$\frac{L}{2}\frac{di_g}{dt} + \frac{R_L}{2} = v_o - v_g \tag{2.11}$$

According to [17], the voltages $v_c$ and $v_o$ can be described using the insertion indices $n_p$ and $n_n$ defined by equation 2.12.

$$n_{p,n} = \frac{1}{N}\sum_{i=1}^{N} n_{p,n}^{i} \tag{2.12}$$

This results in the following:

$$v_p = n_p V_{cp}^{\Sigma} \tag{2.13}$$

$$v_n = n_n V_{cn}^{\Sigma} \tag{2.14}$$

$$v_c = \frac{v_p + v_n}{2} = \frac{n_p V_{cp}^{\Sigma} + n_n V_{cn}^{\Sigma}}{2} \tag{2.15}$$

$$v_o = \frac{-v_p + v_n}{2} = \frac{-n_p V_{cp}^{\Sigma} + n_n V_{cn}^{\Sigma}}{2} \tag{2.16}$$

$$n_p = \frac{v_c - v_o}{V_{cp}^{\Sigma}} \tag{2.17}$$

$$n_n = \frac{v_c + v_o}{V_{cn}^{\Sigma}} \tag{2.18}$$

Here the switching indices can be controlled using the reference voltages for $v_c$ and $v_o$. This is the most commonly referred to model in literature. The downside of this model is that it assumes a constant $V_{DC}$ and neglects variations of the submodule capacitor voltage $v_{SM}$. Therefore this model is not suitable if no constant DC link voltage is present, or it is required to model the submodule capacitor voltages.

## 2.2. MMC Model using the switching function

The MVAC to MVDC conversion using an MMC is the first step of creating an MVAC to LVDC SST. As the SST will be based on a DAB to submodule connection, a mathematical model is required which takes the submodule voltage into account. Figure 2.3 shows a grid-connected MMC setup with active and reactive power control using the Park-Clarke transform. Here, a current controller controls the active and reactive currents, $i_d$ and $i_q$ respectively. This creates the inputs $X_d$ and $X_q$ for the inverse Park-Clarke transform. Dividing the output of the inverse Park-Clarke transform by the measured DC voltage provides the reference signal for the modulator.

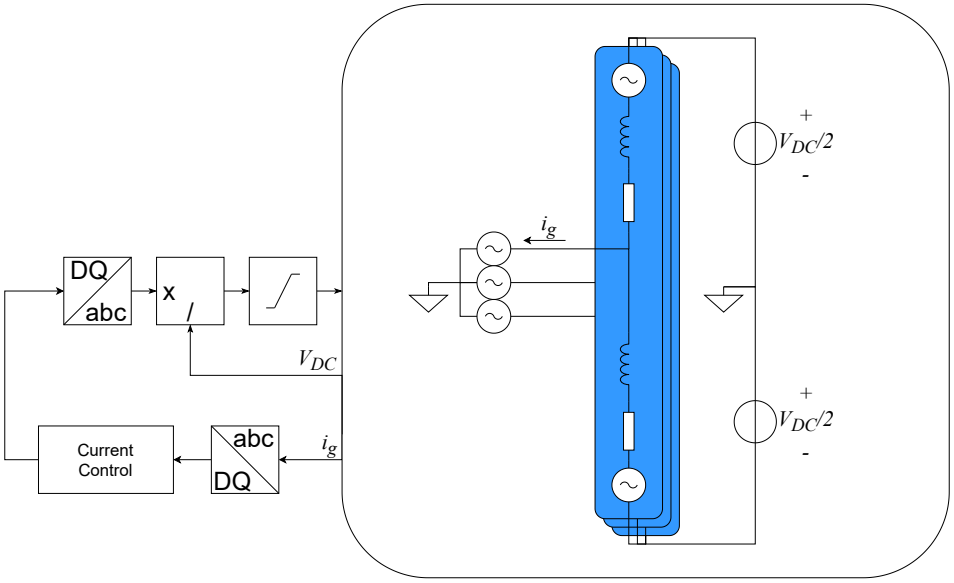



**Figure 2.3:** MMC and control for feeding a DC load from the AC grid

[41] Defines the switching functions for the upper and lower arm $S'_p$ and $S'_n$ respectively, using the modulation index m, as equations 2.19 and 2.20.

$$S'_p(t) = \frac{1 - m \cdot \sin(\omega t)}{2} \tag{2.19}$$

$$S'_n(t) = \frac{1 + m \cdot \sin(\omega t)}{2} \tag{2.20}$$

These switching functions have a relation to the voltages $v_p$ and $v_n$, and assuming even power distribution between the submodules, the submodule currents $I_{SMp}$ and $I_{SMn}$. In the scenario of figure 2.3, the switching functions are determined by the control. Defining the inverse Park-Clarke transform $P^{-1}$ according to [42] results in equation 2.21.

$$\begin{pmatrix} y_a \\ y_b \\ y_c \end{pmatrix} = P^{-1} \begin{pmatrix} x_d \\ x_q \end{pmatrix} = \begin{bmatrix} \cos(\phi) & -\sin(\phi) \\ \cos(\phi - 120°) & -\sin(\phi - 120°) \\ \cos(\phi + 120°) & -\sin(\phi + 120°) \end{bmatrix} \begin{pmatrix} x_d \\ x_q \end{pmatrix} \tag{2.21}$$

Equation 2.22 defines the grid voltages $v_{g,a}$, $v_{g,b}$ and $v_{g,c}$ and the grid peak voltage $\hat{v_g}$. Assuming the angle $\phi$ to be perfectly in phase with the grid results in equation 2.23.

$$v_g = \begin{pmatrix} v_{g,a} \\ v_{g,b} \\ v_{g,c} \end{pmatrix} = \hat{v_g} \begin{pmatrix} \sin(\omega t) \\ \sin(\omega t - \frac{2\pi}{3}) \\ \sin(\omega t + \frac{2\pi}{3}) \end{pmatrix} \tag{2.22}$$

$$P^{-1} = \begin{bmatrix} \sin(\omega t) & -\cos(\omega t) \\ \sin(\omega t - \frac{2\pi}{3}) & -\cos(\omega t - \frac{2\pi}{3}) \\ \sin(\omega t + \frac{2\pi}{3}) & -\cos(\omega t + \frac{2\pi}{3}) \end{bmatrix} \tag{2.23}$$

Now replace the in and outputs of the inverse Park-Clarke transform with the respective desired reference voltages: $V_d^* = x_d$, $V_q^* = x_q$, $v_a^* = y_a$, $v_b^* = y_b$ and $v_c^* = y_c$. Neglecting the saturation gives the switching function $S(t)$ according to equation 2.26. Which consists of $S_p(t)$ and $S_n(t)$, the switching function for the upper and lower arm respectively, given in equations 2.24 and 2.25.

$$S_p(t) = \frac{1}{2} - \frac{1}{V_{DC}} \begin{pmatrix} v_a^* \\ v_b^* \\ v_c^* \end{pmatrix} = \frac{1}{2} - \frac{1}{V_{DC}} P^{-1} \begin{pmatrix} V_d^* \\ V_q^* \end{pmatrix} \tag{2.24}$$

$$S_n(t) = \frac{1}{2} + \frac{1}{V_{DC}} \begin{pmatrix} v_a^* \\ v_b^* \\ v_c^* \end{pmatrix} = \frac{1}{2} + \frac{1}{V_{DC}} P^{-1} \begin{pmatrix} V_d^* \\ V_q^* \end{pmatrix} \tag{2.25}$$

$$S_{MMC}(t) = \frac{1}{2} + \frac{1}{V_{DC}} \begin{bmatrix} -P^{-1} \\ P^{-1} \end{bmatrix} \begin{pmatrix} V_d^* \\ V_q^* \end{pmatrix} = \frac{1}{2} + \frac{1}{V_{DC}} \begin{bmatrix} -\sin(\omega t) & \cos(\omega t) \\ -\sin(\omega t - \frac{2\pi}{3}) & \cos(\omega t - \frac{2\pi}{3}) \\ -\sin(\omega t + \frac{2\pi}{3}) & \cos(\omega t + \frac{2\pi}{3}) \\ \sin(\omega t) & -\cos(\omega t) \\ \sin(\omega t - \frac{2\pi}{3}) & -\cos(\omega t - \frac{2\pi}{3}) \\ \sin(\omega t + \frac{2\pi}{3}) & -\cos(\omega t + \frac{2\pi}{3}) \end{bmatrix} \begin{pmatrix} V_d^* \\ V_q^* \end{pmatrix} \tag{2.26}$$

$v_p$ and $v_n$ can be calculated according to equations 2.27 and 2.28 respectively. Since a phase-shifted modulation is used with the assumption of equal power per submodule, the sum of the submodules per arm can be replaced by one submodule voltage of the arm times the number of submodules in the arm.

$$v_p(t) = S_{p(a,b,c)}(t) \cdot \sum V_{SMp(a,b,c)}(t) = S_p(t) \cdot N \cdot V_{SMp}(t) \tag{2.27}$$

$$v_n(t) = S_{n(a,b,c)}(t) \cdot \sum V_{SMn(a,b,c)}(t) = S_n(t) \cdot N \cdot V_{SMn}(t) \tag{2.28}$$

Using equations 2.8 and 2.9 for $v_o$ and $v_c$ leads to equations 2.29 and 2.30 respectively.

$$v_o(t) = \frac{-v_p(t) + v_n(t)}{2} = \frac{-S_p(t) \cdot N \cdot V_{SMp}(t) + S_n(t) \cdot N \cdot V_{SMn}(t)}{2} \tag{2.29}$$

$$v_c(t) = \frac{v_p(t) + v_n(t)}{2} = \frac{S_p(t) \cdot N \cdot V_{SMp}(t) + S_n(t) \cdot N \cdot V_{SMn}(t)}{2} \tag{2.30}$$

The grid currents $i_g$ and circulating currents $i_c$ can now be calculated according to equations 2.31 and 2.32 respectively.

$$i_g(s) = \frac{v_o - v_g}{(L/2)s + (R_L/2)} \rightarrow \frac{i_g(s)}{v_o - v_g} = \frac{2}{Ls + R_L} \tag{2.31}$$

$$i_c(s) = \frac{(V_{DC}/2) - v_c}{Ls + R_L} \rightarrow \frac{i_c(s)}{(V_{DC}/2) - v_c} = \frac{1}{Ls + R_L} \tag{2.32}$$

Solving the system of equations with equations 2.6 and 2.7, for $i_p$ and $i_n$, gives equations 2.33 and 2.34 respectively.

$$i_p = \frac{i_g}{2} + i_c \tag{2.33}$$

$$i_n = i_c - \frac{i_g}{2} \tag{2.34}$$

[41] gives the relations between the switching function and the submodule current $I_{SM}$ as stated in equations 2.35 and 2.36.

$$I_{SMp}(t) = S_p(t) \cdot i_p(t) \tag{2.35}$$
$$I_{SMn}(t) = S_n(t) \cdot i_n(t) \tag{2.36}$$

The relationship between the submodule current $I_{SM}$ and submodule voltage $V_{SM}$ can be modelled using the submodule capacitance $C_{SM}$ in the Laplace domain according to equation 2.37.

$$\frac{V_{SM}(s)}{I_{SM}(s)} = \frac{R_{C_{SM}} C_{SM} s + 1}{C_{SM} s} \tag{2.37}$$

From $i_p$ and $i_n$, the submodule currents can be calculated according to equations 2.35 and 2.36 respectively. In turn, the submodule voltages can be calculated using equation 3.9. These can then be plugged back into equations 2.27 and 2.28, resulting in a complete model.

## 2.3. MMC Math Models and Accuracy

To check the viability of the presented mathematical models, the equations are implemented in block schematics in PLECS, to be compared to a PSC-based switched simulation of the MMC. Both the mathematical MMC model and the switched MMC model are controlled with the same reference waveform. The models are compared on the submodule voltages and the AC (grid) Currents.

### 2.3.1. MMC Feeding AC Load

The model is compared using an MMC feeding an AC Load. Table 2.1 shows the simulation parameters. The described mathematical model uses a grid voltage $v_g$, which is now replaced by the voltage over the load, using $v_g = i_g \cdot R_g$. Figure 2.5 shows the implementation of the mathematical model in PLECS.

| Symbol | Parameter | Value |
|---|---|---|
| S | Total Appereant Power | 1 [MVA] |
| $V_{DC}$ | DC Link Voltage | 5.4 [kV] |
| $\hat{v_g}$ | AC Peak Voltage | 2.7 [kV] |
| N | Submodules per Arm | 4 |
| $V_{SM}$ | Submodule Voltage | 1.35 [kV] |
| $C_{SM}$ | Submodule Capacitance | 2 [mF] |
| $R_{C,SM}$ | $C_{SM}$ ESR | 1 [mΩ] |
| $L_{arm}$ | Arm Inductance | 10 [mH] |
| $R_L$ | $L_{arm}$ ESR | 1 [mΩ] |
| $R_g$ | AC Load Resistance | 10.935 [Ω] |

**Table 2.1:** Simulation Parameters of the MMC feeding a AC Load

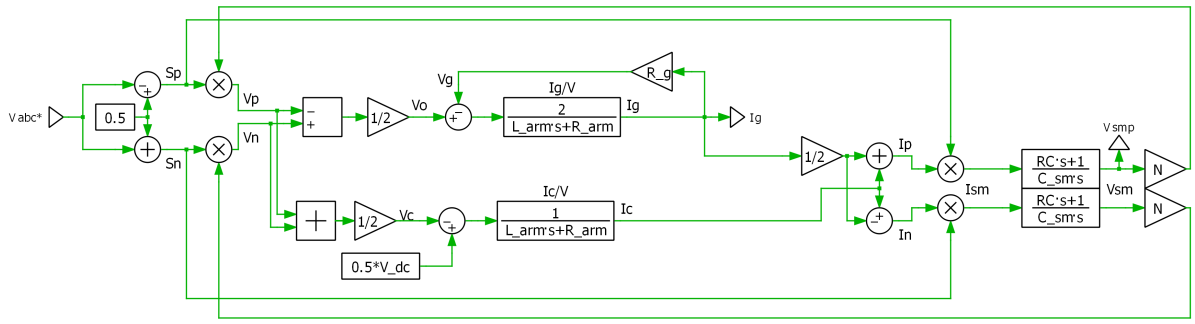



**Figure 2.4:** Mathematical Model of a MMC Feeding an AC Load implemented in PLECS

Figure 2.5 shows the simulation results. The output of the switched simulation and the mathematical model are plotted in the same scope. The plots overlap precisely. This shows that the mathematical equations used are a valid approximation of the MMC in this setting.

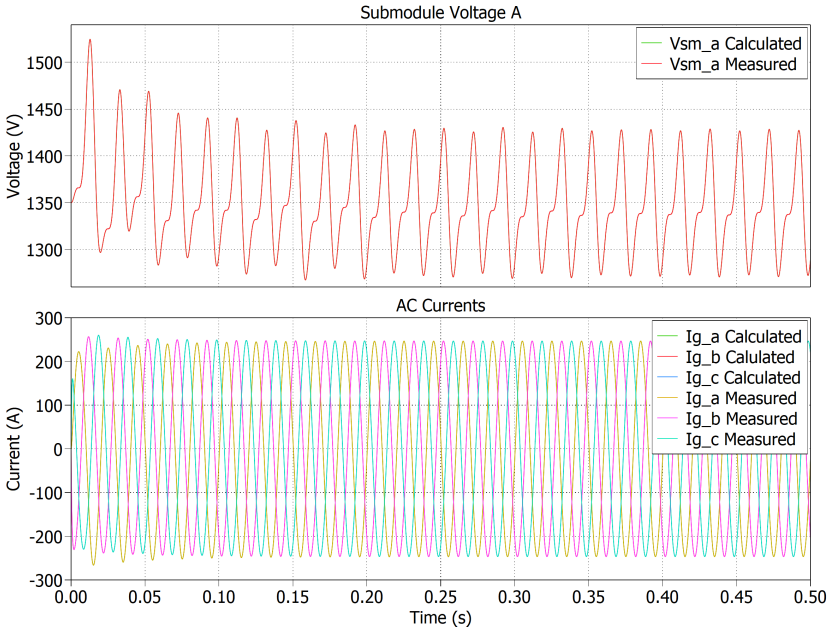



**Figure 2.5:** Comparison of the Mathematical Model and a Switched MMC Simulation feeding an AC Load

### 2.3.2. Grid Connected Current Control

Now consider the setting of figure 2.3. The MMC is now grid-connected and current control is applied. Table 2.2 shows the simulation parameters. Figure 2.6 shows the implementation of the mathematical model in PLECS.

| Symbol | Parameter | Value |
|---|---|---|
| S | Total Appereant Power | 1 [MVA] |
| $V_{DC}$ | DC Link Voltage | 5.4 [kV] |
| $\hat{v_g}$ | AC Peak Voltage | 2.7 [kV] |
| N | Submodules per Arm | 4 |
| $V_{SM}$ | Submodule Voltage | 1.35 [kV] |
| $C_{SM}$ | Submodule Capacitance | 2 [mF] |
| $R_C$ | $C_{SM}$ ESR | 1 [mΩ] |
| $L_{arm}$ | Arm Inductance | 10 [mH] |
| $R_L$ | $L_{arm}$ ESR | 1 [mΩ] |
| $L_g$ | AC Grid Inductance | 0 [H] |
| $R_g$ | AC Grid Resistance | 0 [Ω] |
| $f_g$ | Grid Frequency | 50 [Hz] |
| $f_s$ | MMC Switching Frequency | 10 [kHz] |
| $I_d^*$ | Reference grid current | $-2S/3/\hat{v_g}$ [A] |
| $K_{p,I}$ | Current Control Proportional Gain | 1 |
| $K_{i,I}$ | Current Control Integral Gain | 50 |

**Table 2.2:** Simulation Parameters of the Current Controlled Grid Connected MMC

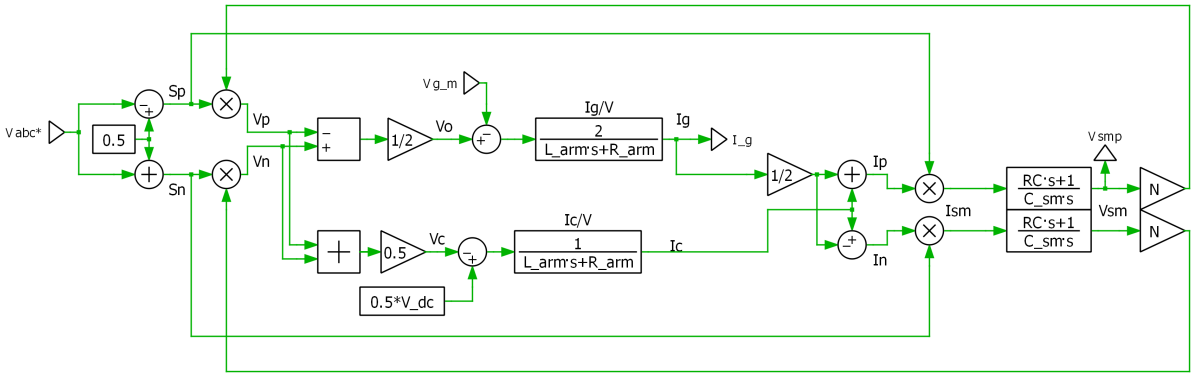



**Figure 2.6:** Mathematical Model of a Current Controlled Grid Connected MMC implemented in PLECS

Figure 2.7 shows the simulation results with the output of the mathematical model and the switched model in the same scope. The plots are almost exactly identical, minor deviations are visible. As the submodule voltage ripple is identical and the shape is similar, it can be concluded that this is an accurate model.

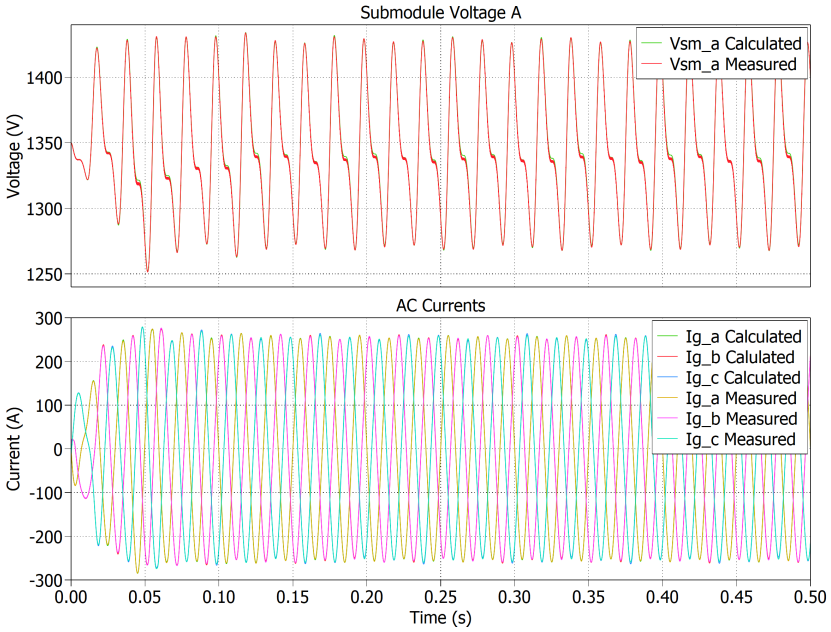



**Figure 2.7:** Comparison of the Mathematical Model and a Grid Connected Current Controlled Switched MMC Simulation

### 2.3.3. Grid Connected Submodule Voltage Control

Consider a scenario where there is no DC source connected to the MMC and the MVDC link is removed. To mimic the behaviour of the SST where there is a DAB connected to each submodule, a load in the form of an ideal DC current source is connected to each submodule. Figure 2.8 shows this MMC configuration.

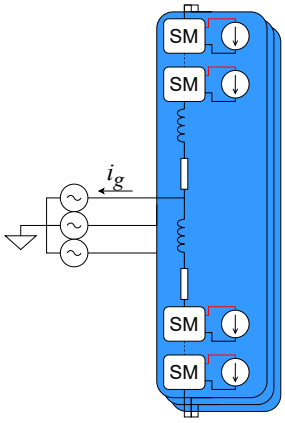



**Figure 2.8:** MMC without MVDC-Link and a Load Connected to each Submodule

With no MVDC-Link, there is still a DC voltage across the MMC which is required to determine the circulating current (Equation 2.32). However, without a DC source, this circulating current will have no DC component (Equation 2.38), which in turn leads to equation 2.39. Using Kirchoff's voltage law, it can be stated that the DC voltage across the MMC is equal to the sum of all the voltages in the upper and lower arm for each phase. Equation 2.40 shows this. Combining equations 2.40 and 2.39 leads to equation 2.41.

$$i_{c,DC} = 0 \tag{2.38}$$

$$\sum v_{L,(a,b,c)} = 0 \tag{2.39}$$

$$\begin{aligned} V_{DC} &= v_{p,a} + v_{n,a} + v_{Lp,a} + v_{Lp,a} \\ &= v_{p,b} + v_{n,b} + v_{Lp,b} + v_{Lp,b} \\ &= v_{p,c} + v_{n,c} + v_{Lp,c} + v_{Lp,c} \end{aligned} \tag{2.40}$$

$$V_{DC} = \frac{1}{3} \sum \left( v_{p,(a,b,c)} + v_{n,(a,b,c)} \right) \tag{2.41}$$

In this MMC with a submodule load, the submodule voltage is now controlled using a PI control, which includes saturation and anti-windup to limit the grid current. Table 2.3 shows the parameters of the simulation. Figure 2.9 shows the implementation of the mathematical model in PLECS.

| Symbol | Parameter | Value |
|---|---|---|
| S | Total Appereant Power | 1 [MVA] |
| $V_{DC}$ | DC Link Voltage | 5.4 [kV] |
| $\hat{v_g}$ | AC Peak Voltage | 2.7 [kV] |
| N | Submodules per Arm | 4 |
| $V_{SM}$ | Submodule Voltage | 1.35 [kV] |
| $C_{SM}$ | Submodule Capacitance | 2 [mF] |
| $R_{C,SM}$ | $C_{SM}$ ESR | 1 [mΩ] |
| $L_{arm}$ | Arm Inductance | 10 [mH] |
| $R_L$ | $L_{arm}$ ESR | 1 [mΩ] |
| $L_g$ | AC Grid Inductance | 0 [H] |
| $R_g$ | AC Grid Resistance | 0 [Ω] |
| $I_{SM,Load}$ | Submodule load current | $P/N/6/V_{SM}$ [A] |
| $K_{p,I}$ | Current Control Proportional Gain | 1 |
| $K_{i,I}$ | Current Control Integral Gain | 50 |
| $K_{p,V}$ | Voltage Control Proportional Gain | 1 |
| $K_{i,V}$ | Voltage Control Integral Gain | 1 |
| $K_w$ | Voltage Control Anti-Windup Gain | 10 |
| $i_{sat}$ | Reference Current Saturation | 250A |

**Table 2.3:** Simulation Parameters of the Voltage Controlled Grid Connected MMC

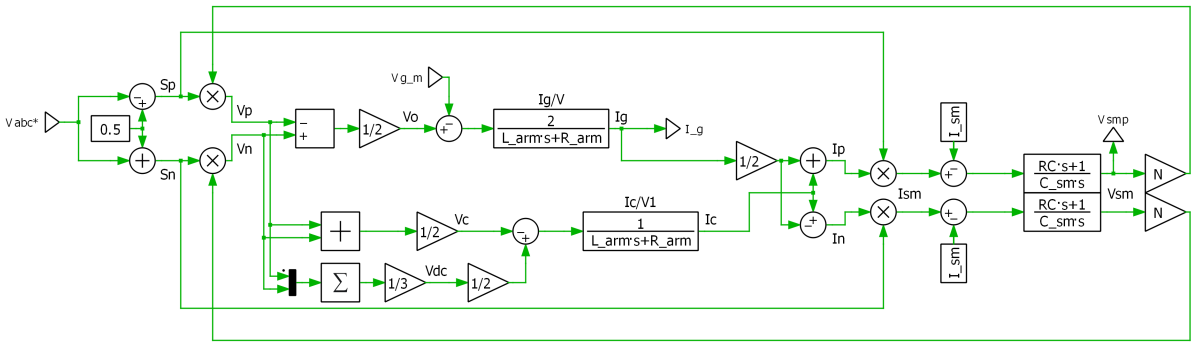



**Figure 2.9:** Mathematical Model of a Voltage Controlled Grid Connected MMC implemented in PLECS

Figure 2.10 shows the results of the simulation. The input reference signal of the MMC is fed into the mathematical model and the submodule voltages of leg A and the grid currents are plotted in the same scope. There are some deviations visible, mainly on the peaks of the submodule voltages and the grid currents. However, the voltages and currents remain stable in both models even though the same input is used. From this, it can be concluded that the model is still accurate when analysing stability.

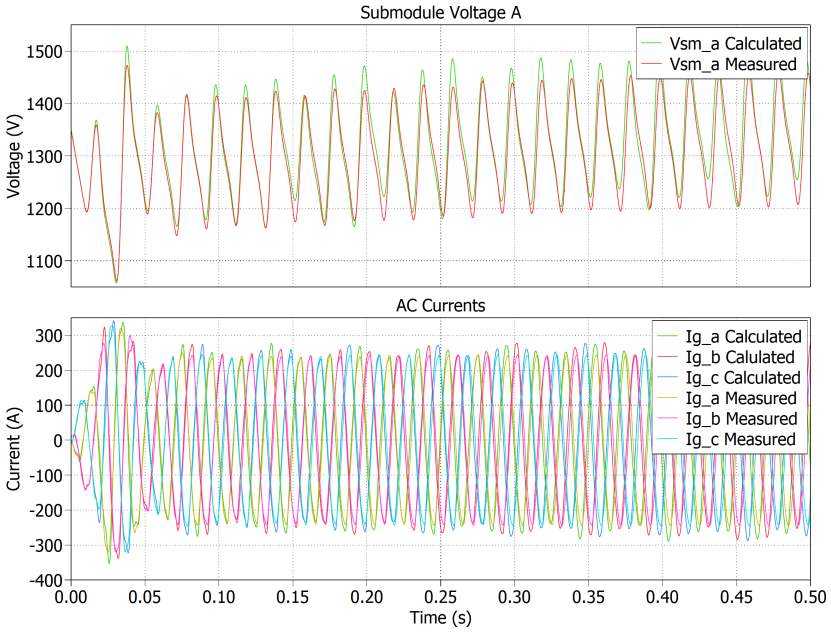



**Figure 2.10:** Comparison of the Mathematical Model and a Grid Connected Voltage Controlled Switched MMC Simulation
Both models use the same input

Alternatively, the mathematical model can be run independently using its own control system. Figure 2.11 shows the result of this. There are similar deviations visible compared to figure 2.10, these deviations become less over time as the control system now acts independently and can remove these deviations. From this, it can be included that the mathematical model can be run as an independent simulation. Such a simulation runs significantly faster than a switched simulation and can be helpful in the tuning of control system parameters.

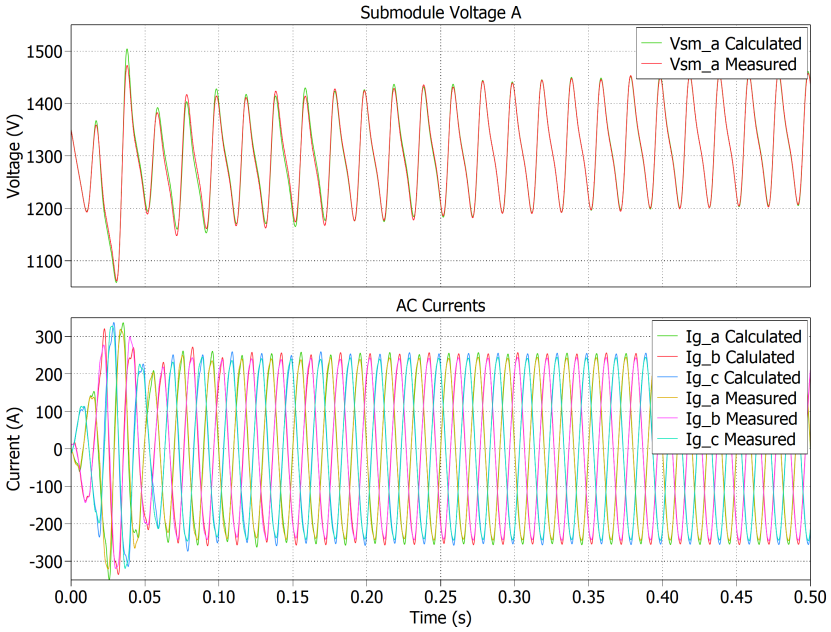



**Figure 2.11:** Comparison of the Mathematical Model and a Grid Connected Voltage Controlled Switched MMC Simulation
Both models use an independent control system

## 2.4. Dual Active Bridge Model

For a mathematical model of the SST, a model of the Dual Active Bridge is required first, which can then be combined with the model of the MMC to achieve an SST model. A Dual Active Bridge (DAB) with a single phase shift control is considered. Figure 2.12 shows this DAB.

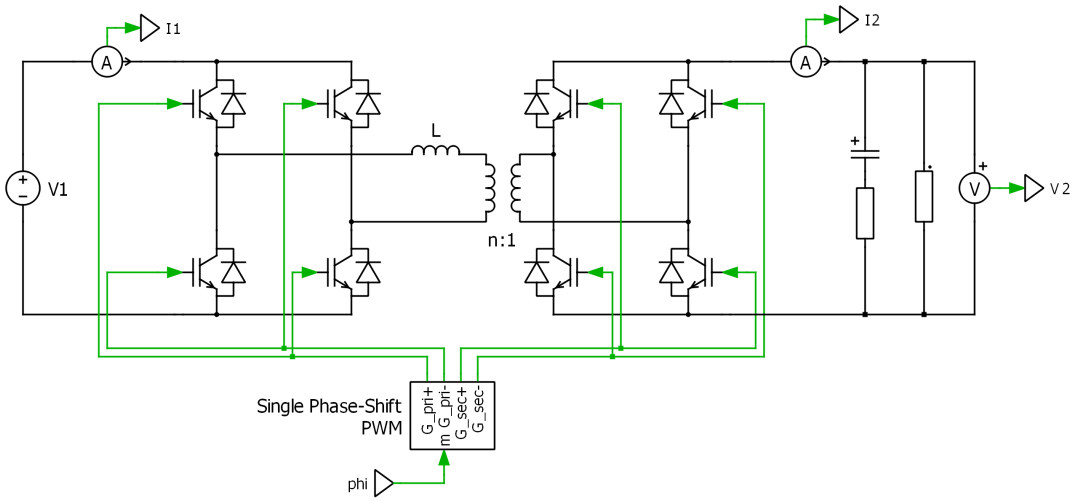



**Figure 2.12:** Dual Active Bridge (DAB) with Phase Shift Control

Various mathematical models are presented in [43–46]. However, a very simple model of the DAB might suffice as the modelling of the behaviour at the desired frequencies ($f_g$ and its SM harmonics) are far lower than the switching frequency of the DAB ($f_g << f_{s,DAB}$). The switching behaviour and speed of the DAB can therefore be neglected.

Various DAB modulation techniques are presented in [47, 48], which also presents the power for phase-shifted modulation. Equation 2.42 shows this relation, using the phase shift $\phi$. The provided equation is for the total unidirectional power, this equation is therefore only valid for positive values of $\phi$. From this the in and output currents can be calculated, equations 2.43 and 2.44 respectively, valid for both positive and negative numbers of $\phi$. The DAB peak power is calculated using equations 2.45 and 2.46.

$$|P_{DAB}| = \frac{V_1 V_2 n}{f_s L}(\phi - 2\phi^2) \tag{2.42}$$

$$I_{DAB,1} = \frac{P_{DAB}}{V_1} = \frac{V_2 n}{f_s L}(|\phi| - 2|\phi|^2) \cdot sign(\phi) \tag{2.43}$$

$$I_{DAB,2} = \frac{P_{DAB}}{V_2} = \frac{V_2 n}{f_s L}(|\phi| - 2|\phi|^2) \cdot sign(\phi) \tag{2.44}$$

$$P_{DAB,max} @ \frac{dP_{DAB}}{d\phi} = 0 \rightarrow \phi = 0.25 \tag{2.45}$$

$$P_{DAB,max} = 0.125 \frac{V_1 V_2 n}{f_s L} \tag{2.46}$$

In the SST, there will be a parallel output connection of multiple DABs. As equal power per submodule has been assumed during the MMC model, only one submodule per leg needs to be modelled. Therefore the total low voltage current becomes the sum of the DAB model from each leg times the amount of submodules per leg. Equation 2.47 shows this relation. Now state that $V_1 = V_{SM}$ and $V_2 = V_{LV}$ Equation 2.48 gives the relation between the low voltage DC current and the voltage, assuming an RC-load on the LVDC-Bus.

$$I_{LV} = N \cdot \sum_{(a,b,c)_{p,n}} I_{DAB,2} \tag{2.47}$$

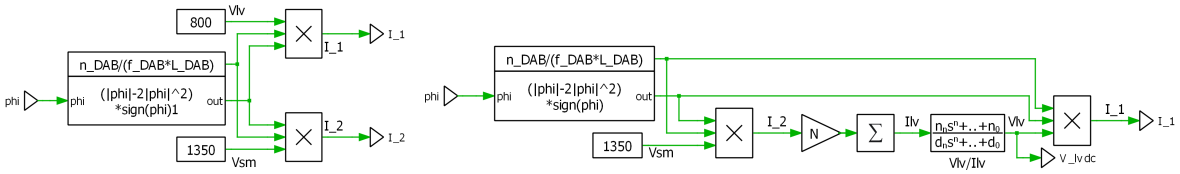
$$\frac{V_{LV}(s)}{I_{LV}(s)} = \frac{R_{LV} R_{C_{LV}} C_{LV} s + R_{LV}}{(R_{LV} + R_{C_{LV}}) C_{LV} s + 1} \tag{2.48}$$

### 2.4.1. DAB Model Accuracy

To test the accuracy of the DAB model, the mathematics are implemented in PLECS and compared to a switched model. Table 2.4 shows the used parameters for the simulation. First, a DAB between two constant ideal DC voltage sources is considered. Figure 2.13a shows the implemented mathematical model, compared to the switched model on the in and output current of the DAB. Second, a DAB feeding an RC load from a constant ideal DC voltage source is considered. Figure 2.13b shows the implemented mathematical model of this. This includes the option to simulate multiple parallel DABs.

| Cymbol | Parameter | Value |
|---|---|---|
| $V_1$ | Input Voltage | 1350V |
| $V_2$ | Output Voltage | 800V |
| $n$ | Transformer Turn Ration | 1350/800 |
| $L$ | DAB Inductance | 220mH |
| $f$ | DAB Switching Frequency | 20kHz |
| $R$ | DC Load Resistance | 12.361Ω |
| $C$ | DC Load Capacitance | 220µF |
| $R_C$ | Capacitor ESR | 10mΩ |

**Table 2.4:** Simulation Parameters of the DAB

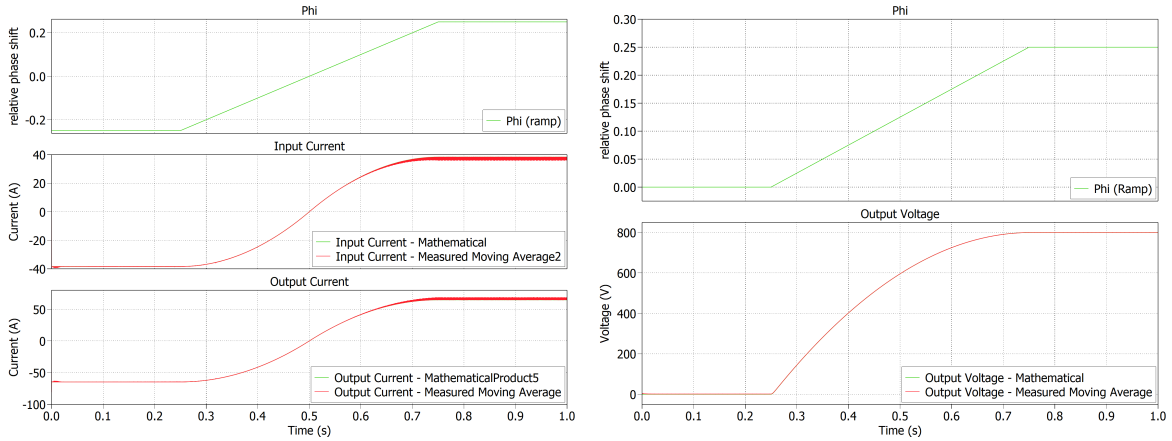



**(a)** DAB Current Comparison with 2 DC Sources

**(b)** DAB Voltage Comparison with RC Load

**Figure 2.13:** Comparison of the Mathematical Model and a switched DAB Simulation

Figure 2.14 shows the simulation results of both simulations. In the current comparison (Figures 2.13a, 2.14a), phi is swept over its maximum effective range from -0.25 to +0.25. In the voltage comparison (Figures 2.13b, 2.14b), phi is swept from 0 to +0.25 for a positive current only. The averaged switched simulation results and the results from the mathematical model have been plotted in the same figure, this shows a clear overlap. It can be concluded that the DAB model is accurate when neglecting switching behaviour.




**(a)** DAB Current Comparison with 2 DC Sources

**(b)** DAB Voltage Comparison with RC Load

**Figure 2.14:** Comparison of the Mathematical Model and a switched DAB Simulation

## 2.5. Solid State Transformer Model

This section describes the combination of the found mathematical models, of the MMC and the DAB, into a single model for the various SST configurations.

### 2.5.1. Double-Star Half-Bridge Model

Figure 2.15 shows the implementation of the mathematical model of the Double-Star Half-Bride SST in PLECS. This model includes the control system described in section 3.2. The MMC model is taken and the DAB input current ($I_{DAB,1}$) is subtracted from the submodule current. Equation 2.49 represents the current flowing into the submodule capacitor.

$$I_{C_{SM}} = I_{SM} - I_{DAB,1} \tag{2.49}$$

The submodule capacitor current is used to calculate the submodule voltage, which is in turn fed into the DAB model. This results in a complete model where the MMC and the DAB part are codependent.

To check the accuracy of the mathematical model, it is implemented in PLECS (Figure 2.15) and compared to a switched simulation. To reduce the simulation time, the SST is simulated with four submodules for 1MVA. Table 2.5 presents the used parameters for this simulation.

| Symbol | Parameter | Value |
|---|---|---|
| S | Total Appereant Power | 1 [MVA] |
| $\hat{v_g}$ | AC Peak Voltage | 2.7 [kV] |
| N | Submodules per Arm | 4 |
| $V_{SM}$ | Submodule Voltage | 1.35 [kV] |
| $C_{SM}$ | Submodule Capacitance | 1.94 [mF] |
| $R_{C,SM}$ | $C_{SM}$ ESR | 1 [mΩ] |
| $L_{arm}$ | Arm Inductance | 10 [mH] |
| $R_L$ | $L_{arm}$ ESR | 1 [mΩ] |
| $L_g$ | AC Grid Inductance | 0 [H] |
| $R_g$ | AC Grid Resistance | 0 [Ω] |
| $f_g$ | Grid Frequency | 50 [Hz] |
| $f_s$ | MMC Switching Frequency | 10 [kHz] |
| $n$ | DAB Transformer Turn Ration | 1350/800 |
| $L_{DAB}$ | DAB Inductance | 228 [µH] |
| $f_{DAB}$ | DAB Switching Frequency | 20 [kHz] |
| $C_{DAB}$ | DAB Output Capacitance | 220 [µF] |
| $R_{C,DAB}$ | $C_{DAB}$ ESR | 10 [mΩ] |
| $R_{lvdc}$ | LVDC Resistive Load | 0.64 [Ω] |
| $K_{p,I}$ | Current Control Proportional Gain | 1 |
| $K_{i,I}$ | Current Control Integral Gain | 50 |
| $K_{p,V}$ | Voltage Control Proportional Gain | 1 |
| $K_{i,V}$ | Voltage Control Integral Gain | 1 |
| $K_w$ | Voltage Control Anti-Windup Gain | 10 |
| $I_{sat}$ | Reference Current Saturation | 271.6 [A] |
| $K_{p,DAB}$ | DAB Control Proportional Gain | $2 \cdot 10^{-5}$ |
| $K_{i,DAB}$ | DAB Control Integral Gain | 0.08 |

**Table 2.5:** Simulation Parameters of Double Star SST and its Mathematical Model

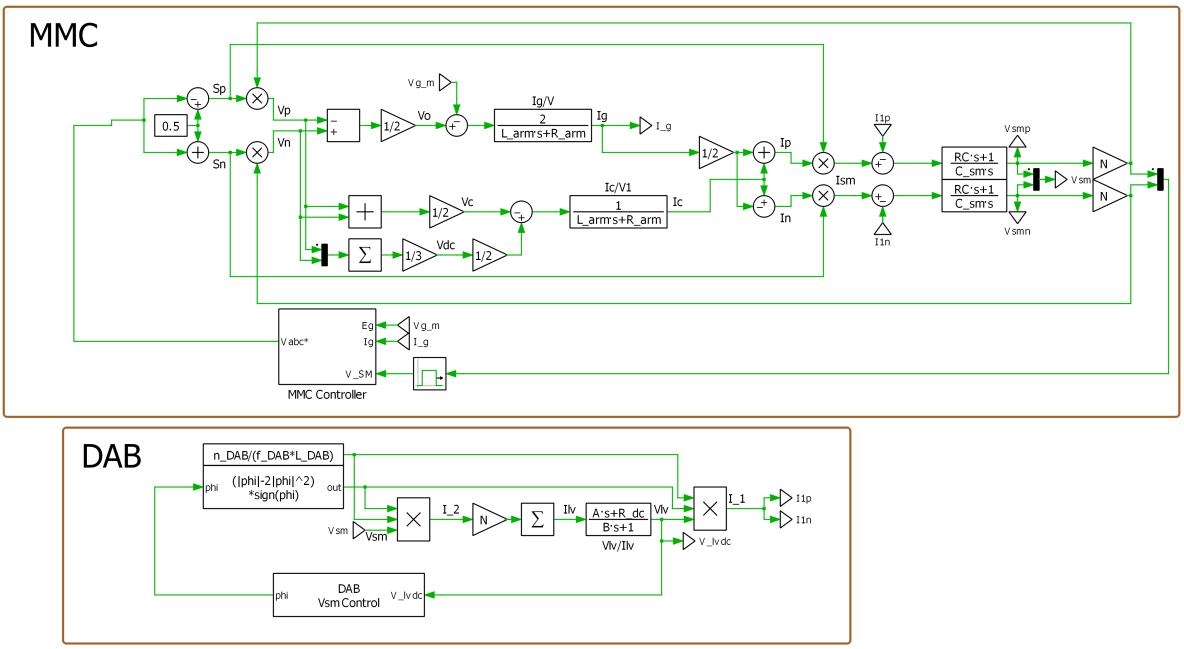



**Figure 2.15:** Mathematical Model of the Double-Star SST

Figure 2.16 presents the simulation results of the comparison. The model is compared on the basis of the generated reference current $I_d^*$, the currents $I_d$ and $I_q$, the submodule voltages of the upper leg in phase A ($V_{SM,a,p}$) and the low voltage DC bus ($V_{LV\,DC}$). The switched simulation and the mathematical model results are plotted in the same scope. Figure 2.16 shows an overlap between the two simulations, concluding that the mathematical modelling of the Double-Star SST is correct.

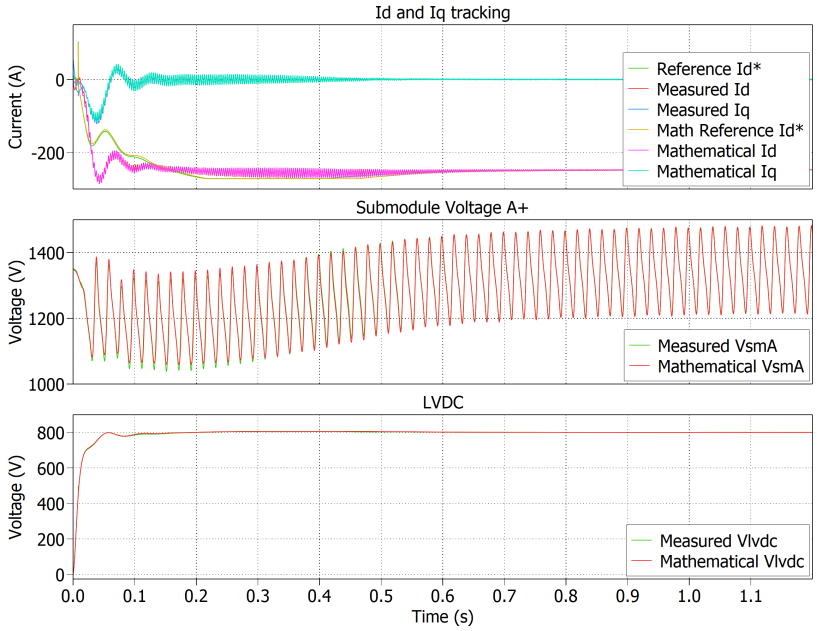



**Figure 2.16:** Comparison of the Mathematical Model and a Switched Double-Star SST Simulation

### 2.5.2. Single-Star Full-Bridge Model

To compare the Single-Star topology to the Double-Star topology, the voltage levels of the star points can be calculated using the inserted voltages $V_i$.

$$v_{star}(t) = v_g(t) + v_L(t) + v_i(t) \tag{2.50}$$
$$V_{star,av} = V_{g,av} + V_{L,av} + V_{i,av} \tag{2.51}$$
$$V_{g,av} = V_{neutral} = 0V \tag{2.52}$$

Because the AC components of the three 120° shifted phases will cancel each other out, only the averages can be considered. As a half-bridge can only insert positive voltages, the average becomes half the total voltage swing, resulting in equation 2.53. This, in turn, results in equation 2.55, matching with the described Double-Star MMC. As a full bridge submodule can insert both a positive and negative submodule voltage, the average becomes equation 2.54. With no DC currents $V_L$ will be zero average, resulting in equation 2.56.

$$V_{i,av,HB} = \frac{1}{2}V_{DC} \tag{2.53}$$
$$V_{i,av,FB} = 0V \tag{2.54}$$
$$V_{star,HB} = \pm\frac{1}{2}V_{DC} \tag{2.55}$$
$$V_{star,FB} = V_{neutral} = 0V \tag{2.56}$$

Figure 2.17 shows the equivalent circuit of the Single-Star MMC arms.

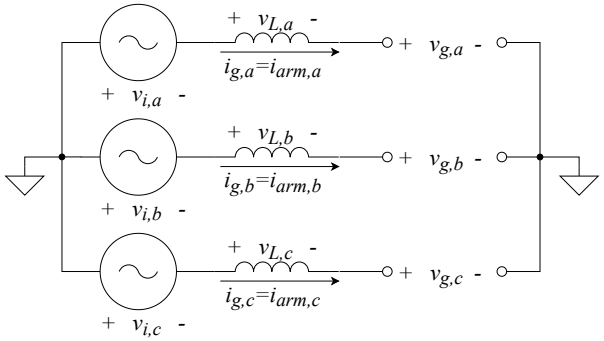



**Figure 2.17:** Single Star Equivalent Circuit

The equivalent circuit already that the grid current is equal to the arm current. Since there are no upper and lower arms, the circulating current, which is present with the Double-Star MMC, does not exist.

$$i_{arm} = i_g \tag{2.57}$$
$$i_c = 0 \tag{2.58}$$

As with a Full-Bridge SM, double the submodule voltage can be inserted. The switching function can now be redefined for the Single-Star MMC according to equation 2.59. This, in turn, results in equations 2.60 and 2.61.

$$S(t) = \frac{-2}{V_{DC}}P^{-1}\begin{pmatrix}V_d^*\\V_q^*\end{pmatrix} \tag{2.59}$$
$$v_{i(a,b,c)}(t) = S_{(a,b,c)}(t)\cdot\sum V_{SM(a,b,c)}(t) \rightarrow v_i(t) = -N\cdot S(t)\cdot V_{SM}(t) \tag{2.60}$$
$$v_L = -v_i - v_g \tag{2.61}$$

Figure 2.18 shows the implementation of this mathematical model in PLECS. It is simulated and compared to a switched model using the parameters of table 2.6.

| Symbol | Parameter | Value |
|---|---|---|
| S | Total Appereant Power | 1 [MVA] |
| $\hat{v_g}$ | AC Peak Voltage | 2.7 [kV] |
| N | Submodules per Arm | 2 |
| $V_{SM}$ | Submodule Voltage | 1.35 [kV] |
| $C_{SM}$ | Submodule Capacitance | 1.55 [mF] |
| $R_{C,SM}$ | $C_{SM}$ ESR | 1 [mΩ] |
| $L_{arm}$ | Arm Inductance | 10 [mH] |
| $R_L$ | $L_{arm}$ ESR | 1 [mΩ] |
| $L_g$ | AC Grid Inductance | 0 [H] |
| $R_g$ | AC Grid Resistance | 0 [Ω] |
| $f_g$ | Grid Frequency | 50 [Hz] |
| $f_s$ | MMC Switching Frequency | 10 [kHz] |
| $n$ | DAB Transformer Turn Ration | 1350/800 |
| $L_{DAB}$ | DAB Inductance | 57.0 [µH] |
| $f_{DAB}$ | DAB Switching Frequency | 20 [kHz] |
| $C_{DAB}$ | DAB Output Capacitance | 220 [µF] |
| $R_{C,DAB}$ | $C_{DAB}$ ESR | 10 [mΩ] |
| $R_{lvdc}$ | LVDC Resistive Load | 0.64 [Ω] |
| $K_{p,I}$ | Current Control Proportional Gain | 1 |
| $K_{i,I}$ | Current Control Integral Gain | 100 |
| $K_{p,V}$ | Voltage Control Proportional Gain | 2 |
| $K_{i,V}$ | Voltage Control Integral Gain | 4 |
| $K_w$ | Voltage Control Anti-Windup Gain | 10 |
| $I_{sat}$ | Reference Current Saturation | 271.6 [A] |
| $K_{p,DAB}$ | DAB Control Proportional Gain | $3 \cdot 10^{-5}$ |
| $K_{i,DAB}$ | DAB Control Integral Gain | 0.012 |

**Table 2.6:** Simulation Parameters of Double Star SST and its Mathematical Model

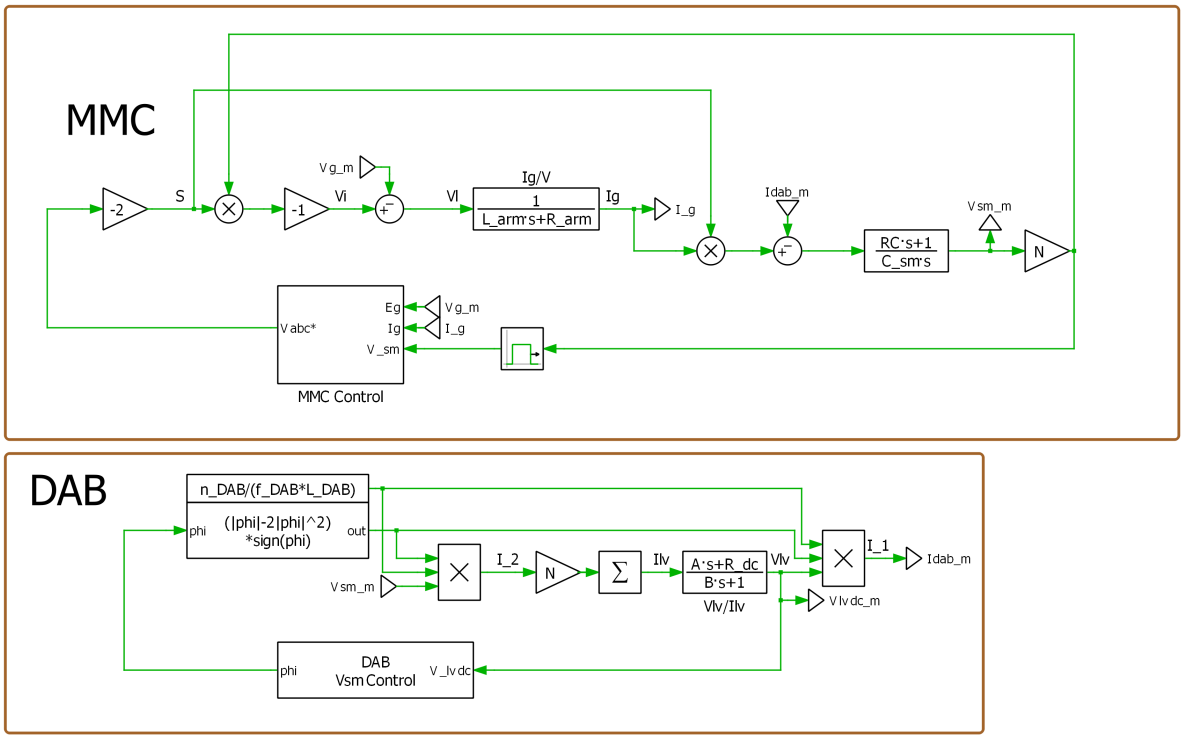



**Figure 2.18:** Mathematical Model of the Single-Star SST

Figure 2.19 shows the simulation results of the comparison, with the results of the mathematical model and the switched simulation plotted in the same scope. There is a deviation visible in the shape of the submodule currents due to the fact that the mathematical model is an approximation. Both the average behaviour of all signals and the total submodule voltage ripple remain the same. Therefore the model is accurate for reviewing the behaviour of the SST.

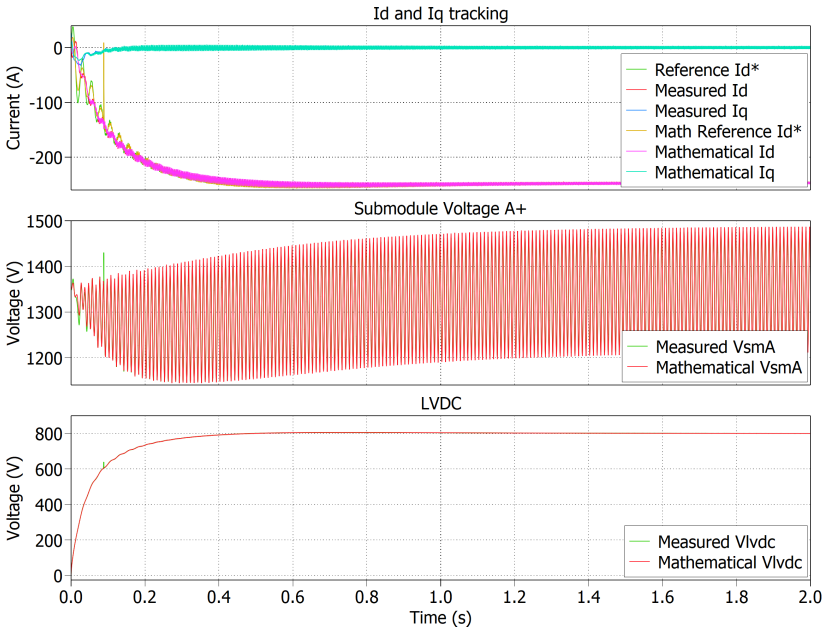



**Figure 2.19:** Comparison of the Mathematical Model and a Switched Single-Star SST Simulation.

### 2.5.3. Single-Delta Full-Bridge Model

For a delta-connected SST the voltage and currents in the MMC arms will be different from those in the grid, unlike the Single-Star SST. Figure 2.20 shows the Delta connection and its voltages and currents used in the model.

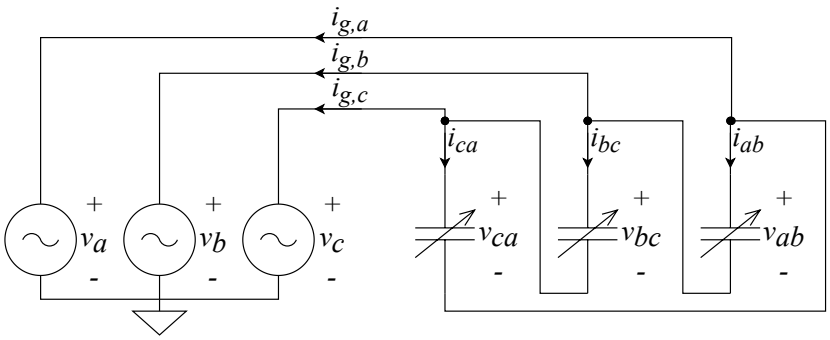



**Figure 2.20:** Delta Connection of the MMC

The voltages across the arms can now be represented as $v_\Delta$ according to equation 2.62. The grid currents ($i_g$) relate to the arm ($i_\Delta$) according to equation 2.63

$$v_\Delta(t) = \begin{pmatrix} v_{ab}(t) \\ v_{bc}(t) \\ v_{ca}(t) \end{pmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} v_g(t) \qquad \text{with: } v_g(t) = \begin{pmatrix} V_{g,a}(t) \\ V_{g,b}(t) \\ V_{g,c}(t) \end{pmatrix} \tag{2.62}$$

$$i_g(t) = \begin{pmatrix} i_{g,a}(t) \\ i_{g.b}(t) \\ i_{g,c}(t) \end{pmatrix} = \begin{bmatrix} -1 & 0 & 1 \\ 1 & -1 & 0 \\ 0 & 1 & -1 \end{bmatrix} i_\Delta(t) \qquad \text{with: } i_\Delta(t) = \begin{pmatrix} i_{ab}(t) \\ i_{bc}(t) \\ i_{ca}(t) \end{pmatrix} \tag{2.63}$$

Figure 2.21 represents the resulting equivalent model of the Delta connected MMC.

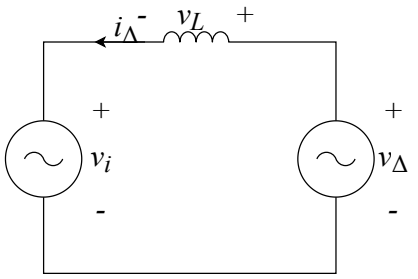



**Figure 2.21:** Delta Arm Equivalent Circuit

The switching function can now be defined according to equation 2.64.

$$S(t) = \frac{2}{V_{DC}} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \left( P^{-1} \begin{pmatrix} V_d^* \\ V_q^* \end{pmatrix} \right) \tag{2.64}$$

Figure 2.22 shows the implementation of this mathematical model in PLECS. The controller contains the Star to Delta transformation after the inverse Park-Clarke Transform. This is simulated and compared to a switched model using the parameters in table 2.7.

| Symbol | Parameter | Value |
|---|---|---|
| S | Total Appereant Power | 1 [MVA] |
| $\hat{v_g}$ | AC Peak Voltage | 2.7 [kV] |
| N | Submodules per Arm | 4 |
| $V_{SM}$ | Submodule Voltage | 1.169 [kV] |
| $C_{SM}$ | Submodule Capacitance | 1.25 [mF] |
| $R_{C,SM}$ | $C_{SM}$ ESR | 1 [mΩ] |
| $L_{arm}$ | Arm Inductance | 10 [mH] |
| $R_L$ | $L_{arm}$ ESR | 1 [mΩ] |
| $L_g$ | AC Grid Inductance | 0 [H] |
| $R_g$ | AC Grid Resistance | 0 [Ω] |
| $f_g$ | Grid Frequency | 50 [Hz] |
| $f_s$ | MMC Switching Frequency | 10 [kHz] |
| $n$ | DAB Transformer Turn Ration | 1169/800 |
| $L_{DAB}$ | DAB Inductance | 85.4 [µH] |
| $f_{DAB}$ | DAB Switching Frequency | 20 [kHz] |
| $C_{DAB}$ | DAB Output Capacitance | 220 [µF] |
| $R_{C,DAB}$ | $C_{DAB}$ ESR | 10 [mΩ] |
| $R_{lvdc}$ | LVDC Resistive Load | 0.64 [Ω] |
| $K_{p,I}$ | Current Control Proportional Gain | 1 |
| $K_{i,I}$ | Current Control Integral Gain | 100 |
| $K_{p,V}$ | Voltage Control Proportional Gain | 2 |
| $K_{i,V}$ | Voltage Control Integral Gain | 10 |
| $K_w$ | Voltage Control Anti-Windup Gain | 10 |
| $I_{sat}$ | Reference Current Saturation | 271.6 [A] |
| $K_{p,DAB}$ | DAB Control Proportional Gain | $5 \cdot 10^{-5}$ |
| $K_{i,DAB}$ | DAB Control Integral Gain | 0.1 |

**Table 2.7:** Simulation Parameters of Double Star SST and its Mathematical Model

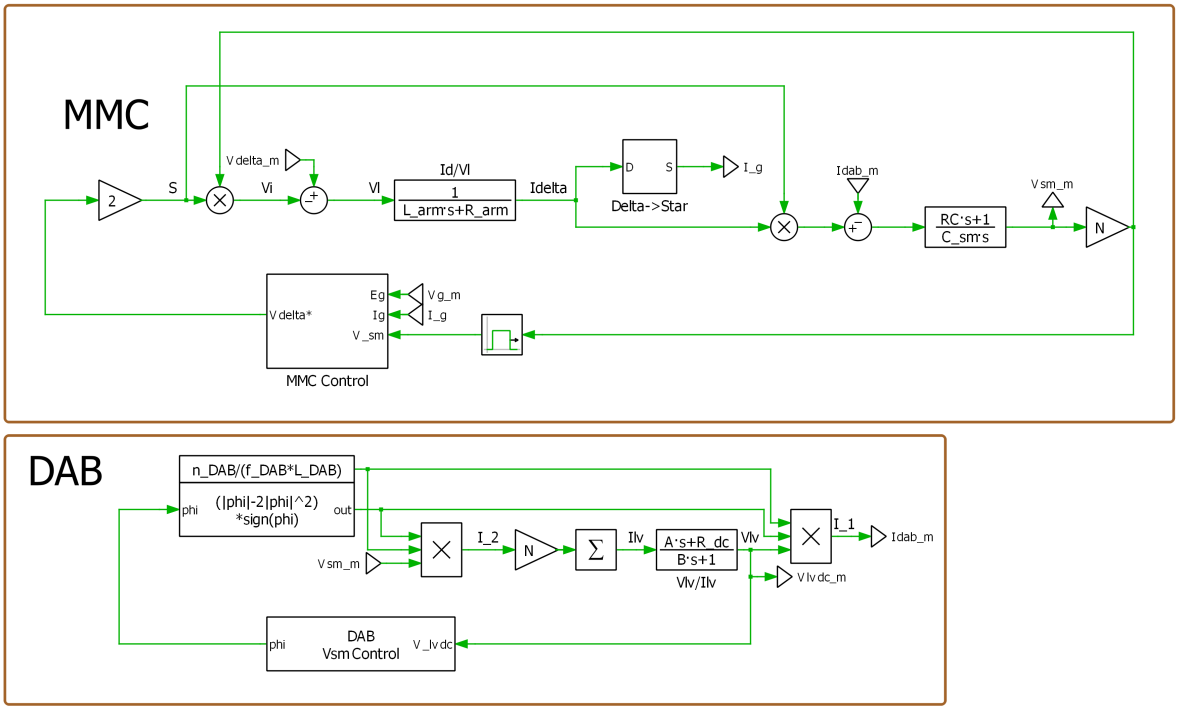



**Figure 2.22:** Mathematical Model of the Single-Delta SST

Figure 2.23 shows the simulation results of the comparison. The mathematical model and the switched simulation results are plotted in the same scope. A high overlap with slight deviations in the submodule voltage waveforms is visible. This is similar to the Single-Star model. This leads to the conclusion that the model is accurate for reviewing the behaviour of the SST.

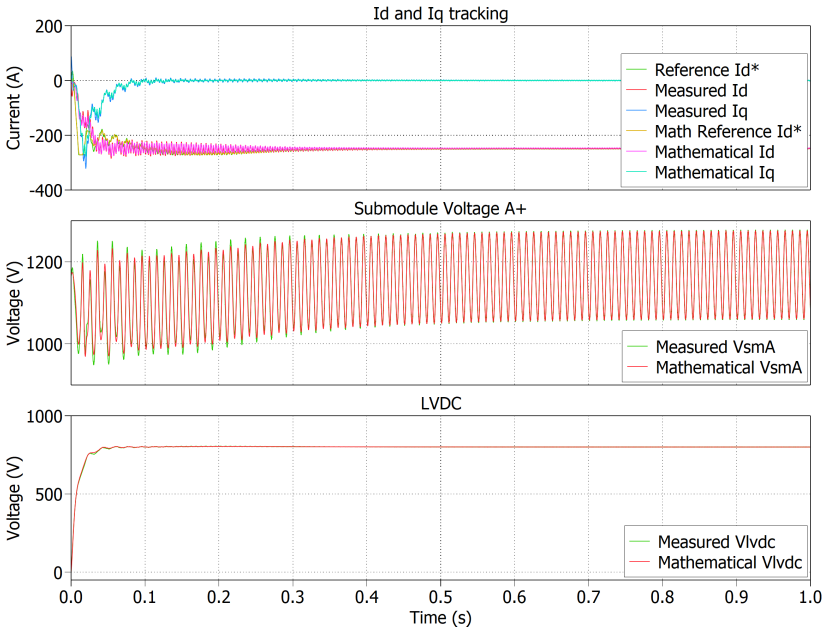



**Figure 2.23:** Comparison of the Mathematical Model and a Switched Single-Delta SST Simulation

## 2.6. Mathematical Modeling Conclusion

To conclude, the various mathematical models for the Solid State Transformers can be used to accurately determine the behaviour of $I_d$, $I_q$, $V_{SM}$, $V_{LV}$ and the control system. The usage of the new mathematical model to simulate an SST is compared to the switched simulation and using the average model [42] in table 2.8.

The mathematical model is the fastest of all three due to the fast DAB modelling and the fact that the simulation speed is independent of the number of submodules per leg (N). However, the model is therefore not able to model unbalances between submodules. The switched model is the most accurate but also the slowest, it is required for accurately determining parameters such as the THD. The switched and average models are built up schematic-wise, which helps to analyse the SST visually. The mathematical model is built using analytical equations, which can help to understand the behaviour and relations between the different voltages and currents.

The mathematical model can be used to evaluate the control system and behaviour of the SST, after which this can be checked in a switched simulation.

| **Switched Model** | **Mathematical Model** | **Average Model** |
|---|---|---|
| Very accurate | Accurate for analysing the behaviour | Accurate for analysing the behaviour |
| Includes switching effects | Does not include switching effects | Does not include switching effects |
| Can model SM Voltage unbalance | Can not model SM Voltage unbalance | Can model SM Voltage unbalance |
| Simulation speed dependent upon N | Simulation speed independent from N | Simulation speed dependent upon N |
| Slow MMC Simulation | Fast MMC Simulation | Fast MMC Simulation |
| Slow DAB Simulation | Fast DAB Simulation based upon phase-shift | Slow DAB Simulation |
| Model built using a schematic | Model built using analytical equations | Model built using a schematic. |

**Table 2.8:** Comparison of switched, mathematical and average modelling of the SST (Table 2.8)

# 3

# Control System Design

## 3.1. MMC Control System

The double-star MMC has a control scheme to balance the MVDC-link voltage, powering a DC load from the MVAC grid. Figure 3.1 shows the controller of this system. The average submodule voltage is used as the input for the voltage controller. The voltage controller uses a PI control on the submodule voltage error to generate a d-component reference current. The PI control uses saturation including anti-windup to limit the grid current. By default, the saturation limit is 10% above the rated grid current.

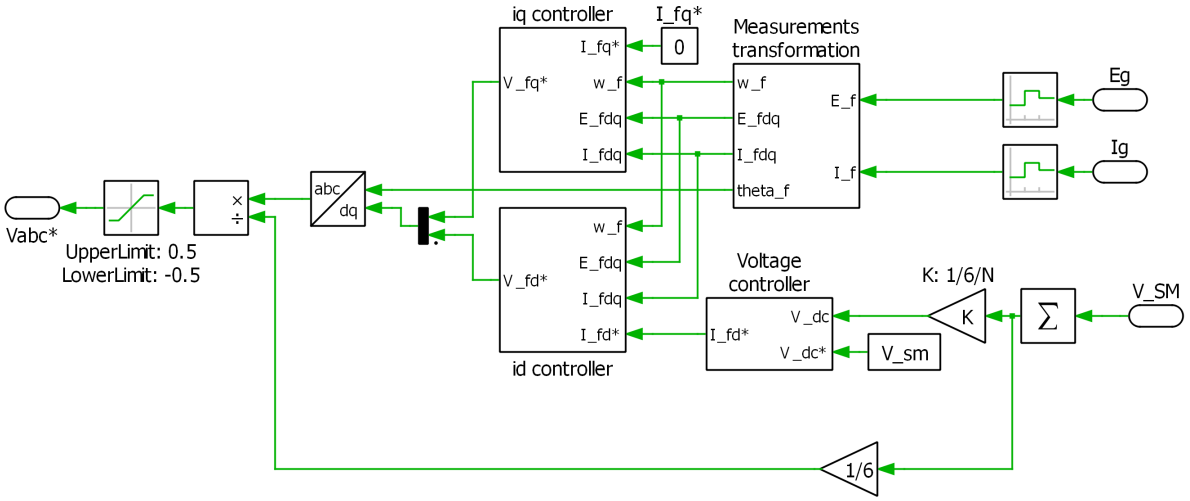
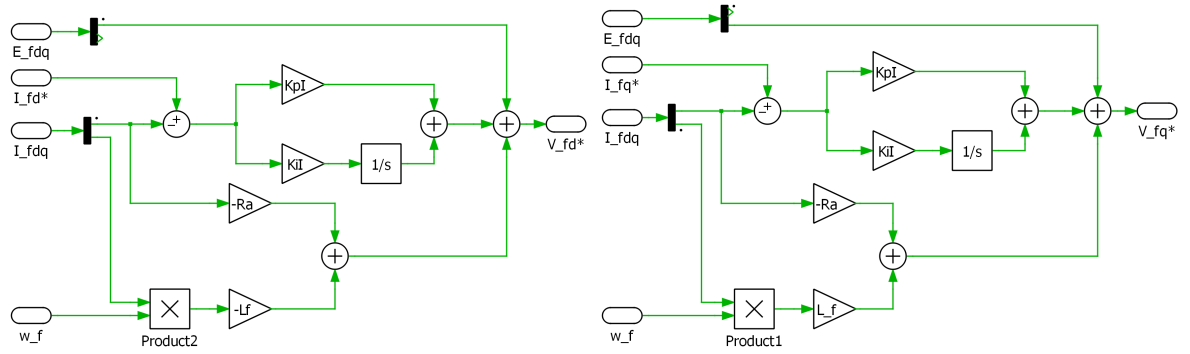



**Figure 3.1:** Control System of the MMC

The measurements transformation uses a 3-phase phase lock loop (PLL), provided by PLEXIM [10]. The measured grid voltages and currents are converted into their d and q components using the Park-Clarke transform $P$. The outputs are used with the generated reference current to generate the desired reference d and q component output voltages of the MMC. Figure 3.2 shows the by PLEXIM [10] provided current controller for the d-component. This current controller is described in [49].




**(a)** d-component controller

**(b)** q-component controller

**Figure 3.2:** Current Controller

The current error goes into a PI-control. The PI output, an $I_d$ and series resistance dependent component, an $I_q$ and series inductance component, and the grid voltage d-component are summed to generate the controller output $V_d^*$. The controller for the q-component works the same using the q- instead of d-components, a 0A reference current, and an $I_d$ and series inductance component.

The values are calculated from the PI cutoff frequency $\alpha_f$ according to the by PLEXIM[10] provided equations:

$$L_f = \frac{L_{arm}}{2} + L_{grid} \tag{3.1}$$

$$R_f = \frac{R_{arm}}{2} + R_{grid} \tag{3.2}$$

$$R_a = \alpha_f \cdot L_f - R_f \tag{3.3}$$

$$K_{p,I} = \alpha_f \cdot L_f \tag{3.4}$$

$$K_{i,I} = \alpha_f \cdot (R_f + R_a) \tag{3.5}$$

The references $V_d^*$ and $V_q^*$ are turned into the reference AC output voltages ($V_o^*$) using the inverse Park-Clarke transform $P^{-1}$. $V_o^*$ is divided by the measured MVDC-link voltage and limited to $\pm 0.5$ using saturation. This gives the reference AC waveforms for the PSC-based modulator, generating the desired switching signals for the submodules.

## 3.2. SST Control System A

The first control system, control system A, is based on the control system of the double-star MMC. Figure 3.3 shows this control system. The same current control is used as with the MMC control (figure 3.2). The reference d-component current is calculated using a PI control on the average submodule voltage of all submodules. The low voltage DC link is controlled through the DAB using single phase shift modulation [47] where the phase shift is generated using a PI control on the low voltage DC bus.

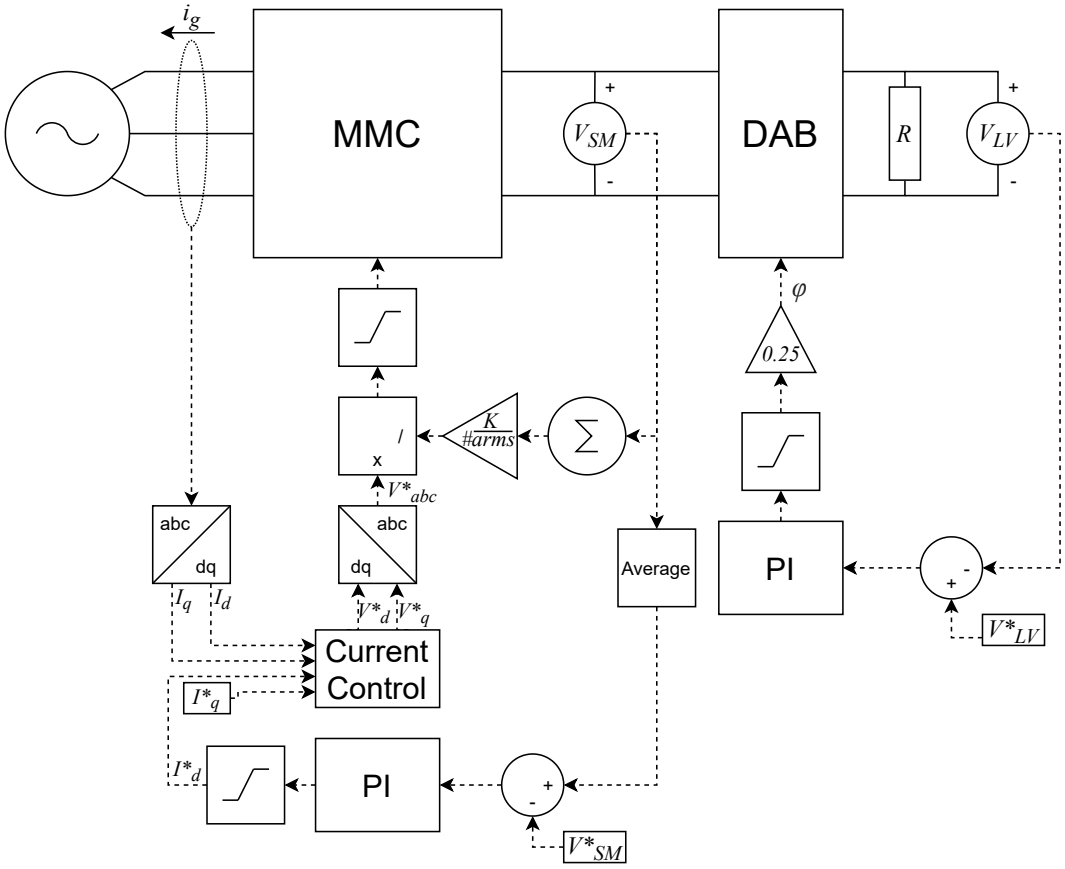



**Figure 3.3:** Control System A

The single-star and delta topologies do not contain an MVDC-Link, therefore the reference AC voltage is now divided by the equivalent DC-Link voltage, calculated by equation 3.6, where K=1 in the case of a half-bridge submodule and K=2 in the case of a full-bridge submodule. #legs is the total number of MMC legs, which is 6 for double-star and 3 for single-star or delta topologies.

$$V_{MVDC,eq} = \frac{K}{\#arms} \sum V_{SM} \tag{3.6}$$

The control system contains three saturation blocks, for the reference AC waveforms, the reference d-component current and the phase shift modulation index. The saturation limits are $\pm 0.5$, $\pm 1.1 \cdot \hat{I}_g$ and $\pm 1$ respectively. The phase-shifted modulator compares the reference AC waveform to a triangular waveform between $\pm 0.5$ and therefore has a maximum input of the same amplitude. The current saturation is in place to limit the grid current and the current flowing through the converter. The current saturation allows for a 10% overshoot on the maximum current. The phase shift modulus is a number between $\pm 1$, resulting in a phase shift between $\pm 0.25$ where maximum power flow occurs according to equation 2.46.

The main advantage of control system A is simplicity. Only one PI controller is required for all the DAB's. The MMC control loop is completely separate from the DAB control loop which can improve the system's stability. The main disadvantage of control system A is that this offers no control over the individual submodule voltages.

## 3.3. SST Control System B

In the second control system, referred to as control system B, the voltage of the LVDC link now controls the d-component reference current, each DAB is controlling its individual submodule voltage. Figure 3.4 shows this control system. The saturation limits are the same as for control system A.

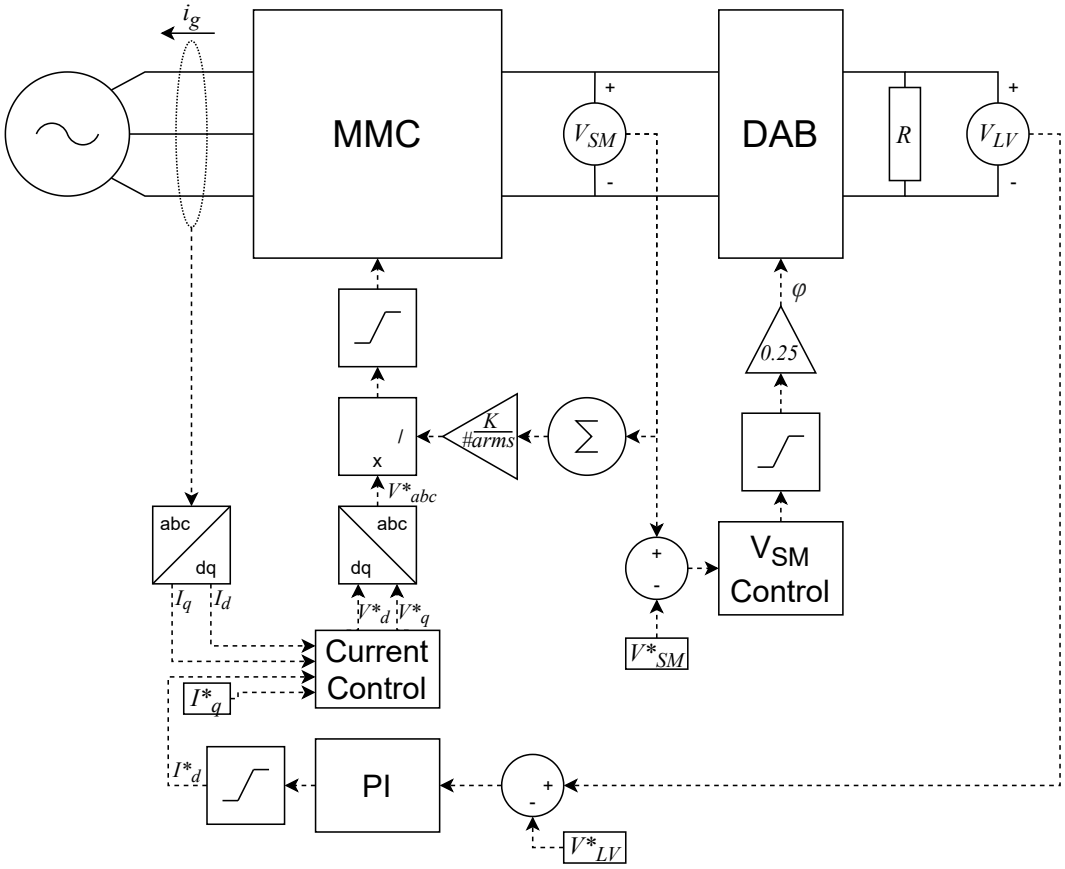



**Figure 3.4:** Control System B

The individual submodule voltages can be controlled by using an individual PI control for each DAB. When $V_{SM}$ exceeds the desired value, the phase shift of the DAB and therefore the DAB current will increase, drawing current from the submodule capacitor, which in turn reduces $V_{SM}$. Vice versa when $V_{SM}$ goes below the desired value. This will influence the LVDC link, which in turn is used to determine the grid and therefore MMC current flowing into the submodule capacitors.

The main advantage of control system B is the capability to control the individual submodule voltages, guaranteeing these to be stable. The main disadvantage is that the different control loops are no longer separate and will influence each other. Therefore, the control parameters can no longer be tuned individually, resulting in higher control parameter tuning complexity than control system A.

## 3.4. SST Control System C

The third control system, referred to as control system C, works similarly to control system B, and assumes a stable voltage source on the LVDC link. This could be achieved by, e.g. a battery energy storage system (BESS). Figure 3.5 shows this control system.

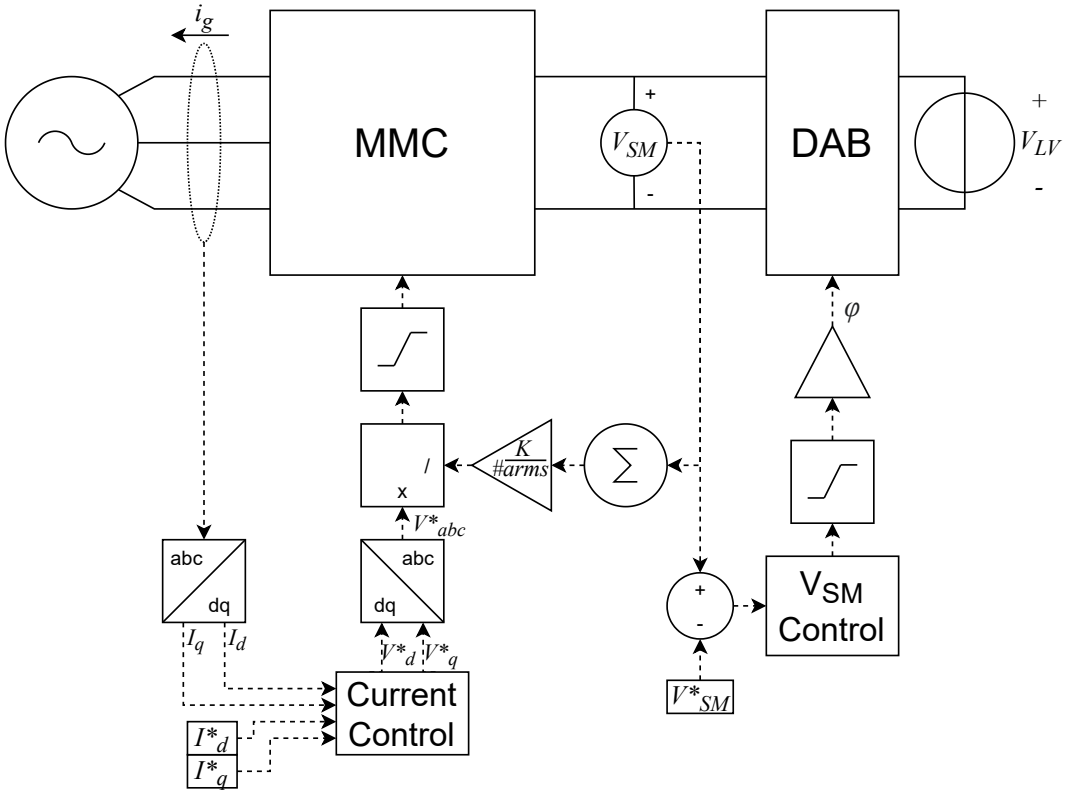



**Figure 3.5:** Control System C

The now present stable voltage source removes the need to control the voltage of the LVDC link. This removes one control loop and reduces the control system's complexity compared to control systems A and B. Furthermore, the DAB can now be controlled using a stable voltage on one side. This allows for easier tuning of the control parameters and faster DAB control while maintaining stability.

The main advantage of control system C is the reduced complexity in the control system and therefore faster operation of the control system while controlling the individual submodule voltages. Therefore, this control system removes the disadvantages of both control systems A and B. The main disadvantage of control system C is the requirement of a stable DC source on the LVDC side.

## 3.5. Improved DAB Control: Control Systems B* and C*

The proposed control systems are not the ideal solution to reduce voltage ripple due to the limited PI controller speed. A novel Improved DAB control using current feedforward combined with an inverted model of the DAB is proposed. Figure 3.6 shows this model. As the submodule input current is the product of the arm current and the switching function (equation 2.35), the input of the submodule can be seen as a current source.

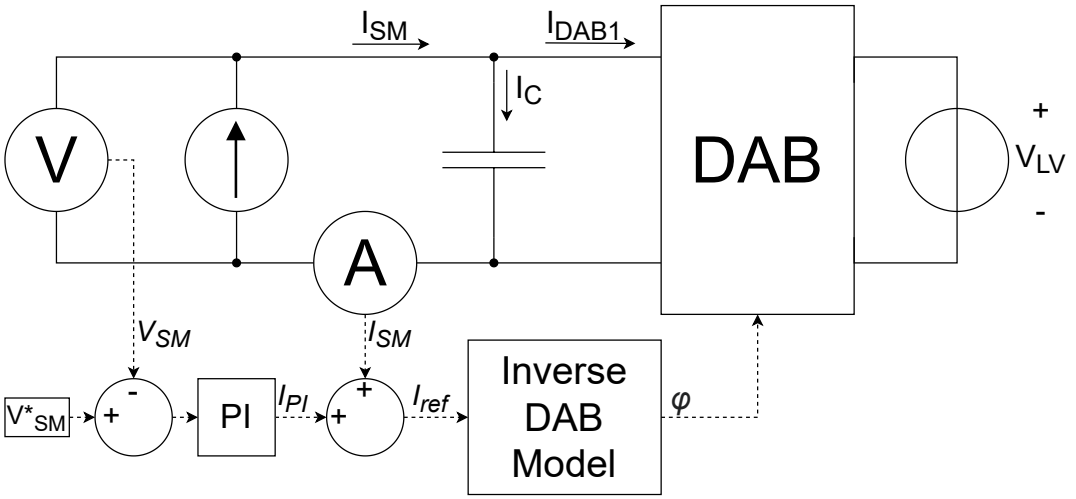



**Figure 3.6:** Proposed improved DAB control, combining current feedforward with the inverse DAB model

The capacitor voltage ripple is caused by the current through the capacitor (equation 3.9). Reducing this current to 0 will remove the voltage ripple (equation 3.11). The proposed mathematical model has been shown to be accurate for determining the DAB input current from the phase shift ($\phi$). Therefore, it is theoretically possible to determine the phase shift ($\phi$) from the DAB input current by inverting the mathematical DAB model.

If the phase shift ($\phi$) is calculated from the pre-capacitor submodule current ($I_{SM}$), the post-capacitor submodule current ($I_{DAB1}$) will theoretically be equal. Therefore, the capacitor current ($I_C$) will be zero, and the submodule voltage ripple will be zero.

As the proposed system is still prone to measurement errors, saturation, and DAB model errors, there might still be small deviations between $I_{DAB1}$ and $I_{SM}$. To ensure stability, a submodule voltage PI control is still used, generating $I_{PI}$. This current would ideally be zero in the case of no voltage ripple. The reference current $I_{ref}$ will then become the sum of $I_{SM}$ and $I_{PI}$, ensuring a stable submodule voltage with reduced ripple.

The novel improved DAB control consists of a combination of current feedforward and the inverse DAB model. Both linearisation based on similar equations and the use of current feedforward is presented in [46, 48, 50]. Though this shows similar control methods, the presented techniques deviate from the proposed model in terms of the combination, controller topology, and/or used equations.

### 3.5.1. Control Derivation with the Inverted DAB Model

Using 2.42 as an approximation for an instantaneous equation gives:

$$P(t) = \frac{V_1(t)V_2(t)n}{f_s L}(|\phi| - 2|\phi|^2) \cdot sign(\phi) \tag{3.7}$$

$$I_1(t) = \frac{V_2(t)n}{f_s L}(|\phi| - 2|\phi|^2) \cdot sign(\phi) \tag{3.8}$$

This means that controlling the DAB with a phase shift is controlling its current. As the submodule voltage is the integral of the submodule current (equation 3.9), the voltage will always be lagging the current. Therefore, a PI control could not be optimal for reducing the voltage ripple.

$$V_{SM}(t) = \frac{1}{C_{SM}} \int_{t=0}^{t=t} I_{C_{SM}}(t)dt + [V_{SM}(t=0) = V^*_{SM}] \tag{3.9}$$

$$I_{C_{SM}}(t) = I_{SM}(t) - I_{DAB1}(t) \tag{3.10}$$

$$V_{SM,ideal}(t) = V^*_{SM} \rightarrow I_{C_{SM},ideal} = 0 \rightarrow I_{SM}(t) = I_{DAB1}(t) \tag{3.11}$$

To remove or reduce the ripple, ideally, the DAB current would equal the SM current (Equation 3.11). As the DAB current is controlled by the SM voltage, which is lagging with respect to the SM current, the generated DAB current will always be lagging the SM current. Therefore, the submodule voltage ripple can never be properly reduced using only PI control, for a dynamic situation. The proposed PI control of control systems B and C is therefore not the ideal solution with the desire to reduce the submodule voltage.

To compensate for the submodule voltage ripple, a component is required which has $I_{DAB1}(t)$ follow $I_{SM}(t)$. Equation 3.8 can be inverted to calculate the required phase shift for a given reference current $I^*_{DAB1}(t)$. Define $\alpha$ according to equation 3.12, as the phase shift dependent scale of the minimum to maximum DAB power. This gives the inverted equation, equation 3.14.

$$\alpha = f(\phi) = (|\phi| - 2|\phi|^2) \cdot sign(\phi) \tag{3.12}$$

$$(-0.25 \leq \phi \leq 0.25) \rightarrow (-0.125 \leq \alpha \leq 0.125) \tag{3.13}$$

$$\phi = f^{-1}(\alpha) = 0.25(\pm 1 \pm \sqrt{1 \pm 8\alpha}) \tag{3.14}$$

For positive $\alpha$, $\phi$ must be between 0 and 0.25 and for negative $\alpha$, $\phi$ must be between -0.25 and 0. This means that $0 \leq \sqrt{1 \pm 8\alpha}) \leq 1$, leading to:

$$\begin{cases} \sqrt{1-8\alpha} & \text{for positive } \alpha \\ \sqrt{1+8\alpha} & \text{for negative } \alpha \end{cases} = \sqrt{1-8|\alpha|} \tag{3.15}$$

Furthermore, the signal must be continuous at $\alpha = 0$ and $0 \leq |\pm 1 \pm \sqrt{1-8|\alpha|}| \leq 1$, which leads to:

$$4\phi = 4f^{-1}(\alpha) = \begin{cases} 1 - \sqrt{1-8|\alpha|} & \text{for positive } \alpha \\ -1 + \sqrt{1-8|\alpha|} & \text{for negative } \alpha \end{cases} = sign(\alpha)(1 - \sqrt{1-8|\alpha|}) \tag{3.16}$$

For a desired input current $I*_{DAB1}(t)$, $\alpha(t)$ can be substituted, leading to:

$$\alpha(t) = \frac{f_s L}{nV_2(t)} I^*_{DAB1}(t) \tag{3.17}$$

$$\begin{aligned} \phi(t) &= 0.25 \cdot sign\left(\frac{f_s L}{nV_2(t)} I^*_{DAB1}(t)\right)\left(1 - \sqrt{1 - 8\left|\frac{f_s L}{nV_2(t)} I^*_{DAB1}(t)\right|}\right) \\ &= 0.25 \cdot sign\left(\frac{f_s L}{nV_2(t)} I^*_{DAB1}(t)\right) - sign\left(\frac{f_s L}{nV_2(t)} I^*_{DAB1}(t)\right)\sqrt{1 - 8\left|\frac{f_s L}{nV_2(t)} I^*_{DAB1}(t)\right|} \end{aligned} \tag{3.18}$$

Using the measured submodule current $I_{SM}(t)$ as reference DAB input feedforwarded current theoretically gives:

$$I^*_{DAB1}(t) = I_{SM}(t) \tag{3.19}$$

$$I_{C_{SM}}(t) = I_{SM}(t) - I^*_{DAB1}(t) = 0 \rightarrow V_{SM}(t) = V_{SM}(t=0) = V^*_{SM} \tag{3.20}$$

### 3.5.2. Improved DAB Control Implementation

While ideally, this would completely remove the ripple, there are two points of discussion with this control. Firstly, as equation 2.46 depicts, there is a maximum power and therefore maximum current in the DAB. With the PI control, the DAB only needs to handle the average SM current. For the current feedforward control, there are two options:

1. Keep a similar maximum DAB current and partly reduce the ripple.
2. Increase the maximum DAB current beyond the peak of the submodule current to avoid saturation and completely remove the ripple.

With these two options, the choice can be made to have a similar ripple with a similarly sized DAB or to oversize the DAB to completely remove the 50Hz ripple, up to anything in between.

Figure 3.7 shows the proposed control system, implemented for a switched model in PLECS. The saturation limits $\alpha$ to $\pm 0.125$, as this leads to the desired phase shift limits and prevents the square root of a negative number. All measured signals are averaged to filter out switching noise.

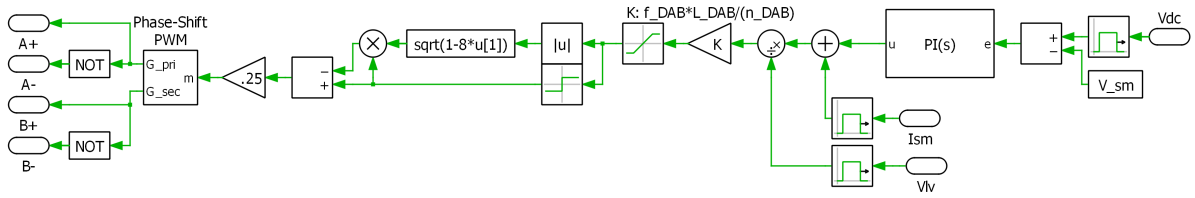



**Figure 3.7:** Proposed improved DAB control based on current feedforward into the inverse DAB model (PLECS)

Control systems B and C, with the improved DAB control, are referred to as control systems B* and C*, respectively.

## 3.6. Tuning of the Control System

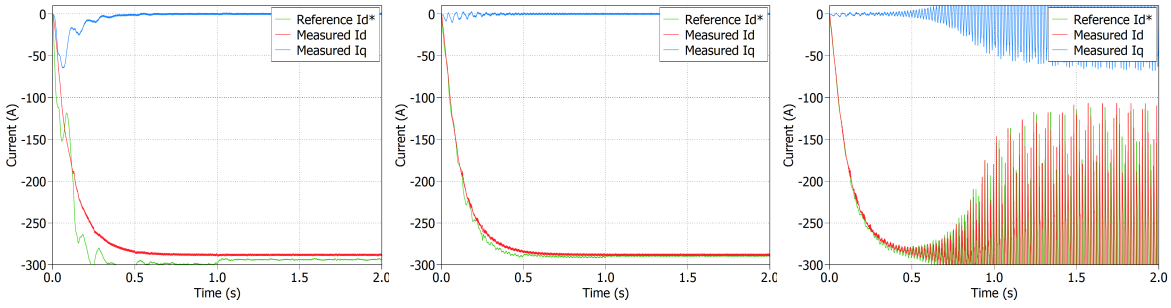
This section describes two different methods of tuning the control system, manual tuning and an automated tuning method using the Genetic Algorithm from Matlab. The following 5 parameters will be tuned: The current control bandwidth $\alpha_f$, the voltage control gains $K_{p,V}$ and $K_{i,V}$, and the DAB control gains $K_{p,DAB}$ and $K_{i,DAB}$. The tuning is done using an implementation of the mathematical model. The tuning will be demonstrated using a 3.5MVA Double-Star SST. Table 3.1 shows the used parameters of this SST. The DAB inductance is chosen such that: $P_{DAB,max} = 1.2 \cdot P_{SM}$

| Symbol | Parameter | Value |
|---|---|---|
| S | Total Appereant Power | 3.5 [MVA] |
| $\hat{V}_g$ | AC Peak Voltage | 8.1 [kV] |
| N | Submodules per Arm | 12 |
| $V_{SM}$ | Submodule Voltage | 1.35 [kV] |
| $C_{SM}$ | Submodule Capacitance | 2.93 [mF] |
| $R_{C,SM}$ | $C_{SM}$ ESR | 1 [mΩ] |
| $L_{arm}$ | Arm Inductance | 10 [mH] |
| $R_L$ | $L_{arm}$ ESR | 1 [mΩ] |
| $L_g$ | AC Grid Inductance | 0 [H] |
| $R_g$ | AC Grid Resistance | 0 [Ω] |
| $n$ | DAB Transformer Turn Ration | 1350/800 |
| $L_{DAB}$ | DAB Inductance | 195 [µH] |
| $f_{DAB}$ | DAB Switching Frequency | 20 [kHz] |
| $C_{DAB}$ | DAB Output Capacitance | 220 [µF] |
| $R_{C,DAB}$ | $C_{DAB}$ ESR | 10 [mΩ] |
| $R_{lvdc}$ | LVDC Resistive Load | 182.9 [mΩ] |

**Table 3.1:** Simulation Parameters of the 3.5MVA Double Star SST used for the control tuning

### 3.6.1. Current Control Bandwidth

Figure 3.8 shows the evaluation of adjusting $\alpha_f$. Comparing Figure 3.8a to 3.8b shows that increasing $\alpha_f$ from 150 to 500 increases the accuracy of $I_d$ and $I_q$ following their references (0 for $I_q$). Figure 3.8c shows that increasing the bandwidth too far can lead to instability of the SST.




**(a)** $\alpha_f$ = 150 **(b)** $\alpha_f$ = 500 **(c)** $\alpha_f$ = 1000

**Figure 3.8:** Evaluation of current control bandwidth ($\alpha_f$) with the Double-Star SST Control System A

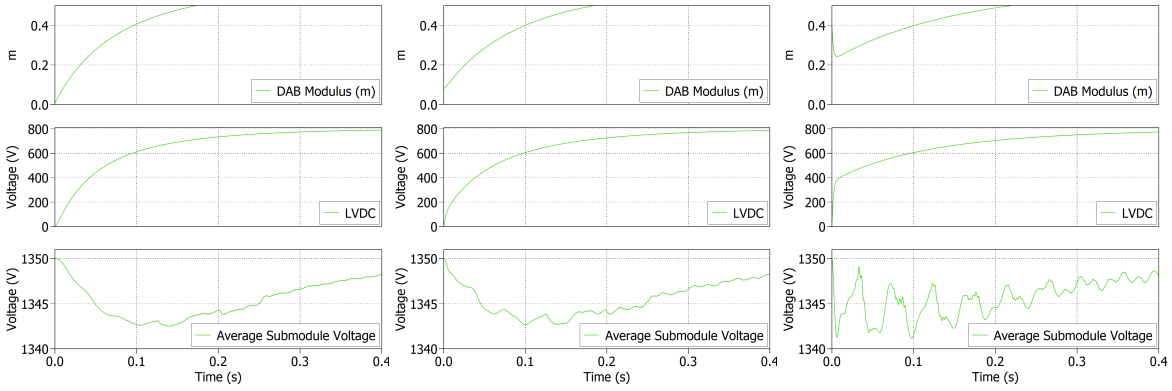
The behaviour of the other parameters are dependent upon the control system which is used.

### 3.6.2. Manual Tuning of Control System A

When the system starts, the DAB control starts working first. This increases the LVDC-bus from 0 to 800V. This will cause a voltage drop on $V_{SM}$ to which the voltage control will respond. Generally speaking the higher the DAB control gains $K_{p,DAB}$ en $K_{i,DAB}$, the faster the output voltage will be increased and the greater the voltage drop on $V_{SM}$ will be.

#### The DAB Control Gains

$K_{p,DAB}$ is a direct factor between the error ($V^*_{SM} - V_{SM}(t)$) and the DAB Modulus (m). The starting modulus will therefore be $m_{DAB}(t = 0) = K_{p,DAB} \cdot V_{LVDC}$. Figure 3.9 demonstrates this changing of the starting position of the DAB modulus and its effect on $V^*_{LVDC}$ and $V_{SM,average}$.

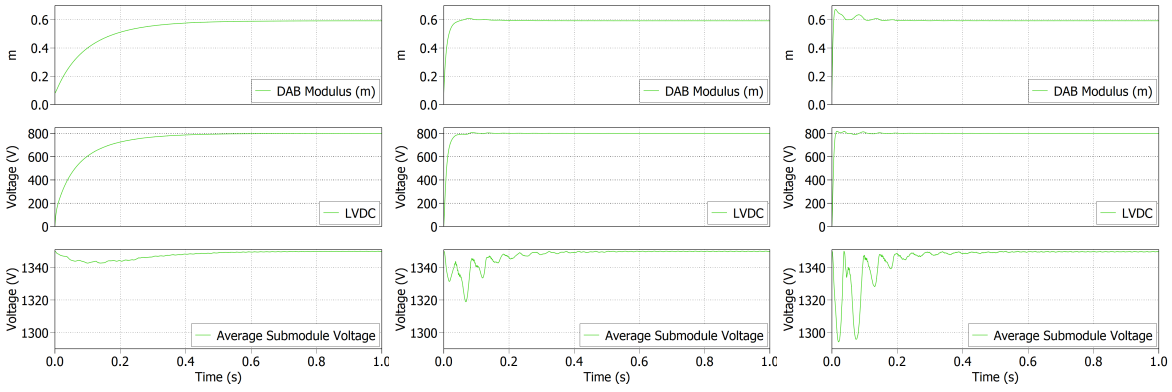



**(a)** $K_{p,DAB} = 0.1 \cdot 10^{-4}$ **(b)** $K_{p,DAB} = 1 \cdot 10^{-4}$ **(c)** $K_{p,DAB} = 5 \cdot 10^{-4}$

**Figure 3.9:** Evaluation of DAB Control Gain $K_{p,DAB}$ with the Double-Star SST Control System A

Increasing the gain will increase the starting point and the initial rise speed of $V_{LVDC}$. Increasing it too far can cause a high transient on the submodule voltage resulting in oscillations, shown in Figure 3.9c.

As $V_{LVDC}$ rises, the error will decrease and so will the effect of $K_{p,DAB}$. This means that $K_{i,DAB}$ has the most effect on the speed at which $V_{LVDC}$ converges. Figure 3.10 demonstrates this effect. Increasing the integrating factor increases the speed at which $V_{LVDC}$ converges as well as the voltage drop on $V_{SM,average}$. Above a particular value, there will be an overshoot on $V_{LVDC}$, as visible in figure 3.10c, where the submodule voltage drop is the largest.

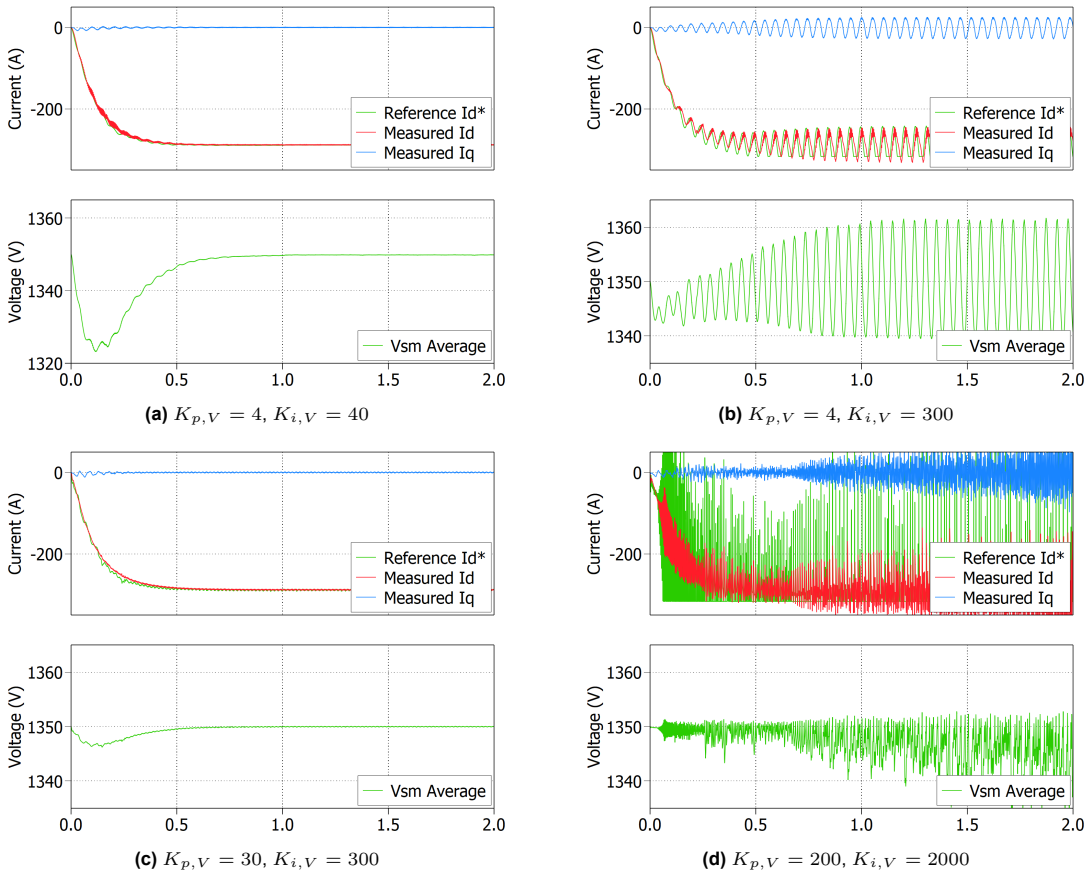



**(a)** $K_{i,DAB} = 0.01$ **(b)** $K_{i,DAB} = 0.08$ **(c)** $K_{i,DAB} = 0.2$

**Figure 3.10:** Evaluation of DAB Control Gain $K_{i,DAB}$ with the Double-Star SST Control System A

### The Submodule Voltage Control Gains

Manually tuning the control gains for the voltage controller is different from that of the DAB. The input error of the controller starts at 0 and gradually increases. Therefore both gains affect the speed at which the reference current $I_d^*$ converges, which in turn determines voltage drop on $V_{SM,average}$. Both gains are limited by the current control bandwidth ($\alpha_f$) as this affects the speed at which the current controller can accurately follow $I_d^*$.




**(a)** $K_{p,V} = 4$, $K_{i,V} = 40$

**(b)** $K_{p,V} = 4$, $K_{i,V} = 300$

**(c)** $K_{p,V} = 30$, $K_{i,V} = 300$

**(d)** $K_{p,V} = 200$, $K_{i,V} = 2000$

**Figure 3.11:** Evaluation of the Voltage Control Gains $K_{p,V}$ and$K_{i,V}$ with the Double-Star SST Control System A

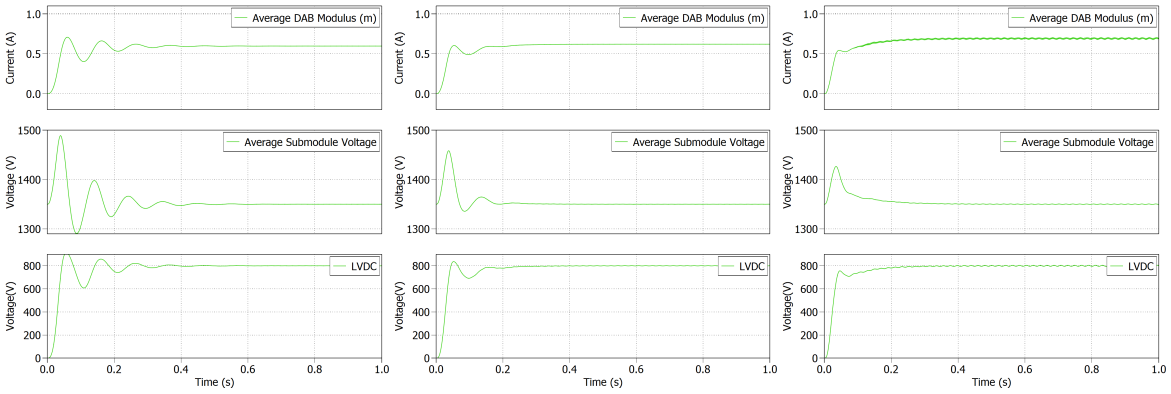
Whereas with the DAB control, the control gains $K_p$ and $K_i$ could be evaluated more independently, this is not the case for the submodule voltage controller. Figure 3.11 demonstrates this. Figure 3.11a shows a stable control, increasing $K_i$ to 300 causes oscillations (Figure 3.11b). However increasing both, reduces the voltage drop and does not cause oscillations (Figure 3.11c). Therefore the ratio between the two gains, also known as the time constant $\tau = \frac{K_p}{K_i}$, determines whether these oscillations occur. Figure 3.11d shows how the system can become unstable when both control gains are too high.

### 3.6.3. Manual Tuning of Control System B

For control system B, the DAB and the voltage controller act the opposite compared to control system A. The voltage controller now acts upon $V_{LVDC}$ and generates the reference current $I^*d$. The DAB Controller now acts upon the submodule voltage.

#### The DAB Control Gains

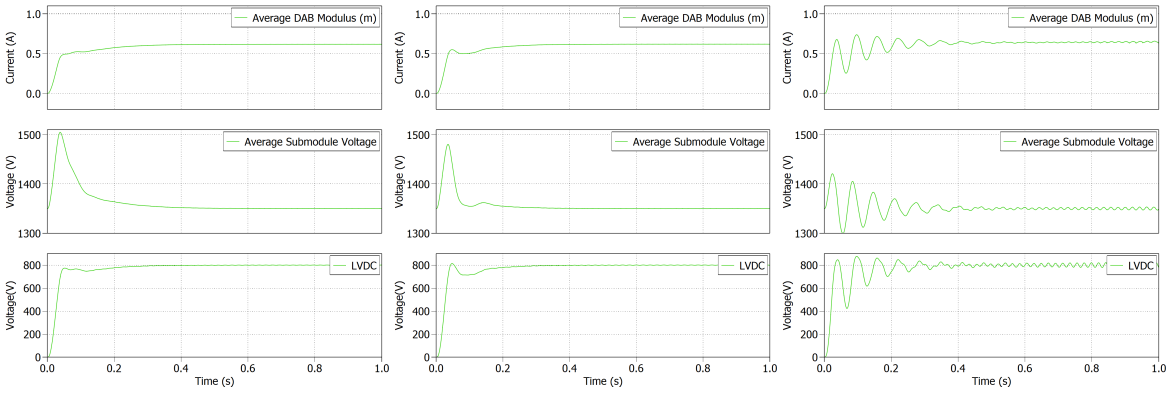
Compared to the other control gains, tThe control gains of the DAB with control system B generally have a smaller margin in which they give the desired result. The control system now acts upon each individual submodule voltage, and such generates a DAB Modulus (m) for each submodule. Only the Average DAB modulus of all the submodules is considered in analysing the control. Figure 3.12 shows the behaviour of the DAB Modules (m), $V_{SM,Average}$ and $V_{LVDC}$ for multiple values of $K_{p,DAB}$. By increasing $K_{p,DAB} = 0.001$ to $K_{p,DAB} = 0.001$ (Figures 3.12a and 3.12b respectively), the voltage overshoot gets reduced and the system converges faster. Further increasing $K_{p,DAB}$ to $0.004$ (Figure 3.12c), further decreases the overshoot. However, this also causes an oscillation on the average DAB modulus, which in turn causes a ripple on $V_{LVDC}$.




**(a)** $K_{p,DAB} = 0.001$ **(b)** $K_{p,DAB} = 0.002$ **(c)** $K_{p,DAB} = 0.004$

**Figure 3.12:** Evaluation of the DAB Control Gain $K_{p,DAB}$ with the Double-Star SST Control System B

The tuning of $K_{i,DAB}$ works similarly. Figure 3.13 shows the effect of increasing $K_{i,DAB}$. Increasing the integral gain reduces the overshoot on the average submodule voltage, however, increasing it too far will cause oscillations within and/or instability of the system. If the DAB control fails to keep the submodule voltage overshoot within a desired margin while remaining stable, the speed of the voltage controller needs to be reduced in order to reduce the overshoot.

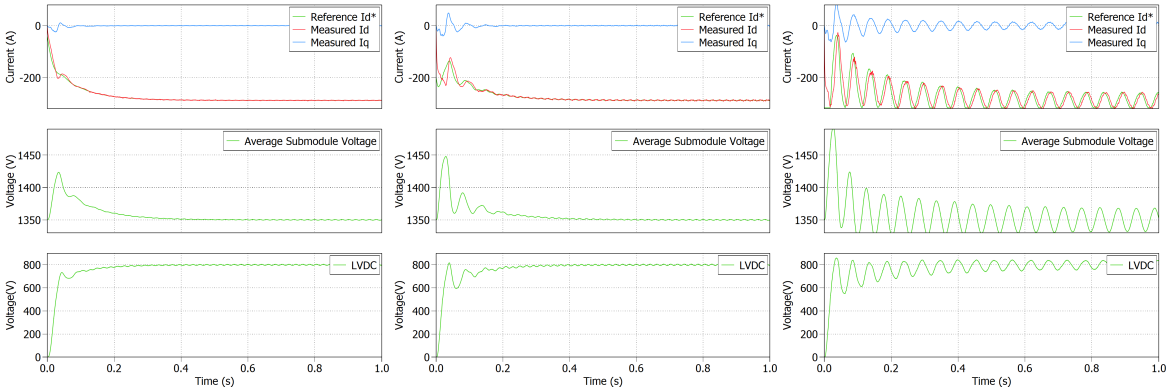



**(a)** $K_{i,DAB} = 0.05$ **(b)** $K_{i,DAB} = 0.1$ **(c)** $K_{i,DAB} = 0.4$

**Figure 3.13:** Evaluation of the DAB Control Gain $K_{i,DAB}$ with the Double-Star SST Control System B

### The LVDC Voltage Control Gains

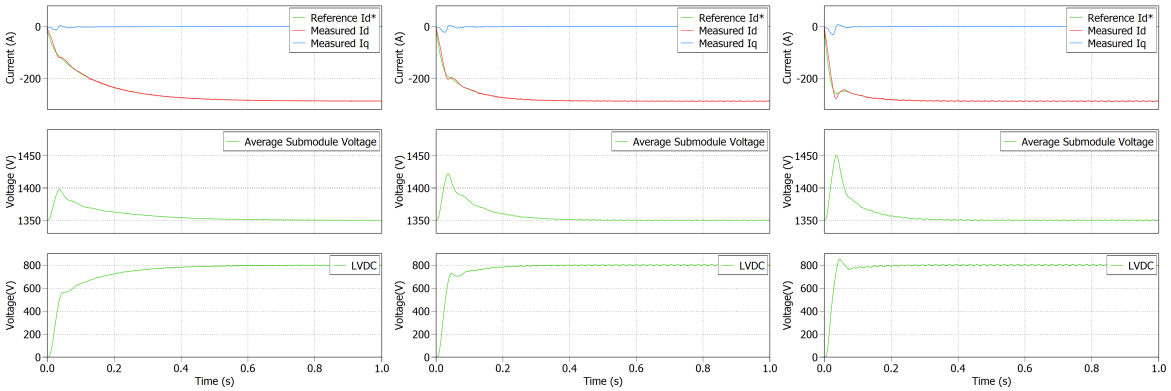
The starting point of the reference current is now determined by $K_{p,V}$. As the current controller starts to work on this reference, the submodule voltage will increase. Therefore the faster the voltage controller works, the higher the submodule voltage drop will be. Figure 3.14 shows the increasing submodule voltage peak together with the increasing starting point of $I_d^*$ as $K_{p,V}$ is increased.




**(a)** $K_{p,V} = 0.05$ **(b)** $K_{p,V} = 0.25$ **(c)** $K_{p,V} = 0.8$

**Figure 3.14:** Evaluation of the Voltage Control Gain $K_{p,V}$ with the Double-Star SST Control System B

Similarly to the integral gain of the DAB in control system A, the voltage integral gain ($K_{i,V}$) of control system B determines how fast the system converges. A higher $K_{i,V}$ leads to a faster convergence, but also to a higher overshoot on the average submodule voltage. Figure 3.15 shows the changes to $I_d^*$, $V_{SM}$ and $V_{LVDC}$ for $K_{i,V} = 5$, $K_{i,V} = 10$ and $K_{i,V} = 15$, confirming the behaviour.




**(a)** $K_{i,V} = 5$ **(b)** $K_{i,V} = 10$ **(c)** $K_{i,V} = 15$

**Figure 3.15:** Evaluation of the Voltage Control Gain $K_{i,V}$ with the Double-Star SST Control System B

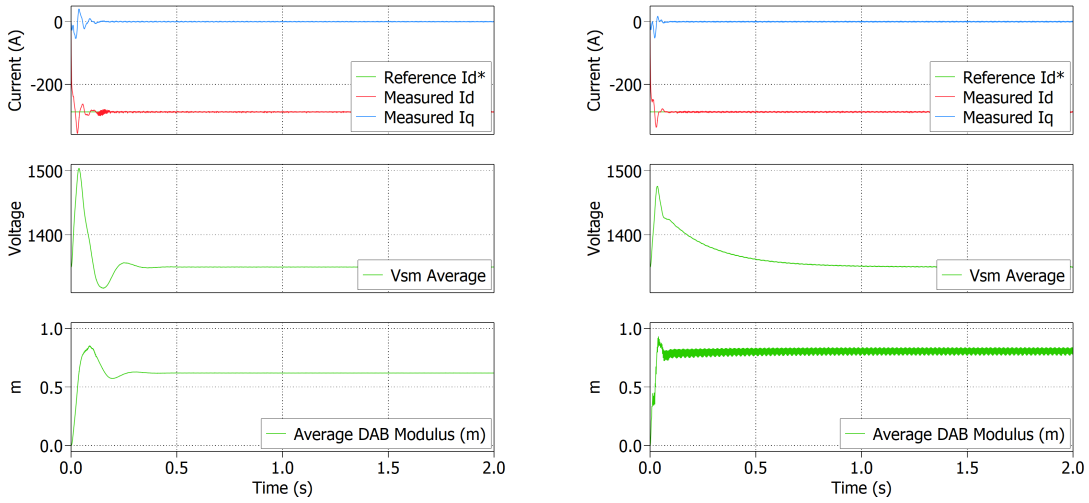
### 3.6.4. Manual Tuning of Control System C

With control system C, there are no voltage control gains to be tuned and the DAB control gains can be tuned similarly to the DAB control gains of control system B.

As the reference current is now set by the desired amount of power, this will naturally give an overshoot on the submodule voltage. Figure 3.16 shows three different methods of reducing the overshoot. These are the following methods:

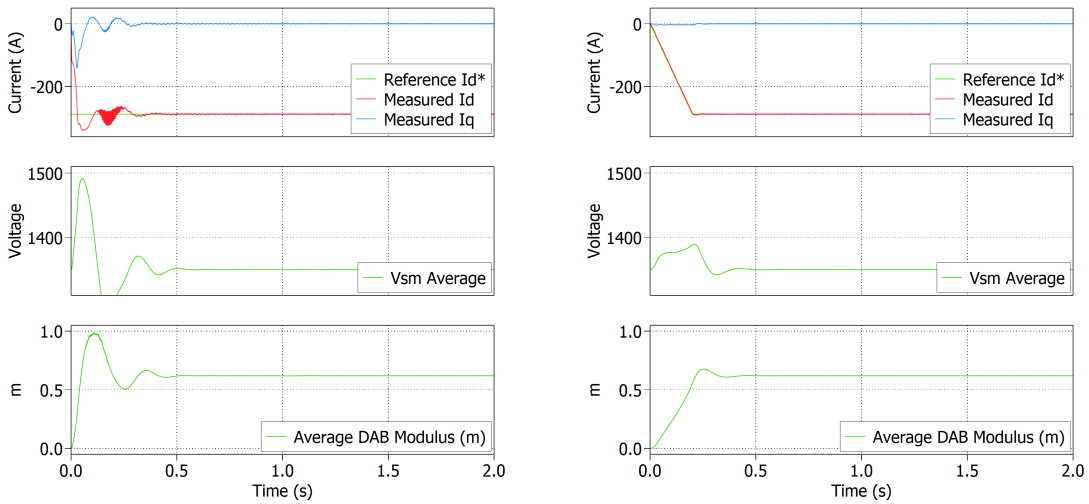
- Increase the DAB gains and allow for a ripple on the average modulus. As the voltage is inherently stable this will not cause instability. (Figure 3.16b)
- Reduce the current control bandwidth $\alpha_f$ to slow down the increase of the current. Reducing this factor too far may cause inaccuracies in the grid current, which can in turn cause the overshoot to increase again. (Figure 3.16c)
- Do not give a set reference current but have it increase gradually. (Figure 3.16d)

It is visible that all three methods reduce the overshoot. However, gradually increasing the desired power gives the most control over the overshoot.




**(a)** $K_{p,DAB} = 0.002$, $K_{i,V} = 0.1$, $\alpha_f = 500$

**(b)** $K_{p,DAB} = 0.02$, $K_{i,V} = 0.1$, $\alpha_f = 500$



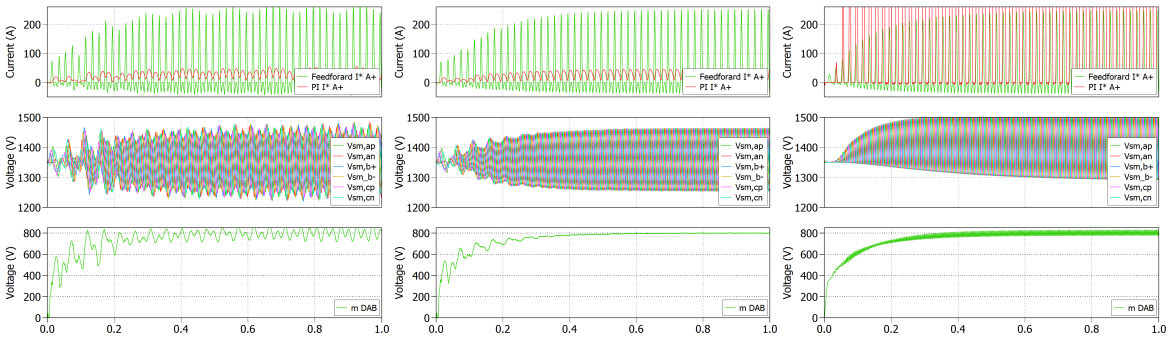

**(c)** $K_{p,DAB} = 0.002$, $K_{i,V} = 0.1$, $\alpha_f = 200$

**(d)** Power reference is increased gradually

**Figure 3.16:** Evaluation of the different methods to reduce the overshoot on $V_{SM}$ with the Double-Star SST Control System C

### 3.6.5. Manual Tuning of Control System B* and C*

The voltage control gains of control system B*, and the DAB integral gain of control system B* and C*, can be tuned similarly to those of control system B. Considering the DAB proportional control gain, the PI values for the DAB will naturally be higher as this generates the reference current instead of a modulus. The current feedforward will naturally help reduce the overshoot. The generated DAB reference current consists of the feedforwarded reference current and the PI control generated reference current. Ideally, only the current feedforward affects the ripple, the PI control can be tuned to a relatively slower speed, only ensuring the average submodule voltage is correct.




**(a)** $K_{p,DAB} = 0.01$ **(b)** $K_{p,DAB} = 0.1$ **(c)** $K_{p,DAB} = 10$

**Figure 3.17:** Effect of $K_{p,DAB}$ with control system B*

Figure 3.17 shows the effect of $K_{p,DAB}$ on control system B+ where the DAB peak power is set to be 2 times the average power requirement. Therefore the sumbodule voltage is affected and the submodule capacitance is reduced to $C_{SM} = 2.5mF$. With a control gain too low the PI generated reference current is not stable, causing an unstable submodule voltage and LVDC bus voltage. Increasing the gain makes the PI generated reference current stable, giving the desired SST behaviour. Increasing the gain too far causes the PI generated reference current to be affected by the submodule voltage ripple and will cause an undesired voltage ripple on the LVDC bus.

### 3.6.6. Automated Tuning of Control System A using the Genetic Algorithm

The control system can also be tuned automatically, using the Genetic Algorithm[51, 52] from Matlab. Figure 3.18 shows the implementation of the mathematical model for control system A as a plant in Matlab Simulink [53]. The implementation of all three topologies is given in Appendix B. Figure 3.19 shows the implementation of control system A, including the plant. The plant can be considered as a non-linear Multiple-Input-Multiple-Output (MIMO) system, therefore there are no conventional methods for tuning such a system. A genetic algorithm can be used to solve highly non-linear problems with multiple parameters [51], which is the case for the SST control system tuning.

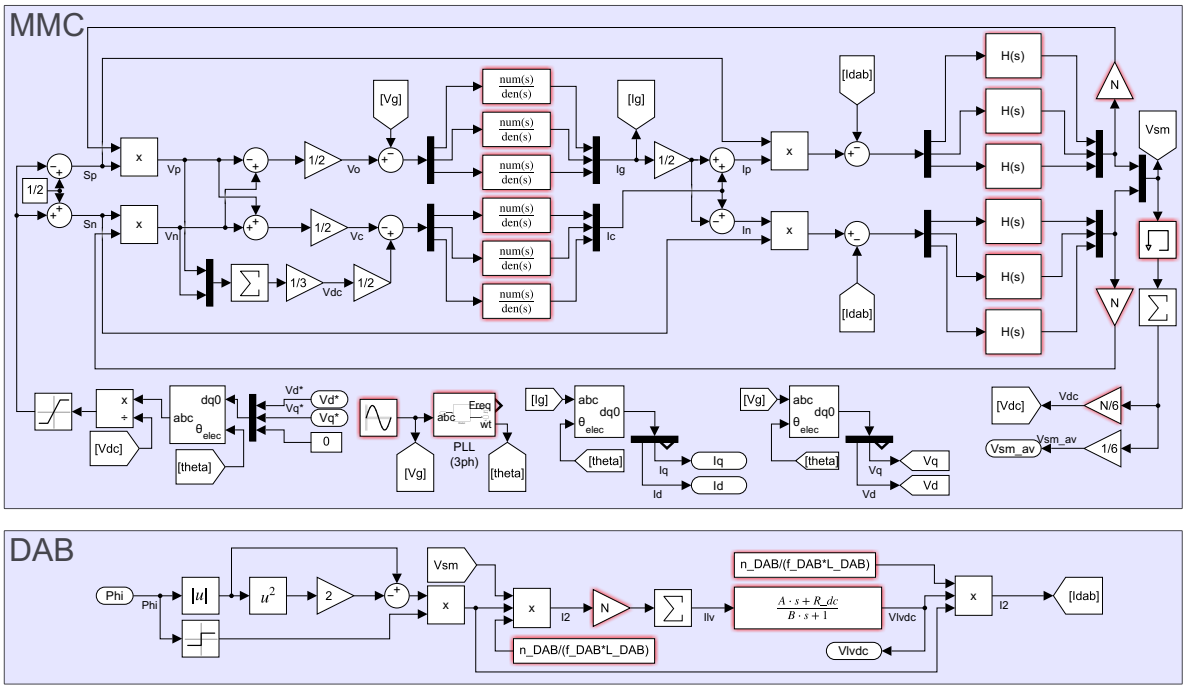



**Figure 3.18:** Implementation of the mathematical model in Matlab Simulink

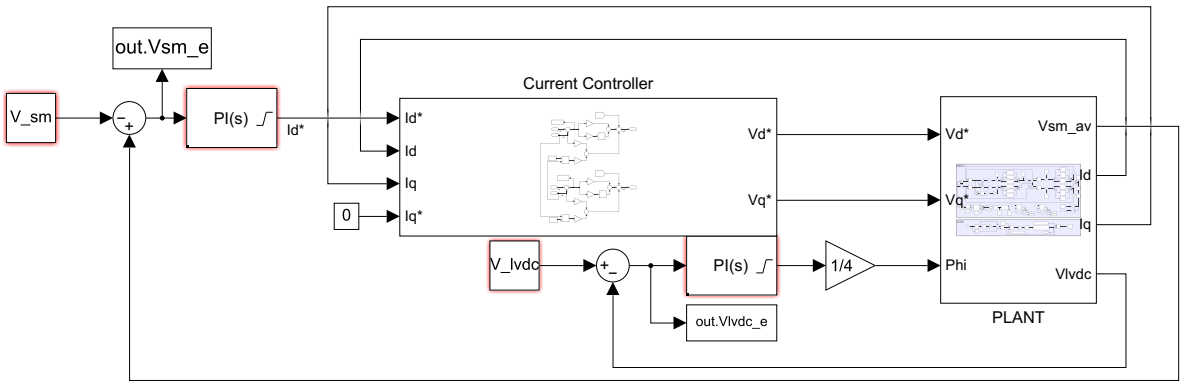



**Figure 3.19:** Implementation of control system A in Matlab Simulink

The implementation of the full switched model of the 3.5MVA SST with N=12 in PLECS takes, depending on the specification of the computer, approximately 6 hours to simulate 2 seconds of behaviour. The same simulation using an implementation of the mathematical model in Matlab Simulink takes approximately 30 seconds. This makes it feasible to run the simulation multiple times to evaluate parameters. The Genetic Algorithm is used to minimise the output of function 3.21. Function 3.21 contains the sum of the square of all errors (SSE) over time of the four outputs of the PLANT, multiplied by four individual weights.

$$ERROR = W_1 \cdot e_{Vlvdc}^2 + W_2 \cdot e_{Vsm}^2 + W_3 \cdot e_{Id}^2 + W_4 \cdot e_{Iq}^2 \tag{3.21}$$

The Genetic Algorithm uses the 5 control parameters ($\alpha_f$, $K_{p,V}$, $K_{i,V}$, $K_{p,DAB}$ and $K_{i,DAB}$) as inputs and will try to optimise these parameters within user given ranges. Optimisation is done to minimise the output of function 3.21. As this algorithm gives no final solution, it requires a user-defined optimisation runtime. The Simulink model is run in parallel on four cores using the Parallel Computing Toolbox [54] in order to maximise the number of iterations for a given time. Furthermore, each time the square error is calculated it first checks if the maximum of the voltage errors does not exceed a 10% overshoot. If it does the error is replaced by a high number ($1 \cdot 10^{32}$), ensuring the algorithm will classify this as a bad solution.

Table 3.1 shows the tuning ranges and results, using a maximum runtime of 6 hours and $W_1 = 0.25$, $W_2 = 1$, $W_3 = W_4 = 1000$.

| | **Input Range** | **Outcome** |
|---|---|---|
| $\alpha_f$ | [50, 500] | 498.2 |
| $K_{p,V}$ | [0.5, 500] | 15.93 |
| $K_{i,V}$ | [1, 1000] | 149.5 |
| $K_{p,DAB}$ | $[5 \cdot 10^{-6}, 5 \cdot 10^{-3}]$ | $8.178 \cdot 10^{-5}$ |
| $K_{i,DAB}$ | $[2 \cdot 10^{-3}, 2]$ | $9.4 \cdot 10^{-3}$ |

**Table 3.2:** Genetic Algorithm Control Tuning ($t = 6h$): Double-Star SST, Control System A

The found control parameters are used in the PLECS Mathematical model. Figure 3.20 shows the result SST behaviour using the automatically tuned control system parameters.

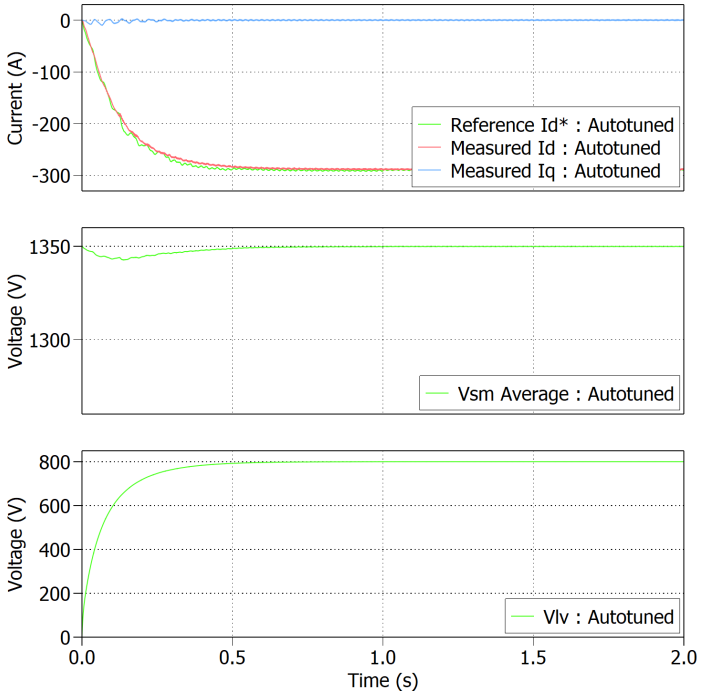



**Figure 3.20:** System response of control system A tuned using the Genetic Algorithm

### 3.6.7. Automated Tuning of Control System C using the Genetic Algorithm

The Genetic Algorithm is run to tune control system C for 3 hours with $W_1 = 0$, $W_2 = 1$ and $W_3 = W_4 = 1000$, $\alpha_f = 500$. Table 3.3 shows the tuning ranges and the results.

| | Input Range | Outcome |
|---|---|---|
| $K_{p,DAB}$ | $[2 \cdot 10^{-4}, 10]$ | 0.0376 |
| $K_{i,DAB}$ | [0.01, 10] | 0.3591 |

**Table 3.3:** Genetic Algorithm Control Tuning ($t = 3h$): Double-Star SST, Control System C

The found control system parameters are used with the PLECS Mathematical model. Figure 3.21 shows the SST behaviour with the found control system parameters.

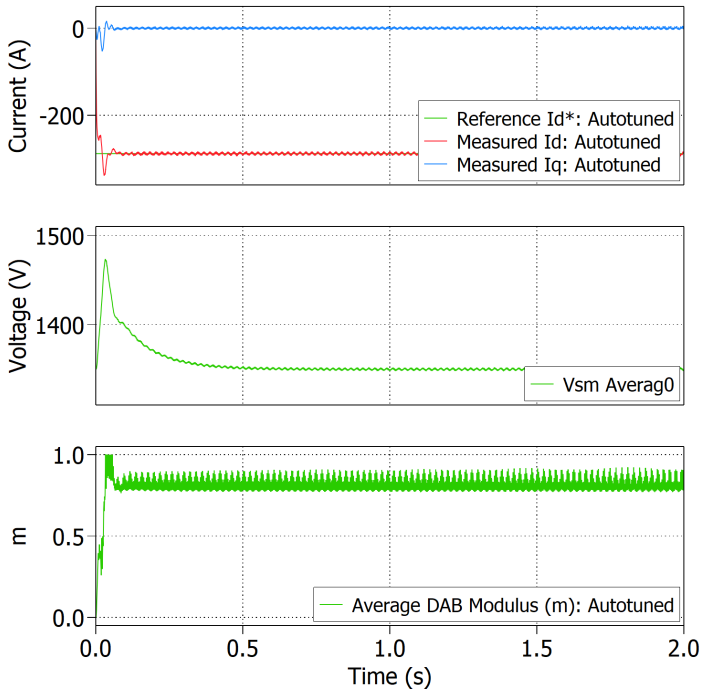



**Figure 3.21:** System response of control system C tuned using the Genetic Algorithm

### 3.6.8. Automated Tuning of Control System B using the Genetic Algorithm

Using the genetic algorithm to tune control system B on all five control parameters leads to a solution with all control parameters at the lower set boundaries. As both the voltage and DAB control gains are dependent upon each other for stability, the Genetic Algorithm is unable to find a fast-converging but stable solution. Alternatively, the DAB control gains found by tuning control system C can be used, such that only the voltage gains of control system B need to be tuned.

The Genetic Algorithm is run to tune control system B for 6 hours with $W_1 = 1$, $W_2 = 100$ and $W_3 = W_4 = 1000$, $\alpha_f = 500$, $K_{p,DAB} = 0.0376$ and $K_{i,DAB} = 0.3591$. Table 3.4 shows the tuning ranges and the results.

| | **Input Range** | **Outcome** |
|---|---|---|
| $\mathbf{K_{p,V}}$ | [0.001, 10] | 0.0840 |
| $\mathbf{K_{i,V}}$ | [0.01, 100] | 1.4225 |

**Table 3.4:** Genetic Algorithm Control Tuning ($t = 6h$): Double-Star SST, Control System B

The found control system parameters are used with the PLECS Mathematical model. Figure 3.22 shows the SST behaviour with the found control system parameters.

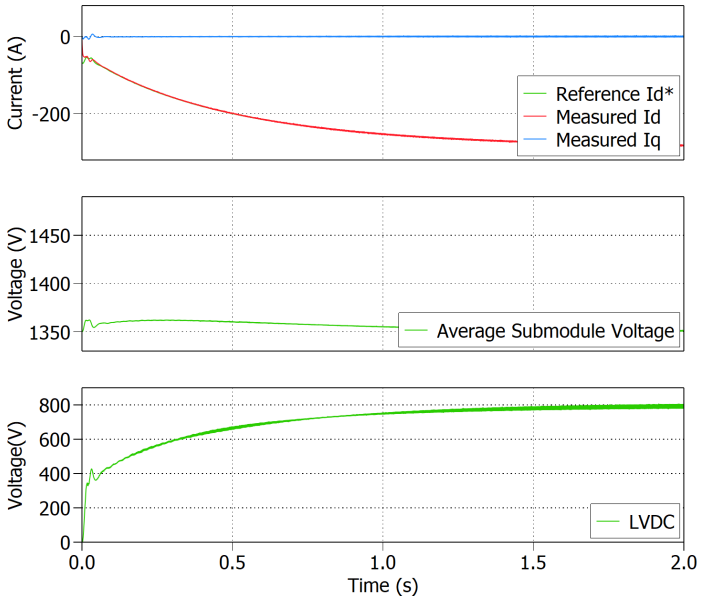



**Figure 3.22:** System response of control system B tuned using the Genetic Algorithm

# 4

# Simulation Results

## 4.1. Simulation Setup

All simulations are set up to be modular with the use of vectorised components, therefore the number of submodules ($N$) can be adjusted only with the initialisation commands. Other user defined parameters are the grid voltage ($\hat{v_g}$), the total apparent power ($S$), the MMC energy storage requirement ($\tau_{mmc} = E_{mmc}/P$ or $C_{SM}$) and the control parameters. Other parameters are equal for all simulations. Table 4.1 shows the generally defined parameters for all simulations, unless mentioned otherwise.

| Symbol | Parameter | Value |
|---|---|---|
| S | Total Apparent Power | 3.5 [MVA] |
| $\hat{v_g}$ | Grid Peak Voltage | 8.1 [kV] |
| $V_{LV}$ | LVDC bus voltage | 800 [V] |
| $R_{C,SM}$ | $C_{SM}$ ESR | 1 [mΩ] |
| $L_{arm}$ | Arm Inductance | 10 [mH] |
| $R_L$ | $L_{arm}$ ESR | 1 [mΩ] |
| $L_g$ | AC Grid Inductance | 0 [H] |
| $R_g$ | AC Grid Resistance | 0 [Ω] |
| $f_g$ | Grid Frequency | 50 [Hz] |
| $f_s$ | MMC Switching Frequency | 10 [kHz] |
| $f_{DAB}$ | DAB Switching Frequency | 20 [kHz] |
| $C_{DAB}$ | DAB Output Capacitance | 220 [µF] |
| $R_{C,DAB}$ | $C_{DAB}$ ESR | 10 [mΩ] |
| $K_{DAB}$ | DAB Oversizing Factor | 1.2 |
| $I_q^*$ | q-component reference current | 0 [A] |
| $I_{d,ss}^*$ | Steady-State d-component reference current | $\frac{-2S}{3\hat{v_g}}$ [A] |
| $I_{sat}$ | Reference Current Saturation | $\pm 1.1 I_{d,ref}$ [A] |
| $R_{lvdc}$ | LVDC Resistive Load | $\frac{S}{V_{LV}^2}$ [Ω] |
| $P_{DAB}$ | DAB Peak Power | $\frac{S}{\#SM_{tot}} K_{DAB}$ [W] |
| $L_{DAB}$ | DAB Inductance | $\frac{nV_{SM}V_{LV}}{8f_{DAB}P_{DAB}}$ [H] |
| $n$ | DAB Transformer Turn Ration | $\frac{V_{SM}}{V_{LV}}$ |

**Table 4.1:** Simulation Parameters of the simulations unless mentioned otherwise

The different topologies are compared in terms of Capacitance, Charge (Equation 4.1) and Energy (Equation 4.2) for a 10% submodule voltage ripple. Furthermore, $\tau_{mmc} = E/P$ is defined as the ratio between the stored energy in the MMC and the total power capacity. Considering the unit of $E/P$, this becomes seconds (s) according to Equation 4.3. Therefore this is a time constant ($\tau$).

$$Q_{mmc} = \#SM_{tot} \cdot C_{SM} \cdot V_{SM} \tag{4.1}$$

$$E_{mmc} = \#SM_{tot} \cdot C_{SM} \cdot V_{SM}^2 \tag{4.2}$$

$$\frac{E}{P} \propto \frac{[J]}{[W]} = \frac{[J]}{[J/s]} = [s] \tag{4.3}$$

Figure 4.1 shows the setup of the SST simulation in PLECS. This includes the MMC controller (A, B or C), a modulator set to a phase-shifted carrier, a DAB block and various measurements.

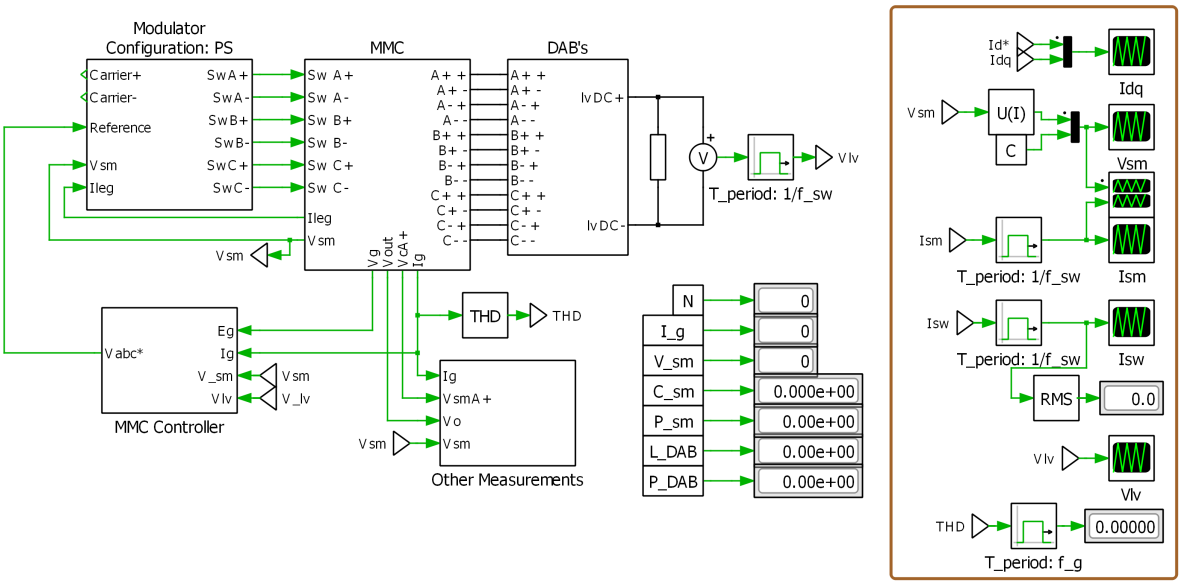



**Figure 4.1:** Overview of the simulation in PLECS

Figure 4.2 shows the Double-Star MMC block using N-sized vectorised half-bridges. The MMC is connected to the MV AC grid. Each vectorised submodule has its own output. Figure 4.3 shows the Single-Star MMC block using N-sized vectorised full-bridges. Figure 4.4 shows the Single-Delta MMC block using N-sized vectorised full-bridges.

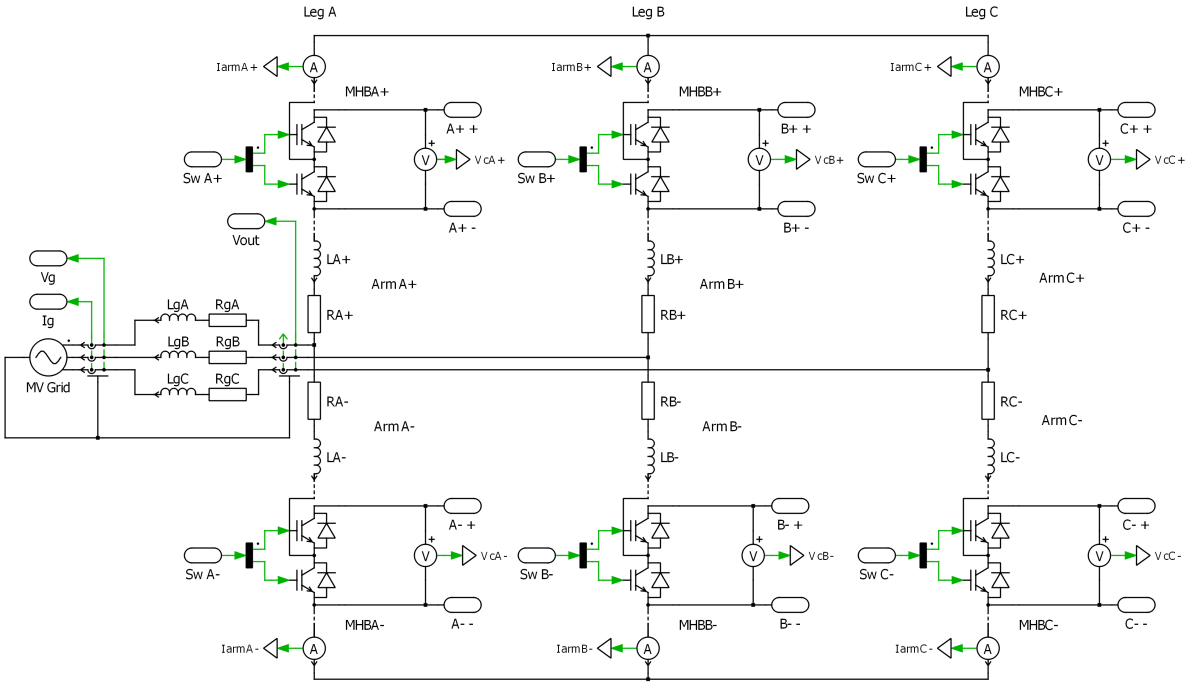



**Figure 4.2:** Overview of the Double-Star MMC in PLECS

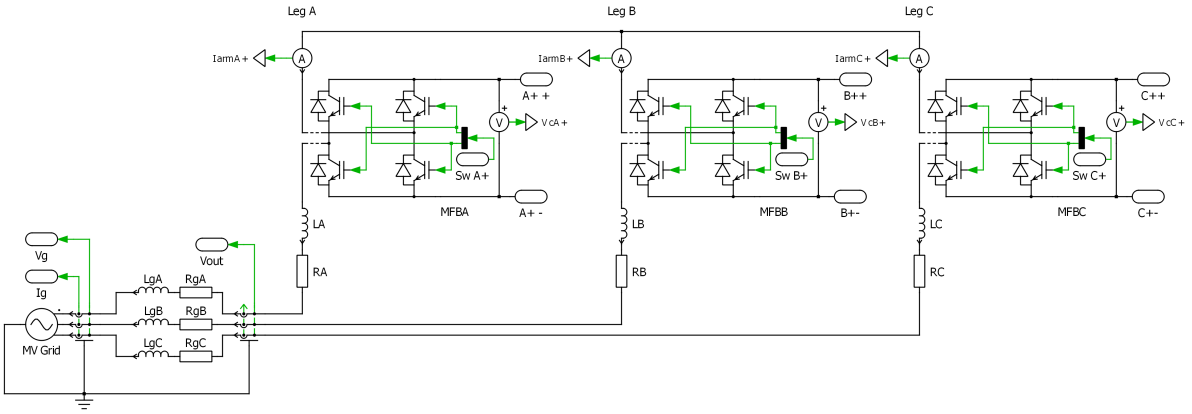



**Figure 4.3:** Overview of the Single-Star MMC in PLECS

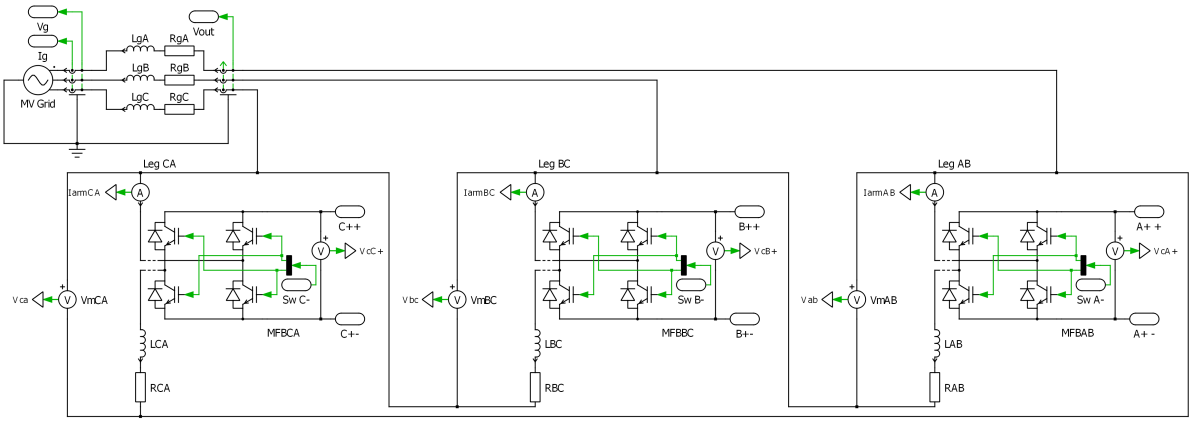



**Figure 4.4:** Overview of the Single-Delta MMC in PLECS

Figure 4.5 shows the DAB block using an N-sized vectorised DAB per MMC arm. The Single-Star and Single-Delta topologies only contain 3 N-sized DAB blocks. The DAB block contains the DAB controllers (A, B/C, B*/C*). The N outputs of each DAB are connected in parallel using a wire selector, which are in turn connected in parallel to each other forming a single LVDC-bus.

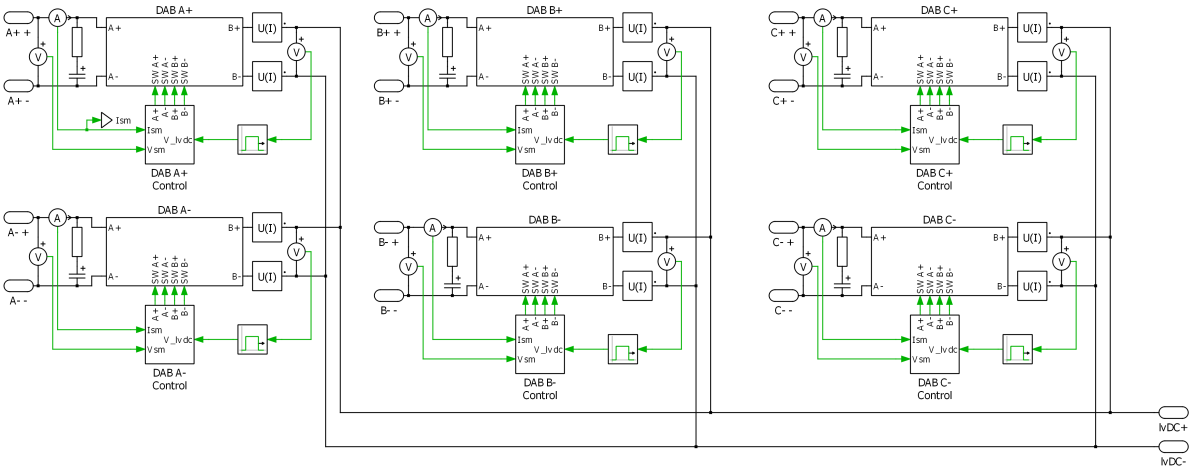



**Figure 4.5:** Overview of the DAB's Block in PLECS

## 4.2. 1MVA SST Topology Comparison

Initially, simulations of a smaller SST have been run to compare the topologies with a reduced simulation time. These simulations have been used to check the accuracy of the mathematical models. They can also be used to check the viability of design choices such as the use of an FB Double-Star topology, and whether to use half the submodule voltage or half the amount of submodules for the Single-Star topology. This has been done for a rating of 1MVA and an MVAC-grid of approximately 3.3kV ($\hat{v_g} = 2.7kV$), only considering control system A. Here, the three topologies are compared for stored charge and energy. Furthermore, the usage of Full-Bridge Submodules with a double-star SST is analysed. This includes half insertion (HI), where the upper arm only inserts positive voltages and vice-versa for the lower arm, and full insertion (FI), where both arms insert the full voltage range, resulting in the MVDC-link voltage becoming 0 (Equations 2.54 and 2.56).

Table 4.2 shows the used control system parameters and the parameters deviating from table 4.1 for all 1MVA SST simulations.

| Symbol | Parameter | Value |
|---|---|---|
| S | Total Appereant Power | 1 [MVA] |
| $\hat{v_g}$ | Grid Peak Voltage | 2.7 [kV] |
| $K_{p,I}$ | Current Control Proportional Gain | 2 |
| $K_{i,I}$ | Current Control Integral Gain | 200 |
| $K_{p,V}$ | Voltage Control Proportional Gain | 2 |
| $K_{i,V}$ | Voltage Control Integral Gain | 20 |
| $K_w$ | Voltage Control Anti-Windup Gain | 10 |
| $K_{p,DAB}$ | DAB Control Proportional Gain | $2 \cdot 10^{-5}$ |
| $K_{i,DAB}$ | DAB Control Integral Gain | 0.1 |
| $K_{p,DAB\Delta}$ | Single-Delta DAB Control Proportional Gain | $2 \cdot 10^{-5}/\sqrt{3}$ |
| $K_{i,DAB\Delta}$ | Single-Delta DAB Control Integral Gain | $0.1/\sqrt{3}$ |

**Table 4.2:** Simulation Parameters of the 1MVA Simulation Parameters

Table 4.3 shows the energy storage simulation results for various topologies. The plots of the submodule voltages and other signals of all the 1MVA Simulations can be found in appendix C

| | **DoubleStar** | | | **SingleStar** | | **SingleDelta** |
|---|---|---|---|---|---|---|
| | **HB** | **FB: HI** | **FB: FI** | **FB** | **FB** | **FB** |
| $V_{SM}$ | 1350 [V] | 1350 [V] | 675 [V] | 675 [V] | 1350 [V] | 1169 [V] |
| $C_{SM}$ (10%) | 2.00 [mF] | 2.00 [mF] | 1.56 [mF] | 3.11 [mF] | 1.56 [mF] | 1.25 [mF] |
| $N$ | 4 | 4 | 4 | 4 | 2 | 4 |
| $\#SM_{tot}$ | 24 | 24 | 24 | 12 | 6 | 12 |
| **$Q_{mmc}$** (10%) | **64.8 [C]** | **64.8 [C]** | **25.19 [C]** | **25.19 [C]** | **12.60 [C]** | **17.54 [C]** |
| **$E_{mmc}$** (10%) | **87.5 [kJ]** | **87.5 [kJ]** | **17.0 [kJ]** | **17.0 [kJ]** | **17.0 [kJ]** | **20.5 [kJ]** |
| $\tau_{mmc} = E/P$ | 87.5 [ms] | 87.5 [ms] | 17.0 [ms] | 17.0 [ms] | 17.0 [ms] | 20.5 [ms] |

**Table 4.3:** SST (1MVA): MMC Stored Charge and Energy Comparison

Table 4.3 shows that, in terms of total stored charge and energy, using full-bridge submodules with half insertion, is equivalent to using a half-bridge submodules. Furthermore, using full-bridge submodules with full insertion, is equivalent to using a single-star topology. Considering the submodule capacitance and amount of submodules, a double-star topology with fully inserted full-bridge submodules, is equivalent to running two single-star full-bridge topologies in parallel. Using half the amount of submodules with a double submodule voltage in the single-star topology, leads to the same amount of stored energy.

These topologies are compared for the stress on the switches as well. Ideally, the stress can be determined according to equation 4.5, using the submodule voltage and the RMS current through the upper switch. However, considering the cost of the switches, the switches can only be bought with certain voltage ratings, which determines the parameters and cost of the switch. Equation 4.6 shows the stress using this voltage.

$$N_{SW} = \#SW_{SM} \cdot \#SM_{tot} \tag{4.4}$$

$$Stress_{sw,1} = N_{SW} \cdot V_{SM} \cdot I_{SW,RMS} \tag{4.5}$$

$$Stress_{sw,2} = N_{SW} \cdot V_{SW,Chosen} \cdot I_{SW,RMS} \tag{4.6}$$

Table 4.4 shows the switch stress comparison between these simulations.

| | **DoubleStar** | | | **SingleStar** | | **SingleDelta** |
|---|---|---|---|---|---|---|
| | **HB** | **FB: HI** | **FB: FI** | **FB** | **FB** | **FB** |
| $V_{SM}$ | 1350 [V] | 1350 [V] | 675 [V] | 675 [V] | 1350 [V] | 1169 [V] |
| $I_{SM,RMS}$ | 71.1 [A] | 40.5 [A] | 62.1 [A] | 124 [A] | 125 [A] | 72.4 [A] |
| $\#SW_{SM}$ | 2 | 4 | 4 | 4 | 4 | 4 |
| $\#SM_{tot}$ | 24 | 24 | 24 | 12 | 6 | 12 |
| $V_{SW}$ | 1700 [V] | 1700 [V] | 1200 [V] | 1200 [V] | 1700 [V] | 1700 [V] |
| $\mathbf{N_{SW}V_{SM}I_{SM,RMS}}$ | **4.61 [MVA]** | **5.25 [MVA]** | **4.02 [MVA]** | **4.02 [MVA]** | **4.05 [MVA]** | **4.06 [MVA]** |
| $\mathbf{N_{SW}V_{SW}I_{SW,RMS}}$ | **5.80 [MVA]** | **6.61 [MVA]** | **7.15 [MVA]** | **7.14 [MVA]** | **5.10 [MVA]** | **5.91 [MVA]** |

**Table 4.4:** SST (1MVA): MMC Switch Stress Comparison

Table 4.4 shows that the ideal switch stress is equal for all topologies using a fully inserted full-bridge submodule. The ideal switch stress lies higher for the half-bridge double-star topology and the highest for the double-star full-bridge topology with half the inserted submodule voltage. Considering the chosen switch voltages, the stress of the double-star full-bridge and the single-star with $V_{SM} = 675V$ is the highest. Therefore, considering the switch stress, using half-bridge submodules for the double-star topology and using half the amount of submodules for the double-star topology, is the best choice.

Table 4.5 shows the summarised simulation results of the three to be further compared topologies.

| | **Double Star (HB)** | **Single Star (FB)** | **Single Delta (FB)** |
|---|---|---|---|
| **N** | 4 | 2 | 4 |
| $\mathbf{V_{SM}}$ | 1350 [V] | 1350 [V] | 1169 [V] |
| **Q** | 64.8 [C] | 12.91 [C] | 17.535 [C] |
| **E** | 87.5 [kJ] | 17.0 [kJ] | 20.5 [kJ] |
| $\tau_{mmc} = E/P$ | 87.5 [ms] | 17.0 [ms] | 20.5 [ms] |
| $\mathbf{N_{SW}V_{SW}I_{SW,RMS}}$ | 5.80 [MVA] | 5.10 [MVA] | 5.91 [MVA] |

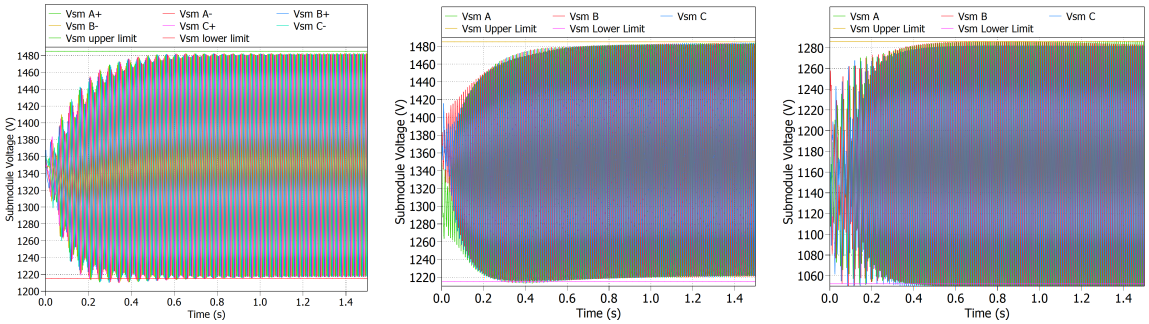
**Table 4.5:** SST (1MVA) Comparison

## 4.3. 3.5MVA SST Simulations with Control System A

The three topologies have been simulated using control system A. The control parameters are derived from the parameters found by the Genetic Algorithm, with manual tweaking in the mathematical model. Table 4.6 shows the control system parameters. Figure 4.6 shows the submodule voltages and their upper and lower limits, figure 4.7 shows the d- and q-component currents and the d-component reference current, figure 4.8 shows the currents through the upper switch of submodule A(+).

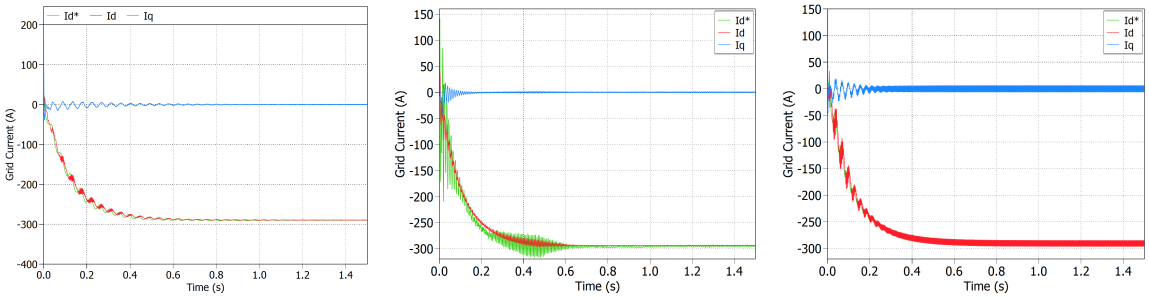
| | **Double-Star** | **Single-Star** | **Single-Delta** |
|---|---|---|---|
| $\alpha_f$ | 500 | 300 | 500 |
| $K_{p,V}$ | 15 | 10 | 1 |
| $K_{i,V}$ | 50 | 50 | 100 |
| $K_{p,DAB}$ | $8.2 \cdot 10^{-5}$ | $5 \cdot 10^{-5}$ | $2 \cdot 10^{-5}$ |
| $K_{i,DAB}$ | $9.4 \cdot 10^{-3}$ | 0.012 | 0.010 |

**Table 4.6:** Control system parameters



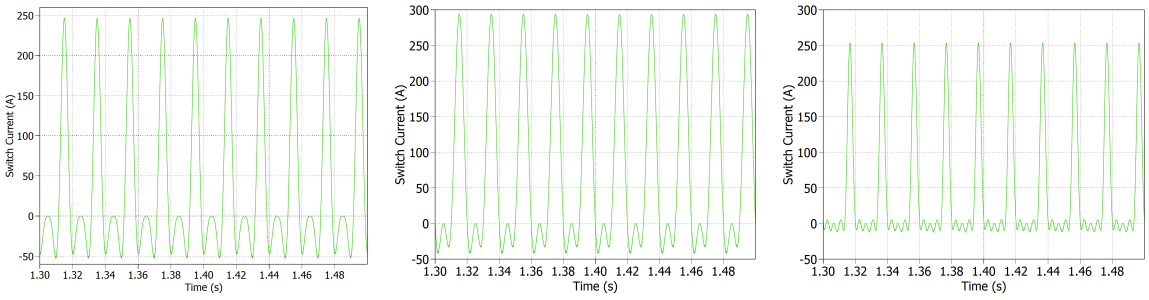

**(a)** Double-Star **(b)** Single-Star **(c)** Single-Delta

**Figure 4.6:** Comparison of $V_{SM}$ with control system A




**(a)** Double-Star **(b)** Single-Star **(c)** Single-Delta

**Figure 4.7:** Comparison of $I_q$, $I_d$ and $I_d^*$ with control system A




**(a)** Double-Star **(b)** Single-Star **(c)** Single-Delta

**Figure 4.8:** Comparison of $I_{sw}$ with control system A

Table 4.7 shows the summarised results and comparison of the simulation.

| | **Double-Star (N=12)** | **Single-Star (N=6)** | **Single-Delta (N=12)** |
|---|---|---|---|
| $\mathbf{C_{SM}}$ | 2.93 [mF] | 1.81 [mF] | 1.78 [mF] |
| $\mathbf{Q_{tot}}$ | 285 [C] | 44.1 [C] | 74.8 [C] |
| $\mathbf{E_{tot}}$ | 385 [kJ] | 59.51 [kJ] | 87.5 [kJ] |
| $\tau_{\mathbf{mmc}} = \mathbf{E}/\mathbf{P}$ | 110 [ms] | 17.0 [ms] | 25.0 [ms] |
| $\mathbf{N_{SW}V_{SM}I_{SW,RMS}}$ | 19.5 [MVA] | 13.4 [MVA] | 15.4 [MVA] |
| $\mathbf{N_{SW}V_{SW}I_{SW,RMS}}$ | 24.5 [MVA] | 16.8 [MVA] | 22.4 [MVA] |
| **THD** | 0.165% | 0.149% | 0.224% |

**Table 4.7:** Topology Comparison With Control System A

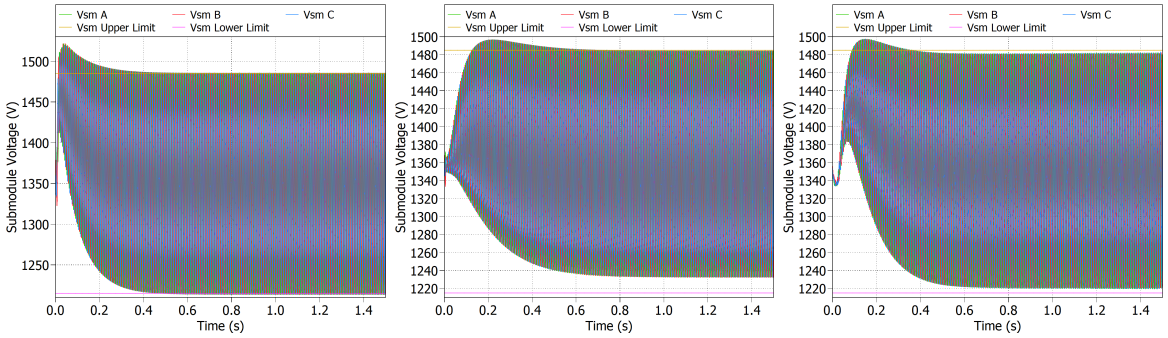
In terms of energy storage, the Single-Star Topology performs the best, followed by the Single-Delta topology and the Double-Star topology respectively. The energy storage requirement is approximately a factor of 6.5 larger for the Double-Star topology compared to the Single-Star topology, whereas the Single-Delta topology requires an approximate factor of 1.5 more energy storage. Furthermore, comparing this to the results of the 1MVA simulation, the energy storage to power ratio $\tau_{mmc}$ is consistent for the Single-Star topology. The increase for the Double-Star topology can be linked to the circulating current. As the current increases, so does the circulating current, causing the required capacitance to not rise linearly with the grid current. The increase for the Single-Delta topology can be linked to the current ripple of figure 4.7c, which in turn causes an increased THD as well. This current ripple will be on the submodule current as well and therefore cause an increased submodule voltage ripple.

In terms of switch stress, the Single-Star topology performs best, followed by the Single-Delta and the Double-Star topologies respectively. In terms of THD, the Single-Star topology performs best as well, followed by the Double-Star and the Single-Delta topologies respectively.

The increased THD of the Single-Delta topology is linked to the increased current ripple. As this ripple does not occur with the 1MVA simulations, it can be linked to the control system. The automated tuning using the Genetic Algorithm with various weights always leads to this ripple. Manually adjusting the control system parameter has not removed this ripple. Therefore, the used tuning methods or the control system itself is unsuitable to achieve the desired behaviour of the 3.5MVA Single-Delta Topology.

## 4.4. 3.5MVA SST Simulations with Control Systems B/B* and C/C*

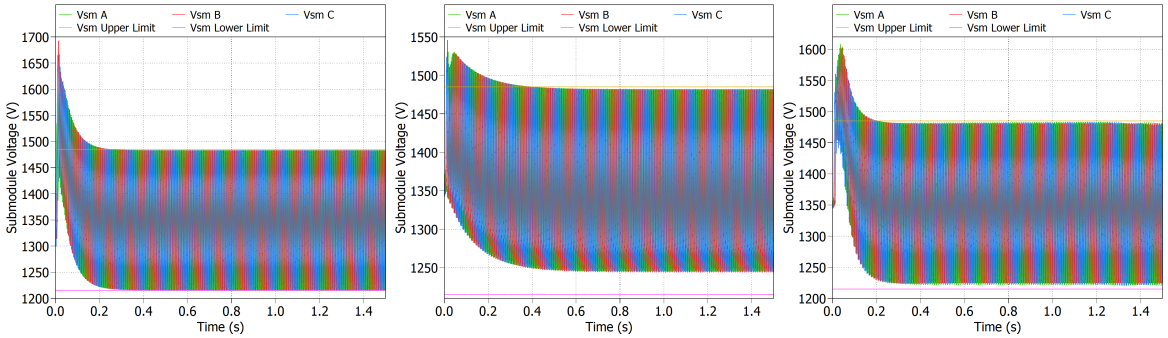
As table 4.7 has shown that the Single-Star topology performs best in terms of required energy storage and switch stress, only this topology is considered for the comparison of the control systems. Control systems B and C are compared on their ability to affect and/or reduce the submodule voltage ripple, resulting in a lower submodule capacitance which can be used. For all simulations, the submodule capacitance is tuned for a submodule voltage ripple of 10% with an accuracy of $\tau_{mmc} = 0.5ms$. A DAB power of 1.2 times the required power is used. For control systems B and C, two types of control are assumed. One with a 'slow' DAB operation and one with a 'fast' DAB operation with the control gains found by the Genetic Algorithm. Furthermore $\alpha_f = 500$, $K_{p,V} = 0.05$ and $K_{i,V} = 10$.




**(a) Control B:** $C_{SM} = 1.71mF$, $K_{p,DAB} = 0.002$, $K_{i,DAB} = 0.05$

**(b) Control B:** $C_{SM} = 1.55mF$, $K_{p,DAB} = 0.0376$, $K_{i,DAB} = 0.3591$

**(c) Control B*:** $C_{SM} = 1.39mF$, $K_{p,DAB} = 0.1$, $K_{i,DAB} = 5$



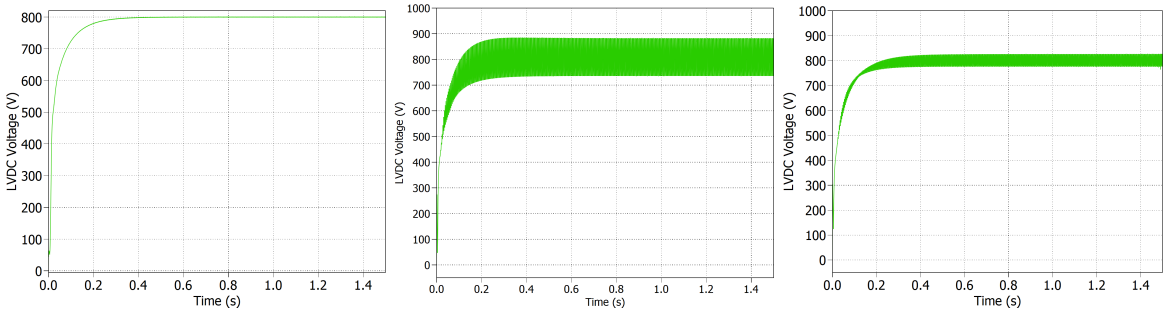

**(d) Control C:** $C_{SM} = 1.71mF$, $K_{p,DAB} = 0.002$, $K_{i,DAB} = 0.05$

**(e) Control C:** $C_{SM} = 1.49mF$, $K_{p,DAB} = 0.0376$, $K_{i,DAB} = 0.3591$

**(f) Control C*:** $C_{SM} = 1.28mF$, $K_{p,DAB} = 0.1$, $K_{i,DAB} = 5$

**Figure 4.9:** Comparison of the submodule Voltages with different control systems for the Single-Star SST

Figure 4.9 presents the effect of control systems B/B* and C/C* on the submodule voltage ripples. This shows a higher voltage overshoot for control systems C/C* than control system B. This can however be prevented (Figure 3.16d). Furthermore, the system generally converges faster with control systems C and C*, compared to B and B*. For these control systems, the fastest convergence happens for B and C with a slower DAB Control and the slowest for B and C with a faster DAB control.



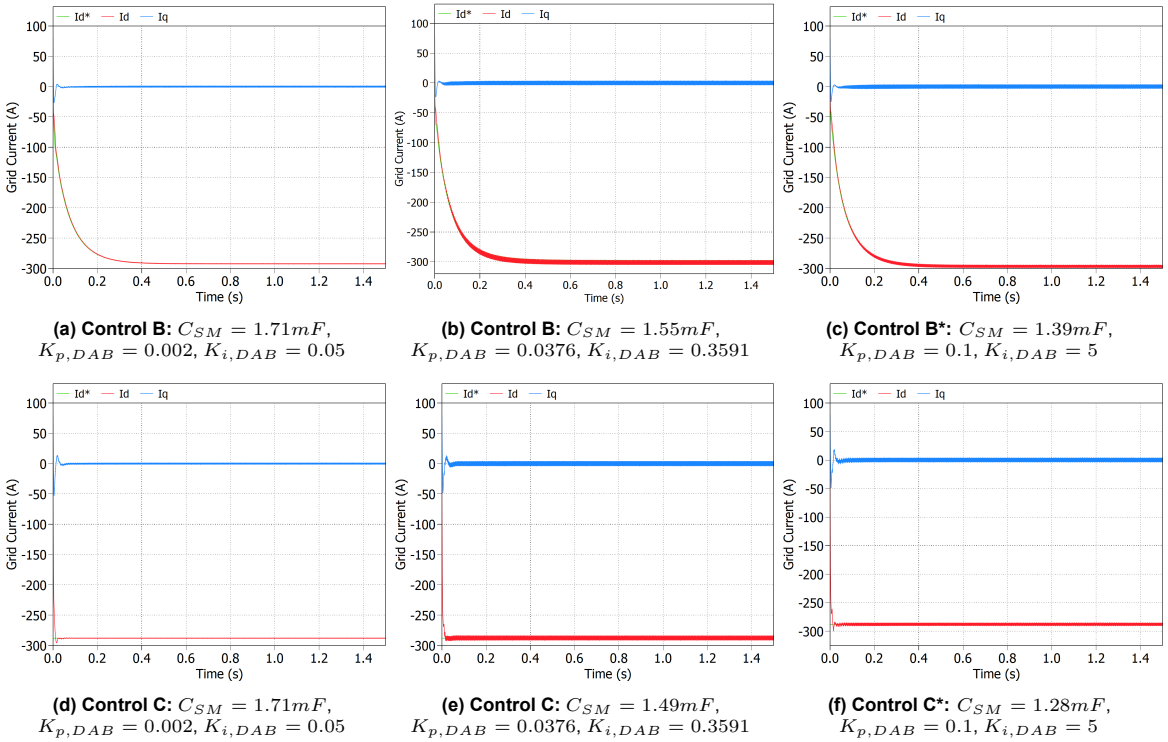

**(a) Control B:** $C_{SM} = 1.71mF$, $K_{p,DAB} = 0.002$, $K_{i,DAB} = 0.05$

**(b) Control B:** $C_{SM} = 1.55mF$, $K_{p,DAB} = 0.0376$, $K_{i,DAB} = 0.3591$

**(c) Control B*:** $C_{SM} = 1.39mF$, $K_{p,DAB} = 0.1$, $K_{i,DAB} = 5$

**Figure 4.10:** Comparison of $V_{LVDC}$ with different control systems for the Single-Star SST

Figure 4.9 presents the effect of control system B/B* on the LVDC bus voltage behaviour. Control systems C/C* are not included as the LVDC bus voltage here is inherently stable. This shows that by increasing the DAB control gains of control system B, a significant ripple occurs on the LVDC-bus which does not occur with the slower DAB control. The usage of control system B* results in a ripple an LVDC ripple as well; however, it is significantly smaller while allowing for a lower submodule capacitance and a faster convergence rate.




**(a) Control B:** $C_{SM} = 1.71mF$, $K_{p,DAB} = 0.002$, $K_{i,DAB} = 0.05$

**(b) Control B:** $C_{SM} = 1.55mF$, $K_{p,DAB} = 0.0376$, $K_{i,DAB} = 0.3591$

**(c) Control B*:** $C_{SM} = 1.39mF$, $K_{p,DAB} = 0.1$, $K_{i,DAB} = 5$

**(d) Control C:** $C_{SM} = 1.71mF$, $K_{p,DAB} = 0.002$, $K_{i,DAB} = 0.05$

**(e) Control C:** $C_{SM} = 1.49mF$, $K_{p,DAB} = 0.0376$, $K_{i,DAB} = 0.3591$

**(f) Control C*:** $C_{SM} = 1.28mF$, $K_{p,DAB} = 0.1$, $K_{i,DAB} = 5$

**Figure 4.11:** Comparison of $I_d^*$. $I_d$ and $I_q$ with different control systems for the Single-Star SST

Figure 4.9 presents the effect of control systems B/B* and C/C* on the grid's current behaviour. This shows that generally, the grid currents can converge vaster with control systems C and C*, compared to B and B*, as the reference d-component current is already set at $t = 0$. The reduction of the submodule ripples leads to a ripple on the d- and q-component currents, which is more significant with control system B than with control system B*.

Table 4.8 shows the summarised results of the control system effects on the Single-Star SST, including control system A.

| Control: | A | B 'slow' | B 'fast' | B* | C 'slow' | C 'fast' | C* |
|---|---|---|---|---|---|---|---|
| $C_{SM}$ | 1.81 [mF] | 1.71 [mF] | 1.55 [mF] | 1.39 [mF] | 1.71 [mF] | 1.49 [mF] | 1.25 [mF] |
| $\tau_{mmc}$ | 17.0 [ms] | 16.0 [ms] | 14.5 [ms] | 13.0 [ms] | 16.0 [ms] | 14.0 [ms] | 12.0 [ms] |
| $N_{SW}V_{SW}I_{SW,RMS}$ | 4.21 [MVA] | 4.16 [MVA] | 4.29 [MVA] | 4.55 [MVA] | 4.10 [MVA] | 4.10 [MVA] | 4.12 [MVA] |
| THD | 0.149% | 0.117% | 0.145% | 0.136% | 0.110% | 0.139% | 0.133% |

**Table 4.8:** Comparison of control systems for the 3.5MVA Single-Star SST

Control system C/C* performs the best in terms of required energy storage, THD, switch stress and convergence rate. Generally, with a desire to reduce the required energy storage, the improved DAB control system performs the best in terms of capacitance reduction, THD and convergence rate. It does lead to a higher switch stress.

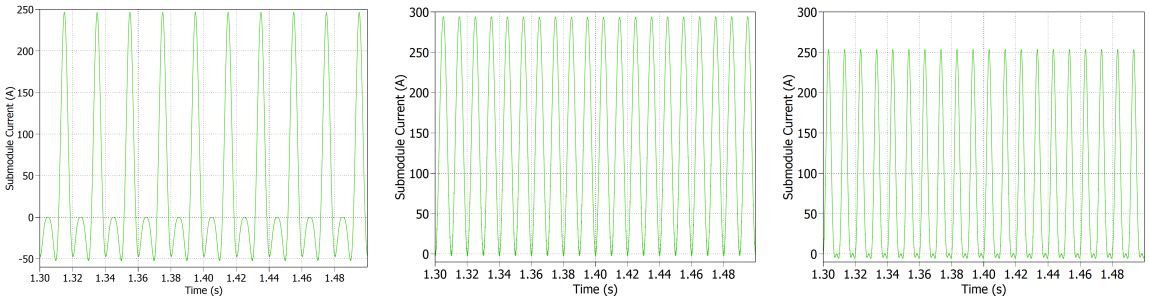
Compared to control system A, control systems B/B* and C/C* all offer a lower THD and energy storage requirement. Using control system B with a faster DAB control or B* results in a higher switch stress; otherwise, the switch stress is lower.

## 4.5. Submodule Voltage Ripple Analysis and DAB oversizing

To understand the required energy storage of the submodule and the effect of DAB upon this requirement, an analysis of the submodule voltages and currents is required.

### 4.5.1. Submodule Voltage Ripple Analysis

The submodule current directly determines the submodule voltage ripple if the DAB current is constant. Figure 4.12 shows the steady-state submodule currents of submodule A(+) of the three different topologies using control system A.




**(a)** Double-Star **(b)** Single-Star **(c)** Single-Delta

**Figure 4.12:** Comparison of $I_{sm}$ of arm A(+) in steady-state with control system A

The submodule current is determined by the product of the switching function of the submodule and the current of the arm of the submodule. As each topology has a different switching function and arm current, the submodule current will be different for each.

$$I_{SM,average} = \frac{P_{sst}}{\#SM_{tot} \cdot V_{SM}} \tag{4.7}$$

Table 4.9 shows the approximate peak-to-average submodule current ratios using control system A.

| | Double-Star | Single-Star | Single-Delta |
|---|---|---|---|
| $\frac{I_{SM,peak}}{I_{SM,average}}$ | $\frac{240}{36.0} = 6.7$ | $\frac{290}{144} = 2.0$ | $\frac{250}{83.2} = 3.0$ |

**Table 4.9:** Submodule current peak to average ratio with control system A

As the peak-to-average ratio is also dependent on the submodule voltage ripple itself, this measured ratio is not directly equal to the required DAB oversizing factor ($K_{DAB}$) which is required to fully remove the submodule voltage ripple.

Assume the simplified switching functions (Equations 2.19 and 2.20) to be true with m=1. This means there is no ripple on the submodule voltages and only a reference d-component voltage exists. This gives equation 4.8, which, in turn, leads to a submodule current according to equation 4.11.

$$v_{c,ideal}(t) = \frac{V_{DC}S'_p(t) + V_{DC}S'_n(t)}{2} = \frac{V_{DC}\left(\frac{1-\sin(\omega t)}{2}\right) + V_{DC}\left(\frac{1+\sin(\omega t)}{2}\right)}{2} = \frac{V_{DC}}{2} \tag{4.8}$$

$$i_{c,ideal}(t) = \frac{1}{sL_{arm} + R_{L,arm}}\left(\frac{V_{DC}}{2} - \left[v_{c,ideal}(t) = \frac{V_{DC}}{2}\right]\right) = 0 \tag{4.9}$$

$$i_{p,ideal}(t) = \frac{1}{2}i_g(t) \approx -144\sin(\omega t) \tag{4.10}$$

$$I_{SMp,ideal}(t) = S'_p(t)i_{p,ideal}(t) \approx -144\left(\frac{1-\sin(\omega t)}{2}\right)\sin(\omega t) = -72\sin(\omega t) + 72\sin^2(\omega t) \tag{4.11}$$

Equation 4.11 has a similar shape to the submodule current in figure 4.12a but with a different amplitude. The peak of equation 4.11 is 144A. Therefore, ideally, the peak to average submodule current ratio would be $\frac{144}{36} = 4$. This process can be repeated for the Single-Star and Single-Delta topologies, where there is inherently no circulating current. Table 4.10 shows this process repeated for all three topologies, where the Single-Star and Single-Delta topologies.

| | Double-Star | Single-Star | Single-Delta |
|---|---|---|---|
| $S'(t)$ | $\frac{1-\sin(\omega t)}{2}$ | $-\sin(\omega t)$ | $\sin\left(\omega t+\frac{\pi}{6}\right)$ |
| $i_{arm,ideal}(t)$ | $-144\sin(\omega t)$ | $-288\sin(\omega t)$ | $\frac{288}{\sqrt{3}}\sin\left(\omega t+\frac{\pi}{6}\right)$ |
| $I_{SM,ideal}(t)$ | $-72\sin(\omega t)+72\sin^2(\omega t)$ | $288\sin^2(\omega t)$ | $166\sin^2\left(\omega t+\frac{\pi}{6}\right)$ |
| $\frac{I_{SM,peak}}{I_{SM,average}}\Big\vert_{ideal}$ | $\frac{144}{36}=4$ | $\frac{288}{144}=2$ | $\frac{166}{83.2}=2$ |

**Table 4.10:** Ideal submodule currents and required DAB oversize factor for ripple removal

Using the ideal submodule current $I_{SM,ideal}(t)$, an equation for the ideal submodule voltage can be determined assuming no effect of the DAB on this submodule voltage ripple. As only the ripple is considered, only the AC components can be considered, therefore the average submodule current can be subtracted from the submodule current. Equation 4.12 shows the equation for this ripple voltage.

$$V_{SM,ripple}(t) = \frac{1}{C_{SM}}\int_0^t I_{SM,ideal}(t) - \left(\frac{1}{T}\int_0^T I_{SM,ideal}(t)dt\right)dt \tag{4.12}$$

Table 4.11 shows these voltage ripples for the three topologies and the required capacitance for a 10% ripple.

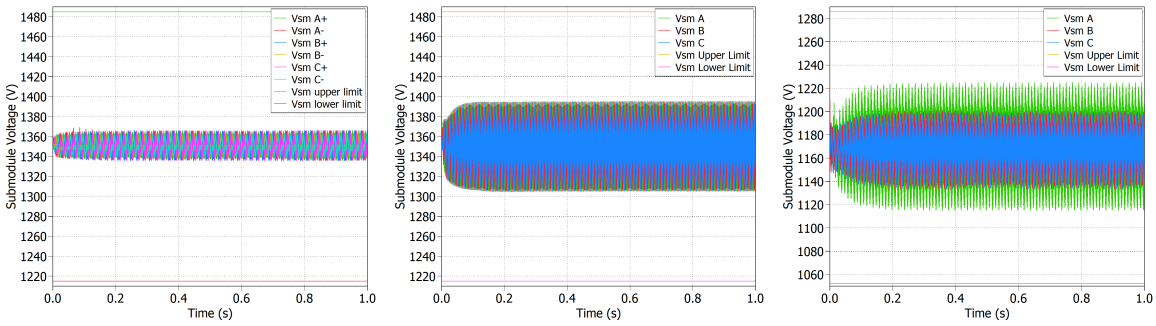
| | Double-Star | Single-Star | Single-Delta |
|---|---|---|---|
| $I_{SM,ideal}(t)$ | $-72\sin(\omega t)+72\sin^2(\omega t)$ | $288\sin^2(\omega t)$ | $166\sin^2\left(\omega t+\frac{\pi}{6}\right)$ |
| $V_{SM,ripple}(t)$ | $\frac{\hat{i_g}}{4\omega C_{SM}}(\cos(\omega t)-0.25\sin(2\omega t))$ | $\frac{-\hat{i_g}}{4\omega CSM}\sin(2\omega t)$ | $\frac{-\hat{i_g}}{4\sqrt{3}\omega C_{SM}}sin(2\omega t+\frac{\pi}{3})$ |
| $V_{SM,ripple,peak}$ | $\frac{1.1\hat{i_g}}{4\omega C_{SM}}=\frac{V^*_{SM}}{10}$ | $\frac{\hat{i_g}}{4\omega C_{SM}}=\frac{V^*_{SM}}{10}$ | $\frac{\hat{i_g}}{4\sqrt{3}\omega C_{SM}}=\frac{V^*_{SM}}{10}$ |
| $C_{SM,min}$ | 1.87 [mF] | 1.70 [mF] | 1.13 [mF] |
| $E_{MMC,min}$ | 245 [kJ] | 55.7 [kJ] | 55.7 [kJ] |

**Table 4.11:** Submodule voltages and required capacitance assuming ideal submodule currents and 10% ripple

The results of table 4.11 for the required capacitance are for a theoretical scenario which cannot occur as the ripples themselves affect the currents and will therefore increase the ripple. Furthermore effects such as switching noise, injected q-component currents and circulating currents can further increase the required submodule capacitance. Compared to the results of table 4.7, the energy storage requirement of the Single-Star topology has the most minor deviation. This concurs with the fact that the Single-Star submodule current (Figure 4.12b) lies the closest to the ideal submodule current. Furthermore, this shows that ideally, the Single-Star and Single-Delta configurations inherently have no difference in required energy storage. This is affected by the Single-Delta MMC's effect of the submodule voltage on the current, the Single-Delta MMC's q-component current, and the Single-Delta MMC's response to the control system.

### 4.5.2. Effect of DAB Oversizing

Table 4.10 shows the ideal peak-to-average submodule current ratio. When the submodule voltage ripple is completely removed, this becomes ideal and effects of the submodule voltage ripple and circulating current should no longer be present. Therefore, when removing the submodule voltage ripple, an oversizing factor $K_{DAB}$ of the ideal peak-to-average submodule current ratio should suffice. To account for q-component currents and switching noise, a margin of 5% is used on these ratios. This is simulated with an energy storage reduction of 80% compared to the ideal minimum required capacitance (Table 4.11). Figure 4.13 shows the submodule voltages while using control system C*, $K_{DAB} = 1.05 \left.\frac{I_{SM,peak}}{I_{SM,average}}\right|_{ideal}$ and a 80% reduction of energy storage compared to the theoretical minimum. This confirms the assumption that the peak-to-average ratios of table 4.9 are not required for $K_{DAB}$, the requirement lies closer to the ideal ratios of table 4.10.




**(a)** Double-Star with $K_{DAB} = 4.2$ and $C_{SM} = 0.37mF$

**(b)** Single-Star with $K_{DAB} = 2.1$ and $C_{SM} = 0.34mF$

**(c)** Single-Delta with $K_{DAB} = 2.1$ and $C_{SM} = 0.23mF$

**Figure 4.13:** Submodule Voltages using Control System C* and 80% Reduced Submodule Capacitance compared to Theoretical Minimum Requirement

With the Double-Star topology, the voltage ripple is approximately half that of the Full-Bridge-based topologies. The voltage ripple is now mostly dependent on the switching noise and less on the submodule current. Therefore, the energy storage advantage of the Full-Bridge is no longer valid. The Double-Star topology still requires double the total DAB peak power compared to the other topologies. For the Single-Delta topology, it is clear that phase A has a higher voltage ripple than the other phases which is linked to the same issues which caused the higher THD and voltage ripples with Control System A.

Table 4.12 shows the switch stress and THD. Comparing this to all other control systems shows a reduction of both switch stress and THD for all three topologies. This can be linked to the reduced submodule voltage ripple which realises a closer to ideal behaviour.

| | **Double-Star (N=12)** | **Single-Star (N=6)** | **Delta (N=12)** |
|---|---|---|---|
| $\mathbf{N_{SW}V_{SM}I_{SW,RMS}}$ | 14.0 [MVA] | 13.1 [MVA] | 11.9 [MVA] |
| $\mathbf{N_{SW}V_{SW}I_{SW,RMS}}$ | 17.7 [MVA] | 16.5 [MVA] | 17.4 [MVA] |
| **THD** | 0.102% | 0.101% | 0.103% |

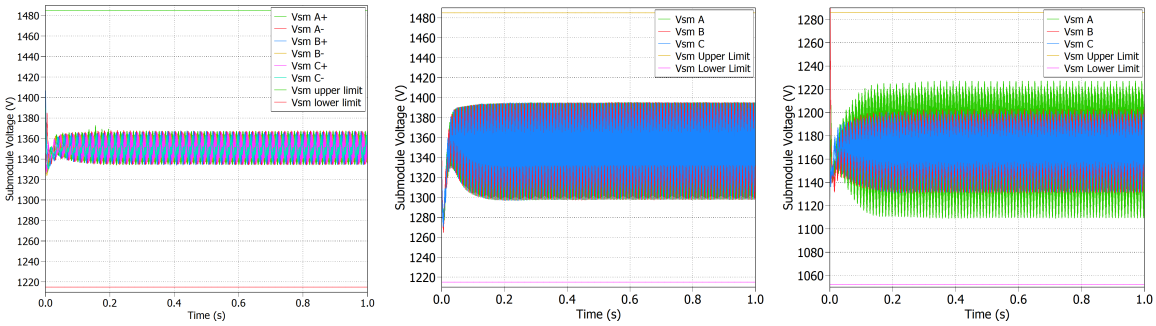
**Table 4.12:** Topology Comparison With Control System C*

Table 4.13 shows the comparison of the Double-Star circulating Current as the RMS value. This shows that by reducing the voltage ripple, the behaviour is closer to ideal and therefore the circulating current is significantly reduced.

| | **Control System A** | **Control System C* with $K_{DAB} = 4.2$** |
|---|---|---|
| $\mathbf{I_{c,RMS}}$ | 70.2 [A] | 11.7 [A] |

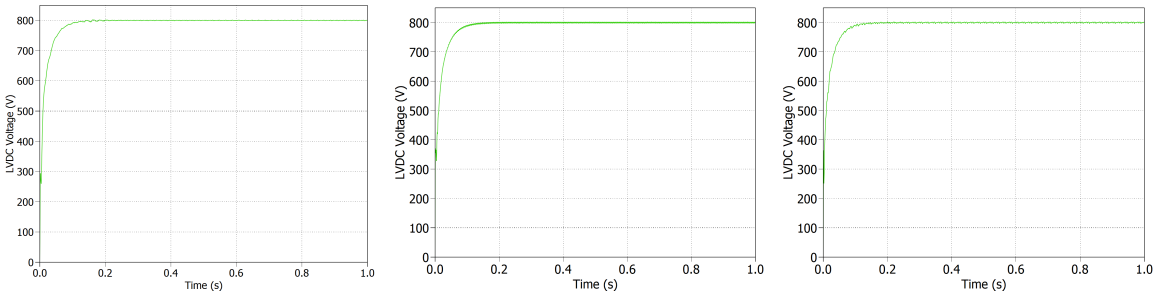
**Table 4.13:** Comparison of the Double-Star Circulating Currents between Control A and C+

The oversizing of the DAB can be applied to control system B* as well. Figure 4.14 shows the submodule voltages using control system B*, $K_{DAB} = 1.05 \left.\frac{I_{SM,peak}}{I_{SM,average}}\right|_{ideal}$ and an 80% reduction of energy storage compared to the ideal minimum requirement.




**(a)** Double-Star with $K_{DAB} = 4.2$ **(b)** Single-Star with $K_{DAB} = 2.1$ **(c)** Single-Delta with $K_{DAB} = 2.1$

**Figure 4.14:** Submodule Voltages using Control System B* and 80% Reduced Submodule Capacitance compared to Theoretical Minimum Requirement




**(a)** Double-Star with $K_{DAB} = 4.2$ **(b)** Single-Star with $K_{DAB} = 2.1$ **(c)** Single-Delta with $K_{DAB} = 2.1$

**Figure 4.15:** LVDC bus voltage using Control System B* and 80% Reduced Submodule Capacitance compared to Theoretical Minimum Requirement

Figure 4.15 shows the LVDC bus voltage using control system B*. Comparing this to the results of figure 4.10c, the ripple on the LVDC bus voltage is now gone. As the DAB no longer goes into saturation, the DAB currents now approximately equal the ideal submodule currents of table 4.10. As these are purely sinusoidal or squared sinusoidal, the AC components of the three 120°phases will cancel each other out. The average current of the three phases will therefore be purely DC.

Table 4.14 shows the switch stress and THD using control system B* with full submodule ripple reduction.

| | **Double-Star (N=12)** | **Single-Star (N=6)** | **Delta (N=12)** |
|---|---|---|---|
| $\mathbf{N_{SW}V_{SM}I_{SW,RMS}}$ | 13.9 [MVA] | 13.2 [MVA] | 12.4 [MVA] |
| $\mathbf{N_{SW}V_{SW}I_{SW,RMS}}$ | 17.7 [MVA] | 16.5 [MVA] | 17.4 [MVA] |
| **THD** | 0.109% | 0.108% | 0.110% |

**Table 4.14:** Topology Comparison With Control System B*

# 5

# Hardware DAB Test Setup: The dynamic response of a DAB

## 5.1. The Test Setup

The improved DAB control system works well in simulation; however, in simulation, an ideal model is used, which neglects effects such as measurement errors but also non-ideal DAB and magnetic characteristics. These include but are not limited to dead time, both temperature and frequency-dependent resistance and inductance, and conductive, switching and magnetic losses. For most of the SST behaviour analysis, such effects can be neglected. As the improved DAB control system is based on the current feedforward into an inverse model of an ideal DAB, it is important to verify the accuracy of this model and the control system's performance in a real setting.

A total of three tests are performed, of which the first two are model verification:

- **Phase Shift Current Measurement:** The input phase $\phi$ is swept, and the measured DC currents are compared to the calculated current.
- **Set Current Measurement:** A reference DC and AC current is given to the inverse DAB model and compared to the output current.
- **Current Step Test:** The DAB is now operating with a closed loop, a current step is given to the primary side, and the response is compared between a PI control and a combined PI, Current Feedforward with the inverse DAB model (Improved DAB Control System).

A Dual Active Bridge is used, which is controlled through a Delfino TMS320F28379D Control Card from the Texas Instruments C2000 microcontroller (MCU) family [55]. The programming is done through the Matlab Simulink C2000 Microcontroller Blockset [56]. A dashboard is set up in Matlab Simulink with various configuration parameters for the DAB. Figure 5.1 shows the lab setup.

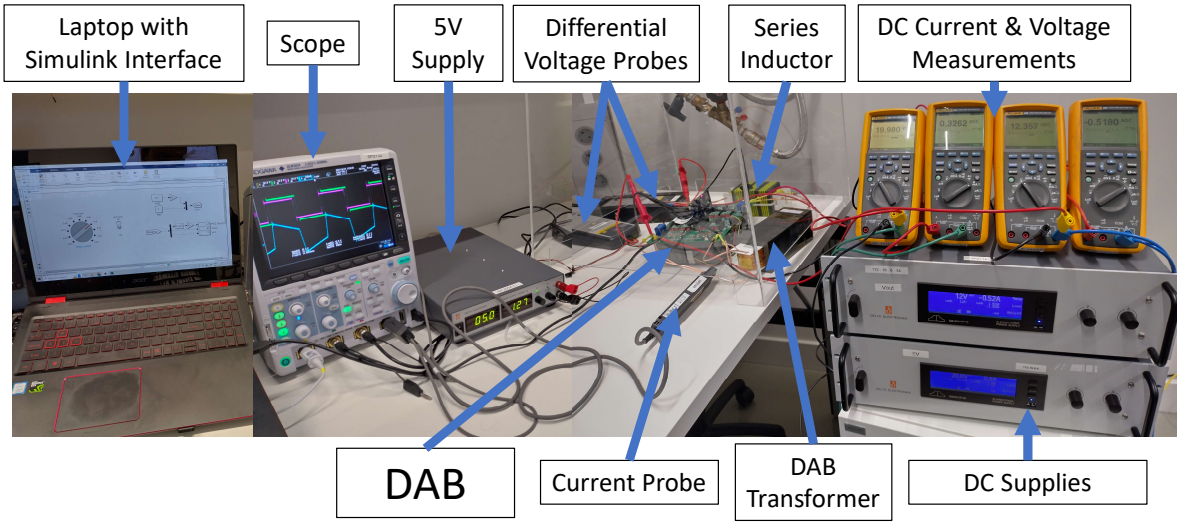



**Figure 5.1:** Lab Setup for the DAB test

Table 5.1 shows the used equipment in the measurements

| | |
|---|---|
| Bidirectional DC Voltage Source | Delta SM1500-cp-30 |
| | Delta SM500-cp-90 |
| Unidirectional DC Current Source | Agilent Technologies N5772A |
| 5V MCU & Electronics Power Supply | Delta es 030-10 |
| Current & Voltage DC Multimeter | Fluke 289 True RMS Multimeter |
| Oscilloscope | Yokogawa DLM3034 |
| Differential Voltage Probe | Yokogawa 700924 |
| | Keysight Technologies N32791A |
| Current Probe | Keysight Technologies N2782B |
| LCR Meter | Hameg Instruments HM8018 |

**Table 5.1:** Used Equipment in the DAB Test

### 5.1.1. DAB Parameters

For the parameters of the Dual Active Bridge and its magnetic components, the equivalent series inductance needs to be determined. The accuracy of this is important as the closed loop feedforward control is based upon knowing this parameter. This is done using the Hameg Instruments HM8018 LCR meter. The series inductor is connected in series with the primary side of the transformer. The secondary side of the transformer is shorted. After calibration, a twister wire pair of the RLC meter is connected to the inductor and transformer. Figure 5.2 shows the measurement setup.

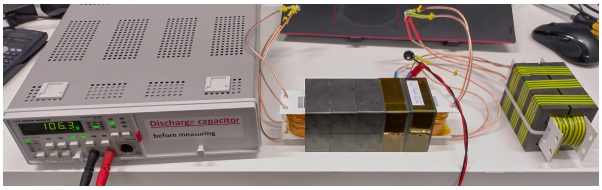



**Figure 5.2:** Inductor Parameter Measurement

The series inductance and resistance are measured for various frequencies. Table 5.2 shows the inductance measurements.

| $f_{mes}$ | $L_s$ | $R_s$ |
|---|---|---|
| 100 [Hz] | 112.0 [µH] | 0.182 [Ω] |
| 1 [kHz] | 106.3 [µH] | 0.079 [Ω] |
| 10 [kHz] | 106.3 [µH] | 0.183 [Ω] |
| 25 [kHz] | 106.3 [µH] | 0.228 [Ω] |

**Table 5.2:** DAB Inductor and Transformer Measurement

Table 5.3 shows the resulting parameters, including the chosen equivalent series inductance and resistance.

| Parameter | Symbol | Value |
|---|---|---|
| Equivalent Series Inductance | $L_s$ | 106.3 [µH] |
| Equivalent Series Resistance | $R_s$ | 0.183 [Ω] |
| Transformer Turn Ratio | n | 16:10 = 1.6 |
| Magnetisation Inductance | $L_m$ | 1.05 [mH] |
| DC-Link Capacitance | $C_{DC}$ | 63 [µF] |
| Switching Frequency | $f_{sw}$ | 50 [kHz] |
| Set Dead Time | $t_{dt}$ | 120 [ns] |
| MCU ADC Sampling Frequency | $f_{ADC}$ | 25 [kHz] |

**Table 5.3:** DAB Parameters of the Hardware Test

### 5.1.2. MCU PWM Setup

Table 5.4 shows the MCU PWM setup. For ePWM1A and ePWM2A, the counter first counts up until PRD=1000 is reached, when the counter equals CAU (WA1 or WA2), the output gets set high. After this, the counter counts back down to zero, where the output gets set low at CBD (WB1 or WB2). ePWM1B and ePWM2B are the inverted of this with an implemented dead-time of 120ns. The ePWM3 and ePWM4 blocks clear when counting up and set when counting down. With the PWM parameters set according to table 5.4, this ensured the implementation of a PWM output of 50kHz, a duty cycle of 50%, the two half-bridges on each side switching inverted, and the phase shift $\phi_2$ between the primary and secondary side.

| | |
|---|---|
| Counting Mode: | Up-Down |
| Timer Period (PRD): | 1000 Clock cycles |
| Action when counter = ZERO: | Do nothing |
| Action when counter = PRD: | Do nothing |
| Action when counter = CAU: | Set (1,2); Clear (3,4) |
| Action when counter = CAD; | Do nothing |
| Action when counter = CBU: | Do nothing |
| Action when counter = CBD: | Clear (1,2); Set (3,4) |
| Deadband polarity: | Active high complementary |
| Deadband period: | 120 [ns] |
| WA1: | $D \cdot PRD + 2\phi_1 \cdot PRD$ |
| WB1: | $D \cdot PRD - 2\phi_1 \cdot PRD$ |
| WA2: | $D \cdot PRD + 2\phi_2 \cdot PRD$ |
| WB2: | $D \cdot PRD - 2\phi_2 \cdot PRD$ |
| D: | 0.5 |
| $\phi_1$: | 0 |
| $\phi_2$: | variable |
| $(2\phi \cdot PRD)$ Saturation Limit: | $\pm 499$ |

**Table 5.4:** Simulink C2000 PWM setup

The phase shift $\phi \cdot PRD$ in clock cycles is limited to $\pm 499$ to ensure that the counter compare values do not equal zero or the period. This keeps the phase shift within the limits: $-0.2495 \leq \phi \leq 0.2495$

## 5.2. Model Verification using the Phase-Sweep Test

Figure 5.3 shows the hardware setup for the phase-sweep test. A bidirectional DC supply is connected to each side of the DAB, multimeters are used to measure the DC voltages and currents on each side.

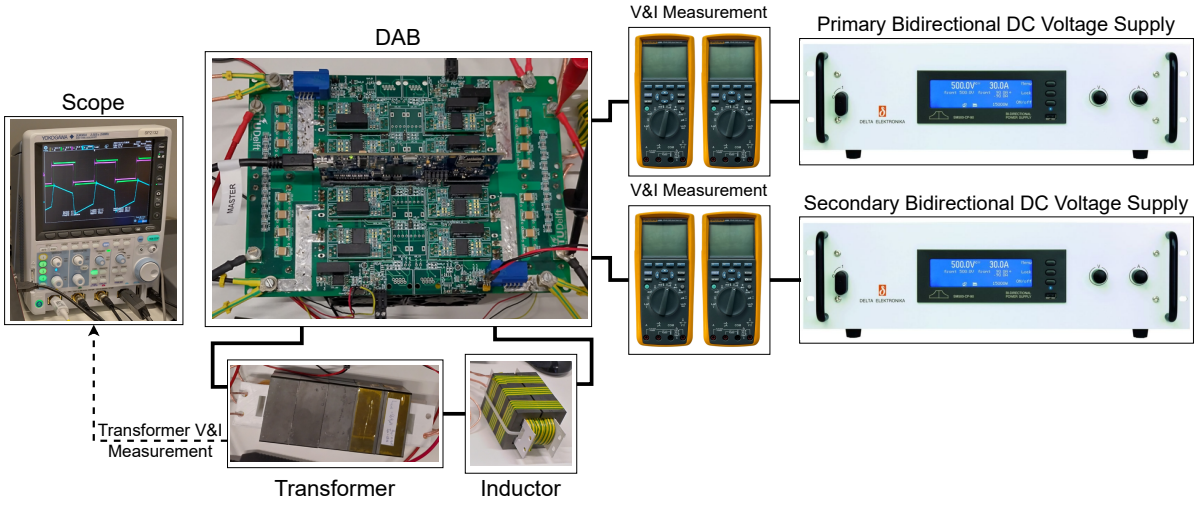



**Figure 5.3:** Test Setup for the Phase-Sweep and Current Reference Test

Figure 5.4 shows the dashboard of the measurement. It displays the angle $\phi$ and both DC voltages as measured by the ADC. The interface contains an on switch and a know to set the phase shift in steps of 0.05. Figure 5.5 shows the C2000 setup in Simulink. The PWM is set up according to table 5.4.

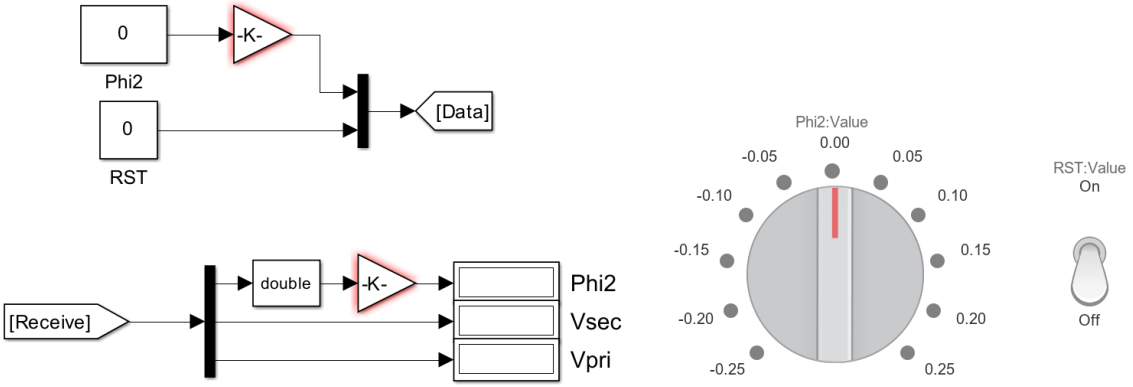



**Figure 5.4:** Dashboard for the DAB Phase-Sweep Test

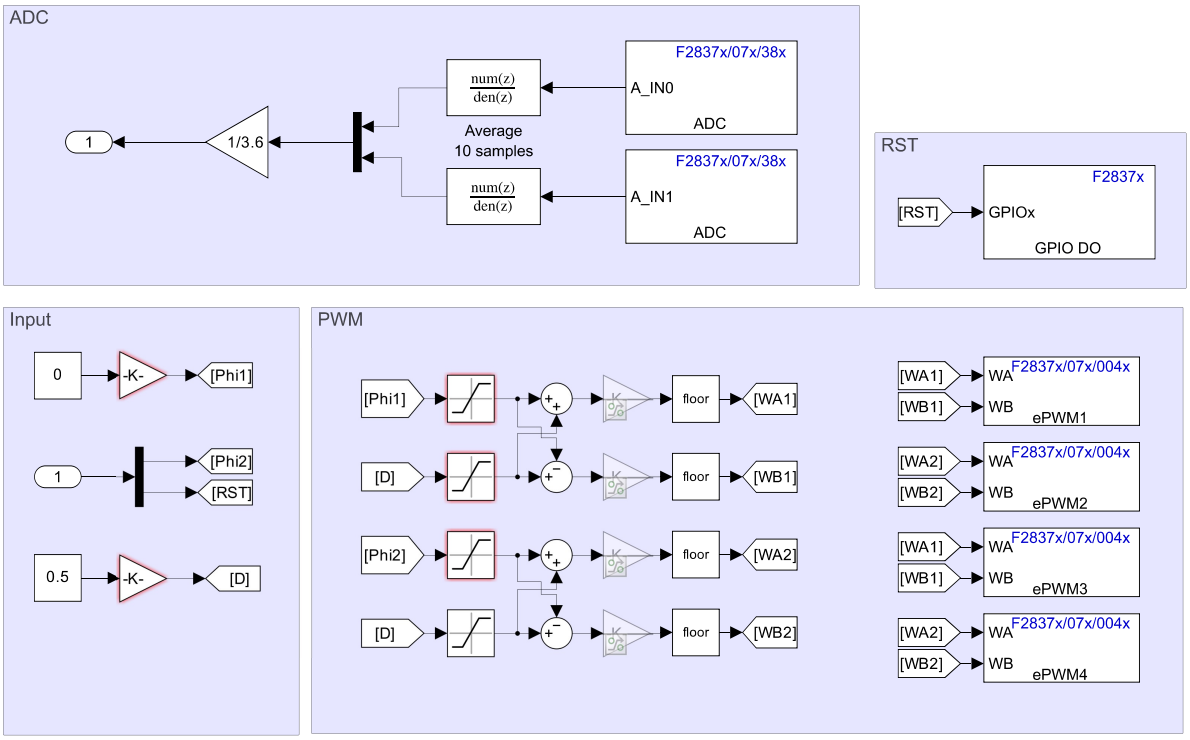



**Figure 5.5:** C2000 Simulink Setup for the DAB Phase-Sweep Test

### 5.2.1. Phase Sweep Test Results

The test has been done using two different voltages. Tables 5.5 and 5.6 show the test results. The test of table 5.6 uses a limited phase range as the maximum multimeter current is 10A. The predicted current follows the measured current. Considering the results of table 5.5, the largest absolute error occurs at the most negative currents. This error is mostly dependent upon the neglection of the series resistance, which causes a voltage drop relative to the current, affecting the voltage across the transformer and series inductance.

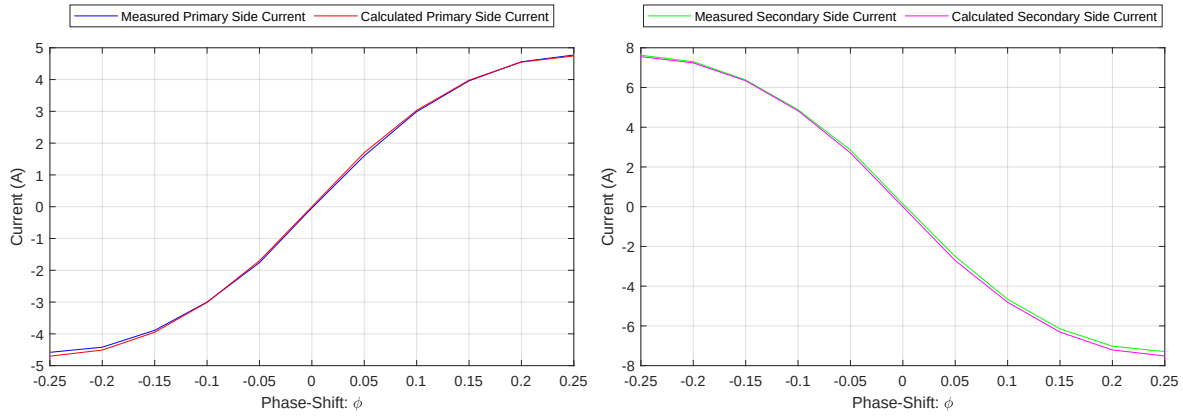
| $\phi$ | **Measured $V_{DC,pri}$** | **Measured $I_{DC,pri}$** | **Calculated $I_{DC,pri}$** | **Measured $V_{DC,pri}$** | **Measured $I_{DC,pri}$** | **Calculated $I_{DC,pri}$** |
|---|---|---|---|---|---|---|
| -0.25 | 200.54 | -4.58 | -4.70 | 124.84 | 7.62 | 7.55 |
| -0.20 | 200.52 | -4.42 | -4.51 | 124.88 | 7.30 | 7.24 |
| -0.15 | 200.47 | -3.89 | -3.95 | 124.95 | 6.38 | 6.34 |
| -0.10 | 200.37 | -3.00 | -3.01 | 125.07 | 4.88 | 4.83 |
| -0.05 | 200.25 | -1.76 | -1.70 | 125.23 | 2.85 | 2.71 |
| 0.00 | 200.07 | -0.04 | 0.00 | 125.45 | 0.14 | 0.00 |
| 0.05 | 199.90 | 1.60 | 1.70 | 125.66 | -2.51 | -2.71 |
| 0.10 | 199.75 | 2.99 | 3.03 | 125.83 | -4.66 | -4.81 |
| 0.15 | 199.65 | 3.96 | 3.98 | 125.96 | -6.15 | -6.31 |
| 0.20 | 199.59 | 4.56 | 4.55 | 126.01 | -7.02 | -7.21 |
| 0.25 | 199.56 | 4.77 | 4.74 | 126.04 | -7.29 | -7.51 |

**Table 5.5:** Phi-Sweep Test Results with $V_{DC,pri} \approx 200V$ and $V_{DC,sec} \approx 125V$

| $\phi$ | **Measured $V_{DC,pri}$** | **Measured $I_{DC,pri}$** | **Calculated $I_{DC,pri}$** | **Measured $V_{DC,pri}$** | **Measured $I_{DC,pri}$** | **Calculated $I_{DC,pri}$** |
|---|---|---|---|---|---|---|
| -0.10 | 400.72 | -5.962 | -6.01 | 249.72 | 9.729 | 9.65 |
| -0.05 | 400.46 | -3.739 | -3.39 | 250.06 | 5.645 | 5.42 |
| 0.00 | 400.11 | -0.143 | 0.00 | 250.48 | 0.345 | 0.00 |
| 0.05 | 399.77 | 2.216 | 3.40 | 250.91 | -5.048 | -5.42 |
| 0.10 | 399.47 | 5.970 | 6.05 | 251.25 | -9.335 | -9.62 |

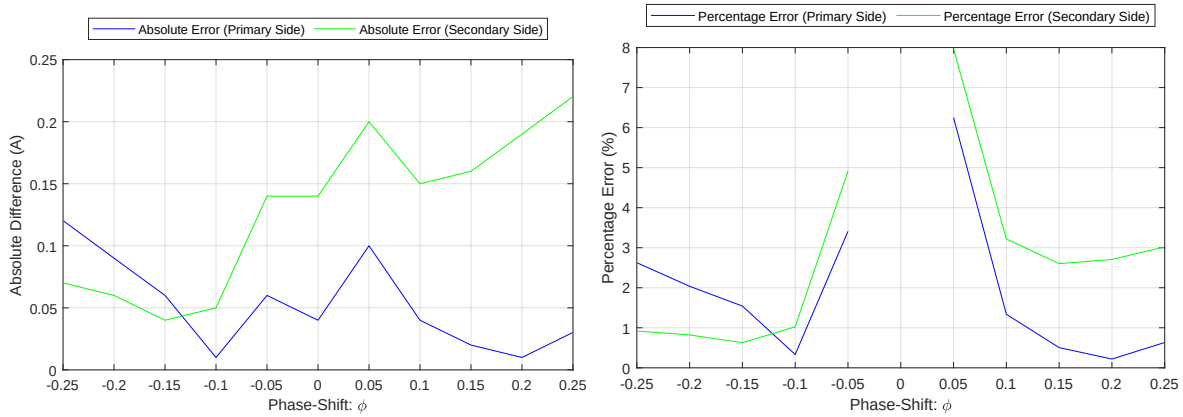
**Table 5.6:** Phi-Sweep Test Results with $V_{DC,pri} \approx 400V$ and $V_{DC,sec} \approx 250V$

Figure 5.6 shows the plotted measured and calculated DC currents for the shifted phase at $V_{DC,pri} \approx 200V$. The calculated current follows the measured current. Figure 5.7 shows the absolute ($e_{abs} = |I_{mes} - I_{calc}|$) and percental ($e_{prc} = e_{abs}/|I_{mes}|$) error over the phase shift. This shows that the absolute error is the largest for negative currents. The percental error increases with the phase shift approaching 0. For $\phi \geq 0.15$ the error stays below 1% for positive currents and below 3% for negative currents. The maximum absolute error is 0.12A for the primary side DC current and 0.22A for the secondary side DC current.




**(a)** Primary DC Side **(b)** Secondary DC Side

**Figure 5.6:** Measured and Calculated DAB DC Currents of the Phase-Sweep Test




**(a)** Absolute Error **(b)** Percental Error

**Figure 5.7:** Error between measured and calculated DC currents of the Phase-Sweep Test

## 5.3. Model Verification with Current Reference Sweep

The second model verification test uses the inverted DAB model generating the phase shift $\phi$ from a user-defined reference current. The hardware setup is the same as with figure 5.1. Figure 5.8 shows the Simulink Dashboard, showing the set reference current and the primary and secondary side DC voltages as measured by the MCU's ADCs. Instead of a phase shift, a current reference can now be chosen. Figure 5.9 shows the Simulink C2000 setup for the test. The phase shift $\phi$ is calculated using the inverse model containing the secondary side DC voltage as measured by the MCU ADC.

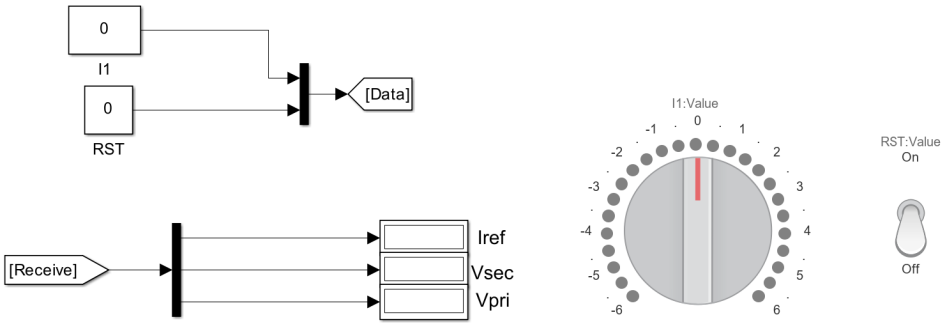



**Figure 5.8:** Dashboard for the DAB Current Reference Test

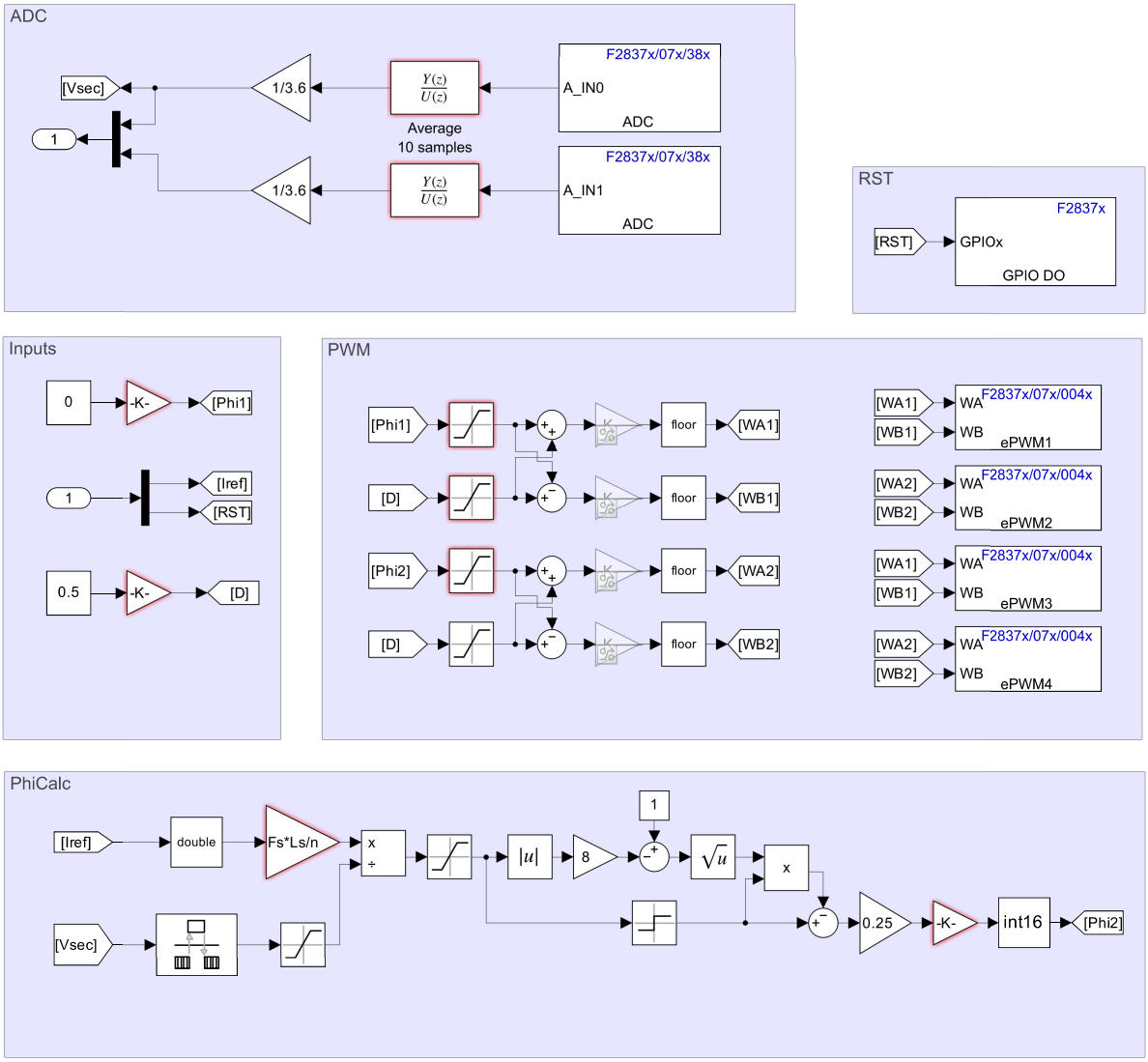


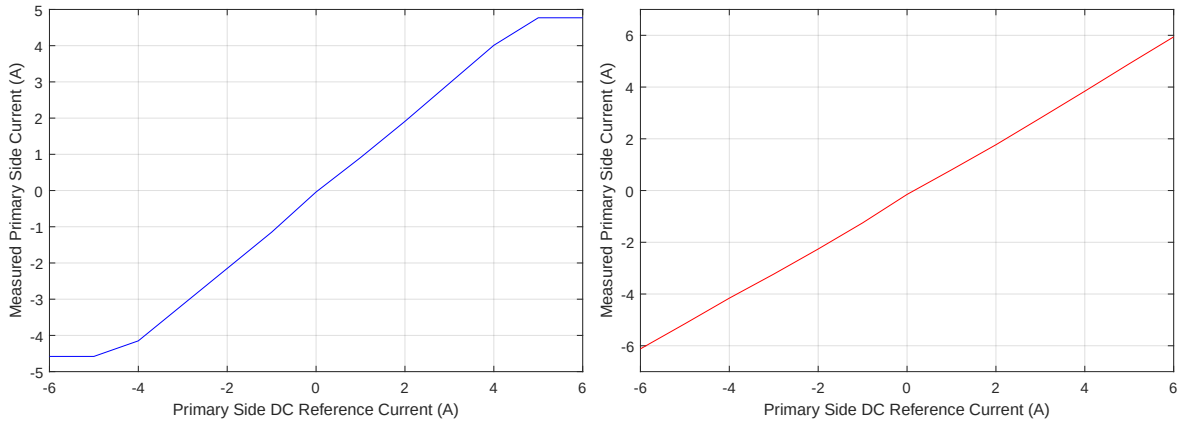

**Figure 5.9:** C2000 Simulink Setup for the DAB Current Reference Test

### 5.3.1. DC Current Reference Test Results

Table 5.7 shows the measured test results of the current reference sweep. Figure 5.10 shows the plotted results. Figure 5.11 shows the absolute and percental errors of the test. With the test using $V_{DC,pri} = 200V$, the current clearly goes into saturation for $\pm 5$ and $\pm 6$ A, as here the maximum phase shift is exceeded. Neglecting the saturation, the maximum absolute current error is 0.15A with the 200V DC link voltage and 0.26A with the 400V DC link voltage. Both tests again show higher errors for negative currents, with the percental error increasing as the current approaches zero.

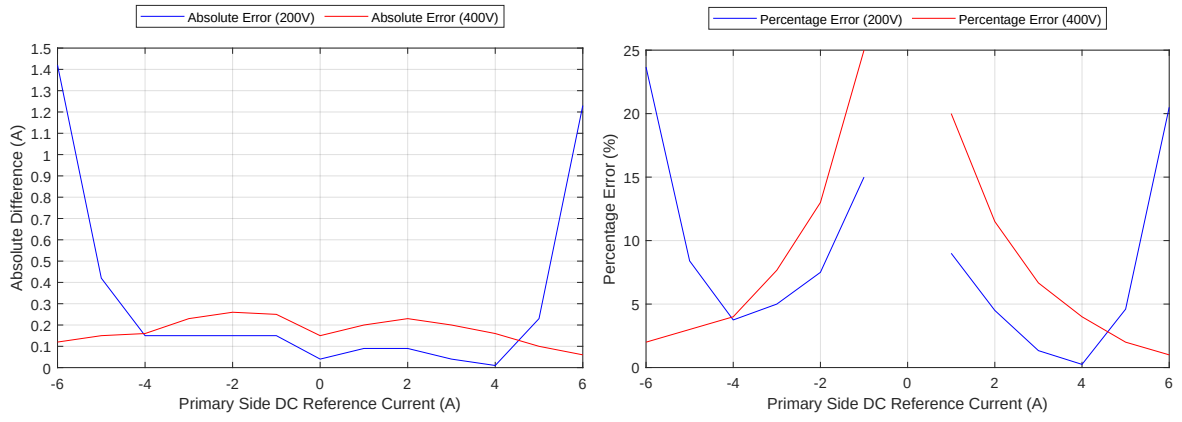
| $I_{ref}$ | -6 | -5 | -4 | -3 | -2 | -1 | 0 | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_{mes}$ $(V_{DC,pri} = 200V)$ | -4.58 | -4.58 | -4.15 | -3.15 | -2.15 | -1.15 | -0.04 | 0.91 | 1.91 | 2.96 | 4.01 | 4.77 | 4.77 |
| $I_{mes}$ $(V_{DC,pri} = 400V)$ | -6.12 | -5.15 | -4.16 | -3.23 | -2.26 | -1.25 | -0.15 | 0.8 | 1.77 | 2.8 | 3.84 | 4.9 | 5.94 |

**Table 5.7:** Reference Current Sweep Test Results




**(a)** $V_{DC,pri} = 200V$ **(b)** $V_{DC,pri} = 400V$

**Figure 5.10:** Measured Primary Side DC Currents with the Current-Sweep Test

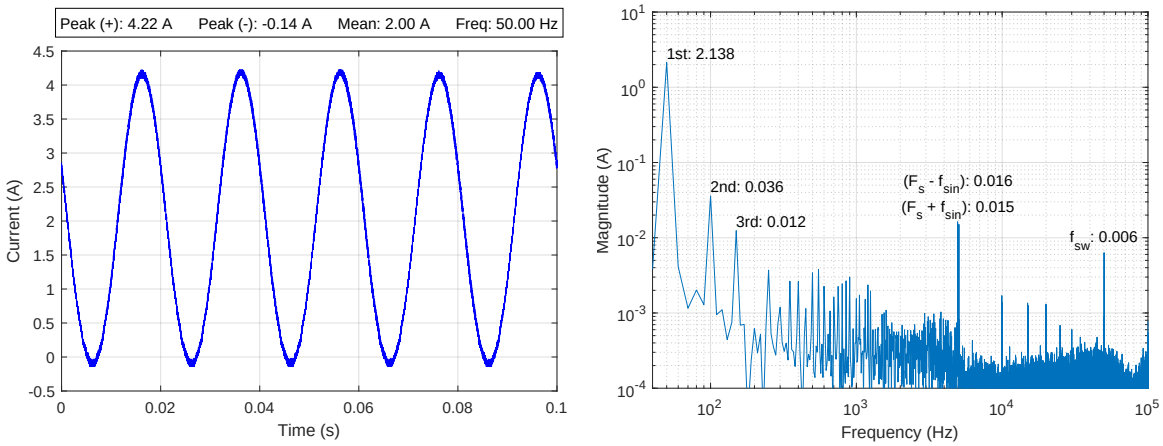



**(a)** Absolute Error **(b)** Percental Error

**Figure 5.11:** Error between Set and Measured Primary Side DC Currents with the Current-Sweep Test

### 5.3.2. Sinusoidal Current Reference Test Results

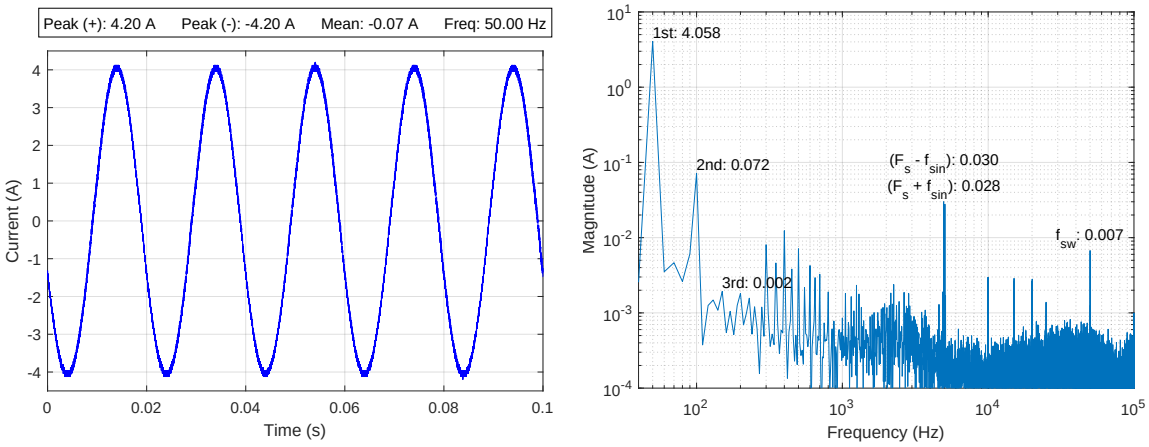
The constant current reference is now replaced with an $f_{sin} = 50Hz$ sine wave, sampled at $F_s = 5000Hz$. This is first done for a sine wave with an amplitude of 0 to 4 A and an offset of 2 A. Secondly it is repeated for a sine wave with an amplitude of $\pm$ 4 A and an offset of 0 A. The primary DC side low-side current is measured using the oscilloscope and the current probe. The measured results are imported into Matlab for analysis. FFT is performed to analyse the harmonics, neglecting any DC offset. Figures 5.12 and 5.13 show the results for these two measurements respectively. Certain harmonics have been highlighted.




**(a)** Time Domain Measured Sine Wave

**(b)** FFT of the Measured Sine Wave

**Figure 5.12:** Measured Primary Side DC Current with a 0 to 4 A Sinusoidal Current Reference




**(a)** Time Domain Measured Sine Wave

**(b)** FFT of the Measured Sine Wave

**Figure 5.13:** Measured Primary Side DC Current with a -4 to 4 A Sinusoidal Current Reference

Considering current level errors as discussed in section 5.3.1, it is possible to recreate sinusoidal waveforms with the use of the inverse DAB model. This will be required when tracking current in the MMC. Considering the harmonics, the fundamental frequency of 50 Hz and its harmonics are visible for both measurements. Furthermore, the sampling frequency of the sine wave with the 50 Hz sidebands is visible as are its harmonics. Lastly, the switching frequency of 50kHz is visible. Manually estimating the THD using the marked harmonics gives 2.07% and 2.05% for both measurements respectively. Only considering the marked lower harmonics gives 1.8% for both measurements, which could be achieved with a higher sampling frequency. Considering these THD levels, it can be stated that with the use of the inverse DAB model, AC waveforms can be generated without excessive harmonic distortion.

## 5.4. The Current Step Test: Closed Loop Voltage Control

The last test is a closed-loop voltage control DAB test with a current step on the primary DC side input. Here, closed-loop PI control is compared to the Improved DAB Control of figure 3.6. This test uses $V^*_{DC,pri} = 200V$ and $V_{DC,sec} = 125V$. Figure 5.14 shows the hardware test setup. The primary side DC supply is now replaced with a unidirectional Agilent Technologies N5772A supply, as this has a higher current precision and can therefore output a more stable DC current compared to the bidirectional Delta supplies. The supply is set to a current of 2.700A and a voltage of 400V, allowing for a factor 2 voltage overshoot. As the DAB has no internal DC current measurement, an external low-side current measurement is used. The external current sensor uses a LEM CASR 6-NP current transducer [57]. A hand-soldered RC lowpass filter (LPF) is used with $R = 820\Omega$ and a $C = 10nF$ ceramic capacitor, resulting in a cutoff frequency of approximately 19.4kHz. Additional 10pF ceramic capacitors are connected to the filters in- and output for filtering. This signal then directly goes to the MCU's ADC, where it is sampled at 25kHz. The oscilloscope measures the low-side primary-side DC current as well as the primary-side DC voltage.

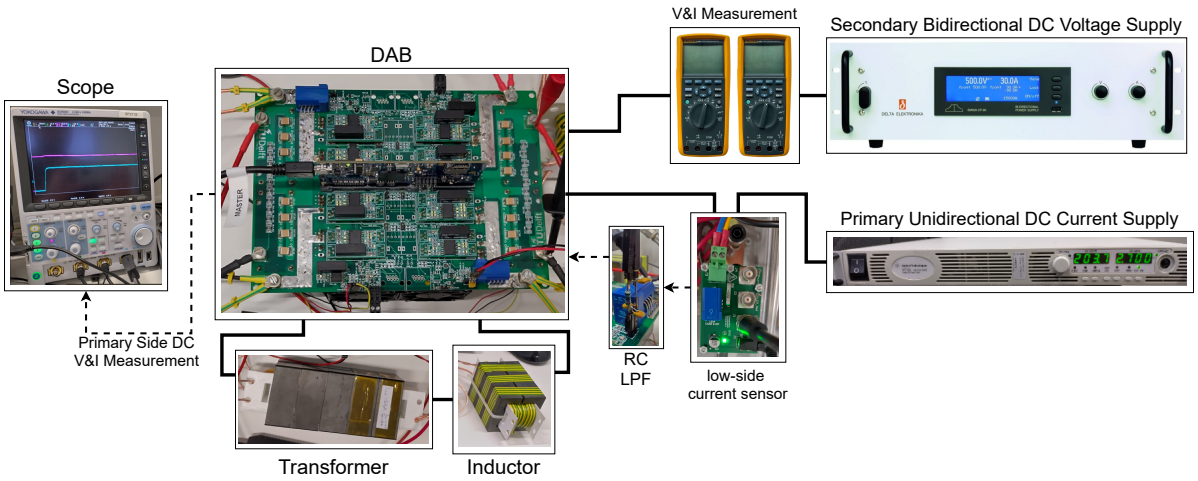



**Figure 5.14:** Test Setup for the Current step Test

Figure 5.15 shows the Simulink Dashboard for the current step test. It shows the MCUs measured DC voltages and primary DC current. The voltage reference values can be set, as well as the PI controller control gains. Furthermore, the toggle switches give the option to disable or enable the current feedforward, the inverse DAB model or the entire system.

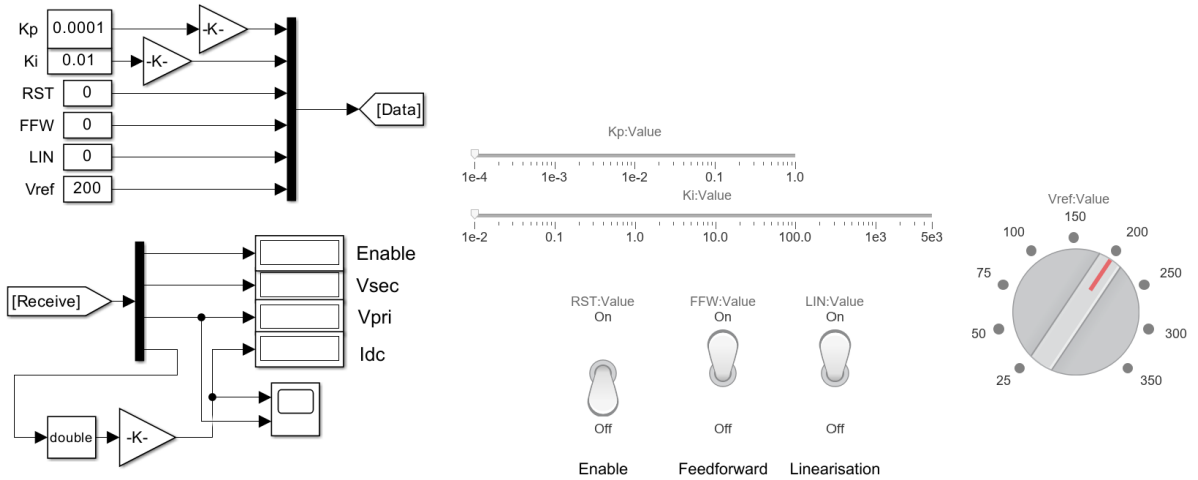



**Figure 5.15:** Dashboard for the DAB Closed-Loop Voltage Control Test

Figure 5.16 shows the Simulink C2000 setup for the closed-loop control for the current step test. The PI control values can be set externally. The output and the integrator are saturated at $\pm 0.25$, the maximum values for $\phi$. Either this output or the inverse-dab model output can be used. The inverse DAB model first contains a gain of 20, effectively increasing $K_p$, $K_i$ and the saturation limits with a factor of 20. Thus, the PI current saturation lies at $\pm 5A$. The PI controller uses back-calculation anti-windup with a gain of 1. Either the measured current or 0 can be added to this output, enabling or disabling the current feedforward. The inverse DAB-model then calculates the required phase shift from this.

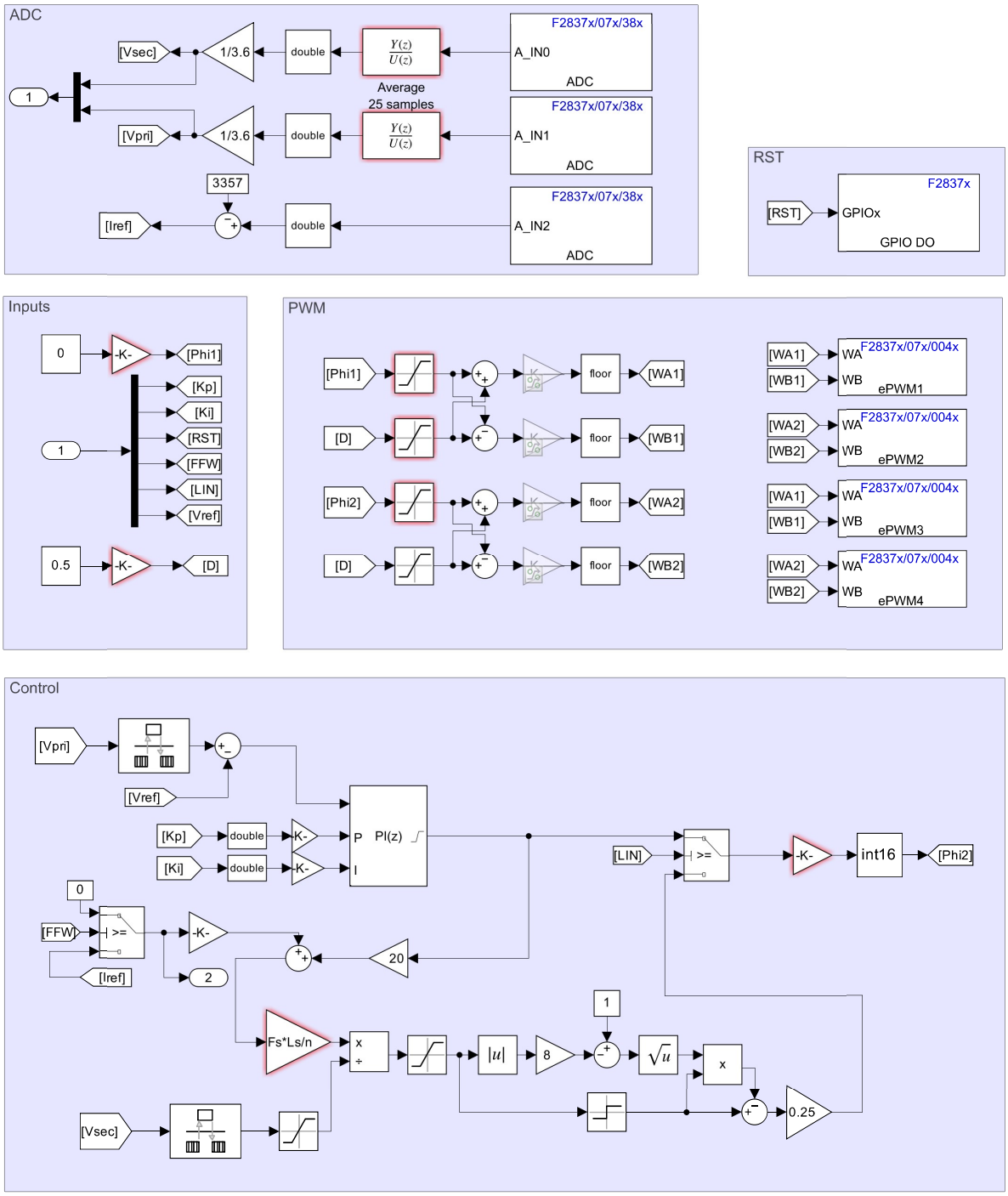
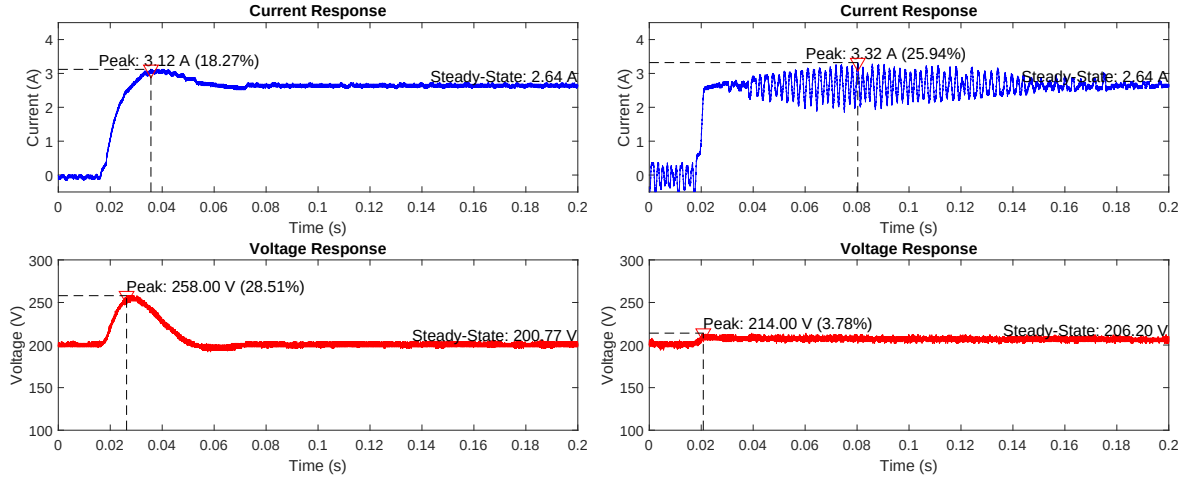



**Figure 5.16:** C2000 Simulink Setup for the DAB Closed-Loop Voltage Control Test

### 5.4.1. Current Step Test Results

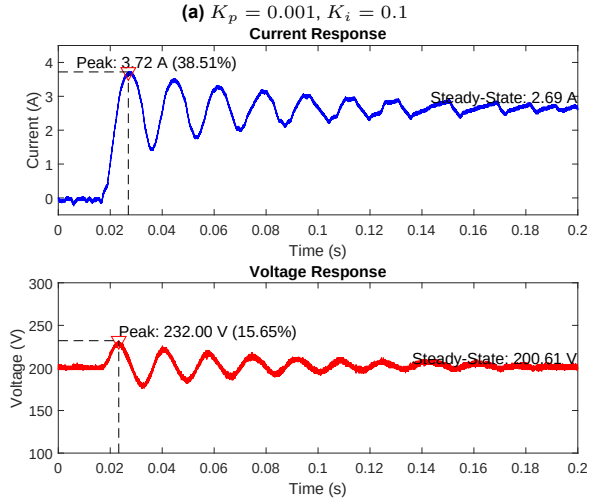
A current step of 2.700A is applied to the primary side DC connection, the control system tries to regulate the voltage to approximately 200V. Figure 5.17 shows the step response using only the PI control. Figure 5.18 shows the step response of the PI control combined with the inverted DAB model. Figure 5.19 shows the step response of the current feedforward and PI control combined with the inverted DAB model. Note that the primary side DC source is not ideal and that the voltage response can affect the current. Appendix D shows the original screenshots of the oscilloscope containing the same measurements.



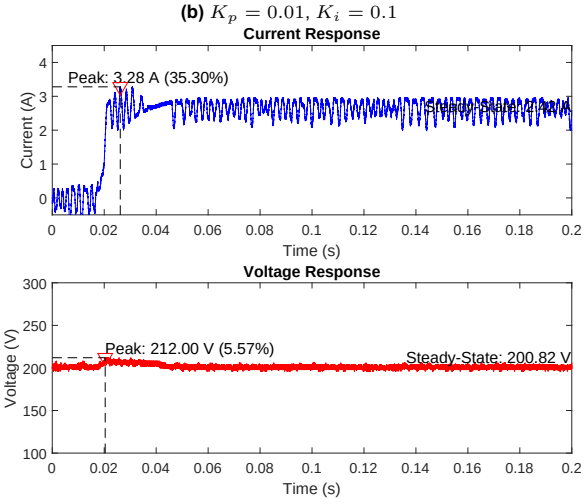

**(a)** $K_p = 0.001$, $K_i = 0.1$




**(b)** $K_p = 0.01$, $K_i = 0.1$

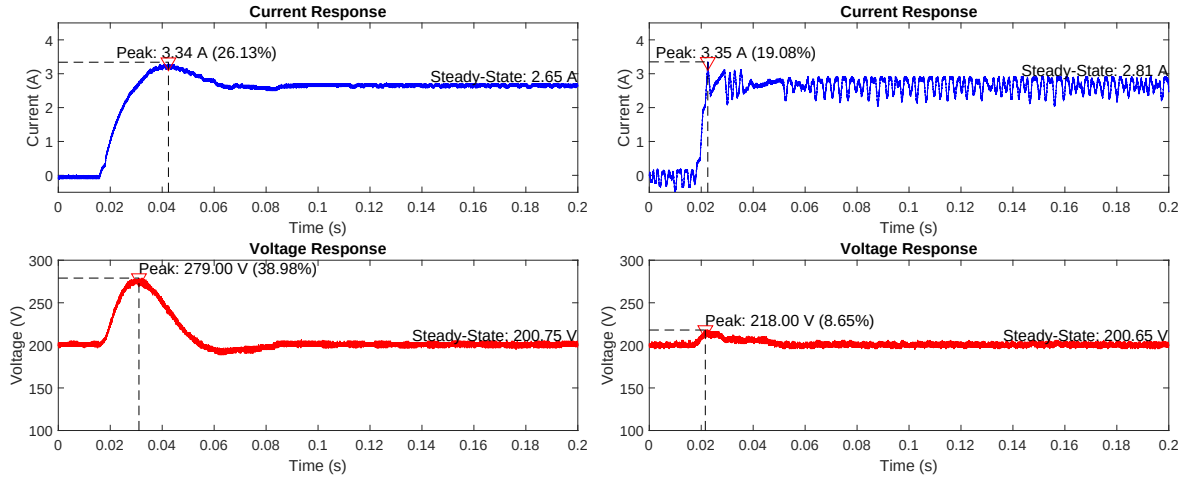



**(c)** $K_p = 0.001$, $K_i = 1$



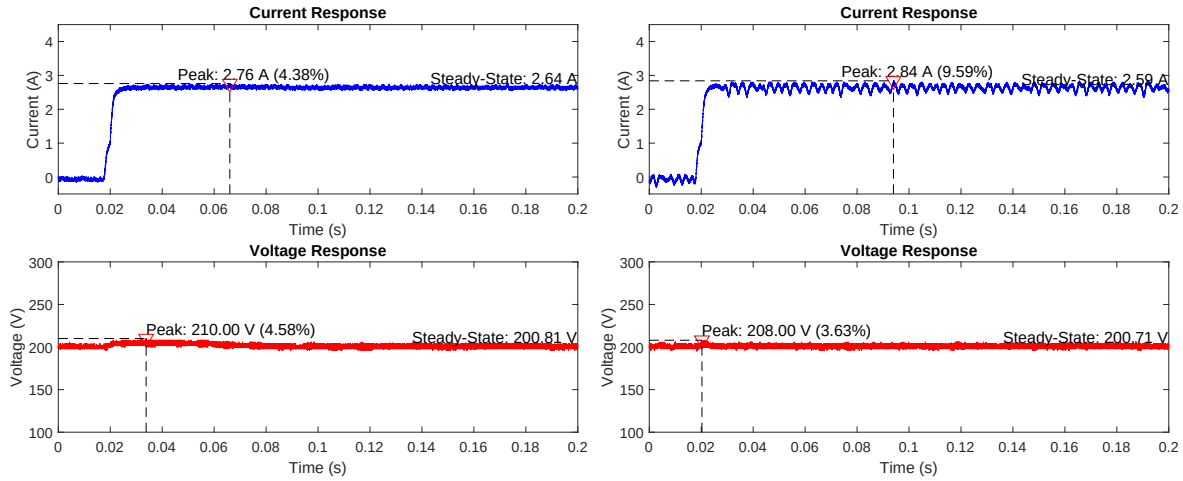

**(d)** $K_p = 0.01$, $K_i = 1$

**Figure 5.17:** Current and Voltage response of the Current-step test using standard PI control




**(a)** $K_p = 0.02$, $K_i = 2$ **(b)** $K_p = 0.2$, $K_i = 20$

**Figure 5.18:** Current and Voltage response of the Current-step test with linearised PI control




**(a)** $K_p = 0.002$, $K_i = 0.2$ **(b)** $K_p = 0.02$, $K_i = 2$

**Figure 5.19:** Current and Voltage response of the Current-step test using current feedforward into the inverse DAB model

| FFW | LIN | $K_p$ | $K_i$ | Overshoot | Note |
|---|---|---|---|---|---|
| No | No | $0.001$ | $0.1$ | 28.51% | - |
| No | No | $0.01$ | $0.1$ | Undefined | *Does not converge within set time.* |
| No | No | $0.001$ | $1.0$ | 15.65% | *Undesired current and voltage ripple.* |
| No | No | $0.01$ | $1.0$ | 5.57% | *Undesired current ripple* |
| No | Yes | $0.001 \cdot 20$ | $0.1 \cdot 20$ | 38.98% | - |
| No | Yes | $0.01 \cdot 20$ | $1.0 \cdot 20$ | 8.65% | *Undesired current ripple* |
| Yes | Yes | $0.0001 \cdot 20$ | $0.01 \cdot 20$ | 4.58% | - |
| Yes | Yes | $0.001 \cdot 20$ | $0.1 \cdot 20$ | 3.36% | *Undesired current ripple* |

**Table 5.8:** Summarised Results of the Current step Test

Table 5.8 shows the summarised results of the current step test, comparing the usage of current feedforward (FFW), linearisation by using the inverse DAB model (LIN) and various control gain values. This shows that the control systems using feedforward always result in the lowest voltage overshoot. Increasing the control gains can reduce the overshoot, at the cost of undesired current ripples and/or increased settling times. Using the current feedforward allows for even lower control gain values compared to the other methods, resulting in a 4.6% overshoot with a desirable current response for $K_p = 0.002$ and $K_i = 0.2$.

# 6

# Conclusion and Recommendations

With the implementation of the new EU Law for regulation for the deployment of alternative fuels infrastructure, including mandatory EV charging stations with pool powers up to 3.6MW across the TEN-T network by 2030, there will be a need for better grid connections. For these higher power (Ultra-) Fast EV Charging stations, a connection to the 10kV MVAC grid is desirable to handle these power levels. For this connection, an MMC-based SST is a better solution compared to the conventional LFT in terms of size, weight and efficiency. In this thesis, this SST, based on three different MMC topologies, has been analysed. A mathematical model has been made to determine the behaviour and allow for control system tuning. Three control systems have been designed for each SST, including an improved DAB control based on current-feedforward combined with the inverse DAB model to reduce the submodule voltage ripples. The DAB control has been tested using hardware and a current-step input. The Single-Star topology generally performs the best in terms of the main MMC cost parameters: Energy storage and switch stress. By oversizing the DAB, the improved DAB control system can further reduce the required energy storage.

## 6.1. The Mathematical Model

A mathematical model has been created for the Double-Star MMC, the DAB and the three SST topologies. The MMC model is based upon the use of a switching function ($S(t)$), which describes the relation between the submodule voltages and the inserted arm voltage, and the relation between the arm current and the submodule current. This mathematical model is able to accurately model the behaviour of the d- and q-component currents, the average submodule voltages and the LVDC bus voltage for all three SSTs including their control system. This model runs significantly faster than the switched model. Compared to the commonly used average model for the MMC, the mathematical model is more suitable for SSTs due to the inclusion of the DAB model. Table 6.1, equal to table 2.8, shows the comparison of the different simulation methods.

| **Switched Model** | **Mathematical Model** | **Average Model** |
|---|---|---|
| Very accurate | Accurate for analysing the behaviour | Accurate for analysing the behaviour |
| Includes switching effects | Does not include switching effects | Does not include switching effects |
| Can model SM Voltage unbalance | Can not model SM Voltage unbalance | Can model SM Voltage unbalance |
| Simulation speed dependent upon N | Simulation speed independent from N | Simulation speed dependent upon N |
| Slow MMC Simulation | Fast MMC Simulation | Fast MMC Simulation |
| Slow DAB Simulation | Fast DAB Simulation based upon phase-shift | Slow DAB Simulation |
| Model built using a schematic | Model built using analytical equations | Model built using a schematic. |

**Table 6.1:** Comparison of switched, mathematical and average modelling of the SST (Table 2.8)

Due to the high accuracy and simulation speed of the mathematical SST model, this can be used for control system analysis and automated tuning of the control system using the Genetic Algorithm. Within a set time (e.g. 12 hours), the model can be run a significantly higher number of times than the switched model. A simulation of the switched model is still required afterwards for verification purposes and to accurately analyse the submodule voltage ripples and converter THD and switch stress.

## 6.2. The Control System

Three different control systems have been designed, which can be classified as control systems A, B and C. An improved DAB control has been designed based on an inverted DAB model, which includes linearisation, and a current feedforward working together with a voltage-reference PI controller. Applying this gives control systems B* and C*. The use of control system C/C* assumed a constant DC voltage source on the LVDC bus; this could be implemented by, for example, a BESS (battery energy storage system).

All control systems have the same current controller, which can be tuned by setting the bandwidth $\alpha_f$ of the controller. For control system A, the reference d-component current is generated using a PI controller on the average submodule voltage. For control system B, this is generated using a PI controller on the LVDC bus voltage. For control system C, the value is set by the desired amount of power. The reference q-component current is always 0.

With control system A, the DAB controller controls the voltage on the LVDC bus. With control systems B and C, the DAB controller controls the individual submodule voltages. Therefore, control system A has no control over the individual submodule voltages. Control systems B and C offer this control, ensuring there is no need for voltage balancing. Control systems B* and C* are the most suitable for reducing the submodule voltage ripple and therefore reducing the required submodule energy storage. Control systems B and C cause a voltage overshoot on the submodule voltage during a transient, whereas control system A causes a voltage dip. Full submodule voltage suppression with control system B* and C* using an oversized DAB removes this overshoot.

The comparison between the different control systems is summarised in table 6.2. This assumes a 'slow' DAB control for control systems B and C, affecting the submodule voltage ripple as little as possible, as this would otherwise increase the THD and create an undesired voltage ripple on the LVDC bus. It also assumes a full ripple suppression for control systems B* and C*, oversizing the DAB. The control systems are ranked from 1 (best) to 5 (worst) on the tunability. The tunability is the ease with which the control system can be tuned, dependent upon the amount of the control system parameters, the influence of the different control systems on each other and the ease with which the control parameters can cause an unstable system.

| | **Control A** | **Control B** | **Control B*** | **Control C** | **Control C*** |
|---|---|---|---|---|---|
| **Individual $V_{SM}$ Control** | no | yes | yes | yes | yes |
| **Effective $V_{SM}$ Ripple Reduction** | no | no | yes | no | yes |
| **$V_{SM}$ overshoot during transients** | no | yes | no | yes | no |
| **Requires DAB Oversizing** | no | no | yes | no | yes |
| **Requires LVDC Voltage Source** | no | no | no | yes | yes |
| **Settling Time (SingleStar)** | <0.70 [s] | <0.35 [s] | <0.15 [s] | <0.25 [s] | <0.10 [s] |
| **THD Performance (SingleStar)** | 0.149% | 0.117% | 0.109% | 0.110% | 0.101% |
| **Tuneability** | 3 | 5 | 4 | 2 | 1 |

**Table 6.2:** Ranking of the control systems

As the use of control systems B* and C* can significantly reduce the required energy storage and improve the general performance of the SST due to stable submodule voltages, these are the preferred control systems. If a voltage source, such as a BESS, is available for the LVDC bus, this will lead to the best general performance of the SST. The oversizing of the DAB is required to increase the allowed peak DAB current while maintaining the same average DAB current. Therefore this will not have a significant impact on the thermal performance of the DAB. Cost-wise, this means that the saved cost of the significantly reduced energy storage weighs more than the increased DAB cost considering oversizing. Without the improved DAB control system, control systems B and C still perform better than control system A and ensure stable submodule voltages. Control system B does, however, have a lower tuneability than control system A due to the dependency of the two voltage controllers upon each other.

## 6.3. Topology Comparison

The Single-Star topology performs the best out of the three compared topologies in terms of the main MMC cost parameters: Energy storage and switch stress. This is followed by the Single-Delta topology and the Double-Star topology respectively. Considering the ideal theoretical submodule voltage ripples, the Single-Delta configuration should perform equally to the Single-Star configuration. However, undesired effects caused by current ripples change this behaviour. The Double-Star configuration will inherently perform less well due to the increased energy storage requirement, caused by each arm only inserting half the voltage. Furthermore, the Double-Star configuration has an undesired circulating current which decreases the performance. Table 6.3 shows a comparison of the three topologies.

| | **Double-Star** | **Single-Star** | **Single-Delta** | ***Control System*** |
|---|---|---|---|---|
| $\mathbf{E_{MMC,min}}$ (theoretical) | 245 [kJ] | 55.7 [kJ] | 55.7 [kJ] | - |
| $\mathbf{E_{MMC}}$ | 385 [kJ] | 59.5 [kJ] | 87.5 [kJ] | *A* |
| $I_{SM,peak}$ deviation to ideal | 67.5 % | 0% | 50% | *A* |
| **THD** | 0.165% | 0.149% | 0.224% | *A* |
| **THD** | 0.102% | 0.101% | 0.103% | *C** |
| $\mathbf{N_{SW}V_{SM}I_{SW,RMS}}$ | 14.0 [MVA] | 13.1 [MVA] | 11.9 [MVA] | *C** |
| $\mathbf{N_{SW}V_{SW}I_{SW,RMS}}$ | 17.7 [MVA] | 16.5 [MVA] | 17.4 [MVA] | *C** |
| $\mathbf{K_{DAB,min}}$ | 4 | 2 | 2 | *B* or C** |
| Circulating Current | yes | no | no | - |

**Table 6.3:** Summary of the three topologies

In this case, the use of the Single-Star topology will lead to the lowest cost. Compared to the Double-Star topology, it inherently performs better in terms of energy storage, furthermore, it has the additional benefit of no circulating current. While with the improved DAB control, the Double-Star SST's circulating current gets significantly reduced, it requires double the DAB oversizing compared to the other topologies. Comparing the Single-Star to the Single-Delta topology should inherently not give a better performance. However, with the used control system, the behaviour of the Single-Star SST lies much closer to the theoretical ideal compared to the Single-Delta topology, which results in the best performance. While the deviation of the switch stress between the topologies is not very significant on the SST cost, the reduction in the MMC energy storage requirement will significantly reduce the cost. This can be reduced even further, simulated with an 80% reduction of the theoretical minimum, further reducing the cost of the SST.

## 6.4. Improved DAB Control and Hardware Test Conclusion

An improved DAB control has been proposed. This control combines a current feedforward from the submodule input current with a feedback PI voltage control and the inverse DAB model. The current feedforward combined with the inverse DAB model removes the capacitor current and therefore the ripple. The PI control ensures voltage stability in case of measurement or model errors, or saturation. As stated in section 6.2, the improved DAB control leads to the best SST performance. Figure 6.1, equal to figure 3.7, shows the improved DAB control system. Similar control methods for DABs have been proposed in literature, though in a different setting with different equations and/or exact control topologies.

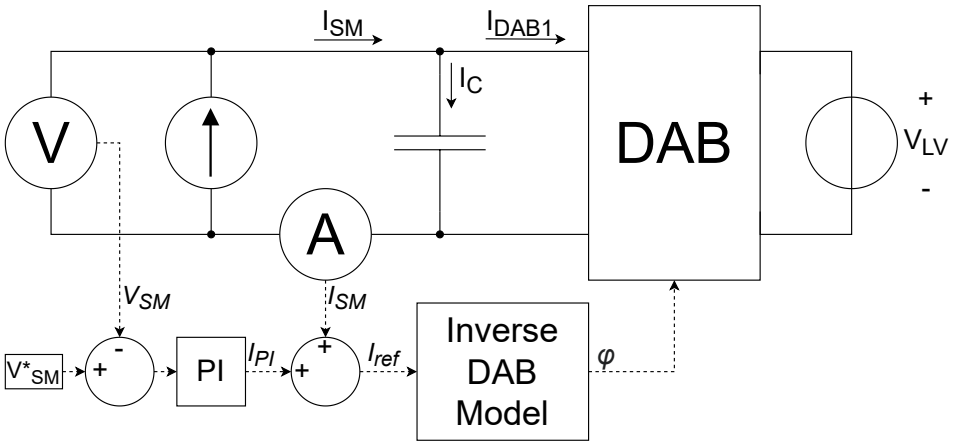



**Figure 6.1:** Proposed improved DAB control, combining current feedforward with the inverse DAB model

A hardware test has been done to test the validity of the (inverse) DAB model. While the neglect of series resistance among other non-ideal parameters causes error, which is the largest for negative currents, the calculated current from the phase angle follows the actual current. The maximum primary side absolute error is 0.12A on a range from -4.58A to 4.77A, which is 1.3% of the range. The maximum secondary side absolute error is 0.22A on a range from -7.29A to 7.62A, which is 1.5% of the range.

Using a DC reference current for the primary DC side has been tested successfully as well, with a primary side DC voltage of 200V, the maximum absolute error is 0.15 on a reference range over $\pm$4A. This has been successfully repeated for a sinusoidal reference, where harmonic analysis by FFT has shown no excessive harmonic distortion.

A closed-loop control and current step test have shown how the control system can perform peak reduction during voltage control. A PI control, linearised or not, leads to an overshoot. This can be reduced by increasing the voltage gains, but this leads to an undesired system response with effects such as high current ripples. The lowest voltage overshoot is always achieved using the current feedforward combined with the inverse DAB model. This gives an overshoot of 4.6%. The lowest achieved overshoot with PI control and without undesired ripples is 28.5%. Comparing these two gives a peak reduction of 6.2 or 84%. As the voltage ripple is proportional to the capacitance, the simulated energy storage reduction of 80% should be achievable. With further optimisation of the hardware implementation with respect to e.g. the sensors used, the MCU speed and the calibration, further increased performance could be achievable.

Applying a slower PI control combined with the current feedforward leads to the most desirable system response. The hardware tests have proven the capability of the improved DAB control system based on the combination of current feedforward, feedback PI control, and the inverse DAB model to be successful.

## 6.5. Recommendation

To summarise the conclusion, in terms of MMC cost, the Single-Star topology with control system B* or C* and a DAB oversizing factor 2 is recommended as this leads to the lowest required energy storage. The capability of the improved DAB control for these control systems has been proven with hardware tests. In terms of switch stress, the differences are less significant compared to the energy storage requirement. In terms of general performance (THD, setting time, deviation from ideal behaviour), the Single-Star topology with control system C* performs the best, followed by control system B*. The tuning of the control system can be done using the newly developed SST mathematical model, which can accurately determine the average behaviour of the SST. This always needs to be checked using a switched model.

Future research of the MVAC to LVDC SST can include, but is not limited to:

- Investigating the option to use a BESS as a voltage source on the LVDC bus to allow for control system C* (best SST performance).
- Investigating the possibility of an analytical method of tuning the control system, using the mathematical model.
- Investigating the possibility of including the series resistance in the inverse DAB model, potentially improving this control.
- Investigating the effect of the hardware DAB voltage and current measurement accuracy and calibration upon the improved DAB control system, potentially improving this control.
- A hardware test setup of a single SST submodule, including the DAB, checking the exact amount of the required energy storage, which can be reduced with the improved DAB control system.
- A DAB cost analysis, comparing the increased cost of the DAB oversizing to the decreased cost of the MMC energy storage.
- A thorough hardware design of the Single-Star SST, including component choices, and thermal and magnetic components design, gives a clear view of the precise cost and requirements.
- A hardware test setup of the full Single-Star SST, to determine the behaviour in a real setting.

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# A

# Publication Draft ITEC 2024: Mathematical Modelling of Solid-State Transformers and Control System Tuning using the Genetic Algorithm

# Mathematical Modelling of Solid-State Transformers and Control System Tuning using the Genetic Algorithm

Casper Grootes, Adnan Ahmad, Pavol Bauer, Zian Qin

***Abstract*—With the upcoming increase in (ultra-) fast EV charging stations consisting of multiple 350kW chargers, an MV grid connection with MVAC to LVDC conversion via MMC-based SSTs seems a promising solution. However, the proposed SST is a highly non-linear MIMO system; therefore, its control tuning is complex and requires simulation. Switched MMC-based SST simulations can take significant time to run, and there needs to be more than the existing sub-cycle average or analytical mathematical MMC models for the MMC-based SST. A novel mathematical model of the SST is developed; the proposed model can be implemented in existing simulation platforms and can accurately determine the average behaviour with reduced computational complexities and time. Moreover, the genetic algorithm combined with the proposed model provides a potential solution for the tuning of control parameters.**

## I. Introduction

In July 2023 a new EU law was passed with mandatory electric recharging infrastructure targets for the road sector, including EV charging pool power requirements up to 3.6MW [1], [2]. A connection to the MVAC grid is desired for these charging stations; this while individual EV chargers with a power rating of up to 350kW require 800V DC. [3]

The Solid-State Transformer (SST) can perform better in terms of volume weight and losses with a similar cost compared to the conventional low-frequency transformer considering MVAC to LVDC conversion. [3], [4] Of the various SST types [5], the Modular Multilevel Converter (MMC) -based SST is the main choice of topology. [6] The MMC types Single-Star, Double-Star, Single-Delta presented in [7] are considered.

The SST is a non-linear MIMO system with a control system that is therefore not straightforward to tune. This requires simulation. Switched simulations of MMCs and MMC-based SSTs take significant time to run. Sub-cycle average MMC models offer decreased simulation time [8], [9] but are not suitable for SSTs simulation due to their Dual Active Bridges (DAB). A mathematical model of the SST could potentially offer this. Known simulation methods or models currently do not offer this for SSTs. Common mathematical MMC models often neglect the submodule capacitor ripples [10], while other mathematical methods only focus on an approximate harmonic analysis [11] of the submodule voltages.

In this paper, a novel mathematical model is derived and proposed which can accurately describe the average MMC behaviour including the submodule voltages and currents. This can in turn be extended with a DAB model, resulting in the proposed mathematical SST model. This model can be used for control system tuning using the Genetic Algorithm [12].

The outline of this paper is as follows: First an overview of the considered SST and its control system is given. Secondly, the proposed mathematical models are outlined for the Double- and Single-Star and -Delta MMCs, the DAB, and the proposed Double-Star SST including its simulation. Thirdly, a description is given of how control system tuning using the Genetic Algorithm can be done using this model and its results are given. Lastly, a conclusion about the proposed mathematical model and its use for control system tuning is given.

## II. The considered SST and its Control System

Double-Star, Single-Star and -Delta MMC-based SSTs are considered. The Double-Star topology uses half-bridge submodules and the Single-Star and -Delta topologies use full-bridge submodules. A phase-shifted carrier (PSC) is used for equal submodule power distribution [13]. A DAB is connected to each submodule as presented in [14], [15], [16], [5], [4], [6]; similar to series to parallel DAB configurations but without the need of an MVDC link.

The MMC current controller is provided by PLEXIM [17]; it is described in [18]. This is a commonly used current controller for grid-tie inverters and can be tuned using MMC parameters and a user-specified bandwidth $\alpha_f$. This controller generates the reference voltages $V_d^*$ and $V_q^*$ from the current references $I_d^*$ and $I_q^*$. In combination with the inverse Park-Clarke transform this results in the AC reference waveforms. $I_d^*$ is provided by a PI control on the average submodule voltage, $I_q^* = 0$. The DAB uses a single-phase-shift control where the phase ($\phi$) is given by a PI control on the LVDC bus. Fig. 1 represents a simplified version of the control system.

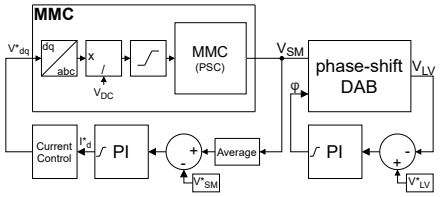


Fig. 1. The SST Control System

A 3.5MVA, N+1-level SST is considered with $V_{g,peak} = 8.1kV \propto V_g \approx 10kV$, $N = 12$, and $V_{SM} = 1.35kV$.

## III. Mathematical Modelling of the SST

### A. The Double-Star MMC

The Double-Star MMC can be analysed per leg using basic network theory combined with the use of a switching function. Fig. 2 shows a single arm of the Double-Star MMC. Applying

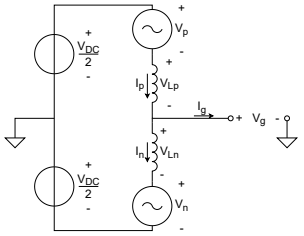


Fig. 2. Single Leg of the Double-Star MMC

Kirchoff's voltage law to both arms, with the inductor voltage defined by equation 1, gives equations and 2 and 3.

$$V_{L(p,n)} = L\frac{dI_{p,n}}{dt} + R_L I_{p,n} \tag{1}$$

$$V_p + L\frac{dI_p}{dt} + R_L I_p + V_g = \frac{V_{DC}}{2} \tag{2}$$

$$V_n + L\frac{dI_n}{dt} + R_L I_n - V_g = \frac{V_{DC}}{2} \tag{3}$$

The grid current $I_g$ and circulating current $I_c$ are given by equations 4 and 5 respectively.

$$I_g = I_p - I_n \tag{4}$$

$$I_c = \frac{I_p + I_n}{2} \tag{5}$$

$V_o$ and $V_c$ can be defined according to equations 6 and 7 with the model of Fig. 3. [10]

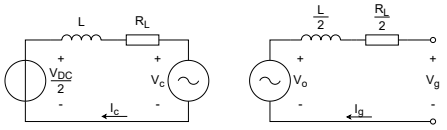


Fig. 3. Single Leg Equivalent of the Double-Star MMC

$$V_o = \frac{V_n - V_p}{2} \tag{6}$$

$$V_c = \frac{V_p + V_n}{2} \tag{7}$$

Modelling the submodule voltages using a switching function is described in [11]. This defines the switching functions for the upper and lower arm $S'_p$ and $S'_n$ respectively, using the modulation index m, as equations 8 and 9.

$$S'_p(t) = \frac{1 - m \cdot \sin(\omega t)}{2} \tag{8}$$

$$S'_n(t) = \frac{1 + m \cdot \sin(\omega t)}{2} \tag{9}$$

These switching functions have a relation to the voltages $V_p$ and $V_n$, the submodule currents $I_{SMp}$ and $I_{SMn}$ (only valid for even SM Power distribution using PSC-modulation). However, with the proposed SST control, the switching behaviour is determined by the inverse Park-Clarke Transform (equation 10). Here, $\phi$ can be replaced by $\omega t$ in the case of an ideal PLL. This leads to the newly defined switching functions according to equations 11 and 12.

$$P^{-1} = \begin{bmatrix} \cos(\phi) & -\sin(\phi) \\ \cos(\phi - 120°) & -\sin(\phi - 120°) \\ \cos(\phi + 120°) & -\sin(\phi + 120°) \end{bmatrix} \tag{10}$$

$$S_p(t) = \frac{1}{2} - \frac{1}{V_{DC}} \begin{pmatrix} V_a^* \\ V_b^* \\ V_c^* \end{pmatrix} = \frac{1}{2} - \frac{1}{V_{DC}} P^{-1} \begin{pmatrix} V_d^* \\ V_q^* \end{pmatrix} \tag{11}$$

$$S_n(t) = \frac{1}{2} + \frac{1}{V_{DC}} \begin{pmatrix} V_a^* \\ V_b^* \\ V_c^* \end{pmatrix} = \frac{1}{2} + \frac{1}{V_{DC}} P^{-1} \begin{pmatrix} V_d^* \\ V_q^* \end{pmatrix} \tag{12}$$

$$V_{p,n}(t) = S_{p,n}(t) \cdot \sum V_{SMp,n}(t) = N S_{p,n}(t) V_{SMp,n}(t) \tag{13}$$

$V_p$ and $V_n$ can be calculated according to equation 13. With Equations 6 and 7 this results in equations 14 and 15.

$$V_o(t) = \frac{S_n(t) \cdot N \cdot V_{SMn}(t) - S_p(t) \cdot N \cdot V_{SMp}(t)}{2} \tag{14}$$

$$V_c(t) = \frac{S_p(t) \cdot N \cdot V_{SMp}(t) + S_n(t) \cdot N \cdot V_{SMn}(t)}{2} \tag{15}$$

The grid and circulating currents can now be found using the Laplace domain with equations 16 and 17.

$$I_g = \frac{V_o - V_g}{(L/2)s + (R_L/2)} \rightarrow \frac{I_g}{V_o - V_g} = \frac{2}{Ls + R_L} \tag{16}$$

$$I_c = \frac{(V_{DC}/2) - V_c}{Ls + R_L} \rightarrow \frac{I_c}{(V_{DC}/2) - V_c} = \frac{1}{Ls + R_L} \tag{17}$$

Solving the system of equations with equations 4 and 5, for $I_p$ and $I_n$, gives equations 18 and 19 respectively.

$$I_p = \frac{I_g}{2} + I_c \tag{18}$$

$$I_n = I_c - \frac{I_g}{2} \tag{19}$$

The relation between the switching function and the submodule current $I_{SM}$ is presented in [11] as stated in equation 20.

$$I_{SMp,n}(t) = S_{p,n}(t) \cdot I_{p,n}(t) \tag{20}$$

Equation 21 gives the submodule voltage $V_{SM}$ from the submodule capacitor current $I_{C,SM}$ in the Laplace domain.

$$\frac{V_{SM}(s)}{I_{C_{SM}}(s)} = \frac{R_{C_{SM}} C_{SM} \cdot s + 1}{C_{SM} \cdot s} \tag{21}$$

By using the found submodule voltage in equation 13, a complete model is achieved which can determine the submodule voltages and currents from the control system output. Fig. 4 shows a schematical overview of the model.

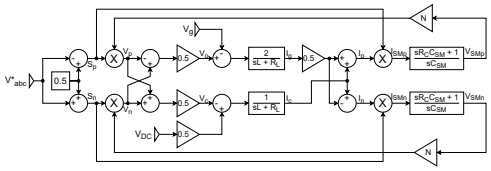


Fig. 4. Double-Star MMC Model

### B. The Single-Star MMC

The Single-Star MMC model is similar to that of the Double-Star model but only contains one arm per phase, capable of inserting both positive and negative voltages, and containing no circulating current. Fig. 5 shows the arms of the three phases of the Single-Star MMC with the inserted voltages $V_i$. There is now only one grid-connected arm per

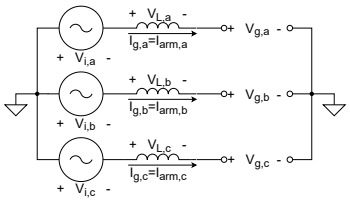


Fig. 5. Single-Star MMC

phase, therefore each arm current is equal to the grid current. As the grid current is sinusoidal, the sum of the three 120°-phase-shifted currents will be zero and there will be no DC currents flowing through the arms. As a result of this, all voltages are zero average and the star-connected point of the three arms will equal the neutral voltage of the grid. Thus, the inductor voltage can be calculated according to equation 22. Equation 23 is used to determine the grid currents.

$$V_L = -V_i - V_g \tag{22}$$

$$\frac{I_g(s)}{V_L(s)} = \frac{1}{sL + R_L} \tag{23}$$

With the use of a Full-Bridge submodule, the total inserted voltage range is double the submodule voltage as the range is determined by the positive and negative submodule voltage. The switching function can now be redefined for the Single-Star MMC according to equation 24. Equation 25 presents the resulting inserted voltage. Equation 26 presents the Single-Star submodule current.

$$S(t) = \frac{-2}{V_{DC}} P^{-1} \begin{pmatrix} V_d^* \\ V_q^* \end{pmatrix} \tag{24}$$

$$V_i(t) = S(t) \cdot \sum V_{SM}(t) \rightarrow V_i(t) = N \cdot S(t) \cdot V_{SM}(t) \tag{25}$$

$$I_{SM}(t) = S(t) \cdot I_g(t) \tag{26}$$

### C. The Single-Delta MMC

The Single-Delta MMC, similar to the Single-Star MMC, contains only one arm capable of inserting both positive and negative voltages, between each two phases. The voltage across the arms can be defined as $V_\Delta$ according to equation 27, where the relation between the grid current $I_g$ and MMC current $I_\Delta$ is given by equation 28.

$$V_\Delta(t) = \begin{pmatrix} V_{ab}(t) \\ V_{bc}(t) \\ V_{ca}(t) \end{pmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{pmatrix} V_{g,a}(t) \\ V_{g,b}(t) \\ V_{g,c}(t) \end{pmatrix} \tag{27}$$

$$I_g(t) = \begin{pmatrix} I_{g,a}(t) \\ I_{g.b}(t) \\ I_{g,c}(t) \end{pmatrix} = \begin{bmatrix} -1 & 0 & 1 \\ 1 & -1 & 0 \\ 0 & 1 & -1 \end{bmatrix} \begin{pmatrix} I_{ab}(t) \\ I_{bc}(t) \\ I_{ca}(t) \end{pmatrix} \tag{28}$$

Fig. 6 shows the single-arm equivalent of the Delta MMC, using the defined voltage $V_\Delta$. The switching function can

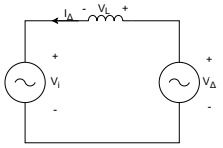


Fig. 6. Single Arm Equivalent of the Delta MMC

now be defined according to equation 29, the inductor voltage as equation 30 and the inductor current $I_\Delta$ as equation 31. The relationship between $V_i(t)$ and $S(t)$ remains the same as equation 25

$$S(t) = \frac{2}{V_{DC}} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \left( P^{-1} \begin{pmatrix} V_d^* \\ V_q^* \end{pmatrix} \right) \tag{29}$$

$$V_L = V_\Delta - V_i \tag{30}$$

$$\frac{I_\Delta(s)}{V_L(s)} = \frac{1}{sL + R_L} \tag{31}$$

The equations for the submodule currents and voltages will remain similar to those of the Double-Star MMC, given by equations 32 and 21.

$$I_{SM}(t) = S(t) \cdot I_\Delta(t) \tag{32}$$

### D. The Dual Active Bridge

A model of the Dual Active Bridge (DAB), to be combined with the model of the MMC to achieve an SST model, is required. A Dual Active Bridge (DAB) with a single phase shift control is considered.

Various mathematical models are presented in [19], [20], [21], [22]. However, a very simple model of the DAB might suffice as the modelling of the behaviour at the desired frequencies ($f_g$ and its SM harmonics) are far lower than the switching frequency of the DAB ($f_g \ll f_{s,DAB}$). Therefore, the switching behaviour can be neglected and an instantaneous description might suffice.

Various DAB modulation techniques are presented in [23], [24], which also presents the power for phase-shifted modulation. Equation 33 shows this relation which uses the phase shift $\phi$. The provided equation is only valid for the total unidirectional power (positive $\phi$). For bidirectional power, the in and output currents can be calculated, equations 34 and 35 respectively.

$$|P_{DAB}| = \frac{V_1 V_2 n}{f_s L_{DAB}}(\phi - 2\phi^2) \tag{33}$$

$$I_{DAB,1} = \frac{P_{DAB}}{V_1} = \frac{V_2 n}{f_s L_{DAB}}(|\phi| - 2|\phi|^2) \cdot sign(\phi) \tag{34}$$

$$I_{DAB,2} = \frac{P_{DAB}}{V_2} = \frac{V_2 n}{f_s L_{DAB}}(|\phi| - 2|\phi|^2) \cdot sign(\phi) \tag{35}$$

In the SST, there will be a parallel output connection of multiple DABs. As equal power per submodule has been assumed during the MMC model, only one submodule per leg needs to be modelled. Therefore the total low voltage current becomes the sum of the DAB model from each leg times the amount of submodules per leg. Equation 36 shows this relation. Now state that $V_1 = V_{SM}$ and $V_2 = V_{LV}$ Equation 37 gives the relation between the low voltage DC current and the voltage, assuming an RC-load on the LVDC-Bus.

$$I_{LV} = N \cdot \sum_{(a,b,c)_{p,n}} I_{DAB,2} \tag{36}$$

$$\frac{V_{LV}(s)}{I_{LV}(s)} = \frac{R_{LV} R_{C,LV} C_{LV} s + R_{LV}}{(R_{LV} + R_{C,LV}) C_{LV} s + 1} \tag{37}$$

By connecting a DAB to each submodule, $I_{DAB,1}$ will be injected into each submodule. This will lead to the submodule capacitor current according to equation 38.

$$I_{C_{SM}} = I_{SM} - I_{DAB,1} \tag{38}$$

### *E. Mathematical and Switched SST Model*

The Double-Star MMC combined with the DAB model leads to the considered SST Model. Fig. 7 shows a schematical overview of this model. The Double-Star is considered here as this model has the highest complexity. The Single-Star

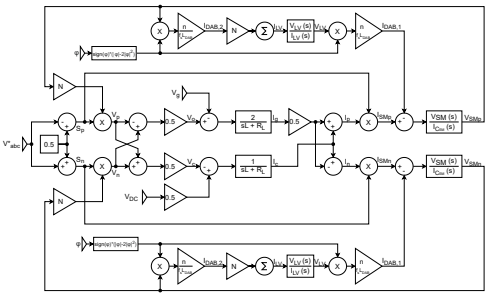

Fig. 7. Proposed Mathematical Model of the Double-Star SST

and Single-Delta models have shown similar results. [25] The mathematical model and a switched model have been implemented in PLECS [17]. Both are run independently with the same control system. To reduce the simulation speed of the switched model, the amount of submodules per arm is reduced to $N = 4$ with a grid peak voltage of $V_{g,peak} = 2.7kV$ and a total power rating of 1MW. Fig. 8 shows simulation results of a switched simulation and the proposed mathematical model plotted upon each other. This shows a clear overlap between the results of the two simulations, from which it can be concluded that the developed mathematical model is accurate.

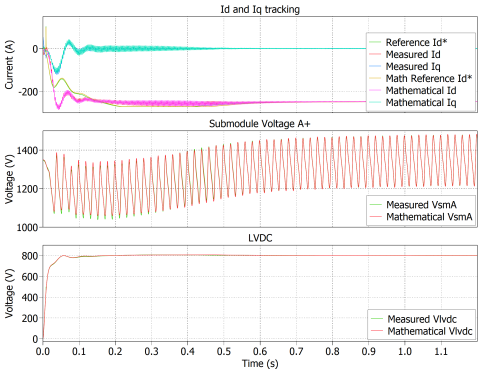


Fig. 8. Comparison of the mathematical and a switched mode

Compared to the switched model, the proposed model neglects all switching behaviour and assumes equal power per submodule, therefore it is only valid for the average behaviour using a PSC-modulation technique but it has a significantly reduced simulation time. Compared to the sub-cycle average model [8], [9], the proposed model also has a reduced simulation time. By assuming the equal power flow per submodule, scaling by N is possible, increasing the simulation speed, especially for high N. The sub-cycle average model still simulates each individual submodule but, therefore does allow different modulation techniques. The proposed mathematical model contains a very simple phase-shift-dependent DAB model, not present in the switched or sub-cycle average models, making the proposed mathematical model more suitable for fast SST simulation. Table I shows a characteristic comparison between the switched, proposed mathematical and sub-cycle average models.

## IV. Tuning of the Control System Parameters using the Genetic Algorithm

The model of the solid-state transformer can be described as a non-linear multiple-input-multiple-output (MIMO) system, therefore finding an analytical method for the tuning of the control system might not be very straightforward and an alternative is desired. When including the (inverse) Park-Clarke transforms in the model, it has the inputs $V_d^*$, $V_q^*$ and $\phi$

| | Switched | Proposed | Average |
|---|---|---|---|
| Highest Accuracy | v | x | x |
| Can model $\widetilde{V_{SM}}$ unbalance | v | x | v |
| Speed independent from N | x | v | x |
| Fast MMC Simulation | x | v | v |
| Fast DAB Simulation | x | v | x |

TABLE I
COMPARISON OF THE SWITCHED, PROPOSED MATHEMATICAL AND SUB-CYCLE AVERAGE SIMULATION TECHNIQUES FOR SSTS

with the outputs $I_d$, $I_q$, $V_{SM}$ and $V_{LV}$ (MIMO). Furthermore, this system can be described as highly non-linear, meaning that a linearised model of the system is non-representative of the system. A genetic algorithm is suitable for finding solutions to a highly non-linear system with multiple tunable parameters. [12] A switched simulation can take a matter of hours to complete a few seconds of simulation, with this such a method is not a viable solution. However as the proposed mathematical model can complete the same simulation in a matter of seconds, it can be easily implemented with the Genetic Algorithm.

Fig. 9 shows the implementation of the proposed mathematical model for the Double-Star SST as a plant in Matlab Simulink [26]. Fig. 10 shows the implementation of the control system including the plant. The Genetic Algorithm is used to

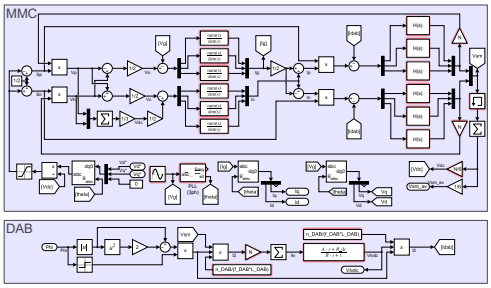


Fig. 9. Implementation of the proposed SST model in Matlab Simulink

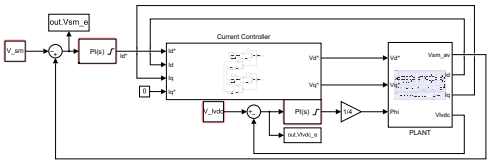


Fig. 10. Implementation of the control system in Matlab Simulink

minimise the output of equation 39. Equation 39 contains the sum of the square of all errors (SSE) over time of the four error outputs of the PLANT, multiplied by four individual weights.

$$E = W_1 \cdot e_{Vlvdc}^2 + W_2 \cdot e_{Vsm}^2 + W_3 \cdot e_{Id}^2 + W_4 \cdot e_{Iq}^2 \quad (39)$$

The Genetic Algorithm uses the 5 control parameters ($\alpha_f$, $K_{p,V}$, $K_{i,V}$, $K_{p,DAB}$ and $K_{i,DAB}$) as inputs and will try to optimise these parameters within user given ranges. Optimisation is done to minimise the output of function 39. As this algorithm gives no final solution, it requires a user-defined optimisation runtime. The Simulink model is run in parallel on four cores using the Parallel Computing Toolbox [27] in order to maximise the number of iterations for a given time. Furthermore, each time the square error is calculated it first checks if the maximum of the voltage errors does not exceed a 10% overshoot. If it does the error is replaced by a high number ($10^{32}$), ensuring the algorithm will classify this as a bad solution.

Table II shows the tuning ranges and results, using a maximum runtime of 6 hours and $W_1 = 0.25$, $W_2 = 1$, $W_3 = W_4 = 1000$.

| | Input Range | Outcome |
|---|---|---|
| $\alpha_\mathbf{f}$ | [50, 500] | 498.2 |
| $\mathbf{K_{p,V}}$ | [0.5, 500] | 15.93 |
| $\mathbf{K_{i,V}}$ | [1, 1000] | 149.5 |
| $\mathbf{K_{p,DAB}}$ | $[5 \cdot 10^{-6}, 5 \cdot 10^{-3}]$ | $8.178 \cdot 10^{-5}$ |
| $\mathbf{K_{i,DAB}}$ | $[2 \cdot 10^{-3}, 2]$ | $9.4 \cdot 10^{-3}$ |

TABLE II
GENETIC ALGORITHM CONTROL TUNING ($t = 6h$): DOUBLE-STAR SST, CONTROL SYSTEM A

The found control parameters are used in the PLECS Mathematical model. Fig. 11 shows the result SST behaviour using the automatically tuned control system parameters. The system is stable and converges to the desired values within the given time and without any undesired overshoot. The d- and q-component currents follow their references and the average submodule voltage deviation is almost negligibly small. Therefore, the genetic algorithm with the proposed mathematical model is suitable for tuning this control system.

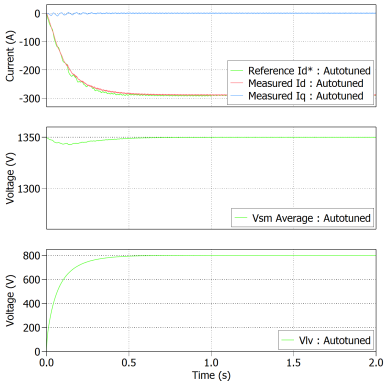


Fig. 11. System response of the Double-Star SST and its control system tuned using the Genetic Algorithm

## V. Conclusion

High-power EV Charging Applications consisting of multiple 350kW Chargers desire an MMC-based solid-state transformer (SST) to connect 800V DC to the MVAC grid. With this comes a need for fast simulations and control system tuning of the SSTs. Existing average simulation models are suitable for MMC simulation and tuning, but not for the presented SST. A novel mathematical model has been proposed, which is based on an existing MMC model, the switching function describing the average switching behaviour, and a simple phase-shift-based DAB model.

Simulating the proposed model independently, and comparing it to a switched model, shows that the proposed model can accurately determine the average behaviour. As even power per submodule is assumed, individual submodule simulation is avoided by using the number of submodules (N) as a factor, making the simulation speed independent of N. Combining this with the neglection on switching behaviour, gives a significantly faster model which can be run in a matter of seconds instead of hours (for N=12).

The reduced simulation time allows for algorithmic-based tuning methods which are suitable for non-linear MIMO systems. The Genetic Algorithm is used to tune the control system parameters. When using the found parameters in simulation, it shows desirable behaviour. Therefore, the proposed mathematical model in combination with such an algorithm is suitable for control system tuning.

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# B

# SST Mathematical Models in Simulink

# B.1. Double-Star Model

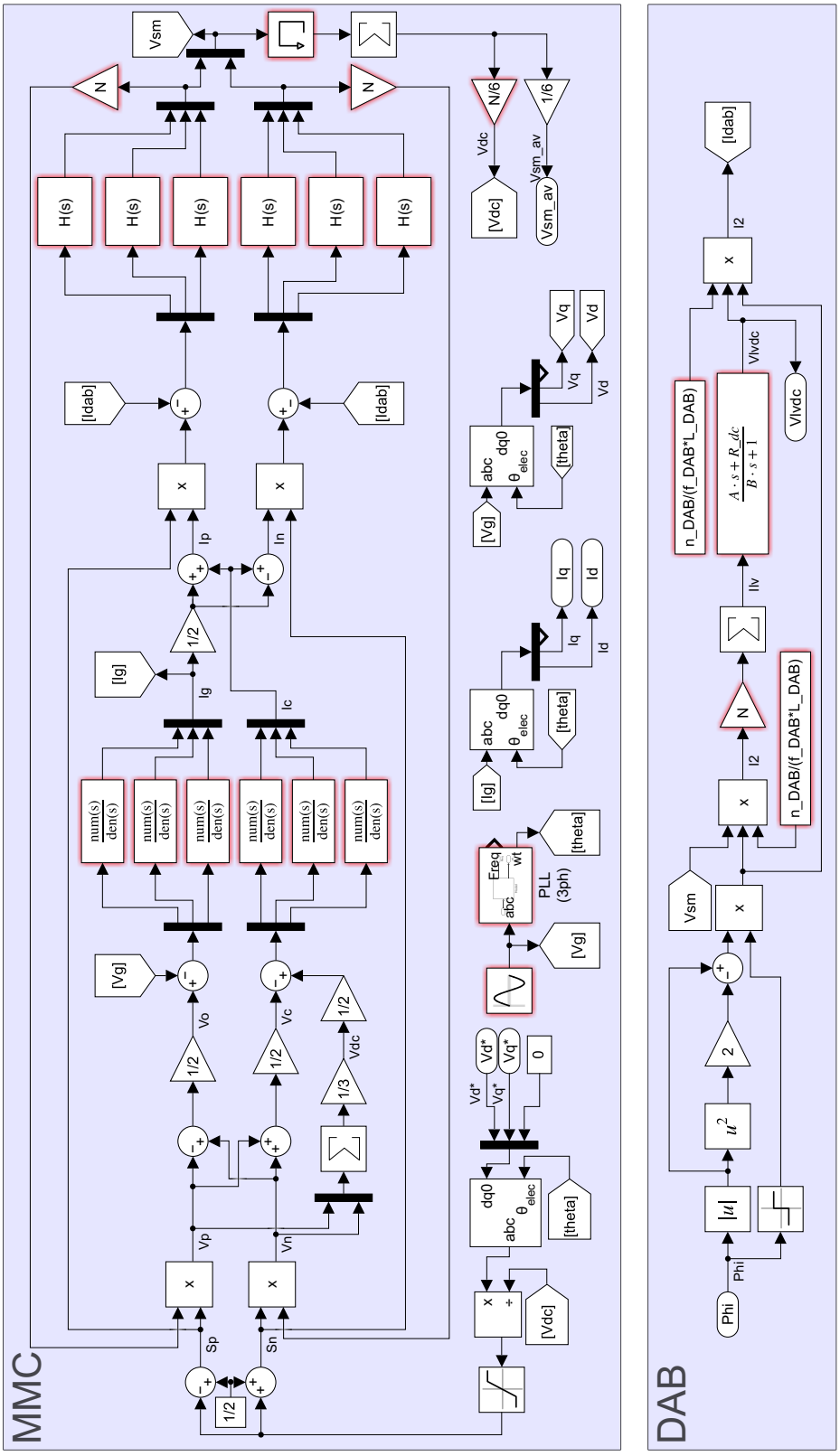



**Figure B.1:** Mathematical Model of the Double-Star SST implemented in Simulink

## B.2. Single-Star Model

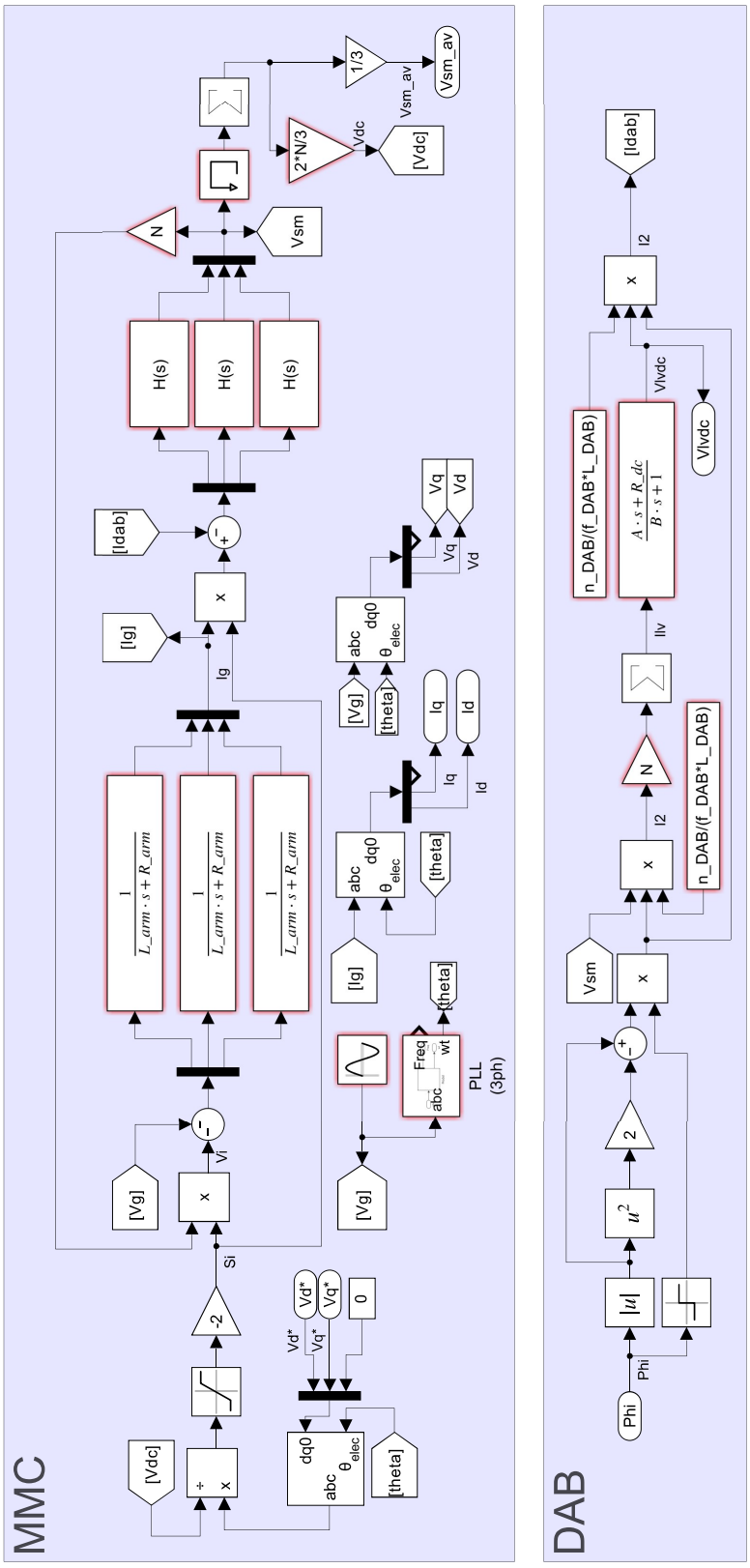



**Figure B.2:** Mathematical Model of the Single-Star SST implemented in Simulink

## B.3. Single-Delta Model

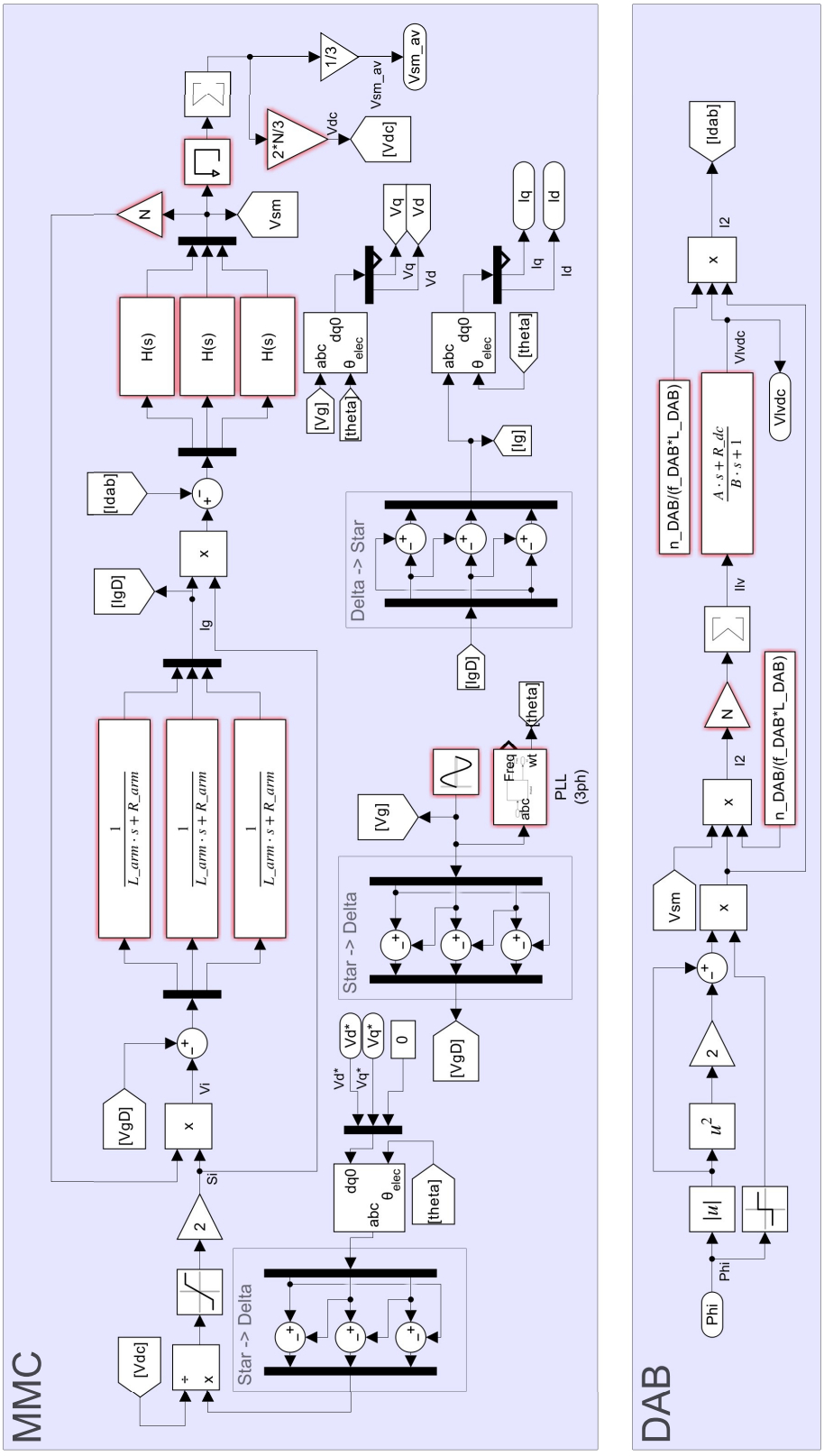



**Figure B.3:** Mathematical Model of the Single-Delta SST implemented in Simulink

# C

# 1MVA SST Simulation Results

# C.1. Double-Star SST with Half-Bridge Submodules

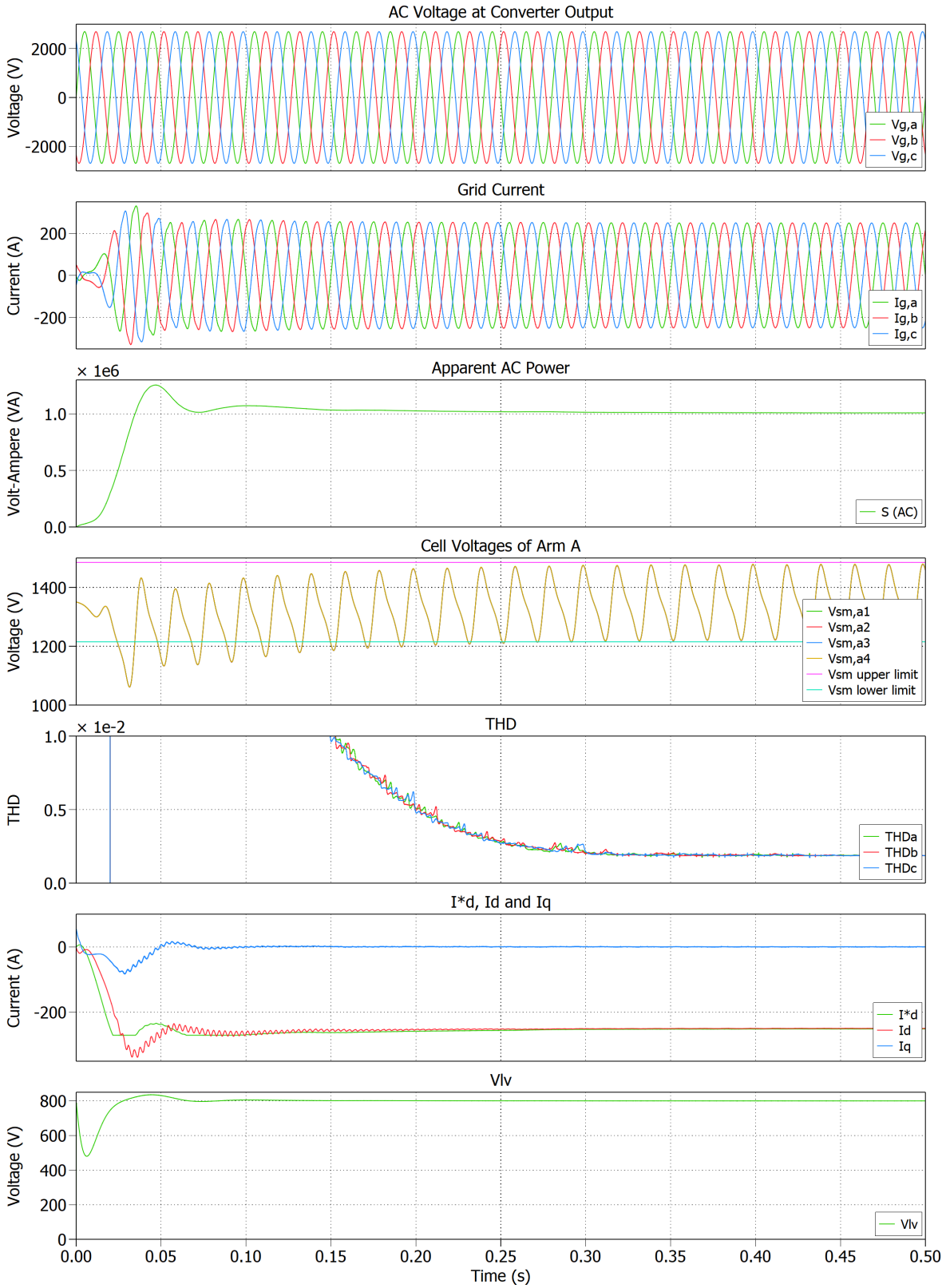



**Figure C.1:** 1MVA Double-Star Simulation with Half-Bridge Submodules

## C.2. Double-Star SST with Half-Inserted Full-Bridge Submodules

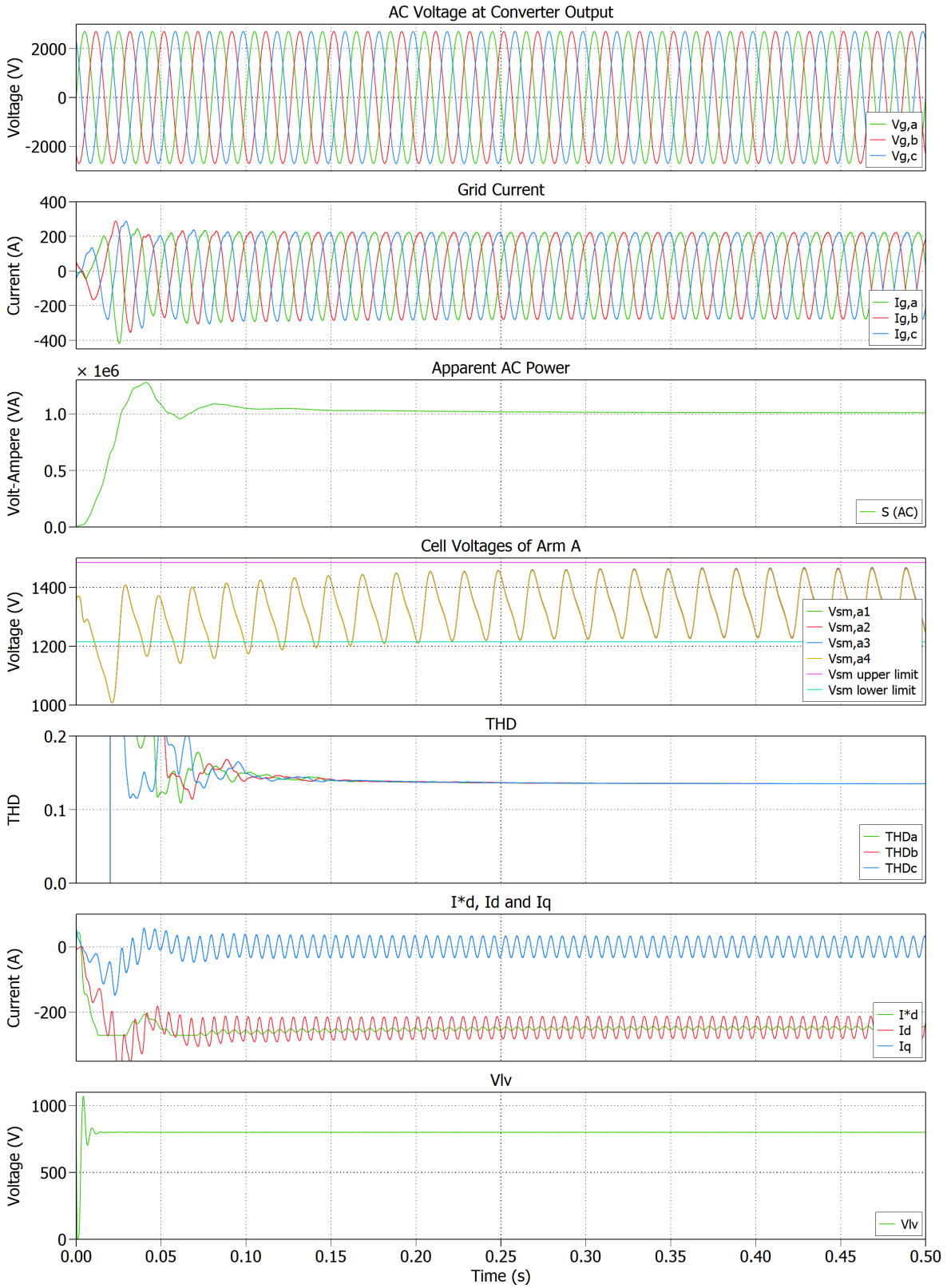



**Figure C.2:** 1MVA Double-Star Simulation with Half-Inserted Full-Bridge Submodules

# C.3. Double-Star SST with Full-Inserted Full-Bridge Submodules

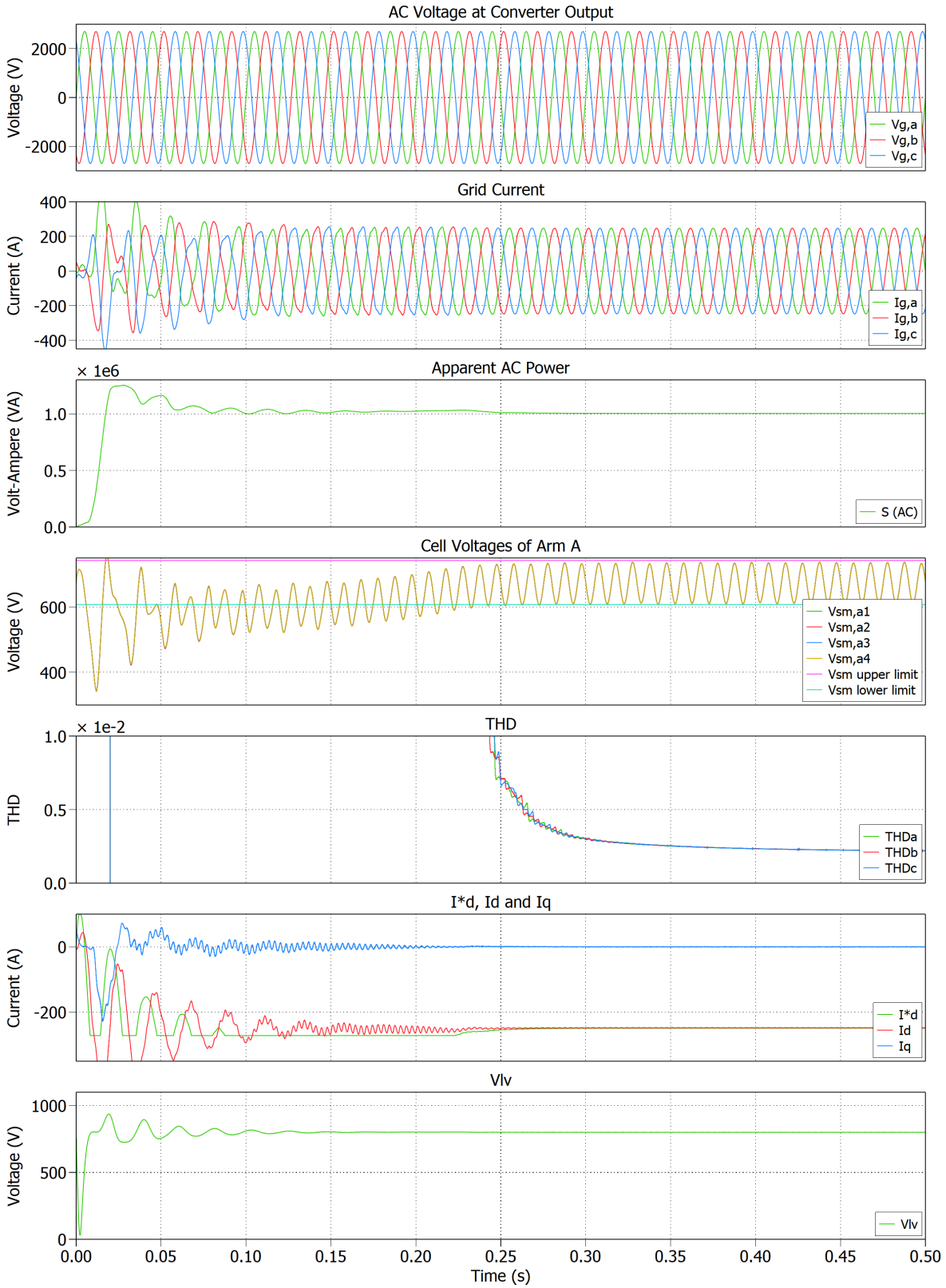



**Figure C.3:** 1MVA Double-Star Simulation with Full-Inserted Full-Bridge Submodules

# C.4. Single-Star SST with N=4

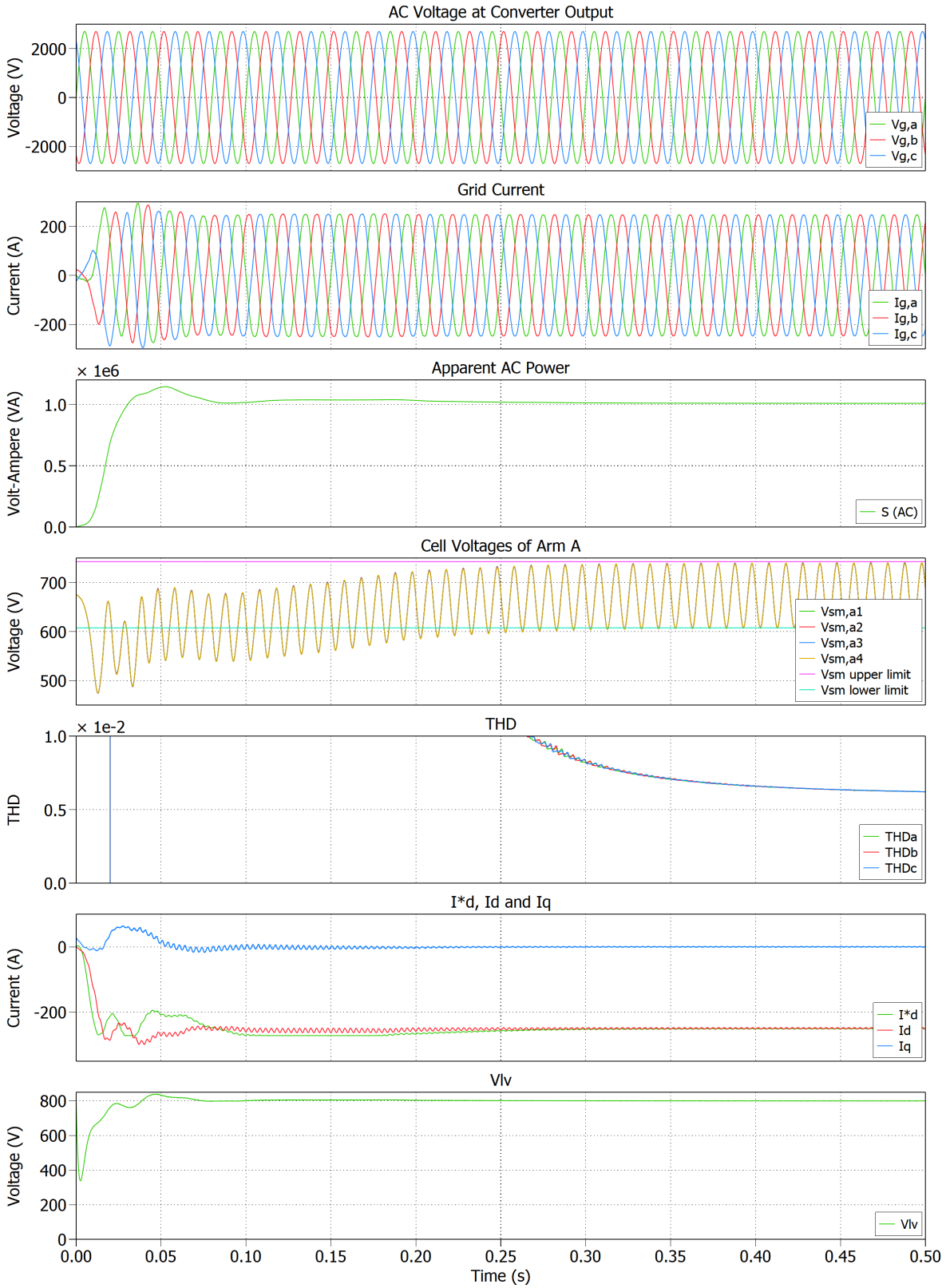



**Figure C.4:** 1MVA Single-Star Simulation with N=4

# C.5. Single-Star SST with N=2

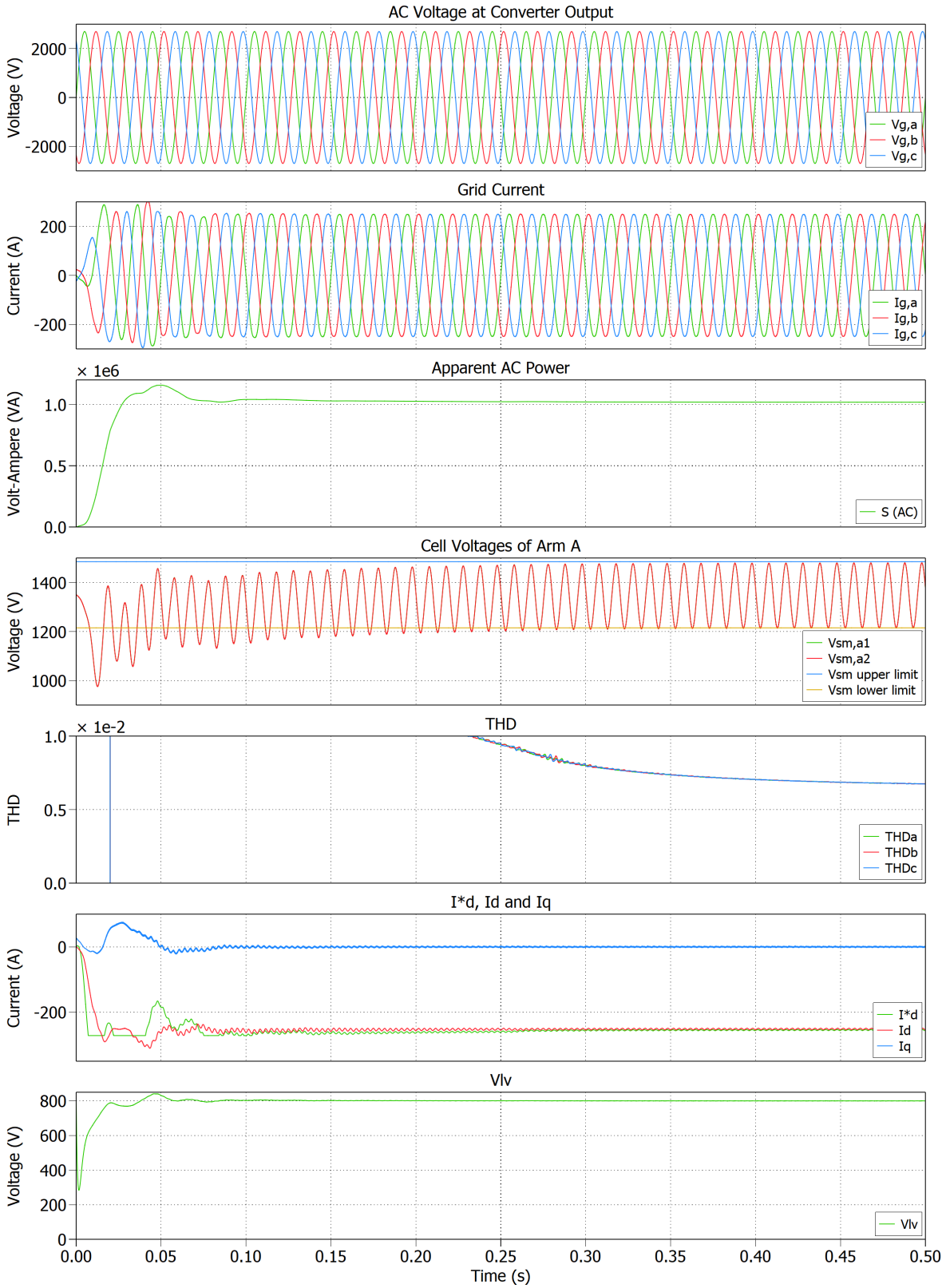



**Figure C.5:** 1MVA Single-Star Simulation with N=2

# C.6. Single-Delta SST

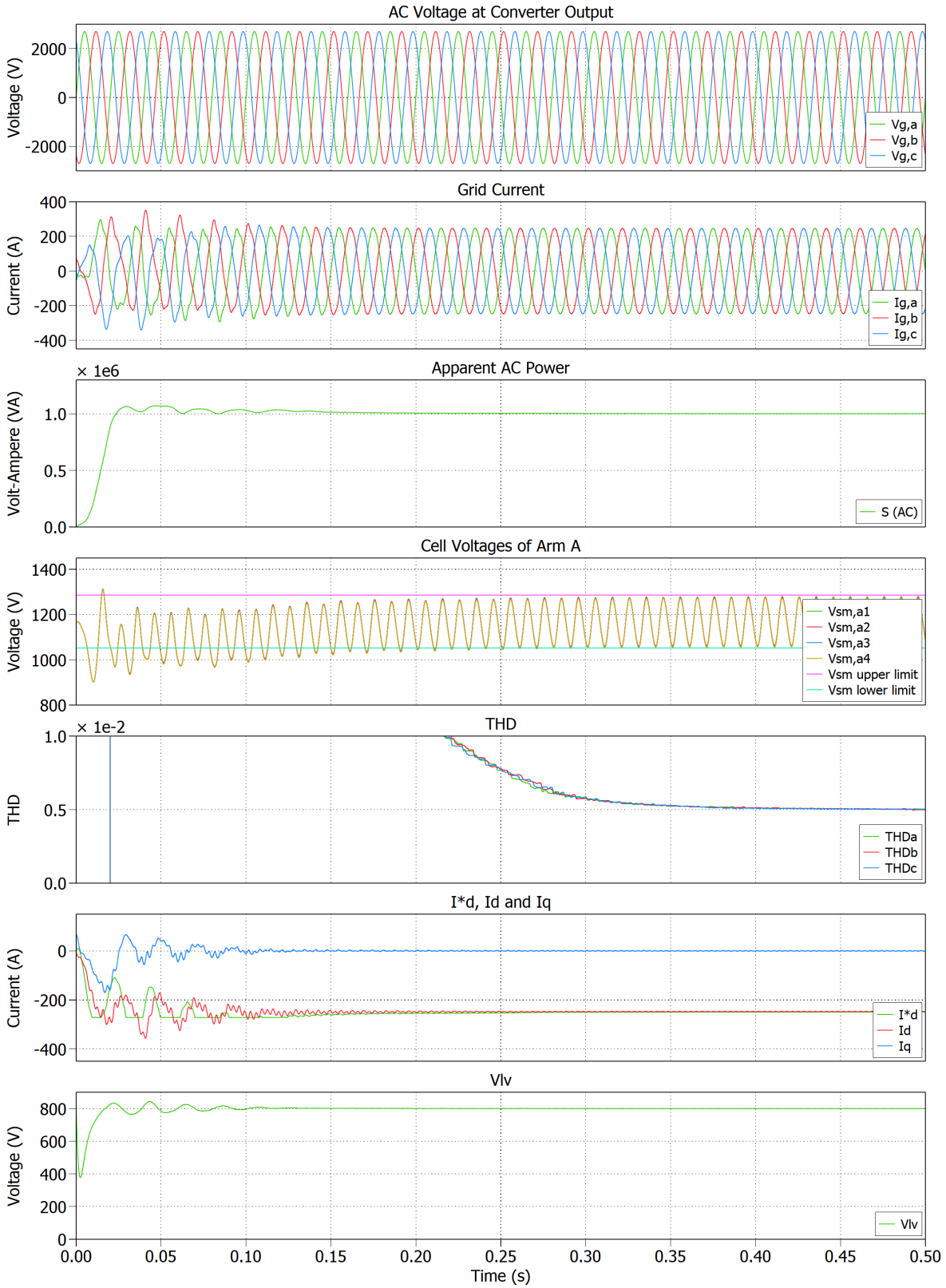
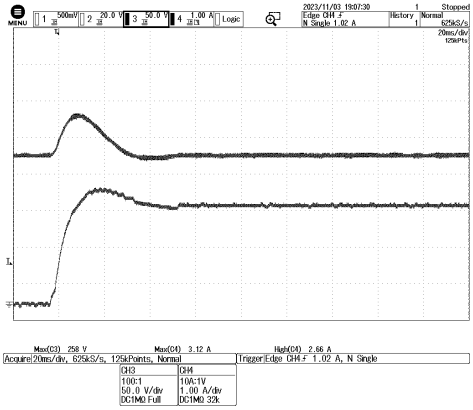


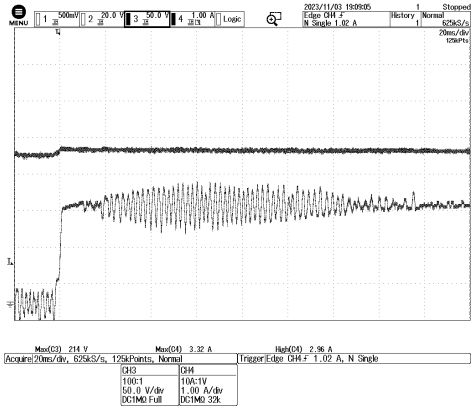

**Figure C.6:** 1MVA Delta Simulation

# D

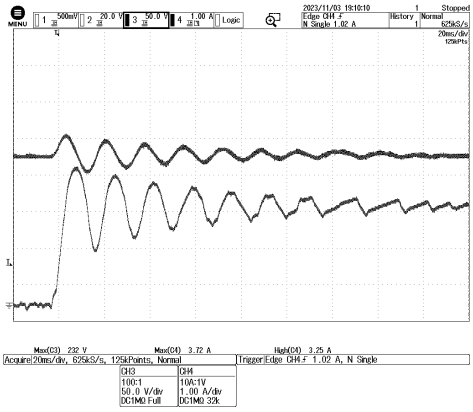
# Oscilloscope Screenshots of the Hardware DAB Current Step Test Results



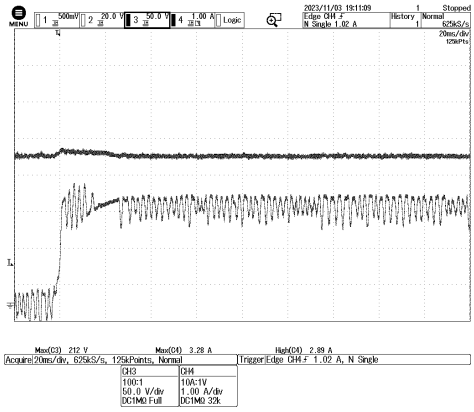
**(a)** $K_p = 0.001$, $K_i = 0.1$



**(b)** $K_p = 0.01$, $K_i = 0.1$

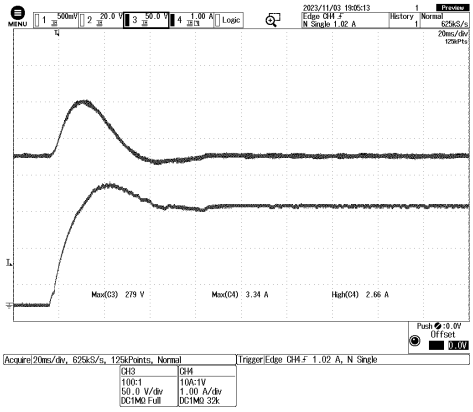


**(c)** $K_p = 0.001$, $K_i = 1$

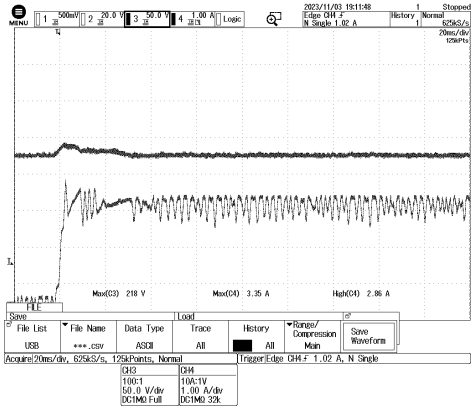


**(d)** $K_p = 0.01$, $K_i = 1$

**Figure D.1:** Current (lower signal) and Voltage (upper signal) response of the Current-Pulse test using standard PI control

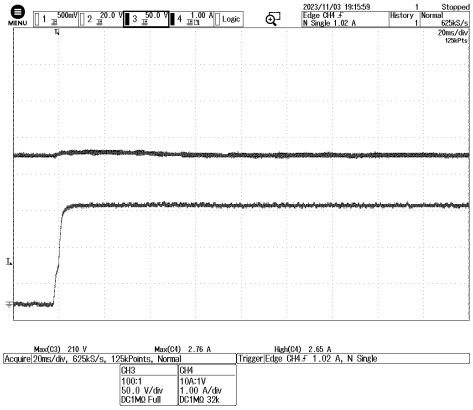


**(a)** $K_p = 0.02$, $K_i = 2$

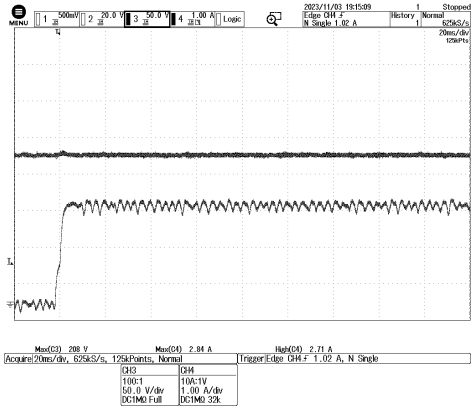


**(b)** $K_p = 0.2$, $K_i = 20$

**Figure D.2:** Current (lower signal) and Voltage (upper signal) response of the Current-Pulse test with linearised PI control



**(a)** $K_p = 0.002$, $K_i = 0.2$



**(b)** $K_p = 0.02$, $K_i = 2$

**Figure D.3:** Current (lower signal) and Voltage (upper signal) response of the Current-Pulse test using the current feedforward