Pattern transfer on a vertical cavity sidewall using SU8

2009 J. Micromech. Microeng. 19 074018

(http://iopscience.iop.org/0960-1317/19/7/074018)

J. Micromech. Microeng. **19** (2009) 074018 (6pp) doi:10.1088/0960-1317/19/7/074018

Pattern transfer on a vertical cavity sidewall using SU8

T M Verhaar, J Wei and P M Sarro

DIMES (Delft Institute of Microsystems and Nanoelectronics), Electronic Components, Technology and Materials Laboratory, Delft University of Technology, Feldmannweg 17, 2628 CT Delft, The Netherlands

E-mail: J.Wei@tudelft.nl

Received 23 December 2008, in final form 13 May 2009
Published 30 June 2009
Online at stacks.iop.org/JMM/19/074018

Abstract

In this paper, a process to realize metal lines on the sidewall of high aspect ratio cavities is developed. As an alternative to conventional photoresist, SU8 is used to define patterns on vertical sidewalls of deep cavities while maintaining compatibility with conventional IC processes. When transferring a pattern onto a 3D structure, especially the coating process, cavity filling and step coverage become important issues and require specific attention. A highly uniform SU8 coating is obtained and 20 μm wide aluminium lines across 60 μm deep cavities are realized. Problems related to overexposure and to aluminium etching are presented as well. The resistance of the aluminium structures on top, bottom and sidewall of the cavities is measured and discussed.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

With the advancement of IC and MEMS technology, more and more 3D structures with tapered or vertical sidewalls, such as mechanical structures or micro-fluidic channels have been integrated on silicon wafers. This offers great flexibility for micro-system design but, at the same time, poses many challenges for the photolithographic process, especially when patterns have to be made across different horizontal levels, or even on the sidewalls. The possibility of pattern transfer on high topography surface, such as creating electrical connections across high steps and electrodes placed on a cavity sidewall (see figure 1), can essentially improves the flexibility for MEMS design (especially for microfluidic systems), system integration and packaging.

In conventional photolithography for IC-fabrication, a UV-light source is used to expose the photoresist on the substrate planar surface in the perpendicular direction, creating patterns on the horizontal plane. Several methods have been developed to realize patterns on 3D structures. A slight tapered cavity sidewall and conventional exposure methods can be used [1]. However, the depth of the cavity is limited to several μm. For deeper (or higher) sidewalls, special methods to deposit the photoresist, such as spray coating and electrodeposition [2, 3], are developed. Exposure could be done by using a special equipment, or a mask with a diffraction pattern to bend the light to the sidewall [4].

To keep the process within the conventional photolithography, we have developed a method to pattern structures on a vertical plane which utilizes a conventional contact aligner, and requires no special or dedicated equipment. In order to do this, the photoresist, covering the vertical plane, has to be exposed completely from the top to the bottom. This requires a photoresist with a uniform absorption of UV-light energy, such as SU8. SU8 is an epoxy-based negative tone photoresist, and is mainly used for MEMS applications. Thick layers (up to several hundreds of micrometers) can be made using a single coating step, and uniformly exposed using light in the near UV region [5].

In this paper, after a brief description of the fabrication steps, the challenges that were encountered in each step are discussed. The experiments done to overcome these challenges are presented, and the optimized fabrication process is given. Finally, to validate the process some test structures for electrical measurements are designed, fabricated and measured.

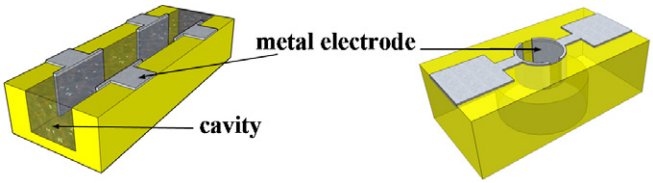


Figure 1. Electrodes placed on the vertical sidewalls of cavities.

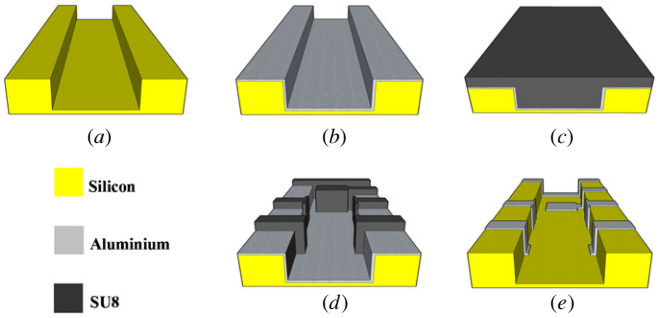


Figure 2. Schematic process flow: (*a*) cavity etching, (*b*) aluminium deposition, (*c*) SU8 coating, (*d*) SU8 exposure and development, (*e*) aluminium etching and SU8 removal.

2. Experimental details

To demonstrate the potential of SU8 for pattern transfer on vertical sidewalls, several test structures were designed and fabricated. Figure 2 shows a schematic description of the fabrication steps. First, 60 μm deep cavities are etched into the silicon substrate by deep reactive ion etching (DRIE) and a 3 μm thick aluminium layer is coated on the entire surface by RF-sputtering. Then, SU8 photoresist is applied, completely covering the high topography surface. The photoresist both in the cavities and on the wafer surface is exposed and developed. After aluminium etching, the SU8 mask can be removed. For the DRIE and aluminium sputtering steps standard recipes are used and thus these steps are not discussed in detail [6]. The other steps are individually considered and described in the following sections.

2.1. Coating and prebake

Coating a wafer with cavities presents several challenges. Not only adhesion and surface uniformity, which are important in conventional IC technology as well, but also cavity filling and step coverage are critical. An ideal coating has to completely fill the cavities, with vertical sidewalls (figure 2(*c*)), and in a uniform manner even for cavities with different dimensions. That is crucial for the later exposure step, since both air bubbles and curved SU8 surfaces will cause refraction of the UV light [7].

2.1.1. Adhesion. Adhesion influences the thickness of the photoresist layer and the photoresist wetting inside the cavity. These depend on several factors, such as the type of underlying layer, moisture and contaminations. To investigate the effect of the underlying layer, SU8 was coated on bare silicon, thermally grown silicon oxide and aluminium (sputtered at 50 and 350 °C). To avoid moisture formation, which occurs when wafer is exposed to air, a dehydration bake at a high temperature (around 200 °C) needs to be performed. Other contamination such as organic particles can be removed in a high power oxygen plasma treatment.

SU8 adheres very well to silicon oxide, while quite poor adhesion to aluminium is observed. By using a dehydration bake or plasma treatment, the adhesion to aluminium substrate is slightly improved.

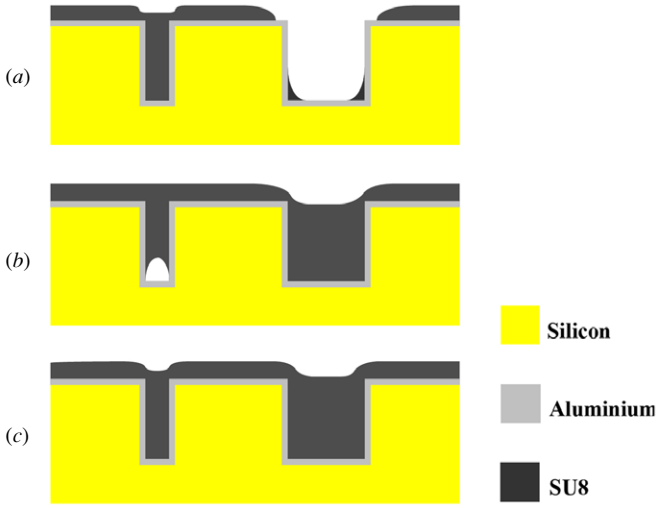


Figure 3. Coating problems encountered with high topography surfaces and variable cavity size: (*a*) low viscosity resist, (*b*) high viscosity resist, (*c*) surface non-uniformity.

2.1.2. Cavity filling and step coverage. When coating photoresist on a high topography surface with HAR structures, reliable cavity filling and good step coverage are crucial to both the lithographic process and the later etching step. Air bubbles will cause reflection and refraction of the UV-light during the exposure, and any non-continuity in the photoresist layer will later cause unwanted etching of aluminium. Both issues relate to the viscosity of the applied photoresist.

A photoresist with a low viscosity can easily reach the bottom of the narrow trenches and small cavities, giving a good filling without any air bubble. However, during wafer spinning, a large amount of the photoresist will be spun away from the wide trenches and big cavities, resulting in bad step coverage (see figure 3(*a*)). A high viscosity photoresist, on the other hand, gives good step coverage on large steps, but may trap air bubbles inside the small cavities (see figure 3(*b*)). For the above reasons, the viscosity of the phtotoresist has to be chosen carefully according to the size and shape of the structures that have to be coated.

When cavities with large differences in size have to be coated, the situation becomes more complex, since a photoresist with a certain viscosity alone cannot satisfy the requirements for all cavities. In this case, a multi-layer coating combining photoresists with different viscosities can be used.

In the experiments good step coverage was already obtained when only SU8 2025 was used to coat the wafer, with

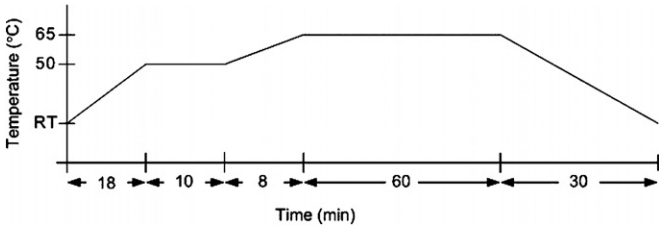


Figure 4. Experimental procedure for prebake of the SU8.

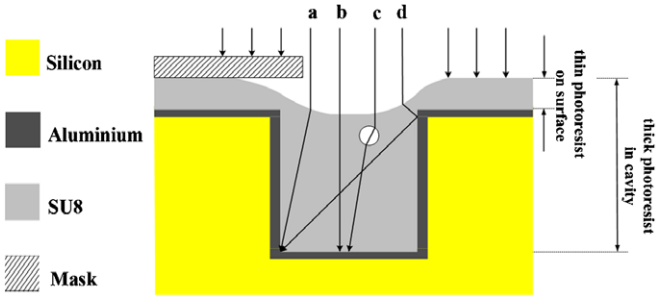


Figure 5. Refraction and reflection that may affect the SU8 exposure.

a spinning rate of 2000 rpm. However, trenches smaller than 10 μm and holes of 50 μm or smaller could not be reliably filled. A less viscous SU8 type, such as SU8 2002, gave a better filling, but after five layers the step coverage was still not good enough. A better solution was to use first a layer of SU8 2002, followed by a layer of SU8 2025. To get the best cavity filling, after the SU8 was applied, the wafer was put on a hotplate at 50 °C for 5 min before spinning. Heating the SU8 makes it less viscous, allowing better filling of the cavities.

Due to the high topography structures it will be difficult to get a uniform SU8 layer. Careful coating at low spinning rate gives the SU8 time to sink into the cavities and create a level surface.

When two layers of SU8 2002 are used before applying the SU8 2025 the surface uniformity greatly improves. Spinning of the SU8 2002 layers was done at 1500 rpm, with an acceleration of 100 rpm s^{-1}. The spinning rate of the SU8 2025 layer was slightly higher, 2000 rpm, also with an acceleration of 100 rpm s^{-1}. Heating of the SU8 2025 (30 min at 50 °C), before deposition, reduced the number of air bubbles inside the photoresist and improved the surface uniformity as well.

2.1.3. Prebake. The most important function of the prebaking step is to remove the solvent from the SU8 layer. Baking was done using a hotplate as when a convention oven is used a thin layer on the SU8 surface is quickly hardened, preventing the total evaporation of the solvent. When heating the wafer, stress is introduced, as SU8 and silicon have different coefficients of thermal expansion (CTE). To keep the stress as low as possible, baking is done at a temperature of 65 °C [8, 9] for 60 min to remove the solvent from the SU8 layer.

The other important function of the prebaking step is to enhance the reflow of the photoresist [10], since SU8 has a lower viscosity when slightly heated. Before ramping to 65 °C a 10 min stop is done at 50 °C, to improve the surface uniformity. The complete prebake heating and cooling rate is shown in figure 4.

2.2. Exposure and post-exposure bake

As the SU8 layer has different thicknesses at the planar top surface and in the cavity (bottom and sidewalls), and the energy needed to expose it depends on the thickness of the layer, attention needs to be paid to the exposure time. It has in fact to be chosen in such a way that the SU8 inside the cavities is completely exposed without too much overexposure of the SU8 on the surface of the wafer.

Another problem related to the cavities on the wafer are local non-uniformities of the SU8 layer, across the cavity opening (see figure 5). Air will introduce another refractive surface, and bend light to other regions which are not planned to be exposed (see line a in figure 5). Line b in figure 5 shows the path of the light without refraction, line c shows the refractive effect of an air bubble. Reflection of the light on horizontal surfaces will not be a real problem, but in combination with refraction it may pose problems similar to refraction, see line d.

To determine the best exposure time, a test was performed with pillar structures, which are more sensitive to exposure conditions than lines.

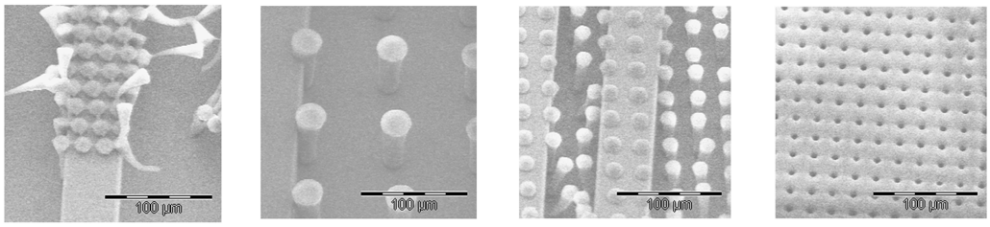
On the surface of the wafer the SU8 layer is about 20 μm thick, inside the 60 μm deep cavities the SU8 layer is 80 μm. As can be seen in figure 6, 30 s exposure time was not enough to completely expose the SU8 inside the channel. The pillar structures in the cavity were washed away during the development. An exposure time of 120 s has too much overexposure, connecting the pillars. Both 60 and 90 s look to have the same result. For 90 s, however, there will be more overexposure, especially on the planar top surface of the wafer. Another exposure experiment was done with 50 and 60 s exposure times. Although the 50 s part looked completely exposed, it peeled off more easily during developing. Based on these results an exposure time of 60 s is chosen as optimum value.

Because of overexposure, there is a limit on the minimal spacing between adjacent SU8 structures. Figure 7(*b*) shows that at ~10 μm spacing, overexposure becomes a problem, and at 5 μm spacing (figure 7(*a*)) the SU8 lines connect with each other. Figure 7(*d*) however shows that SU8 lines with different widths can be patterned successfully across trenches with different widths.

For the PEB the conditions reported in [11] are used, there a PEB time of 4 h is reported as giving the best results for a 30 μm thick SU8 layer. Such a long baking time is needed to obtain vertical sidewalls. During our experiments the PEB time was reduced to 3 h without apparent negative effects.

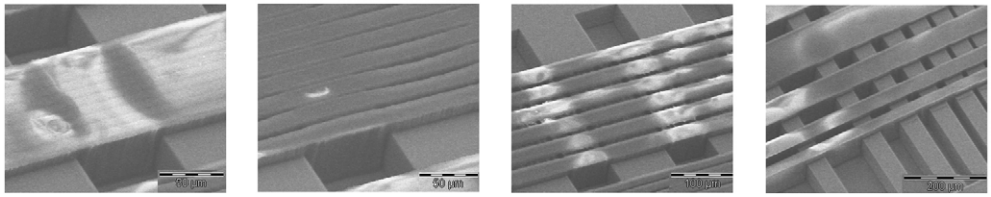
2.3. Aluminium etching and SU8 removal

Aluminium is wet etched, by using a phosphoric acid solution (770 ml H_3PO_4, 144 ml HNO_3, 140 ml CH_3COOH and



(*a*) (*b*) (*c*) (*d*)

Figure 6. SU8 pillars patterned in 60 μm deep trenches: (*a*) 30 s, (*b*) 60 s, (*c*) 90 s, (*d*) 120 s.



(*a*) (*b*) (*c*) (*d*)

Figure 7. Exposure results: (*a*) 5 μm SU8 lines, 5 μm apart, (*b*) 10 μm SU8 lines, 10 μm apart, (*c*) 20 μm SU8 lines, 20 μm apart, (*d*) SU8 lines with different width across different cavities.

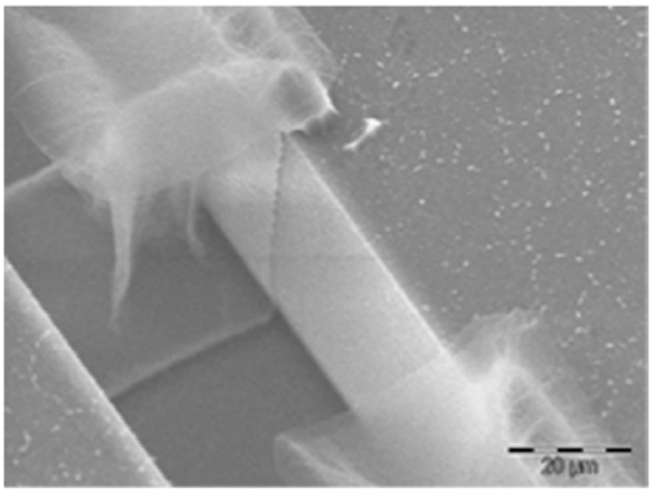


Figure 8. Thin SU8 shell left after oxygen plasma treatment.

Table 1. Process flow.

	Step	Conditions
1	Oxygen plasma treatment	30 min
2	Heating of SU8 2025	30 min at 50 °C Apply SU8 on the wafer
3	Deposit SU8 2002	Bake the wafer 5 min at 50 °C Spin 30 s at 1500 rpm
4	Repeat step 3	
5	Deposit heated SU8 2025	Spin 60 s at 2000 rpm
6	Prebake (see figure 4)	10 min at 50 °C 60 min at 65 °C
7	Exposure	60 s
8	Post-exposure bake	3 h at 65 °C
9	Development	15–20 min in the SU8 developer
10	Aluminium etch	20–25 min in Al etching solution at 35 °C
11	SU8 removal	5 min dip in 99% nitric acid 30 min oxygen plasma treatment

76 ml H_2O). To increase the etch rate the etching fluid was heated to 35 °C. An etching time of 20 min was needed to completely etch the 3 μm aluminium layer on the surface of the wafer.

There are several ways to remove the exposed SU8 from a wafer. The easiest way to remove SU8 would be to ash it in a furnace heated to 600 °C, which will give problems with the aluminium electrodes. Oxygen plasma with some additional fluorine containing gas, or oxidizing acids such as piranha etch or nitric acid, can also be used to remove the SU8.

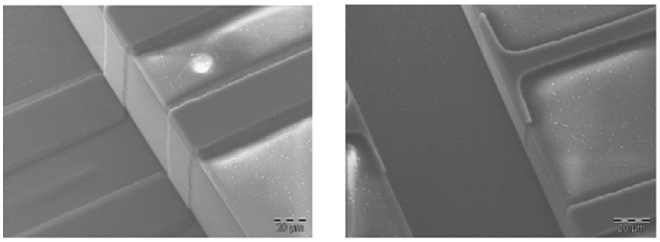
In our experiment a high-power oxygen plasma was used in a first attempt to remove the SU8. Figure 8 shows that most of the SU8 is removed, only a thin shell remained. When CF_4 or SF_6 were added to the plasma, the SU8 structures were etched from the top down. The etching rate however was slow (several hours are required to completely remove all the SU8). Alternatively a 5 min dip in a 99% nitric acid solution is used to remove most of the SU8 from the surface, followed by oxygen plasma to remove the SU8 residuals inside the cavities.

3. Result analysis and discussion

From the experiments described in the previous section, the following optimized fabrication process (table 1) was found and successfully used to realize aluminium patterns on a high aspect ration cavity sidewall. Silicon wafers with 60 μm deep cavities, ranging from 10 to 200 μm in width, coated with a 3 μm thick Al layer are used as the starting material. The duration of each major process step is indicated in table 1 as well. The total duration of the process is about 9 h. As previously mentioned the double coating process and long PEB are accountable for the longer process time.

Figure 9 shows the successfully created aluminium patterns on the vertical sidewalls. Metal lines slightly smaller than 20 μm with about 20 μm spacing are patterned. The maximum line width that was realized was about 80 μm (figure 9(*b*)).

From the performed experiments a number of observations could be made. Low adhesion between SU8 and



(*a*) (*b*)

Figure 9. Successful pattern transfer on the vertical sidewalls of DRIE etched channels: (*a*) 20 μm wide lines, 20 μm apart, (*b*) 80 μm wide sidewall electrode.

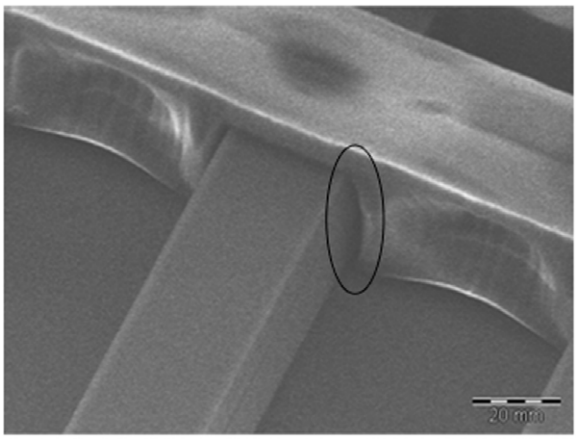


Figure 10. A slight gap between the SU8 and the sidewall (circle area) due to stress in the SU8 layer.

aluminium, together with the aluminium underetch during wet etching, causes patterns smaller than 5 μm wide to peel off. Roughening the aluminium surface, using a short dry etching step for example, may improve the adhesion.

The light used to expose the SU8 contains some wavelengths below 350 nm, light with these wavelengths are absorbed near the surface of the SU8 layer, resulting in overexposure. Limiting the spacing between SU8 structures to 15 μm, this could be lowered if a filter is used to block wavelengths below 350 nm.

After aluminium etching significant underetch was observed. During etching the resist peels off quite easily, improving the adhesion could reduce the underetch. Stress in the SU8 layer could be another reason [5]. Figure 10 shows a small gap between the SU8 layer and the sidewall, indicating that the etching fluid can reach the aluminium underneath the SU8. Using a slower temperature ramping when baking the wafer, or a different etching method may reduce this effect. The aluminium deposition method could also be the cause, at the top of the sidewall the aluminium layer could be slightly thicker, see figure 11. This will cause a shadow during exposure and the SU8 near the sidewall will be removed during developing.

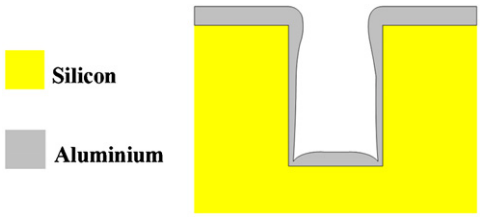


Figure 11. The aluminium thickness variation at different regions of the cavity.

3.1. Resistance measurements

To validate the process some electrical structures were designed to measure the resistance (see figure 12) on the bottom or sidewall of the cavity, or from one side of the cavity to the other.

Structures (*a*) and (*f*) are completely on the surface of the wafer and used as a reference. To characterize the aluminium layer on the bottom of the cavity, structures (*b*) and (*c*) are used, while structure (*d*) is used to characterize the sidewall. Structure (*e*) combines (*c*) and (*d*) and measures the resistance of a through cavity line. A probe station is used to send a current through the structure (from I1 to I2, see figure 12(*a*)), the resulting voltage is measured across V1 and V2, so that a precise resistance measurement can be performed by avoiding the influence of the probe contact. The cavity is 200 μm wide and 50 μm deep; the designed aluminium lines are 40 μm wide.

The measurements on structure (*a*) and (*b*) give the resistance value of $R_a = 2.7$ mΩ and $R_b = 2.9$ mΩ, respectively. Considering that the aluminium deposited on the wafer surface is 3 μm thick, this indicates that the aluminium

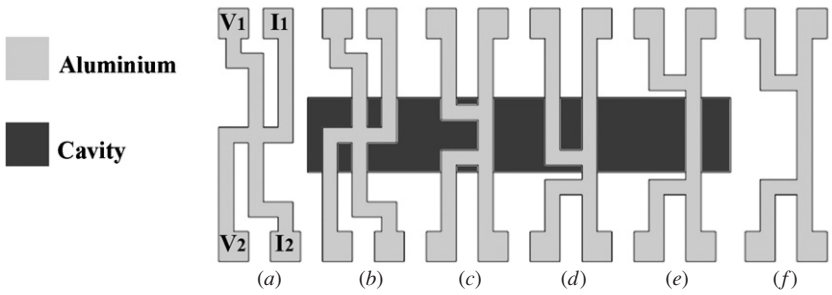


Figure 12. Resistance measurement structures, (*a*) surface square, (*b*) cavity square, (*c*) cavity line, (*d*) sidewall line, (*e*) through cavity line, (*f*) surface line.

thickness on the cavity bottom is 2.8 μm thick. The line in the cavity bottom (*c*) is measured to be $R_c = 38.6$ mΩ, while the line on the sidewall (*d*), including the top and bottom corners, is $R_d = 217.5$ mΩ. From those values, the entire line across the cavity is calculated as $R_c + 2R_d = 473$ mΩ, which is similar to the measured value 499 mΩ, from structure (*e*). The measured resistance R_d from the line on the sidewall is much larger than the resistance R_c. That is mainly due to the fact that the thickness of the sputtered aluminium layer is much thinner, especially at the bottom corner of the cavity.

4. Conclusions and recommendations

Using a modified coating process and conventional lithography, aluminium patterns were successfully fabricated on a vertical cavity sidewall. The minimal aluminium line width that could be achieved was 20 μm, on the sidewall of a 60 μm deep cavity. Resistance measurements show that it is possible to create an aluminium line going through the cavity, connecting both sides. The process has some critical steps that have been identified and discussed. Improvements can be made when the adhesion of the SU8 to the aluminium is improved and a better way to etch the aluminium is employed.

References

[1] Koch A, Evans A G R and Brunnschweiler A 1999 Design and fabrication of a micromachined coulter counter *J. Micromech. Microeng.* **9** 159–61

[2] Yu L, Lee Y Y, Tay F E H and Iliescu C 2006 Spray coating of photoresist for 3D microstructures with different geometries *J. Phys.: Conf. Ser.* **34** 937–42

[3] Schnupp R, Baumgärtner R, Kühnhold R and Ryssel H 2000 Electrodeposition of photoresist: optimization of deposition conditions of lithographic processes and chemical resistance *Sensors Actuators* **85** 310–35

[4] Nellissen T, Wang L, Wehrens R, van den Heuvel E and Weterings J 2003 *14th European Microelectronics and Packaging Conf. and Exh. (Friedrichshafen, Germany, 23–25 June 2003)* pp 347–51

[5] Lorenz H, Despont M, Fahrni N, Brugger J, Vettiger J and Renaud P 1998 High-aspect-ratio, ultrathick, negative-tone near-UV photoresist and its applications for MEMS *Sensors Actuators* A **64** 33–39

[6] Wei J, Van Der Velden M and Sarro P M 2007 *Transducers & Eurosensors The 14th Int. Conf. on Solid-State Sensors, Actuators and Microsystems (Lyon)* pp 1613–6

[7] Zhang J, Chan-Park M B and Conner S R 2004 Effect of exposure dose on the replication fidelity and profile of very high aspect ratio microchannels in SU8 *Lab Chip* **4** 646–53

[8] Chu Duc T, Lau G K and Sarro P M 2008 Polymeric thermal microactuator with embedded silicon skeleton, part II. Fabrication, characterization and application for 2 DOF microgripper *J. Microelectromech. Syst.* **17** 823–31

[9] Anhoj T A, Jorgensen A M, Zauner D A and Hübner J 2006 The effect of soft bake temperature on the polymerization of SU-8 photoresist *J. Micromech. Microeng.* **16** 1819–24

[10] Bohl B, Steger R, Zengerle R and Koltay P 2005 Multi-layer SU-8 lift-off technology for microfluidic devices *J. Micromech. Microeng.* **15** 1125–30

[11] Olivadoti C, Pham H T M and Sarro P M 2007 Vertical sidewall controlling of high viscosity SU-8 photoresist patterning using UV lithography *Proc. 18th Micromechanics Europe Workshop (Guimares)* pp 195–8