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Stress Analysis of Pressure-assisted Sintering for the Double-side Assembly of Power Module

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Abstract

Purpose: Crack and stress distribution on dies are the key issues for the pressure-assisted sintering bonding of power modules. The aim of this research is to build the relationship among the stress distributions, the sintering sequences, and the sintering pressures during the sintering processes.

Design/methodology/approach: Three sintering sequences, S(a), S(b) and S(c), have been designed for the double-side assembly of power module in this paper. Experiments and finite element method (FEM) analysis are conducted to investigate the crack and stress distribution.

Findings: The sintering sequence had significant effects on the crack generation in the chips during the sintering process under 30 MPa pressure. The simulation results revealed that the module sintered by S(a) showed lower chip stress than those by the other two sintering sequences under 30 MPa. In contrast, the chip stress is the highest when the sintering sequence follows S(b). The simulation results explained the crack generation and prolongation in the experiments. S(a) was recommended as the best sintering sequence because of the lowest chip stress and highest yield rate.

Originality/value: This study investigated the stress distributions of the double-side sintered power modules under different sintering pressures. Based on the results of experiments and finite element method (FEM) analysis, the best sintering sequence design is provided under various sintering pressures.

Keywords: Reliability, sintering, double-side assembly, power chip

1. Introduction

High-voltage power modules have achieved significant progress to meet the increasing demands and applications of power chips, such as insulated gate bipolar transistor (IGBT) and fast recovery diode (FRD) in automotive, energy transfer, and aerospace industries in the near years [1-3]. The trends to develop power chips with high voltage and high power density have posed new challenges for the assembly technology of power modules due to reliability concern [4, 5]. As one of the critical assembly processes, the die attach technology is a governing restriction to improve the reliability of the power modules.

Soldering and silver sintering are typical die attach methods for power modules [6, 7]. Soldering achieves wide applications in the assembly of low power modules because of its advantages such as high-efficiency, low-cost, and self-alignment [8-11]. However, there are three major challenges which restrict the application of soldering in the assembly of high power modules. The first one is the low creep resistance of the solder joints in high temperature environment [12]. The high service temperature of high power modules is a threat to the reliability of the solder joints. The second major challenge is the evolution of the brittle interfacial intermetallic compounds (IMC) in the solder joints [13, 14], which is considered as the leading factor for the generation and prolongation of interfacial crack in the solder joints. Besides, the electro-migration in the solder joints may be intensified in high power applications [15]. In contrast, the silver-sintered connections show better thermal stability and higher reliability than the solder joints [16, 17]. Due to reliability concern, sintering is considered as a promising method for the assembly of high power modules [18, 19].

Compared with silver bulks, silver-sintered layer shows some worse performances, such as mechanical properties, thermal conductivity and electrical conductivity. The biggest challenges for silver sintering are to decrease the porosity and to improve the comprehensive performances of the sintered layers. Youssef *et al.* (2015) demonstrated that the lifetime of nanosilver sintered power module is affected by the porosity ratio inside the sintered layer [20]. Herboth *et al.* (2013) identified that the decrease of porosity in the sintered layer greatly improved the lifetime of sintered package during thermal shock test [21]. The performances of the sintered layers can be improved by optimizing sintering parameters, sintering environment and composition of the sinter paste, etc [22]. Zhang *et al*. [23] investigated the bridging effect of Ag_2O in pressure-less silver sintering. It showed that the proper amount of additives, such as Ag_2O, facilitated the bridging connection between Ag particles, which led to microstructure densification and strength enhancement. Li *et al.* (2016) [24] and Mei *et al.* (2014) [25] indicated that the sinter joints by current-assisted or ultrasonic-assisted sintering showed significant improvement on their shear strength. Besides the pressure-less sintering, pressure-assisted sintering is another commonly-used die attach process for power modules. On one hand, the increasing mechanical pressure improves the densification rate and the strength of the sinter layer. On the other, pressure-assisted sintering shows good process stability for industrial production. The application of pressure during sintering process significantly enhances the densification of nanoparticles and thus decreases porosity of sintered interconnection (Zabihzadeh *et al*., 2015) [19]. Le *et al.* (2015) [26] used the finite element analysis method to evaluate the reliability of sintered package. It was found that the pressure-assisted nanosilver sintered package exhibited much higher thermo-

mechanical resistance to thermal swings when comparing with soldered ones. Similar results were verified by Fu *et al.* (2015) [27]. However, applying pressure aggravates the risk of crack generation in chips. Thus it is critical to control the stress in the modules by optimizing the sintering process to improve the yield of production.

As stated above, the stress distributions of the double-side sintered power modules under different sintering pressures were investigated. The power module used in this study is a press-pack structure with different geometric size substrates on the double sides of the power chips. Accordingly, there are three sintering sequence designs for this structure. The aim of this research is to build the relationship among the stress distributions, the sintering sequences, and the sintering pressures during the sintering processes. Based on the results of experiments and finite element method (FEM) analysis, the best sintering sequence design is provided under various sintering pressures.

2. Experiments

2.1 Sintering sequence design and experimental procedures

Fig.1 shows the schematic diagram of the sintering design in this research. The whole process includes two parts: the lamination of silver film onto Mo plates and the sintering process. In this study the geometric dimension of the top Mo plate is smaller than that of the bottom Mo plate. Thus three different sintering sequences can be designed for the double-side sintering process. In sintering sequence (a), the power chip is sintered onto the bottom Mo plate, and then the top Mo plate is sintered onto the chip with the bottom Mo plate. Fig.1 (b) shows another possible sintering sequence. Here the top Mo plate is sintered onto the chip at first. Then, the chip with the top Mo plate is

sintered onto the bottom Mo plate. Compared with the sintering sequence (a) and (b), there is a more simple sintering method, a one-step process, which is shown in Fig.1 (c). The bottom Mo, the chip, and the top Mo are put into the sintering tool in sequence, and then they are sintered in one step. In this paper we use S(a), S(b), and S(c) to represent the sintering sequence (a), (b), and (c), respectively.

The sintering process is conducted by a pressure sintering equipment as shown in Fig.2 (a). Before the sintering process, the Ag film is laminated to the Ag-coated Mo layer at 130 ℃ under 5 MPa for 2 mins. Fig.2 (b) and (c) show the morphology of the surface of the Mo layer before and after being laminated. The power chip used in this study is the dummy Si chip with Ag coated on the surfaces as shown in Fig.2 (d). The sintering process is conducted at 250 ℃ under 30 MPa for 3 mins. Fig.2 (e) shows the morphology of the well-sintered samples.

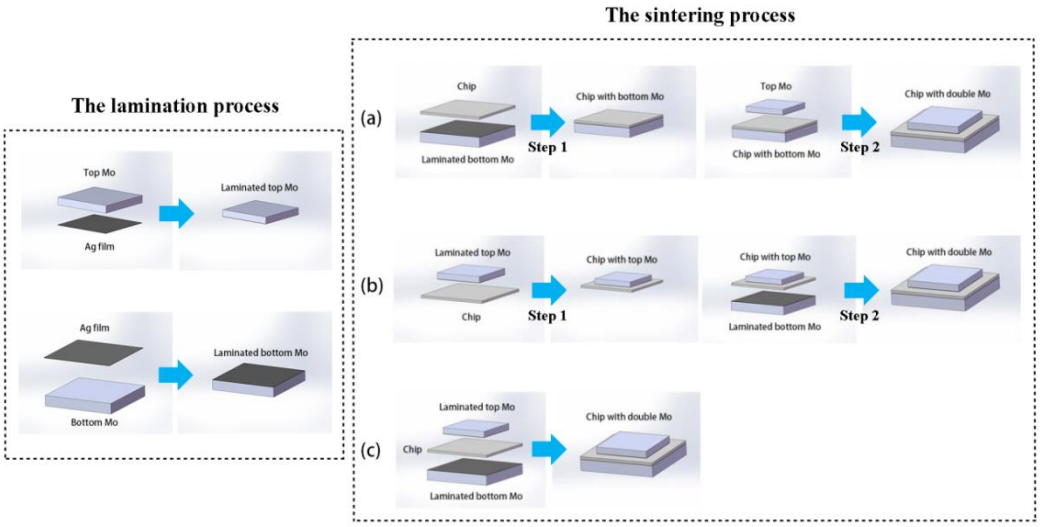

Fig.1 Schematic diagram of the sintering procedures by sequence (a), (b), and (c)

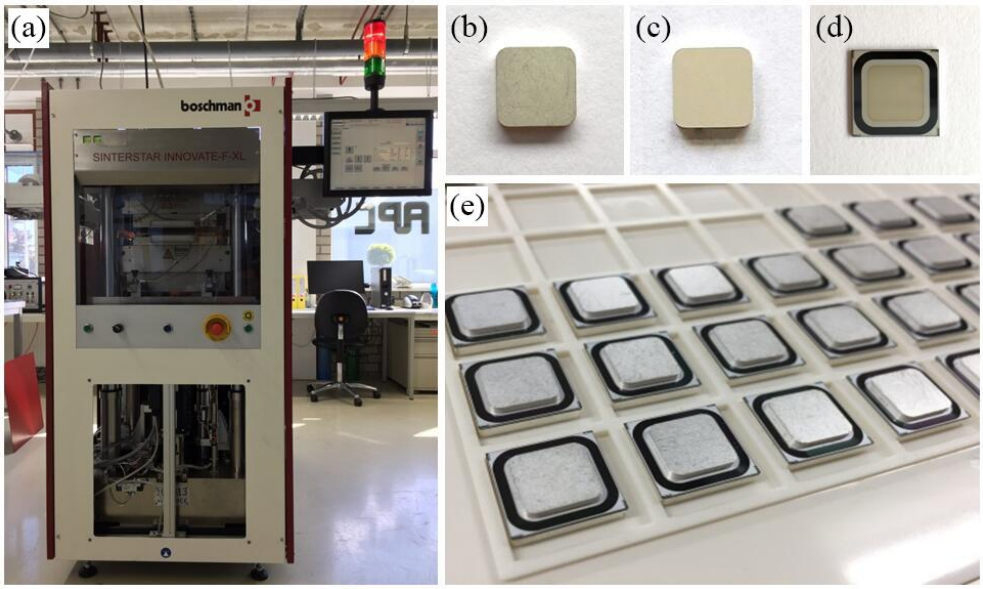

Fig.2 Sintering equipment and specimens: (a) Boschman pressure-assisted sintering equipment, (b) Mo layer, (c) laminated Mo layer, (d) power chip, (e) sintered samples

2.2 Yields of the samples by different sintering sequences

The morphology of the sintered samples under 30 MPa sintering pressure can be observed in Fig.3. As shown in Fig.3 (a), the power chip is sintered onto the bottom Mo plate in the first sintering procedure by S(a). Fig.3 (b) shows the double-side sintered sample after the second sintering procedure by S(a). No cracks appeared in the modules during both the two sintering procedures by this sintering sequence. Fig.3 (c) shows the sintered chip with the top Mo plate in the first sintering procedure by S(b). In the second sintering procedure, the sample as shown in Fig.3 (c) is sintered onto the bottom Mo plate. The double-side sintered sample is as shown in Fig3 (d), in which clear cracks can be observed in the power chip. The typical distribution of cracks in the samples by S(b) is as described in the schematic diagram in Fig.3 (e). As shown in Fig.1 (c), S(c) is a one-step sintering process, during which both the top and the bottom Mo plates are sintered onto the power chip simultaneously. According to the experimental results, there is not any crack on most of the samples by S(c) as shown in Fig.3 (f), while the others appear

cracked chips as presented in Fig.3 (g). Fig.3 (h) shows the schematic diagram describing the crack prolongation in Fig.3 (g).

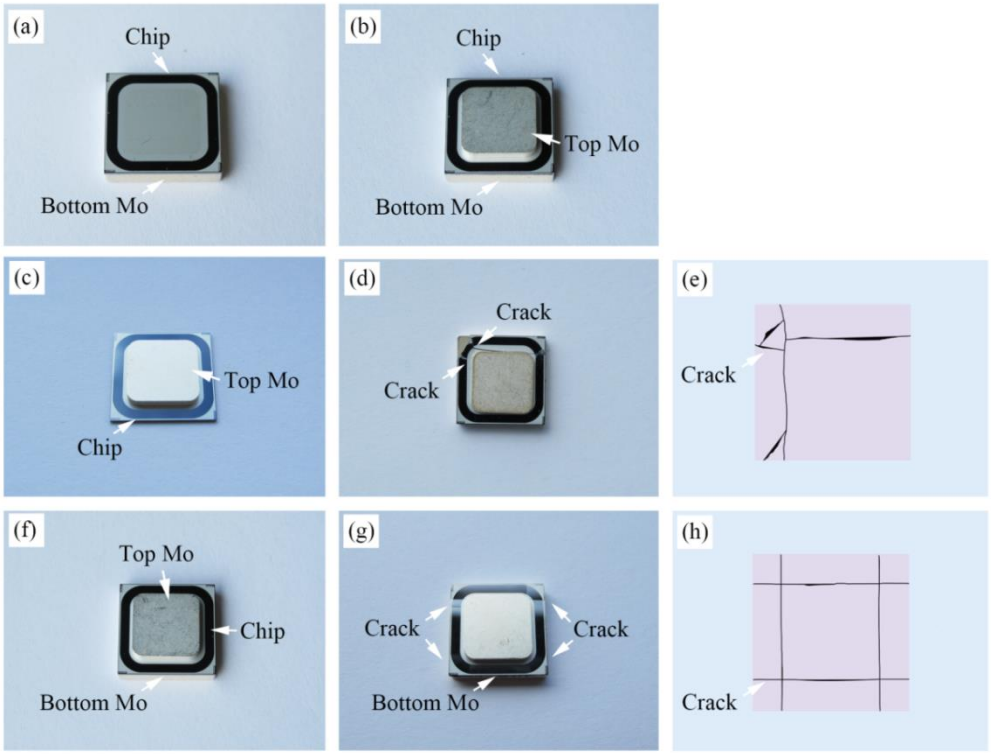

Fig.3 Morphology of the sintered samples under 30MPa by different sintering sequences: (a) chip with the bottom Mo by S(a), (b) the double-side sintered sample by S(a), (c) chip with the top Mo by S(b), (d) the double-side sintered sample by S(b), (e) schematic diagram describing the cracks in (d), (f) good sample by S(c), (g) sample with cracks by S(c), and (h) schematic diagram describing the cracks in (g)

Tab.1 The yield of the samples by different sintering sequences

Sintering sequence	Number of samples	Number of samples with crack	Yield
(a)	459	0	100%
(b)	9	9	0
(c)	9	2	78%

The numbers of the cracked samples by different sintering sequences are listed in Tab. 1. Firstly, every sintering sequence involved nine samples. It was found that all of the nine samples by S(b) showed cracked chips. Two chips broke during the sintering process by S(c). In contrast, no crack appeared in the chips sintered by S(a). Thus this

sintering sequence is used for the batch production of the double-side sintering of the power chips and 450 more samples were sintered. The results show that the yield of this sintering process is 100% for all the 450 samples.

For S(a), the chip and bottom Mo have already joined together and formed one new part in the first sintering process. In the second sintering process, the applied pressure on top Mo will uniformly distributed on the bottom Mo and will not introduce too much stress into the chip. However, for S(b), the silver film between the joined top Mo/chip and the bottom Mo shows low elastic modulus. Also the bottom surface of the chip is unconstrained on the bottom Mo. Therefore, the pressure applied on the top Mo will cause high stress concentration on the chip at the lower corner area of top Mo and lead to the generation of cracks. For S(c), both the top and bottom surfaces of the chip are unconstrained, this gives more flexibility for the deformation of chip and results in lower stress than S(b).

According to the experimental results, we can draw some conclusions as follow:

1. All the cracks appear in the chips which is the weakest part in the power module.

2. For the two-step sintering sequences of S(a) and S(b), no crack generates after the first sintering process.

3. All the cracks appear during the sintering process at 250 ℃ under 30 MPa instead of the cooling process.

It is of great significance to investigate the stress distribution in the samples during the sintering processes, and then to take the stress as a standard to design the sequence of the sintering processes under various sintering pressures.

3. Finite element analysis

3.1 FEM model and material properties

FEM method is used to analyze the stress distribution in the samples by different sintering sequences under various sintering pressures (0, 10, 20, and 30 MPa). The 3D FEM model of the power module is built and shown in Fig.4. Tab.2 lists the geometric parameters and the material properties of each part of the module. Here the size of the top Mo layer is 9.4 × 9.4 × 1.2 mm, which is smaller than the chip and the bottom Mo layer. Accordingly, the length and the width of the Ag film between the top Mo and the chip is 9.4 mm equally, while the thickness of this film is only 20 μm. Likewise, the Ag film between the chip and the bottom Mo layer has a similar dimension of 13.6 × 13.6 mm in length and in width.

As discussed above, no chip damages appeared during the first sintering steps by S(a) and S(b). Meanwhile, the residue stress is limited in the modules after the first sintering steps by S(a) and S(b). Therefore, the simulation works in this study mainly focus on the second sintering steps of S(a) and S(b). By this means, the simulation works are significantly simplified. A simple model as shown in Fig.4 can be used for the second steps sintering for S(a) and S(b), as well as the one-step sintering process of S(c). The major differences among these sintering sequences are supposed to be the Young's modulus of the up and the down Ag films in the models. The sintering film used in this study is mainly formed by Ag nanoparticles and the Young's modulus of the film is very low before sintering process. Literature reported [28] that the Young's modulus of nanoscale Ag film was 2.64 GPa at the temperature of 120 ºC, and 1.58 GPa at the temperature of 150 ºC. Based on the data provided, the Young's modulus of the laminated Ag film was set as 0.5 GPa during the sintering process at 250 ºC.

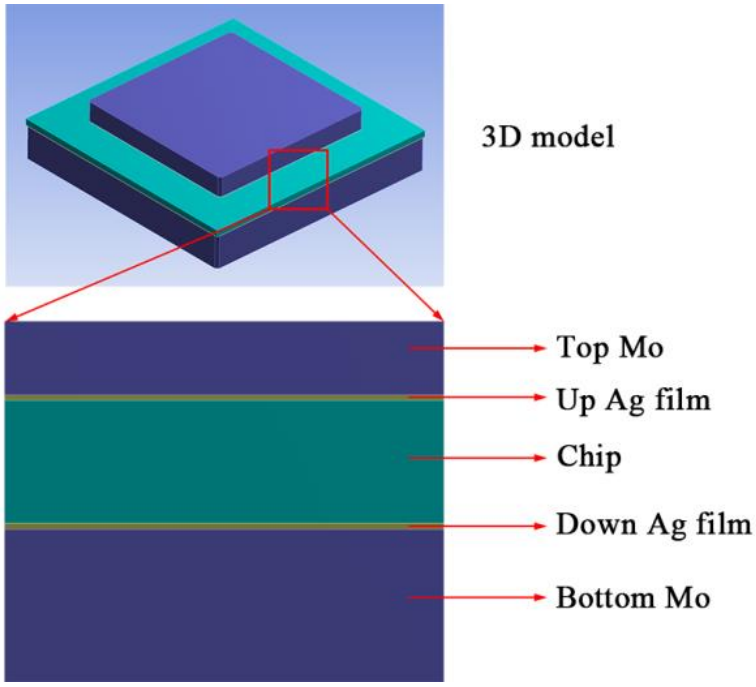

Fig.4 3D model of the double-side sintering module

Tab.2 Geometrical size and material properties of each layer [24, 25]

Layer	Length (mm)	Width (mm)	Thickness (mm)	Poisson's ratio	Young's modulus (GPa)	CTE (C^{-1})
Top Mo	9.4	9.4	1.2	0.28	320	5.0×10^{-6}
laminated Ag	9.4	9.4	0.02	0.25	0.5	2.03×10^{-5}
Chip	13.53	13.53	0.41	0.28	131	4.2×10^{-6}
Sintered Ag	13.6	13.6	0.02	0.25	23 °C, 32 100 °C, 22 200 °C, 32 250 °C, 6.02	2.03×10^{-5}
Bottom Mo	13.6	13.6	2.0	0.28	320	5.0×10^{-6}

The Garofalo model [29] was applied for describing the creep properties of sintered Ag layer which has been sintered once, and it can be expressed as:

$$\dot{\varepsilon} = \mathrm{A} \cdot [\sinh(\alpha \cdot \sigma)]^n \cdot exp\left(\frac{-E_a}{R \cdot T}\right) \quad (1)$$

where $\dot{\varepsilon}$ represents the steady state creep rate, σ represents the stress (MPa), R represents the universal gas constant and T represents the temperature (K), A, α, n, E_a are constants and can be defined in Tab. 3.

In the model by S(a), the up Ag film was laminated Ag and the Young's modulus was set as 0.5 GPa. Meanwhile, the down Ag film was sintered Ag and the Young's modulus was summarized in Tab. 2 during the second sintering process. In contrast, the up Ag film was sintered Ag and the down Ag film was laminated Ag by S(b). For the one step sintering process of S(c), however, both the up and the down Ag films were laminated Ag. The Young's moduli for both of them were given to be 0.5 GPa during the sintering process.

Tab. 3 Garofalo model parameters

Material	A (s^{-1})	α (MPa^{-1})	n	E_a ($kJ\ mol^{-1}$)
Sintered Ag	0.12	0.25	0.9	55.04

The sintering temperature was set as 250 ºC and the sintering time was 3 min. After sintering, the module was cooled down to room temperature within 3 min. The sintering pressure was applied to the top Mo layer uniformly, and the pressure was set as 0, 10, 20, and 30 MPa, respectively. The pressure was only applied during sintering at 250 ºC. In order to simplify the simulation model, some assumptions are proposed as following:

1. Only stress distribution is taken into account when the max stress appears in the modeling. Thus some transformation like the Young's modulus, CTE, and geometric size of the laminated Ag layers are neglected during the sintering process.

2. The thin-coated Ag layers on the surfaces of Mo layers are neglected in the

models.

3. The residue stress, which is limited in the one-side sintered module during the first sintering process of S(a) and S(b), is also neglected.

3.2 Von Mises stress distribution under 30MPa pressure

Fig.5 (a) shows the 3-D view describing the von Mises stress distribution in the double-side sintering model by S(a) at 250 ºC under 30 MPa sintering pressure. The top view, the bottom view, and the cross sectional view of the module can be observed in Fig.5 (b), (c), and (d), respectively. It is remarkable that the maximum von Mises stress in the whole module is 115 MPa, which is located on the bottom Mo layer. The stress in the up Ag layer is similar to that in the down Ag layer, as shown in Fig.5 (d).

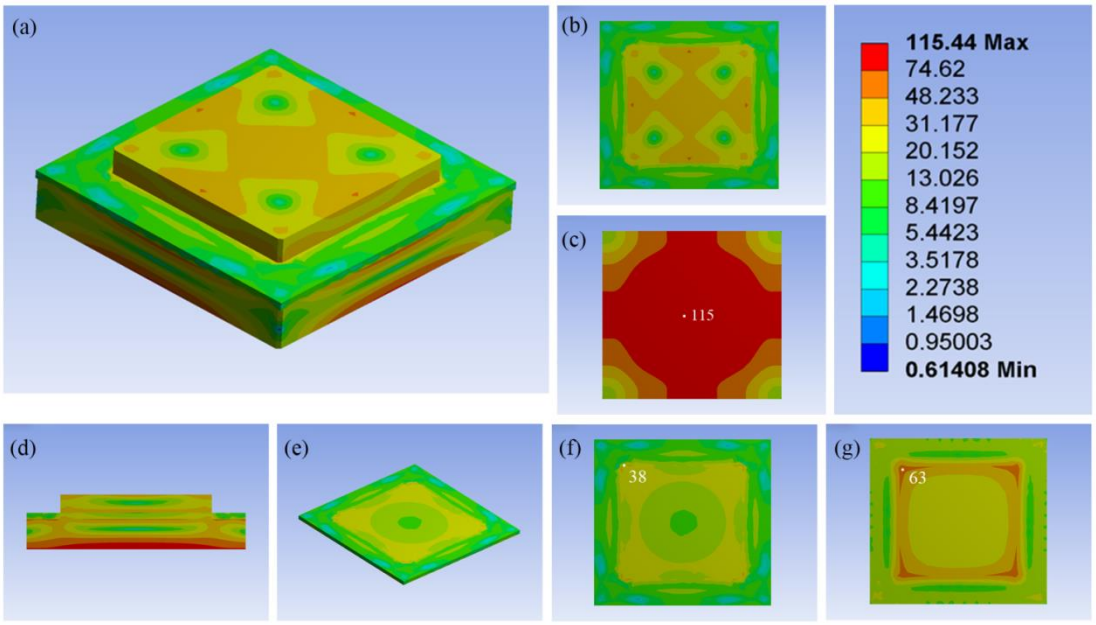

Fig.5 Von Mises stress distribution in the model with 30 MPa by S(a). (a) the 3-D view of the model, (b) the top-view of the model, (c) the bottom-view of the model, (d) the cross-sectional view of the model, (e) the 3-D view of the chip, (f) the top-view of the chip, and (g) the bottom-view of the chip

Because the weakest part in the whole module is suggested to be the chip, more attention should be paid to the stress on the chip than that on the other parts in the

module. Fig.5 (e) shows the stress distribution on the chip. The top view and the bottom view of the chip can be seen in Fig.5 (f) and (g), respectively. As presented in the figures, the maximum von Mises stress on the chip is 63 MPa, which is located on the bottom surface of chip, and the corner area of the corresponding up Ag layer. According to the experimental tests, no damages appear in these layers.

Fig.6 shows the von Mises stress distribution in the double-side sintering model by S(b) at 250 ºC under 30 MPa sintering pressure. In contrast to S(a), the up Ag layer is first sintered with top Mo layer in the model by S(b). Meanwhile, the down Ag layer is the laminated layer whose Young's modulus is 0.5 GPa. As presented in Fig.6 (d), the maximum von Mises stress in the module by S(b) is 211 MPa, which appears in the corner areas of the up Ag layer.

The stress distribution on the chip in this model can be seen in Fig.6 (e), (f), and (g). The maximum von Mises stress is 152 MPa on the top surface of the chip. It is observed that the points with maximum von Mises stress are located in the corners where the chip is connected to the up Ag layer. Consequently, the high stress concentration on the chips leads to the generation and prolongation of the cracks during the sintering process by S(b) as shown in Fig.3 (d) and (e).

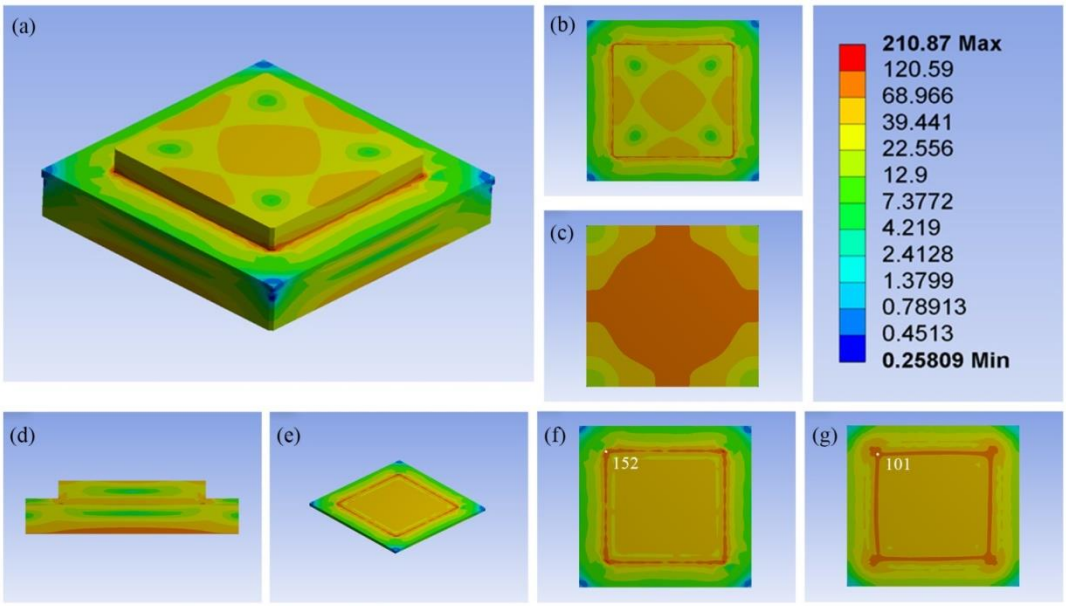

Fig.6 Von Mises stress distribution in the model under 30 MPa by S(b). (a) the 3-D view of the model, (b) the top-view of the model, (c) the bottom-view of the model, (d) the cross-sectional view of the model, (e) the 3-D view of the chip, (f) the top-view of the chip, and (g) the bottom-view of the chip

The von Mises stress distribution in the double-side sintering model by S(c) at 250 ºC under 30 MPa is shown in Fig.7. In this one step sintering process, the Young's modulus of both the up and the down Ag layers is 0.5 GPa. As presented in the figure, the maximum von Mises stress is 129 MPa which is located on the bottom Mo layer. Meanwhile, as shown in Fig.7 (e), (f), and (g), the maximum von Mises stress on the chip is 85 MPa in this model. The stress concentration areas are mainly located on the back side of chip, and the areas where correspond to the edges of the up Ag layer. As shown in Fig.3 (g) and (h), the experimental results certify that the cracks mainly generate and propagate along the stress concentration areas by S(c).

Among the three sintering sequences, the module sintered by S(a) under 30 MPa pressure shows the lowest von Mises stress of 63 MPa on the chip. In contrast, the stress on the chip reaches 152 MPa by S(b), which is the highest in the three sequences.

Meanwhile, the maximum von Mises stress on the chip by S(c) is about 85 MPa under the same simulation conditions. It is obvious that the simulation results reach a proper agreement with the experiments. The simulation results of the stress on the chips reflect the possibility of the crack generation on the chips in the experiments. Thus, the stress on the chip is considered as an index for the sintering sequence design under various sintering pressures.

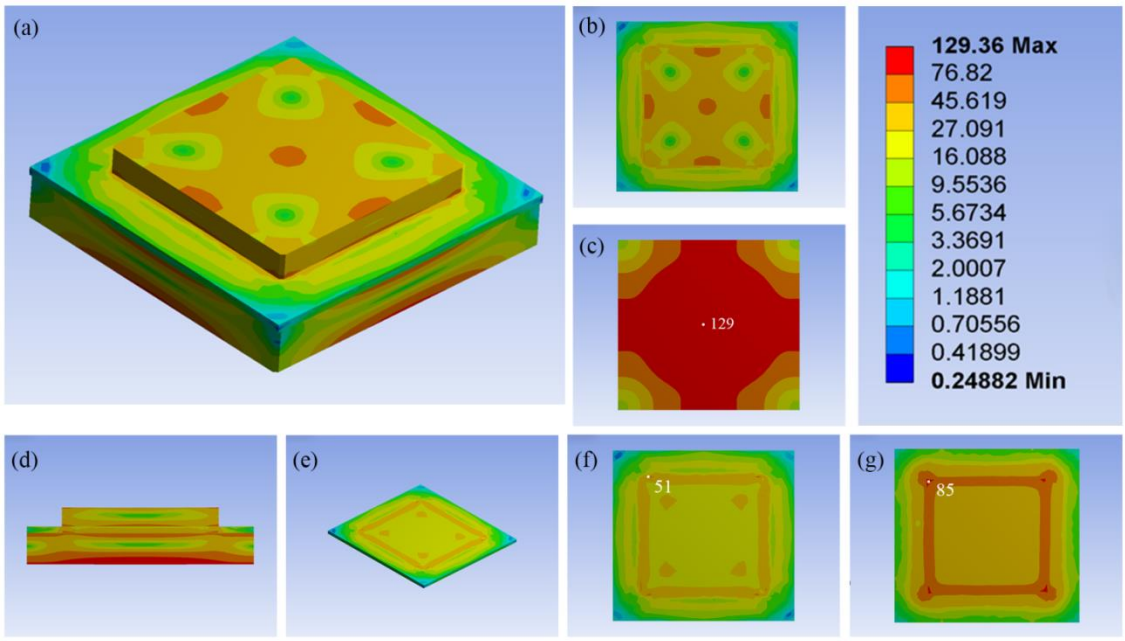

Fig.7 Von Mises stress distribution in the model under 30 MPa by S(c). (a) the 3-D view of the model, (b) the top-view of the model, (c) the bottom-view of the model, (d) the cross-sectional view of the model, (e) the 3-D view of the chip, (f) the top-view of the chip, and (g) the bottom-view of the chip

3.3 The effect of sintering pressure on the stress distribution

The stress distribution in the modules was simulated with various sintering sequences and pressures. The maximum von Mises stress for each sintering condition is shown in Tab.4. Because chip is the weakest part in the module, it is vital to concern the maximum von Mises stress on the chip during the sintering process. Fig.8 presents the maximum von Mises stress on the chips under various sintering conditions. As indicated

in the figure, the chips show much higher maximum von Mises stress by S(b) than by the other two sintering sequences. The chips by S(a) shows the lowest maximum von Mises stress among all the three sintering sequences. With the increase of sintering pressure from 0 to 30 MPa, the maximum von Mises stress on the chips by all the three sintering sequences increase. Although the one step sintering of S(c) is the most effective process, it will induce higher stress on chip and thus bring more risks to the reliability of chip when comparing to S(a). Thus, S(a) is highly recommended for the double-side sintering process.

Tab.4 Maximum von Mises stress in the modules and on the chips

Pressure (Mpa)	**Sintering order**	**Maximum von Mises stress (MPa)**	**Location**	**Stress on chip^{up} (MPa)**	**Stress on chip^{down} (MPa)**
0	a	47	Down Ag layer	27	28
0	b	47	Up Ag layer	30	30
0	c	28	Chip	26	27
10	a	47	Down Ag layer	24	38
10	b	94	Up Ag layer	69	49
10	c	45	Bottom Mo	25	41
20	a	78	Bottom Mo	28	51
20	b	151	Up Ag layer	111	76
20	c	87	Bottom Mo	36	63

30	a	115	Bottom Mo	38	63
30	b	211	Up Ag layer	152	101
30	c	129	Bottom Mo	51	85

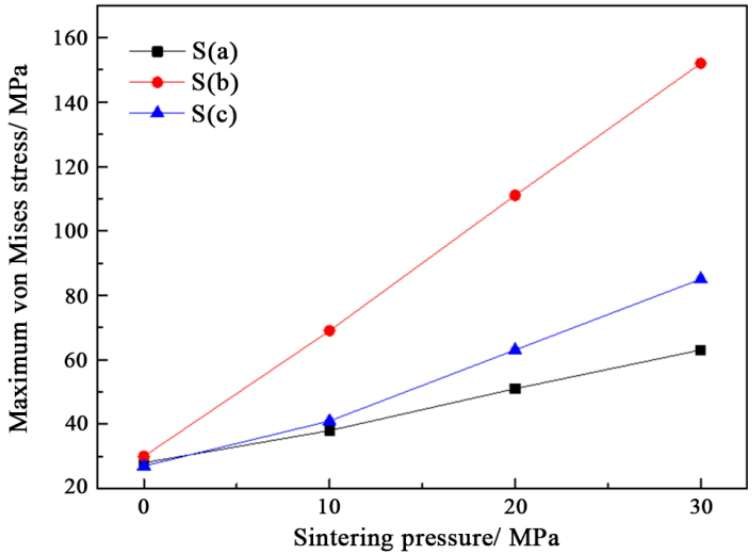

Fig.8 Effect of sintering pressure on the maximum von Mises stress on the chips

4. Conclusions

1. The chip, where cracks may generate during the pressure-assisted sintering process, is the weakest part in the double-sintered module. Designing proper sintering sequences is positive to suppress the generation of cracks.

2. When the sintering pressure is 30 MPa, the chip sintered by S(b) shows the highest von Mises stress. In contrast, the chip that sintered by S(a) showed the lowest von Mises stress.

3. The increase of the sintering pressure (0 to 30 MPa) elevates the maximum von Mises

stress on the power chips for all the modules by different sintering sequences. Moreover, the maximum von Mises stress on the chip by S(a) shows the lowest stress level.

4. Combining the test results and simulation results, S(a) is recommended as the best sintering sequence because of its high yield rate and lowest von Mises stress on the power chip.

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