Investigation of textured c-Si wafers for application in silicon heterojunction solar cells

Spyridon Alivizatos

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Graduate
Spyridon Alivizatos
MSc Sustainable Energy Technology
Faculty of Applied Sciences
spyaliv@gmail.com

Supervisors
Dr. R.A.C.M.M van Swaaij
ir. D. Deligiannis

Examination Committee
Prof. dr. M. Zeman
Dr. W.A. Smith
Dr. R.A.C.M.M van Swaaij
ir. D. Deligiannis

Delft University of Technology
Department of Electrical Sustainable Energy
Photovoltaic Materials and Devices

TU Delft Delft University of Technology

PVMD Delft University of Technology

to my family.

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Abstract

The hydrogenated amorphous/crystalline silicon (a-Si:H/c-Si) heterojunction (SHJ) solar cell is considered a great competitor of the most commercialized homojunction c-Si solar cells while it combines the high performance and the low cost potential of c-Si and a-Si technologies, respectively. Furthermore, the implementation of thin intrinsic (*i*) a-Si:H film between the c-Si wafer and the *p/n* doped a-Si:H layers has increased even more the high efficiency potential of the SHJ solar cell due to the excellent surface passivation of c-Si. By applying a randomly textured wafer instead of a double-side polished, optical enhancement is achieved resulting in significant reflection reduction and high short-circuit current densities (J_{SC}). However, texturing-induced defects lead to an a-Si:H/c-Si interface with higher recombination which limits the open circuit voltage (V_{OC}) of the SHJ device after using the same cleaning treatment as for the flat wafer. Thus, a one-to-one transfer of process parameters from flat to textured c-Si substrate is not necessarily appropriate and a different wet-chemical treatment needs to be developed.

Random pyramidal texturing is commonly achieved by chemical anisotropic etching in potassium hydroxide (KOH) or sodium hydroxide (NaOH) and isopropyl alcohol (IPA). Since an a-Si:H/c-Si interface of high quality is of great importance, etching solution based on tetramethyl ammonium hydroxide (TMAH) of low concentration due to its high cost, is used as an alternative for avoiding contamination from K^+ and Na^+ metal ions. Afterwards, investigation for the development of an appropriate wet-chemical treatment of the textured substrate prior to a-Si:H layer deposition is realized.

This thesis reports a texturing recipe consisting of low concentration TMAH and IPA which provides a pyramidal morphology with an average reflectance ($R_{350nm-1100nm}$) of 11.8% at the wavelength range of 350 nm-1100 nm. The reproducibility and homogeneity of the textured surface are confirmed by using scanning electron microscopy (SEM) along with reflectance measurements. Subsequently, a wet-chemical treatment of the pyramidal surface involving multiple oxidation steps in 69% nitric acid (HNO_3) solution at 110^{o}C is developed and leads to high a-Si:H/c-Si interface lifetime measurements. Finally, the textured substrate and the newly developed treatment prior to the a-Si:H layer growth result in the fabrication of textured SHJ devices with efficiencies above 18% due to the significant improvement of the V_{OC}, highlighting the efficiency of 19.5% mainly thanks to the considerable achievement of a V_{OC} of 680 mV which is similar to the V_{OC} measured on SHJ solar cells with flat substrate.

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Nomenclature

Abbreviations

AM	air mass
BSF	back surface field
DI	deionized
DTF	deposition time for flat wafers
EIA	U.S. Energy Information Administration
EQE	external quantum efficiency
FZ	float zone
IEA	International Energy Agency
IS	integrating sphere
ITO	indium tin oxide
NAOC	nitric acid oxidation cycle
PV	photovoltaic
PECVD	plasma enhanced chemical vapour deposition
PVMD	photovoltaic materials and devices
PVD	physical vapour deposition
RCA	Radio Corporation of America
RF	radio frequency
RT	room temperature
SC	standard cleaning
SEM	scanning electron microscopy
SHJ	silicon heterojunction
SR	spectral response
STC	standard test conditions
TCO	transparent conductive oxide

TEM	transmission electron microscopy
UHV	ultra high vacuum

Symbols

a	absorption coefficient, (m^{-1})
a	lattice constant, (m)
c	speed of light in vacuum, ($m \cdot s^{-1}$)
Δp	excess minority carrier (holes) concentration, (m^{-3})
E_g	energy band gap, (eV)
E_{ph}	energy of a photon, (eV)
Φ	photon flux, (photons $m^{-2} \cdot s^{-1}$)
FF	fill factor, (-)
G	photogeneration rate of charge carriers, ($m^{-3} \cdot s^{-1}$)
η	efficiency, (-)
θ_i	angle of incident light, (degrees)
θ_r	angle of reflected light, (degrees)
θ_t	angle of refracted light, (degrees)
h	Planck's constant, (eV·s)
i	imaginary unit, (-)
I_0	initial intensity of incident light, ($W \cdot m^{-2}$)
$I(x)$	light intensity a distance x in the wafer, ($W \cdot m^{-2}$)
J_{mpp}	current density at maximum power point , ($A \cdot m^{-2}$)
J_{SC}	short circuit current density, ($A \cdot m^{-2}$)
κ	extinction coefficient, (-)
λ	light wavelength, (m)
μ_n	electron mobility, ($m^2 \cdot V^{-1} \cdot s^{-1}$)
μ_p	hole mobility, ($m^2 \cdot V^{-1} \cdot s^{-1}$)
v	light frequency, (s^{-1})

$\tilde{n}$	complex refractive index, (-)
n	refractive index, (-)
$P(\lambda)$	spectral irradiance, ($W \cdot m^{-2} \cdot m^{-1}$)
P_{in}	incident power, (W)
$P_{deposition}$	amorphous silicon layers deposition pressure, (bar)
P_{max}	maximum power output, (W)
q	elementary charge, (C)
R	recombination rate, ($m^{-3} \cdot s^{-1}$)
R	reflectance, (-)
R_D	diffuse reflectance, (-)
R_P	shunt resistance, (Ω)
R_S	series resistance, (Ω)
R_T	total reflectance, (-)
$R_{350nm-1100nm}$	Average reflectance at the wavelength range 350 nm-1100 nm, (-)
$R(\lambda)$	Spectral reflectance, (-)
σ_L	conductance, (S)
T	transmittance, (-)
T_D	diffuse transmittance, (-)
T_T	total transmittance, (-)
$T_{substrate}$	temperature of the substrate during amorphous silicon deposition, (°C)
τ_{bulk}	bulk lifetime, (s)
τ_{eff}	effective carrier lifetime, (s)
τ_{flash}	decay time constant of the Sinton flash lamp, (s)
$\tau_{surface}$	surface/interface lifetime, (s)
V_{mpp}	voltage at maximum power point, (V)
V_{OC}	open circuit voltage, (V)
W	wafer thickness, (m)

Chapter 1

Introduction

1.1 Solar Energy field & Development of PV technologies

The continuously growing global energy demand, the imminent depletion of fossil fuels and the prevention of climate change and global warming have created the urgent need for the implementation of renewable energy sources that can be replenished constantly and naturally. Among wind energy, hydropower, geothermal energy, biomass and solar energy, the last one is the most promising energy source candidate. Solar energy is the cleanest and most abundant renewable energy source available today. Every hour the Earth receives from the Sun enough energy to cover the entire planet's energy needs for one year [1]. This energy relation is projected by the International Energy Agency (IEA) in *Figure 1.1*.

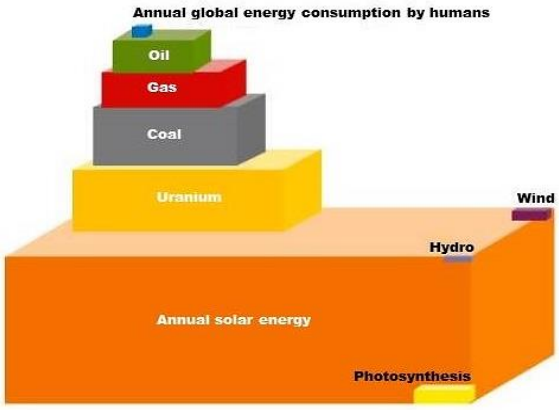


Figure 1.1: The annual energy received from the sun (orange) is roughly 10000 times as much as all the energy that humans consume on the planet annually (blue on the top). The annual solar energy is compared with the total estimated resources of oil (green), gas (red), coal (grey) and uranium (yellow) highlighting the abundance of the amount of energy provided by the sun [1].

The sun offers mankind virtually unlimited energy potential. The annual amount of energy received from the sun far surpasses the total estimated fossil resources, including uranium

fission. It also minimizes the yearly potential of renewable energy deriving from solar energy: photosynthesis (biomass), hydro power and wind power.

Solar energy can be tapped in many ways, which should be combined to best fulfill the energy needs of the global population and economy. However, this thesis focuses only on the photovoltaic (PV) devices or else solar cells which are a simple and elegant method of harnessing the sun's energy. They are unique in that they directly convert the incident solar radiation into electricity, with no noise, pollution or moving parts, making them robust, reliable and long lasting. The major obstacle of using solar energy for terrestrial electricity generation has been a much higher price of the solar electricity when compared to the price of electricity generated from the traditional sources. Therefore, there has been much effort in the field of solar cells to reduce the price of solar electricity to a level that is comparable to the conventional electricity [2].

After the first solar cell was demonstrated in silicon (Si) 55 years ago the cost has declined by a factor of nearly 200, and high-throughput mass-production compatible processes are omnipresent all over the world. At present, PV wafer based c-Si dominates in the current production with more than 90% globally [3]. c-Si solar cell technology represents today not only single crystalline silicon wafer-based solar cells, but also multi-crystalline silicon solar cells. Both technologies that deal with “bulk” c-Si are considered ***the first generation*** solar cells for terrestrial applications (see *Figure 1.2*).

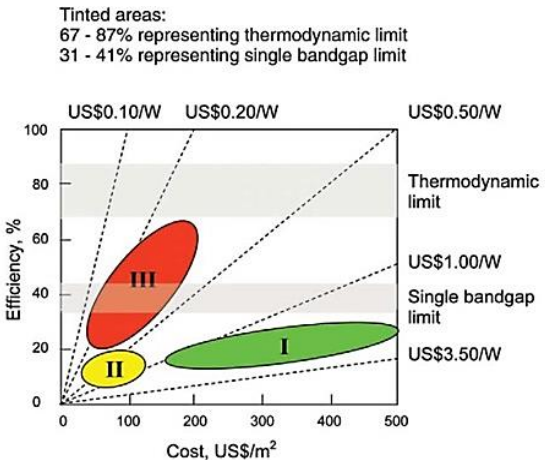


Figure 1.2: The three generations of solar cells presenting the cost-efficiency relation in each case [2].

However the challenge of developing a PV technology to a cost competitive alternative for established fossil-fuel based energy sources remains enormous and new cell concepts based

on thin films of various types of organic and inorganic materials are entering the market. In order to decrease the material costs of c-Si solar cells, research has been directed to develop low-cost thin-film solar cells, which represent ***the second generation*** solar cells. There are several semiconductor materials that are good candidates for thin-film solar cells, namely hydrogenated amorphous silicon (a-Si:H), copper indium gallium diselenide (CIGS), cadmium telluride (CdTe) and solar cells based on organic materials which are showing fast progress but the conversion efficiency still remains low for terrestrial applications [2]. Finally, there have been approaches which aim at applying innovative concepts to conventional materials and manufacturing ultra-high efficiency solar cells via advanced materials. Solar cells based on these concepts and processes are referred to as ***the third generation*** and are under research.

So, although solar energy represents a tiny fraction of the world's current energy mix, it appears to have the most rapid growth in global electricity generation for the period 2010-2040 according to the U.S. Energy Information Administration (EIA) [4]. Around the world, countries and companies are investing in solar generation capacity on an unprecedented scale, and, as a consequence, costs continue to fall and technologies improve.

1.2 Solar energy conversion into electricity

1.2.1 Solar Radiation

The Sun emits energy in the form of electromagnetic radiation consisting of a mixture of electromagnetic waves which are characterized by certain wavelength (λ) and frequency (v) depending on the region of the spectrum that correspond. Alternatively, quantum mechanics describes electromagnetic radiation as packets of energy which are called photons. These elementary particles have a discrete amount of energy for each wavelength, defined in *Equation 1.1*, where h is Planck's constant and c is the speed of light in vacuum. It is obvious that there is an inverse relationship between the energy (E_{ph}) and the wavelength of a photon, meaning the shorter the wavelength, the higher the energy of the photon.

$$E_{ph} = hv = \frac{hc}{\lambda} \tag{1.1}$$

1.2.2 Electrical properties of a semiconductor

The energy emitted from the Sun can be harnessed due to the electrical properties of the semiconductor materials that compose solar cells. These properties differentiate semiconductors from metals and insulators and can be illustrated using electronic band structures which reflect the potential energy levels that an electron (e^-) could occupy in the material as shown in *Figure 1.3*.

Generally, materials have two distinct bands, the valence band (lower) where e^- are not mobile and well bounded to the atoms of the material and the conduction band (upper) where e^- can be excited, freely move and contribute to the conduction. The forbidden energy gap between them is called band gap (E_g) and no energy states which can be occupied by e^- exist in it. The larger the E_g, the smaller is the probability that an e^- can have enough energy to occupy a state in the conduction band. Thus, in insulators with a large E_g, the valence band can be considered as a fully occupied band and the conduction band as completely empty. In metals the conduction band overlaps with the valence band, the E_g can be considered zero and e^- can move freely around so that metals are characterized with high conductivity.

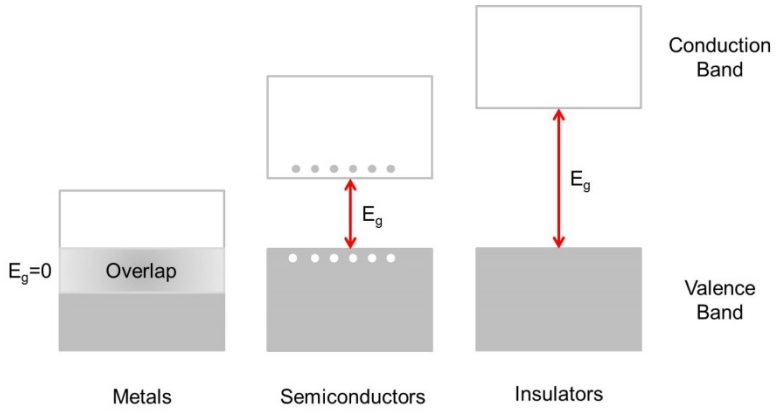


Figure 1.3: Band structures of metals, semiconductors and insulators. E_g stands for the band gap of each material.

On the contrary, a semiconductor as Si exhibits intermediate behaviour between metals and insulators. The E_g is smaller than that of insulators and e^- can have enough energy to jump from the valence band to the conduction band. This energy can be provided by light if a photon has $E_{ph} \geq E_g$. Electrons (grey dots) in the conduction band leave behind in the valence band empty

entities which are called holes (h^+) (white dots) and can diffuse in the valence band in the same way as e^- in the conduction band.

1.2.3 The Photovoltaic Effect

The working principle of all today solar cells is based on the photovoltaic effect which consists of three basic processes:

a. generation of the charge carriers due to the absorption of photons in the materials that form a *p-n* junction,
b. subsequent separation of the photo-generated charge carriers at the *p-n* junction and
c. collection of the photo-generated charge carriers at the terminals of the *p-n* junction.

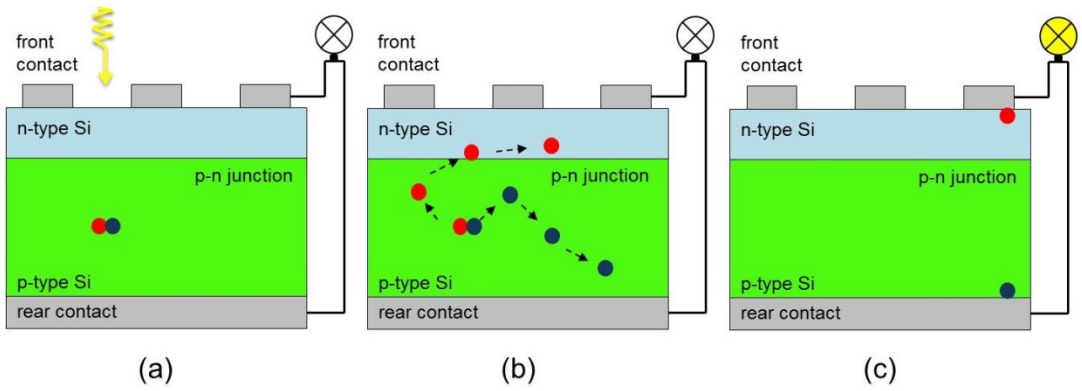


Figure 1.4: The photovoltaic effect illustrated by the simplest structure of a Si p-n junction. (a) Generation of e^- (red dot)/h^+ (blue dot) pair due to light absorption, (b) separation of e^-/h^+ at the p-n junction, (c) Collection of e^- and h^+ at the front and back electrode.

The photovoltaic effect is schematically illustrated in *Figure 1.4* by using the simplest structure of a c-Si *p-n* junction and its explanation will be based on the conventional homojunction c-Si as well. The so called *p-n* junction is the fundamental building block of the solar devices and is formed when a *p*- type and an *n*- type material are joined together. A *p*- type and an *n*- type material result from doping the intrinsic material with elements with a different number of valence e^-. So in case of c-Si, every atom has four valence e^- making bonds with the neighboring four atoms. If the perfectly pure Si lattice is doped with phosphorus which has five valence e^-, four of them will be occupied due to the bonds with the four Si atoms around and the

extra e^- will move freely in the network. At the same time a positively charged ion is created where the phosphorus atom is residing. This is called *n*- doping (negative) and e^- are the majority charge carriers as their concentration density is much higher than that of the h^+ which are the minority charge carriers. Now, boron impurities are incorporated in Si. Since boron has three valence e^-, one e^- is missing to make a bond with the fourth neighboring Si atom. This empty entity represents a h^+ which is easily excited to a free charge carrier as well. Boron is not neutral anymore and becomes negatively charged. Adding boron impurities, extra h^+ are available resulting in *p*- doping (positive) where h^+now are the majority charge carriers. Phosphorus and boron impurities are called donors and acceptors, respectively, while the former donates extra e^- and the latter accepts e^- from the valence band.

When the *p*- type and *n*- type materials are brought together, e^- will diffuse from the *n*- type to the *p*- type material and h^+ will diffuse to the opposite way due to the concentration gradient. In the meantime, an internal electric field is gradually created by donors and acceptors at the depletion region of the junction where no charge carriers exist. Under the influence of the internal electric field, some e^- and h^+ flow in the opposite direction to the flow caused by diffusion. These opposing flows eventually reach a stable equilibrium and the net flow of e^- and h^+ across the *p-n* junction is zero.

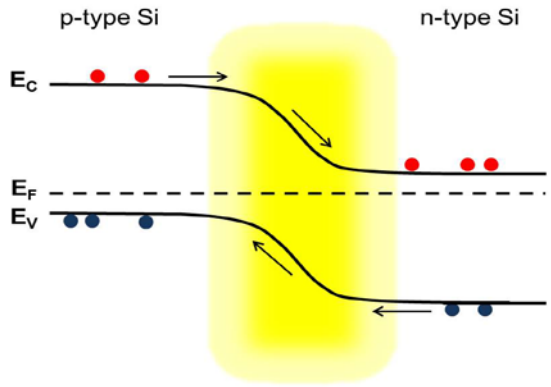


Figure 1.5: Band diagram of the Si p-n junction. The yellow part represents the depletion region and E_C, E_V and E_F stand for the conduction band, the valence band and the Fermi energy level, respectively.

The energy band diagram of the c-Si *p-n* junction under equilibrium is illustrated in *Figure 1.5*. The band bending of the conduction (E_C) and valence band (E_V) represents the existence of the internal electric field at the depletion region. E_F stands for the Fermi energy which can be described as the average energy of e^- and its position is determined by the majority carriers in

semiconductor material so that in the *p*- type layer, the Fermi energy level is close to E_V while in the *n*- type layer it is close to E_C.

Under illumination, extra e^-/h^+ pairs are generated and the minority carrier concentration increases significantly in each layer. In the *p*- layer for example, e^- will diffuse towards the junction and will be attracted towards the positive charge on the *n*- type material side due to the "built-in" electric field. Similarly, the h^+ are attracted to the negative charge of the *p*- type material side. If e^- and h^+ reach each other they will be annihilated in a process called recombination. Otherwise, they will be collected at the terminals and direct current will flow if an electrical load is connected to the solar cell as the final process of the photovoltaic effect shown in *Figure 1.5.c*.

1.3 Heterojunction with intrinsic thin film solar cell

It is a fact that nowadays larger values of the conversion efficiency of PV technology have been reached with the realization of sophisticated c-Si cell structures, involving numerous and very complicated steps. At the same time an inevitable increase of costs is observed which is not compatible with industrial production requirements and reproducibility. In order to realize reliable devices characterized by high efficiency and low cost, an approach has been developed on the basis of a-Si:H/c-Si heterojunction or else SHJ (Silicon Heterojunction) solar cells, which combines wafer (1^{st} generation) and thin film technologies (2^{nd} generation). In this area impressive results have been achieved by the a-Si:H/c-Si heterojunction device with intrinsic thin layer, the so called HIT solar cell, developed by Panasonic with the highest efficiency in the world of 24.7% [5].

The optimal design of the most recently developed SHJ solar cell as well as the devices fabricated in this work, is based on a c-Si wafer sandwiched by thin a-Si:H layers. On an *n*- type c-Si absorber layer, a *p* a-Si:H layer is deposited as the front emitter and a highly *n*- doped a-Si:H layer is implemented as back surface field (BSF) for repulsion of the generated h^+ and better separation of the charge carriers. Due to the doped a-Si:H layers, the defects at the interface with c-Si substrate are increased. In order to reduce the interface recombination and achieve good passivation of the c-Si surface, an *i* a-Si:H thin layer is incorporated in the *p* a-Si:H/*n* c-Si and *n* c-Si/*n* a-Si:H interfaces.

This particular structure can be illustrated in the band diagram shown in *Figure 1.6.* By fabricating layers with that particular order, a sufficient charge carrier transport is provided because of the large band offsets created in the E_C and the E_V from the different E_g of the participating semiconductors. The conduction band offset at the *p-i/n* junction ensures the e^- (black dots) flow only towards the *n* a-Si:H layer while the offset at the valence band at the *n-i/n* junction serves as a barrier for the h^+ (white dots) preventing them from travelling to the back contact and being easily recombined as the minority charge carriers.

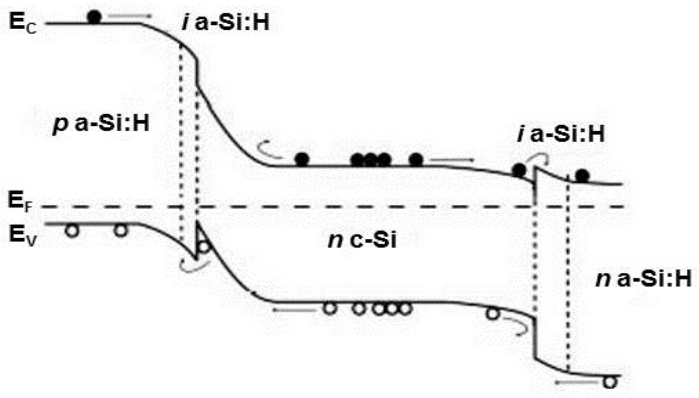


Figure 1.6: Schematic band diagram of the SHJ devices fabricated in this thesis at the PVMD group [6].

Comparing the SHJ solar cell with the conventional c-Si solar cell described in *Section 1.2.3*, apart from the discontinuities which are responsible for the better separation of the energy carriers, the fabrication of the SHJ device is relatively fast and simple (see *Figure 1.7*).

The thermal budget during the heterojunction formation is considerably reduced compared to homojunction formation. The deposition temperature of a-Si:H layers (plasma) is realized at a temperature below 250ºC. Due to the low processing temperature of the SHJ solar cell and its symmetric structure, wafer bowing is suppressed [7], so that the use of thinner substrates is enabled reducing even more the material cost. On the contrary, the fabrication of a c-Si solar cell involves complicated and demanding processing steps approaching high temperatures of approximately 1000ºC. Furthermore, the time required to form the junction and deposit contact layers is also shorter for SHJ than for conventional c-Si solar cells. Last but not least, although the SHJ solar cell is composed of a-Si:H and c-Si materials, it exhibits neither a strong performance degradation under light exposure, as is the case for thin-film a-Si:H solar cells, nor a strong temperature dependence of the performance as observed in c-Si solar cells resulting in high performance stability.

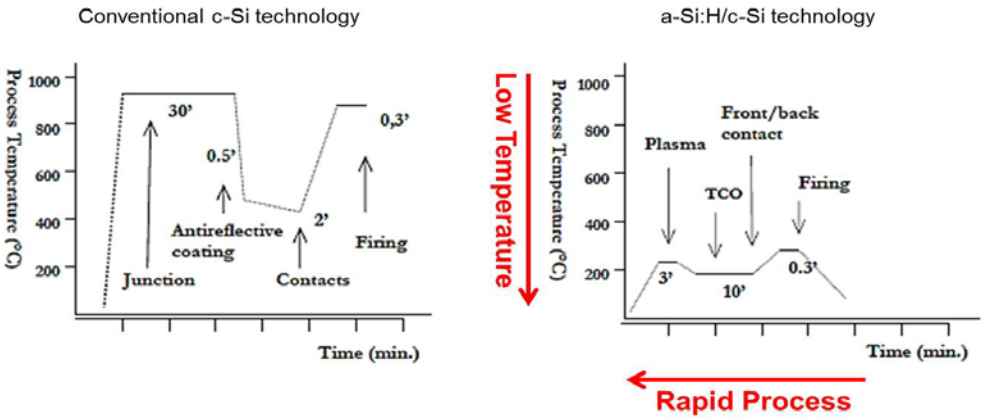


Figure 1.7: Comparison of the fabrication process of the conventional c-Si and the SHJ solar device [8].

1.4 Limiting factors in silicon heterojunction solar cell

Optical and recombination losses strongly contribute to the reduction of the energy conversion efficiency of today's solar cells as well as SHJ solar devices. Optical losses consist of spectral mismatch and reflection. Spectral mismatch implies the non-absorption of photons with $E_{ph} < E_g$ and the thermalization process during which the excess energy of photons with $E_{ph} > E_g$ is converted into heat.

Apart from the E_g as an optical parameter, every material is defined by different optical constants which are expressed in the complex refractive index in *Equation 1.2*,

$$\tilde{n} = n - i\kappa \tag{1.2}$$

where the real part n is the refractive index defined as the ratio of the speed of light in the vacuum and in the medium and the imaginary part κ is the extinction coefficient associated with the absorption of light in the medium. Both of them are function of λ. When light reaches an interface of two different medium a part of it is reflected and a part of it is transmitted (refracted) into the medium as shown in *Figure 1.8*.

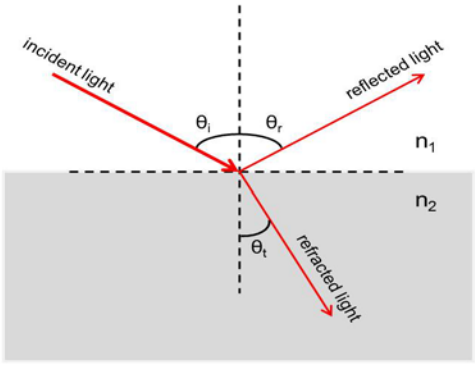


Figure 1.8: Reflection and transmission (refraction) of light at the interface formed by two different medium.

In case of a flat and smooth interface, the angles of incident (θ_i) and reflected (θ_r) light are equal as the reflection is always specular. The relationship between the angles of incidence and refraction (θ_t) is described by Snell's law in *Equation 1.3*.

$$\frac{sin\theta_t}{sin\theta_i} = \frac{n_1}{n_2} \tag{1.3}$$

If roughness exists at the interface, diffuse reflection is observed where incident light is reflected at many angles.

It should be noted that in this thesis, instead of reflection and transmission, the wavelength dependent terms reflectance (R) and transmittance (T) will be used which are the fraction of the total incident energy that is reflected and transmitted at the interface, respectively. While SHJ solar cell is composed of different layers stacked together, R occurs at every interface of the device. All these processes result in a total reflectance (R_T) between the SHJ solar cell and air and is considered one of the main optical losses in a solar cell and should be minimized.

Subsequently, when light penetrates into a material, it will be absorbed as it propagates through the material. The light absorption in a material depends on the absorption coefficient (α) which is related to κ with *Equation 1.4*.

$$\alpha = \frac{4\pi\kappa}{\lambda} \tag{1.4}$$

In general, light is absorbed in all layers that form the solar cell. However, light absorption in transparent conductive oxide (TCO) and a-Si:H layers at short wavelengths does not contribute to the generation of e^-/h^+ pairs and is called parasitic absorption. The TCO layer is deposited at

the illuminated front of the solar cell for enhancing the energy carriers conductivity and the antireflective properties of the cell. On the other hand, at long wavelengths parasitic absorption is observed in free charge carriers. Therefore, only the part of the incident light that is absorbed in the absorber layer can contribute to the creation of e^-/h^+ pairs. Due to the limited thickness of the absorber layer, not all the light entering the absorber layer is absorbed. Incomplete absorption in the absorber due to its limited thickness is an additional loss that lowers the efficiency of the energy conversion.

Concerning recombination losses, the final step of the photovoltaic effect is the collection of the e^- and h^+ at the electrodes of the solar cell. However, not all the photogenerated carriers manage to reach the terminals due to the recombination process. Recombination loss mechanism occurs mainly because of the existence of defects in the bulk of the material and at the interface of the junction. In SHJ, the absorber layer is a highly pure c-Si wafer so that the recombination loss is mainly limited by the a-Si:H/c-Si interface.

Finally, additional factors such as a high series and a low shunt resistance of the solar cell and a higher shading loss due a non-optimal design of the front metal grid will limit the power output and subsequently the performance of the solar cell.

1.5 Scope of this research

Globally, the highest efficiency a-Si/c-Si solar cell of 24.7% [5] has been demonstrated by Panasonic. The research conducted at the PVMD group to contribute to this progress is relatively young and there is ample opportunity for improvement.

Among the aforementioned limitations of a solar cell, this work aims at the reduction of the reflectance of the SHJ solar cell and the recombination losses at the interface formed at the junction between the c-Si substrate and the *i* a-Si:H layer. For the first objective, a randomly textured wafer and an antireflective coating at the illuminated front are applied. The anti-reflective coating working principle is based on the destructive interference and the refractive index matching between the ambient, the coating layer and the device. Indium Tin Oxide (ITO) will be deposited as antireflective coating having at the same time properties of an excellent TCO resulting in the SHJ structures illustrated in *Figure 1.9*. The ITO thickness of 80 nm and 75 nm will be used for polished and textured substrate, respectively, as they have been already optimized by *Zhang et al.* [9].

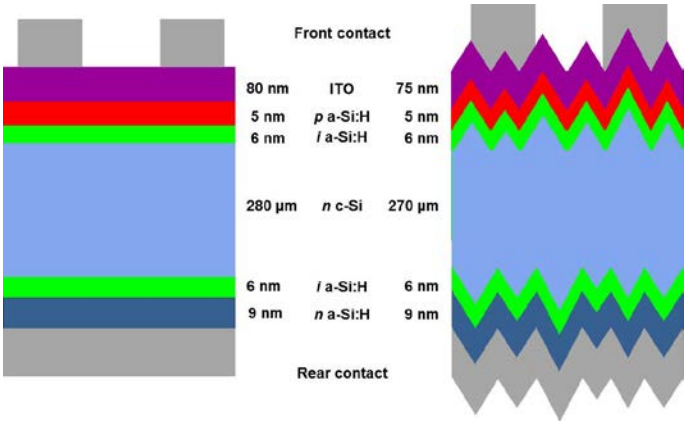


Figure 1.9: SHJ structures of solar cells fabricated on flat and textured substrates in this thesis at the PVMD group.

On the other hand, a textured wafer can minimize the reflection due to multiple "bounces" of light on the textured surface and at the same time increase the optical path length leading to enhanced photon absorption in the absorber layer. Thus, the first part of the research is spent on the development of a reproducible texturing recipe which provides substrates with homogeneous pyramidal morphology and low reflectance resulting in high J_{SC}.

However, texturing seems to lead to an a-Si:H/c-Si interface with higher recombination which limits the V_{OC} of the SHJ device after using for the textured wafer a cleaning treatment same as for the flat wafer. Up to now, although SHJ solar cells have been fabricated on textured wafers demonstrating high J_{SC}, the V_{OC} is limited at 638 mV. Having as a reference the V_{OC} of the SHJ achieved with a flat substrate, the second objective of this work is the development of a proper wet-chemical treatment of the textured substrate before the deposition of the *i* a-Si:H. This targets at the preparation of a clean and smooth surface resulting in less defects, high a-Si:H/c-Si interface quality and higher values of the V_{OC}.

1.6 Thesis outline

This thesis consists of eight chapters. *Chapter 1* provides insight into the solar energy and photovoltaic technology. After analyzing the photovoltaic effect as the working principle of a solar cell, the structure of the SHJ device fabricated in this work and the factors that limit its performance are described. Finally, the objectives of the current research and the outline of this thesis are given.

In *Chapter 2*, the equipment for accomplishing the different fabrication steps of a SHJ solar cell and the tools for the characterization of the device are presented. The techniques used for the deposition of the a-Si:H layers, TCO and metal contacts are firstly described. Subsequently, the methods for electrical and optical characterization are explained.

Chapter 3 highlights the benefit provided by a textured c-Si wafer incorporated in a SHJ solar cell as the absorber layer of the device. The chemical path describing the steps of the texturization process and the agents participating in this process are analytically described. Then, the two mechanisms of a textured absorber layer of a SHJ solar cell which result in higher J_{SC} are explained. At the end, texturing-related issues that may lead to the offset of the benefit provided by a textured c-Si wafer as substrate in a SHJ solar cell are presented.

The proper surface conditioning of the textured c-Si substrate of the heterojunction solar cell is a prerequisite for forming an a-Si:H/c-Si interface with excellent electrical properties. Contamination removal, surface smoothening and H-termination of the c-Si surface are key parameters for achieving this and are discussed in *Chapter 4*.

Moving on to the experimental part, *Chapter 5* presents the development of an efficient recipe for a good quality texturing in low TMAH concentration solution. After explaining the necessity for IPA addition to low TMAH concentrations, the experimental process for the development of a recipe for a homogeneous, smooth and reproducible texturing with low reflectance is described.

Chapter 6 presents the experimental process for the investigation of the optimal treatment before the *i* a-Si:H deposition on the textured c-Si substrate. RCA, Piranha, treatment in HNO_3 solutions and combinations of them are compared by using lifetime measurements as the evaluation tool of each treatment.

The results obtained from the characterization of the SHJ devices fabricated through this research are presented in *Chapter 7*. The impact of the application of the already developed texturing recipe and pre-deposition treatment on the SHJ solar cells is described by the external parameters of the devices along with EQE and lifetime measurements.

Finally, *Chapter 8* summarizes the concluding remarks derived from this thesis and presents recommendations for future work which may lead to further improvement of the SHJ solar cell performance.

Chapter 2

Instrumentation for heterojunction device fabrication and characterization

2.1 Fabrication process

2.1.1 Plasma-enhanced chemical vapour deposition

The growth of the intrinsic, *n*- doped and *p*- doped a-Si:H layers on the textured c-Si substrate is realized by radio-frequency plasma-enhanced chemical vapour deposition (RF PECVD). This technique is known for enabling the deposition of thin films at low operating temperatures while at the same time high quality, good adhesion, good coverage of textured structures and uniformity are the main properties of these films.

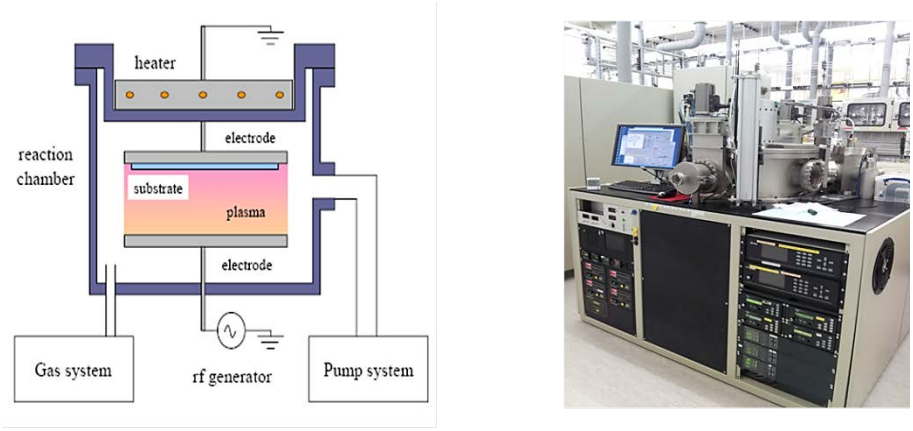


Figure 2.1: (a) Schematic diagram of RF-PECVD [10]*, (b) the RF PECVD setup "AMOR" at the PVMD group.*

In detail, silane (SiH_4) and other gases like molecular hydrogen or dopants are introduced in the ultra-high vacuum (UHV) reaction chamber. There, the gas mixture is transformed into a glow discharge (plasma) by applying an oscillating electric field between two conductive

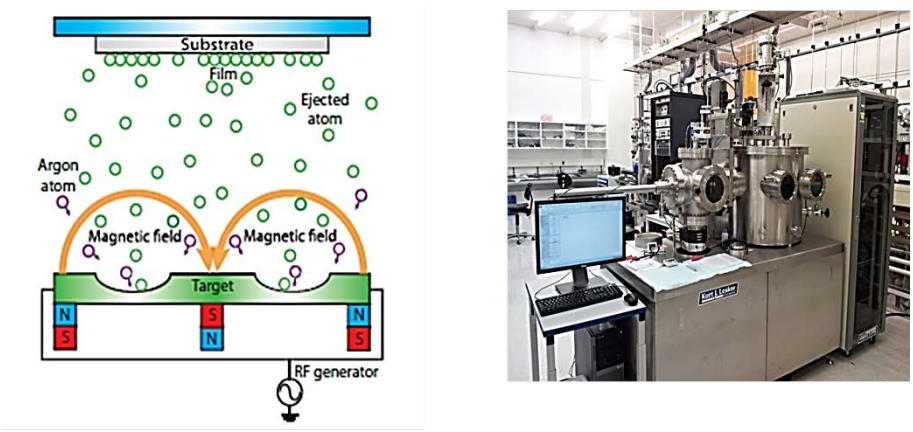
electrodes through a RF signal of 13.56 MHz. Plasma is composed by reactive radicals, ions, neutral atoms, molecules as well as e^-. Since the formation of these reactive and energetic species occurs by collision in the gas phase, the substrate can be maintained at a low temperature. These atomic and molecular fragments interact with the substrate which is kept grounded with a lower potential than the plasma and the thin film layer is formed since only neutral or positively charged particles can diffuse towards the substrate [11].

AMOR UHV multi-chamber cluster by Elettrorava S.p.A. is the tool utilized for depositing *i*, *n* and *p* a-Si:H layers. *Figure 2.1* shows *(a)* schematically the RF-PECVD and *(b)* the setup of the AMOR where the process occurs.

2.1.2 Radio-frequency magnetron sputtering

As already introduced, ITO is deposited on top of the *p* a-Si:H layer of the SHJ solar cell as an antireflective coating with high electrical conductivity. The ITO layer is deposited using RF magnetron sputtering.

This technique involves the ejection of sputtering material and its deposition on the substrate (anode) due to the bombardment of ions to the ITO target (cathode). The vacuum chamber is filled with inert gas argon (Ar) and plasma is ignited by applying an oscillating RF electromagnetic field between the anode and the cathode. Positively charged argon ions (Ar^+), generated in the plasma region, are accelerated to the target surface. Atoms are ejected from the target which are directed to the substrate and eventually settled. Electrons which are released during Ar ionization are accelerated to the anode substrate, subsequently colliding with additional Ar atoms, creating more ions and free e^- in the process, continuing the cycle. To enhance this process, magnets are added underneath the cathode surface in order to trap e^- near the target instead of being attracted toward the substrate, resulting in higher ionization efficiency and a denser plasma. One of the main benefits of the RF magnetron sputtering method is the control of the RF power which enables the determination of the ion bombardment energy and consequently the prediction of the sputtering rate and the layer thickness.



(a) (b)

Figure 2.2: (a) Schematic diagram of RF magnetron sputtering process [6]*, (b) the sputtering machine at the PVMD group.*

The ITO is deposited on the textured SHJ device by using the RF magnetron sputtering system by Kurt J. Lesker Company. The schematic diagram of the process and the setup are depicted in *Figure 2.2, (a)* and *(b)* respectively.

2.1.3 Physical vapour deposition

Metal contacts are deposited on the solar cells through metal evaporation. A metallic source is heated above its sublimation temperature and evaporated to form a film on the surfaces where the metallic vapour is condensed. In this work, the physical vapour deposition (PVD) is based on thermal and electron beam (e-beam) evaporation under vacuum conditions. For thermal evaporation, the metal to be deposited is loaded into a boat-crucible which is resistively heated by applying high current through it. The temperature of the material continuously increases until the metal starts evaporating. During e-beam PVD, e^- are generated by applying high DC voltage to a tungsten filament located under the crucible. The electron beam is accelerated and directed towards the source material by several bending magnets. When the e^- strike the metal their kinetic energy is converted to thermal energy resulting in the metal evaporation.

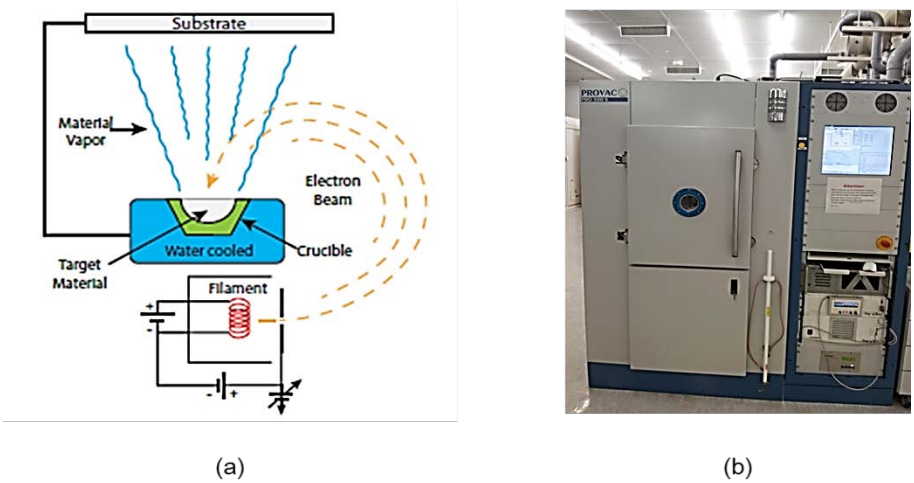


Figure 2.3: (a) Schematic diagram of the PVD of the metal contacts [6]*, (b) the metal evaporator at the PVMD group.*

The physical vapour deposition occurs in a high vacuum PRO500S metal evaporator by Provac which is shown above in *Figure 2.3* along with the schematic illustration of the e-beam evaporation process. Provac system is equipped with a 4 pocket (crucible) e-gun for evaporation of aluminium (Al), chromium (Cr), titanium (Ti) and ceramics. Silver (Ag) can be deposited by thermal evaporation. Furthermore, the desirable metal pattern can be created on the solar cell by using stencil masks. Pumping cycles and deposition recipes are fully programmable.

2.2 Characterization measurements

2.2.1 Spectrophotometry

For the optical characterization of the absorber layer the PerkinElmer Lambda 950 UV/VIS/NIR spectrophotometer is extensively used. This spectrophotometer is equipped with a deuterium arc lamp for ultraviolet light and a tungsten-halogen lamp for visible and infrared light. With these two lamps, a wavelength spectrum between 175 nm and 3300 nm is covered.

The reflectance and transmittance of a specimen are measured when an Integrating Sphere (IS) is mounted on the spectrophotometer. The IS has a diameter of 150 mm and is internally coated with Spectralon, a highly scattering and highly reflective material over the ultraviolet, visible and near-infrared regions of the spectrum. The sphere contains two detectors at the bottom dealing with the aforementioned wavelength range.

When the sample is fixed at the transmittance port and a cap is placed at the reflectance port (see *Figure 2.4*), the light enters through the sample experiencing multiple reflections. The electromagnetic field in the IS becomes homogeneous and allows measuring the total transmittance T_T. The cap at the reflectance port can be removed so that the specular transmitted light escapes from the system and only the diffuse transmittance T_D is measured. Similarly, the total reflectance R_T can be measured by mounting the sample at the reflectance port. The diffuse reflectance R_D is measured by removing another cap next to the transmittance port.

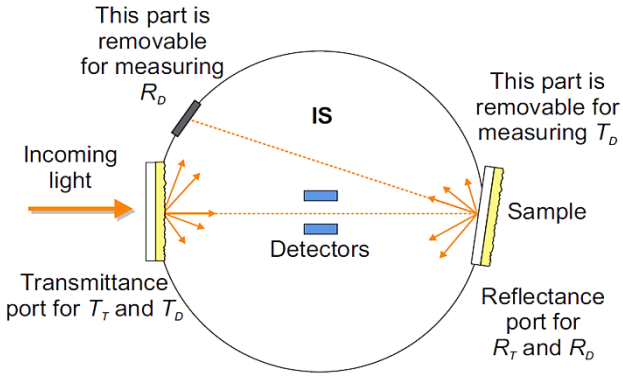


Figure 2.4: Descriptive sketch of integrating sphere operation for PerkinElmer Lambda 950 UV/VIS/NIR spectrophotometer [11].

2.2.2 Scanning electron microscopy

Scanning electron microscopy (SEM) enables the investigation of specimens with a resolution down to the nanometer scale. It is used for the visualization of the surface morphology of textured substrates and any nano-scale features that may be present on the pyramidal structure.

A normal scanning electron microscope operates at a high vacuum. The working principle is that a highly energetic beam of e^- (typically from 0.2 to 40 keV) is generated by a suitable source, typically a tungsten filament or a field emission gun. The electron beam is accelerated through a high voltage and pass through a system of apertures and electromagnetic lenses to produce a thin beam of e^-. The beam scans the surface of the specimen by means of scan coils and e^- and X-rays are emitted from the specimen by the action of the scanning beam. In the

most standard detection mode, secondary e^- are detected and converted into a signal that is sent to a screen producing very high-resolution images revealing details less than 1 nm in size.

SEM images presented in this work are carried out either by SEM JEOL JSM-6360 at the PVMD group or FEI-Philips XL30 SEM of Kavli Institute at TU Delft.

2.2.3 Minority carrier lifetime measurement

The minority carrier lifetime measurement is one of the most important characterization techniques used in this work. The measurement targets at evaluating the quality of the a-Si:H/c-Si interface of the SHJ solar cell. The minority carrier lifetime is directly related to the V_{OC} of the solar cell. Low lifetimes witness a more defective interface and inefficient passivation. A higher number of defect states results in higher recombination and a lower V_{OC}.

The lifetime is measured by placing the sample on a stage which contains a built-in coil underneath. Light is pulsed onto the sample to create the excess carriers, and the coil circuit senses the increase in conductance of the sample due to the carriers. The change in conductance is analyzed and the lifetime of the excess carriers is reported. In this work, the WCT-120 Photoconductance Lifetime Tester by Sinton Instruments is used for the minority carrier lifetime measurement.

The effective carrier lifetime (τ_{eff}) can be expressed by *Equation 2.1* [12]:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{1}{\tau_{surface}} \tag{2.1}$$

and reflects the recombination level of the measured sample in the bulk (τ_{bulk}) and at the surface/interface ($\tau_{surface}$). A sufficiently pure c-Si substrate with a perfect structure with each atom in its optimal place in the lattice can have very high bulk lifetime and the bulk recombination can be neglected. In that case, the effective carrier lifetime will be limited by the surface/interface recombination and consequently the first term on the right-hand side of *Equation 2.1* can be neglected.

For an *n*- type wafer, the excess minority carrier (h^+) concentration can be expressed by the general continuity equation [13]:

$$\frac{\partial \Delta p}{\partial t} = G - R + \frac{\nabla J}{q} \tag{2.2}$$

where Δp is the excess minority carrier concentration, G is the photogeneration rate of charge carriers, R is the recombination rate, q is the elementary charge and J is the h^+ current density. Assuming spatially uniform photogeneration and no electric field, the last term on the right-hand side of *Equation 2.2* vanishes. Furthermore, the relationship between recombination rate R and effective lifetime τ_{eff} given by [14] is:

$$R = \frac{\Delta p}{\tau_{eff}} \tag{2.3}$$

Combining *Equations 2.2* and *2.3*, the lifetime τ_{eff} is determined by:

$$\tau_{eff}(\Delta p) = \frac{\Delta p(t)}{G(t) - \frac{d\Delta p(t)}{dt}} \tag{2.4}$$

Depending on the expected minority carrier lifetime, two are the standard operating modes of the light source that can be used during the measurement, the quasi-steady-state (QSS) mode suitable for lifetimes below 100 μs and the transient mode for lifetimes above 100 μs [15]. The difference between these two modes is the duration of illumination, indicated by the decay time constant of the flash lamp (τ_{flash}). A long time constant leads to QSS measurement where $\tau_{flash} \gg \tau_{eff}$. Under these conditions, the excess carrier concentration is in steady-state, the term $\frac{d\Delta p(t)}{dt} = 0$ and *Equation 2.4* is reduced to:

$$\tau_{eff}(\Delta p) = \frac{\Delta p(t)}{G(t)} \tag{2.5}$$

On the other hand, a short decay constant is selected for the transient mode where $\tau_{flash} \ll \tau_{eff}$. In this case, there is no generation, the carrier concentrations are not in steady state and *Equation 2.4* is reduced to:

$$\tau_{eff}(\Delta p) = \frac{-\Delta p(t)}{\frac{d\Delta p(t)}{dt}} \tag{2.6}$$

τ_{eff} is measured as a function of the excess minority carrier concentration and the result is a graph as the one depicted in *Figure 2.5*. Although the entire data trace as a function of carrier density is shown for a single-point measurement, the lifetime that is reported is for Δp=10^{15}cm^{-3}. This has been used for the majority of reported data over the last 15 years. The sample presented as an example in *Figure 2.5* corresponds to τ_{eff}=3 ms.

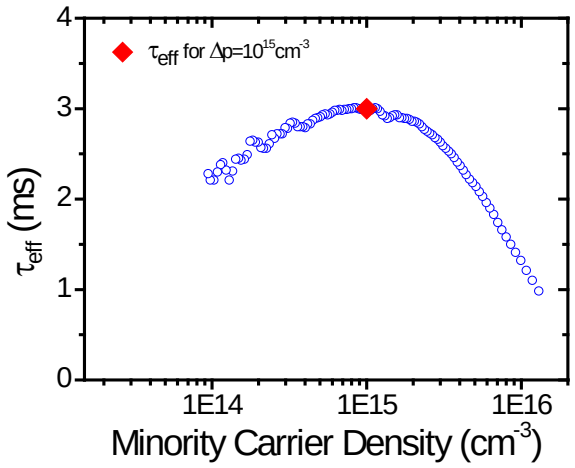


Figure 2.5: Measured lifetime of a textured n-type c-Si wafer passivated with i a-Si:H layers at both sides, under transient conditions.

The photogenerated excess e^- and h^+ densities, Δn and Δp, result in an increase in the conductance of the sample. The excess photoconductance is given by [16]:

$$\sigma_L = q(\Delta n_{av}\mu_n + \Delta p_{av}\mu_p)W \tag{2.7}$$

where σ_L is the conductance of the wafer, μ_n and μ_p are the e^- and h^+ mobilities and W is the thickness of the wafer. During illumination, the excess e^- and h^+ are generated in pairs, then Δp_{av}= Δn_{av} and *Equation 2.7* can be expressed as:

$$\sigma_L = q\Delta p_{av}(\mu_n + \mu_p)W \tag{2.8}$$

The thickness of the wafer is known and the mobilities can be easily found in literature. Further details on τ_{eff} measurement are available in [16].

2.2.4 Illuminated J-V characteristics

The electrical performance of a solar cell is characterized by using a solar simulator. This setup enables the measurement of the main external parameters of a solar cell which are the short circuit current density J_{SC}, the open circuit voltage V_{OC}, the fill factor FF and the maximum power P_{max}.

The J_{SC} is the maximum current density that a solar cell provides when no voltage is applied across the solar cell or when its electrodes are short circuited. The J_{SC} is strongly dependent on the absorption of the absorber layer and the total reflection of the solar cell. On the other hand, the maximum voltage of a solar cell is the V_{OC} when no current flows through the contacts. Finally the P_{max} is the maximum power produced by a solar cell when it operates at the maximum power point. The current density and voltage which correspond to this point are J_{mpp} and V_{mpp} respectively.

Every solar device has unique performance characteristics under prevailing conditions and can be graphically represented. The graph is called a "*J-V* curve" and obtained by sweeping the applied voltage across the solar cell electrodes and measuring the outgoing current. A typical example of the graphical output including the external parameters of a solar cell is depicted in *Figure 2.6.*

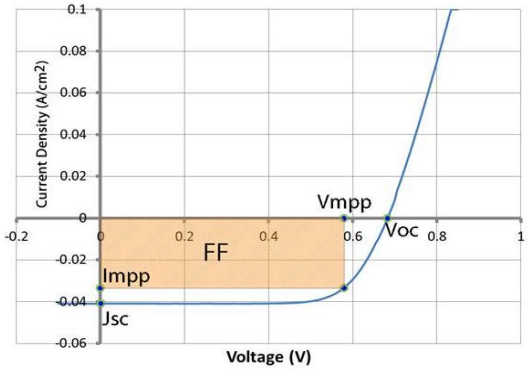


Figure 2.6: J-V curve of a SHJ solar cell under illumination [17].

The fill factor is defined as $FF = \frac{J_{mpp}V_{mpp}}{J_{SC}V_{OC}}$ and the conversion efficiency (η) of the solar cell is calculated as the ratio between the generated maximum power and the incident power (P_{in}):

$$\eta = \frac{P_{max}}{P_{in}} = \frac{J_{mpp}V_{mpp}}{P_{in}} = \frac{J_{SC}V_{OC}FF}{P_{in}} \tag{2.9}$$

In a non-ideal solar cell (see *Figure 2.7*) the series resistance (R_S) and the shunt resistance (R_P) have a strong impact on the *FF* of the device. The R_S results from the bulk resistance of each component of a solar device, the junction resistances and the electrodes resistance. The R_P represents the leakage current of the device.

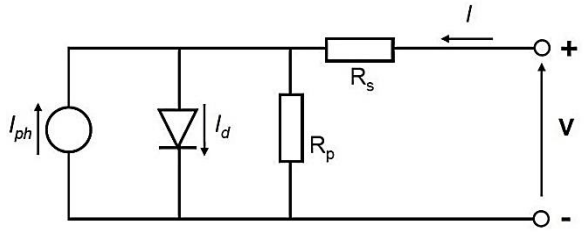


Figure 2.7: The equivalent circuit of a non-ideal solar cell [2].

The electrical performance of a solar cell is generally rated under standard test conditions (STC) which correspond to irradiance of 1000 W/m^2 (1 sun), AM 1.5 solar spectrum and device temperature at 25°C. AM 1.5 is the standard spectrum under which solar cells are tested and refers to the terrestrial solar spectral irradiance. In this work, the Wacom WXS-156S-L2 solar simulator equipped with a xenon and a halogen lamp for improved spectral distribution is used. The solar simulator setup and its spectral concurrence to the AM 1.5 spectrum are shown in *Figure 2.8*. Furthermore, the reported V_{OC} and *FF* measurements are determined by the solar simulator, while the J_{SC} is confirmed through the external quantum efficiency (EQE) measurement in order to avoid miscalculation due to indefinite solar cell area.

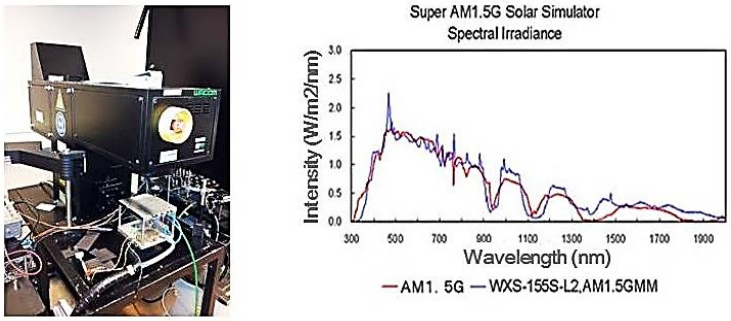


Figure 2.8: (a) Wacom WXS-156S-L2 solar simulator at the PVMD group, (b) Spectral match provided by the solar simulator for AM1.5 [18].

2.2.5 External quantum efficiency

When a solar cell is illuminated, not all incident photons contribute to the current delivered by the solar cell. Some of the photons have energy lower than the E_g of the absorber layer and are not absorbed and some are reflected. Furthermore, generated charge carriers may not be collected at the terminals due to recombination. This current loss is portrayed by the EQE of a solar cell which is defined as the number of e^-/h^+ pairs created and successfully read out by the device for each incoming photon at a certain wavelength.

EQE ideally has a square shape and for every measured wavelength it is equal to unity. However, the EQE graph of a typical SHJ solar cell depicts a curve with a "bell" shape due to losses. As an example, the EQE measurement of a SHJ device with textured substrate fabricated during this work is presented in *Figure 2.9*. At short wavelengths, reflection and parasitic absorption in ITO and a-Si:H layers are observed. On the other hand, at long wavelengths reflection and absorption in rear contact are the dominant losses as well as parasitic absorption in free charge carriers.

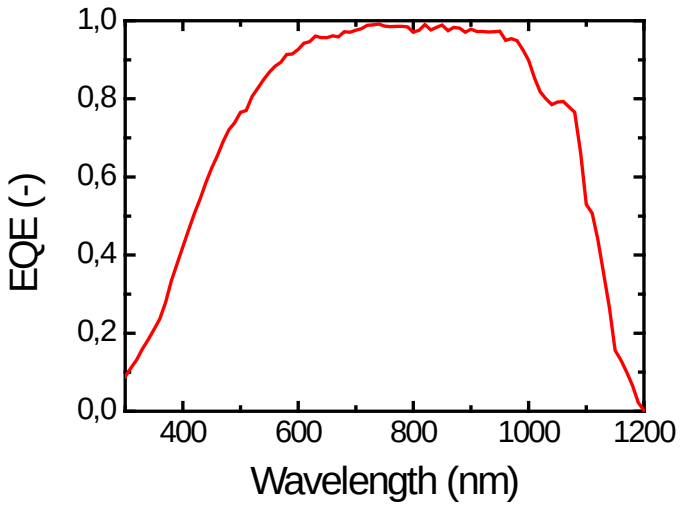


Figure 2.9: EQE measurement of a SHJ solar cell with textured absorber layer.

EQE relates to the response of a solar cell to the various wavelengths in the spectrum of light impinging on the cell. The spectral response (SR) is defined as the ratio of the current generated by the solar cell to the power incident on the solar cell. SR is conceptually similar to EQE and their relation is expressed by *Equation 2.10*:

$$EQE(\lambda) = SR(\lambda)\frac{hc}{q\lambda} \tag{2.10}$$

A reliable current density is obtained by the calculation of EQE:

$$J_{SC} = q\int_{\lambda_{min}}^{\lambda_{max}} \Phi(\lambda)EQE(\lambda)d\lambda \tag{2.11}$$

$\Phi(\lambda)$ is the photon flux and is equal to:

$$\Phi(\lambda) = \frac{P(\lambda)\lambda}{hc} \tag{2.12}$$

where $P(\lambda)$ is the spectral irradiance incident on the solar cell which corresponds to AM 1.5 spectrum. Combining *Equations 2.10*, *2.11* and *2.12* the J_{SC} is calculated through the SR:

$$J_{SC} = \int_{\lambda_{min}}^{\lambda_{max}} SR(\lambda)P(\lambda)d\lambda \tag{2.13}$$

The EQE setup consists of an illuminator/monochromator, a chopper, a sample holder and a lock-in amplifier. Its working principle is to collect and measure the photo-generated current after illuminating the solar cell with monochromatic light coming from a xenon arc lamp. A chopper is required for the distinction between the illuminated current coming from the monochromator and a current offset from other sources. Finally, the voltage over the solar cell and the shunt resistor is controlled by a power supply. The measurement of the voltage across the resistor by a lock-in amplifier enables the measurement of the current.

Measurement is preceded by calibration with a reference Si diode. The resultant current of the measured solar cell is provided as J_{SC} instead of I_{SC} in order to eliminate the dependence of the solar cell area.

Chapter 3

Theoretical Background on Texturing

3.1 Texturization process

Reflection is one of the main losses in a SHJ solar cell. Furthermore c-Si substrate should be as thin as possible in order to reduce bulk recombination and material costs. However, absorption of light is strongly reduced in thin wafers [2]. Texturing is a method for overcoming these issues by reducing the total reflectance of the device, keeping the physical thickness of the absorber layer as thin as possible and at the same time maximizing its effective optical thickness [19].

Although many ways [20][21][22] exist to texture a c-Si wafer, in this work texturing is addressed to the wet chemical etching of Si in anisotropic alkaline solutions. It is the most widely used and mature technique in Si technology due to its simplicity, ease of use, low-cost and no physical damage introduced to the bulk [20][23].

Anisotropic etching of Si refers to the direction-dependent etching of Si meaning that the etching rate of an exposed surface depends strongly on the crystal orientation of the surface. Atoms in c-Si are arranged in a diamond lattice structure formed by the repetition of a cubic unit cell. Three planes are commonly considered in this structure, the (100), (110) and (111) and are shown in *Figure 3.1*.

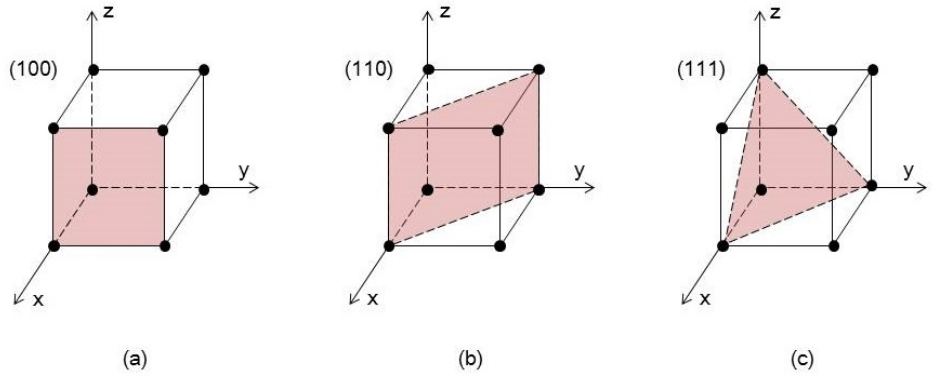


Figure 3.1: The three most common lattice planes of the c-Si structure: (a) (100) plane, (b) (110) plane, (c) (111) plane.

The integers in (100), (111) and (110) are called Miller indices [14] and denote the orientation of a plane of the cubic unit cell and regular repetitions of that plane with a particular spacing lead to a specific orientation of the crystal structure. Detailed analysis of the different crystal orientations (100), (110) and (111) of the c-Si is provided in [14]. Si atoms in a (100) and (111) plane will be referred as (100) oriented and (111) oriented atoms, respectively.

With the texturization process, (100) oriented silicon surface atoms are etched and the planar surface is naturally converted into a surface covered with upright square based pyramids of microns in dimensions. These pyramids are typically bounded by intersecting four (111) equivalent facets at 54,7° to the wafer surface [24] and four (110) ridges due to the anisotropic etching behavior of the etchant solution [25][26][27]. In *Figure 3.2*, the texturing process for the c-Si unit cell at the surface of a wafer is depicted where the (100) plane is textured resulting in a plane with orientation (111).

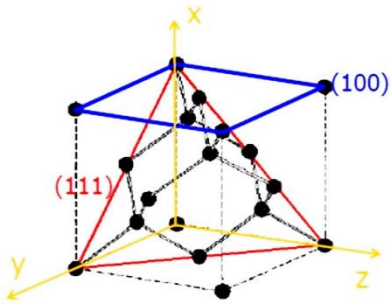


Figure 3.2: During texturing, the (100) plane (blue square) of a c-Si surface unit cell is etched resulting in a (111) plane (red triangle) [28].

Moreover, two images captured using SEM are illustrated in *Figure 3.3* showing the pyramidal surface morphology of a textured c-Si wafer and the angle of 54.7° between one of the (111) facets of the pyramid and the flat surface of the wafer.

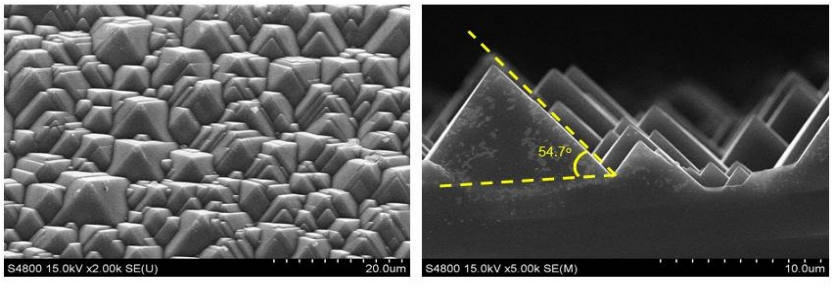


Figure 3.3: a) Oblique SEM image (tilted at a small angle) illustrating the pyramidal surface morphology of a textured(100) oriented c-Si wafer, b) SEM image of the cross section of the same wafer indicating the angle of 54.7° between the flat base and one of the (111) planes of the pyramid.

Before proceeding with the description of the reaction steps occurring during texturing, the fundamental differences between crystal orientations of Si are highlighted. The discussion is limited to (100) and (111) orientations which are the main interest of this work since the pyramidal surface of a textured c-Si wafer is dominated by (111) facets resulting from the anisotropic etching of a planar (100) surface.

The atoms in c-Si are arranged in a diamond lattice structure. All Si atoms within the bulk of the crystal are in a tetrahedral environment and each Si atom forms four covalent bonds with the four surrounding atoms implying that eight e^- are being shared between each atom and its four surrounding atoms [14]. However, at the surface of the crystal, the perfect configuration of atoms is interrupted and each surface atom has less nearest neighbors than an atom within the bulk of the material resulting in unpaired valence e^-. These “incomplete” bonds are exposed by the surface Si atoms and are commonly called dangling bonds.

Figure 3.4.a shows a section of the (111) and (100) surfaces of a Si cubic lattice viewed perpendicular to these planes. As mentioned above, each Si atom in the bulk is bonded to four other atoms. In contrast the surface atoms (atoms shown in blue) are each bonded to three other atoms (atoms in red) in (111) structure and only two atoms (atoms in red) in (100). Consequently, a (111) surface atom has one dangling bond while a (100) surface atom possesses two dangling bonds. The bonds between the (blue) surface atoms and the (red) bulk atoms underneath are called Si-Si backbonds.

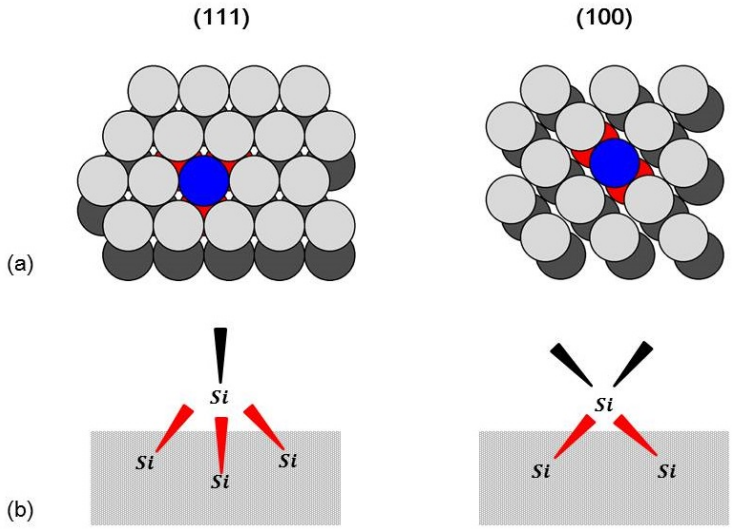


Figure 3.4: (a) Perpendicular view of (111) and (100) c-Si surface showing the different bond configuration of the surface atoms for these planes and the different atomic density as well [29]*, (b) Cross section of (111) and (100) c-Si surfaces highlighting the different number of dangling bonds (black bonds) and Si-Si backbonds (red bonds) corresponding to (111) and (100) surface atoms.*

Furthermore, *Figure 3.4.b* depicts the cross section of the c-Si surface emphasizing the different bond configuration of the surface atoms between (111) and (100) orientation. The black bonds represent the dangling bonds and the red bonds correspond to the Si-Si backbonds for each orientation. The different number of dangling bonds between (111) and (100) surfaces is the reason [30] of the considerably lower etching rate of (111) surface in comparison with the etching rate of (100) surface atoms leading to anisotropic Si etching [31].

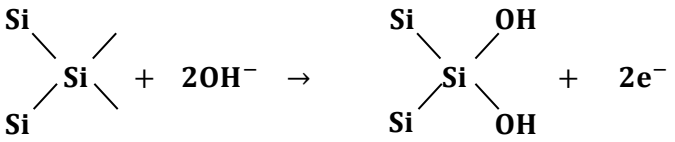
Finally, information on the atomic density of (111) and (100) structures can be extracted from *Figure 3.4.a.* The (111) surface consists of more densely packed atoms than (100) surface. The distance between two (111) atoms is equal to $\frac{a}{\sqrt{2}}$ while for (100) atoms is a which is the lattice constant of Si referring to the constant distance between the cubic unit cells in the lattice [14].

The most widely known alkali hydroxide etchants used to texture c-Si wafers have been aqueous mixtures of KOH or NaOH and IPA [20][32][33]. The main agent responsible for the Si etching is the hydroxide ions (OH^-) provided by the aqueous alkaline solution while the addition of IPA improves the wettability of the Si surface leading to homogeneity of pyramids and improved surface smoothness, predominantly for low concentration alkaline solutions [34], at the cost of a slight reduction in the etching rate of Si.

An electrochemical model has been proposed by *Seidel et al.* [30], describing the anisotropic etching behavior of Si in all alkaline solutions. The model consists of two main steps, an oxidation and a reduction step. In the first stage, in case of a (100) oriented silicon wafer, four OH^- react with one surface Si atom, leading to the breaking of the Si-Si backbonds accompanied by the injection of four e^-. This step is considered to be rate limiting and determines the rate of the etching reaction. Afterwards, in the reduction step, the four injected e^- react with water molecules to form new OH^- and hydrogen.

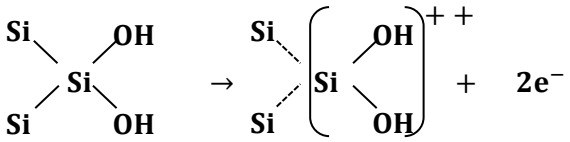
In more detail, after the immersion of a (100) c-Si wafer into the aqueous alkaline solution which acts as an electrolyte, a solid/liquid interface is formed between the Si surface and the etching solution.

In the first reaction step (*Equation 3.1*), the two dangling bonds of a Si surface atom with (100) orientation are bonded with two OH^- by injecting two e^- which stay localized near the semiconductor surface.



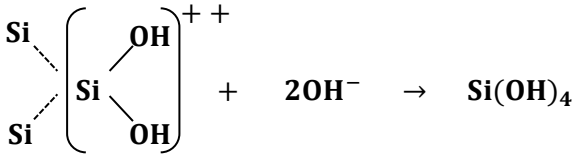
(3.1)

Due to the presence of the bonded OH^- on the solid surface and the strong electronegativity of the oxygen atom, the strength of the Si-Si backbonds of the surface Si atoms will be reduced. The continuous weakening of the Si-Si backbonds (dashed lines) leads to the creation of a positively charged Si-OH^- complex by injecting two more e^- (*Equation 3.2*).



(3.2)

The Si-OH^- complex reacts further with two more OH^- and a Si atom is removed from the solid surface by producing orthosilicic acid $Si(OH)_4$.



(3.3)

The equations above describe the oxidation step of the texturization process where the breaking of the backbonds and the bonding of OH^- according to *Equations 3.2* and *3.3* respectively, happen more or less simultaneously. The neutral $Si(OH)_4$ molecule is removed from the solid surface by diffusion and dissociated in the bulk of the solution due to high pH value producing silicate species shown in *Equation 3.4*.

$$\mathbf{Si(OH)_4} \rightarrow \mathbf{SiO_2(OH)_2^{2-} + 2H^+} \tag{3.4}$$

The e^- injected during the oxidation step are consumed for the reduction (*Equation 3.5*) and dissociation (*Equation 3.6*) of the water molecules which are located near the solid surface.

$$4H_2O + 4e^- \rightarrow 4H_2O^- \quad (3.5)$$

$$4H_2O^- \rightarrow 4OH^- + 2H_2 \quad (3.6)$$

During the reduction step, hydrogen bubbles and OH^- are produced where the latter are considered to be the ones reacting in the oxidation step. Further details on the electrochemistry of the texturing process concerning the energy levels position of the Si and electrolyte and the way charge transfer occurs when the Si/electrolyte interface is formed are out of the scope of this research and can be found in [35].

KOH and NaOH aqueous solutions have been the most widely investigated and used alkaline solutions for texturing representing a mature and cost-effective etching technology. However, these solutions are toxic and pollutant. Especially for the SHJ solar cell where high quality a-Si:H/c-Si interface is a prerequisite for the fabrication of a high efficiency solar cell, the contamination of the silicon surface by K^+ and Na^+ ions should be avoided [20][36]. Tetramethylammonium hydroxide (TMAH, $(CH_3)_4NOH$) has been investigated and proposed as an alternative to KOH and NaOH solutions. TMAH is not pollutant or toxic. Furthermore, its solution is anisotropic, non-volatile and most importantly presents uncontaminating ions [20][23][27][36]. The main drawback of TMAH is its high cost but as far as low concentration solutions are efficient enough to texture the surface of c-Si wafers, this method has become very cost competitive [20].

TMAH is widely used in Si microelectronics systems when anisotropic etching is required [23][37]. However, a suitable process involving TMAH has not yet been established for photovoltaics with reproducibility, homogeneity, and multi-wafer processing as the main residual issues [23]. This thesis investigates a texturing recipe using TMAH as the main agent and targets at overcoming and controlling the aforementioned issues with reflectance measurements and SEM being the characterization tools for the texturing quality.

3.2 Benefit of Texturing

Texturing is a measure which aims at minimizing energy losses connected with the reflection of incident light. It leads to reduction of the total reflectance of the solar device,

potential increase of the number of photons that are absorbed in the c-Si substrate and consequently improvement of the cell efficiency [38]. This is realized through the promotion of multiple bounces of the incident light at the highly facetted front surface, as well as the improved light trapping mechanism due to the oblique passage of light through the cell [39] and these two mechanisms are described in the two following sections.

3.2.1 Low Reflectance

In the case of flat polished wafers, approximately 30% of the incident light is reflected. On the contrary, the reflected light from textured surfaces can be significantly reduced to even below 10% in the visible wavelength region.

When light impinges on the facet of the pyramid it either enters the cell or is reflected. If it is reflected it bounces off at an angle and strikes another pyramid located in the close vicinity of the first pyramid where again it can either enter the cell or be reflected. This increases the chances of reflected light bouncing back onto the surface, rather than out to the surrounding air which is the case of the flat wafer, resulting in more chances that a photon of light will enter the cell. *Figure 3.5* presents the mechanism described above which leads to the reduction of light reflection at the surface of a textured solar cell.

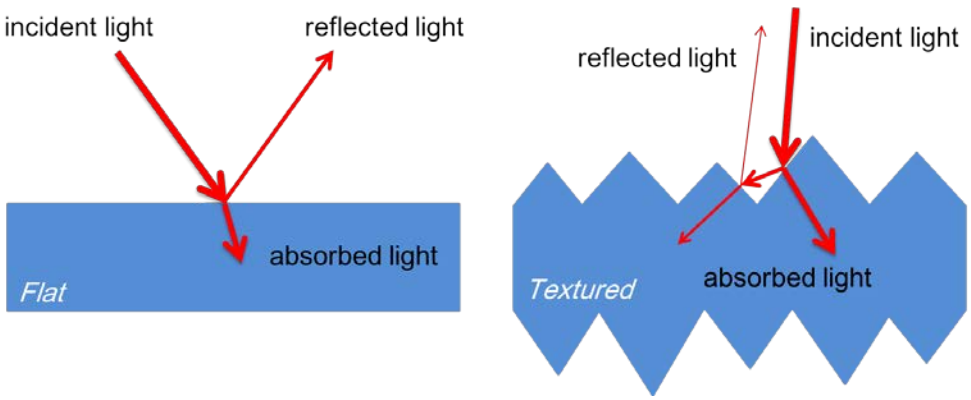


Figure 3.5: Comparison between a flat and a textured c-Si wafer highlighting the larger part of light that is absorbed in a textured wafer due to the pyramidal surface structure.

3.2.2 Enhanced optical path

The second mechanism refers to the enhanced optical path length provided by a textured wafer. Due to the weak absorption of near-infrared light in c-Si an effective light trapping scheme is essential for thin c-Si substrates. This also applies to the *n*- type absorber layer of the SHJ solar cells fabricated in this work having a thickness of approximately 270 µm.

When light propagates in the c-Si substrate, its intensity will be reduced exponentially due to the light absorption in the substrate. This reduction in light intensity when light travels through a medium is described by the Lambert-Beer law (Equation (3.7)).

$$I(x) = I_0 e^{-\alpha x} \tag{3.7}$$

where I_0 represents the initial intensity of the incident light, $I(x)$ is the light intensity of the light travelling through a distance x and α is the absorption coefficient of the medium which refers to the light fraction absorbed in the medium. *Figure 3.6* presents the absorption coefficient of *i* c-Si as a function of wavelength for the wavelength range 300 nm-1200 nm which has almost identical trend with the absorption coefficient of the *n* c-Si absorber layer of the SHJ device measured by *Digdaya* [6].

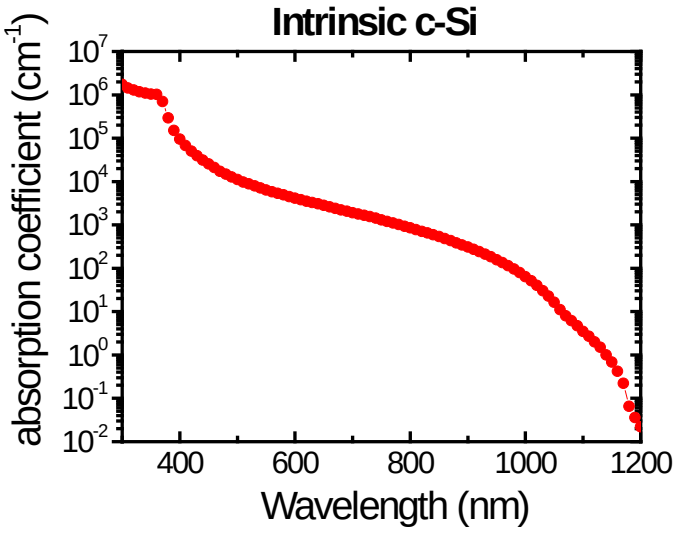


Figure 3.6: The absorption coefficient of intrinsic c-Si. The plotting data are available in [40].

Considering the absorption coefficient of c-Si, the light intensity for high wavelengths can be calculated by applying the Lambert-Beer law. The result leads to the conclusion that texturing is beneficial for trapping light at the near-infrared wavelengths even for an absorber layer thickness of 270 nm while light has not been fully attenuated.

Figure 3.7 represents the cross section of a textured c-Si substrate. The absorbed light is trapped inside the textured absorber layer experiencing multiple reflections on the surface of the pyramid structure. The light stays longer inside the wafer and is attenuated after every internal reflection since it is partially absorbed. In this way the total reflectance of the wafer is minimized [20] and the chance of the photons being absorbed is enhanced [27].

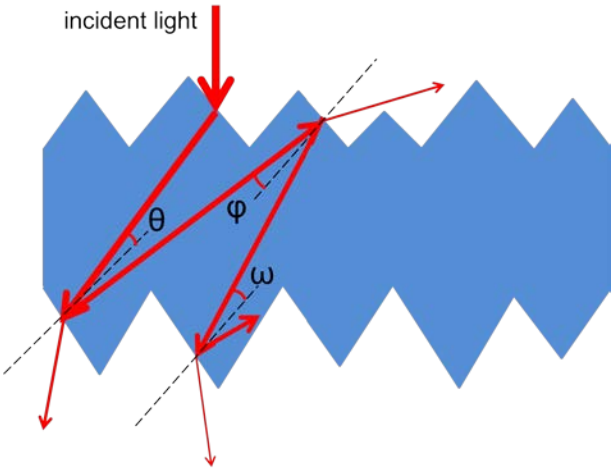


Figure 3.7: Light trapping mechanism of a textured c-Si wafer leading to an increase in the absorption of photons in the absorber layer of the solar cell.

For sake of clarity, only four passes of the trapped light across the wafer are depicted. The angles θ, φ and ω are the angles of incidence at each internal reflection. Total internal reflection of light can occur if the angle of incidence is above a specific angle called the critical angle [41].

Additionally, it has been reported [42] that with both surfaces pyramidally textured and the rear surface reflective, as in the case of a textured SHJ solar cell with a metal back contact, the random pyramid layout allow virtually all the light to be trapped in the cell for at least four passes across it (see *Figure 3.8*).

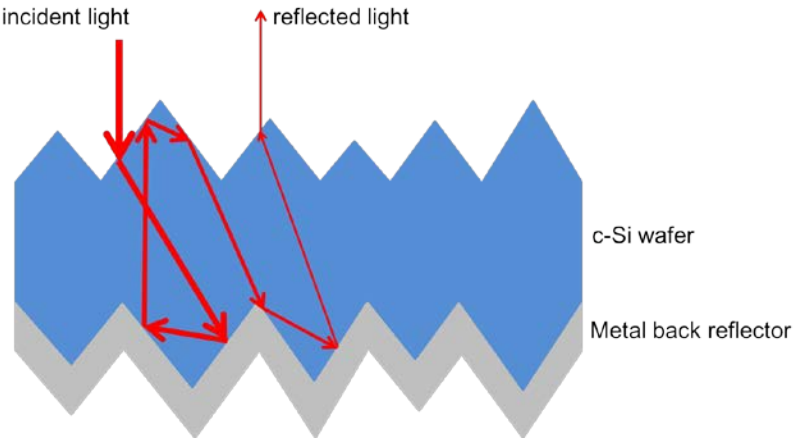


Figure 3.8: Textured c-Si wafer combined with metal back reflector can achieve total internal reflection of the absorbed light for at least four passes of the light while travelling inside the wafer.

These two mechanisms describe the benefit provided by a textured c-Si substrate of a solar cell. They lead to light collection improvement which corresponds to an increase in the e^-/h^+ pairs generation resulting in a higher J_{SC} for the solar cell [20][27].

3.3 Challenging issues introduced by texturing

The optical benefit provided by texturization is partially mitigated by the additional recombination it may invoke [43]. The benefit of the increased J_{SC} provided by texturing is generally offset by a considerable reduction of the V_{OC} of the heterojunction solar cell due to the increased surface defect-state density and its strong impact on the passivation quality at the a-Si:H/c-Si interface [7].

The higher number of surface defect states has been mainly attributed to the higher number of dangling bonds exposed on the (111) facets of a textured surface [43] in comparison with the equivalent (100) surface, considering that the surface area of a randomly textured wafer is 1.73 times greater than the equivalent planar surface of a flat wafer [43][44].

Complicating matters further, the preparation-induced nano-roughness on the facets of a textured wafer may lead to a high level of surface irregularities and higher defect-state density resulting in an a-Si:H/c-Si interface with high recombination [45][46][47][48].

Last but not least, a textured substrate with a surface fully covered with random pyramids creates the additional challenge of ensuring that the surface is correctly cleaned and properly

prepared for the deposition of the ultrathin *i* a-Si:H layer. The cleaning process is an important step before the deposition of the a-Si:H layers, which can improve the passivation of the wafer and therefore increase the V_{OC} of the SHJ solar cell [3].

Thus, this thesis also investigates a post-texturing treatment of the c-Si wafer responsible for the contamination removal, the roughness minimization by surface smoothening and the saturation of dangling bonds at the c-Si surface, prior to the *i* a-Si:H layer deposition targeting at the optimization of the *i* a-Si:H/c-Si interface quality resulting in a higher V_{OC} for the textured SHJ device. The contamination removal, surface smoothening and surface passivation are defined in *Chapter 4* and the way they contribute to the optimization of the a-Si:H/c-Si interface is described.

Chapter 4

Theoretical Background on Cleaning

4.1 Contamination removal

Si wafer cleaning targets at the removal of the contaminants from the semiconductor surface. Wet-chemical, plasma, dry-physical, vapour phase, and supercritical fluid methods have been developed in order to achieve this objective [49]. However, the wet-chemical process is only investigated in this work while being the most widely used method for Si wafer cleaning in the semiconductor industry today [49]. Impurities on Si wafer surfaces essentially exist in the form of particles, organic, and metallic contaminants [47]. According to *Angermann et al.* [50], surface contamination could be completely removed after applying a wet-chemical oxidation step and a subsequent dip in hydrofluoric acid (HF). This means that practically, the wet-chemical cleaning procedure consists of two steps. During the first step, aqueous oxidation of the Si surface occurs and during the second step, the previously grown oxide layer is stripped off with the simultaneous elimination of the surface contaminants.

The standard cleaning process of the Radio Corporation of America (RCA) has been the most commonly used process in the semiconductors industry. The effectiveness of this method in removing particles as well as organic and metallic surface contaminants, has been examined and verified by various analytical methods since 1970 [51]. Another process is called “Piranha etch” known for its voracious ability to eradicate organic impurities and it usually precedes the RCA cleaning treatment [49]. Currently at the PVMD group, the treatment applied for the cleaning of the c-Si substrate of the HJ solar cell is a cleaning procedure involving concentrated and diluted HNO_3 solutions. The three aforementioned processes and modifications of them are compared in order to evaluate their effectiveness on the textured c-Si wafer.

Apart from cleaning, the smoothening of the surface by reducing the nano-roughness on it, is a key parameter for the formation of a high quality *i* a-Si:H/c-Si interface and is described in the following section.

4.2 Surface Smoothening

It has been shown [46][48] that the minimum value of the surface defect-state density on Si substrates is strongly related to the preparation-induced surface nano-roughness and the increased nano-roughness results in higher surface state densities. Nano-roughness refers to the nanoscale irregularities on the silicon surface.

As already mentioned in *Chapter 3*, during the texturing of a (100) oriented Si surface is converted to a surface covered with randomly sized pyramids composed by (111) oriented facets. After a closer inspection of the Si surface, the different dangling bond configuration between (100) and (111) orientation can be observed. *Figure 4.1* illustrates how the texturization of a flat (100) Si surface with two dangling bonds per atom results in a pyramidal structure whose (111) facets expose surface atoms with one dangling bond. The red spheres represent Si surface atoms.

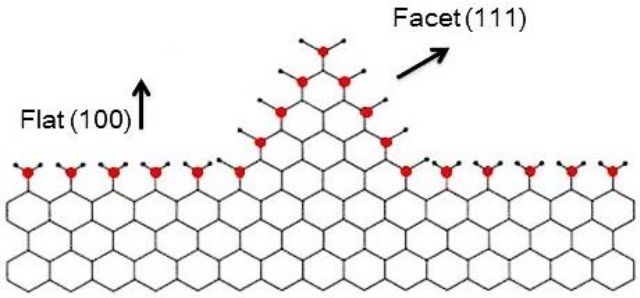


Figure 4.1: The (111) Si pyramidal structure resulting from the texturing of a (100) surface [52].

The ideal case would be the existence of a clean and abrupt pyramidal surface consisting only of the Si surface atoms totally prepared for the passivation of their dangling bonds by the *i* a-Si:H layer, as shown in *Figure 4.1*. Undoubtedly, this scenario is unrealistic considering the conditions that the process is realized. The wet chemical oxidation during the texturing and cleaning procedure and a possible native oxide growth lead to the formation of a Si/SiO_2 interface which extends over only a few angstroms [53]. Surface states are localized in this interlayer resulting from strained ($\boldsymbol{Si_3 \equiv Si - Si \equiv Si_3}$) bonds and dangling bond defects ($\boldsymbol{Si_3 \equiv Si-}$) on Si(111) which are backbonded to Si atoms only [54][55]. Especially, in the case of textured c-Si substrates fully covered with (111)-faceted pyramids, anisotropic etching leads to a strong increase of such irregularities on different crystallographic surface orientations. An

additional roughness would be detrimental for the subsequent surface passivation by the thin *i* a-Si:H layer by increasing the interface recombination [50].

Thus, an optimized cleaning process aims at the removal of the contaminants from the semiconductor surface without damaging the substrate surface. The surface of the wafer must not be affected in such a manner that roughness or other structure irregularities negate the results of the cleaning process. The standard RCA and Piranha cleaning processes are mainly based on H_2O_2-containing solutions which increase the nano-roughness of the Si surface as a side effect to the H_2O_2 decomposition [46][56]. Therefore, special smoothening procedures subsequent to these cleaning treatments are necessary to reduce nano-roughness and minimize the state density on the silicon substrate. Recent investigations [50][57] have shown that the smoothening procedure on textured c-Si substrates prior to a-Si:H deposition in a-Si:H/c-Si HJ solar cells, results in a significant increase of the parameters and efficiency of the solar cell. The last step of the pre-deposition treatment of the textured c-Si substrate is the H-termination of the Si surface and is explained in the third section of the chapter.

4.3 Surface Passivation

Generally, there are two predominant ways to passivate Si surfaces chemically. The first produces a hydrophilic silicon oxide terminated surface easily wetted by aqueous solutions and is achieved by growing a thin layer of SiO_2 using acidic or alkaline solutions mixed with H_2O_2. The second way to passivate the Si surface results in H-terminated surfaces by dissolving the previously grown oxide layer in hydrofluoric acid (HF) or ammonium fluoride (NH_4F) aqueous solutions known for their high etch selectivity of SiO_2 to Si. The H-terminated surfaces are characterized as oxide-free surfaces with dangling bonds passivated with single hydrogen atoms. Furthermore, they are hydrophobic and are not wetted by aqueous solutions [51]. H-terminated Si surfaces have been given highest priority, because of their cleanliness, smoothness and their excellent electrical properties [58]. After anisotropic texturing of (100) c-Si wafer and surface conditioning, a completely dry H-terminated surface is a prerequisite for achieving high-quality surface passivation by intrinsic a-Si:H [59]. However, only Si monohydride ideally exist at the Si surface after H-termination while dihydrides and trihydrides contribute to the increase of the nano-roughness [60] .

For a long time, fluorine (F) termination was considered to be responsible for the chemical passivation and stability of the HF-treated silicon surface. In the late 1980s, H-termination started gaining ground in the debate against F-termination, when it was finally confirmed that the remarkable Si surface passivation is resulted by hydrogen terminated dangling bonds and fluorine is considered as a minor contaminant on the silicon surface [61][62][63]. *Figure 4.2* depicts schematically the reaction mechanism leading to the H-termination of an (111)-oriented silicon surface during HF treatment, firstly proposed by *Ubara et al.* [64].

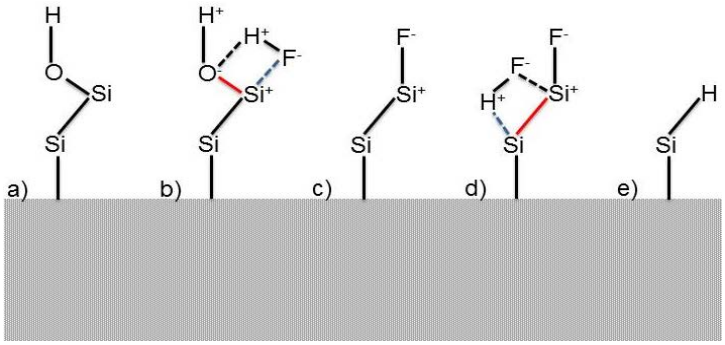


Figure 4.2: H-termination mechanism for passivating dangling bonds at (111) Si surface.

The HF treatment is subsequent to the wet-chemical oxidation of the Si surface. Hypothetically, the reaction starts from the last oxidized Si atom which needs to be broken before reaching the Si substrate (*Figure 4.2*.a). Due to the high electronegativity of oxygen, the Si–O is highly polarized, facilitating the HF molecule attack. Naturally, as a consequence of the Coulomb attraction, the positively charged H atom is associated with the negatively charged O atom and the negatively charged F atom is associated with the positively charged Si atom of the Si–O bond (*Figure 4.2*.b). This releases H_2O into the solution and leaves Si–F in its place on the surface (*Figure 4.2*.c). The large electronegativity difference between Si and F atoms leads to high polarization of the Si-F bond. Proceeding, the Si–Si back-bond is polarized allowing HF attack of the back-bond (*Figure 4.2*.d). The outcome of this reaction is the release of stable SiF_x species into the solution leaving behind H-terminated Si atoms protecting the surface from further chemical attack (*Figure 4.2*.e).

The most common alternative of HF for producing H-terminated Si surfaces is NH_4F solutions. However, NH_4F containing solutions produce various ammonium salts by the reaction with Si and SiO_2 which are deposited on the Si surface. Especially, $(NH_4)_2SiF_6$ salt cannot be removed even by intensive water rinse, because the solubility is relatively low in water and

depends on the concentration and pH of the etching solution. Furthermore, the formation of these deposits seems to start particularly on surface particle contaminations, or on crystallographic irregularities of the structured surfaces [57][60]. Hence, in this thesis, the H-termination of the Si surface occurs in dilute HF solution targeting at the efficient passivation of the c-Si surface preventing the oxidation of the sample before its introduction to the vacuum chamber where the PECVD takes place.

After taking into consideration that a clean, smooth and H-terminated c-Si surface is of great importance for achieving excellent passivation with a-Si:H, this work investigates the development of an optimized pre-deposition treatment of the pyramidal c-Si substrate. The formation of an a-Si:H/c-Si interface with excellent properties requires that the a-Si deposition would be started with a perfectly clean, smooth and undamaged surface.

Chapter 5

Development of the texturing recipe

5.1 Introduction

The first objective of this research is the development of a reproducible recipe for the efficient texturing of the c-Si substrates of the SHJ solar cells without the use of KOH or NaOH. Thus, in order to avoid metallic contamination, aqueous alkaline solution consisting of low concentration of TMAH and IPA is used for the anisotropic etching of c-Si wafers. The development of the texturing recipe is based on *Iencinella et al.* [20] and *Rosa et al.* [37] where low reflectance values are reported by using TMAH as the main agent for texturing.

According to *Zubel and Kramkowska* [34], it is assumed that in an aqueous TMAH solution, the components OH^-, H_2O, TMA^+ and $SiO_2(OH^-)_2^{2-}$ coexist and all of them interact with the Si surface by adsorption or desorption. Apart from the oxidation and reduction reactions during Si etching, simultaneously adsorption of reactive and non-reactive particles (TMA^+) on the Si surface occurs as well as desorption of etching products ($SiO_2(OH^-)_2^{2-}$) from the surface. Theoretically, the optimized texturing can be achieved when equilibrium is reached between the adsorption of OH^- ions and H_2O molecules and the adsorption of TMA^+ ions on the Si surface. Si etching in high TMAH concentrations (above 25%) results in very good morphology and smooth pyramidal surface. It has been suggested that this occurs due to the enhanced adsorption of TMA^+ ions on the Si surface decreasing the etching rate by hindering the aggressive attack of OH^- ions on the surface. On the other hand, in low TMAH concentrations, the adsorption rate of OH^-/H_2O exceeds the adsorption rate of TMA^+ on the Si surface due to scarcity of TMA^+ ions resulting in a higher etching rate and rough pyramidal surface. Therefore, IPA is added to the solution without participating in any of the oxidation or reduction step of the texturing process but acting as a surfactant and playing the role of the missing TMA^+ ions.

However, finite amount of IPA should be added to the solution because at very high IPA concentrations the adsorption rate of IPA particles on the Si surface exceeds that of OH^-/H_2O,

the access of OH^-/H_2O on the surface is restricted and consequently the etching process will be hindered. Thus, in order to develop a low cost and efficient texturing recipe, the optimum amount of IPA is investigated for a fixed low TMAH solution concentration.

5.2 Experimental Process

The etching experiments are carried out in a 3 l borosilicate glass (Pyrex) beaker equipped with a magnetically stirring bar and a lid especially designed to seal the beaker and limit evaporation. The beaker is placed on a stirring hot plate and the etching conditions are constantly set at 100 rpm and 80°C for the agitation and temperature, respectively. A thermocouple is also inserted in the etching solution for monitoring its temperature. All the samples are 4" diameter double-side polished FZ c-Si (100) wafers, n-type, with 1-5 Ωcm resistivity and a thickness of 280±20 μm. The wafers are mounted on Teflon sample holders and textured in a mixture made up of high purity (18 MΩ) deionized (DI) water and commercial solutions of 25% TMAH and 99.9% IPA. Before the texturing process, all the samples are dipped in a 0.5% HF solution for 90 s at room temperature (RT) to remove the native oxide and after the etching process the samples are rinsed in DI water for 120 s. Although the set-up allows the simultaneous etching of two full wafers, half wafers are used before attaining the optimized recipe for texturing. The main parameter under investigation is the IPA concentration in a solution with a fixed TMAH concentration of 5% for keeping cost low and etching conditions (agitation, temperature) as mentioned above. After every trial the texturing quality is characterized by measuring the total reflectance of the sample and using SEM when available. An optical microscope is also used for capturing images but only the most substantial are reported here due to their low resolution.

Although the spectral reflectance $R(\lambda)$ for the wavelength range 300 nm-1200 nm is measured for every sample, the average reflectance ($R_{350nm\text{-}1100nm}$) for the wavelength range 350 nm-1100 nm is mainly reported for the evaluation of the texturing result. While the E_g of Si is 1100 nm (1.12 eV), the $R_{350nm\text{-}1100nm}$ is generally used in literature [23][36] for reporting the efficiency of the pyramidal morphology achieved in TMAH solutions. $R_{350nm\text{-}1100nm}$ is calculated by *Equation 5.1*:

$$R_{350nm-1100nm} = \frac{\int_{350}^{1100} R(\lambda) d\lambda}{\int_{350}^{1100} d\lambda} \quad (5.1)$$

5.3 Results and Discussion

The first three samples are etched one after another for 45 min each, in a fresh solution of 5% TMAH without the addition of IPA. Optical microscopy images (see *Figure 5.1*) show a surface with flat regions and regions with accumulated pyramids. The ratio of the pyramidal area to the untextured area shows a tendency to increase at the second sample and even more at the third sample.

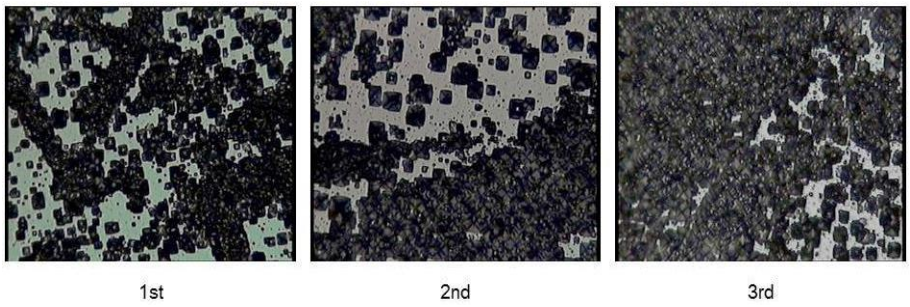


Figure 5.1: Optical microscopy images show the surface morphology of three wafers after being textured in fresh 5% TMAH solution for 45 min each.

More trials are executed using fresh TMAH solution and larger number of samples each time. The results indicate a surface with non-homogeneous texturing, especially on the wafers textured first. The surface homogeneity is continuously improved while more wafers are being textured in the same solution. This is in agreement with the hypothesis reported in [20] that dissolved Si in the TMAH solution increases the effectiveness of the anisotropic etching. However, the exact mechanism is not clear yet. The dissolved Si coming from the wafer during the etching process in a fresh solution is not enough to promote a homogeneous texturing.

After adding a few Si pieces in a fresh solution and leaving the etching solution to dissolve some Si from the pieces first, a homogeneous pyramidal structure is grown on the surface of even the first wafer that is immersed in the fresh solution. Thus, 0.5 g of Si is added to the beaker every time a fresh TMAH solution is prepared.

So far, a quite homogeneous texturing can be acquired in a 5% TMAH solution with the c-Si surface fully covered with pyramids in 45 min. However, every etched sample presents a rough texturing and even spots corresponding to damaged regions can be observed under optical microscope. In low TMAH concentrations (5%), the adsorption rate of OH^-/H_2O exceeds that of TMA^+ on the Si surface, the aggressive Si etching by OH^- is enhanced resulting in a rough texture. Even though, $R_{350nm-1100nm}$ values below 15% are measured for these TMAH-treated samples, a smooth pyramidal structure is a fundamental prerequisite for the formation of high quality a-Si/c-Si interface in the SHJ solar cell.

It has been stated [34][65] that a smooth pyramidal structure is obtained with IPA addition in low TMAH concentration solutions at the cost of slight reduction of etching rate. In order to attain the optimized IPA concentration for a 5% TMAH solution the IPA concentration range 0.8%-16.7% is examined.

After many trials, optical microscopy images (not reported here) shows that IPA 7.4% is the lowest concentration which results in a smooth textured surface. A complete coverage of the wafer with pyramids of dimensions approximately 5-10 μm is obtained at 60 min of etching. For IPA 7.4%-10%, similar results are obtained concerning the surface smoothness but further reduction in etching rate is observed as the concentration increases and more time is needed for the wafer to be fully covered with pyramids. For even higher concentrations, the etching process is retarded even more and it is practically impossible to obtain a fully textured surface within a reasonable timeframe. This may be attributed to the fact that higher IPA concentrations are close to the saturation level and the adsorption rate of non-reactive IPA/TMA^+ on the Si surface exceeds that of OH^-/H_2O. Consequently, the access of OH^-/H_2O on the surface is limited and the etching process is hindered.

The smooth texturing realized in the aqueous solution of 5% TMAH and 7.4% IPA is verified using SEM and the captured images are depicted in *Figure 5.2*. From the top and angular view of the etched surface it can be observed that the pyramids appear with quite smooth facets and no damaged region exists on the surface. The faint white spots which can be distinguished on the pyramids should be dust particles.

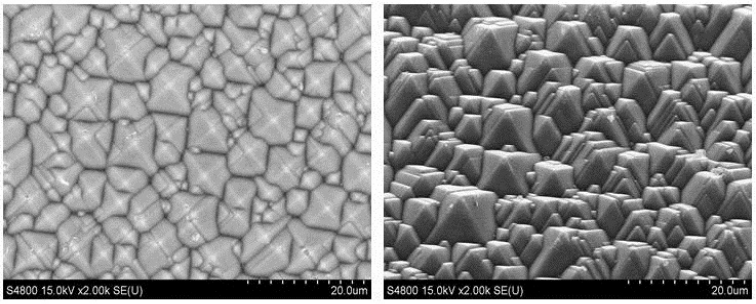


Figure 5.2: SEM images present (a) the top view and (b) the oblique view of the smooth pyramidal structure of wafer surface after being textured in an aqueous solution of 5% TMAH and 7.4% IPA for 60min.

Furthermore, the total reflectance of the textured sample is measured on three different spots (see *Figure 5.3*). The three different reflectance curves look identical. The lack of spread among the reflectance measurements of the three different spots implies the truly homogeneous texturing that is achieved and at the same time $R_{350nm-1100nm}$= 11.8% is obtained. This value is really low comparing with reflectance measurements on TMAH textured samples reported in literature [23][36]. Similar results are obtained after repeating the same process for a set of ten samples.

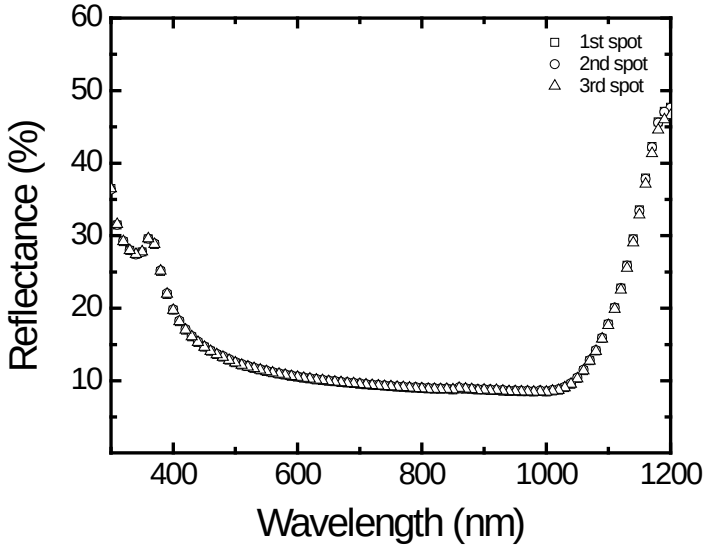
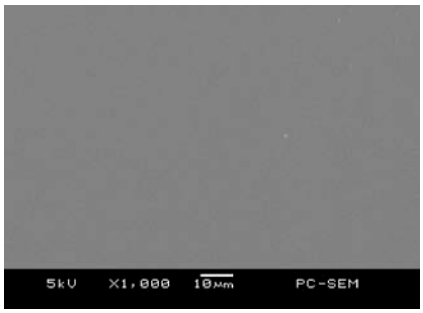
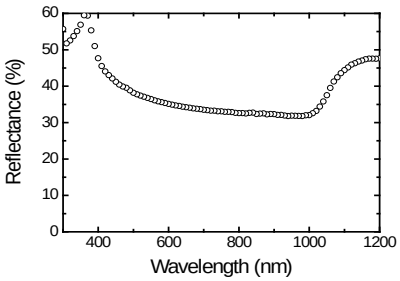
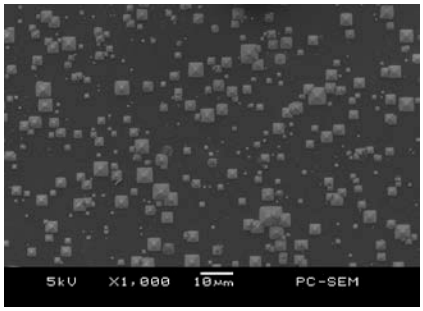
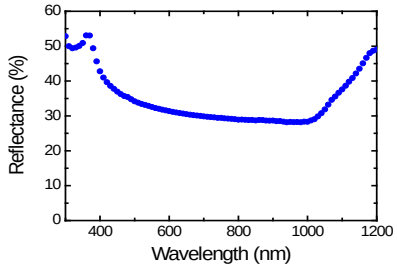
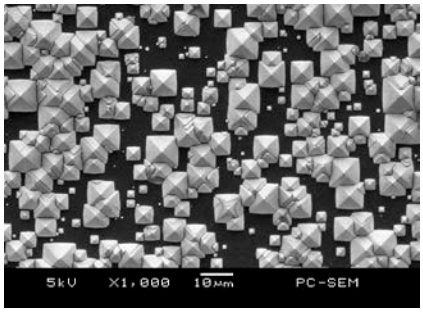
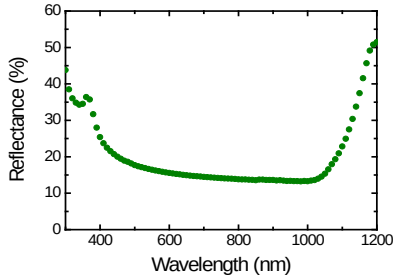


Figure 5.3: Total reflectance measured for 3 different spots of the sample textured in 5% TMAH and 7.4% IPA for 60 min.

Subsequently, in order to monitor the progress of the pyramids formation during texturing and find the optimum etching time, three half wafers are cut in the middle creating six samples of

approximately the same dimensions. These six samples are immersed together in a fresh solution of 5% TMAH and 7.4% IPA at t=0 min (t=time). Every 15 min a sample is removed until t=90 min. The sample for t=0 min corresponds to the double-side polished wafer. At the end of the experiment, SEM images are captured and reflectance measurements are conducted for each different sample.

The results are presented in *Table 5.1*. Before capturing a SEM image, a scan over the entire surface of the sample is performed to ensure the surface homogeneity. Thus, every image reported in *Table 5.1* is representative of each sample. Also, the reflectance measurements presented in *Table 5.1* correspond to the average reflectance of three spots on each sample and minimum spread is again observed among the three measurements.

Etching Time	*Surface Morphology*	*Reflectance Measurements*
0 min		
15 min		
30 min		

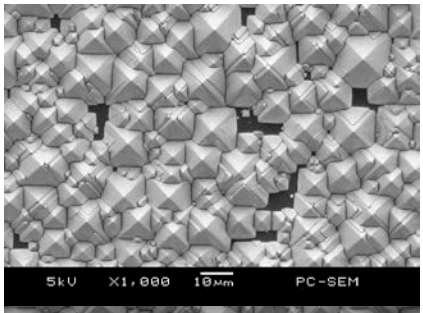
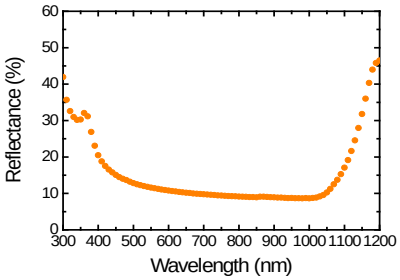
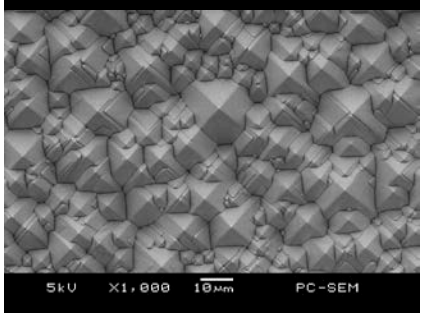
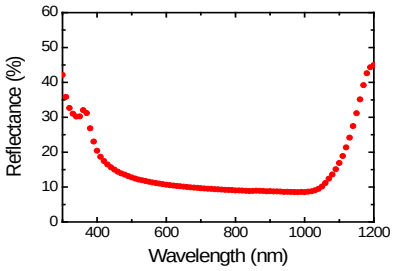
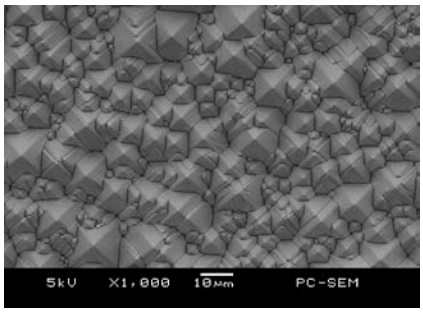
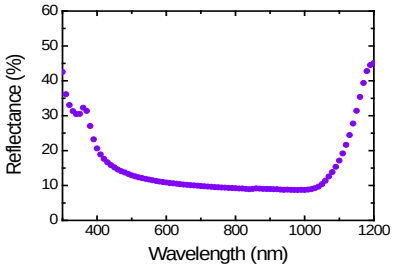
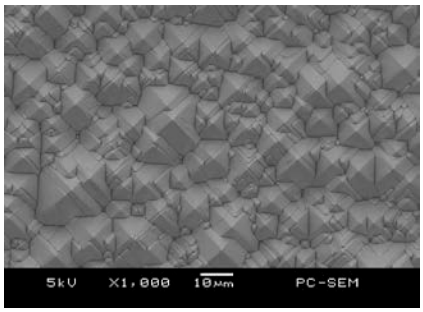
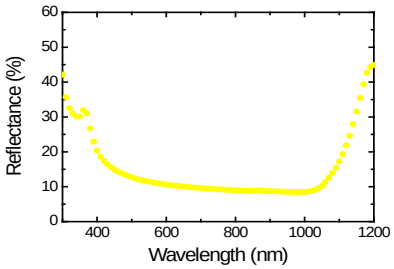
45 min		
60 min		
75 min		
90 min		

Table 5.1: SEM images and reflectance measurements for the monitoring of the etching progress in a solution of 5% TMAH and 7.4% IPA for the time range t=0-90 min.

As it can be observed from the SEM images, flat regions are present even after 45 min of texturing while a full coverage of the surface with pyramids is achieved at t=60 min. When the sample is fully covered with pyramids, the surface is dominated by (111) atoms. Considering that the etching rate of (111) orientation is much lower compared to that of (100) direction [31], etching the samples 30 min further will not result in any distinguishable changes of the surface morphology. However, etching the sample without a time limit will lead to the total consumption

of Si and the sample will be disappeared, as it is verified experimentally. The time required for this is dependent on the etching rate of Si under specific etching conditions.

Furthermore, by plotting all the reflectance curves from *Table 5.1* in the same graph (see *Figure 5.4*) the reflectance is drastically reduced after 30 min of etching and similar results are acquired for the samples etched for 45 min-90 min corresponding to very low reflectance.

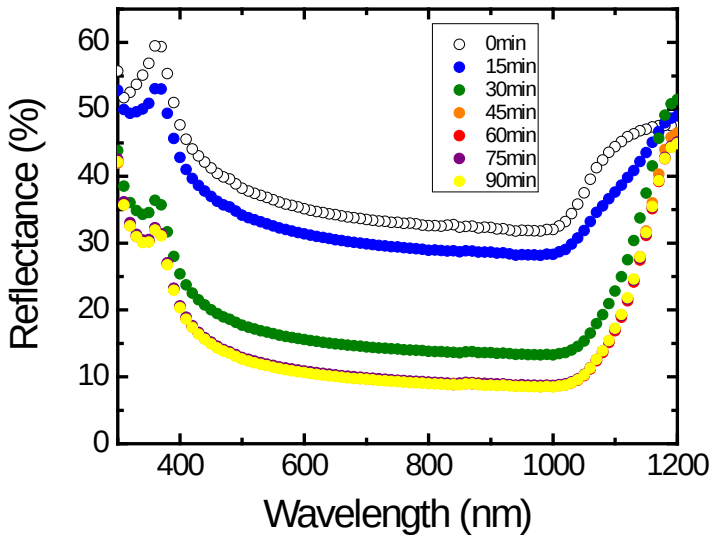


Figure 5.4: Reflectance measurements of the samples etched in 5% TMAH and 7.4% IPA for different time.

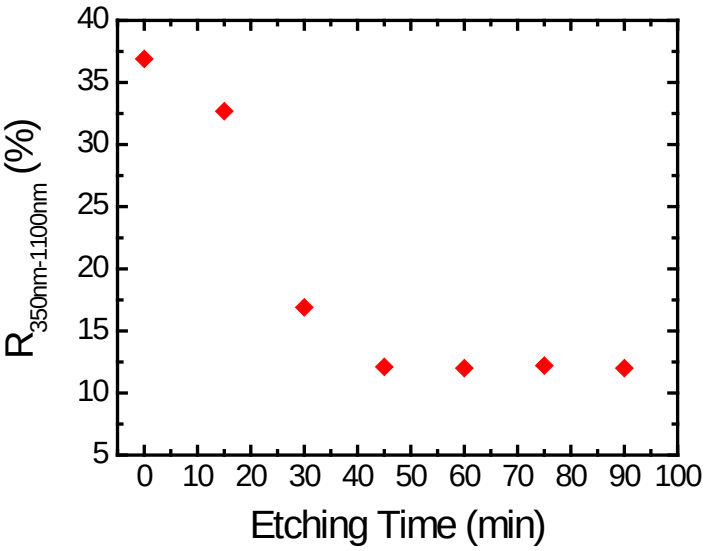


Figure 5.5: Average reflectance for the wavelength range 350 nm-1100 nm vs. etching time in 5% TMAH and 7,4% IPA.

Figure 5.5 also reports $R_{350nm-1100nm}$ as a function of the etching time in 5% TMAH and 7.4% IPA. Reflectance decreases rapidly between 15 and 45 min of etching, and then it stabilizes around 12%.

Comparing results in *Table 5.1* and *Figure 5.5*, 60 min etch is sufficient to cover the whole surface of the sample with pyramids and at the same time minimum reflectance is achieved. Low reflectance is also measured for a 45 min etch. However, a textured substrate with flat regions will not be compatible with the fabrication of the optimal SHJ device while untextured areas will lead to the growth of a thicker a-Si:H layer at these regions resulting in higher parasitic absorption of the light and a higher series resistance. Thus, etching in an aqueous solution of 5% TMAH/7.4% IPA at 100rpm/80^{o}C for 60 min provides the optimum result, a homogeneous and smooth texturing with $R_{350nm-1100nm} \simeq$ 12%.

For the investigation of texturing reproducibility, two sets of samples consisting of ten half wafers each are prepared. The first ten samples are textured two by two in a 5% TMAH/7.4% IPA solution at 100rpm/80^{o}C for 60min. The experiment is repeated with the second set of samples being etched in a newly prepared solution with the same composition as the previous one and under the same conditions. *Figure 5.6* reports the deviation of the reflectance measurements above and below the average spectral reflectance of the 20 samples.

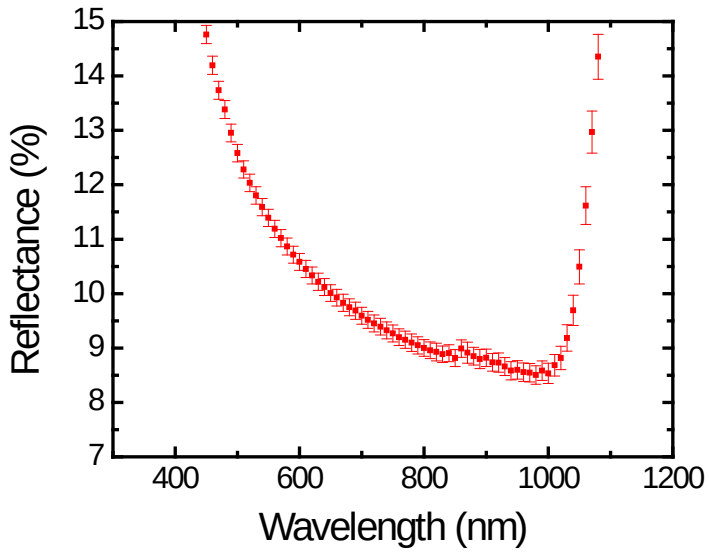


Figure 5.6: Total reflectance of 20 samples textured in 5% TMAH/7.4% IPA at 100rpm/80^{o}C for 60 min showing the deviation (red bar) from the average value (red square) at every measured wavelength.

A reflectance spread less than 1% at every wavelength indicates that a reproducible texturing can be achieved under the specified conditions. A restricted but representative range of reflectance data is only illustrated so that graph features can be distinguished.

Concluding, an optimized recipe is reported for c-Si wafer random pyramidal texturing. A reproducible, smooth and homogeneous pyramidal structure with $R_{350nm-1100nm} \simeq$ 12% is obtained after 60 min of etching in 5% TMAH/7.4% IPA at 100rpm/80^{o}C. Indispensable ingredient of the texturing recipe is the 0.5 g of Si added every time a fresh solution is prepared. When a new solution is prepared, warming up and stirring is required under the specified conditions for 2-3 hours. The immersion of the samples occurs the day after. This process ensures a good mixing of the agents and a sufficient amount of dissolved Si coming from the pieces in the solution.

Full (4") c-Si wafers can be also textured with the same recipe. The pyramidal structure and reflectance measurements are similar to the results reported here. Considering that the current set-up allows simultaneous etching of two full wafers, the production of two full textured substrates every 60 min is quite efficient for lab-scale texturing.

Finally, it should be noted that at this stage of experimental work, the roughness on the wafer and the pyramids facets is evaluated only under the characterization tools (SEM, optical microscope) enabling only the microscopic view of the surface and the observation of micro-scale features and is different from the nano-roughness which corresponds to the nano-irregularities of the surface as discussed in *Chapter 4.*

Chapter 6

Development of the pre-deposition treatment

6.1 Introduction

After developing a texturing recipe which produces substrates having a homogeneous pyramidal surface and low reflectance, next step is the investigation of a treatment which ensures the preparation of a clean, smooth and well-passivated pyramidal c-Si surface as well as the subsequent formation of high quality a-Si:H/c-Si interface of the SHJ device. Such a treatment, as discussed in *Chapter 4*, targets at removing surface contamination, diminishing any nano-roughness that may exist on the pyramids and H-terminating the c-Si surface. Ideally, this should be achieved without causing any further damage to the surface mainly due to the preparation-induced nano-roughness of H-terminated Si surfaces which results from the wet-chemical oxidation of the Si surface as well as the etching behaviour of Si oxide and Si substrate [66].

In order to develop an efficient treatment of the textured absorber layer prior to *i* a-Si:H deposition, popular wet-chemical cleaning procedures RCA and Piranha which are used extensively in semiconductors industry, the cleaning process currently used at the PVMD group and combinations of them are investigated. The PVMD cleaning procedure is used as reference and will be called NAOC (nitric acid oxidation cycle) for the sake of brevity.

The efficiency of each treatment is evaluated and monitored by measuring the minority carrier lifetime with Sinton instrument. Every textured substrate, after undergoing a specific treatment, is passivated by thick enough *i* a-Si:H layers at both sides. Subsequently lifetime measurement is conducted. The effective lifetime reflects the recombination level of a sample. As explained in *Section 2.2.3,* the effective carrier lifetime of a sufficiently pure c-Si substrate is limited by the recombination at the surface of the wafer while the bulk recombination can be considered negligible. For the *i* a-Si:H/c-Si/*i* a-Si:H stack, by using high quality FZ wafers, a high bulk lifetime is ensured so that the effective carrier lifetime is limited by the a-Si:H/c-Si interface recombination. A higher lifetime measurement corresponds to a less defective a-Si:H/c-Si interface implying a more efficient pre-deposition treatment.

6.2 Experimental Process

Half c-Si wafers whose characteristics described in *Chapter 5* are textured in the already developed recipe of 5% TMAH/ 7.4% IPA. Afterwards, RCA, Piranha, NAOC and combinations of these treatments are applied to the wafers. RCA consists of two standard cleaning steps SC-1 and SC-2. SC-1 and SC-2 steps are performed with a 1:1:5 solution of NH_4OH (ammonium hydroxide), H_2O_2 (hydrogen peroxide), DIW, and a 1:1:6 solution of HCl (hydrochloric acid), H_2O_2, DIW, respectively, at 80°C for 10 min each. As an intermediate step between SC-1 and SC-2, wafers are dipped in 0.5% HF at RT for 60 s in order to remove the oxide layer grown previously in SC-1. SC-1 and SC-2 are prepared by mixing commercial solutions of 35% NH_4OH, 30% H_2O_2 and 37% HCl. RCA steps are summarized in *Table 6.1*.

RCA steps	**SC-1** 1:1:5 of $NH_4OH:H_2O_2$:DIW at 80°C	**Intermediate HF 0.5%**	**SC-2** 1:1:6 of $HCl:H_2O_2$:DIW at 80°C
Step Duration	10 min	60 s	10 min

Table 6.1: Steps of RCA treatment.

Piranha treatment is realized in a 1:3 solution of concentrated H_2SO_4 (sulfuric acid) and 30% H_2O_2 for 20 min at approximately 120°C. For both RCA and Piranha, the set-up configuration is the same as for the texturing solution. Finally, NAOC consists of a 10 min step in concentrated HNO_3 at RT and a 10 min step in 69% HNO_3 at 110°C. Every treatment step is followed by rinsing of the textured substrate in DIW for 4 min. Last step of every process is the H-termination of the Si surface in 0.5% HF at RT for 75 s.

After every treatment *i* a-Si:H layers are grown with PECVD symmetrically on both sides of the wafer to standard thicknesses of around 50 nm. Ultrathin *i* a-Si:H layers with a thickness of 6 nm unprotected by the doped (*n* and *p*) layers of a SHJ device are quite unstable when they are exposed to air and are not suitable for practical use. Thus, at this stage of experimental work *i* a-Si:H 50 nm thick are fabricated for the passivation of c-Si surface in order to monitor the a-

Si:H/c-Si interface quality and ensure that any change in the lifetime would be attributed to interface recombination and not to post-oxidation effects of the a-Si:H/c-Si interface [44].

Afterwards, the effective carrier lifetime of the samples is measured under transient mode. “Pre/post-annealing” and “stable” lifetime measurements are reported here. The first refer to the measurements realized prior to and after annealing of the samples at 170 ^{o}C for 1 h and the latter correspond to the results obtained by measuring the lifetime one month after the samples fabrication. Annealing occurs one day after samples fabrication and is a heat treatment that improves dangling bond passivation due to local redistribution of the hydrogen of the *i* a-Si:H at the a-Si:H/c-Si interface. According to *De Wolf and Kondo* [67], pre/post-annealing lifetime measurements are a straightforward way to determine the abruptness of a-Si:H/c-Si interface. A higher post annealing lifetime implies an abrupt a-Si:H/c-Si interface and consequently better c-Si surface passivation. On the other hand, stable lifetimes are considered as the most representative measurement of the a-Si:H/c-Si interface quality. After sample fabrication and annealing treatment, a month is assumed to be enough time for the lifetime to be degraded and “stabilized” at a certain range where no remarkable changes occur so that stable lifetime measurements can be considered suitable for the comparison of the different pre-deposition treatments.

6.3 Results and Discussion

The experimental process starts with the investigation of the impact of NAOC, Piranha and RCA treatments on the textured c-Si substrate. Furthermore, samples are treated with Piranha and RCA followed by NAOC with an intermediate step of 0.5% HF dip for 3 min. Finally, a treatment consisting of two runs of NAOC (2x NAOC) with the aforementioned intermediate HF step is realized.

As it can be observed in *Figure 6.1*, considering the lifetime measured for the reference NAOC treatment, a really low lifetime is obtained after Piranha treatment. This may be attributed to the contamination of the pyramidal c-Si surface by the sulphur contained in Piranha solution. Furthermore, a certain kind of nano-roughness caused by the decomposition of H_2O_2 as reported in [68] may have also led to an a-Si:H/c-Si interface with increased recombination. When Piranha is followed by NAOC, an improvement of the lifetime is noticed possibly due to

smoothening of the surface and partial or total removal of the suphuric contaminats from it, resulting in a less defective a-Si:H/c-Si interface.

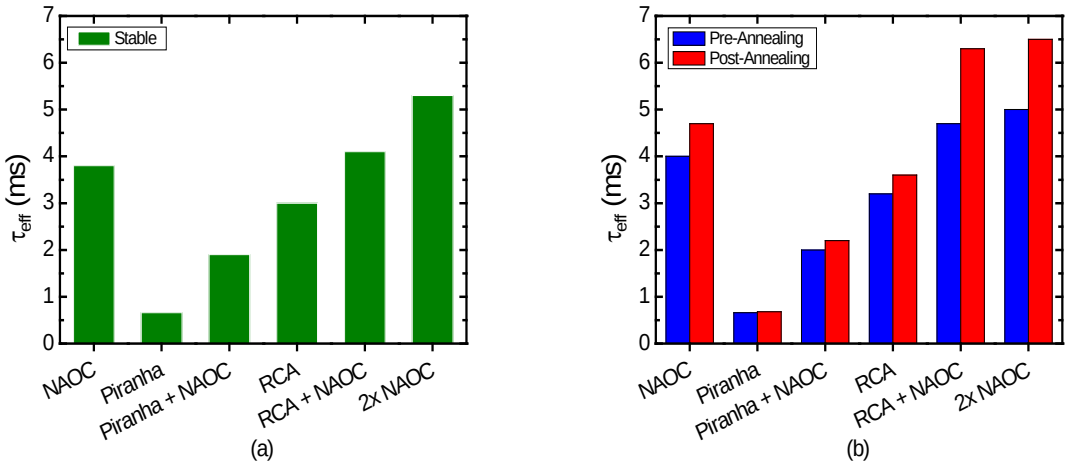


Figure 6.1: (a) Stable and (b) pre/post-annealing lifetime measurements for the 1st series of textured samples after being treated with NAOC, Piranha, "Piranha+NAOC", RCA, "RCA+NAOC" and "2x NAOC".

RCA, the most widely used cleaning treatment in industry, results in a lifetime comparable with lifetime measured after the reference treatment. The high contamination removal efficiency of RCA is mainly associated with the continuous oxidation and oxide removal by H_2O_2 and NH_4OH agents respectively in SC-1. However, a possible nano-roughness induced by the decomposition of H_2O_2 may result in a limitation of the interface lifetime that can be achieved. A further improvement of the lifetime when RCA is followed by NAOC and the highest lifetime of 5,3 ms that is measured after the "2x NAOC" treatment reflect the benefit provided by the textured surface treatment in the particular HNO_3 solutions.

The pre/post-annealing measurements in *Figure 6.1*, indicate an abrupt a-Si:H/c-Si interface for all treatments while the lifetime increases after annealing the samples in all cases. The abruptness of a-Si:H/c-Si interface is mainly influenced by the surface morphology of the c-Si substrate and the growth conditions of a-Si:H layer on it which can be assumed to be identical for all the samples. Nevertheless, the higher lifetime improvement after annealing the samples treated by "RCA+NAOC" and "2x NAOC" witnesses a better quality of the a-Si:H/c-Si interface comparing with the other treatments.

Considering “RCA+NAOC” and “2x NAOC” as the main candidates for the optimal treatment, the latter results in a higher lifetime and its set-up already existed in the lab. Thus, the complex RCA process can be eliminated and further investigation is based on the multiple runs of NAOC treatment. From one to five runs of NAOC are performed and a step of 0.5% HF dip for 3 min is realized between every two runs. NAOC, “2x NAOC”, “3x NAOC”, “4x NAOC” and “5x NAOC” correspond to the different number of cycles of HNO_3 treatment and the results are reported in *Figure 6.2*.

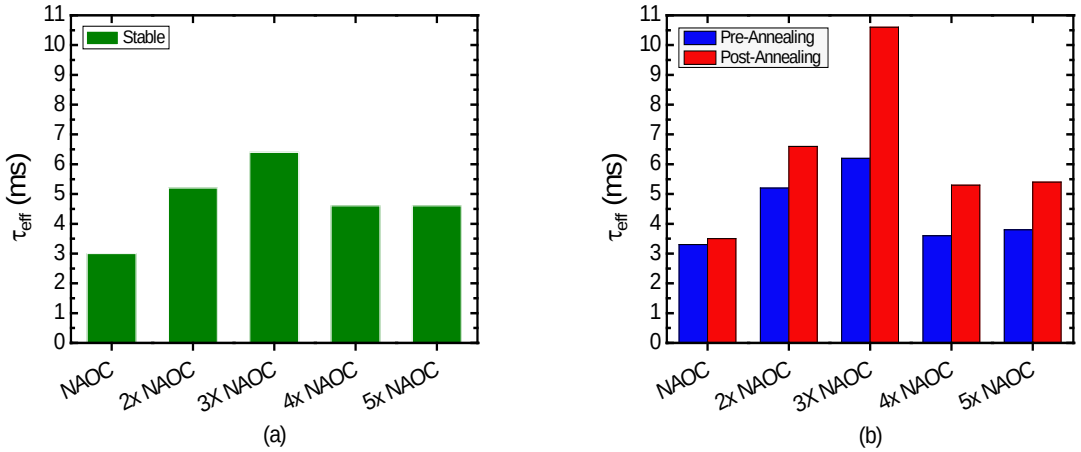


Figure 6.2: (a) Stable and (a) pre/post-annealing lifetime measurements for the 2nd series of textured samples after being treated with NAOC, “2x NAOC”, “3x NAOC”, “4x NAOC” and “5x NAOC”.

As depicted in the stable lifetime graph, the effective lifetime increases as the number of runs of NAOC increases, reaches a peak for a HNO_3 treatment consisting of three sequential cycles and subsequently the measured lifetime becomes lower and seems to be stabilized for treatments of four and five runs of NAOC. Pre/post annealing lifetime measurements show the quality of the a-Si:H/c-Si interface emphasizing the lifetime measured for the “3x NAOC” whose lifetime is almost doubled after annealing.

In order to develop an overview of the lifetime range that would be considered as optimal for the textured substrates, a comparison with the lifetime measured in case of a perfectly abrupt (111) flat substrate is realized. Two (111) double-side polished samples are treated with NAOC and “2x NAOC” and passivated with *i* a-Si:H of the same thickness as for the textured samples. The results are presented in *Figure 6.3* together with the lifetime measurements already presented in *Figure 6.2* for a visual comparison between textured and flat samples.

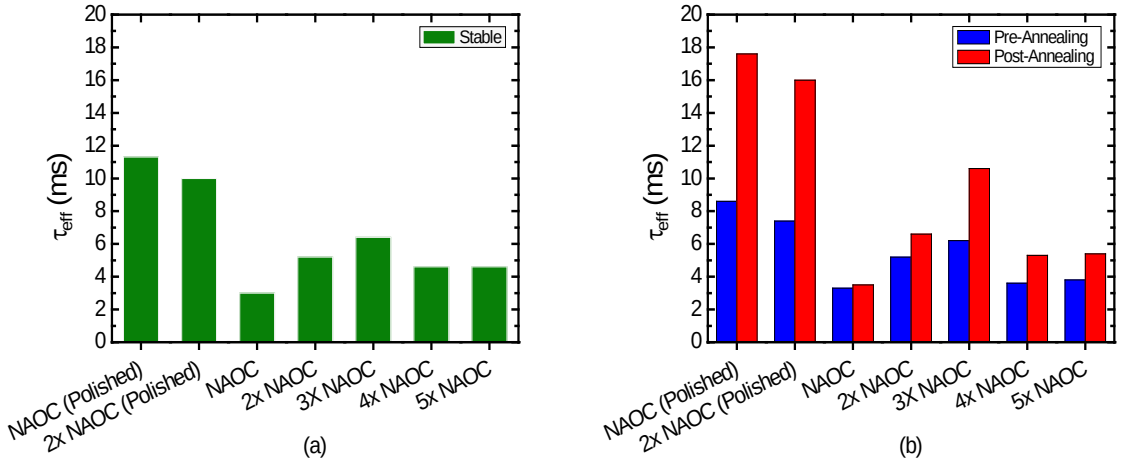


Figure 6.3: (a) Stable and (b) pre/post-annealing lifetime measurements of (111) polished samples after being treated with NAOC and "2x NAOC" and are incorporated in the same graph with the 2nd series of textured samples for visual comparison.

The reference NAOC treatment currently used for the flat SHJ device fabrication at the PVMD group results in a stable lifetime of 11.3 ms for the polished sample and a lifetime reduction is observed after the "2x NAOC" treatment. A polished (111) c-Si surface can be considered as an atomically flat surface presenting almost no atomic scale irregularities. The almost perfect underground of a polished wafer prepared for the a-Si:H growth and the high quality of the a-Si:H/c-Si interface are reflected by the pre/post-annealing lifetime measurements where a relative increase over 100% is observed for the polished samples while for the textured samples the lifetime increase is limited to a certain level. When this surface is exposed to NAOC, oxidation in HNO_3 occurs with subsequent removal of the oxide layer and the simultaneous surface H-termination in HF for 75 sec. The results in *Figure 6.3* reveal that further oxidation of the polished surface and the 3 min intermediate step of the HF dip possibly deteriorate the surface.

It has been reported [69][70] that oxidation of atomically flat (111) c-Si in 69% HNO_3 at 120^{o}C results in the formation of an atomically smooth Si/SiO_2 interface as well as a smooth surface after stripping off the oxide layer in 0.5% HF. In the case of NAOC, the oxidation in 69% HNO_3 is realized at 110^{o}C, and as the temperature difference is limited it can be assumed that the behaviour during the process is similar. Thus, regarding the polished sample, the "black sheep" of the "2x NAOC" treatment seems to be the intermediate HF step during which nano-roughness may be induced leading to a more defective a-Si:H/c-Si interface. Treatment time is a crucial parameter for the nano-irregularities induced on HF-treated c-Si (111) surfaces [61][47].

An intermediate HF dip with a duration of 3 min seems to be more than enough for the removal of the oxide layer grown during the first run of “2x NAOC” and a further HF treatment after stripping off the oxide completely may cause damage on the surface resulting in a lower lifetime. Concerning textured samples, a pyramidal surface with already existing roughness due to texturing is exposed to the multiple runs of NAOC. Instead of “2x NAOC” treatment, three runs of NAOC consisting of two intermediate HF steps are needed for achieving an optimized pyramidal surface and the highest lifetime for the a-Si:H/c-Si interface. On the other hand, further treatment with more than three runs of NAOC leads to the deterioration of the surface and a lower lifetime.

Now, setting the lifetime of 11.3 ms of the polished sample as an upper limit for the development of an efficient treatment for the textured substrate, “3x NAOC” appears to meet the requirements for an optimized treatment for the substrates textured with the already developed recipe. As already mentioned in *Chapter 3*, the surface area of a randomly textured wafer is 1.73 times greater than the equivalent planar surface of a flat wafer. Assuming that the number of textured surface defects is 1.73 larger than the number of defects on the equivalent flat surface, it is almost impossible to achieve the same surface passivation under the same preparation conditions for the textured and flat substrate. Considering only the area factor as the main responsible for the difference between the optimal lifetimes measured for the flat and textured samples, the optimal quality of the a-Si:H/c-Si interface of a textured substrate would be 1.73 times lower than the optimal quality of the a-Si:H/c-Si interface of the equivalent flat substrate. Thus, concerning the lifetime measurements, “3x NAOC” can be characterized as optimal treatment for the textured substrates providing a lifetime of 6.4 ms which is approximately 1.73 times lower than the lifetime of 11.3 ms achieved for the polished substrate.

In order to check the reproducibility of the different NAOC treatments for the textured surfaces, the previous experiment is repeated for the “2x NAOC”, “3x NAOC”, “4x NAOC” and “5x NAOC” treatments. The results shown in *Figure 6.4* present the same trend for the “2x NAOC” and “3x NAOC” while lifetime measurements for the “4x NAOC” and “5x NAOC” are higher in comparison with the results obtained from the samples which were previously exposed to the same treatment. However, next chapter describes the fabrication of SHJ devices after multiple runs of NAOC and the highest device lifetime is measured again after the “3x NAOC” treatment. This topic will be discussed more extensively in *Chapter 7*.

Thus, at this experimental stage, the increasing trend of the lifetime that is observed as the number of runs of NAOC increases cannot be attributed to a particular reason and further investigation of the surface quality after every step of NAOC should be performed.

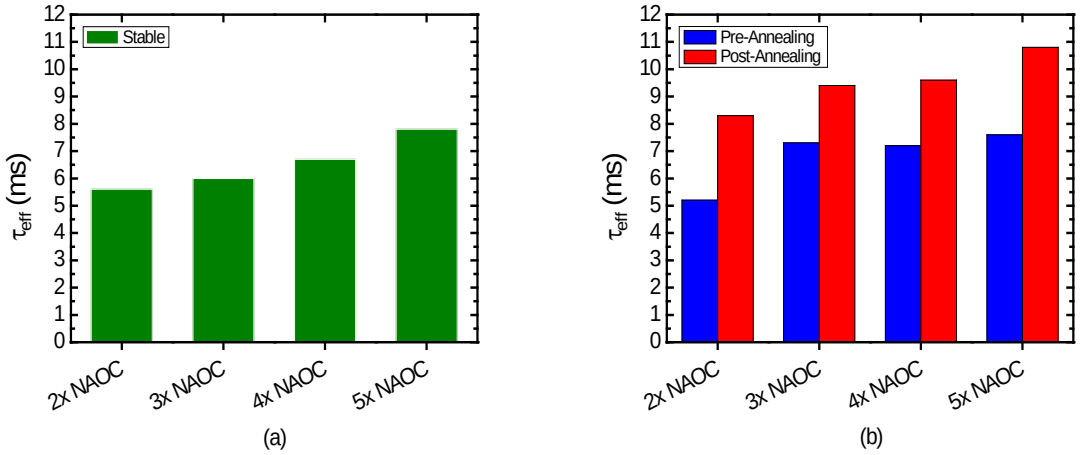


Figure 6.4: (a) Stable and (b) pre/post-annealing lifetime measurements of the 3rd series of textured samples after being treated again with "2x NAOC", "3x NAOC", "4x NAOC" and "5x NAOC" for the examination of treatments reproducibility.

Summarizing, *Figure 6.5* illustrates the average lifetime measurement of every treatment and the deviation from it after conducting the same experiment twice for the evaluation of the treatment consisting of multiple runs of NAOC. The "3x NAOC" corresponds to the treatment with the highest average lifetime and the lowest deviation of the measurements showing a stable and reproducible behaviour.

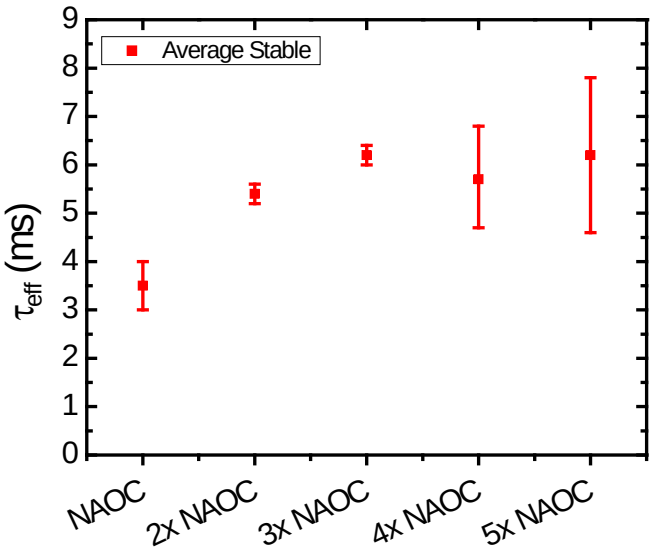


Figure 6.5: Average stable lifetime (red square) and the deviation from the average value (red bar) of the 2nd and 3rd series of textured samples showing the difference in stability and reproducibility among NAOC, "2x NAOC", "3x NAOC", "4x NAOC" and "5x NAOC" treatments.

A conclusion that can be derived from the reported results is that after a point, contamination removal has been fully accomplished and nano-roughness on the c-Si surface is the factor which affects the quality of a-Si:H/c-Si interface. For example, when the polished (111) wafer is treated with two runs of NAOC, a lifetime decay is observed. While the possibility for surface contamination due to further cleaning can be excluded, induced nano-roughness seems the only reason for the a-Si:H/c-Si interface quality deterioration. “3x NAOC” treatment presents the most stable and reproducible behaviour leading to a high interface lifetime. Thus far, a treatment consisting of three sequential runs of NAOC with a 3 min intermediate step of 0.5% HF dip can be considered the most appropriate for contamination removal and smoothening of the textured substrates.

Chapter 7

Silicon Heterojunction devices

7.1 Introduction

So far, the highest efficiency SHJ device fabricated in the PVMD group is a SHJ solar cell based on a textured substrate and consisting of a double-layer antireflective coating [6]. Due to the optical enhancement, a high J_{SC} was measured resulting in a solar cell efficiency of 19%. However, the V_{OC} was limited to a value of 638mV while at the same time values of 670 mV-680 mV are measured for the V_{OC} of a flat SHJ after its substrate is treated with NAOC.

Hence, the current research aims at the fabrication of a SHJ device with a textured absorber layer incorporated for the enhancement of the J_{SC} and at the same time high a-Si:H/c-Si interface quality resulting in a sufficiently high V_{OC}. The impact of the application of the already developed texturing recipe and pre-deposition treatment on the SHJ solar cells is described by the external parameters of the devices along with EQE and lifetime measurements.

7.2 Experimental Process

Double-side polished and textured substrates obtained from the already developed recipe of 5% TMAH/ 7.4% IPA are used for the fabrication of SHJ solar cells. The characteristics of these c-Si substrates are described in *Chapter 5*.

The SHJ devices are fabricated by PECVD targeting the following structure: *p* a-Si:H (5 nm)/ *i* a-Si:H (6 nm)/ *n* c-Si/ *i* a-Si:H (6 nm)/ *n* a-Si:H (9 nm). After the post-texturing treatment, less than 10 min are needed for the introduction of the c-Si substrates in the PECVD vacuum system. Separate chambers are used for the deposition of *i*, *n* and *p* a-Si:H layers. The deposition conditions, which are the same for both polished and textured surfaces, are reported in *Table 7.1*.

Layer	RF (MHz)	$T_{substrate}$ (°C)	$P_{deposition}$ (mbar)	SiH_4 (sccm)	B_2H_6 (sccm)	PH_3 (sccm)
i **a-Si:H**	13.56	180	0.7	40	-	-
p **a-Si:H**	13.56	180	0.7	20	1	-
n **a-Si:H**	13.56	180	0.6	40	-	11

Table 7.1: PECVD deposition conditions used in SHJ solar cells fabrication: plasma frequency, substrate temperature, gas pressure and gas flow rates.

Subsequently to PECVD, “as-deposited” lifetime measurements are conducted on the SHJ devices which present no degradation due to the field-effect passivation from the internal field created after the deposition of *p* and *n* a-Si:H layers. Afterwards, ITO antireflective coating is deposited by RF magnetron sputtering targeting a thickness of 80 nm for the polished and 75 nm for the textured solar cells and the front and rear metal contacts consisting of 100 nm Ag/30 nm Cr/1900 nm Al are deposited by using PVD. Finally the solar cells are annealed for 1 h at 170^{o}C in air.

J–V measurements are performed at room temperature using Wacom solar simulator for the determination of the V_{OC} and *FF*. The J_{SC} is confirmed through the EQE measurement and then the efficiency of the solar cells is calculated. On the same c-Si substrate eight 1x1 cm^2 and nine 0.4x0.4 cm^2 solar cells are fabricated at every run. However, the results reported here correspond only to the solar cell with the best performance among all the devices from the same run.

7.3 Results and Discussion

During the first stages of the research, the deposition time (DT) required to fabricate ITO and a-Si:H layers on the textured substrate with the desirable thickness in comparison with the deposition time for flat (DTF) substrates is the parameter under investigation. The first device fabricated is a SHJ solar cell based on a (111) double-side polished c-Si substrate and is used as a reference for the textured SHJ solar cells. Afterwards, three textured SHJ solar cells are

fabricated where the DT for the a-Si:H and ITO layers vary and correspond to “1x DTF”, “1.73x DTF” and “3x DTF” respectively. Although 75 nm is the optimized thickness of the ITO for textured substrates, 80 nm is the target for the ITO layer at this run in order to identify the match between the textured and polished substrate. An ITO thickness of 75 nm will be used for all the subsequent runs. Polished and textured substrates are treated with the reference NAOC. The J_{SC}, V_{OC}, FF and η of the SHJ textured solar cells are compared with the same parameters of the polished SHJ device in *Figure 7.1* .

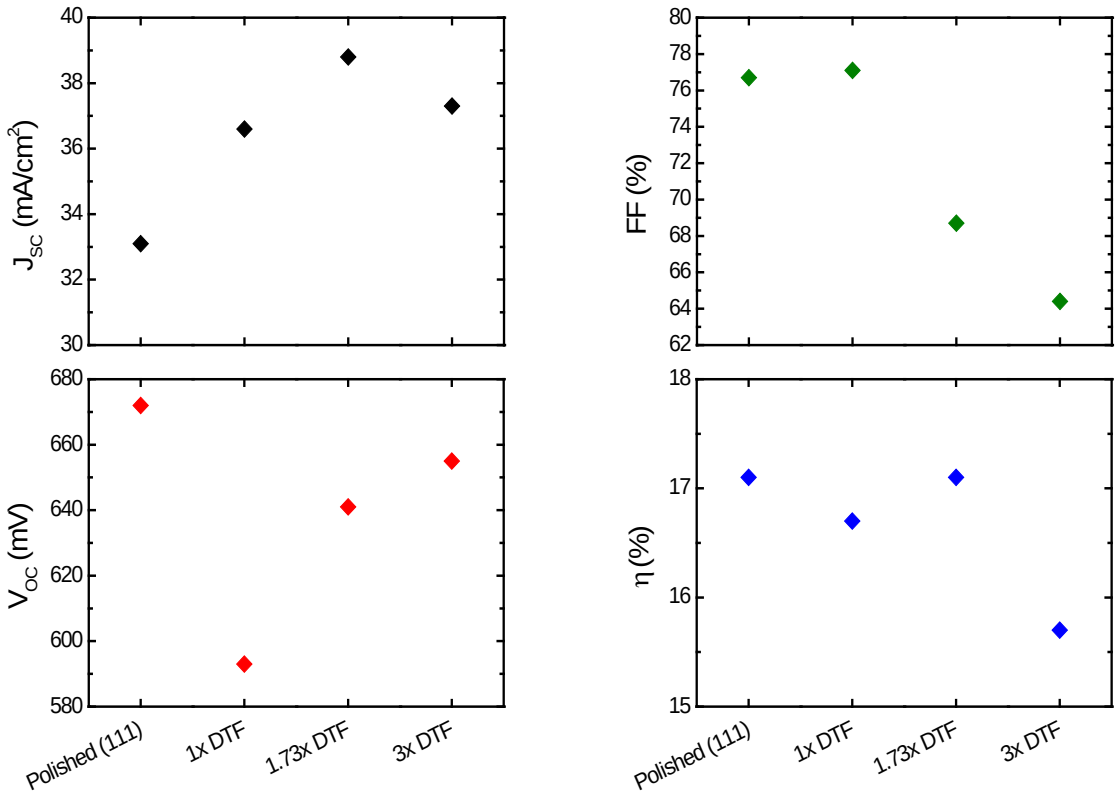


Figure 7.1: a-Si:H and ITO layers deposition time (DT) dependency of the short circuit current density (J_{SC}), open circuit voltage (V_{OC}), fill factor (FF) and efficiency (η) of textured SHJ devices in comparison with the deposition time for flat (DTF) substrates.

A very low V_{OC} is measured for the “1x DTF” solar cell reflecting the inefficient passivation of the c-Si surface from the *i* a-Si:H layers due to their low thickness. The J_{SC} graph reveals that the antireflective property of the ITO is optimal neither for the “1x DTF” nor for the “3x DTF” but only for the “1.73x DTF” device. As mentioned above, 75 nm is the optimal thickness of ITO on textured devices. However, at this run 80 nm of ITO is the target. Considering that during

research no remarkable differences have been observed between the J_{SC} values acquired when 75 nm or 80 nm ITO is used, “1.73x DTF” solar cell corresponds to the targeted 80 nm thickness of ITO. On the other hand, the “3x DTF” textured device appears to have a-Si:H layers with a higher thickness than that of the desirable structure while the *FF* is very low due to the high series resistance caused by the high layer thickness.

The best performance is observed when the DT used for the a-Si:H and ITO layers is 1.73 times the DTF. The highest J_{SC} is measured for the “1.73x DTF” solar cell reflecting the optimally enhanced antireflective properties of the device due to the combination of the pyramidal morphology of the substrate and the ITO layer with the targeted thickness. Furthermore, despite the low *FF*, the high J_{SC} along with a V_{OC} of 641 mV comparable with the V_{OC} reported for the record efficiency SHJ device of the previous research [6], results in an efficiency of 17.1%.

Considering that the surface area of a randomly textured wafer is 1.73 times larger than the equivalent planar surface of a flat wafer and assuming that the flux of growth particles is perpendicular to the wafer, it can be understood that in order to deposit on a textured substrate nano-layers with thickness approximately the same as on flat wafer the DTF should be multiplied with 1.73. Thus, by using the 1.73 factor for the DT under the same growth conditions as for the flat wafer the desirable structure can be fabricated in case of textured substrates. The rule of 1.73 has been incorporated for the fabrication of all the devices that follow, unless stated otherwise.

Depending on the ITO thickness, the EQE of a SHJ device presents a maximum at a specific wavelength where destructive interference occurs. By examining the EQE measurements of “polished (111)”, “1x DTF”, “1.73x DTF” and “3x DTF” devices in *Figure 7.2*, it seems that only the blue curve appears to have approximately the same maximum with the black curve at around 600 nm. On the contrary, there is a mismatch between the maximum of the black curve and the maximum of red and green curves. This enhances the concept that the ITO thickness of the “1.73x DTF” device approximates the thickness of the ITO layer grown on the “polished (111)” device.

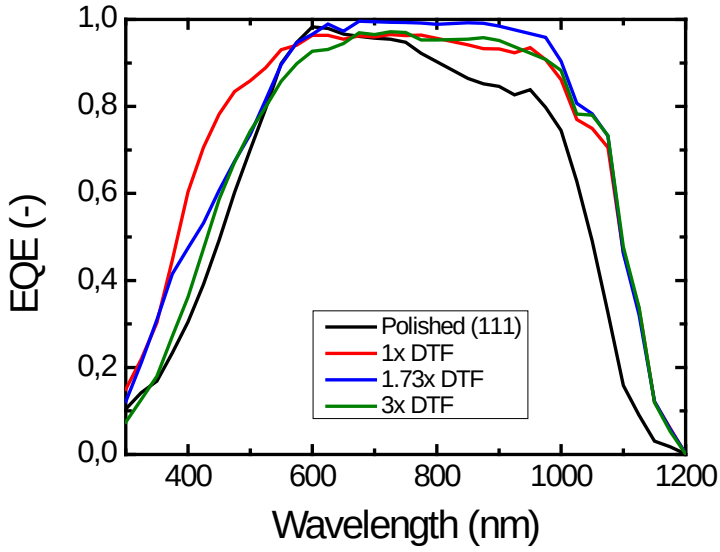


Figure 7.2: EQE measurements of the "polished (111)", "1x DTF", "1.73x DTF" and "3x DTF" devices showing that only the ITO layer of the textured "1.73x DTF" device has approximately the same thickness with the ITO layer of the "polished (111)" while their EQE graphs have their maximum approximately at the same wavelength,

Now, by measuring the as-deposited effective lifetime of these solar cells, *Figure 7.3* depicts that the lifetime increases as the DT increases for the textured devices.

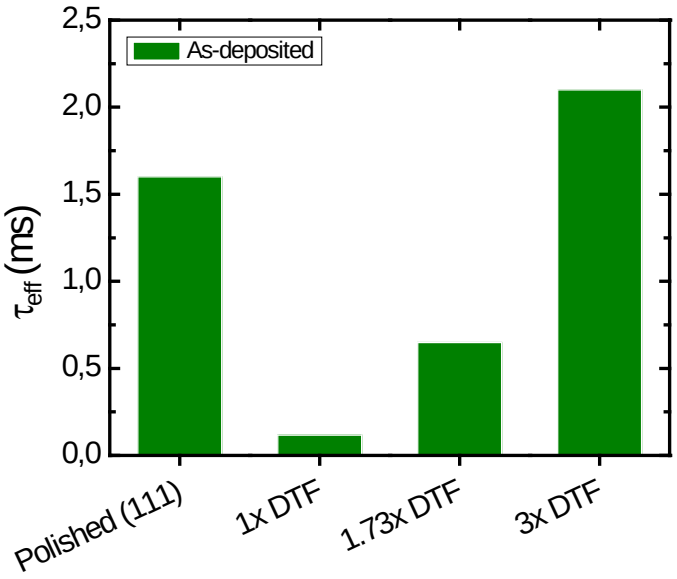


Figure 7.3: As-deposited lifetime measurements of the "polished (111)", "1x DTF", "1.73x DTF" and "3x DTF" devices.

However, this increase in lifetime and a-Si:H/c-Si interface quality is only attributed to the increased thickness of the *i* a-Si:H layers while the substrates of all the devices are treated with NAOC. As already discussed in *Chapter 6*, the highest lifetime of a-Si:H/c-Si interface formed by a polished wafer was reported after the substrate was treated with NAOC. Therefore, the lifetime of 1.6 ms of the polished device would be considered as the upper limit of the lifetime that could be measured on a textured SHJ device. It should be noted that the measured lifetime of the interface of the devices results from the combination of chemical and field-effect passivation. However, chemical passivation due to the ultrathin *i* a-Si:H layer of 6 nm is much lower than the passivation achieved by 50 nm *i* a-Si:H in *Chapter 6* and the field-effect passivation due the internal electric field created by the *n* and *p* a-Si:H layers dominates.

Meanwhile, two more "1.73x DTF" and "3x DTF" devices are fabricated, but this time their substrates are exposed to "2x NAOC" treatment. *Figure 7.4* illustrates the effect of "2x NAOC" treatment on devices with identical structures resulting in a higher lifetime and V_{OC} and verifies the results reported in *Chapter 6* about the improvement of the textured a-Si:H/c-Si interface by using two runs of NAOC instead of one.

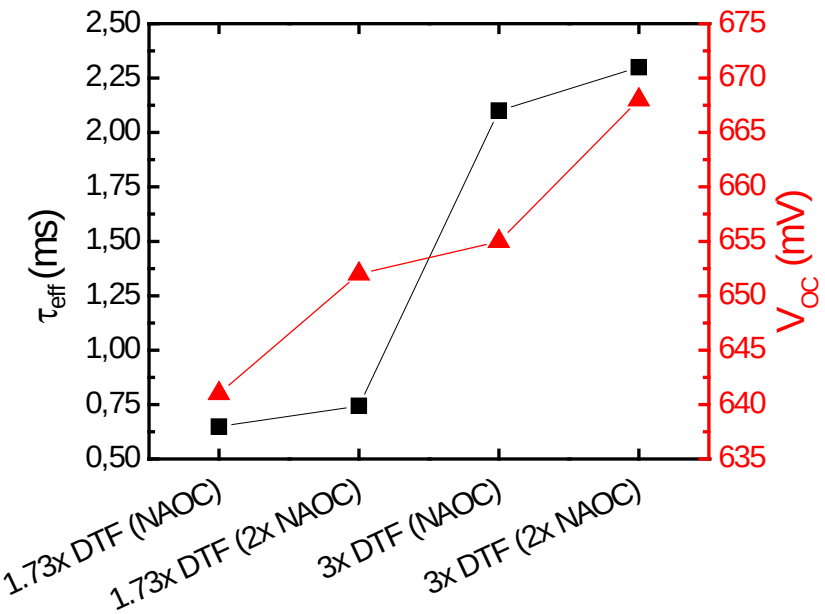


Figure 7.4: Lifetime and V_{OC} improvement of SHJ devices with identical structures due to the implementation of "2x NAOC" as a pre-deposition treatment.

The next step of the experimental process is the fabrication of SHJ solar cells after their textured substrates are treated with "2x NAOC", "3x NAOC", "4x NAOC" and "5x NAOC" in order

to investigate the impact of each treatment mainly on the V_{OC} and consequently the efficiency of the device.

Observing the results in *Figure 7.5*, all the treatments contribute to the improvement of the V_{OC}, but as expected the highest value of 680 mV is obtained from the device whose substrate is treated with the optimized "3x NAOC" treatment. In general, all the SHJ devices fabricated after implementing the multiple runs of NAOC appear to have a good performance with efficiencies above 18%. However, the efficiency of 19.5% of the "3x NAOC" SHJ device should be highlighted as it corresponds to the highest efficiency SHJ solar cell at the PVMD group. The measured J_{SC} are quite high and similar to each other while the different treatment on the substrates has no impact on the produced current. The J_{SC} is dependent on the structures of the SHJ devices which are almost identical.

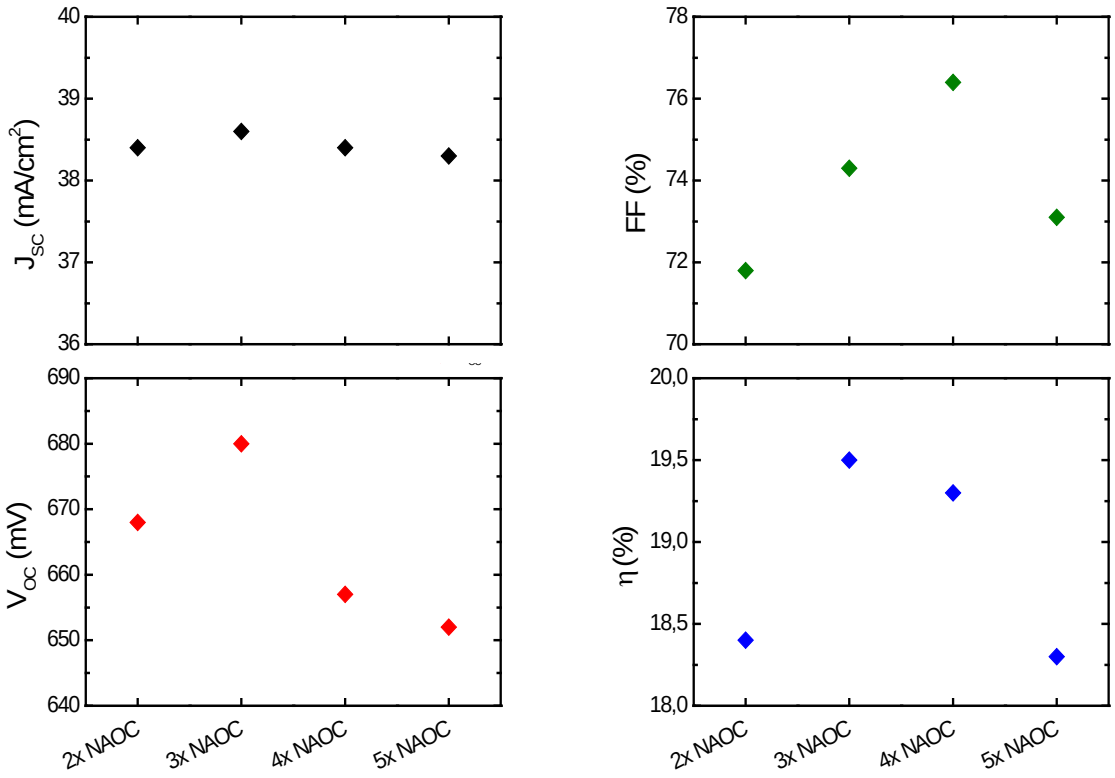


Figure 7.5: Multiple runs of NAOC treatment dependency of the short circuit current density (J_{SC}), open circuit voltage (V_{OC}), fill factor (FF) and efficiency (η) of textured SHJ devices with identical structures.

This is also shown in *Figure 7.6* where there is a strong matching among the EQE graphs of the devices.

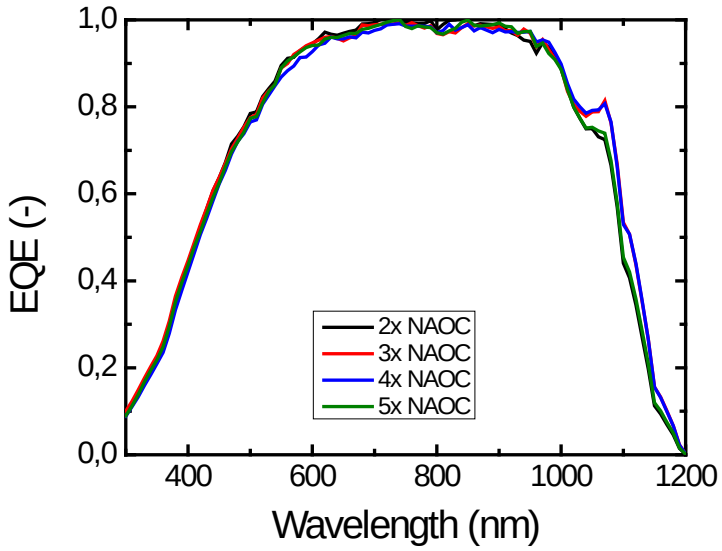


Figure 7.6: EQE measurements of the "2x NAOC", "3x NAOC", "4x NAOC" and "5x NAOC" SHJ solar cells.

Further verification of the highest a-Si:H/c-Si interface quality achieved after the "3x NAOC" treatment is provided by the as-deposited lifetime measurements of the devices (see *Figure 7.7*).

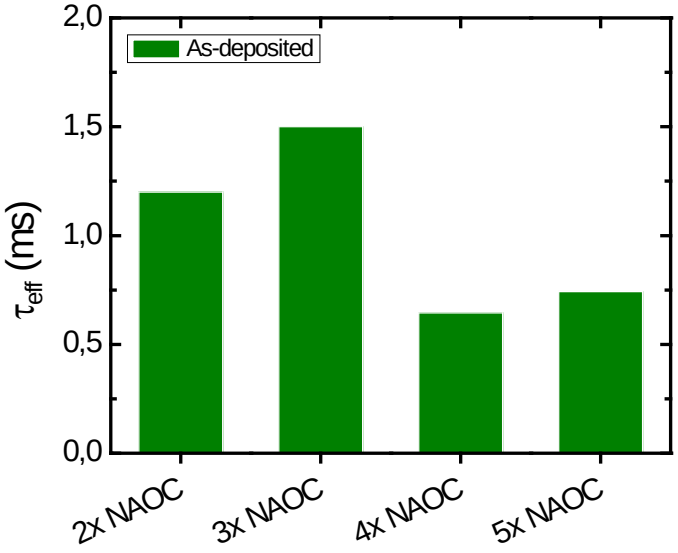


Figure 7.7: As-deposited lifetime measurements of the "2x NAOC", "3x NAOC", "4x NAOC" and "5x NAOC" SHJ devices.

Lifetime increases until three cycles of NAOC and decreases for the "4x NAOC" and "5x NAOC" treatments. The highest lifetime and V_{OC} achieved for the "3x NAOC" confirms its implementation as the most appropriate treatment for the textured substrates. In fact, the lifetime of 1.5 ms measured on the "3x NAOC" device is not only comparable but quite similar with the lifetime measured on the "polished (111)", reflecting that the treatment consisting of 3 cycles of NAOC can be considered optimal for textured substrates. Furthermore, the lifetime decrease after "4x NAOC" and "5x NAOC" treatments is in accordance with the lifetime results of the 2nd series of textured samples reported in *Chapter 6* so that further investigation is demanded for the reason of measuring higher lifetimes for the 3rd series of samples after "4x NAOC" and "5x NAOC" treatments.

Now, the lifetime results acquired from the 2nd and 3rd series of textured samples in *Chapter 6* and the SHJ devices in *Chapter 7* after being treated with the different number of NAOC treatment can be summarized in *Figure 7.8*. It can be clearly seen that the 2nd series of samples and the SHJ devices present a peak for the "3x NAOC" treatment. Furthermore, the a-Si:H/c-Si interface quality achieved on textured wafer after "3x NAOC" is similar to the a-Si:H/c-Si interface quality on flat substrate. Therefore, "3x NAOC" treatment can be considered optimal for the pyramidal c-Si surface and further investigation should be conducted for explaining the further lifetime increase observed for the 3rd series of samples after "4x NAOC" and "5x NAOC".

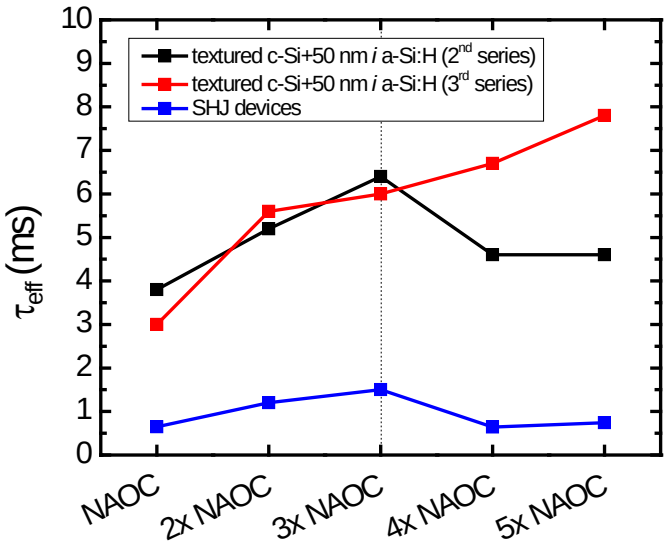


Figure 7.8: Summary of the lifetime measurements acquired from the 2nd and 3rd series of textured samples passivated with 50 nm i a-Si:H and the SHJ devices after being treated with NAOC, "2x NAOC", "3x NAOC", "4x NAOC" and "5x NAOC".

Although the last series of SHJ devices have the same structure, there is a wide distribution of the *FF.* Low *FF* are measured due to higher R_S and/or lower R_P of the solar cells than expected. In order to investigate the impact of the *i* a-Si:H layer thickness on the R_S and consequently on the *FF*, SHJ devices with "3x NAOC" treatment are fabricated by varying only the thickness of the *i* layer. Instead of the 1.73 factor, the "1.6x DTF", "1.4x DTF", "1.2x DTF" and "1x DTF" factors are used only for the *i* layer. Under the assumption that the incorporation of the 1.73 factor leads to the fabrication of 6 nm thick *i* a-Si:H layer on the textured wafer, the 1.6, 1.4, 1.2 and 1 factors would correspond to *i* a-Si:H thicknesses ($d_{i\text{-}layer}$) of 5,5 nm, 4,8 nm, 4 nm and 3,5 nm, respectively. The results after the characterization of the devices are illustrated in *Figure 7.9*.

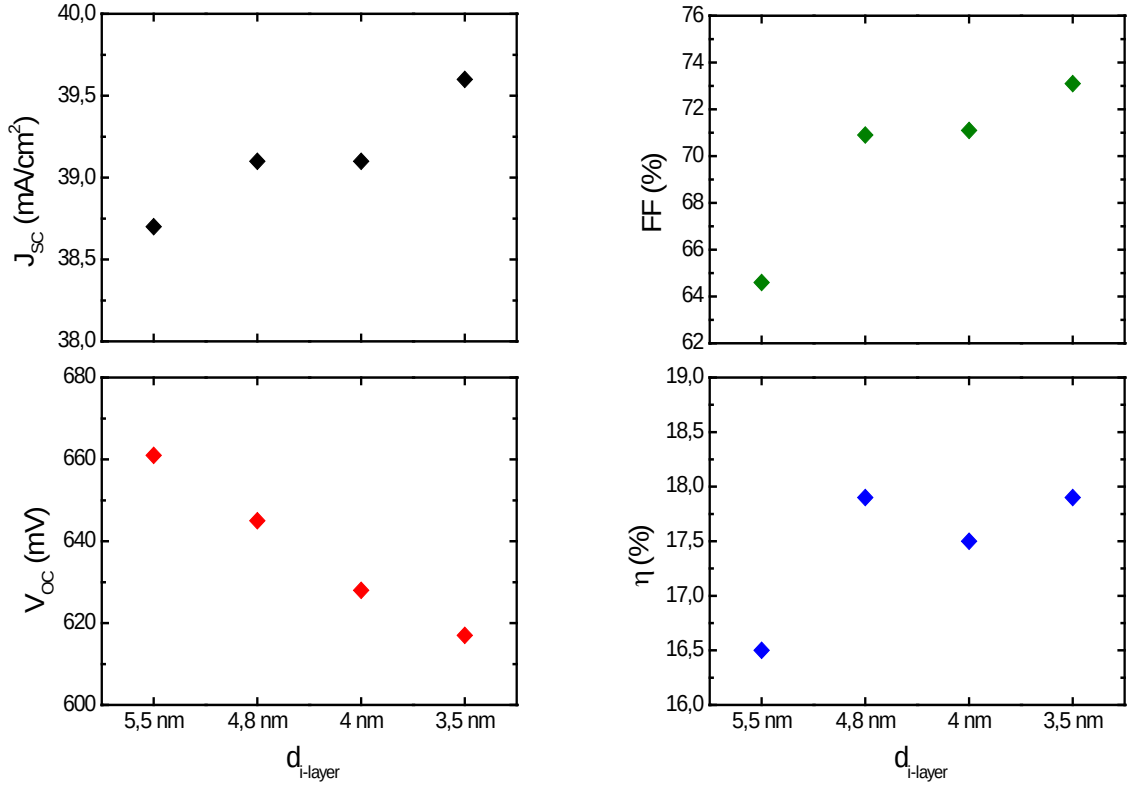


Figure 7.9: i a-Si:H layer thickness dependency of the short circuit current density (J_{SC}), open circuit voltage (V_{OC}), fill factor (FF) and efficiency (η) of the textured "3x NAOC" SHJ devices.

As the *i* layer thickness decreases, the light absorption in the *i* a-Si:H decreases. As a result an increase is observed in the light absorption in the c-Si absorber layer and the J_{SC} of the device increases. Regarding the V_{OC} graph, lower *i* layer thickness implies lower passivation of

the textured c-Si surface and worse quality of the a-Si:H/c-Si interface resulting in a decrease in the V_{OC} of the device. Last but most important, the *FF* appears to increase as the *i* layer thickness becomes lower. Even though, the reported results correspond to the device of the same run with the higher *FF*, a wide distribution of the *FF* is observed and the majority of the devices appear to have a low *FF*.

Additionally, the decrease in the parasitic absorption in the *i* a-Si:H layer leading to higher absorption in the absorber layer of the SHJ device is depicted in the EQE graph in *Figure 7.10.*

Looking carefully at short wavelengths a wider EQE can be observed as the *i* a-Si:H layer thickness decreases. The increase in EQE implies an increase in the spectral response of the device resulting in higher J_{SC}.

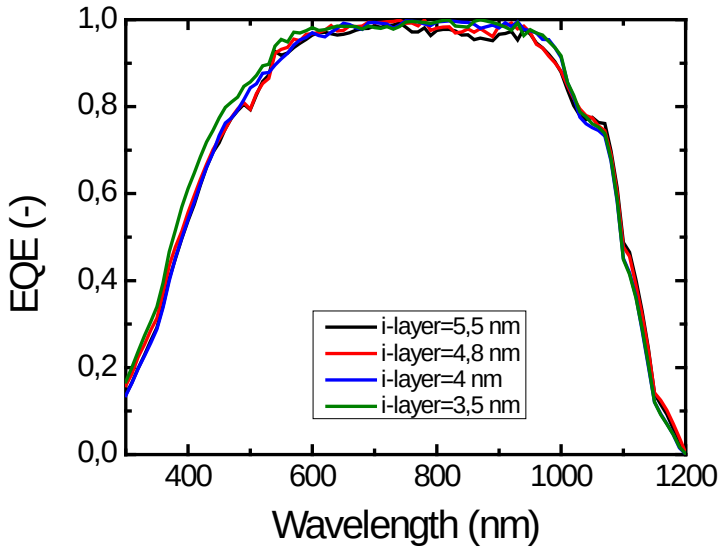


Figure 7.10: i a-Si:H layer thickness dependency of the EQE of the textured "3x NAOC" SHJ devices.

The passivation quality of the textured c-Si surface with the *i* layer of different thickness and the deterioration of a-Si:H/c-Si interface quality as the *i* a-Si:H layer becomes thinner are clearly depicted in *Figure 7.11* where the lifetime of the devices is experienced an exponential-like decrease as *i* layer thickness decreases.

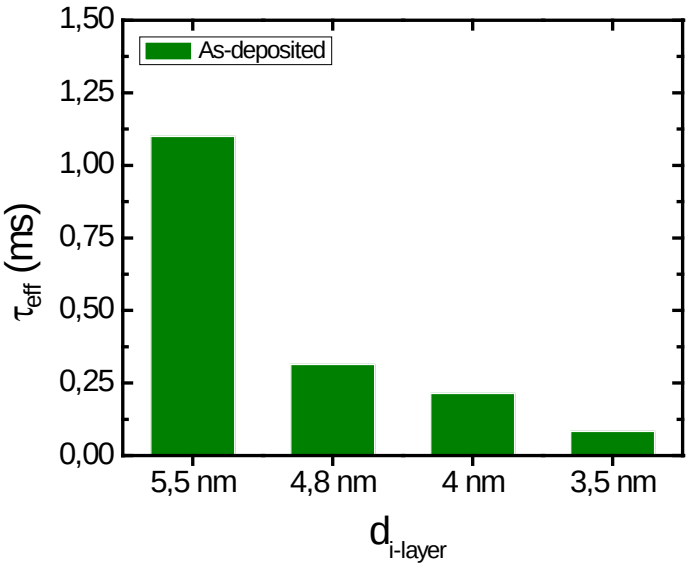


Figure 7.11: i a-Si:H layer thickness dependency of the as-deposited lifetime measurements on the textured "3x NAOC" SHJ devices.

Reaching the end of the investigation and summarizing the results, high efficiency SHJ solar cells with the *p* a-Si:H (5 nm)/ *i* a-Si:H (6 nm)/ *n* c-Si (270 nm)/ *i* a-Si:H (6 nm)/ *n* a-Si:H (9 nm)/ ITO (75nm) structure can be fabricated when a textured c-Si substrate is applied and "3x NAOC" is implemented as a pre-deposition treatment.

Apart from the SHJ efficiency of 19.5%, the main achievement of this work is the improvement of the a-Si:H/c-Si interface quality of the textured SHJ device reaching V_{OC} values similar to the V_{OC} measured on flat SHJ solar cells.

Finally, characterization measurements witness a high standard deviation of the *FF* values. The large distribution of *FF* implies an inhomogeneity issue. Although it has been shown already that a quite homogeneous pyramidal morphology without untextured areas can be achieved for the c-Si substrate, the very sharp features of the pyramids in combination with the currently used deposition rate in PECVD may lead to the formation of non-homogeneous layers.

Chapter 8

Conclusions and Recommendations

8.1 Conclusions

The research reported in this thesis has investigated the application of textured wafers in SHJ solar cells for its optical enhancement and the development of an appropriate treatment of the textured substrate prior to *i* a-Si:H deposition targeting high a-Si:H/c-Si interface quality.

Avoiding KOH and NaOH alkaline solutions due to their metallic contaminants, a texturing recipe consisting of 5% TMAH and 7.4% IPA has been developed. A certain amount of dissolved Si is a prerequisite for every newly prepared solution. Etching c-Si wafers with this recipe results in a reproducible and homogeneous pyramidal surface morphology with an average reflectance of approximately 12% in the wavelength region between 350 nm and 1100 nm. The efficient light trapping mechanism of the textured substrates has been confirmed by measuring high J_{SC} of around 38,5 mA/cm^2 after their implementation in the SHJ devices.

However, it has been shown that texturing leads to an a-Si:H/c-Si interface with higher recombination, which limits the V_{OC} of the SHJ solar cell after using for the textured wafer a cleaning treatment same as for the flat wafer. This has been attributed to the 1.73 times larger area of the textured surface in comparison with the equivalent planar area of a flat wafer and the texturing-induced nano-roughness resulting in a more defective a-Si:H/c-Si interface. Thus, a one-to-one transfer of process parameters from flat to textured c-Si substrate is not necessarily appropriate. A treatment of three sequential NAOC instead of one as in the case of the flat wafer has been proved to be optimal for the textured absorber layer leading to the fabrication of SHJ devices with lifetime and V_{OC} similar to those measured on flat SHJ devices.

NAOC consists of c-Si oxidation in HNO_3 solutions followed by removal of the previously grown SiO_2 layer in 0.5% HF. By removing the oxide layer, the surface defects are also removed. Considering that the surface defects have a certain depth, three cycles of NAOC are optimal for the complete removal of these defects leaving behind a smooth (111) surface. Comparing the thickness of the oxide layer [70][71] growing at every cycle and the etching rate

of this oxide in 0.5% HF [72], it can be understood that in a 3 min intermediate HF dip after every NAOC the oxide layer is completely etched and HF interacts further with c-Si surface inducing roughness on it [46]. Therefore, additional cycles of NAOC on an already smooth surface will deteriorate the surface quality as in the case of “4x NAOC” and “5x NAOC”.

Applying the “3x NAOC” treatment for the fabrication of the textured SHJ solar cell, V_{OC} increases from 641 mV to 680 mV reaching the same range of V_{OC} values measured for the flat SHJ device. This increase in V_{OC} also confirms the compatibility of the texturing provided by the recipe developed in this work with the fabrication of the investigated SHJ devices. Together with a measured J_{SC} of 38.6 mA/cm^2 an efficiency of 19.5% is achieved implying a gain of 14% in efficiency due to the improvement of V_{OC}.

8.2 Recommendations

NAOC consists of a 10 min step in 99% HNO_3 and a 10 min step in 69% HNO_3 at 110ºC. Between these steps, only the latter contributes to the formation of a very high quality and density oxide layer so that after its removal, an atomically smooth surface is left behind. However, the thickness of this oxide layer is approximately 1.4 nm [71]. Further investigation of the parameters for an oxide layer growth with higher thickness in a HNO_3 solution and the optimal time for its removal in diluted HF may lead to the replacement of the additional cycles of NAOC with only one treatment step resulting in a shorter process time.

The optimal behaviour of the “3x NAOC” treatment is the outcome acquired from the fabrication of two series of textured substrates passivated with thick *i* a-Si:H layer and the fabrication of one series of SHJ devices. In the future, it is worth to fabricate more series of *i* a-Si:H/c-Si samples and SHJ devices for the comparison of the impact of the different number of cycles of NAOC.

The *FF* of the fabricated SHJ devices appear to have a high standard deviation resulting from the several ups and downs of the series and shunt resistance of the solar cells which reflects a non-uniformity issue of the a-Si:H layers. The sharp features of the pyramidal surface along with the currently used deposition rate may lead to the growth of a non-uniform layer. In this research, an attempt for inspecting the cross section of the samples has been realized with SEM but no information could be extracted for the a-Si:H layer due to the low resolution. In the future, the use of transmission electron microscopy (TEM) with resolutions even in sub-nanometrical

scale will enlighten the way a-Si:H layers are grown on the substrate. A suggestion is to use wet chemical treatments such as HF:HNO_3:CH_3COOH solution for the polishing of the pyramids. This will lead to the curving of the peaks and valleys of the pyramids which may result in a more uniform a-Si:H layer growth at the cost of a small increase of the reflectance.

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