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Characterization, Modeling, and Test of Intermediate State Defects in STT-MRAMs

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Abstract—The manufacturing process of STT-MRAM requires unique steps to fabricate and integrate magnetic tunnel junction (MTJ) devices which are data-storing elements. Thus, understanding the defects in MTJs and their faulty behaviors are paramount for developing high-quality test solutions. This article applies the advanced device-aware test to intermediate (IM) state defects in MTJ devices based on silicon measurements and circuit simulations. An IM state manifests itself as an abnormal third resistive state, which differs from the two bi-stable states of MTJ. We performed silicon measurements on MTJ devices with diameter ranging from 60nm to 120nm; the results show that the occurrence probability of IM state strongly depends on the switching direction, device size, and bias voltage. We demonstrate that the conventional resistor-based fault modeling and test approach fails to appropriately model and test such a defect. Therefore, device-aware test is applied. We first physically model the defect and incorporate it into a Verilog-A MTJ compact model and calibrate it with silicon data. Thereafter, this model is used for a systematic fault analysis based on circuit simulations to obtain accurate and realistic faults in a pre-defined fault space. Our simulation results show that an IM state defect leads to intermittent write transition faults. Finally, we propose and implement a device-aware test solution to detect the IM state defect.

Index Terms—Memory test, device-aware test, STT-MRAM, MTJ-internal defect, defect characterization, intermediate state, fault model

1 Introduction

Spin-transfer torque magnetic random access memory (STT-MRAM) is one of the most promising emerging memory technologies, thanks to its advantageous features: non-volatility, fast access speed, high endurance, nearly zero leakage power, and CMOS-compatibility [1]. The flexible trade-off between write speed, endurance, and retention also empowers it to be tailored and fitted into different layers ranging from high-retention storage to high-performance caches in the present memory hierarchy [2]. Therefore, STT-MRAM has stimulated several start-ups (e.g., Everspin [3], Avalanche [4]) and major global semiconductor companies (e.g., Intel [5], TSMC [2]) to commercialize this technology. Nevertheless, to enable high-volume production of STT-MRAM, high-quality test solutions are paramount to meet the increasingly stringent quality requirements of IC chips being shipped to end-customers. The STT-MRAM manufacturing process involves not only conventional CMOS process but also magnetic tunnel junction (MTJ) fabrication and integration [6]. The latter is more vulnerable to defects as it requires deposition, etch, and integration of magnetic materials with new tools [7]. A blind application of conventional tests for existing memories such as SRAM and DRAM to STT-MRAM may lead to test escapes and yield loss. Hence, understanding MTJ-internal defects and their resultant faulty behaviors are crucial for developing high-quality STT-MRAM test solutions.

STT-MRAM testing is still an on-going research topic [8], [9]. Several fault models such as multi-victim, kink, and write destructive faults [10] were proposed for field-driven MRAMs. However, these fault models are not applicable to current-driven STT-MRAMs. Chintaluri *et al.* [11] derived fault models such as transition faults and read disturb faults in STT-MRAM arrays by simulating the impact of resistive defects in the presence of process variations; a March algorithm and its built-in-self-test implementation were also introduced. Nair *et al.* [12] performed layout-aware defect injection and fault analysis, whereby they observed dynamic incorrect read fault. Nevertheless, all these papers assume that STT-MRAM defects including those in MTJ devices are equivalent to linear resistors without any justification. Recently, Wu *et al.* [13] presented both experimental data and simulation results of pinhole defects in MTJ devices, and demonstrated that modeling pinhole defects as linear resistors is inaccurate and results in wrong fault models. To address the limitations of the traditional fault modeling and test approach, Fieback *et al.* [14], [15] proposed the concept of *Device-Aware Test* (DAT), a step beyond cell-aware test. The DAT approach models physical defects accurately by incorporating the impact of such defects into the technology parameters and subsequently into the electrical parameters of the device. With the obtained defective device model, a systematic fault analysis can be conducted to develop realistic fault models; these fault models are then used to develop high-quality test solutions.

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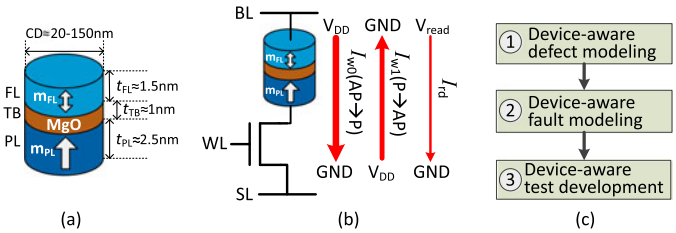

Fig. 1. (a) MTJ stack, (b) 1T-1MTJ cell, and (c) three-step DAT approach.

In this paper, we characterize *intermediate* (IM) state defects in STT-MRAMs and apply the DAT approach to model this defect, obtain accurate and realistic fault models, and develop an appropriate test. Normally, an MTJ device only has two bi-stable resistive states representing logic '0' and '1'. However, due to some physical imperfections such as unreversed magnetic bubbles [16], inhomogeneous distribution of stray field [17] or even skyrmion generation [18], a third resistive state may arise, leading to unintended memory faulty behaviors. This article is an extension of our prior work [19] and the contents differ from our prior studies on defect and fault modeling methodology [7], interconnect [20], pinhole [13], and SAFF defects [21]. The main contributions of this paper are as follows.

- Characterize IM state defects in MTJs with diameter 60-120nm based on *silicon measurements*.
- Demonstate the conventional resistor-based fault modeling and test approach fails to derive effective fault models and tests to detect IM state defects.
- Develop a Verilog-A compact model for a defective MTJ device suffering from an IM state defect, and calibrate the model with silicon data.
- Perform device-aware fault modeling to develop accurate and realistic fault models induced by IM state defects.
- Propose and implement an effective test solution with weak write operations.

The remainder of this paper is organized as follows. Section 2 introduces the fundamentals of STT-MRAM and device-aware test. Section 3 presents characterization results of IM state defects. Section 4 discuses limitations of testing the SAFF defect using conventional resistive defect models. Sections 5, 6, and 7 apply the DAT approach to physically model the IM state defect, derive accurate fault models, and develop a test solution, respectively. Section 8 concludes this paper.

2 Background

2.1 MTJ Device Technology

Magnetic tunnel junction (MTJ) is the most important component in STT-MRAMs, as it is the data-recording element which encodes two bi-stable magnetic states into one-bit data. Fig. 1a shows the schematic of a simplified MTJ device; its *Critical Diameter* (CD) is typically 20-150nm. The *cross-sectional area* $A_0 = \frac{1}{4}\pi \mathrm{CD}^2$ is a key technology parameter of the device. Fundamentally, the MTJ consists of three layers.

1) Free Layer (FL): This is the top layer typically made of CoFeB-based materials (t_{FL}≈1.5nm [20]). The magnetization of the FL can be switched by a spin-polarized current going through it or an external perpendicular magnetic field. The *saturation magnetization* M_{s} and *magnetic anisotropy field* H_{k} are two key technology parameters determining the *thermal stability factor* Δ as well as the switching characteristics of the FL [22], as listed in Table 1.

TABLE 1
STT-MRAM Key Parameters

Technology Parameters		Electrical Parameters	
A_0	Cross-sectional area of MTJ	R	Device resistance
M_{s}	Saturation magnetization of FL	I_{c}	Critical switching current
H_{k}	Magnetic anisotropy field of FL	t_{w}	Switching time
TMR	Tunneling magnetoresistance ratio		

2) Tunnel Barrier (TB): This is the MgO dielectric layer below the FL. As the TB layer is ultra-thin, typically t_{TB}≈1nm [23], electrons have a chance to tunnel through it, making the device behave as a tunneling-like resistor. To compare the sheet resistivity of different MTJ designs, the *Resistance-Area* (RA) product [22] is used. This is a figure of merit which is commonly used in MRAM community, and it is independent on device size.

3) Pinned Layer (PL): This is the bottom CoFeB-based layer (t_{PL}≈2.5nm) with its magnetization strongly pinned to a certain direction by a synthetic anti-ferromagnetic structure [23]. As a result, the FL's magnetization can be either parallel (P state) or anti-parallel (AP state) to the PL's.

The MTJ's resistance depends on both t_{TB} and the magnetic state (i.e., P or AP). This is well known as the *tunneling magneto-resistance* (TMR) effect [22], which is characterized by the TMR ratio, defined as: $(R_{\mathrm{AP}} - R_{\mathrm{P}})/R_{\mathrm{P}}$ where R_{AP} and R_{P} are the resistances in AP and P states, respectively.

Similar to other NVMs, enough retention time is required to retain the data in STT-MRAMs for an expected period of time depending on the target application. An STT-MRAM retention fault occurs when the magnetization of the MTJ's FL flips spontaneously to the opposite direction due to thermal fluctuation. Thus, the STT-MRAM retention time is generally characterized by the *thermal stability factor* (Δ) [22]. The higher the Δ, the longer the retention time.

2.2 1T-1MTJ Cell Design

Fig. 1b shows a bottom-pinned 1T-1MTJ memory cell and its corresponding read/write (R/W) operations. The three-terminal cell includes an MTJ device (storage element) and an NMOS transistor (access selector). The three terminals are connected to a bit line (BL), a source line (SL), and a word line (WL), as shown in the figure.

The voltages on the BL and SL control R/W operations on the cell when the WL is asserted. For instance, a write '0' operation requires the BL at V_{DD} and the SL grounded, which leads to a current I_{w0} flowing from BL to SL. In contrast, a current I_{w1} with the opposite direction goes through the cell during a write '1' operation. To guarantee a successful transition of the MTJ state, the magnitude of write current (both I_{w0} and I_{w1}) has to be larger than the *critical switching current* I_{c}. The larger the current above I_{c}, the faster the switching can be. It is worth noting that the *actual switching time* t_{w} under a fixed pulse varies from one cycle to another since the STT-induced magnetization switching is intrinsically stochastic. During a read operation, a significantly smaller voltage V_{read} than V_{DD} is applied on the BL to draw a read current I_{rd}, which can be as small as $\sim 10\mu$A or $0.06I_{\mathrm{c}}$ [24], to read the resistive state (R_{P} or R_{AP}) of the MTJ device by a sense amplifier.

Table 1 lists the key technology parameters of MTJ device to be used for defect modeling.

2.3 Device-Aware Test

In conventional tests or cell-aware tests, fault models are derived based on defect injection and circuit simulations at netlist or layout level. All defects irrespective of their physical natures in both interconnects and devices are modeled as *linear resistors*; e.g., a device-internal defect is typically modeled as a resistor either in parallel to or in series with a defect-free device model, as can be found in the prior work [11], [12]. However, it has been demonstrated in recent years that this defect modeling approach is inaccurate to tackle pinhole defects in MTJs [13], forming defects in RRAM devices [14], and gate oxide pinhole defects in transistors [25]. Moreover, conventional memory faults are typically described by the fault primitive notation [26], where only '0' and '1' states exist. However, in emerging non-volatile memories such as STT-MRAM and RRAM, undefined and extremely low/high resistive states may occur due to defects [20]. This calls for an expansion of memory fault space.

To address the above limitations, *Device-Aware Test* (DAT) [14] was proposed to provide a systematic framework for appropriate fault modeling and test of device-internal defects. DAT consists of three steps, as illustrated in Fig. 1c. First, manufacturing defects in devices are characterized and modeled physically; the impact of the defect on the technology parameters of the defective device is determined. Subsequently, such impact is incorporated into the device's electrical parameters to obtain a parameterized defective device compact model which can be calibrated by silicon data if available. Second, the defect-free model of the device used in the netlist (simulation model) is replaced with the defective device model obtained in step 1; a systematic fault analysis is then performed to validate realistic faults within a predefined complete fault space. Third, based on the fault modeling results in step 2, appropriate test solutions are developed; e.g., March tests, Design-for-Testability (DfT), stress tests, etc.

3 Defect Characterization

Electrical characterization with pulses is a common practice to evaluate the write performance of STT-MRAM devices. When we performed comprehensive characterization on devices with CD ranging from 60nm to 120nm, some devices showed an abnormal third resistive state in addition to the two bi-stable P and AP states. As the resistance of this unexpected state is always between R_{P} and R_{AP}, we refer to it as *intermediate* (IM) state in this article. In this section, we first introduce the experimental set-up for measuring IM state defects. Thereafter, the measured results of MTJ devices with and without IM state are presented and compared. Then, we elaborate the dependence of IM state occurrence probability on bias voltage, device size, and switching direction. Finally, we briefly review the related work in literature and discuss root causes of IM state defects.

3.1 Measurement Set-up

Figs. 2a and 2b show the pulse configurations in each cycle for AP→P and P→AP switching characterization, respectively. For AP→P switching characterization, a positive voltage pulse ($V_{\mathrm{p}} = 0.6\mathrm{V}$, $t_{\mathrm{p}} = 50\mathrm{ns}$) was applied to the MTJ device under test to initialize it to AP state. The pulse was followed by a read operation using a relatively long but small voltage pulse ($V_{\mathrm{p}} = 10\mathrm{mV}$, $t_{\mathrm{p}} = 0.7\mathrm{ms}$) to check whether the device has been initialized to AP state successfully. After the read, a negative pulse with $t_{\mathrm{p}} = 15\mathrm{ns}$ was applied to the device to study AP→P switching. Similarly, a second read was applied to read out the resistive state of the device. As the switching behavior is intrinsically stochastic, we repeated these four operations for 10k cycles to obtain a statistical result. To cover the switching probability P_{sw} from 0% to 100%, we swept the pulse amplitude V_{p} of the second pulse in a carefully-tuned range. For P→AP switching characterization, a similar measurement was conducted with the polarity of both write pulses reversed, as shown in Fig. 2b.

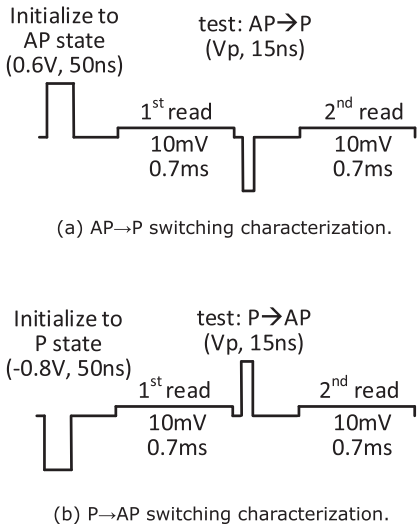

Fig. 2. Pulse configuration in each cycle.

3.2 Identification of IM State Defects

Figs. 3a and 3b show the measured results of a representative normal MTJ A (nominal CD=100nm) for AP→P switching and P→AP switching, respectively; each point represents a readout resistance of the second read pulse in Fig. 2. It can be seen that when $V_{\mathrm{p}} = -0.74\mathrm{V}$, AP→P switching probability is 100% in the measured 10k cycles. When $V_{\mathrm{p}} = 0.45\mathrm{V}$, P→AP switching probability is 99.2%, meaning that 0.8% of the 10k cycles experience failed transitions (marked with red triangles), due to the STT-switching stochasticity. Note that these two V_{p} values are just two examples showing the measurement results; in our measurements, we swept V_{p} values, as can be seen in Fig. 4. In both cases, there is no third resistive state observed. In contrast, Figs. 3c and 3d show the measurement data of a typical device with IM state (MTJ B) with the same size and experimental conditions. It is clear that a line of unexpected orange points (i.e., IM state) show up between the two lines representing AP and P states. The occurrence probability of IM state in AP→P switching direction is 1.6% when $V_{\mathrm{p}} = -0.74\mathrm{V}$ while it is 0.6% in the opposite switching direction when $V_{\mathrm{p}} = 0.45\mathrm{V}$. It is also worth noting that the probability of failed transition of MTJ B is much higher than that of MTJ A under the same applied pulses. The disparity of R_{P} (red lines) and R_{AP} (green lines) between these two devices is

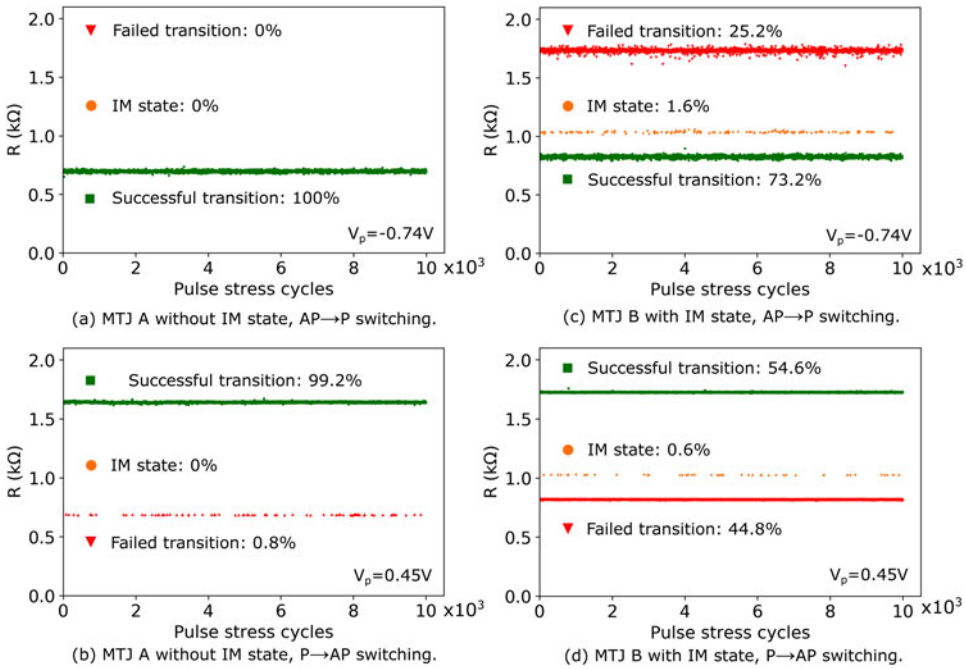

Fig. 3. Measurement results: MTJ A without IM state (left) versus MTJ B with IM state (right).

attributed to process variations; the slight TMR drop in this defective MTJ was not a common rule in all observed defective MTJs with IM states, compared to good MTJs.

3.3 Dependence of IM State Defects

We observed that the occurrence of IM state significantly depends on the applied bias voltage, switching direction (i.e., AP→P or P→AP), and device size in our experiments.

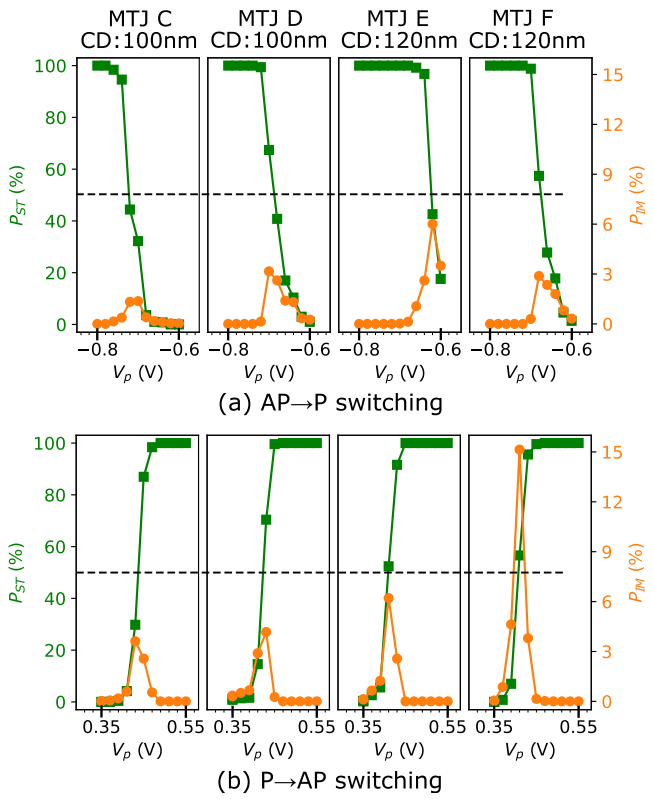

Fig. 4. Bias voltage dependence of IM state.

Figs. 4a and 4b show the bias voltage dependence of IM state of four different MTJ devices in AP→P and P→AP switching directions, respectively; the nominal CD of MTJ C and D is 100nm while it is 120nm for MTJ E and F. It can be seen that the *successful transition probability* (P_{ST}) between P and AP states (marked with green square points corresponding to the left y-axis) increases from 0% to 100%, as the amplitude of V_{p} increases in both switching directions. The orange circle points represent the *occurrence probability of IM state* (P_{IM}) corresponding to the right y-axis at various V_{p} points. One can observe that P_{IM} increases with the amplitude of V_{p} until reaching a peak at $P_{\mathrm{ST}}{\approx}50\%$ (marked with the horizontal dash line), then it decreases as V_{p} further increases; this rule applies for all four devices in both switching directions despite the peak height of P_{IM} varies from one device to another. Furthermore, even for the same device, there is a large difference in the peak height of P_{IM} for the AP→P and P→AP switching directions. This indicates that P_{IM} also depends on the switching direction.

To investigate whether the MTJ size plays a role in determining the occurrence probability of IM state, we repeated the same measurements on MTJ devices with four different sizes, 100nm, and 120nm. For each size, we measured 60 devices; the number of devices with IM state is shown with the blue histogram (left y-axis) in Fig. 5. It is clear that the smaller the MTJ device (i.e., smaller CD), the less likely to see IM states in our devices. More specifically, 57 devices out of the measured 60 devices with CD=120nm exhibit IM states in the measurement, whereas the number is 5 and 0 for MTJs with CD=75nm and 60nm respectively. Among those devices with observed IM states, the median of the maximum occurrence probability of IM state (i.e., the peak height of P_{IM} in Fig. 4) becomes smaller when CD decreases, as shown with the two orange curves corresponding the right y-axis in Fig. 5. It is also worth noting that the median of the maximum P_{IM} in AP→P switching direction is slightly smaller than that in P→AP switching direction for a given MTJ size.

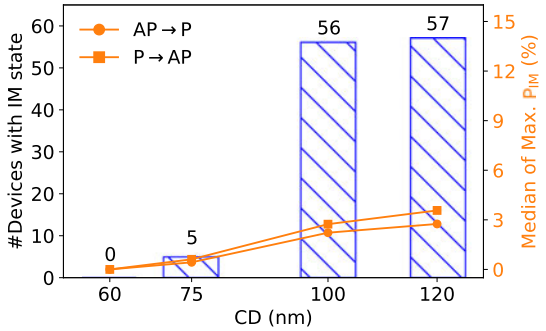

Fig. 5. Device size dependence of IM state.

This is probably because AP→P switching generates more Joule heating than the opposite switching direction, which reduces the retention time of IM state; thus, the captured number of IM states on average is smaller in AP→P switching direction under the same measurement set-up. Interestingly, Intel also presented similar measurement results in [17]. Based on the above observations, it can be inferred that STT-MRAM technology down-scaling is helpful in reducing IM state defects in MTJs, thus leading to a more deterministic and uniform transition between the bi-stable AP and P states.

3.4 Related Work and Potential Causes

There are several prior works on studying IM states in MTJ devices based on experiments and/or simulations, as listed in Table 2. Yao *et al.* [27] observed stable IM states in both P→AP and AP→P switching directions after the removal of write pulses with a similar measurement set-up to ours; the read pulse width is 200ms, indicating that the retention time of IM state (RT_{IM}) is at least 200ms. They attributed the physical causes of IM state to the multi-structure of the FL induced by the dipole field and large device size. Aoki *et al.* [28] also observed IM states during STT-switching with sub-10ns pulses and claimed that those IM states are metastable meaning that they disappear after the removal of write pulses; the claimed physical cause is similar to the above one. Subsequently, more research works [16], [17], [29] were conducted and reported that the observed IM states are metastable due to the inhomogeneous distribution of stray field at the FL and unreversed magnetic bubbles, as elaborated in the table. In recent two years, studies in [18], [30] on IM states reveal that IM states in MTJ devices take place due to Skymion formation and their retention time can be as long as the bi-stable P and AP states.

In this work, our measurement data also clearly demonstrates the existence of IM states in MTJ devices especially for large sizes (CD > 75nm). It manifests as a third resistive state between P and AP states. The occurrence of IM state is probabilistic depending on the switching direction, applied bias voltage, and device size. In addition, we swept the read pulse width from $50\mu s$ to 10ms in our measurements; the results show that the IM states occur in all these configurations indicating that RT_{IM} is larger than 10ms after the removal of write pulses. The root causes can be attributed to some physical imperfections such as unreversed magnetic bubbles, inhomogeneous distribution of stray field or even skyrmion generation. To accurately describe the faulty behavior of STT-MRAM cell in the presence of an IM state defect, we need to have an accurate defect model.

4 Limitations of Conv. Test Approach

In conventional memory testing, manufacturing defects are typically modeled as linear resistors, namely opens, shorts, and bridges. The resistance value represents the defect strength. This approach is also inherited to test emerging non-volatile memories such as STT-MRAM, as can be found in the prior art [10], [11], [12], [20]. For any defect in the MTJ device, it is modeled as a linear resistor either in parallel to (R_{pd}) or in series with (R_{sd}) a defect-free MTJ model, as illustrated in Fig. 6. The physical mechanism of defect is never taken into account and manifested as a difference in the defect model.

To verify the effectiveness of resistive models in modeling the IM state defect, we injected R_{sd} and R_{pd} separately into our STT-MRAM simulation circuits and performed static fault analysis. A static fault is defined as a fault that can be sensitized by at most one operation. To describe static memory faults in a systematic way, we adopted the *fault primitive* (FP) notation [26]. An FP is denoted as a three-tuple $< S/F/R >$, where

- S (sensitization) denotes the operation sequence that *sensitizes* the fault. $S \in \{0, 1, 0\mathrm{w}0, 0\mathrm{w}1, 1\mathrm{w}0, 1\mathrm{w}1, 0\mathrm{r}0, 1\mathrm{r}1\}$;

TABLE 2
Related Work on IM State Defects in MTJ Devices in the Literature

Institute	Method	Stability & Retention	Claimed Physical Cause
Minnesota Unv. (2008) [27]	Experiments	Stable, $RT_{\mathrm{IM}} > 200$ms	Multi-domain structure of the FL induced by the dipole field and large device size
Tohoku Univ. (2010) [28]	Experiments	Metastable, RT_{IM} =?	Inhomogeneous magnetization behavior induced by multi-domain and/or vortex creation
NYU&STT Inc. (2016) [29]	Experiments	Metastable, RT_{IM}= 1us	Inhomogeneous distribution of stray field at the FL from SAF layers
CNRS (2016) [16]	Experiments	Metastable, RT_{IM} =?	Unreversed magnetic bubble forms during the switching process
Intel Corp. (2018) [17]	Experiments	Metastable, RT_{IM} =?	Inhomogeneous distribution of stray field at the FL from SAF layers
Beihang Univ. (2018) [18]	Simulations	Stable, $RT_{\mathrm{IM}} = RT_{\mathrm{P}} / RT_{\mathrm{AP}}$	Skyrmion formation due to non-uniformity of stray field and the DMI effect
UCLA (2019) [30]	Experiments+Simulations	Stable, $RT_{\mathrm{IM}} = RT_{\mathrm{P}} / RT_{\mathrm{AP}}$	Skyrmions formation in MTJs without the DMI effect

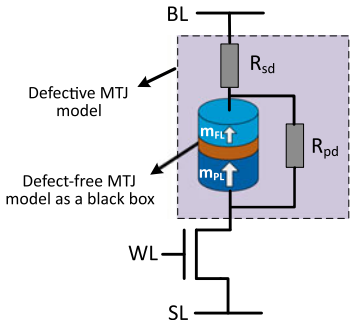

Fig. 6. Resistive models for MTJ-internal defects in the conventional test.

'0' and '1' are logic values, 'r' and 'w' denote a read and a write operation, respectively.

- F (faulty effect) describes the value of the faulty cell after S is performed; $F \in \{0, 1\}$.
- R (readout value) describes the output of a read operation in case the last operation in S is a read. $R \in \{0, 1, -\}$ where '$-$' denotes that R is inapplicable.

For example, $<0\mathrm{w}1/0/->$ denotes a w1 operation to a cell containing '0' (S=0w1) fails, the cell remains in its initial value '0' (F=0), and the read output is not applicable (R=$-$). Using the above FP notation, the entire fault space for single-cell static faults can be defined; it can be easily derived that it consists of 12 FPs [21]. The fault modeling results are shown in Table 3. It can be seen that four different FPs were sensitized; they are IRF0, IRF1, TF1, and TF0. Note that a single defect may cause different FPs, depending on its strength (i.e., resistance in this case).

These four FPs can be used to generate test solutions such as March algorithms. First, each sensitized FP is assigned its own detection condition. For instance, IRF0=$<0\mathrm{r}0/0/1>$ requires a read operation on the faulty cell at state '0' to guarantee its detection, denoted as $\Updownarrow(...0, \mathrm{r}0, ...)$, where $\Updownarrow$ means that the detection condition does not depend on the addressing direction [26]. The detection condition for TF1=$<1\mathrm{w}0/1->$ is $\Updownarrow(...1, \mathrm{w}0, \mathrm{r}0, ...)$, meaning that a down-transition write followed by a read is enough to detect this fault, regardless of the addressing direction. The detection conditions of all sensitized FPs are compiled into the following optimal March test with three march elements:

$$\{\Updownarrow(\mathrm{w}0); \Uparrow(\mathrm{w}1, \mathrm{r}1); \Downarrow(\mathrm{w}0, \mathrm{r}0)\}.$$

Note that different versions of March tests can be generated as long as the test satisfies all the detection conditions.

TABLE 3
Static Fault Modeling Results for IM State Defects Using Resistive Models

Defect model	Resistance (Ω)	Sensitized FP	FP name and abbreviation	Detection Condition
Series resistor R_{sd} (open)	(466, 870]	⟨0r0/0/1⟩	Incorrect Read Fault: IRF0	⇕ (...0, r0, ...)
	(870, 1.6k]	⟨0r0/0/1⟩	Incorrect Read Fault: IRF0	⇕ (...0, r0, ...)
		⟨1w0/1/-⟩	Transition Fault: TF1	⇕ (...1, w0, r0, ...)
	(1.6k, +∞]	⟨0r0/0/1⟩	Incorrect Read Fault: IRF0	⇕ (...0, r0, ...)
		⟨1w0/1/-⟩	Transition Fault: TF1	⇕ (...1, w0, r0, ...)
		⟨0w1/0/-⟩	Transition Fault: TF0	⇕ (...0, w1, r1, ...)
Parallel resistor R_{pd} (bridge)	[0, 1.1k]	⟨1r1/1/0⟩	Incorrect Read Fault: IRF1	⇕ (...1, r1, ...)
		⟨1w0/1/-⟩	Transition Fault: TF1	⇕ (...1, w0, r0, ...)
		⟨0w1/0/-⟩	Transition Fault: TF0	⇕ (...0, w1, r1, ...)
	[1.1k, 3.1k]	⟨1r1/1/0⟩	Incorrect Read Fault: IRF1	⇕ (...1, r1, ...)
		⟨1w0/1/-⟩	Transition Fault: TF1	⇕ (...1, w0, r0, ...)

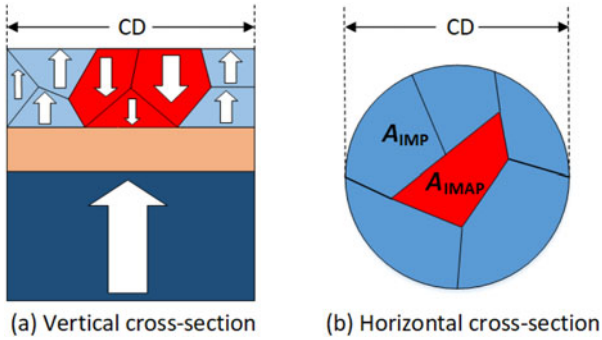

Fig. 7. MTJ schematics with both P-state and AP-state regions in the FL simultaneously.

Based on our measurement results in the previous section, one can easily observe that the sensitized four FPs using the conventional fault modeling approach cannot cover the faulty behaviors of IM state defects in MTJ devices. This is because an IM state defect manifests itself as a resistive state between R_{P} and R_{AP} with an occurrence probability. This means that this defect may turn an MTJ device into the undefined state 'U' and this faulty behavior occurs intermittently. The conventional fault modeling and test approach consider the MTJ device as an *ideal black box* (only state '0' and '1'). Therefore it fails to capture the above-mentioned characteristics of IM state defect. As the four FPs are inappropriate to represent IM state defects, March tests that target these faults obviously cannot detect such defects. Therefore, we need to apply DAT to IM state defects for accurate defect and fault modeling, which will eventually lead to high-quality test solutions that we desire.

5 Device-Aware Defect Modeling

In order to investigate the faulty behavior of memory cell in the presence of an IM state defect, first an appropriate physics-based defect model needs to be developed. In this section, we will follow the device-aware defect modeling approach proposed in [7], which consists of three steps: 1) physical defect analysis and modeling, 2) electrical modeling of defective MTJ device, and 3) fitting and model optimization. Next, we will work out these three steps for the IM state defect.

5.1 Physical Defect Analysis and Modeling

Based on the characteristics and potential forming mechanisms of IM state, as presented with silicon measurements in Section 3, we physically model the IM state at three key aspects as follows.

5.1.1 *Partial Switching Behavior of the FL*

As explained in the previous section, the most probable cause of IM state in MTJ devices is that some parts of the FL switch to the intended state under a write pulse while the rest remain in their initial state due to unreversed magnetic bubbles, inhomogeneous distribution of stray field at the FL, or even skyrmion generations. Therefore, we model this partial switching behavior by splitting the FL into two regions: 1) P-state region and 2) AP-state region with the assumption that these two regions are independent magnetically and electrically. Figs. 7a and 7b show the vertical and horizontal cross-section schematics of an MTJ device with

both P-state and AP-state regions, respectively. As a result, we can derive:

$$1 = \frac{A_{\mathrm{P}}}{A_0} + \frac{A_{\mathrm{AP}}}{A_0} = A_{\mathrm{IMP}} + A_{\mathrm{IMAP}}, \tag{1}$$

where A_0 is the entire cross-sectional area of the MTJ, A_{P} and A_{AP} are the cross-sectional area of the P-state and AP-state regions, respectively. A_{IMP} and A_{IMAP} are the corresponding normalized area with respect to A_0; they can be any value in the range of [0,1]. Note that this model also covers the defect-free case where only P and AP states can exist exclusively; i.e., $A_{\mathrm{IMP}} = 0$ represents AP state whereas $A_{\mathrm{IMP}} = 1$ means P state.

5.1.2 Probabilistic Occurrence of IM State

As introduced previously, the IM state does not show up in all write cycles. Instead, we observed experimentally that it has a certain occurrence probability depending on the applied bias voltage V_{p}, MTJ size CD, and the switching direction. Apart from that, it is expected that the FL thickness (t_{FL}) also plays a role in determining the IM occurrence probability, as it significantly influences the thermal stability of the device [22].

We define a discrete random variable X as whether or not the IM state occurs. For a given V_{p}, CD, and t_{FL}, X obeys a Bernoulli distribution. Its probability mass function Pr (X) is:

$$Pr(X) = \begin{cases} 1 - P_{\mathrm{IM}}(V_{\mathrm{p}}, CD, t_{\mathrm{FL}}) & X = 0 \\ P_{\mathrm{IM}}(V_{\mathrm{p}}, CD, t_{\mathrm{FL}}) & X = 1, \end{cases} \tag{2}$$

As shown in Fig. 4, the correlation between P_{IM} and V_{p} exhibits a curve which is quite similar to Gaussian function (Bell curve). Thus, we model the V_{p} dependence of P_{IM} as:

$$P_{\mathrm{IM}} = H_{\mathrm{IM}} \cdot \exp\left(\frac{-(V_{\mathrm{p}} - V_{\mathrm{pk}})^2}{2V_{\mathrm{wd}}^2}\right), \tag{3}$$

where V_{pk} is the applied bias voltage when P_{IM} reaches its peak H_{IM}, and V_{wd} is a parameter controlling the width of the Bell curve. Note that the polarity of V_{p} determines the switching direction; a negative V_{p} results in an AP→P transition while a positive V_{p} leads to a reversed transition. Since H_{IM} shows a linear scaling trend with CD, as shown in Fig. 5, it can be modeled as a linear piecewise function:

$$H_{\mathrm{IM}} = \begin{cases} S_{\mathrm{lp}} \cdot (CD - 60) & CD \geq 60 \\ 0 & CD < 60, \end{cases} \tag{4}$$

where S_{lp} is the slope of the curve. Since all the measurements we performed were on MTJ devices with the same t_{FL}, it is assumed that t_{FL} has no impact on P_{IM}. However, for a generic model for devices with different P_{IM}, such impact should be incorporated. Combing Equations (2-4), S_{lp}, V_{pk}, and V_{wd} are three fitting parameters which can be tuned and fitted to measurement data, which will be covered later.

5.1.3 Retention Time Estimation of IM State

The retention time of IM state (RT_{IM}) indicates how long the IM state remains after the removal of write pulses; it determines the time period where the memory fault behavior appears in the presence of the IM state. Thus, it is important to estimate RT_{IM} of our devices and integrate it into the defect model if necessary. Conventionally, the following static model is used to roughly estimate the retention time of AP or P state for a given Δ [1]:

$$RT = \tau_0 \exp(\Delta), \tag{5}$$

where τ_0 is the inverse of the attempt frequency ($\sim$1ns). However, the retention time for STT-MRAMs has intrinsic stochasticity, as the magnetization flip induced by thermal fluctuation is unpredictable. This static model fails to capture the stochastic property. Actually, the calculated retention time using Equation (5) corresponds to the time after which the MTJ state flips at a probability of 63%, as pointed out in [31]. As an alternative, a statistic model derived from the switching model in thermal-activation regime is widely used, as can found in [22], [31], [32]:

$$RT = \tau_0 \exp(\Delta) \cdot \left(\frac{1}{1 - P_{\mathrm{RT}}}\right), \tag{6}$$

where P_{RT} is the switching probability of a certain MTJ state due to thermal fluctuation after time RT (i.e., the confidence in the estimation of RT). Next, we will model the retention time of IM state RT_{IM} based on this statistic model.

As illustrated in Fig. 7, the IM state takes place when some parts of the FL switch while the rest remain in their initial state. Thus, the retention time of IM state RT_{IM} is the time period before the magnetization of the P-state or AP-state region spontaneously flips to the opposite direction under the influence of thermal perturbation such that the two regions merge again into an entire one. In other words, RT_{IM} is the smaller one in the retention time of the P-state region and AP-state region.

$$RT_{\mathrm{IM}} = min\{RT_{\mathrm{IMP}}, RT_{\mathrm{IMAP}}\}, \tag{7}$$

$$RT_{\mathrm{IMP}} = \tau_0 \exp(\Delta_{\mathrm{P}} \cdot \sqrt{A_{\mathrm{IMP}}}) \cdot \left(\frac{1}{1 - P_{\mathrm{RT}}}\right), \tag{8}$$

$$RT_{\mathrm{IMAP}} = \tau_0 \exp(\Delta_{\mathrm{AP}} \cdot \sqrt{A_{\mathrm{IMP}}}) \cdot \left(\frac{1}{1 - P_{\mathrm{RT}}}\right). \tag{9}$$

In the above equations, Δ_{P} and Δ_{AP} are the thermal stability factor of the normal P and AP states of MTJ, respectively. RT_{IMP} and RT_{IMAP} are the retention time of the P-state and AP-state regions in IM state, respectively. The modeling principle for RT_{IMP} and RT_{IMAP} is based on the observation with device-level silicon measurements that Δ scales linearly with CD (i.e., $\sqrt{A}$) when CD $>$ 40nm [33].

Fig. 8 shows the estimated retention time in IM state RT_{IM} as a function of A_{IMP}. It can be seen that RT_{IM} increases with A_{IMP} until reaching a peak at $A_{\mathrm{IMP}} = 0.64$, after which it goes down. The maximum RT_{IM} can be up to one day for both P_{RT}=63.0% and 99.9%. However, it is still more than three orders of magnitude smaller than RT_{P}; note that RT_{P} is smaller than RT_{AP} due to the existence of stray field at the FL. Furthermore, the large amount of Joule heating generated under switching pulses may increase the junction

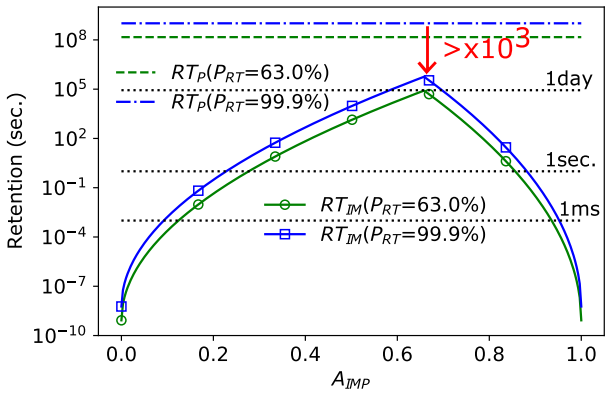

Fig. 8. Retention time estimation of IM state.

temperature by more than $50°$ [34]. This will further reduce RT_{IM} in practice.

5.2 Electrical Modeling of Defective MTJ Device

With the obtained physical model of IM state, we can map it to the three key electrical parameters: R, I_{c}, and t_{w} as a reflection of the impact on the device's electrical behavior.

As we model the IM state by splitting the FL into AP-state and P-state regions (see Fig. 7), electrons can go through via either the P-state region or the AP-state region under an electric field. Therefore, the overall conductance of IM state is the sum of the conductance of these two parallel regions.

$$G_{\mathrm{IM}}(A_{\mathrm{IMP}}) = G_{\mathrm{P}} \cdot A_{\mathrm{IMP}} + G_{\mathrm{AP}} \cdot (1 - A_{\mathrm{IMP}}), \tag{10}$$

where G_{P} and G_{AP} are the conductance when the entire FL is in P and AP states, respectively. A_{IMP} is the normalized area of P-state region in IM state with respect to the entire cross-sectional area of the FL. By replacing conduction with resistance (G=1/R) in the above equation, we can derive:

$$R_{\mathrm{IM}}(A_{\mathrm{IMP}}) = \frac{R_{\mathrm{P}} \cdot R_{\mathrm{AP}}}{R_{\mathrm{P}} \cdot (1 - A_{\mathrm{IMP}}) + R_{\mathrm{AP}} \cdot A_{\mathrm{IMP}}}. \tag{11}$$

R_{P} and R_{AP} are both dependent on the bias voltage V_{MTJ} applied across the MTJ device. Fig. 9a shows the measured R-V loop of MTJ C, the same one shown in Fig. 4; the red solid curves are fitting curves used to extract the exact resistance at a given bias voltage with the physical model in [13]. With R_{P} and R_{AP} extracted from measurement data at different bias voltages, we can calculate R_{IM} for different A_{IMP} values using Equation (11); the results are shown in Fig. 9b for V_{p}= 10mV, 300mV, and 700mV.

Conventionally, the switching spectrum between P and AP states in STT-MRAMs can be divided into two regimes: 1) precessional regime for short pulses ($<\sim 40$ns for our devices), 2) thermal activation regime for long pulses [13], [22]. The switching behavior in the precessional regime is dominated by the STT effect while the thermal effect plays a major role in determining the switching behavior in the thermal activation regime. To model the switching behavior between P, AP, and a third IM state, we modify the equation of the critical switching current I_{c} in the STT-switching model as follows [22].

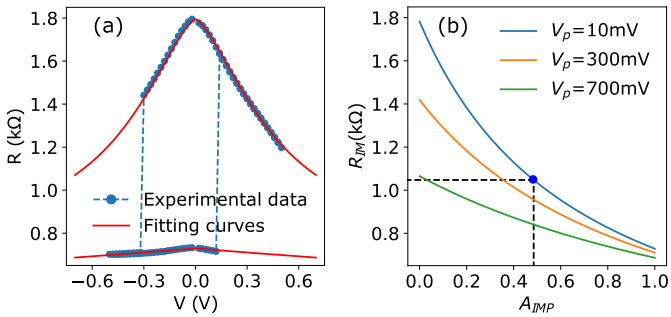

Fig. 9. (a) R-V loop experimental data versus fitting curves to extract R_{P} & R_{AP} at varying voltage, (b) R_{IM} versus A_{IMP} with respect to three voltages.

$$I_{\mathrm{c}}(A_{\mathrm{IMP}}) = \begin{cases} \frac{1}{\eta}\frac{2\alpha e}{\hbar} M_{\mathrm{s}} H_{\mathrm{k}} t_{\mathrm{FL}} A_0 A_{\mathrm{IMP}}, & \mathrm{IM(P)} \rightarrow \mathrm{AP} \\ \frac{1}{\eta}\frac{2\alpha e}{\hbar} M_{\mathrm{s}} H_{\mathrm{k}} t_{\mathrm{FL}} A_0 (1 - A_{\mathrm{IMP}}), & \mathrm{IM(AP)} \rightarrow \mathrm{P} \end{cases} \tag{12}$$

In this equation, η is the STT efficiency, α the magnetic damping constant, e the elementary charge, $\hbar$ the reduced Planck constant. The rest of parameters have already been introduced previously. When $A_{\mathrm{IMP}} = 1$ (indicating P state), the above equation collapses to the original equation for I_{c}(P→AP). When $A_{\mathrm{IMP}} \in (0, 1)$ (indicating IM state), I_{c}(IM→AP) is smaller than I_{c}(P→AP) as only the P-state region in the FL necessitates a flip. Similar interpretation can be inferred for IM(AP)→P switching. Note that the switching from P or AP state to IM state is governed by the aforementioned statistical model in Equations (2) and (4).

Furthermore, the switching time t_{w} in the precessional regime (namely, switched by the STT-effect) can be estimated using the Sun's model as follows [13]:

$$\mu(t_{\mathrm{w}}) = \left(\frac{2}{C_{\mathrm{E}} + \ln(\frac{\pi^2 \Delta}{4})} \cdot \frac{\mu_{\mathrm{B}} P}{e \cdot m \cdot (1 + P^2)} \cdot I_{\mathrm{d}} \right)^{-1}, \tag{13}$$

$$I_{\mathrm{d}} = \frac{V_{\mathrm{p}}}{R(V_{\mathrm{p}})} - I_{\mathrm{c}}(A_{\mathrm{IMP}}), \tag{14}$$

$$t_{\mathrm{w}} \sim \mathcal{N}(\mu(t_{\mathrm{w}}), \sigma(t_{\mathrm{w}})^2). \tag{15}$$

Here, C_{E}≈0.577 is Euler's constant, Δ the thermal stability in P or AP or IM depending on the switching direction, μ_{B} the Bohr magneton, P the spin polarization, and m the FL magnetic moment. V_{p} is the bias voltage across the MTJ device to switch its state. $R(V_{\mathrm{p}})$ is the resistance of the MTJ device; it shows a non-linear dependence on V_{p} (see Fig. 9a). In addition, we assume that t_{w} obeys a normal distribution for a given V_{p} as a model for the switching stochasticity [35].

5.3 Fitting and Model Optimization

In the third step of our device-aware defect modeling approach, fitting and model optimization can be conducted if silicon data is available. With the measured data presented in the Section 3, next we will illustrate this step by fitting the obtained model to a specific device MTJ C as an example. Note that our MTJ compact model is generic and device-to-device variations due to process variations can be modeled by assigning a Gaussian distribution to the key technology parameters of MTJ.

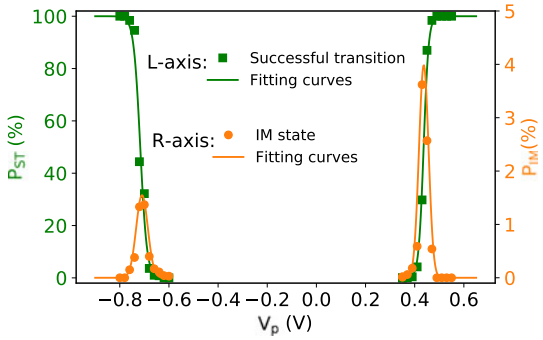

Fig. 10. Curve fitting of P_{ST} and P_{IM} to measurement data.

First, R_{P} and R_{AP} of MTJ C can be extracted from its R-V loop, as shown in Fig. 9a. As the measured $R_{\mathrm{IM}} = 1050\ \Omega$ (see Figs. 3c and 3d) and the read bias is 10mV, we can calculate the A_{IMP} value based on our model. The result is marked with the blue point (A_{IMP}=0.48) in Fig. 9b. Second, the fitting results of P_{ST} and P_{IM} are shown in Fig. 10. On the positive side $V_{\mathrm{p}} > 0$ for P→AP switching, S_{lp}=1e-3, V_{pk}=0.4369, and V_{wd}=0.0145. On the negative side $V_{\mathrm{p}} < 0$ for AP→P switching, S_{lp}=3.9e-4, V_{pk}=-0.7096, and V_{wd}=0.0182. Third, the critical switching current I_{c} is not directly measurable. Thus, I_{c} fitting is not applicable here. In addition, the switching time t_{w} changes with V_{p} as well. The fitting process and results are presented in [13], thus will not be repeated here.

The output of device-aware defect modeling is a calibrated Verilog-A MTJ compact model. After verifying and calibrating the MTJ model in Python as presented previously, we moved this model to Verilog-A so as to make it compatible with circuit simulators. Fig. 11 shows the verification results of the MTJ model integrating the following three variation sources affecting the switching behavior.

- *Switching stochasticity (STO)*: In Fig. 11a, only the switching stochasticity (cycle-to-cycle variation) is enabled while process and temperature variations are disabled. We swept the bias voltage V_{p} from 0.3V to 0.5V in 50 steps, each of which involved a 5k-cycle Mente Carlo simulation to obtain statistical switching results. It can be seen that the circuit simulation results accurately emulate the measurement and fitting results shown in the positive part in Fig. 10.
- *Process variation (PV)*: Process variations in MTJ's geometrical parameters (e.g., CD, t_{FL}, t_{TB}) and magnetic properties (e.g., H_{k} and M_{s}) greatly contribute to the device-to-device variation in the switching behavior on top of the intrinsic switching stochasticity, as shown with silicon data in [36], [37]. Our MTJ model takes into account process variation by introducing a Gaussian distribution to each of the above parameters. Fig. 11b shows the switching statistics with PV enabled only; we set the 3σ corner at 10% away from the average (i.e., 3σ=0.1μ). One can observe that PV on this scale introduces a slightly wider distribution in both P_{ST} and P_{IM} than STO in Fig. 11a.
- *Temperature variation (TV)*: The operating temperature also has a large impact on the switching behavior in STT-MRAM as demonstrated in [37], [38]. In our simulations, we took into account temperature variation by assigning a uniform distribution to the operating temperature from $-40°$ to $125°$ (typical industrial standard). Fig. 11c shows the switching statistics with TV enabled only; it is clear that TV has a contribution as large as STO and PV in the switching variation of STT-MRAM.

Fig. 11d shows the switching statistics combining all the above three sources of variation. It shows that V_{p} may span more than 0.2V from 0% to 100% switching probability; across the entire switching curve, the IM state appears with varying probability as shown in the figure. Due to the large variation in the switching behavior, it is unwise to adopt fixed overdrive pulse amplitude and duration in order to obtain 100% switching in all cells, all cycles, and all operating temperature for write operations in practice.

6 Device-Aware Fault Modeling

Device-aware fault modeling consists of two sub-steps: 1) fault space definition, 2) fault analysis. The former defines all possible faults theoretically. The latter validates realistic faults in the presence of the defect under investigation in a pre-defined fault space using SPICE-based circuit simulations. Next, we will work out these two sub-steps for IM state defects in MTJ devices and compare the fault modeling results with that of the conventional resistive model. Finally, we study the distribution of observed memory faults on write voltage and time for the purpose of test development.

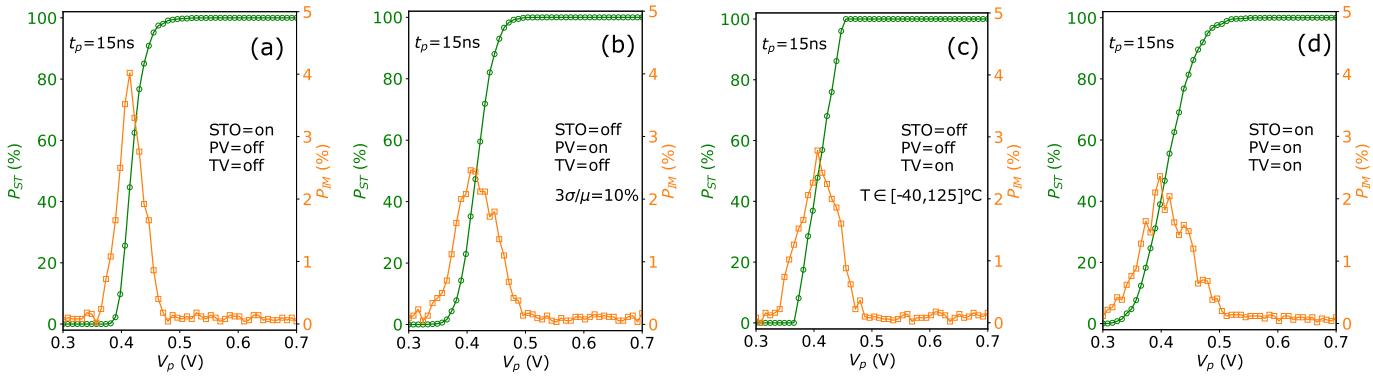

Fig. 11. Verification of Verilog-A MTJ compact model with Cadence Spectre: (a) Switching stochasticity (STO) enabled only, (b) process variation (PV) enabled only, (c) temperature variation (TV) enable only, and (d) all the three sources of variation enabled simultaneously.

6.1 Fault Space Definition

In device-aware fault modeling, we expand the fault space to cover all possible memory faults that we have observed in STT-MRAMs based on measurement data. The upgraded FP notation is $<S/F_n/R>$, where S (sensitizing sequence) remains the same as the one described in Section 4, F_n and R are explained as follows.

- F_n (faulty effect). $F \in \{0, 1, U, L, H\}$, where the additional states 'U', 'L', and 'H' denote undefined, extreme low, and extreme high resistive states, respectively, as have been observed in real fabricated devices [20]. In STT-MRAMs, data is stored in MTJ devices whose pre-defined resistance ranges determine the logic states '0' and '1'. Due to defects or extreme process variations, the MTJ's resistance can be outside of these ranges, as demonstrated with measurement data presented in [20]. The subscript 'n' specifies the nature of the faulty effect. $n \in$ {p, i, t}, where 'p', 'i', and 't' denote permanent, intermittent, and transient faults, respectively. When n=p, it is omitted as a compatibility measure to the conventional notation.
- R (readout value). $R \in \{0, 1, ?, -\}$, where the additional '?' denotes a *random* readout value in case the sensing current is very close to sense amplifier's reference current (e.g., the cell under read is in a 'U' state).

For example, *write transition fault* W0TFU=$<1w0/U->$ means that a down-transition operation (S=1w0) turns the accessed memory cell to an undefined state (F_n=U) permanently; more details about the FP notation and naming scheme can be found in [14], [20]. Based on the above FP definition, the *entire* fault space can be redefined. The total number of *static faults* consists of 52 single-cell faults.

6.2 Fault Analysis

After IM state defects are accurately modeled and a complete fault space is defined, the STT-MRAM netlist with/without an IM state defect can be simulated in a SPICE-compatible circuit simulator to validate the corresponding faults in the space. Our fault analysis consists of seven steps [20]: 1) circuit generation, 2) defect injection, 3) stimuli generation, 4) circuit simulation, 5) fault analysis, 6) FP identification, and 7) defect strength sweeping and repetition of steps 2 to 6 until all defects and their sizes are covered. Given the number of defects is N_{def}; for each defect, we sweep its strength in a certain range with M_{step} steps. Therefore, we will have $N_{\text{def}} \times M_{\text{step}}$ iterations in our fault simulations. Since each iteration is independent on each other, we can run our simulations in parallel to speed up the fault simulation process.

6.2.1 Simulation Setup

The simulation circuits were from [20] with a 3×3 1T-1MTJ array and peripheral circuits (e.g., write driver and sense amplifier). All transistors in the netlist were built with the 90nm predictive technology model (PTM). Process variations in transistors were lumped into the variation in the threshold voltage Vth with 10% away from its nominal value at 3σ corners. For the nine MTJ devices in the memory array, our Verilog-A MTJ compact model with CD=100nm was adopted; Variations in MTJ performance were covered by enabling STO, PV, and TV options in the MTJ model, as detailed in Section 5.3. Three array pitches (3eCD, 2eCD, and 1.5eCD) were selected in our simulations.

The defect injection was executed by replacing the defect-free MTJ model (with only P and AP states) located in the center of the array with a defective one (with P, AP, and IM states) presented in the previous section. The defect strength was configured by assigning a float number to $A_{\text{IMP}} \in (0,1)$ as an input parameter of the Verilog-A MTJ model; it was swept from 0 to 1 in 100 steps in the simulations. The remaining eight MTJs surrounding the central one were always defect-free.

In terms of stimuli, we simulated $S \in$ {0, 1, 0w0, 1w1, 0w1, 1w0, 0r0, 1r1}, i.e., all static operations. V_{DD} was set to 1.6V and V_{WL} at 1.8V. Note that boosting the voltage on the WL is a common practice in the MRAM community due to the source degeneration (i.e., $V_{\text{GS}} < V_{\text{DD}}$) of NMOS selectors [5], [39]. The write pulse width was set to 20ns and read pulse width at 5ns. Due to the large variation in the switching behavior induced by STO, PV, and TV, we conducted 2k Monte Carlo simulations for each sensitizing sequence S.

Since the simulation overhead is immense due to Monte Carlo simulations (2k cycles), we performed the circuit simulations in a cluster with eight compute nodes to speedup the simulation by exploiting job-level parallelism. We first ran the simulation with a defect-free netlist. Thereafter, the whole simulation process was repeated after injecting an IM state defect with certain A_{IMP} value into the netlist. Finally, fault analysis and FP identification can be conducted by comparing the simulation results of the above defect-free and defective cases.

TABLE 4
Fault Modeling Results of IM State Defects Using Our Device-Aware (DA) Defect Model

Defect model	A_{IMP}	Sensitized FP	FP name and abbreviation	Detection condition
DA model	[0.30, 0.61]	$\langle 0w1/U_i/- \rangle$	intermittent write transition fault: W1TFU$_i$	DfT
		$\langle 1w0/U_i/- \rangle$	intermittent write transition fault: W0TFU$_i$	

6.2.2 Fault Modeling Results

Table 4 lists the fault modeling results due to IM state defects. When $A_{\text{IMP}} \in [0.30, 0.61]$, two FPs were observed: $<0w1/U_i/->$ and $<1w0/U_i/->$. The intermittent write transition fault W1TFU$_i$=$<0w1/U_i->$ means that an up-transition operation on a memory cell with inital state '0' transforms the memory cell into a 'U' state with a certain probability (i.e., intermittently). Similarly, the intermittent write transition fault W0TFU$_i$=$<1w0/U_i->$ was also observed. Since these two FPs both involve the 'U' state and are intermittent, they belong to hard-to-detect faults [20]. Their detection cannot be guaranteed by March tests and thus requires DfT solutions. Note that transition failures due to switching stochasticity are typically not considered as memory faults induced by defects [12]; thus, they are excluded here. In addition, no coupling effect of the IM state

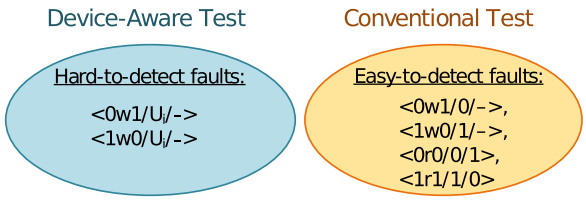

Fig. 12. Comparison of sensitized fault primitives using device-aware defect model (left) and the conventional resistive model (right).

defects was observed in our simulations, irrespective of array pitch, and data pattern in the neighborhood.

6.3 Comparison to the Conventional Resistive Model

Fig. 12 shows a Venn diagram which compares the fault modeling results using our device-aware (DA) defect model and the conventional resistive model. Clearly, the DA model leads to two hard-to-detect faults while the resistive model results in four easy-to-detect faults. There is no overlap between the two circles. This means that IM state defects in MTJ devices exhibits unique faulty behaviors which cannot be covered by the resistor-based defect models. The two FPs sensitized using our DA model are intermittent and involve the 'U' state, which make them hard to be detected by March tests. In contrast, the resistive models resulted in only easy-to-detect faults, since the MTJ device was considered as an *ideal black box* and thus only '0' and '1' states were observed in the simulations.

6.4 Fault Distribution versus Write Voltage and Duration

To investigate the dependence of the observed write transition faults on write voltage and duration, we swept V_{WL} from 1.4V to 2.2V and t_{p} from 10ns to 40ns in our circuit simulations. Fig. 13 shows the simulation result statistics of S=0w1 at varying V_{WL} and t_{p} in the defect-free case. The successful transition probability P_{ST} rises from 0% (red area) to 100% (blue area) as V_{WL} and t_{p} increase. However, one can observe that the transition area occupies a large area in the contour map, which poses a big design challenge for reliable and deterministic write operations in STT-MRAMs. This clearly indicates that write schemes with a fixed configuration of write voltage and duration are unwise in practice with four drawbacks: 1) large energy consumption, 2) long

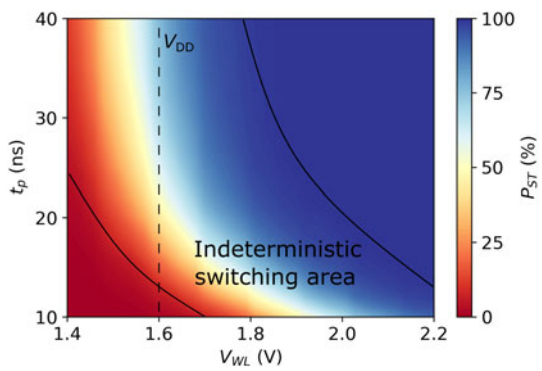

Fig. 13. Successful transition probability P_{ST} statistics in 0w1 operations at varying WL voltage V_{WL} and pulse width t_{p} in the defect-free case.

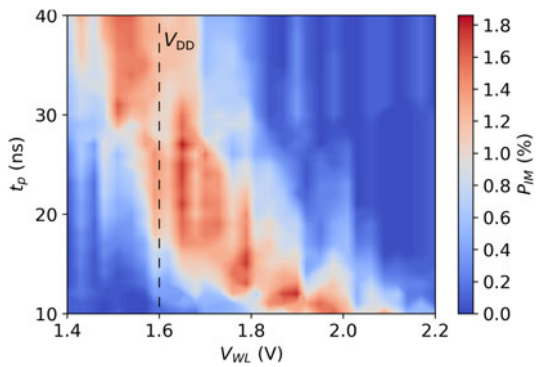

Fig. 14. IM state occurrence probability P_{IM} statistics in 0w1 operations at varying WL voltage V_{WL} and pulse width t_{p} in the defective case.

write latency (performance loss), 3) more susceptible to back-hopping effect [40], [41], and 4) reduced endurance or even early breakdown induced by aggressively wearing out the untra-thin MgO tunnel barrier under a large switching current. This has led to the introduction of more flexible write schemes such as write-verify-write scheme by Intel [5] and self-write-termination scheme by TSMC [42].

Fig. 14 shows the IM state statistics in S=0w1 operations at varying V_{WL} and t_{p} in the defective case (A_{IMP}=0.48 as an example). It can be seen that the IM state shows up with different probability P_{IM} in a large area of the contour plot, especially in the area where P_{ST} is near 50%. Obviously, the closer to the top-right corner, the less likely to see an IM state and more likely to have a successful transition. However, large V_{WL} and t_{p} incur the aforementioned four drawbacks. Hence, in practice, a trade-off has to be made and a flexible and self-adaptive write scheme is more desirable. The simulation results for S=1w0 are similar, thus they are excluded due to space limitations.

7 Device-Aware Test Development

The last step of DAT is to develop appropriate test solutions for the derived faults: W1TFU$_{\mathrm{i}}$ and W0TFU$_{\mathrm{i}}$. In this section, we first explain the test philosophy. Thereafter, a test solution with weak write operations is introduced. Its circuit implementation will also be presented and discussed.

7.1 Test Philosophy

To detect IM state defects, the following two key steps are crucial: 1) fault sensitization, 2) fault detection. The former forces a defective MTJ into the IM state so that it exhibits faulty behavior, whereas the latter distinguishes it from the normal memory behavior. Fig. 15a illustrates the energy barrier diagram of a defect-free MTJ with bi-stable AP and P states [1]. The energy barrier in AP→P switching is larger than that of the opposite switching direction, due to the existence of stray field which is in favor of AP state. Fig. 15b illustrates the energy barrier diagram of a defective MTJ with AP, P, and IM states. As already discussed in previous sections, the IM state can be set with write operations with certain occurrence probability P_{IM}; the peak of P_{IM} occurs at the bias voltage where P_{ST}=~0.5 (see Fig. 4). Once the IM state is set, the device may stay in IM state without external interference for certain period of time (i.e., retention time of the IM state). To skip the IM state and completely switch to P state from AP state, a

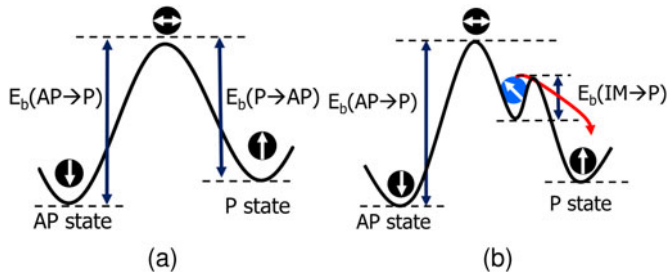

Fig. 15. Comparison of energy barriers between: (a) A defect-free MTJ with bi-stable AP and P states and (b) a defective MTJ with AP, P, and IM states.

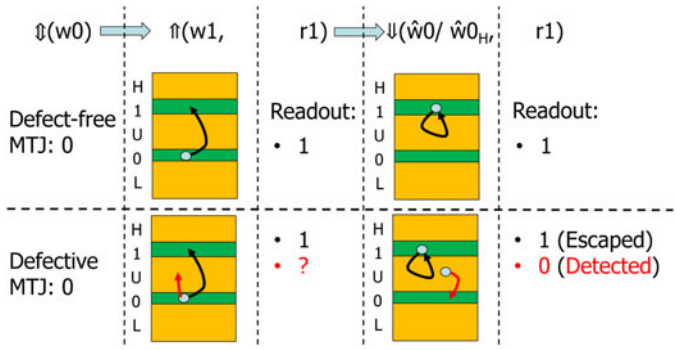

Fig. 16. Proposed March algorithm with a weak write operation $\widehat{\mathrm{w}}0/\widehat{\mathrm{w}}0_{\mathrm{H}}$.

higher energy statistically overcoming the energy barrier E_{b}(AP→P) has to be provided when comparing to the defect-free case. Typically, a higher energy is translated to a larger write voltage or wider write pulse for the current-based switching method. This is root cause of the WER ballooning effect, as observed in several works such as [36].

Depending on the retention time, the IM state can be meta-stable or stable. If the IM state is meta-stale, it will turn to the bi-stable states: P or AP spontaneously. In this case, we do not consider it as a defect. Nevertheless, a soft read fault may occur if a read operation is very close to a write operation which switches an MTJ device to the IM state; this fault can be tolerated by error correction code. If the IM state is stable (which is the case for our devices), we have to test it since it results in hard faults. To distinguish the IM state from P and AP states, a feasible solution is to provide sufficient external energy to push the device in IM state back to P (or AP) state while avoiding disturbing devices in AP (or P) state.

Typically, there are mainly three sources of external energy which can be provided to affect the thermal stability factor Δ of MTJ. They are thermal energy reflected as temperature (T), electric current (I), and magnetic field (H). The quantitative correlation between these three variables and Δ can be approximately expressed as follows [22], [43]:

$$\Delta(T, I, H) = \frac{E_{\mathrm{B}}}{k_{\mathrm{B}}T} \cdot \left(1 - \frac{I}{I_{\mathrm{c}}}\right) \cdot \left(1 \pm \frac{H}{H_{\mathrm{k}}}\right)^2. \tag{16}$$

First, the above equation indicates that Δ can be reduced by heating up the MTJ devices (i.e., burn-in test). The elevated temperature leads to an increase in thermal perturbation, which in turn increases the chance of spontaneous flip of one state to the others. Although this approach is effective in kicking an MTJ device out of the IM state, the switching direction (i.e., IM→P or IM→AP) is not controllable. Thus, burn-in test is an unsuitable approach to detect IM state defects. Second, applying an electric current I going through the MTJ is also an approach to reduce Δ due to its Joule heating effect. After being spin-polarized, it is also used to switch the magnetization in the FL. More importantly, current-induced switching is bipolar, meaning that the switching direction is controlled by the current direction. Third, external magnetic field H has a large influence on Δ. It is widely used in the characterization test of MRAM and serves as the write method in the first generation of MRAM technology, also referred to as Toggle MRAM. Field-induced switching is also bipolar, as the direction of H determines the switching direction of magnetization in the FL.

In summary, the detection of IM state defects can be achieved by applying a weak write current/field, which provides a moderate energy to push a defective MTJ out of its IM state without disturbing the bi-stable P and AP states of defect-free MTJs. Next, we will elaborate the test process with weak write operations.

7.2 Test Solution With Weak Write Operations

To detect IM state defects, the following March algorithm can be used, as illustrated in Fig. 16.

$$\{\Updownarrow(\mathrm{w0}); \Uparrow(\mathrm{w1}, \mathrm{r1}); \Downarrow(\widehat{\mathrm{w}}0/\widehat{\mathrm{w}}0_{\mathrm{H}}, \mathrm{r1})\}.$$

The first march element $\Updownarrow(\mathrm{w0})$ initializes all memory cells to state '0' in normal mode. The second march element is composed of two operations in normal mode; the first one is an up-transition write and the second one is a read. For a defect-free MTJ, the MTJ state switches from '0' to '1' as intended and the readout is logic '1'. Note that we do not take into account failed transitions caused by the switching stochasticity, since they can be mitigated by circuit-level designs such as write-verify-write as mentioned previously. For a defective MTJ with IM state, the w1 operation may result in a transition to '1' (AP) or 'U' (IM) state. If the device ends up in the 'U' state, the readout value can be *random* ('?'); i.e., sometimes '0', sometimes '1', unpredictably. The third march element consists of a weak down-transition operation in DfT mode and a read operation in normal mode. The weak write operation can be implemented as a relatively weak current ($\widehat{\mathrm{w}}0$) or field ($\widehat{\mathrm{w}}0_{\mathrm{H}}$) with reduced amplitude or duration in comparison to normal write operations. The weak write induces an IM→P transition while it is not strong enough to change AP state. As a result, the readout is expected to be logic '1' for MTJs which are in AP state before the weak write. However, the readout of those MTJs which are in IM state before the weak write is logic '0'.

The implementation of weak write operations requires dedicated DfT. Since STT-MRAM exploits an electric current for w0 and w1 operations in normal mode, adding a DfT circuit to write drivers to tune the write voltage or duration will provide a feasible solution with minimal area overhead. For example, if a weak write voltage on the WL ($\widehat{\mathrm{V}}_{\mathrm{WL}}$) is utilized for the DfT circuit, it has to meet the following requirement: $V_{\mathrm{WL}}(P_{\mathrm{SIM}}{=}1) < \widehat{\mathrm{V}}_{\mathrm{WL}} < V_{\mathrm{WL}}(P_{\mathrm{ST}}{=}0)$, where P_{SIM} is the switching probability of IM state to either P or AP state and P_{ST} is the switching probability between P and AP states. This ensures that defective memory cells

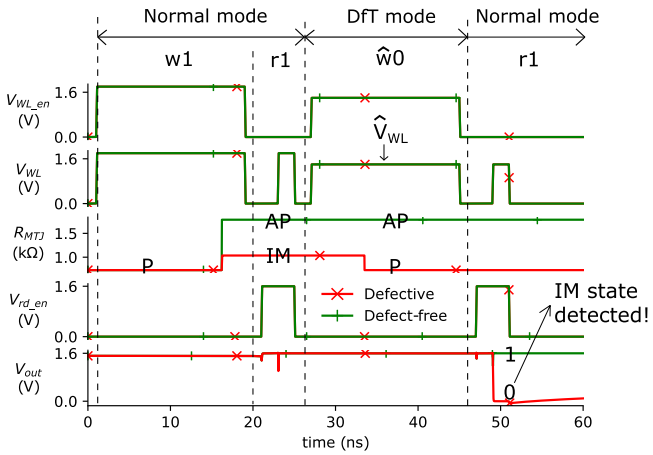

Fig. 17. Test implementation and verification.

are detected while defect-free ones are not over killed. Given this consideration, $\hat{V}_{WL}$ can be set to a point in the black curve in the bottom-left corner of Fig. 13; it marks the boundary of the area where P_{ST}=0. Hamdioui *et al.* [44] proposed a programmable DfT scheme for weak write operations to detect open defects in RRAMs; this DfT scheme can also be adopted here to configure the weak write operations for STT-MRAMs. In addition, Naik *et al.* [38] proposed an internal bias control design for setting optimal write bias voltages in STT-MRAM in order to adapt to different operating temperature. This bias control design for normal write can also be reused to select $\hat{V}_{WL}$ in DfT mode.

We implemented the above March test and verified the design based on circuit simulations of a 3×3 memory array with all peripherals. An IM state defect was injected into the central cell in the array. Fig. 17 shows the waveforms of five key signals in both defect-free and defective cases. First, both the defect-free and defective MTJs are initialized to state '0' (P), as shown with the MTJ resistance (R_{MTJ}) waveform. The normal w1 operation turns the defect-free MTJ into AP state as intended and the defective MTJ into IM state (sensitizing the W1TFU$_i$ fault). Note that $V_{DD} = 1.6$V whereas V_{WL_en} and V_{WL} are both boosted to 1.8V. Next, the r1 operation reads out the MTJ state on the signal V_{out}. The readout of IM state is unpredictable; on the waveform, it outputs a fake '1'. The third operation is a weak write 0 operation $\hat{w}0$ with V_{WL} degraded to 1.4V and t_p unchanged at 20ns in DfT mode. It switches the defective MTJ from IM state to P state, while the defect-free MTJ remains in AP state as the provided energy is not high enough to invoke a full transition from AP state to P state. The last r1 operation detects the IM state defect, since the defective MTJ outputs a '0' while the defect-free case is '1', as illustrated in the figure.

It is worth noting that the above simulation result is a demonstration of the proposed test to detect IM state defects. In practice, the detection of IM state defects is essentially a statistical process, since the IM states appear with certain probability. A single shot of the test cannot give us 100% test coverage of all IM state defects in a large STT-MRAM array. To increase the test coverage, repeating the above march test for a certain number of times can be considered; but this comes with an increase in the test time. Therefore, a trade-off between the test coverage and test cost has to be made, depending on the target applications and required test quality. This will be an important part of our future work to collect statistical data of the proposed test in both large array simulations and silicon implementation.

8 Conclusion

This paper presents comprehensive characterization of IM state defects in STT-MRAM devices. The occurrence probability of IM state depends on the switching direction, device size, bias voltage, and FL thickness. It also demonstrates that the traditional fault modeling and test approach based on linear resistors fails to accurately model this defect at the functional behavior; hence it fails to detect such a defect during manufacturing tests. The use of device-aware test suggests that an IM state defect leads to intermittent write transition faults. To detect them, we propose and implement a test solution based on weak write operations.

Emerging memory technologies such as STT-MRAM, RRAM, and PCM require unique manufacturing steps which could cause *unique* defects. These may not be detected by traditional memory tests, neither can be modeled with traditional fault modeling approaches. This calls for a better understanding of new defect mechanisms and better fault modeling and test approaches such as device-aware test.

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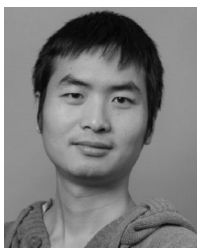

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