An Energy-Efficient 3.7-nV/√ Hz Bridge-Readout IC with a Stable Bridge Offset Compensation Scheme

Jiang, Hui; Makinwa, Kofi A.A.; Nihtianov, Stoyan

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9.8 An Energy-Efficient 3.7nV/√Hz Bridge-Readout IC with a Stable Bridge Offset Compensation Scheme

Hui Jiang, Kofi A. A. Makinwa, Stoyan Nihtianov

Delft University of Technology, Delft, The Netherlands

Wheatstone bridge sensors are often used in precision instrumentation and measurement systems, e.g., for μK-resolution temperature sensing in wafer steppers [1] and mPa-resolution differential pressure sensing in precision air gauges [2]. Since they output small differential signals superimposed on a large common-mode (CM) voltage, typical bridge readout ICs (ROICs) consist of an instrumentation amplifier (IA) followed by an ADC [1]. This paper describes a low-noise energy-efficient ROIC, which achieves a 3.7nV/√Hz input-referred noise PSD and a power efficiency factor (PEF) of 44.1. The latter represents a 5× improvement on the state of the art [3].

As shown in Fig. 9.8.1, the ROIC consists of a capacitively coupled instrumentation amplifier (CCIA) followed by a continuous-time ΔΣ modulator (CTΔΣM). Compared to 3-opamp and current-feedback IAs, CCIAs only require a single amplifier, and are thus more energy-efficient [1,3]. Furthermore, due to their beyond-the-rails capability [4], the bias voltage of the bridge V_{bias} can be much higher than the ROIC's supply voltage, thus maximizing the output of the bridge, as well as the system's overall energy efficiency. Since bridge output is typically much smaller than bridge offset, the CCIA's useful dynamic range, and thus its energy efficiency, is further maximized by an offset-compensation scheme (resistive voltage divider and $CDAC_1$) that reduces bridge offset before it is amplified. Finally, bridge loading is reduced by boosting the CCIA's input impedance via digital ($CDAC_2$) and analog (C_{pf}) positive feedback paths.

A simplified schematic diagram of the CCIA is shown in Fig. 9.8.1. It is based on a 2-stage Miller opamp with a PMOS input pair and a gain of 120dB. As in [1], its up-modulated offset is suppressed by a ripple reduction loop (RRL), which maximizes the useful dynamic range of the following CTΔΣM. The CCIA's input chopper consists of capacitively driven [4] thick-oxide MOSFETs, allowing it to handle bridge CM voltages up to 3.3V (limited by an ESD-protected pad), while operating from a 1.8V supply. C_{in} = 10pF and C_{fb} = 100fF, resulting in a CCIA gain of C_{in}/C_{fb} = 100.

The offset-compensation scheme employs a resistive divider, a 6b capacitive DAC ($CDAC_1$), controlled by an off-chip trimming code ($D_{5\text{-}0}$) and a bank of choppers (Fig. 9.8.1). These can then compensate for part of the chopped input signal by injecting a scaled and chopped version of V_{bias}, i.e., $V_{refchop}$, into the CCIA's virtual ground, as shown in Fig. 9.8.2. Since both the compensating signal and the bridge output are proportional to V_{bias}, the amplified component of bridge output is robust to variations in temperature and V_{bias}. To accommodate bridge bias voltages up to 6.6V, the divider consists of isolated polysilicon resistors with a total resistance of 36kΩ. These scale V_{bias} by k_1=1/4 (MSBs) and k_2=1/8 (LSBs), allowing the DAC's choppers to be driven by 1.8V logic. The choppers are protected by connecting the k_1 tap to an ESD-protected pad. The polarity of the compensating signal can be inverted via the choppers, and so the amplifier's output can be expressed as $(V_{in}C_{in} \pm Q_{DAC})/C_{fb}$, where Q_{DAC} is defined by the trimming code $D_{5\text{-}0}$, the scaled V_{bias} and the DAC's capacitance C_{DAC}. In this design, C_{in}/C_{DAC} = 11.4, which means that the divider's input-referred noise is much less than that of the CCIA.

A known drawback of CCIAs is that they output spikes at twice the chopping frequency $2f_{chop}$ [4]. This is mainly because C_{in} must be rapidly charged and discharged by the bridge whenever the choppers change state. To minimize the amplitude of these spikes, most of the necessary current is provided by the combination of a positive feedback capacitor C_{pf} [4] and a capacitive DAC ($CDAC_2$) which is controlled by the trimming code ($D_{5\text{-}0}$) (Fig. 9.8.1). The latter provides a current proportional to the compensated offset, which is no longer present at the CCIA's output. This approach decreases the spike amplitude and increases the CCIA's input impedance.

The residual output spikes are quite short (decaying within 100ns), and can be avoided by synchronously sampling the CCIA's output with a discrete-time ΔΣ modulator (DTΔΣM) [4]. However, this limits the sampling frequency f_s to $2f_{chop}$ (=400kHz), thus limiting modulator resolution (for a given topology). Synchronously over-sampling the CCIA's output, while possible, would require more output current, and hence, more supply current. In this work, a CTΔΣM is used to relax the CCIA's loading. It samples at f_s = 2MHz, and its input is gated to avoid the CCIA's spikes. As shown in Fig. 9.8.3, the CTΔΣM's inputs are connected to the CCIA's outputs when ϕ_{gate} is high, and briefly shorted to a CM voltage when ϕ_{gate} is low. The ROIC's overall gain is then defined by capacitor ratios (CCIA), resistor ratios (CTΔΣM), and the duty cycle of the gating clock.

Figure 9.8.3 shows the schematic of the gated 2nd-order feedforward 1b CTΔΣM. For high linearity, the 1st integrator employs an active-RC topology based on a folded-cascode OTA with 86dB DC gain. Its input stage is chopped at f_s to suppress 1/*f* noise and offset. The 2nd integrator employs a Gm-C OTA with source degeneration, which saves power and achieves sufficient linearity. The feedforward coefficient is stably defined by the ratio between the degeneration resistors R_s, and the resistors R_{22} in series with the integrating capacitors.

The ROIC occupies an active area of 0.73mm² (Fig. 9.8.7) and consumes 1.2mA from a 1.8V supply. An FFT of its output bitstream, based on 2×10^7 samples, is shown in Fig. 9.8.4. After chopping the modulator's 1st integrator, the 3.7nV/√Hz noise floor is flat from 0.1Hz to 2kHz, which corresponds to a resolution of 15.4b with respect to a full-scale input amplitude of ±10mV. By decimating the ROIC's output with an off-chip $sinc^3$ filter and then acquiring 2×10^8 samples of the filter's output over 100s, the ROIC's 1/f corner frequency was found to be about 0.04Hz.

Measurements on 10 samples show that the ROIC achieves <70pA offset current, 0.3% gain error, 7μV offset. Enabling $CDAC_2$ reliably boosts input impedance by 5× (Fig. 9.8.5). Gating the CTΔΣM reduces the ROIC's gain drift from 74.6 to 8.9ppm/°C, and reduces its offset drift from 105 to 12.5nV/°C when an 118mV (worst case) bridge offset is compensated. As shown in Fig. 9.8.5, gating the CTΔΣM also improves the ROIC's INL from 105 to 28ppm.

The ROIC's performance is summarized in Fig. 9.8.6 and compared with the state of the art. It achieves high accuracy and energy efficiency for ±10mV bridge signals, while accommodating up to ±118mV bridge offset and up to 3.3V input common-mode voltages. With a 3.7nV/√Hz input-referred noise PSD and a PEF of 44.1, this ROIC is about 5× more efficient than [3]. These features make it well suited for the energy-efficient readout of low noise and high precision Wheatstone bridges.

Acknowledgments:
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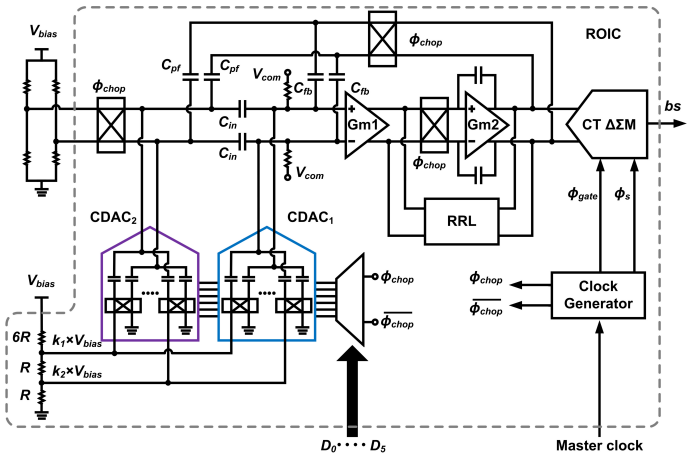

Figure 9.8.1: Simplified circuit diagram of the bridge ROIC.

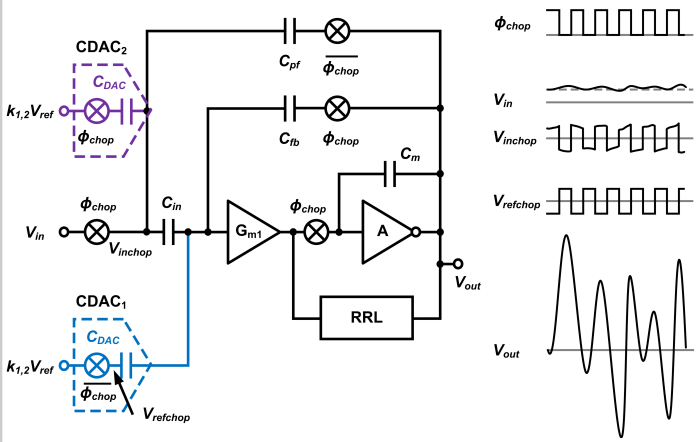

Figure 9.8.2: Block diagram of the CCIA illustrating the operation of the offset compensation and input impedance boosting loops.

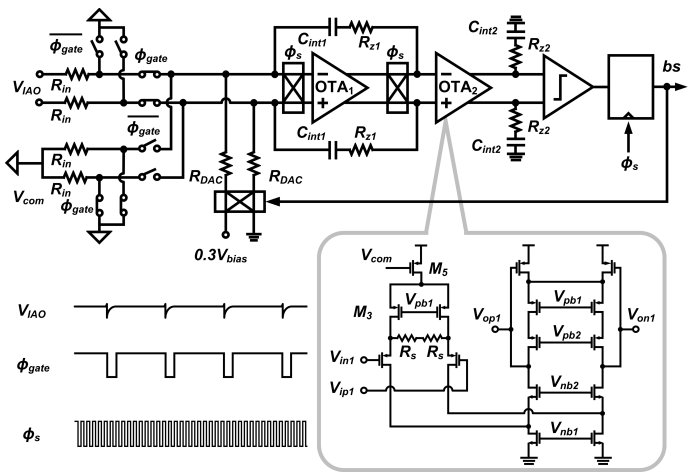

Figure 9.8.3: Simplified schematic of the gated 2nd-order feedforward 1b CTΔΣM.

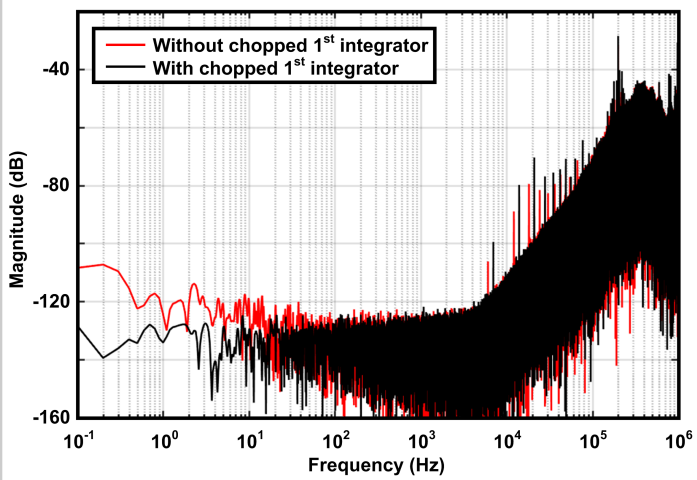

Figure 9.8.4: PSD of the ROIC's bitstream (2× averaging, 2×10⁷ samples with Kaiser window and the residual offset has been subtracted).

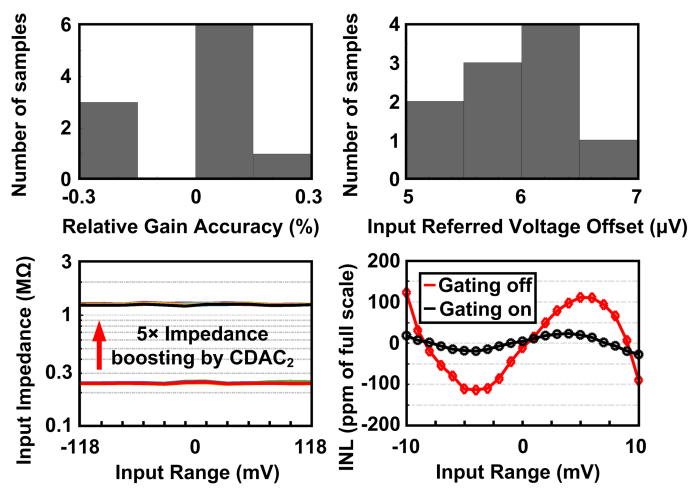

Figure 9.8.5: Measured Relative Gain Accuracy, Offset, Input Impedance and INL of the ROIC.

	This work		[1]	[3]**	[5]	[6]
Architecture	CCIA+ CTΔΣM		CFIA+ DTΔΣM	3-Opamp IA+ CTΔΣM	SHA+ DTΔΣM	AD7193
Technology	0.18μm		0.7μm	0.18μm	0.35μm	--
Year	2016		2011	2016	2011	2011
Supply Voltage (V)	1.8		5	1.55	3.3	5
Supply Current (mA)	1.2		0.27	1.56	2	4.3
±Input range (mV)	118 (offset)	10 (signal)	40	10***	1.65	39
DC CMRR (dB)	134		140	--	--	110
CM Input Range (V)	0 – 3.3		--	--	0 – 3.3	0.3 – 4.8
Gain Drift (ppm/°C)	< 8.9		< 1.2	--	--	1
Offset Drift (nV/°C)	< 12.5		10	--	--	5
Conversion Time (ms)	0.5		170	50	4.1	2.1
Input referred noise density (nV/√Hz)	3.7		16.2	8.2	6.7	5
NEF / PEF* of ROIC	5.0/44.1		10.4/541	12.5/242	11.6/444	12.7/806

* PEF = VDD×NEF²
** Only the current consumption of the IA+ADC is taken into account
*** Calculated as Full Scale Range/Max IA Gain

Figure 9.8.6: Performance summary and comparison with the state of the art.

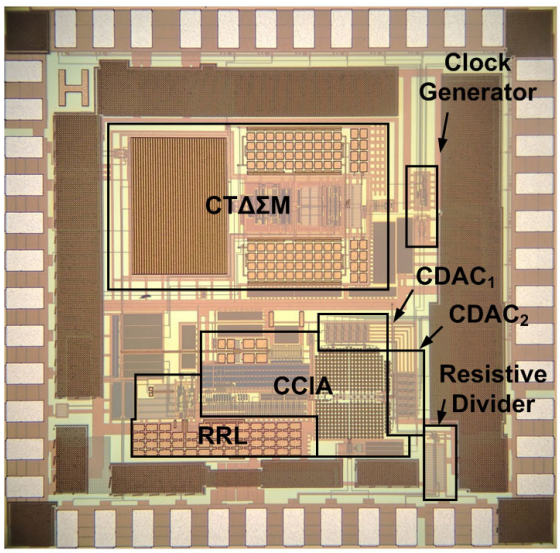

Figure 9.8.7: Die micrograph of the ROIC.

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