Introduction of Zener Diodes, JFETs and DMOSTs in a BiCMOS Process and Implementation of OTP Memory

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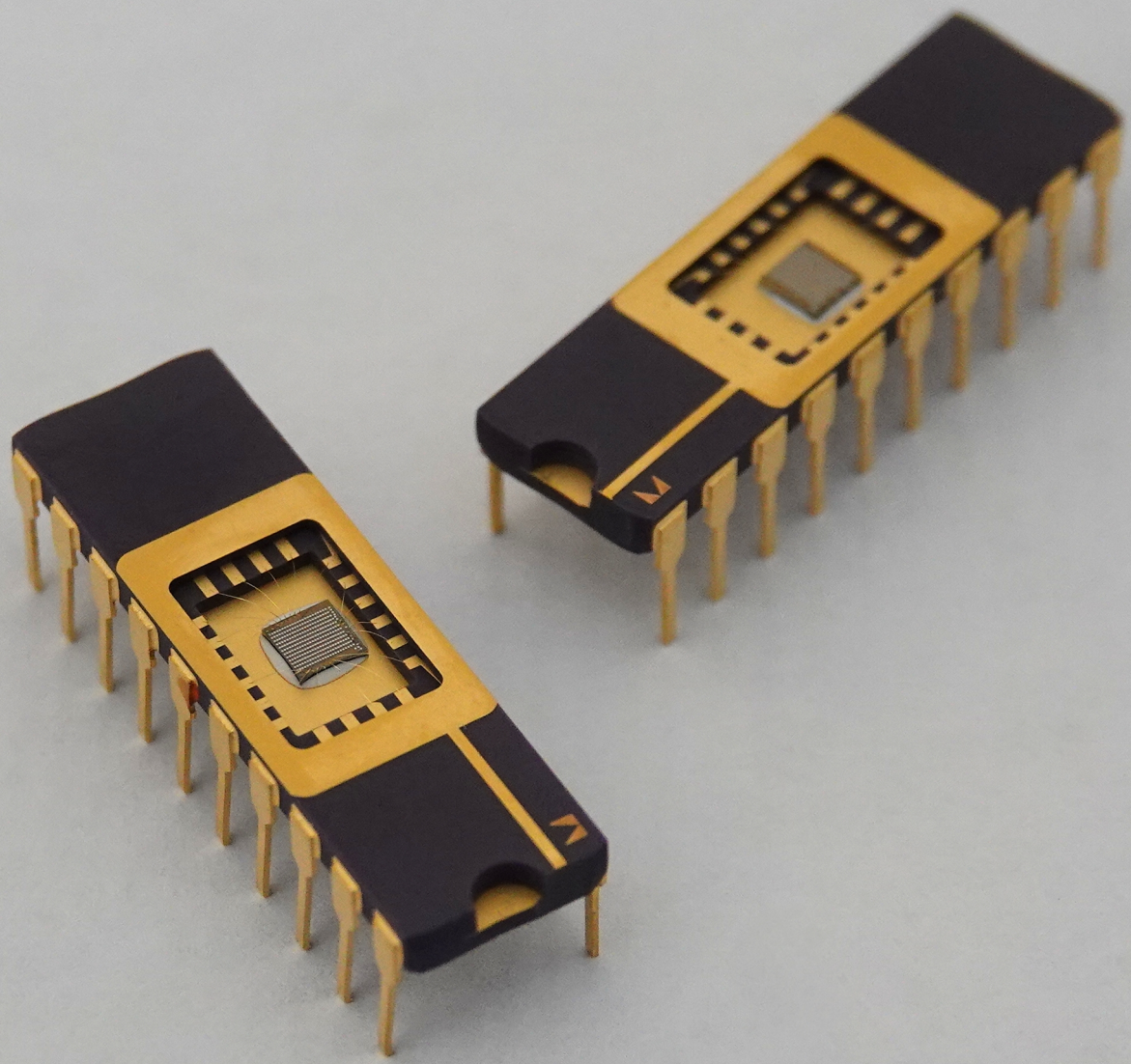

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by

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Abstract

In this research a feasibility study was performed on introducing Zener diodes, junction field-effect transistors (JFETs) and double-diffused MOS transistors (DMOSTs) in an existing silicon 0.25 µm BiCMOS process. As a restriction, no changes to the process were allowed. Lateral polysilicon Zener diodes were designed and optimized for low breakdown voltage and current for the application of One-Time-Programmable (OTP) memory. The selected Zener diode obtained a linear 1 kΩ characteristic by means of a forward biased 10 µs, 8 mA current pulse with 5 V compliance. From cross-sections and (S)TEM images it was concluded that the silicide and cathode dopants migrated into the anode and shorted the junction. Read and write circuitry were successfully designed and implemented into a 405 μm^2 OTP flipflop. This is only about double the size of a standard flipflop in the used BiCMOS technology.

JFETs and DMOSTs were researched to be used in a high-voltage digital signal driver. A functional NJFET and a functional PJFET were fabricated, but the pinch-off voltages were too high to be used for the target application. Both NDMOS and PDMOS transistor variants were successfully implemented with either 10 nm sacrificial oxide (SOX) or shallow trench isolation (STI) as a thick oxide. The selected STI-based NDMOS (SOX-based PDMOS) transistor for 5 V compliance featured a drain-source breakdown voltage of 10 V (−14 V) and 192 µA/µm (−127 µA/µm) drain saturation current. These devices may be used in a high-voltage digital signal driver, possibly in combination with SOX-based thick-oxide PMOS transistors.

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List of Abbreviations

BiCMOS Bipolar and Complementary Metal-Oxide-Semiconductor
CMOS Complementary Metal-Oxide-Semiconductor
DC Direct Current
DMOS(T) Double-Diffused Metal-Oxide-Semiconductor (Transistor)
DTI Deep Trench Isolation
DUT Device Under Test
EDX Energy-Dispersive X-ray
ESD Electrostatic Discharge
FIB Focused Ion Beam
HVDSD High-Voltage Digital Signal Driver
JFET Junction Field-Effect Transistor
NJFET N-channel Junction Field-Effect Transistor
NDMOS(T) N-type Double-Diffused Metal-Oxide-Semiconductor (Transistor)
NMOS(T) N-type Metal-Oxide-Semiconductor (Transistor)
nldd N-type Lightly Doped Drain
OTP One-Time-Programmable
PJFET P-channel Junction Field-Effect Transistor
PDMOS(T) P-type Double-Diffused Metal-Oxide-Semiconductor (Transistor)
pldd P-type Lightly Doped Drain
PMOS(T) P-type Metal-Oxide-Semiconductor (Transistor)
POR Power-On-Reset
RF Radio-Frequency
RTC Resistance Temperature Coefficient
SEM Scanning Electron Microscopy
SOX Sacrificial Oxide
STEM Scanning Transmission Electron Microscopy
STI Shallow Trench Isolation
TEM Transmission Electron Microscopy

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Sander van Dijk
Berkel en Rodenrijs, The Netherlands
August 2, 2018

Chapter 1

Introduction

The level of functional integration on chips is increasing in the semiconductor industry. By adding more functionality on a single die, benefits in terms of interconnect cost, space and performance are obtained. Technologies are typically optimized for a single purpose, e.g. radio-frequency (RF), fast digital, low-noise analog, and additional features are typically outside of this optimized usage region. It would be advantageous to have an optimization of a more generic nature to be able to serve more applications and markets without additional costs. In this study, such an expansion is researched for an existing 0.25 µm RF-optimized BiCMOS process. No additional masks or changes in the process flow are allowed to achieve this. Additional manufacturing costs are then prevented and the RF process optimization preserved.

Two additional features outside the optimized usage region are requested to be used as building blocks for a large variety of RF chips. First, the ability to store per-product information is requested, which is described in Section 1.1. Second, it would be useful if a digital output voltage could be generated with a voltage swing that is larger than the standard MOS voltage limit, without introducing a static power consumption. This is described in Section 1.2.

Both goals require new, non-standard devices that are not readily available in the used BiCMOS process. Therefore, the feasibility of these new devices was studied. The aim is to realize these new devices by means of innovative combinations of existing process steps. This means that process layers and masks can be combined in ways that have not been explored before, but no masks can be added and no process steps can be changed.

1.1 One-Time-Programmable (OTP) Memory

One-Time-Programmable (OTP) memory is a form of programmable read-only memory where every bit can only be written once. OTP memory is widely used in the semiconductor industry, an example is given in Section 1.1.1. It is ideal for serial numbers and other static, per-device information. Furthermore, OTP memory enables better control of process spread by means of parameter trimming. This is an opportunity with large upside in terms of yield and circuit performance. Ideally, all fabricated integrated circuits of a certain type are identical. In reality, there are tolerances in (local) dopant concentrations, layer thicknesses, lateral displacements and many more due to a multitude of causes. The transistors, resistors, capacitors and other devices that are made with this non-ideal process will consequently

show deviation as well. In turn, circuit designers use these devices to create circuits which then inherently deviate too. At multiple steps in the process, parameters are measured and evaluated against tolerance specifications, as illustrated in Table 1.1.

Table 1.1: Hierarchical view on process spread in semiconductor fabrication, from low-level on the left to top-level on the right.

	Material layers	Devices	Products
Element examples	Silicon, dopants, oxide, nitride	CMOS and bipolar transistors, resistors, capacitors	Amplifiers, timers, processors
Spread examples	Layer thicknesses, dopant concentrations	Resistance, threshold voltage, saturation current	Current consumption, maximum frequency, amplifier gain
Measurement	In-line	Process-Control-Monitoring	Wafer test, final test

The final test is performed on every single product and checks whether the performance specification limits stated in the datasheet are achieved. Products that pass the test are shipped to customers and the remaining products are considered yield loss. To minimize this yield loss, outer specification limits can be enlarged which then deteriorates the product. As a better alternative, per-device programmable functionality can be implemented. After measuring the device, adjustments can be made to achieve the specification limits.

1.1.1 Existing OTP Memory Implementation

OTP memory functionality can universally be implemented by fusing a polysilicon resistor by means of a high-current pulse. The change in resistance can then be measured by a sense amplifier. A simple OTP memory circuit is depicted in Figure 1.1.

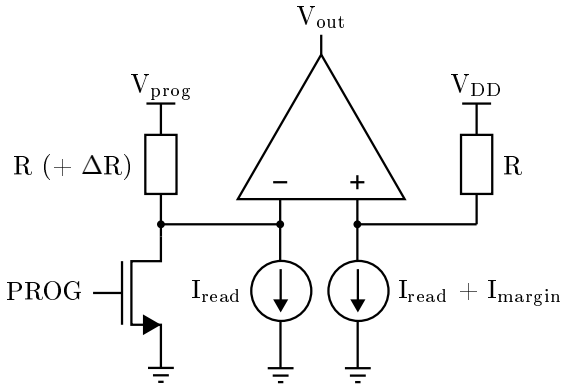


Figure 1.1: OTP memory implementation that increases resistance R with ΔR selectively by means of a high-current pulse, read out by a sense amplifier. During read-out, $V_{prog} = V_{DD}$.

This implementation consumes a relatively large amount of chip area, making the fabrication of the chip more expensive. The polysilicon resistor itself is tiny, but the current that is

required to fuse this resistor has to be selectively switched with a large transistor. In designs similar to Figure 1.1, the transistor that fuses the resistor is mainly determining the die area. Furthermore, the sense amplifier for resistor value readout is large.

When a small-footprint OTP memory implementation is introduced, it becomes more feasible to include it in a chip design. This could reduce the design time and consequently the time to market.

The read process is typically initiated at the startup signal of the power-on-reset (POR). The polysilicon resistor memory elements are then read by the sense amplifiers and the resulting values stored in flipflops to be used during operation. The initial resistor value is low to facilitate the high-current programming pulse at a reasonable voltage. The resistance increases during fusing and consequently the current decreases, decelerating the fusing process and limiting the maximum resistor value. Therefore, the obtainable ΔR from Figure 1.1 is small. A high readout current is then required to achieve sufficient differential voltage margin on the sense amplifier input and therefore facilitate reliable operation of the OTP memory.

1.1.2 Targets for Improving OTP Memory

Compared to fusing a resistor, new devices are experimented to better implement permanent memory functionality in terms of programming current and distinction of the state. With these new devices, new OTP circuits can be designed that aim to improve on the following three aspects.

- **Compact Design** By reducing the die area per implemented OTP memory bit, larger OTP memories become feasible. More opportunities from implementing OTP memory can then be utilized. This is the primary improvement.
- **Easy to Implement** As opposed to streaming out the OTP memory values into external flipflops, the OTP memory implementation preferably already contains a flipflop per OTP cell. OTP functionality is then effectively added to a standard flipflop. These OTP flipflops can then be chained in a shift register to implement a larger memory efficiently. Furthermore, the OTP flipflops should fit in the digital cell structure for close integration with digital circuitry.
- **Reduce Readout Current** Low current consumption is beneficial, especially for mobile applications where battery life is important. Furthermore, by reducing the readout current, more memory elements can be readout in parallel before the maximum instantaneous current consumption is reached. Having more parallel readout then reduces the total readout time.

1.2 High-Voltage Digital Signal Driver

Supply voltages in modern CMOS nodes scale down with the feature size [15]. However, higher voltages are often still required to perform specific tasks within a chip or for interfacing with the outside world, as illustrated in Figure 1.2. A conversion from a low-voltage digital signal to a high-voltage digital signal is then required. In this study, a conversion from the standard 2.5 V MOS voltage swing to 5 V is investigated.

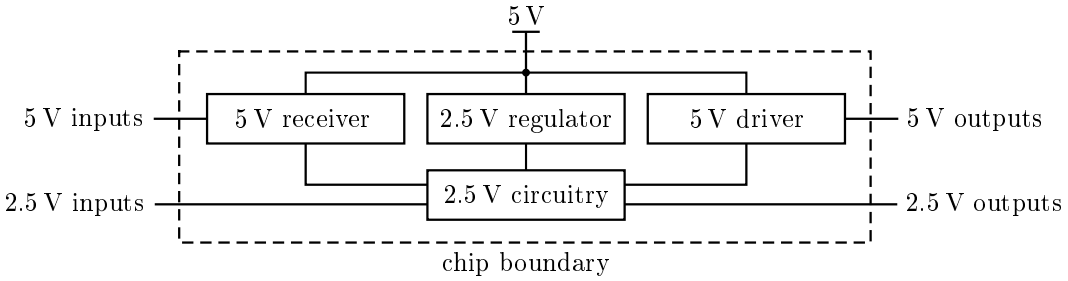
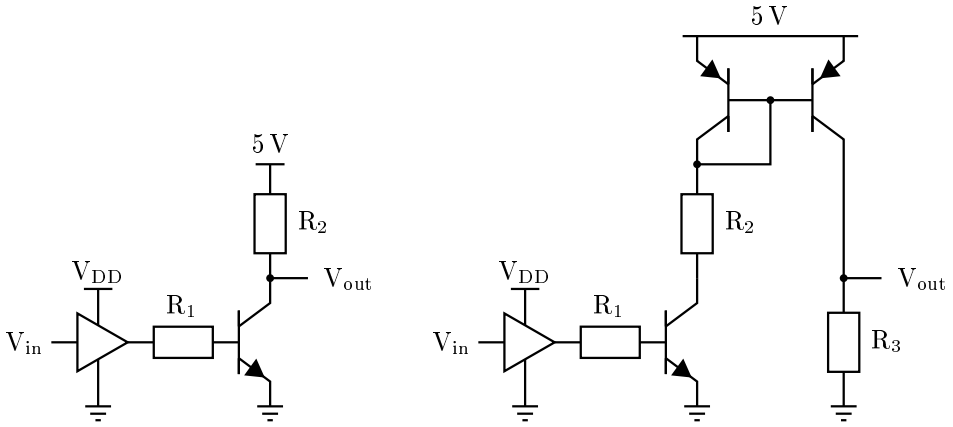


Figure 1.2: A typical system including high-voltage interfacing.

1.2.1 Existing High-Voltage Digital Signal Driver Implementation

The used BiCMOS technology is limited to 5 V with the currently implemented semiconductor devices. The circuits of Figure 1.3 can be constructed with the available transistors to create a 5 V digital signal driver that can be controlled with a digital 2.5 V CMOS output signal.



(a) Active low output, static power consumption when output is low.

(b) Active high output, static power consumption when output is high.

Figure 1.3: High-voltage digital signal driver implementations.

These two circuits have large static current consumption in either one of the output states. This contributes significantly to the total power consumption of the chip, especially when multiple high-voltage outputs are implemented.

With system-on-a-chip emerging, more subsystems are introduced on a single chip, yet the total current consumption may not be increased proportionally. Therefore, less current is allowed per subsystem. Scaling down the current of the high-voltage driver is a big step in reducing the current of these increasingly complex chips.

Furthermore, the circuits from Figure 1.3 are not suitable for voltages over 5 V as the bipolar transistors are reliable only up to 5 V. If future applications would require so, there is no straightforward implementation available.

Finally, the passive state in the two circuits show high output impedance R_2. However, lowering R_2 further increases the static current consumption. This imposes a trade-off between output impedance and static current consumption.

1.2.2 Targets for Improving the High-Voltage Digital Signal Driver

By means of introducing new devices that are capable of handling high voltages, more suitable high-voltage digital signal driver circuits are enabled. Three targets for improving the high-voltage digital driver are identified.

- Minimizing the static current consumption (most critical);
- Achieving low output impedance in both output states;
- It would be advantageous to reach higher voltage ratings than the required 5 V.

1.3 Research Methodology

A feasibility study was performed to solve the problems mentioned by introducing new devices in the existing BiCMOS technology. Zener diodes, JFETs and DMOSTs were researched, designed and fabricated for this purpose. As no device models were available for these new devices, an empirical methodology was used by learning from measurements on fabricated devices. Optimal layout parameters were found by measuring the effects of changing single parameters of the devices at a time; this is design by experiment. The fabrication of these integrated circuits on silicon wafers is time consuming, so only a limited number of production cycles and thus iterations were available.

Two wafer production cycles of three months fitted into the project period. Zener diode, JFET and DMOST structures in various layouts were created in the first iteration. The designs, measurements and discussions of these devices are given in Chapters 3, 5 and 7. This includes DC measurements for each device and additionally current pulse tests for the Zener diodes. Using the measurement results of these devices, improved device designs are proposed in Chapters 4, 6 and 8 and realized in the second production cycle. Each of these chapters include DC measurements and their discussions. Furthermore, Zener diodes are forward biased "programmed" with a current pulse and examined with SEM and (S)TEM in Chapter 4.

The second production cycle also featured circuit implementations of the OTP memory. These circuits are described and the measurement results discussed in Chapter 9. No functional high-voltage digital signal driver was fabricated. A conclusion on the total study and recommendations are given in Chapter 10.

Chapter 2

Background and Implementation Analysis

To solve the problems stated in Chapter 1, implementation options are presented and selected in this chapter. First, the available layers in the used BiCMOS technology are listed and described. Then implementation options for the OTP memory are elaborated and the most suited option for the used BiCMOS is selected. This new OTP memory implementation requires a new semiconductor device to function. Target specifications for the new device are then stated and the first research question is formulated, focused on this new device.

Three implementation options are discussed for the high-voltage digital signal driver and two are selected. The devices required to create these circuits are then discussed, target specifications listed and two research questions are stated.

2.1 Technology

Standard CMOS layers and additionally bipolar layers are available in the used silicon BiCMOS technology. The main layers are listed in Table 2.1. The minimum feature size is 0.25 µm.

Layer	Description
Buried n	N-type low-ohmic buried layer, located just under the wells
Buried p	P-type low-ohmic buried layer, located just under the wells
Active area	Bipolar or CMOS active area, surrounded by shallow trench isolation
Deep trench isolation	Deep isolation barrier
Deep n	N-type highly doped implantation to connect shallow n^+ to buried n
N-well	Moderately doped n-type well
P-well	Moderately doped p-type well
Deep n-well	Moderately doped n-type buried well below the buried layers
Sacrificial oxide	10 nm SiO_2 to mitigate ion steering during well implantations and is selectively removed after
Gate polysilicon	CMOS gate polysilicon, can be n^+, p^- or p^+-doped and can have a silicide layer on top or not
Shallow n^+	Highly doped shallow n-type implantation
Shallow p^+	Highly doped shallow p-type implantation
N-type lightly doped drain	Shallow n-type implantation
P-type lightly doped drain	Shallow p-type implantation
NPN collector	N-type implantation on active area
Emitter polysilicon	N-type highly doped polysilicon
Base polysilicon	P-type polysilicon
Silicide	Low-ohmic metalization of bulk silicon or polysilicon

Table 2.1: Available front-end layers in the used 0.25 µm BiCMOS technology.

To illustrate the layers from Table 2.1, cross-sectional overviews of the CMOS transistors and a resistor are given in Figure 2.1 and Figure 2.2, respectively. The CMOS transistors from Figure 2.1 implement the bulk with either a p-well or n-well which are both back-contacted with low-resistance buried layers. The buried n layer overdopes the buried p layer. The NMOST bulk is automatically connected to the substrate by the buried p layer, but the PMOST bulk is junction isolated by default. After depositioning the gate polysilicon, the n-type lightly doped drain (nldd) and p-type lightly doped drain (pldd) are implanted in the NMOST and PMOST regions, respectively. These regions diffuse under the gate to secure inversion over the full length of the channel during operation. Spacers are then created around the gate and the source/drain n^+ and p^+ implantations are performed. Finally, low-resistance silicide is formed on the silicon surfaces. The nldd/pldd, source/drain and silicide operations are self-aligning with the gate.

As the gate polysilicon is also implanted with the nldd/pldd and n^+/p^+, polysilicon resistors can be made. Figure 2.2 is an example of a gate polysilicon resistor.

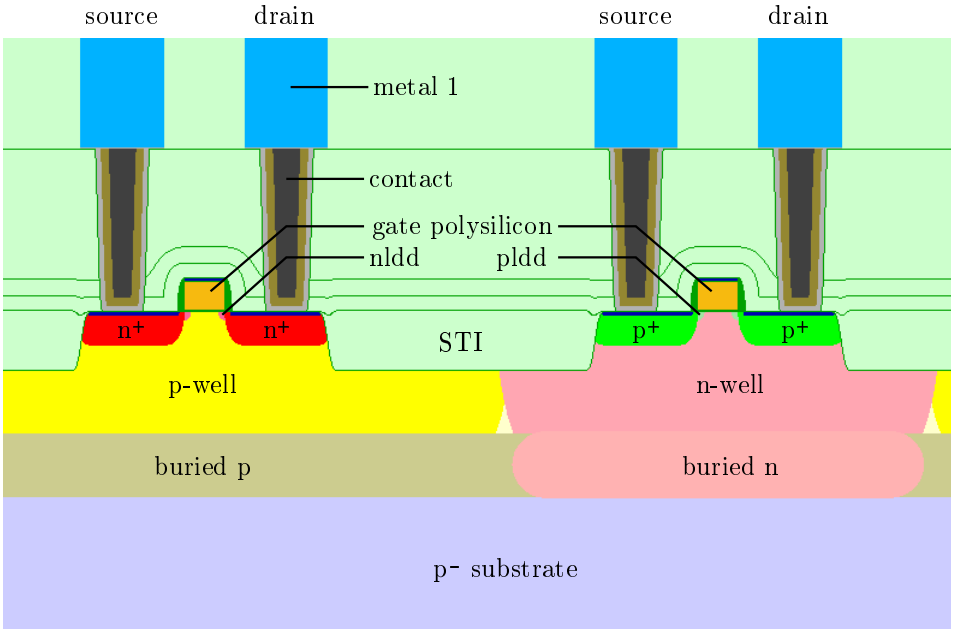


Figure 2.1: NMOS transistor (left) and PMOS transistor (right) from the BiCMOS process used in this study.

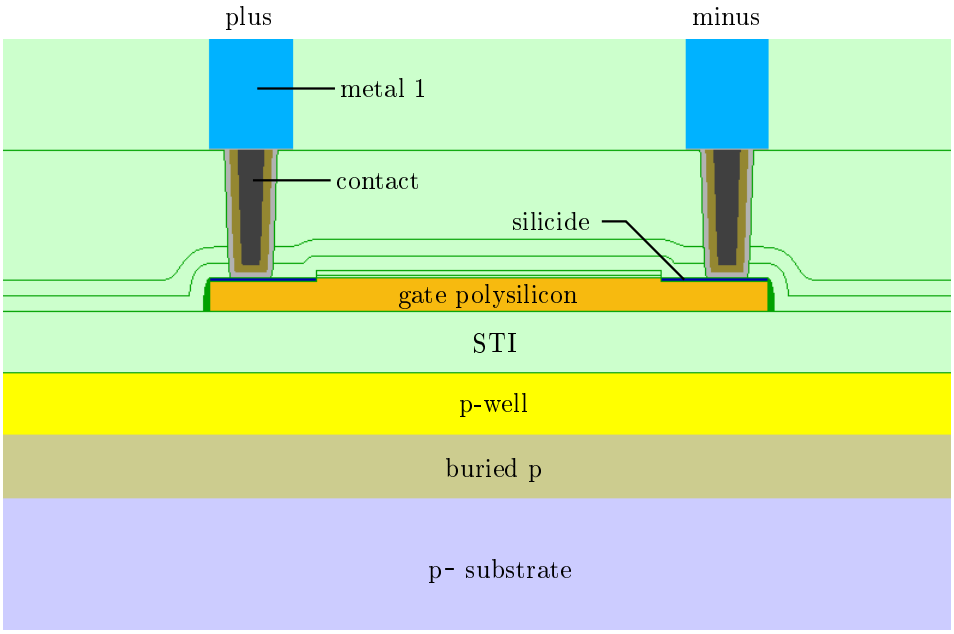


Figure 2.2: Polysilicon resistor from the BiCMOS process used in this study.

2.2 One-Time-Programmable Memory

Multiple OTP implementations are described in literature of which the most common are elaborated in this section. Results from publications are compared while keeping in mind the differences between the technologies used in the publications and the technology used in this

study. In order to enable the selected OTP memory, a new device needs to be implemented within certain specifications. A research question on this new device is then formulated.

2.2.1 OTP Memory Implementation Options

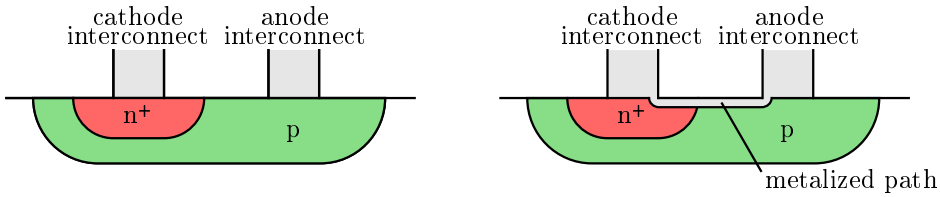
In order to implement a permanent one-bit memory function, at least one element is required that distinguishes between the two states and retains this state when the supply voltage is turned off. This is generally achieved by changing device characteristics with a breakdown mechanism, the type of device and breakdown mechanism however varies. The most common breakdown mechanisms for OTP memory are listed.

Polysilicon Resistor Fusing as OTP Memory Implementation Option

Polysilicon resistors can be fused by means of a voltage pulse. Silicide is typically added to the polysilicon to obtain low-ohmic resistors which fuse at a sufficiently low voltage. The minimum polysilicon width is determined by the technology feature size and is used to obtain minimal fuse power. A maximum of 90 mA was observed by Li when applying a 5 V pulse to a silicidized polysilicon resistor in a 0.6 µm CMOS process [11]. In 90 nm CMOS, a peak of 16 mA was observed by Doorn when applying a 3 V pulse [10]. The breakdown power can be used to compare the two studies; 450 mW in 0.6 µm CMOS and 48 mW in 90 nm CMOS.

Zener Zap Anti-Fusing as OTP Memory Implementation Option

One-Time-Programmable memories are often implemented with Zener zap anti-fusing. Zener zap occurs when a reverse biased Zener diode generates sufficient local heating to facilitate atom migration from the interconnect into the silicon. Along the current path, close to the surface, metal atoms from the cathode interconnect will move towards the anode. This is driven by a phenomenon called electromigration; transport of metal atoms due to momentum exchange with electrons. It occurs at higher current densities at elevated temperatures. The metal atoms from the interconnect will then create a low-resistance metalized path between the anode and cathode, effectively shorting the junction. This is illustrated in Figure 2.3. The metalized path is typically formed at the oxide-silicon interface as the dopant concentration is typically highest at this location and thus the breakdown voltage is lowest here. Typically aluminum is used as electromigration occurs at relatively low temperature and current density, 100 °C and 1×10^5 A/cm^2, respectively [9].



(a) Before. (b) After.

Figure 2.3: Zener zap anti-fusing.

Electromigration might also occur unwillingly, which is called aluminum spiking. Interconnect aluminum atoms migrate into the silicon, changing the silicon characteristics or even shorting junctions entirely. Thin barrier metals such as TiN and TiW were introduced to

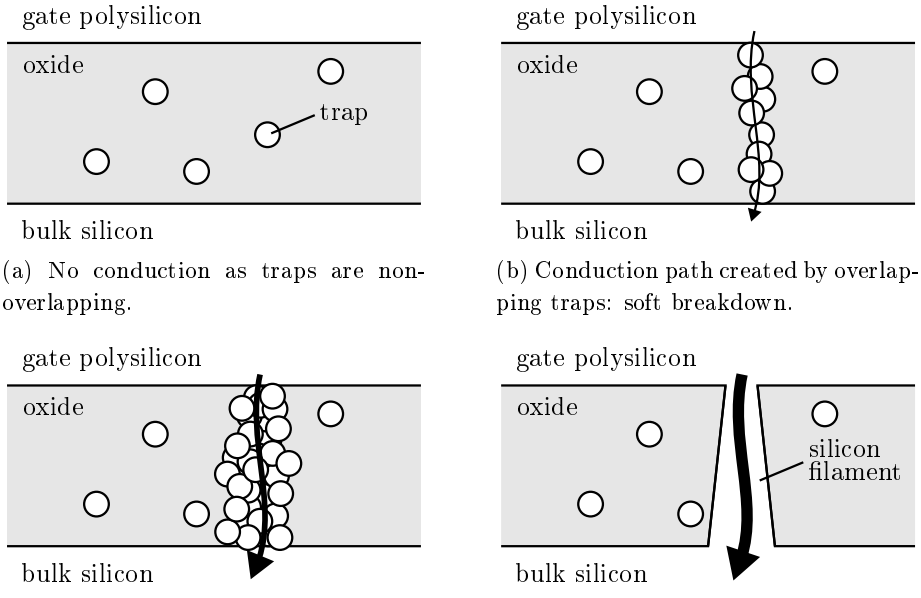
prevent this effect under normal operating conditions, separating the direct contact of aluminum on silicon. Zener zapping remains possible when enough heat is generated to destroy the thin barrier. Such Zener zap anti-fuse OTP memory was implemented by Teichmann, yielding a programming current of 50 mA for a 0.2 µm x 0.2 µm Zener diode [3].

For the high aspect ratios in modern deep-submicron technologies, aluminum does not sufficiently fill the contact openings. Tungsten plugs were introduced to create these contacts instead, while keeping aluminum lines connecting these contacts. The distance between the silicon and interconnect aluminum is too large to facilitate Zener zapping, unless non-standard contact sizing is used as described by McCormick [7].

Gate Oxide Anti-Fusing as OTP Memory Implementation Option

Another way of implementing OTP memory is by anti-fusing gate oxide. Figure 2.4 illustrates the steps of gate oxide breakdown due to traps which is also known as time-dependent dielectric breakdown. At first, no conductive path can be formed between the individual traps in the oxide as they are non-overlapping. However when more traps are generated, the traps are more likely to overlap which then creates a conductive path. Soft breakdown is achieved when there is a current path from one interface of the oxide to the other. Because current will start flowing through the oxide and will heat it up, more traps are generated, creating positive thermal feedback. When enough heat is generated, the silicon at the interface of the oxide melts and forms a filament crossing the oxide. Hard breakdown is then reached [12] [4].

Traps are generated in the oxide through various means and are described by different models. Some well-known models are the anode hole injection model, thermochemical model and hydrogen release model. Furthermore, channel hot-carriers and irradiation are linked to trap generation. Traps can be also be created during fabrication.



(a) No conduction as traps are non-overlapping.

(b) Conduction path created by overlapping traps: soft breakdown.

(c) Additional traps form due to thermal damage, conduction increasing.

(d) Hard breakdown: silicon filament bridging the oxide.

Figure 2.4: Steps of oxide breakdown due to traps [12].

Gate oxide anti-fusing has been evaluated by He in a 0.18 µm CMOS process, yielding a programming voltage of 7 V and current under 1 mA [2]. The readout is simple as the oxide is either an open or short circuit. The oxide thickness in the used 0.18 µm CMOS process is thinner than in the 0.25 µm BiCMOS process used in this study. This predicts a high breakdown voltage for the 0.25 µm technology.

Second Breakdown Damage as OTP Memory Implementation Option

Thornton and Simmons first described the abrupt transition to a low voltage circuit mode at high current densities in bipolar PNP transistors [1]. This is known as second breakdown and appears to occur in all junction devices, regardless of geometric and dopant properties [8]. The reverse-biased, avalanching junction from Figure 2.5 transitions to a higher state of conduction during second breakdown.

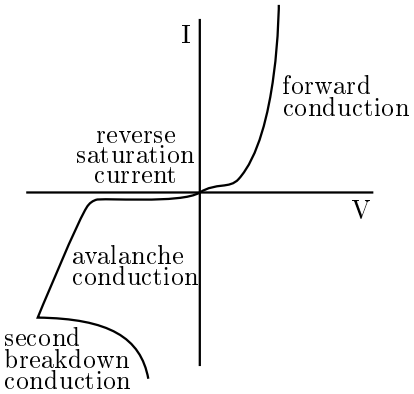


Figure 2.5: I-V characteristic for a diode transitioning to second breakdown [8].

Where avalanche breakdown does not generally leave permanent damage, second breakdown generally does. Smith, Pontius and Budenstein showed that melt filaments were created that bridged the entire depletion region when a 300 mA, 100 µs pulse permanently damaged their 550 µm × 1 µm diode on sapphire substrate. The melt filaments were modeled as a permanent 10 kΩ resistor in parallel with the junction.

Second breakdown is a non-linear thermoelectric effect, for which many models have been proposed in literature. A thermal DC model was proposed by Olson, describing the transition from avalanche conduction to second breakdown conduction. Initially, the avalanche current density is evenly distributed over the junction width as the avalanche breakdown voltage has a positive temperature coefficient. Quasi-uniform heating occurs, only being slightly warmer at the center of the junction due to minimal heat sinking towards its surroundings. When 400 °C is reached, the avalanche voltage temperature coefficient turns negative [8]. The positive thermal feedback makes the diode unstable here, which is considered the second breakdown point. Current filamentation then further raises the temperature locally, burning the diode out when 1600 °C is reached [14].

Avalanche conduction is dominant for electric fields smaller than 5×10^5 V/cm, while electron tunneling is dominant for electric fields over 1×10^6 V/cm. Fair showed that the Zener breakdown voltage drops for higher temperatures, which is primarily because the bandgap voltage E_g decreases for higher temperatures [6]. For avalanching diodes, the breakdown voltage has a positive temperature coefficient initially, but turns negative above 400 °C [14].

Selection of OTP Memory Implementation Option

The four OTP implementation options that have been described are distinctly different, making it too time consuming to research more than one option. The options were therefore weighed and a single method was chosen.

Two studies from literature were used as reference for polysilicon resistor fusing. The feature size used in this study is between the feature sizes from the studies. The fusing power in the used 0.25 µm BiCMOS technology will therefore be between the fusing powers from the two studies; 48 mW and 450 mW. At 5 V, this is between 9.6 mA and 90 mA and was therefore deemed uncompetitive.

Gate oxide anti-fusing is not feasible for its high programming voltage in the 0.25 µm BiCMOS process used in this study. No available transistor operates reliably over 5 V, making the programming, readout and ESD protection circuitry design excessively complex.

The used BiCMOS technology includes tungsten plug contacts, making Zener zap anti-fusing impossible when standard contacts are used. Opportunities for Zener zapping may arise when using non-standard contact sizing, but its effectiveness is unpredictable. The current required to destroy the barrier metal and the effectiveness of the barrier metal to keep the aluminum from spiking the silicon are unknown. Furthermore, the first metal layer might not be planarized properly anymore as it is depositioned in the contact opening instead of on the tungsten plug. A void is then left where the aluminum interconnect should have been.

Smith has shown that avalanching diodes permanently change characteristics when second breakdown occurs. All diodes will experience second breakdown and can be optimized for the voltage and current at which it occurs. The breakdown voltage for an ideal, one-sided diode with abrupt junction is defined as

$$V_B = \frac{\epsilon_s E_{crit}^2}{2eN_B} \tag{2.1}$$

in which V_B is the reverse breakdown voltage, E_{crit} is the critical electric field at which breakdown occurs and N_B is the semiconductor doping in the low-doped region of the one-side junction. An important note is that higher doping concentrations will decrease the reverse breakdown voltage. When solving Equation (2.1) for $V_B = 5\,\mathrm{V}$ in silicon at 300 K, $E_{crit} \approx 12 \times 10^5\,\mathrm{V/cm}$ and $N_B \approx 1 \times 10^{18}/\mathrm{cm}^3$ [13].

For the diodes fabricated in this study the junction is not abrupt, there is a temperature dependence on the critical electric field and poly-crystalline silicon is used instead of mono-crystalline silicon. Therefore, the equation is for the mere purpose of illustration and orientation from which can be concluded that a highly doped diode is required to achieve breakdown voltages under 5 V. Electron tunneling dominates for these diodes as $N_B > 5 \times 10^{17}/\mathrm{cm}^3$, so the diode is classified as Zener diode.

For a 300 µm wide diode, a breakdown power of 100 mA × 33 V = 3.3 W was obtained by Ker in reverse bias. By scaling to a 0.25 µm wide diode, a breakdown power of 2.75 mW is obtained which is 0.55 mA at 5 V. When lateral diodes are used, the breakdown voltage can be adjusted by only changing geometric parameters [5]. Because of the low expected current and the possibility to adjust the breakdown voltage, the lateral Zener diode was chosen as memory element in the OTP memory.

Zener diodes were not previously implemented in the BiCMOS technology used in this study. In order to create OTP memory with Zener diode memory elements, these diodes

were researched and the feasibility and advantages of the Zener diode based OTP memory were evaluated.

2.2.2 Zener Diode Target Specifications for OTP Memory

- An important target is to decrease the programming current, which is the second breakdown current for the Zener diode. This then decreases the size of the programming transistor.
- The second breakdown voltage should be below 5 V for the available transistors to operate reliably in the programming and readout circuitry. Furthermore, the second breakdown voltage should be above 2.5 V in order to survive readout.
- The Zener diode should be small to minimally contribute to the OTP memory die area and thus make larger OTP memory arrays feasible. As reference, a standard flipflop from the library of the used technology is 189 µm^2, so a 10 µm^2 Zener diode is relatively small.
- There should be a distinct difference in device characteristics between the default and programmed Zener diode. The readout circuit specifications are then relaxed and will therefore shrink in size.

2.2.3 Research Question for OTP Memory

The first research question is formulated as follows:

1. Is it possible to implement Zener diodes in a standard BiCMOS process?
    i. How do the geometric properties of these devices affect its characteristics?
        (a) Breakdown voltage
        (b) Forward current
        (c) Reverse current
    ii. How do these characteristics change after a second breakdown event?
    iii. Is it possible to implement a One-Time-Programmable memory with these Zener diodes and what are the optimal geometry and circuit topology for this application?

2.3 High-Voltage Digital Signal Driver

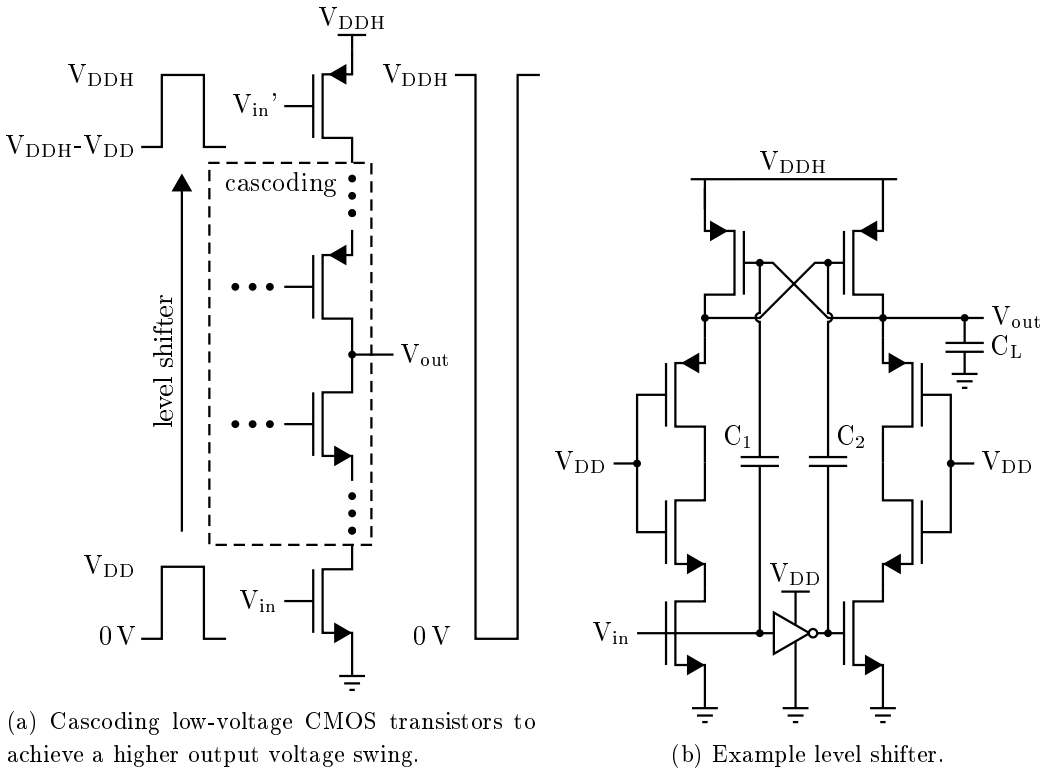
An important requirement of the high-voltage digital signal driver is the static power consumption. Instead of the transistor-resistor solution mentioned in Section 1.2.1, a complementary circuit could achieve this. For instance, CMOS has negligible static current consumption because there is no static current path between the supply rails.

Multiple low-leakage solutions are presented and discussed in this section. Besides fulfilling the improvements stated in Section 1.2.2, a robust and easily implementable solution is aimed for.

2.3.1 High-Voltage Digital Signal Driver Implementation with Stacked Low-Voltage CMOS Transistors

By stacking multiple low-voltage CMOS transistors, a higher voltage rating can be achieved. A circuit illustrating the stacking principle is depicted in Figure 2.6. The disadvantage of the circuit is that level-shifted gate control signals are required. A basic level shifter is depicted in Figure 2.6b, in which capacitors C_1 and C_2 ideally maintain the difference between V_{DDH} and V_{DD} and therefore shift the input signal up by this voltage. A disadvantage is that low frequency input signals are not allowed as the output voltage is only capacitively stored.

A major design consideration is to keep the voltage between the terminals of each transistor within the technology limits. As a constraint in the circuit of Figure 2.6b, V_{DD} should be available before V_{DDH} to properly bias the cascodes. However, as illustrated in Figure 1.2, V_{DD} is typically derived from V_{DDH}. Therefore, the stacked low-voltage CMOS transistor topology was not deemed feasible.



(a) Cascoding low-voltage CMOS transistors to achieve a higher output voltage swing.

(b) Example level shifter.

Figure 2.6: High-voltage digital signal driver with stacked low-voltage CMOS transistors. A level shifter similar to (b) could convert V_{in} to V_{in}' in (a).

2.3.2 High-Voltage Digital Signal Driver Implementation with Junction Field-Effect Transistors

Low static current consumption can be achieved by means of the technology-standard 2.5 V CMOS transistors in combination with JFETs. A JFET cascode limits the voltage over the cascoded low-voltage transistor to the absolute pinch-off voltage of the JFET as it does not conduct beyond this point. As opposed to MOS transistors, JFETs do not typically include thin gate oxides which makes them robust. Junction breakdown typically occurs

at relatively high voltages and additionally, no startup sequence requirements apply on the supply voltages. Because JFETs are voltage controlled devices, no static current is required for operation.

Cascoding of a low-voltage NMOS transistor with an NJFET is depicted in Figure 2.7. The load line demonstrates that the voltage V_x is limited to the absolute pinch-off voltage $|V_p|$ of the NJFET. The NJFET should be qualified for at least 5 V drain-source voltage to guarantee reliable operation.

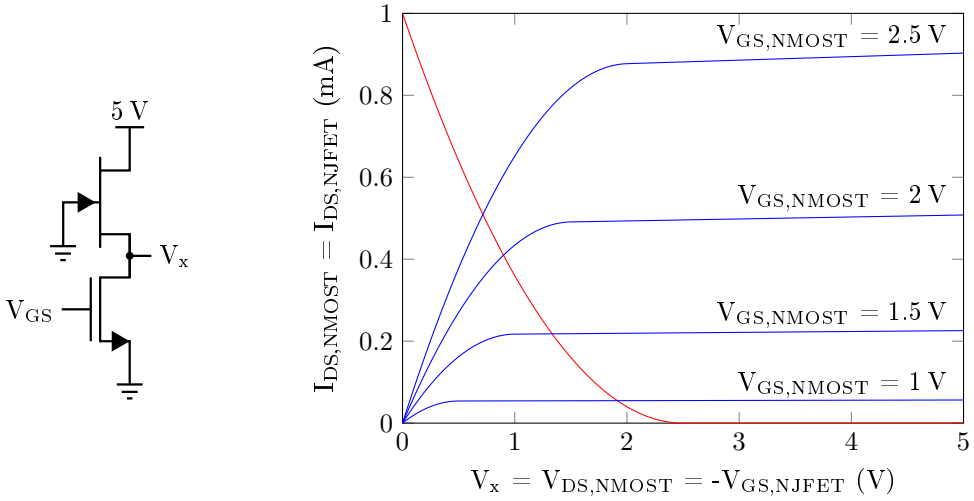


Figure 2.7: Load lines to find V_x for different NMOST gate-source voltages for the circuit on the left, assuming $V_p = -2.5$ V. NMOST V_{DS}-I_D in blue, NJFET V_{SG}-I_D in red and the intersections correspond to V_x.

Similarly, a PMOST can be protected with a PJFET cascode. The PJFET gate is connected to the 5 V supply and the source is connected to the drain of the PMOST. The voltage over the PMOST is then limited to the absolute pinch-off voltage.

High-Voltage Digital Signal Driver Circuit Design with Junction Field-Effect Transistors

By combining both NMOST and PMOST cascoding, the high voltage driver of Figure 2.8 is constructed. The input voltage V_{in} and its inverse $\overline{V_{in}}$ are 2.5 V digital signals that control the 5 V digital output voltage V_{out}. The cross-coupled PMOST pair has two stable operation points which occur when one of the PMOST gates is at 2.5 V and the other at 5 V. Furthermore, when the gates are at equal potential, metastability is achieved. In practice this is an unstable point where any noise will make the system converge towards one of the stable points.

The output stage is required to improve output impedance. Otherwise, by loading the similar node in the level shifter, the cross-coupled PMOST pair could change state.

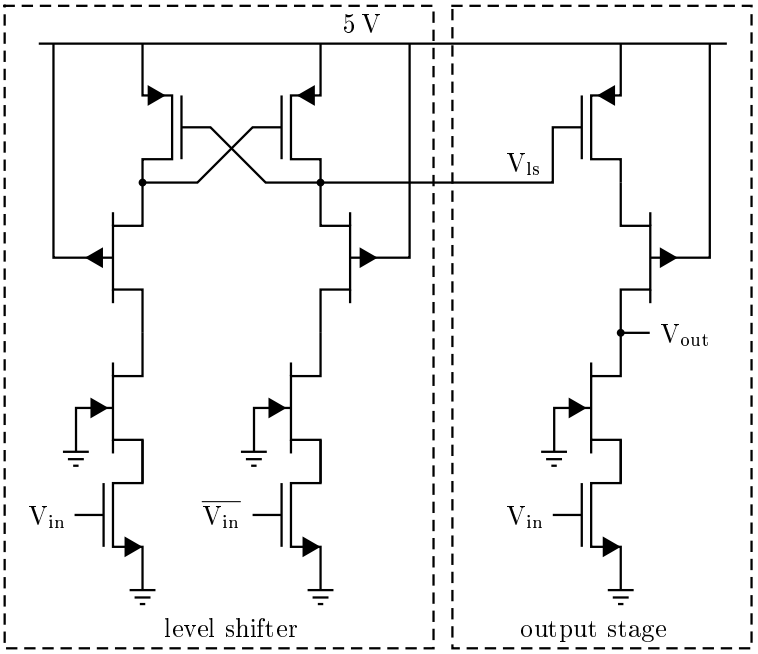


Figure 2.8: High voltage driver implementation with NJFETs, PJFETs and low-voltage NMOSTs and PMOSTs.

Research Question for High-Voltage Digital Signal Driver Implementation with Junction Field-Effect Transistors

The second research question is formulated as follows:

2. Is it possible to implement 5 V drain-source voltage compatible n and p-channel JFETs in a standard 2.5 V BiCMOS process?

    i. How can the pinch-off voltage of these devices be adjusted without changing the process flow?

    ii. What is the limiting factor in breakdown voltage and how can this be optimized for?

2.3.3 High-Voltage Digital Signal Driver Implementation with Double-Diffused MOS Transistors

Instead of protecting the current low-voltage MOS transistors, higher voltage MOS devices could be introduced in the current technology. A type of high-voltage MOS transistor is the Double-Diffused MOS (DMOS) transistor. These transistors feature a double drain diffusion and thicker gate oxide at the drain side compared to the standard MOS transistor.

High-Voltage Digital Signal Driver Circuit Design with Double-Diffused MOS Transistors

The high-voltage digital signal driver circuit from Figure 2.8 can be improved with DMOSTs, see Figure 2.9. Each combination of low-voltage NMOST and NJFET can be replaced with

a single NDMOST. Similarly, the combination of low-voltage PMOS and PJFET in the output stage can be replaced with a single PDMOST. However, the cross-coupled low-voltage PMOST pair, cascoded by the PJFETs can not be replaced with PDMOSTs as that would expose the gate to a destructive signal swing.

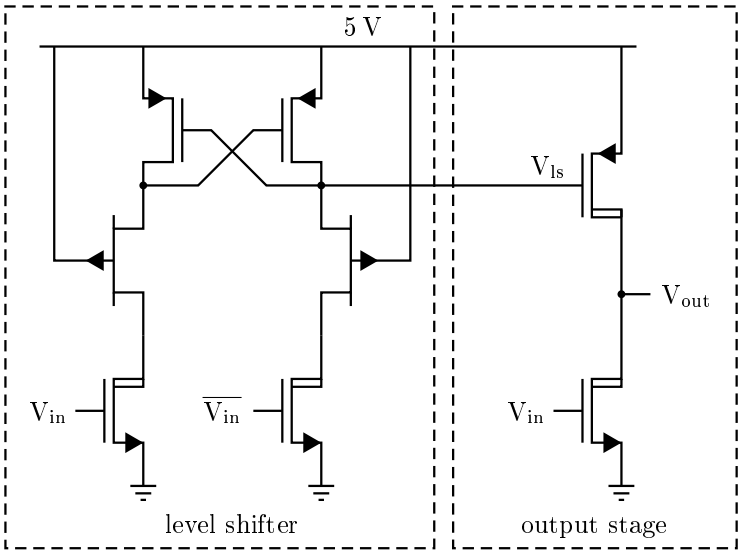


Figure 2.9: High voltage driver implementation with NDMOSTs, PDMOST, PJFETs and low-voltage PMOSTs.

Research Question for High-Voltage Digital Signal Driver Implementation with Double-Diffused MOS Transistors

The final research question is formulated as follows:

3. Is it possible to implement 5 V drain-source voltage compatible n and p-type DMOSTs in a standard 2.5 V BiCMOS process?

    i. How do the geometric properties of these devices affect its characteristics?

        (a) Breakdown voltage

        (b) Threshold voltage

        (c) V_{GS}-I_D curve

        (d) V_{DS}-I_D curve

Chapter 3

Zener Diodes

The requirements on the Zener diode are described in Section 2.2.2. Only the standard, unaltered technology layers from Section 2.1 may be used to meet these requirements. First, suitable layers are selected to form a basic structure for the Zener diode. Then variations on this basic structure are presented and their aimed effect described. DC measurements are performed to characterize the static characteristics of the Zener diode and the effect of each varied parameter on these characteristics. Forward and reverse biased diode breakdown of these Zener diodes is then further examined with current pulse tests. Finally, the devices that are most suited for OTP memory are selected and improvements for the second design iteration are defined.

3.1 Zener Diode Structure

In Section 2.2.1, second breakdown and its strong thermal dependence were described. Reverse diode breakdown is primarily an electric effect and is generally not destructive. Therefore, second breakdown should be reached to change device parameters permanently. Both heat and applied voltage play a role in the second breakdown effect.

Maximizing heat at the junction accelerates the transition from breakdown to second breakdown. Therefore, heat sinking was minimized. Diodes made in the silicon bulk inherently have large heat sinking compared to polysilicon diodes. This is because the polysilicon is thermally isolated from the bulk by thick oxide. Three polysilicon layers are available in the used technology; the CMOS gate polysilicon and the bipolar base and emitter polysilicon. As the base polysilicon is always p-type, no Zener diode can be formed in this polysilicon layer alone. Similarly, the emitter polysilicon is always n-type. Combining the two into a Zener diode is not possible because there is an isolator in between. The intrinsic base is in contact with the emitter, but is too lowly doped to facilitate low breakdown. The gate polysilicon has both p-type and n-type high-concentration implantation options and was therefore selected.

The gate polysilicon is p-type lowly blanket doped and has a high sheet resistance. More heavily doped p-type (p^+) can selectively be created and n-type (n^+) can be obtained by overdoping the polysilicon. With these p, p^+ and n^+ doped regions, lateral polysilicon diodes similar to those researched by Ker can be created [5]. Ker made p^+, p^-, n^+ diodes in which the p^- region length defined the second breakdown voltage and current. The breakdown voltage was altered by using the p^- region as space-charge "buffer".

The high-resistance p- region contributes greatly to the series resistance of the diode. For forward bias this is the turn-on resistance and for reverse bias this is the breakdown resistance. These resistances decrease the voltage over the actual diode and therefore increase the second breakdown voltage of the diode.

Electron tunneling in reverse biased Zener diodes generates heat at the edges of the thin depletion region. However, thermal diffusion occurs towards the surrounding polysilicon, creating a heat gradient around the junction. The reverse current also heats up the surrounding polysilicon due to its resistance.

The local temperature at the junction defines whether second breakdown occurs, but solving for this variable is difficult as this is a complex and dynamic thermo-electric problem. Generally, it can be concluded that heat is ideally focused in the junction region to achieve lower breakdown at constant power. This is proven by Ker when comparing the second breakdown power for forward versus reverse biased diodes. About five times more power was required to achieve second breakdown in forward bias than in reverse bias for equal diodes. In forward bias, the power is mainly determined by the turn-on resistance, which generates heat more equally over the device compared to the reverse biased diode. This is because forward biased junctions cannot exceed the barrier voltage which is typically significantly lower than the reverse breakdown voltage.

The width of the diode did not affect the second breakdown voltage noticeably in Ker's experiment, but the second breakdown current was strongly positively correlated. Diode widths between 150 µm and 500 µm were measured here, being significantly wider than the small Zener diodes for the OTP implementation [5].

Combining the layers from the used BiCMOS technology, the Zener diode from Figure 3.1 was designed. The cross-section is comparable to the resistor from Figure 2.2.

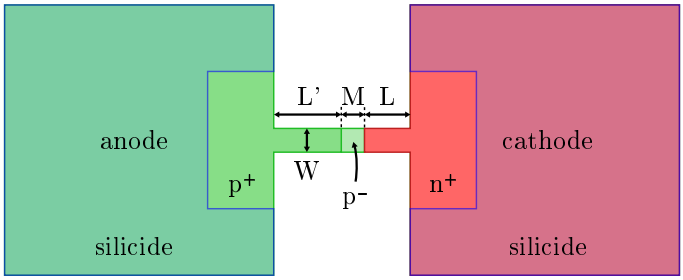


Figure 3.1: Zener diode structure in which L'=L+0.25 µm.

3.1.1 Varied Parameters of the Zener Diode

The basic structure that was presented in Section 3.1 is fabricated in a multitude of variations. Following the design by experiment methodology, the effects of geometric properties are determined by measurements. Starting with a default Zener diode layout, single layout parameters were varied to evaluate the effects.

The diode width (W), middle region length (M) and highly doped region lengths (L) were varied, see Figure 3.1. The experimented variations with these parameters are listed in Table 3.1 and further explained in this section. Additionally, more different variations are experimented as described later.

Table 3.1: Zener diode parameter W, M and L variations, changing only one parameter at a time while keeping default value (in bold) for the remaining parameters. This yields 28 variants in total.

Parameter	Value (µm)										
Width (W)	**0.25**	0.30	0.35	0.40	0.45	0.50	0.60	0.70	0.80	0.90	1.00
Middle (M)	0	0.05	0.10	0.15	0.20	**0.25**	0.30	0.40	0.50	0.75	1.00
Length (L)	**0.5**	0.75	1.0	1.5	2	2.5	5	10			

Width of the Zener Diode

By changing the diode width (W), the diode current in all operation regions scales proportionally, ideally. However, heat sinking becomes relatively less important with wider diodes. Therefore, it is expected that second breakdown occurs at a lower voltage for wider diodes. Furthermore, wider Zener diodes were expected to have more distinct and therefore measurable characteristic changes after second breakdown.

It was mentioned in Chapter 3 that the Zener diode should be small enough to facilitate large arrays of OTP memory cells on a small die area. Therefore, a size constraint of $10\,\mu m^2$ was stated. The maximum diode width was therefore chosen to be 1 µm. The 0.25 µm technology feature size was the minimum width.

Middle Region Length of the Zener Diode

The middle region length (M) is the key parameter in defining the breakdown voltage and the series resistance. The combination of these two then mainly defines the second breakdown voltage, where a shorter middle region causes a lower second breakdown voltage.

As minimum, there is no middle region (M = 0 µm). As maximum, 1 µm is chosen since the depletion region will not be wide enough to stretch through larger middle regions.

Highly Doped Region Length of the Zener Diode

The highly doped region lengths (L, L'=L+0.25 µm) were expected to alter the characteristics via thermal diffusion. More local warming is achieved when heat sinking is minimized, which then lowers the second breakdown power. Therefore, the value of L was expected to show negative correlation with the breakdown voltage and current.

An additional variation was created that takes the diode with L = 10 µm as starting position and adds silicide closer to the junction, see Figure 3.2. Silicide is generally used to create low-ohmic polysilicon connections as it decreases the polysilicon sheet resistance drastically. Siliciding polysilicon up to closer to the junction lowers the total series resistance and thus lowers the second breakdown voltage. On the contrary, silicidized polysilicon was expected to have a higher thermal conduction, facilitating more heat sinking. Furthermore, sufficient distance should be kept between the silicide and the junction to prevent shorting the junction.

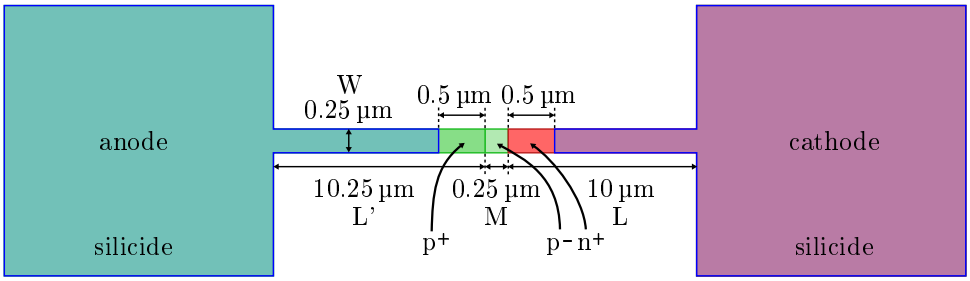


Figure 3.2: Zener diode variation with an extended region of silicide closer to the junction. L and L' are not drawn to scale.

Cathode Implantation Options of the Zener Diode

Two additional Zener diodes were designed that were implanted with n-type lightly doped drain (nldd) in the n^+ region. One variation combines the default n^+ implantation with nldd, the other replaces it. Adding extra doping to the n^+ region decreases the breakdown voltage and reduces the series resistance.

3.2 DC Measurements of the Zener Diode

The DC measurements were performed at wafer level on a wafer prober station using DC probing needles. Triaxial cables were used to connect the needles to an Agilent HP 4155A semiconductor parameter analyzer. Kelvin connections were used to mitigate the effects of series resistance in the cables.

The characteristics of the default Zener diode are first presented, followed by the measurement results of diodes with varied parameters. An evaluation on the effects of each parameter on the characteristics is given and opportunities for the target application are stated. The specifications of all fabricated Zener diodes are listed in Appendix A.

3.2.1 Characterization of the Default Zener Diode

The default Zener diode structure transitions to second breakdown at 8.6 V reverse bias, see Figure 3.3. After a second breakdown event, the structure obtains the linear V-I characteristics of a resistor for both forward and reverse bias. The replacing resistance has typical values in the 10-100 kΩ range. However, outliers were found in the 1-100 MΩ range.

The reverse breakdown effect typically starts around 5.5 V reverse bias and turns linear when the series resistance starts to dominate. Just before the second breakdown voltage is reached, the series resistance drops rapidly, indicating a thermal feedback loop. Before this point, no significant heating occurs as the curves are mostly linear.

In forward bias, diode breakdown typically occurs at 5.3 V, see Figure 3.3. A similar resistive connection between the two terminals is obtained after the breakdown event as in reverse bias.

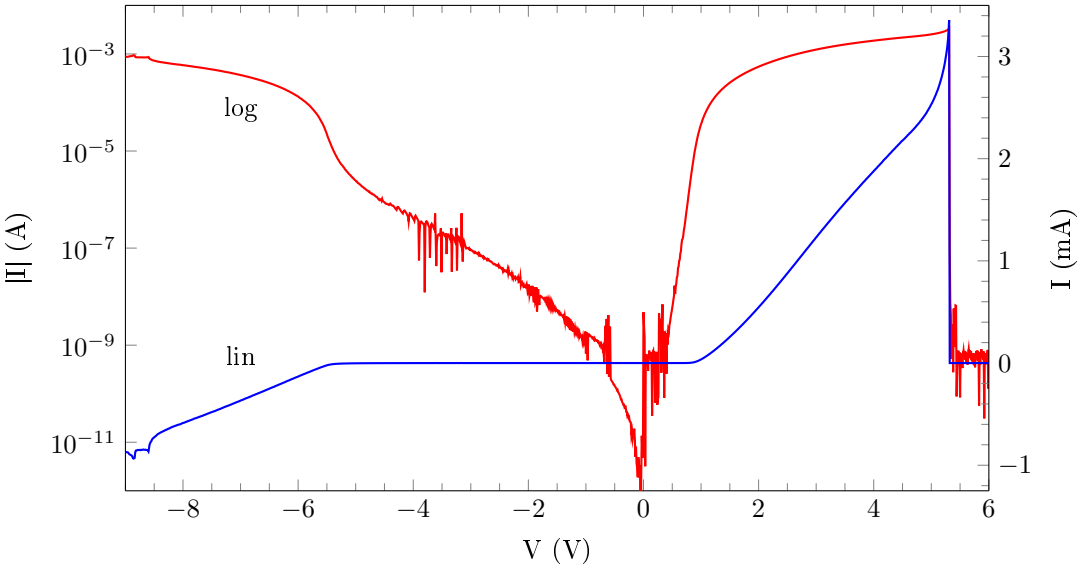


Figure 3.3: Zener diode characteristics for default Zener diode structure with W = 0.25 µm, L = 0.5 µm and M = 0.25 µm. Forward and reverse biased breakdown were recorded in separate measurements.

In Section 2.2.2, a maximum second breakdown voltage of 5 V was specified. This is not achieved for the default Zener diode geometry in either forward or reverse bias. Furthermore, the characteristics change significantly at breakdown and a large deviation was found on the value of the resulting resistance.

3.2.2 Effect of the Diode Width on the Zener Diode Characteristics

Effect of the Diode Width on the Reverse Bias Zener Diode Characteristics

The reverse bias V-I characteristics of Zener diodes with different widths are plotted in Figure 3.4. Wider devices generally transition to second breakdown at lower reverse bias than thinner devices. Both the differential resistance and the reverse breakdown voltage contribute to the second breakdown voltage. As expected, the differential resistance decreases with increasing device width. The reverse breakdown voltage varies per diode and is typically between 4.5 V and 6 V at I = 0.1 mA. No unambiguous relation between device width and reverse breakdown voltage could be found. Instead, it would appear to be a probabilistic effect where wider devices have more chance on lattice defects at the junction. In polysilicon, these defects are expected when the grain boundaries intersect with the junction.

After a second breakdown event occurred during the voltage sweep, wide diodes occasionally formed a permanent low-ohmic (kΩ range) resistive connection between the two terminals. For instance, the 1 µm wide diode in Figure 3.4 demonstrates this phenomenon. This effect was not repeatable, but instead the replacement resistance would range between semi-open circuit ($>$ 10 MΩ) and semi-short circuit ($<$ 10 kΩ).

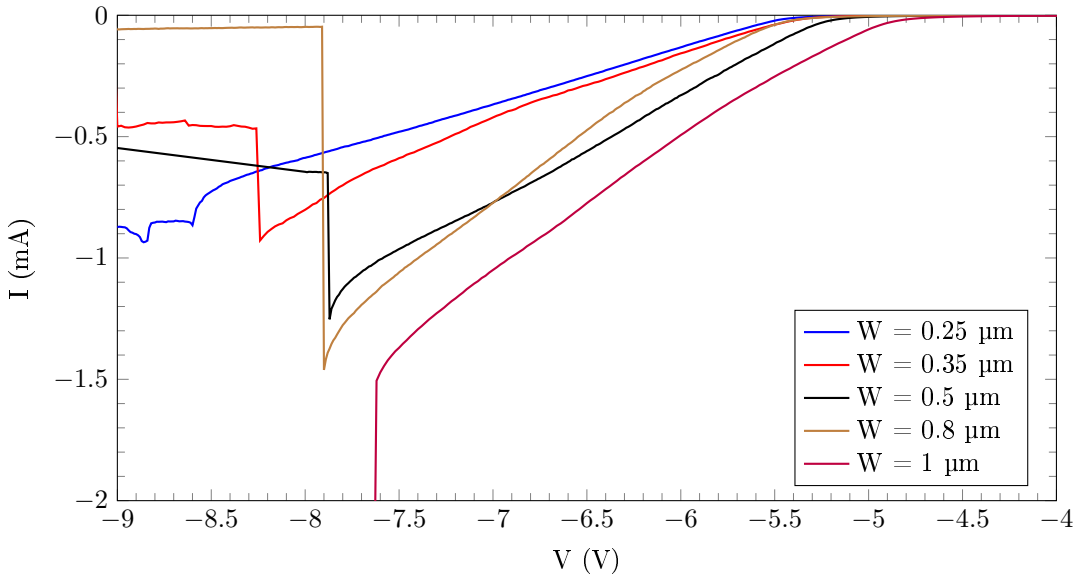


Figure 3.4: Reverse bias V-I characteristics of Zener diodes with different widths. For all cases L = 0.5 µm and M = 0.25 µm.

Effect of the Diode Width on the Forward Bias Zener Diode Characteristics

Lower breakdown voltages are obtained in forward bias than in reverse bias, see Figure 3.5. Furthermore, the current is significantly higher and the total dissipated power at breakdown is about double. This was identified to be caused by the location of heat generation in Section 3.1. In reverse bias, the heat is located primarily at the junction where electron tunneling occurs. In forward bias, the heat generation is spread out more evenly over the length of the device as the actual diode can maximally support the barrier voltage. More heat sinking then occurs in forward bias and therefore, more power is required to heat up the junction to breakdown temperature.

After a breakdown event occurred for diodes wider than 0.5 µm, a low-ohmic connection was typically formed. This was also observed in reverse bias, but in forward bias the resistance was lower (~500 Ω) and the effect was reproducible. When the high-current state was maintained for too long, the resistance increased drastically. Burn-out of the diode fits this increase in resistance.

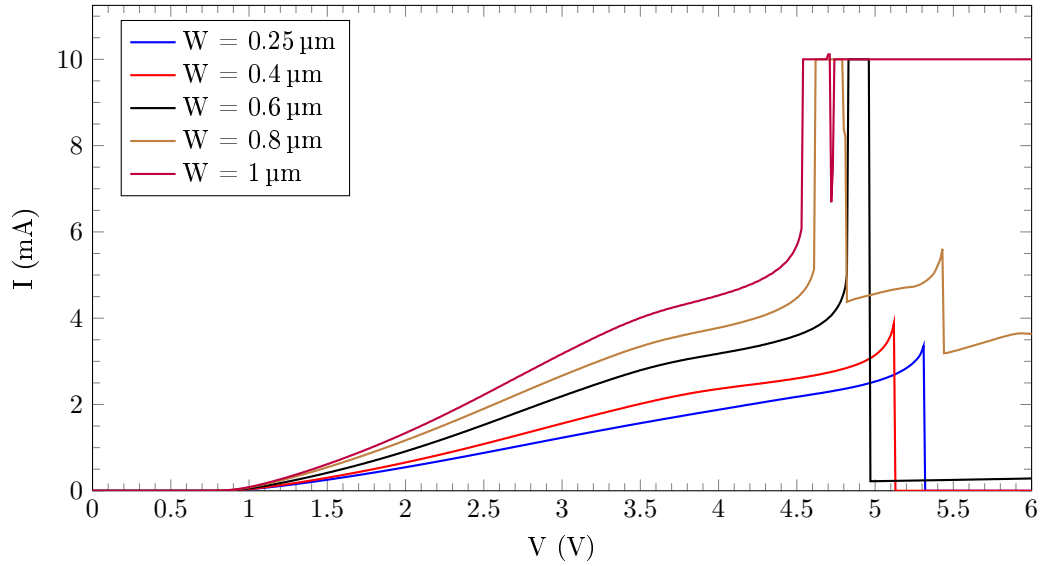


Figure 3.5: Forward bias V-I characteristics of Zener diodes with different widths. For all cases L = 0.5 µm and M = 0.25 µm.

3.2.3 Effect of the Middle Region Length on the Zener Diode Characteristics

Effect of Middle Region Length on the Reverse Bias Zener Diode Characteristics

By lowering the middle region length M, the series resistance decreases, see Figure 3.6. Furthermore, the reverse breakdown voltage decreases for lower values of M which decreases the second breakdown voltage further.

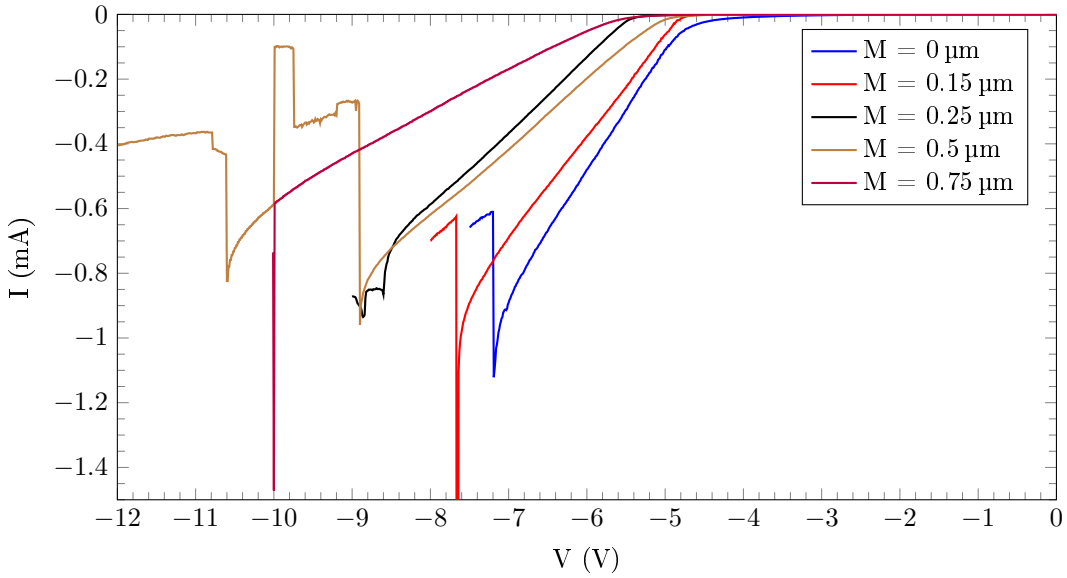


Figure 3.6: Reverse bias V-I characteristics of Zener diodes with different middle p^- region lengths M. For all cases W = 0.25 µm and L = 0.5 µm.

Effect of the Middle Region Length on the Forward Bias Zener Diode Characteristics

The forward biased measurement results of Zener diodes with different middle p- region lengths M are plotted in Figure 3.7. Good control over the breakdown voltage is achieved; lower values of M decrease the breakdown voltage. The diode barrier voltage remains unaltered when M is varied, indicating that the doping concentrations at the junction are similar. The resistance after breakdown varies strongly.

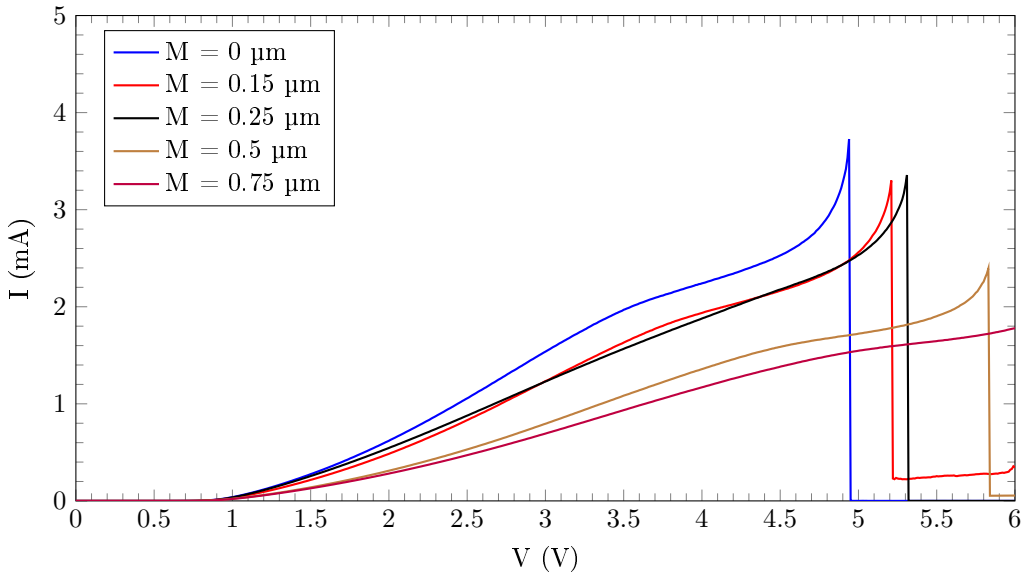


Figure 3.7: Forward bias V-I characteristics of Zener diodes with different middle p- region lengths M. For all cases W = 0.25 µm and L = 0.5 µm.

3.2.4 Effect of the Highly Doped Region Length on the Zener Diode Characteristics

Effect of the Highly Doped Region Length on the Reverse Bias Zener Diode Characteristics

The reverse bias I-V characteristics of the Zener diodes with different highly doped outer region lengths L are plotted in Figure 3.8. By increasing L, the series resistance increases and as result, the second breakdown voltage increases.

The diode with L = 10 µm and silicide closer to the junction has a lower second breakdown voltage than the default Zener diode. Furthermore, the breakdown current is lower, making the total second breakdown power lower as well. A highly repeatable high-current state was found for this long, silicidized Zener diode which is similar the observed effect in forward bias for wide Zener diodes. The second breakdown current is significantly lower than for the wide diodes, but the second breakdown voltage is higher. Similarly, the average resistance after a second breakdown event is 500 Ω.

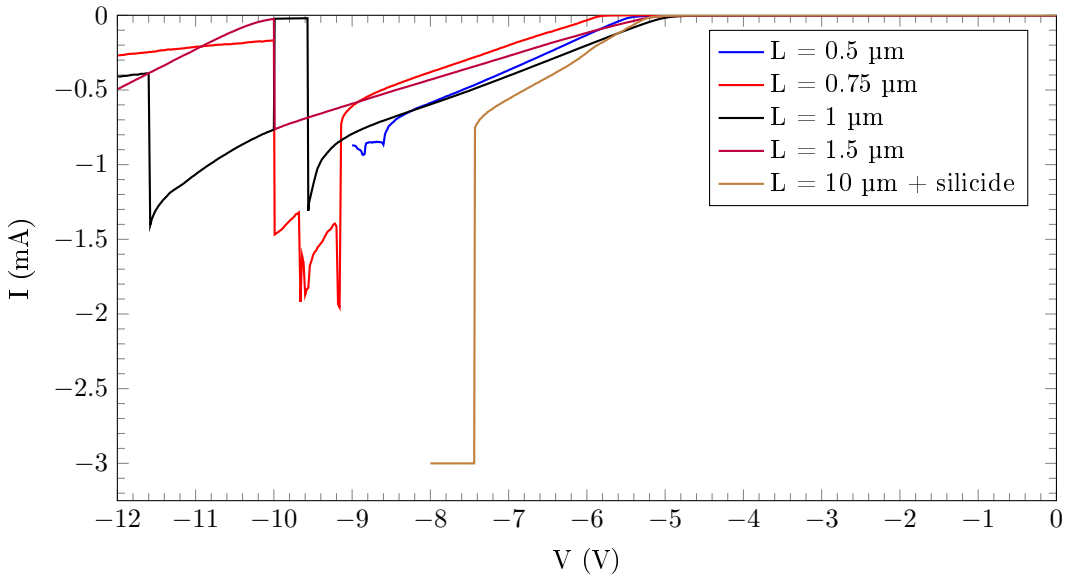


Figure 3.8: Reverse bias V-I characteristics of Zener diodes with different highly doped outer region lengths L. For all cases W = 0.25 µm and M = 0.25 µm.

Effect of the Highly Doped Region Length on the Forward Bias Zener Diode Characteristics

Similar to reverse bias, the series resistance increases for larger values of L which increases the breakdown voltage. The breakdown current decreases from L = 0.5 µm to L = 0.75 µm, but then saturates to a constant value. Heat sinking then primarily occurs towards the surrounding oxide instead of the interconnects. Therefore, it is not advantageous in terms of either breakdown voltage or current to make L larger than 0.75 µm.

The variant with L = 10 µm with silicide added closer to the junction is not advantageous in forward bias. The series resistance is lower, but the breakdown current significantly higher without improving the breakdown voltage compared to the default Zener diode structure. Furthermore, the high-current state that was observed in reverse bias was not repeatable in forward bias.

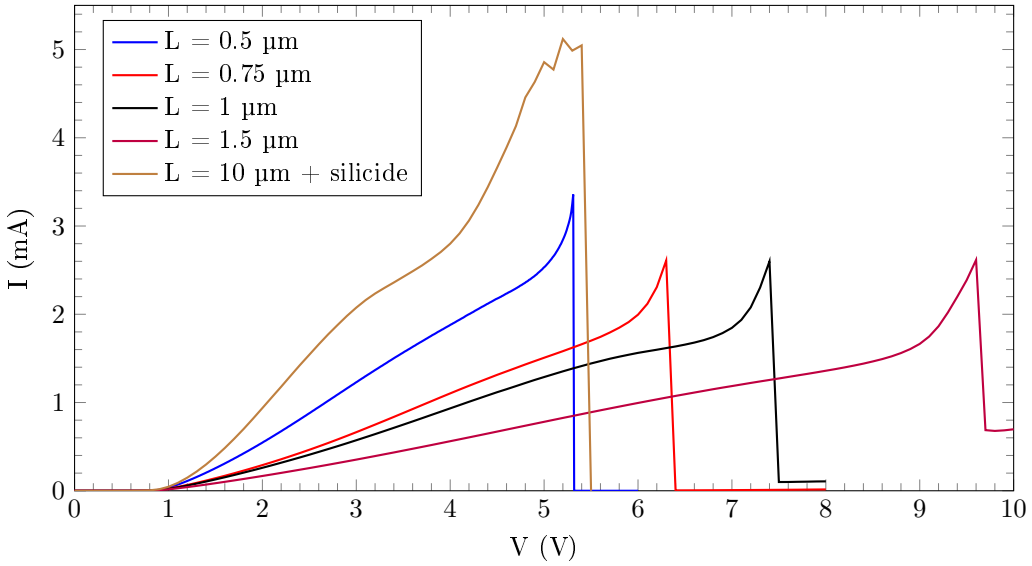


Figure 3.9: Forward bias V-I characteristics of Zener diodes with different highly doped outer region lengths L. For all cases W = 0.25 µm and M = 0.25 µm.

3.2.5 Effect of the Cathode Implantation on the Zener Diode Characteristics

The standard diode structures are implanted with n^+ in the cathode region. Two different masking options were experimented: nldd only and nldd in combination with n^+. The results for reverse bias are plotted in Figure 3.10 and for forward bias in Figure 3.11. Adding nldd to the cathode region is found to lower the (second) breakdown voltage in both forward and reverse bias.

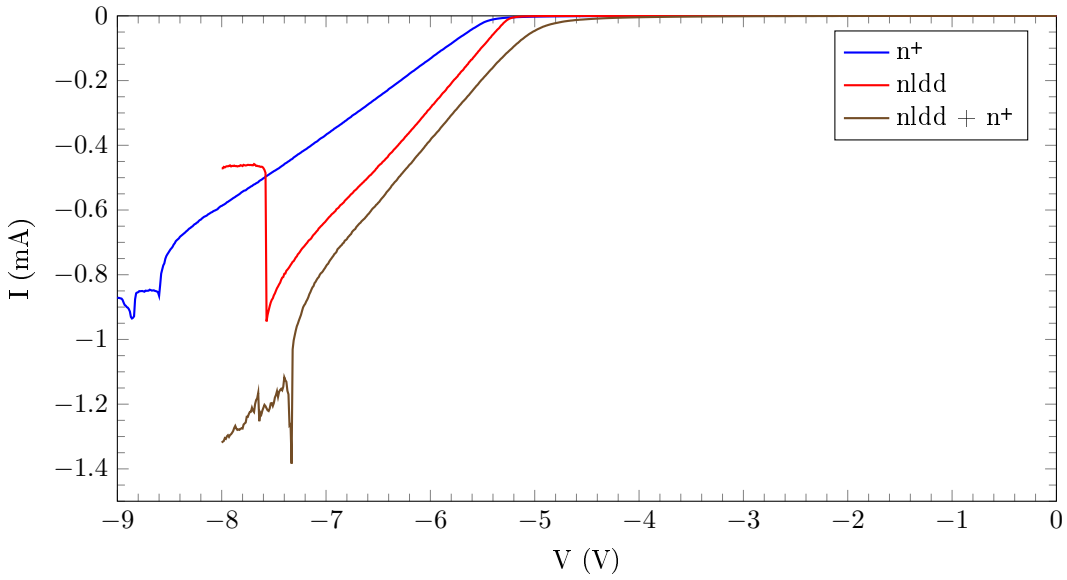


Figure 3.10: Reverse bias V-I characteristics of Zener diodes with different cathode implantations. For all cases W = 0.25 µm, L = 0.5 µm and M = 0.25 µm.

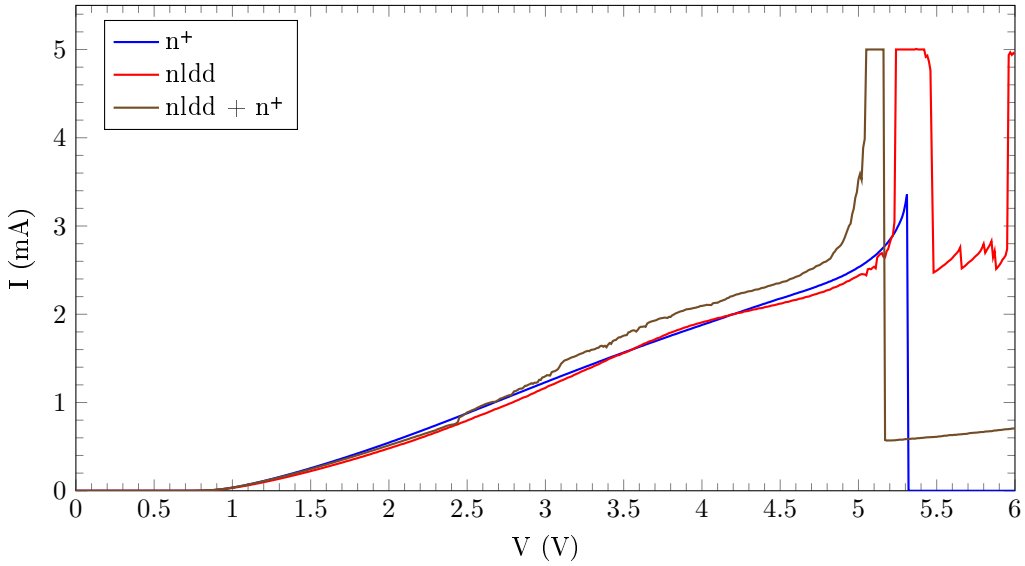


Figure 3.11: Forward bias V-I characteristics of Zener diodes with different cathode implantations. For all cases W = 0.25 µm, L = 0.5 µm and M = 0.25 µm.

3.2.6 Discussion of the Zener Diodes

For the target application of OTP memory, the Zener diode should change characteristics after "programming" by means of a current pulse. Diodes wider than 0.5 µm consistently entered a high-conduction state in forward bias when an appropriate current compliance was set. When the diode did not burn out, the diode characteristic was replaced by a linear 500 Ω characteristic. A large difference in characteristic is then obtained which is suitable for OTP memory.

To understand the effects leading to a breakdown event, the characteristics of the 0.8 µm wide diode were analyzed. The curve sections A-F are defined in Figure 3.12.

A Exponential diode behavior.

B Diode series resistance dominates, linearizing the curve. Little effects of heating are detected.

C Differential resistance increases as defined by the slope of the curve. This implies a positive differential resistance temperature coefficient (RTC) for the total diode, as heating is the primary changing factor in the setup. The diode barrier-voltage decreases for higher temperatures so only an increase in polysilicon sheet resistance fits the phenomenon.

D The stage before abrupt breakdown is a decrease in differential resistance. The average temperature in the diode will be higher than in the previous curve segment, implying the RTC to turn negative. However, no thermal runaway occurs and no damage to the device was observed when the measurement was repeated. The existence of a temperature gradient over the diode length (and width) in combination with a temperature-resistance curve that exhibits both positive and negative slopes could explain this. The outer parts of the diode are cooler and therefore have a positive RTC and the center region would be hot enough to exhibit negative RTC.

E At this voltage, sufficient polysilicon area has a negative RTC to create thermal runaway. Breakdown occurs and the current either drops significantly or clamps up to the current limit of the measurement setup. Diodes wider than 0.5 µm generally transitioned towards a high-current state and thinner diodes towards a low-current state. When the applied voltage was removed in either situation, a low-ohmic, respectively high-ohmic resistance had permanently replaced the diode. Resistances as low as 500 Ω and as high as 100 MΩ were observed. A silicide melt channel through the device, shorting the anode and cathode, matches the low-ohmic finding. Electromigration would drive this effect, having both high current density and elevated temperature present as required for this process. Furthermore, it is possible that the doping of the anode and cathode diffuse into a single resistor by the elevated temperature.

When a high current is maintained for long duration, burn-out occurs, melting the polysilicon junction region partially or entirely. The duration of the high-current state before transitioning to a high-resistance burn-out state strongly relates to the diode width. Logically, the narrower devices pass the high-current state E too, but are not registered by the parameter analyzer as only stable read points are saved. Lowering the current limit did not result in any measurable high-current state for the thinner diodes.

F After a partial burn-out occurred, the remaining diode structure breaks down again at a higher voltage, similar to a thinner diode.

In reverse bias, a similar high-current state was observed for the 1 µm wide diode in the plot of Figure 3.4. Therefore, it can be assumed that a similar breakdown effect occurs in reverse bias.

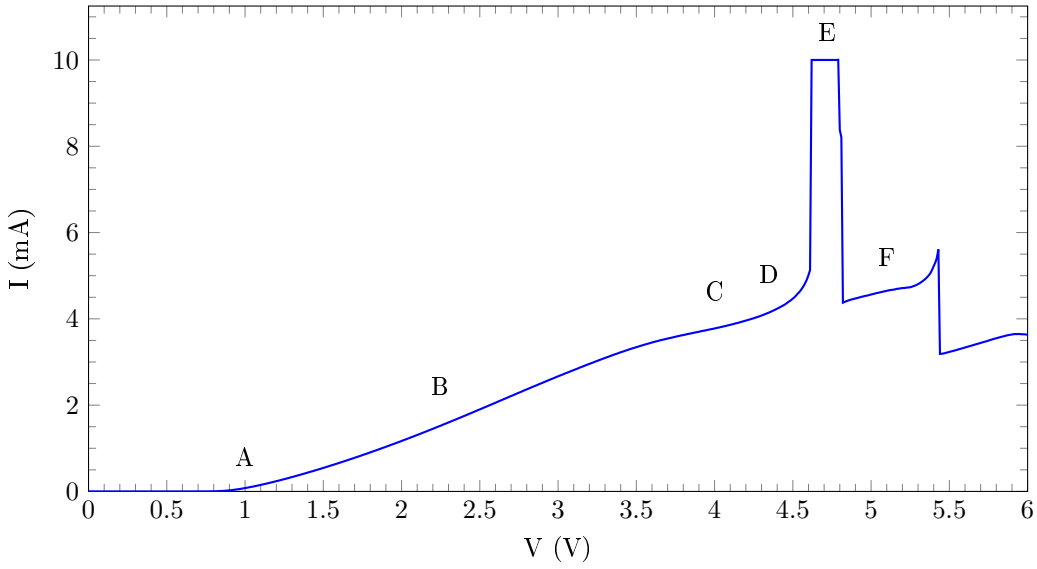


Figure 3.12: Forward bias V-I characteristic with labels to indicate curve sections of a Zener diode with W = 0.8 µm, L = 0.5 µm and M = 0.25 µm.

3.3 Current Pulse Tests on the Zener Diodes

In practice, a current pulse with fixed duration will be applied to alter the diode characteristics and thus "write" the OTP memory bit. Applying a voltage pulse would generate an

excessively high current after breakdown, causing burn-out in the diode shortly after. As the voltage sweep only measures steady-state situations, a time-based test was performed to ensure the programming time specification mentioned in Section 2.2.2 was met.

The Agilent HP 4155A semiconductor parameter analyzer can generate current pulses down to 500 µs. A minimum pulse duration of 500 µs is chosen. The pulse current is varied in order to find the range of acceptable currents. Ideally, a large range of currents generate the low-ohmic resistance as this indicates more reliable breakdown.

To evaluate the outcome of each current pulse, the forward biased I-V characteristic is inspected. When the pulse current was too low, the curve remained unaltered. For properly valued pulse currents, a low resistance was measured. Finally, too high currents would generate diode burn-out, creating a high-resistance path or open circuit. Only when the diode characteristic did not change at all, the diode was re-used.

3.3.1 Forward Biased Current Pulse Tests on the Zener Diodes

Table 3.2 lists the results of the forward biased tests on Zener diodes with different widths. The breakdown current and burn-out current are lower for thinner diodes. However, the difference between the breakdown current and burn-out current then decreases.

Table 3.2: Results of 500 µs forward biased current pulse tests on diodes with L = 0.5 µm, M = 0.25 µm and varying W. Evaluated by the resistance R_b obtained from the forward characteristic after the pulse. "No change" indicates an exponential forward characteristic, implying breakdown did not occur.

Diode width W (µm)	Current (mA)	R_b (kΩ)
1	9	no change
1	10	0.727
0.9	8	0.511
0.8	8	0.411
0.7	8	0.791
0.6	6	no change
0.6	7	0.459
0.6	10	open
0.5	6	1.303
0.5	8	open
0.45	6	open
0.4	4	no change
0.4	6	open
0.35	4.75	no change
0.35	5	open
0.3	6	1.641
0.25	6	open

3.3.2 Reverse Biased Current Pulse Tests on the Zener Diodes

The same current pulse test was performed in reverse bias. Only the diode with L = 10 µm with silicide closer to the junction achieved highly repeatable results. The results for this diode are listed in Table 3.3. The required current is significantly lower for this diode than for the wide diodes in forward bias. However, a higher compliance voltage was required as predicted by the characteristics found in Section 3.2.

Table 3.3: Results for 500 µs reverse biased current pulse tests on the diode with L = 10 µm and silicide closer to the junction. Evaluated by the resistance R_b obtained from the forward characteristic after the pulse. "No change" indicates an exponential forward characteristic, implying no second breakdown occurred.

Current (mA)	R_b (kΩ)
10	0.395
5	0.423
1	0.701
0.8	0.790
0.7	0.980
0.6	no change

3.3.3 Analysis of the Current Pulse on the Zener Diodes

The forward biased 10 mA, 500 µs current pulse from Table 3.2 was measured with an oscilloscope and plotted in Figure 3.13. The rise time of the current pulse is significantly longer than the hard breakdown at 165 µs lasts. When 5 V is reached, the voltage decreases with increasing current, indicating a negative resistance. No negative-sloped curve segment appears in the parameter analyzer plots in forward bias so the negative resistance was presumed to be a dynamic and unstable effect due to heating.

At the falling edge of the current pulse, the voltage increases. When re-applying the current pulse, a similar phenomenon is observed at the rising edge as well. This cannot be caused by inductance in the test setup as the voltage would decrease instead of increase at the falling edge. Furthermore, the peaks were not observed in all tests, which should be the case for a high-inductive test setup.

The instantaneous diode resistance at the middle of the high-current pulse is approximately half the resistance measured at low voltages. Together with the peaks at the pulse flanges, this suggests a high-conductive mode of operation similar to the second breakdown in reverse bias. The resistance measured at low voltages changed when applying more current pulses, indicating that destructive breakdown also occurs outside the short initial breakdown such as at 165 µs in Figure 3.13. Generally, the resistance increased when more pulses were applied.

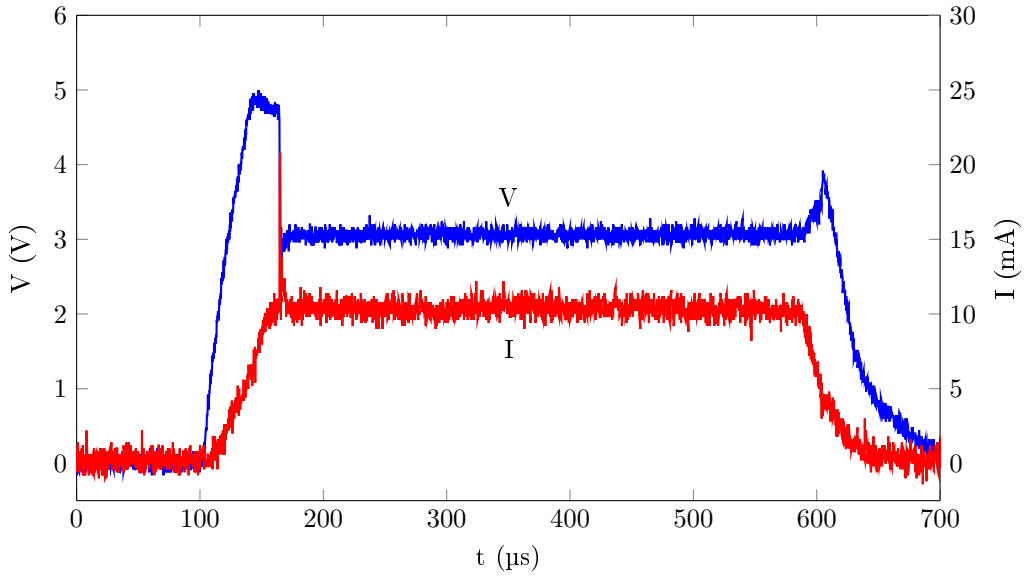


Figure 3.13: Forward breakdown of Zener diode with W = 1 µm, L = 0.5 µm and M = 0.25 µm when applying a 10 mA, 500 µs current pulse. At the breakdown point at 165 µs, a 20 mA current spike occurs for just under 1 µs.

3.4 Conclusion on the Zener Diodes

Breakdown was found in all measured diode variants and the voltage and current at breakdown strongly correlate with the varied parameters. The ideal diode for the target application transforms into low-ohmic resistor at a breakdown voltage between 2.5 V and 5 V at a low current. Wide diodes in forward bias comply, although the current is relatively high. In reverse bias, only the variant with L = 10 µm and extended silicide complied, except for the second breakdown voltage requirement. To solve this, methods for lowering the second breakdown voltage and high-voltage read/write circuitry were further researched.

The wide diode and long, silicidized diode were further improved and implemented in OTP circuitry. By observing the effects of parameter variation, insights were obtained to improve the two diode geometries. Both benefit from silicide closer to the junction as it reduces the series resistance and thus the breakdown voltage. By decreasing the p- region length M and adding nldd to the cathode region, the series resistance is decreased further.

The breakdown was presumably caused by thermal runaway, creating a low-ohmic connection through the device. Either silicide was expected to short the junction or the anode and cathode dopant atoms diffuse into a single resistor.

Chapter 4

Improved Zener Diodes

The Zener diodes from the first iteration had promising characteristics for implementing OTP memory. Wider diode structures were effective for forward biased programming and long, silicidized diodes for reverse biased programming. However, these diodes had to be improved in terms of breakdown current and voltage to meet the specifications. The second iteration of Zener diodes is described in this chapter and was fabricated in the second production cycle.

DC measurement results of the improved Zener diodes are presented and discussed in this chapter. Furthermore, current pulse tests are performed and discussed. Cross-sections and (S)TEM were performed on Zener diodes after breakdown to identify the cause of the low-ohmic connection.

4.1 Structure of the Improved Zener Diodes

Two primary types of diode geometry were designed: a wide, short diode and a thin, long diode. The wide type proved effective for forward biased programming and the thin type for reverse biased programming.

For both types, the series resistance had to be decreased to reduce the programming voltage. This was done by adding silicide closer to the junction and shortening the high-resistance p^- middle region. The amount of vias connecting to the first metal layer was reduced to fit the programming current.

The structure and renewed geometric parameters of the improved Zener diode are given in Figure 4.1. Compared to the parameters varied in the first iteration, a parameter was introduced; the distance between the silicide and the junction S. Parameter L changed to the silicide region length. Long Zener diodes were folded up to better fit in the OTP memory circuit layout.

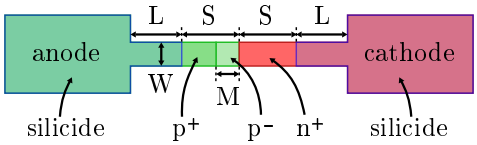


Figure 4.1: Top view of the improved Zener diode structure with renewed parameters.

4.2 Varied Parameters of the Improved Zener Diodes

OTP flipflop shift registers were implemented for the second production cycle. These shift registers enable testing a large amount of Zener diodes on a relatively small amount of die area. Therefore, combinations of parameter variations were created. As a disadvantage, the tests turn binary because programming can only be successful or unsuccessful. To also measure V-I characteristics and exact breakdown voltages, individually connected diodes were also implemented. A selection of the diodes implemented in the OTP memory circuits were measured this way to benchmark the OTP memory tests.

The new parameter S, the distance between the junction and the silicide, was valued approximately 1 µm in the wide diode reference, see Figure 3.1. Smaller values are beneficial for lowering the breakdown voltage, so S was varied between 0.3 µm and 1 µm. Table 4.1 lists the parameter values, where all combinations of parameters were implemented in the OTP circuit. Additionally, every device was also created with n-type lightly doped drain (nldd) implantation on top of the n^+ implantation in the cathode region.

Table 4.1: Varied parameters of the Zener diode for forward breakdown. All combinations are created in OTP memory circuits twice, yielding 150 variants.

Parameter	Value (µm)				
Silicidized length (L)	0.15				
Width (W)	0.25	0.4	0.6	0.8	1
Middle p^- length (M)	0	0.15	0.25		
Silicide-junction distance (S)	0.3	0.4	0.6	0.8	1

Parameter S is also added for the long, thin Zener diode. As the reference diode for these variations had 0.5 µm distance to the p^- region it is chosen as maximum S.

Table 4.2: Varied parameters of the Zener diode for reverse breakdown. All combinations are created in OTP memory circuits twice, yielding 216 variants.

Parameter	Value (µm)					
Silicidized length (L)	0.15	0.5	1	2	4	8
Width (W)	0.25	0.6				
Middle p^- length (M)	0	0.15	0.25			
Silicide-junction distance (S)	0.3	0.4	0.5			

4.3 DC Measurements of the Improved Zener Diodes

A voltage sweep was applied to the Zener diodes with an Agilent HP 4155A semiconductor parameter analyzer at wafer level using probing needles. These measurements were performed to determine the breakdown voltage and the minimum required current for breakdown. At breakdown, a large current was typically pulsed into the diode by the parameter analyzer, disrupting the measurement. Therefore, any curve segment after the breakdown event is uncontrolled and not representative of the device characteristics after breakdown. The last stable read-point before the breakdown event only describes a lower boundary

to the minimum programming voltage and current. This is a limitation of the DC measurement setup that was solved in the current pulse measurement setup of Section 9.4. In Section 9.4, the actual minimum programming current for current pulses of a set duration are determined.

The breakdown voltage, current and power specifications for a selection of the improved Zener diodes are listed in Appendix A.

4.3.1 The Effect of the Silicide-Junction Distance on the Characteristics of the Improved Zener Diodes

The V-I characteristics of Zener diodes with different silicide-junction distances S are plotted in Figures 4.2 and 4.3 for forward and reverse bias. In both biases, the breakdown voltage decreases as a result of the decreasing series resistance. For S below 0.4 µm (and sometimes even for S below 0.5 µm), the diode shows a considerable leakage current even before applying a current pulse. These diodes cannot be used to implement an OTP memory as the leakage current may trigger the read-out circuitry to falsely obtain a "1".

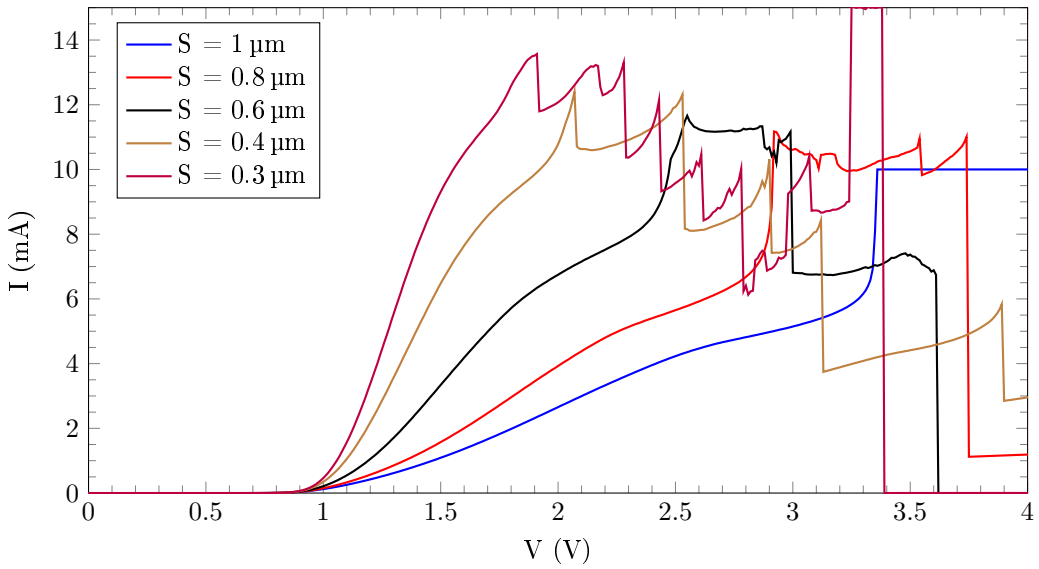


Figure 4.2: Forward bias V-I characteristics of Zener diodes with different silicide-junction distances. For all cases W = 1 µm, M = 0.25 µm and L = 0.15 µm.

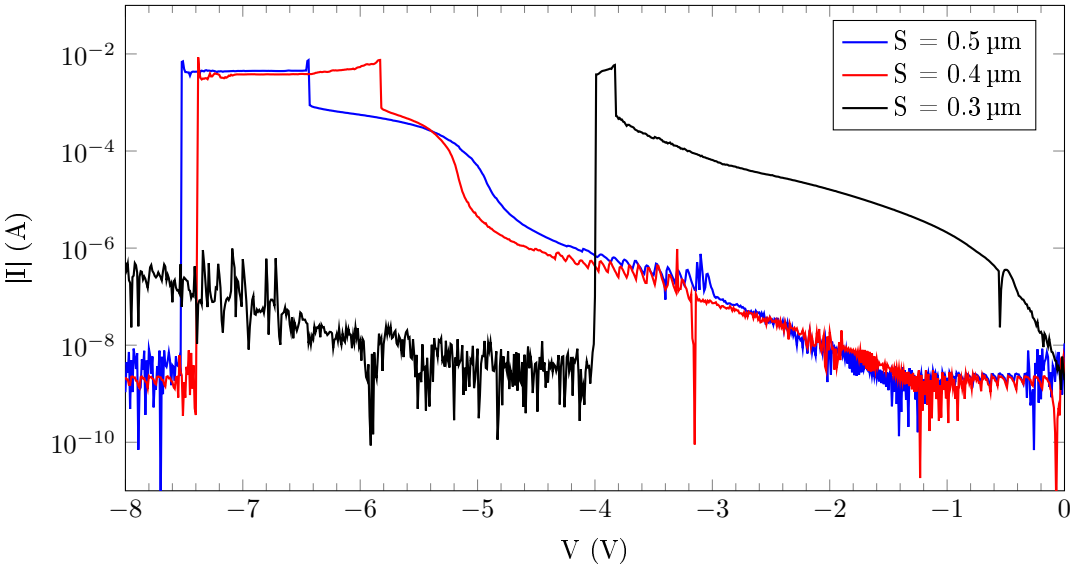


Figure 4.3: Reverse bias V-I characteristics of Zener diodes with different silicide-junction distances. For all cases W = 0.25 µm, M = 0.25 µm and L = 8 µm.

4.3.2 The Effect of the Silicidized Length on the Characteristics of the Improved Zener Diodes

The measurement results for forward bias are listed in Table 4.3. Larger values of L increase the forward breakdown voltage while keeping the required current constant. This can be explained by the increase of series resistance by the silicidized regions outweighing the thermal benefits that were aimed for. The resistance lowers the voltage drop over the actual diode and therefore a higher voltage over the diode terminals is required.

In reverse bias, no correlation between L and breakdown current or voltage was found. Reverse breakdown generates heat primarily at the junction with little benefits of large L. Furthermore, the reverse breakdown current is significantly lower than the forward breakdown current. Series resistance then influences the breakdown voltage less.

Table 4.3: Last stable measurement point before forward breakdown Zener diodes with different L. For all cases W = 0.25 µm, M = 0.25 µm and S = 0.5 µm.

L	0.15 µm	0.5 µm	1 µm	2 µm	4 µm	8 µm
V_{BD} (V)	2.83	2.72	2.84	2.97	3.45	4.08
I_{BD} (mA)	5.05	4.57	4.71	4.70	4.89	4.87

4.3.3 The Effect of the Middle p- Region Length on the Characteristics of the Improved Zener Diodes

The middle p- region length M does not significantly change the forward characteristic of the Zener diode. In reverse bias, more leakage is observed for diodes with smaller values of M, see Figure 4.4. However, no appreciable changes in second breakdown voltage were observed. A low leakage is favorable for the OTP memory application to achieve a more distinct characteristic change by programming the memory bit, so M = 0.25 µm is preferred.

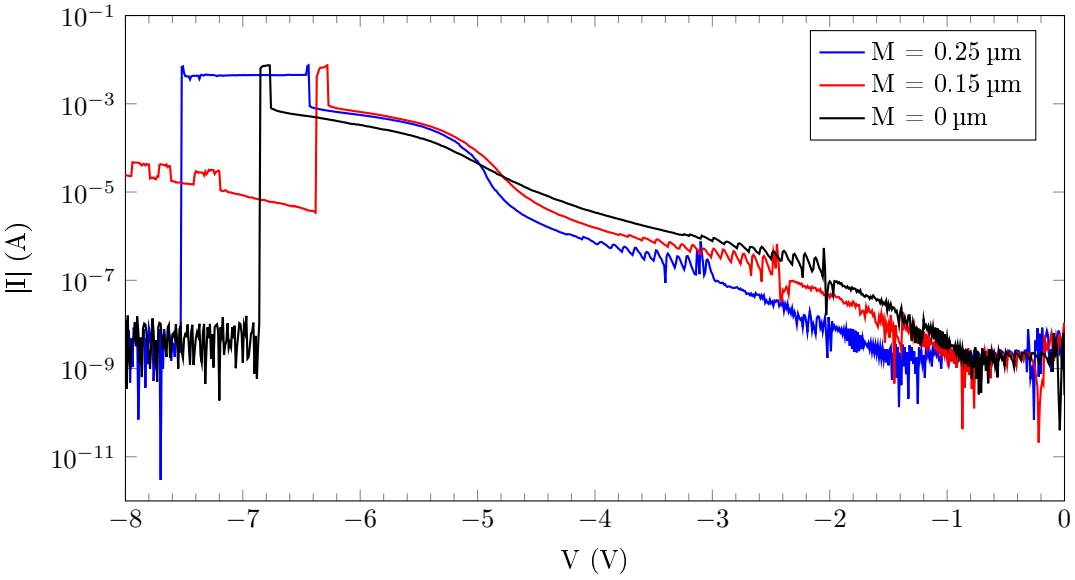


Figure 4.4: Reverse bias V-I characteristics of Zener diodes with different value of M. For all cases W = 0.25 µm, S = 0.5 µm and L = 8 µm.

4.3.4 The Effect of the Cathode Implantation on the Characteristics of the Improved Zener Diodes

The cathode of the Zener diode consists of the shallow CMOS source/drain n^+ implantation, possibly complemented by an n-type lightly doped drain (nldd) implantation. Diodes with nldd had a lower breakdown voltage at a higher current in forward bias, see Table 4.4. In reverse bias, the breakdown current remains similar but the voltage decreases for Zener diodes with nldd.

Table 4.4: Last stable measurement point before breakdown of Zener diodes with different cathode implantations. For all cases W = 0.25 µm, L = 8 µm, M = 0.25 µm and S = 0.5 µm.

	Forward bias			Reverse bias		
Cathode	V_{BD} (V)	I_{BD} (mA)	P_{BD} (mW)	V_{BD} (V)	I_{BD} (mA)	P_{BD} (mW)
n^+	4.04	4.48	18.1	-6.68	-0.89	5.94
n^+, nldd	3.84	4.73	18.1	-6.43	-0.88	5.65

4.3.5 Discussion of the Improved Zener Diodes

The silicide-junction distance S is the most effective parameter to change the forward and reverse breakdown voltage. However, a minimum value of 0.5 µm should be kept to prevent considerable leakage current. The effect of the middle p^- region length M on the breakdown voltage that was observed in Section 3.2.3 was primarily due to the change in silicide-junction distance that was implicitly introduced. Furthermore, both forward and reverse breakdown voltages decrease by increasing diode width.

- In forward bias
  - the minimum breakdown voltage is obtained for large W, small L, small S and nldd added to the cathode. With W = 0.5 µm, L = 0.15 µm, S = 0.5 µm, M = 0.25 µm and nldd added to the cathode, the breakdown voltage is 2.46 V and breakdown current at least 7.04 mA.
  - the minimum breakdown current is obtained for small W, small L, large S and no nldd added to the cathode. With W = 0.25 µm, L = 0.15 µm, S = 0.5 µm, M = 0.25 µm and no nldd added to the cathode, the breakdown voltage is 2.81 V and breakdown current at least 3.96 mA.
- In reverse bias
  - the minimum breakdown voltage is obtained for large W and nldd added to the cathode. With W = 1 µm, L = 0.15 µm, S = 0.6 µm, M = 0 µm and nldd added to the cathode, the breakdown voltage is 5.89 V and breakdown current at least 1.88 mA.
  - the minimum breakdown current is obtained for small W. With W = 0.25 µm, L = 8 µm, S = 0.5 µm, M = 0 µm and nldd added to the cathode, the breakdown voltage is 6.76 V and breakdown current at least 0.81 mA.

In Section 2.2.2, a maximum breakdown voltage of 5 V was specified. This is only achievable in forward bias.

4.4 Current Pulse Tests on the Improved Zener Diodes

In order to find out what creates the low-ohmic connection in the Zener diodes after breakdown, cross-sections and TEM/STEM were performed. The samples are prepared by means of a 10 µs current pulse. The current pulse setup is first described, then the changes in diode characteristic are discussed for both forward and reverse bias. The forward biased programmed Zener diode is then examined with cross-sections and (S)TEM.

4.4.1 Current Pulse Test Setup for the Improved Zener Diodes

A schematic view of the test board is given in Figure 4.5. The Zener diode is contacted with DC probe needles and is depicted in the schematic as the device under test (DUT).

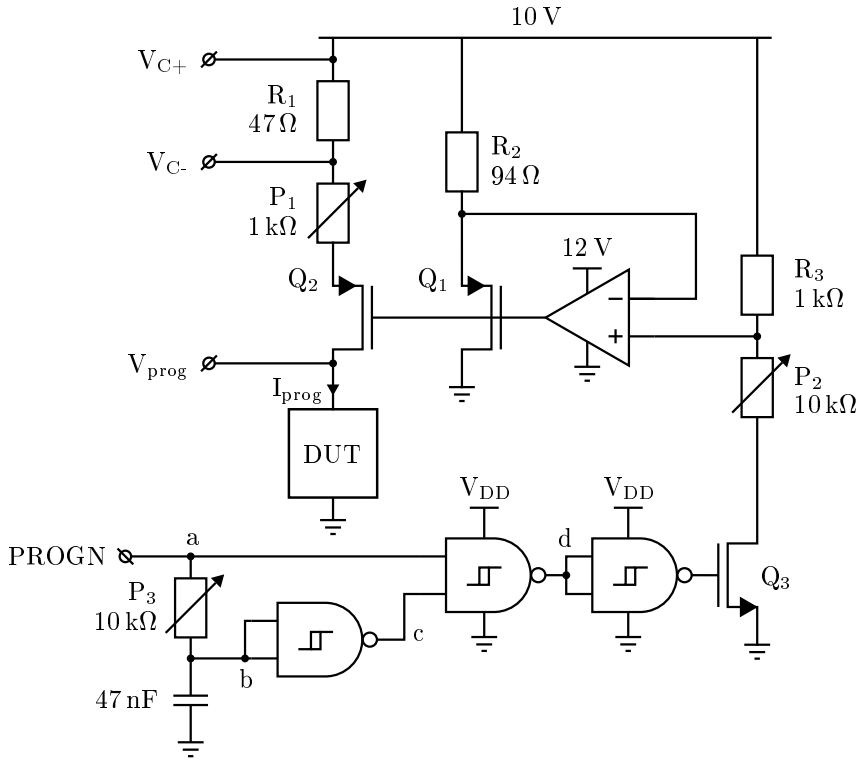


Figure 4.5: Schematic view of the test setup, the DUT depicts either a Zener diode in forward or reverse bias.

By creating a delayed signal with the RC filter, a short pulse is created with the two NAND Schmitt triggers at a rising edge of the digital 2.5 V PROGN input signal. The pulse length can then be selected by trimming P_3. Figure 4.6 illustrates the subcircuit with voltages at the intermediate nodes. An oscilloscope is used to trim the pulse length to 10 µs.

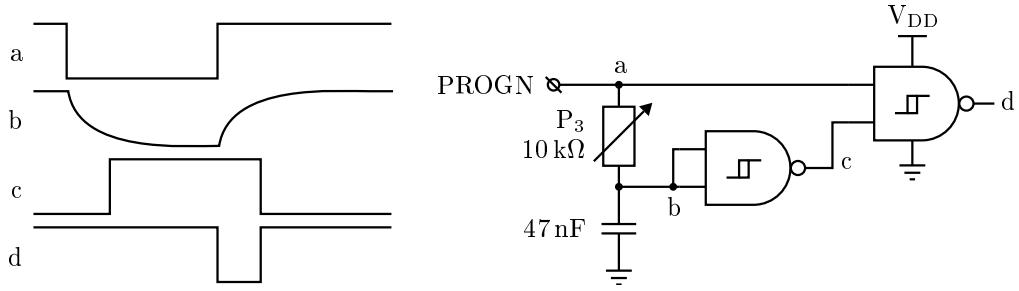


Figure 4.6: Creating a short pulse with two NAND Schmitt triggers and an RC filter. The intermediate nodes are marked on the right and correspond to the signals on the left.

The current through the DUT is limited to a selectable current limit by the parallel, identical PMOST pair Q_1 and Q_2 and the opamp. Q_1 is biased by the opamp for a drain current around 10 mA by setting the non-inverting input of the opamp at 9 V. This is done by trimming P_2 while manually keeping the gate of Q_3 at 2.5 V. Since the drain of Q_1 is grounded, a maximum for the drain current of Q_2 is also set and can be linearly scaled with P_1. When trimming, the DUT connection V_{prog} is shorted to ground to generate the

maximum current. The current limit can then be read-out as I_{lim} = (V_{C+} - V_{C-}) / 47 Ω.

About 2 V is required over Q_2 and the series resistances R_1 and P_1 before the current limit is reached, see Figure 4.7. Therefore, at least 2 V headroom is required for V_{supply} above the breakdown voltage of the Zener diode.

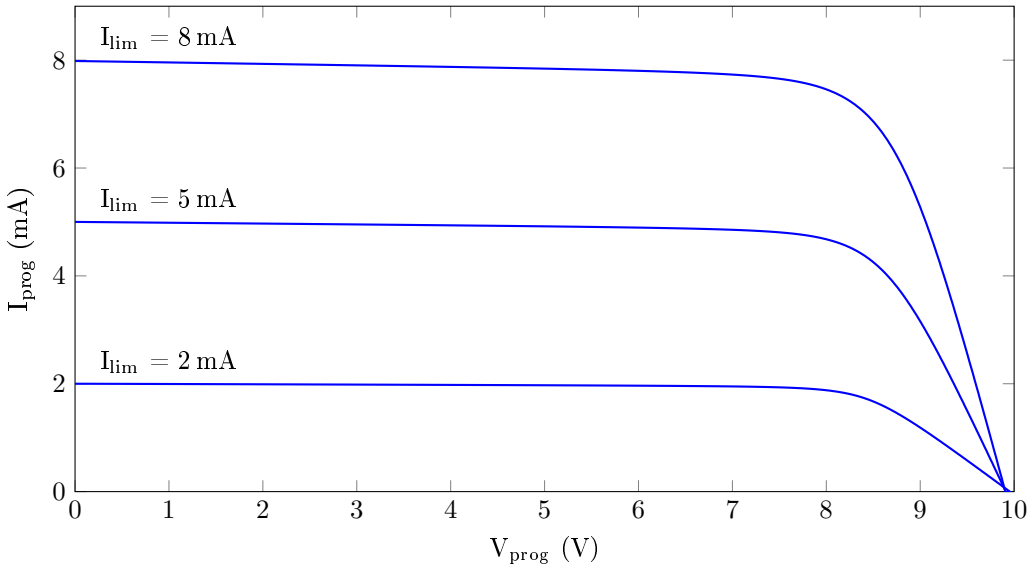


Figure 4.7: V-I characteristics of Figure 4.5 when tuned to different values of I_{lim}.

4.4.2 Reverse Biased Current Pulse Tests on the Improved Zener Diodes

Reverse breakdown was observed to be around 1 mA for all Zener diodes with W = 0.25 µm in Section 4.3. This was measured with long-term applied signals. However, 10 µs, 2 mA did not change the diode characteristic of such device. The 5 mA current pulse of Figure 4.8 does significantly change the diode characteristics, but not as severely as with the forward biased current pulses. The diode characteristics before and after the current pulse are plotted in Figure 4.9. Similar tests resulted in leakage currents up to 1 mA at V = −2.5 V and were generally strongly non-linear.

The transients on the voltage signals from Figure 4.8 are typical for Zener diodes as the reverse breakdown voltage has a positive temperature coefficient. The current limit is then reached and the voltage drops significantly which makes the diode leave breakdown regime and cool down. The voltage then increases again, which then again triggers the breakdown or stabilizes. The parasitic inductance in the test setup increases the oscillation effect.

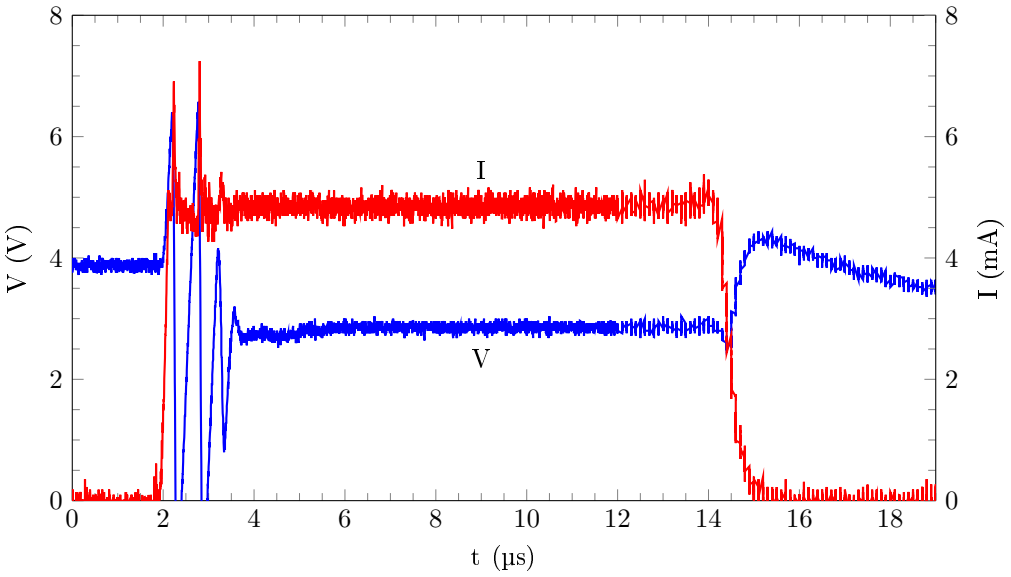


Figure 4.8: Reverse biased 5 mA current pulse through a Zener diode with W = 0.25 µm, L = 0.15 µm, M = 0.25 µm and S = 0.5 µm.

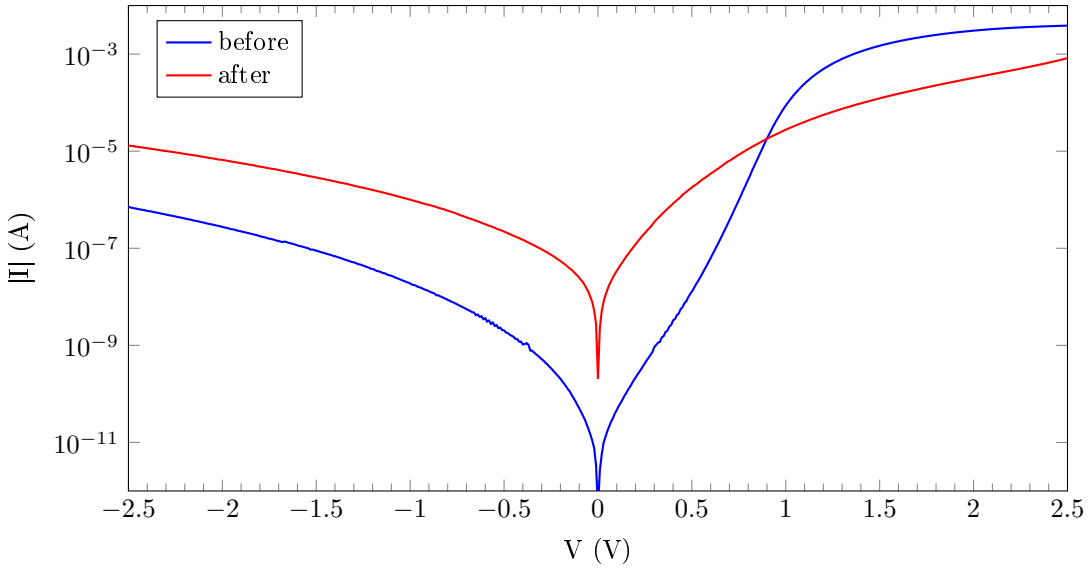


Figure 4.9: Characteristics of Zener diode with W = 0.25 µm, L = 0.15 µm, M = 0.25 µm and S = 0.5 µm before and after the 5 mA current pulse of Figure 4.8.

4.4.3 Forward Biased Current Pulse Tests on the Improved Zener Diodes

The forward biased current pulse tests were performed on diodes with W = 0.25 µm, L = 0.15 µm, M = 0.25 µm and S = 0.5 µm. These diodes were found to be stable up to 5.05 mA at 2.83 V in Section 4.3. The 10 µs, 8 mA current pulse from Figure 4.10 was applied which changed the diode characteristic to a linear 1 kΩ characteristic. The transients on the signals are presumably caused by inductance in the test setup. The characteristics before and after

the current pulse are plotted in Figure 4.11. Only the range [-1, 1] V was measured for the diode after breakdown to prevent burn-out.

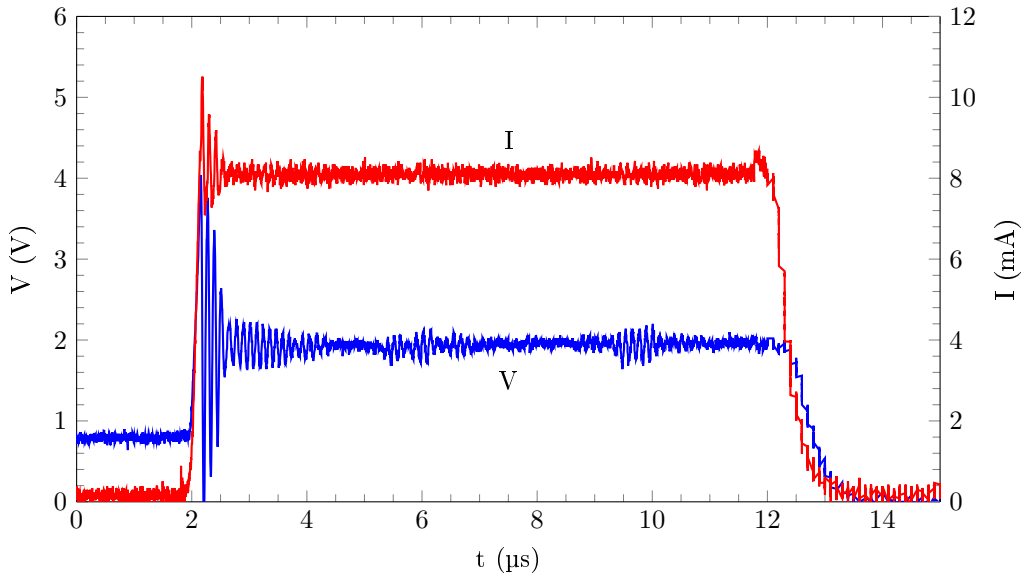


Figure 4.10: Forward biased 8 mA current pulse through a Zener diode with W = 0.25 µm, L = 0.15 µm, M = 0.25 µm and S = 0.5 µm.

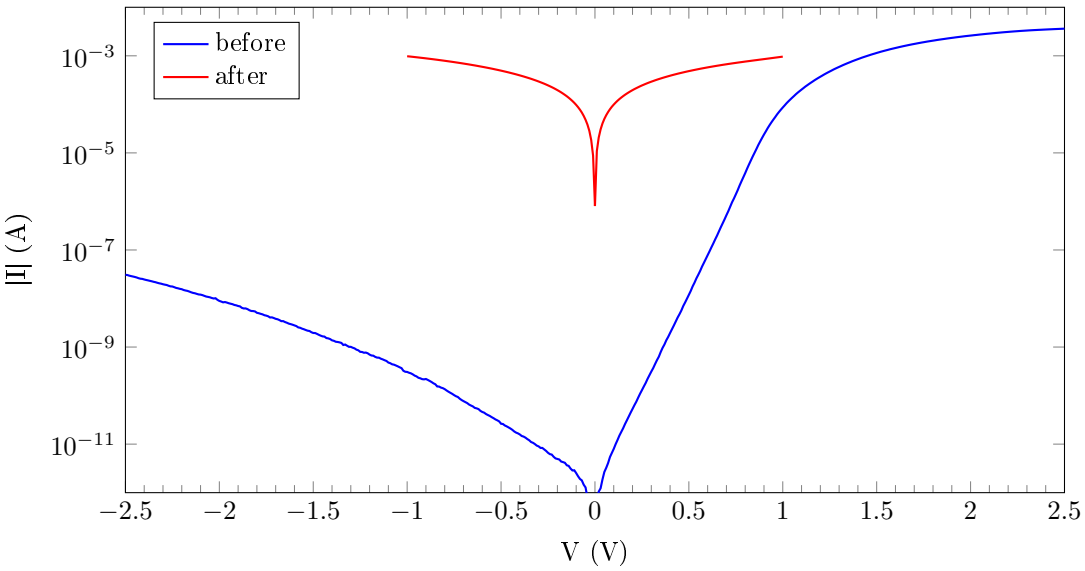


Figure 4.11: Characteristics of a Zener diode with W = 0.25 µm, L = 0.15 µm, M = 0.25 µm and S = 0.5 µm before and after the forward biased 8 mA current pulse of Figure 4.10.

FIB Cross-Sections and TEM/STEM of Zener Diodes After Breakdown

A Focused Ion Beam (FIB) cross-section was performed on a forward biased programmed Zener diode. The Zener diode was identical to the diode from Figure 4.11 before programming. The characteristics changed to a 500 Ω resistance after a current pulse similar to

the current pulse from Figure 4.10 was applied. Cross-sections were performed about every 50 nm along the diode width and images were captured with a Scanning Electron Microscope (SEM) for every slice. The orientation of the cross-sections are illustrated in Figure 4.12. The images are depicted in Figure 4.13 and conclude that the anode silicide migrated towards the junction in the center of the diode. The location of this effect was expected as the center has the least heat sinking.

Halfway through the diode while performing the cross-sections, the ion beam was "digging" in front of the diode instead of on the cross-section face. Charged particles that were removed in the process attached to the diode structure as depicted in Figure 4.14. Presumably, a charging effect on these particles makes them visible in the SEM image. The difference between the anode and cathode suggests a change in polysilicon composition or grain size. When the melting temperature of silicon is locally approached, the silicon atoms become mobile and may leave the crystal structure. Amorphous or small-grain polysilicon may then be obtained, which would explain the observed phenomenon.

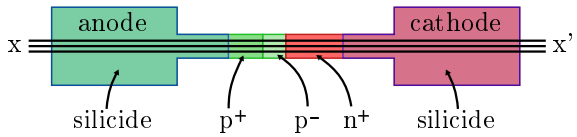


Figure 4.12: Cross-sections are along the Zener length x-x' and successive images are captured long the diode width, three example cross-sections are illustrated with horizontal lines.

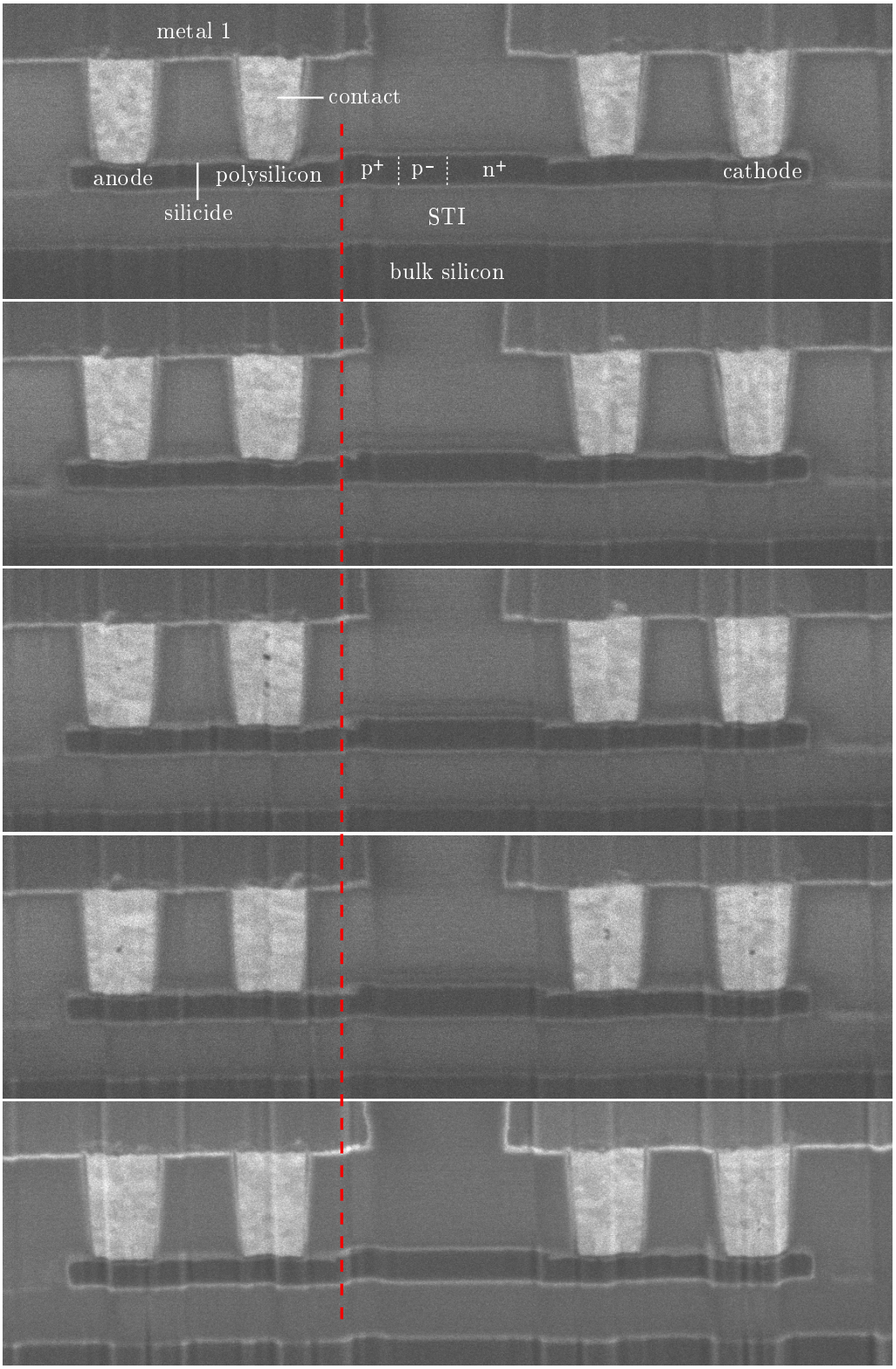


Figure 4.13: FIB cross-sections about every 50 nm of a Zener diode that was transformed into a 500 Ω resistance with a current pulse similar to Figure 4.10. The dashed red line is the presumed initial silicide edge.

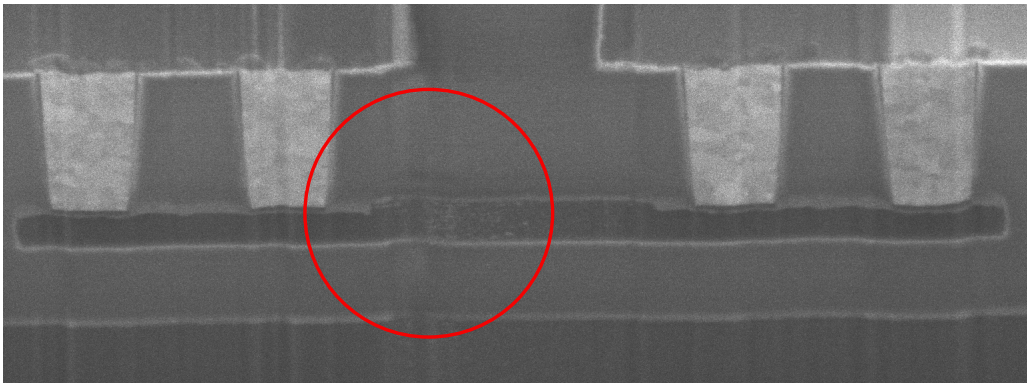
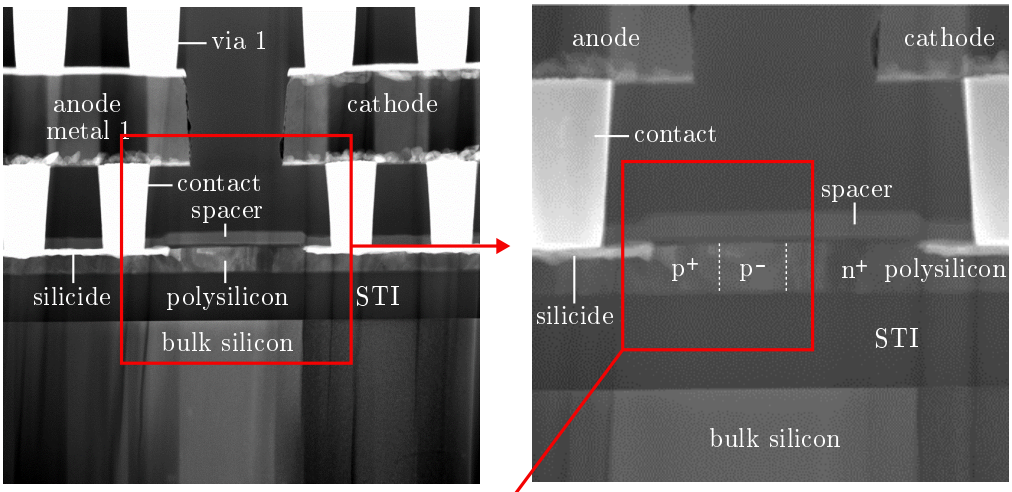


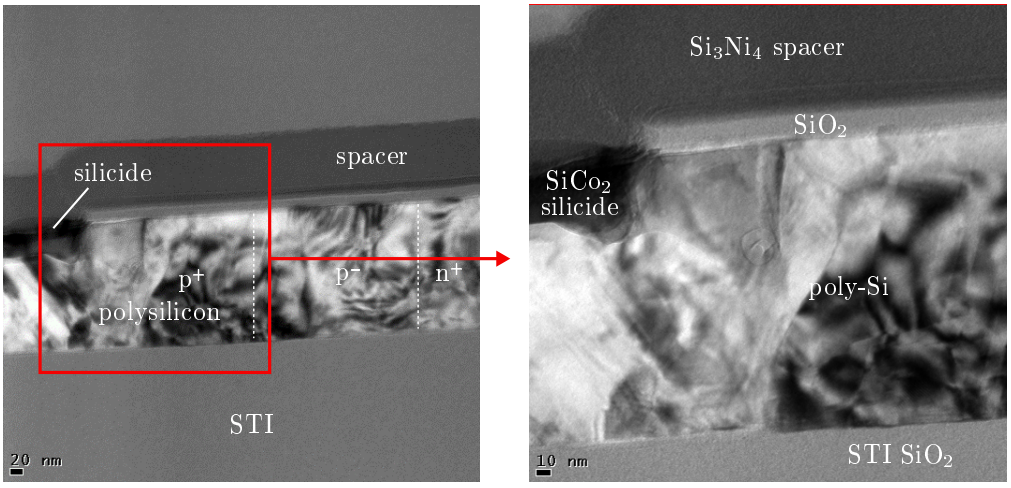
Figure 4.14: Charged loose particles from FIB operation in front of the cross-sectional front plane attach to anode region, suggesting that the anode polysilicon structure changed.

The (Scanning) Transmission Electron Microscope ((S)TEM) images of Figure 4.15 indicate that the current pulse from Figure 4.10 heats up the diode sufficiently to create feathering on the silicide and diffusion of As dopant atoms from the cathode. Ti and As have equal colors in the STEM EDX image from Figure 4.15f but a split-out indicates only As. The silicide and As dopant atoms bridge the entire anode and therefore short the junction. This matches the low-ohmic linear characteristics that were obtained for this device. The fan-out of the silicide and the As dopant atoms meet close to the original silicide location which indicates that mainly the As causes the breakdown effect.



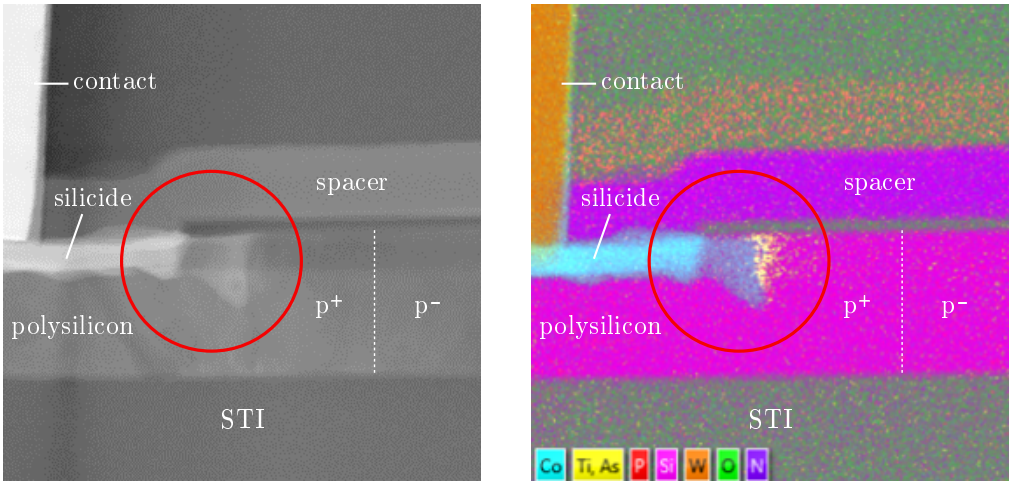
(a) TEM image with specification of parts.

(b)



(c)

(d) TEM close-up of the silicide feathering.



(e) STEM mass contrast image.

(f) STEM EDX image indicates that silicide and As dopant atoms have moved.

Figure 4.15: TEM/STEM images of the diode with characteristics from Figure 4.11 after applying the programming current pulse from Figure 4.10. The anode silicide and the cathode As dopant atoms bridge the anode and short the junction. Red square indicates zoom/location of next image.

4.5 Conclusion of the Improved Zener Diodes

A large improvement was observed for the second iteration of the Zener diodes in terms of breakdown voltage. For 0.25 µm wide diodes the forward breakdown voltage decreased from 5.3 V to 2.8 V. The required power remains around 15 mW. The distance between the silicide and the junction S was found to be the key parameter in defining the voltage and therefore also the current.

In Chapter 3 it was found that wider diodes are beneficial to create the low-ohmic connection after forward breakdown. However, current pulse tests with the setup from Section 4.4.1 proved that 0.25 µm wide diodes are also suitable. The applied current pulses from Section 3.3 generated high-current peaks at breakdown which disrupted the test and burned 0.25 µm wide diodes out. Thin diodes break down at a lower current and still comply with the 5 V maximum breakdown voltage and are therefore preferred.

Reverse biased current pulse tests disproved that relatively low breakdown currents can be achieved. Over 2 mA is required to reliably change the characteristics of the measured Zener diodes. Furthermore, the change in characteristics is more drastic for the diodes after a forward breakdown event. Instead of the low-ohmic linear connection, a non-linear leakage occurs after a reverse breakdown event which matches junction defects.

The specifications listed in Section 2.2.2 included a maximum breakdown voltage of 5 V. Both first and second iteration Zener diodes do not comply with this maximum reverse breakdown voltage. The reverse breakdown current benefit is not large enough to outweigh the reverse breakdown voltage non-compliance. Therefore, forward biased breakdown is preferred for the fabricated Zener diodes for the target application OTP memory. In forward bias the minimum breakdown current is obtained for Zener diodes with small W, small L, large S and no nldd added to the cathode. With W = 0.25 µm, L = 0.15 µm, S = 0.5 µm, M = 0.25 µm and no nldd added to the cathode, the breakdown voltage is 2.81 V and breakdown current at least 3.96 mA. This diode obtains a 1 kΩ linear characteristic after a 10 µs, 8 mA current pulse is applied.

TEM/STEM images were made to observe the physical effects of forward breakdown in the Zener diodes. Both silicide and cathode n^+ dopant atoms migrate into the p^+ anode and short the junction. These observations fit the reproducible low-ohmic connection between anode and cathode.

Chapter 5

Junction Field-Effect Transistors

JFETs were proposed as a transistor cascode in the high-voltage digital signal drivers presented in Section 2.3. In this chapter, the working principle of JFETs is explained and used to select suitable layers and structures. Layout parameters in these structures are varied and their aimed effects on the characteristics are described. The measurement results are then elaborated.

5.1 Working Principle of the JFET

The JFET controls the drain current by changing the channel thickness. By default, the channel conducts, but by applying a voltage on the gate, the channel is pinched and eventually isolates the source and drain entirely at the pinch-off voltage V_p. It is the depletion region from the reverse biased gate-channel junction that pinches the conductive channel. As all free charge carriers are swept away in the depletion region, it does not conduct anymore. Either one or two sides of the channel are pinched, resembling a single-gate or double-gate JFET, respectively. A double-gate NJFET is illustrated in Figure 5.1.

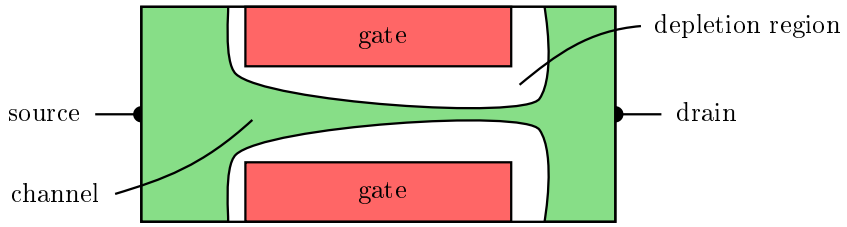


Figure 5.1: By pinching the channel, the depicted NJFET closes the channel between source and drain partially ($V_{GS} > V_p$, $V_{DS} > 0$).

Two general types of JFET can be defined: n-channel JFETs (NJFETs) and p-channel JFETs (PJFETs). For NJFETs it holds that $V_p < 0$, which means that the drain and source are isolated for gate-source voltages below its V_p. For PJFETs it holds that $V_p > 0$, which means that the drain and source are isolated for gate-source voltages above its V_p. To prevent the gate-channel junction from getting forward biased, the gate-source (and gate-drain) voltage should always be of the same polarity as the pinch-off voltage.

For the high-voltage digital signal driver application, two JFET operation regions can be

identified when the output has settled. When the cascoded MOS transistor is on, the JFET is in the ohmic region since $V_{GS} = V_{DS} = 0\,V$ for the JFET. When the cascoded MOS transistor is off, the JFET is in the cut-off region since $V_{GS} = V_p$ and $|V_{DS}| = V_{DDH}$ - $|V_p|$ for the JFET.

For this specific application, the pinch-off voltage is most important. When the magnitude of the pinch-off voltage is too high, the cascoded low-voltage MOS transistor cannot be operated reliably. The pinch-off voltage is mainly determined by the channel thickness and doping concentration. For NJFETs, the channel is n-type and for PJFETs, the channel is p-type. The gate is opposite type and significantly higher doped, creating a one-sided diode where the depletion region is mainly in the channel.

5.2 Structure of the JFETs

JFETs can be constructed with either a single or a double-gate structure. The channel thickness of a double-gate JFET should equal double the thickness of its single-gate counterpart to maintain constant pinch-off voltage. Therefore, channel thickness tolerances deteriorate double-gate structures less than single-gate structures.

5.2.1 Structure of the PJFETs

The gate of the PJFET can be implemented with a highly doped n-type layer such as deep n, buried n and n^+. A lateral PJFET with two deep n gates could be constructed, but the high deep n lateral diffusion tolerance predicts large spread on the pinch-off voltage. Instead, the buried n and n^+ layers are combined to create the gates of a lateral double-gate PJFET.

The channel of the PJFET is low to moderately doped p-type for which only the p^- substrate and p-well qualify. Because only the p-well is located between the n^+ drain/source implantation and the buried n, it is selected.

In order to pinch the entire channel, a circular design is required as depicted in Figure 5.2. By default, JFETs do not have a distinct source or drain and can be used interchangeably. However, the voltage swing of the drain is larger and breakdown should be avoided. To minimize contact with surroundings, the center is chosen as drain. Additionally, the drain benefits from having low capacitance which is achieved best in the center of this circular design.

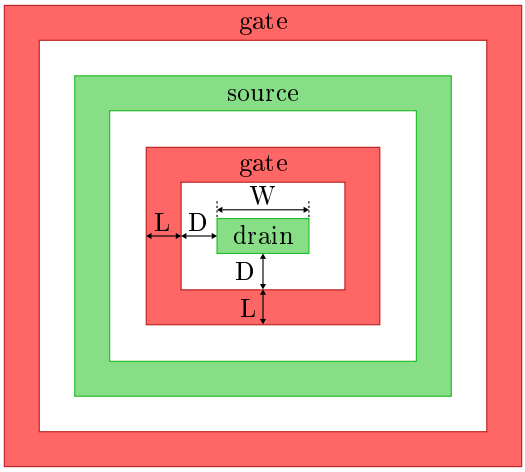


Figure 5.2: PJFET top view with varied parameters W, L and D indicated.

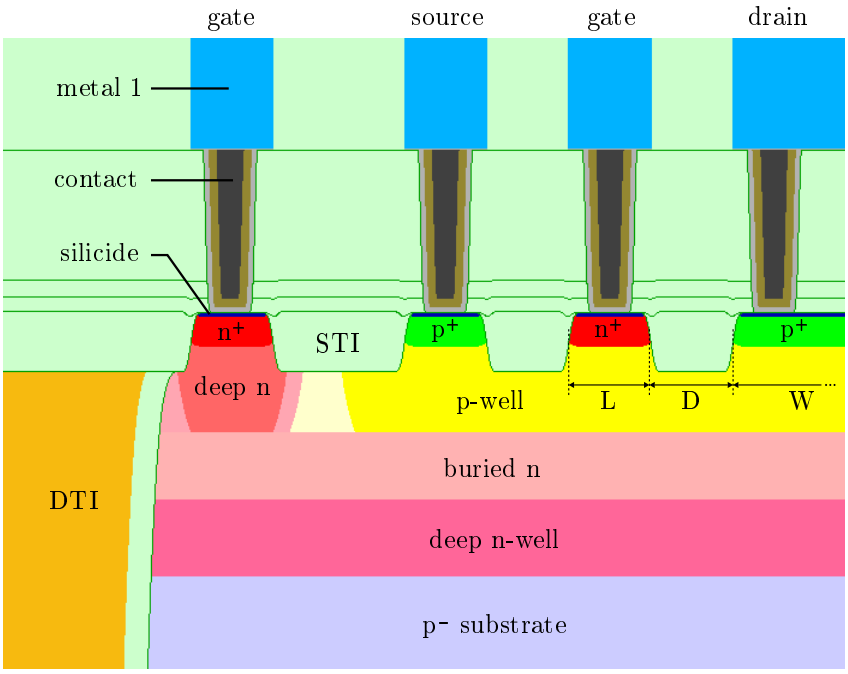


Figure 5.3: PJFET cross-section of half the symmetric device with varied parameters W, L and D indicated.

5.2.2 Structure of the NJFETs

The NJFET should have a lightly to moderately doped n-type channel. In the used technology, the n- epi, n-well and deep n-well comply. The deep n-well cannot be pinched by a highly doped layer underneath and is therefore ruled out.

Both n- epi and n-well are feasible options, in which the n-well is expected to have a higher pinch-off voltage as it is more heavily doped. However, the n-well adds buried n underneath by default when drawing the design layer. The bottom gate then disappears as buried n overdopes buried p. Custom mask scripting was required to selectively convert the n-well

design layer to only the physical n-well mask. This was not done for the first iteration so only the n- epi option was included.

Analogous to the PJFET, the NJFET requires a circular construction, see Figure 5.4. A cross-section of this device is depicted in Figure 5.5.

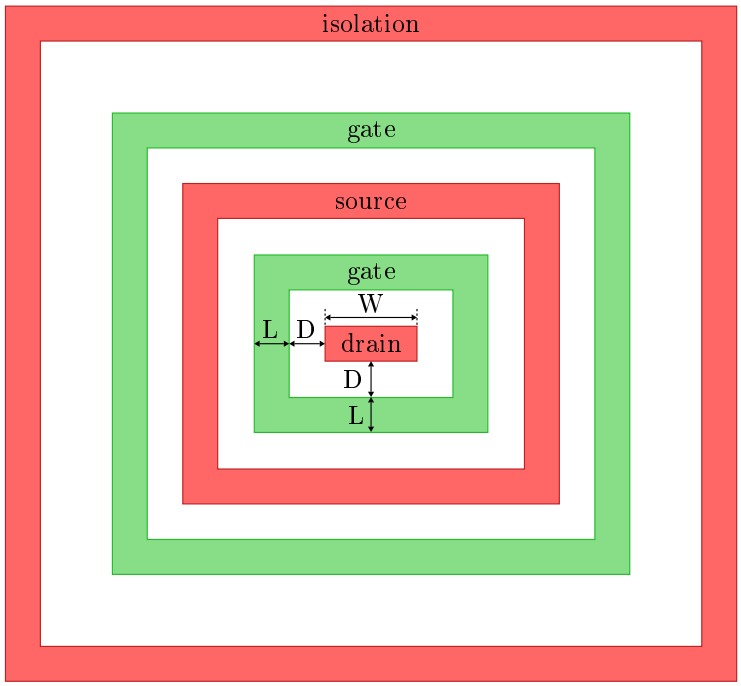


Figure 5.4: NJFET top view with varied parameters W, L and D indicated.

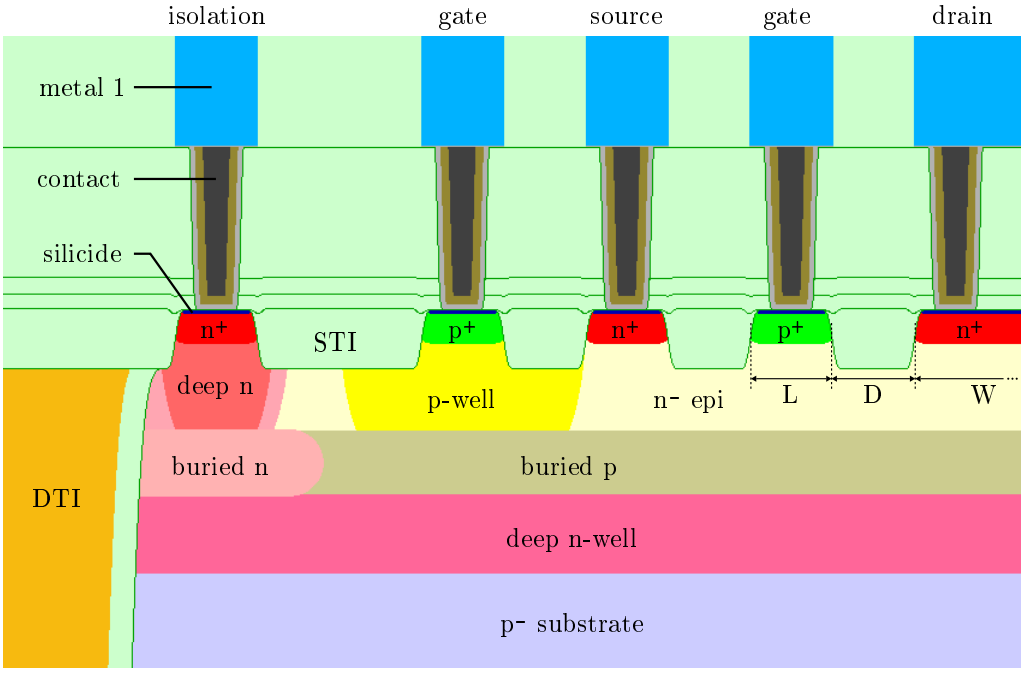


Figure 5.5: NJFET cross-section of half the symmetric device with varied parameters W, L and D indicated.

5.3 Varied Parameters of the JFETs

Gate length (L), drain width (W) and the distance between the gate and the drain (D) are varied in both NJFET and PJFET. The definitions of these parameters are given in Figures 5.2 to 5.5.

Varying the gate length is expected to change the pinch-off voltage slightly. This is because pinching is two-dimensional when the channel is not significantly longer than its thickness. Elongation of the gate will then lower the pinch-off voltage. Furthermore, the on-resistance increases for longer gates, decreasing the maximum transistor current.

Increasing the drain width will decrease the on-resistance non-linearly for its circular construction. The perimeter of the drain is proportional to the on-resistance so scaling in two directions is area-inefficient. When the drain aspect ratio increases, the on-resistance will scale more linearly with W.

Breakdown was expected to first occur at the drain-gate junction. The breakdown voltage then increases with larger distances D between these regions.

The varied parameters are equal for NJFET and PJFET and are listed in Table 5.1.

Table 5.1: Varied parameters of the JFETs, changing only one at a time while keeping the default value (in bold) for the remaining parameters. This yields 8 NJFETs and 8 PJFETs in total.

Parameter	Value (µm)			
Width (W)	**1.3**	2.1	3.7	9.3
Gate length (L)	**0.5**	1.3	2.1	
Gate-drain distance (D)	**0.5**	1.3	2.1	

5.4 Measurements and Discussion of the JFETs

The JFET structures were measured and found not to function. Where the JFETs should have drain-source conduction at $V_{GS} = 0\,V$, none did. In forward bias, the gates conducted to the source before the drain-source channel was opened.

Presumably, this was caused by the shallow trench isolation between the active areas. If the STI etch reaches as deep as the buried bottom gate, the channel disappears. Improvements are proposed in the next chapter.

Chapter 6

Improved Junction Field-Effect Transistors

The JFET structures proposed in Chapter 5 were found to be not functional. This was presumably caused by the shallow trench isolation (STI) that separates the n^+ and p^+ regions. In this chapter, this problem is aimed to be solved by redesigning the JFETs. The measurement results of these improved devices are then discussed and a conclusion is stated.

6.1 Structure of the Improved JFETs

To replace the STI, polysilicon spacers were created with the self-aligned MOS transistor gates. The spacer separates the n^+ and p^+ regions by shielding the underlaying well from the shallow implantations. Negligible bulk material is removed, leaving the channel open and therefore solving the problem encountered in the first iteration.

The thin gate oxide is not reliable for voltages over 2.5 V so sacrificial oxide (SOX) is added. SOX is 10 nm thermal SiO_2 and reduces the ion steering effect during the well implantations. As ions are "bombarded" through the SOX, its thickness and quality decrease. In standard CMOS processes, all SOX is removed after the implantations but in the used BiCMOS process the SOX is removed selectively by means of an extra mask. Since this is a standard mask in the used technology, no extra production costs apply by adding SOX to the JFETs. Thin gate oxide is grown underneath the SOX but does not grow as fast because the SOX layer slows the oxidation down. A total of about 10 nm thick gate oxide was expected after all processing.

The thicker oxide also decreases the inversion and accumulation effects that are introduced by creating the MOS structure. Depending on the gate voltage, either of the two effects is active, potentially changing the characteristics of the JFET. The spacers were connected to standard JFET terminals to keep the amount of terminals of the transistor limited. Leaving the spacers floating was not deemed a valid solution as this creates unpredictable and volatile behavior.

In the single-gate configurations, the spacer voltage affects the pinching of the channel. With accumulation, a low-ohmic path is formed between source and drain. This effect hinders pinching the channel and therefore inversion is preferred instead. With inversion, the gate will push away free charge carriers in the channel, making the channel less conductive. This

is obtained by connecting the spacer to the source.

In the double-gate configurations, one spacer is connected to the source and one spacer is connected to the drain. The adjacent source/drain connection is selected as only a small voltage then appears over the oxide.

As opposed to the first design iteration, custom mask scripting was performed. This is a non-standard conversion from design layers to physical masks to obtain full control over the generated masks. Specifically, n-well without buried n underneath and therefore more NJFET structures become available. Figure 6.1 illustrates the implemented structures and the cross-sections of these devices are depicted in Figures 6.3 to 6.4.

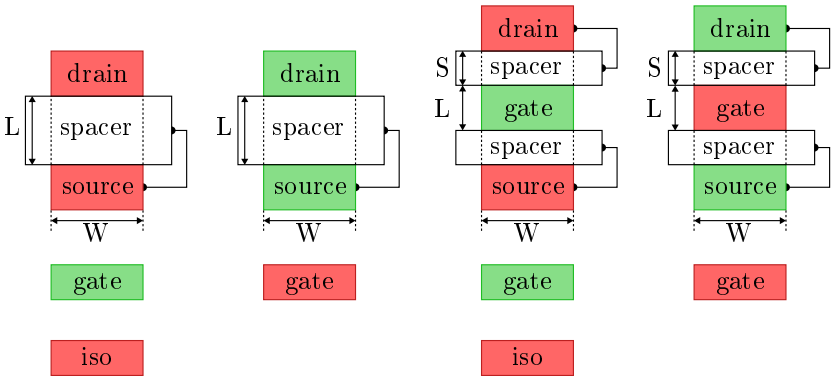


Figure 6.1: Top view of the single-gate NJFET, single-gate PJFET, double-gate NJFET and double-gate PJFET from left to right.

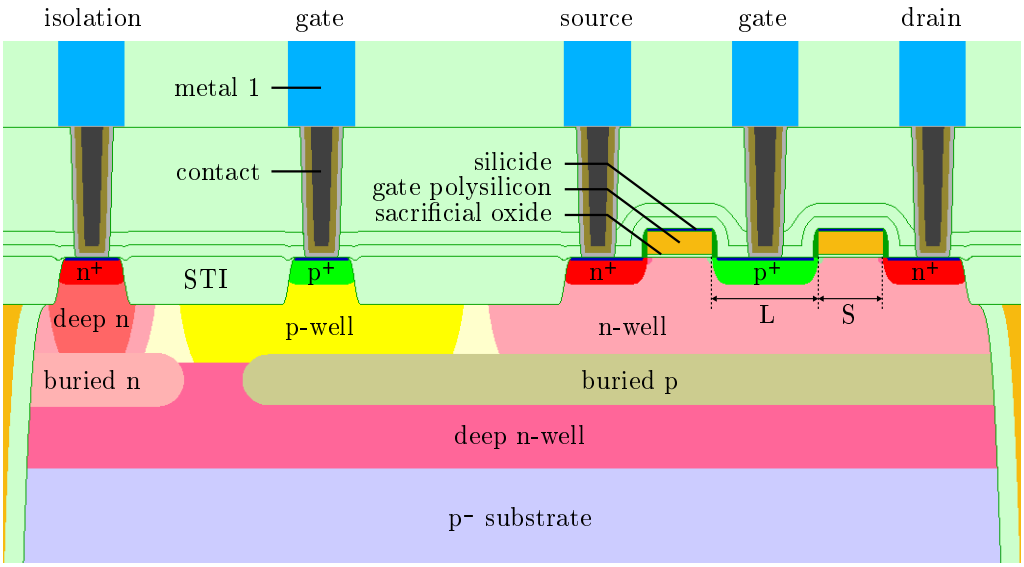


Figure 6.2: Cross-section of the double-gate NJFET structure using an n-well channel.

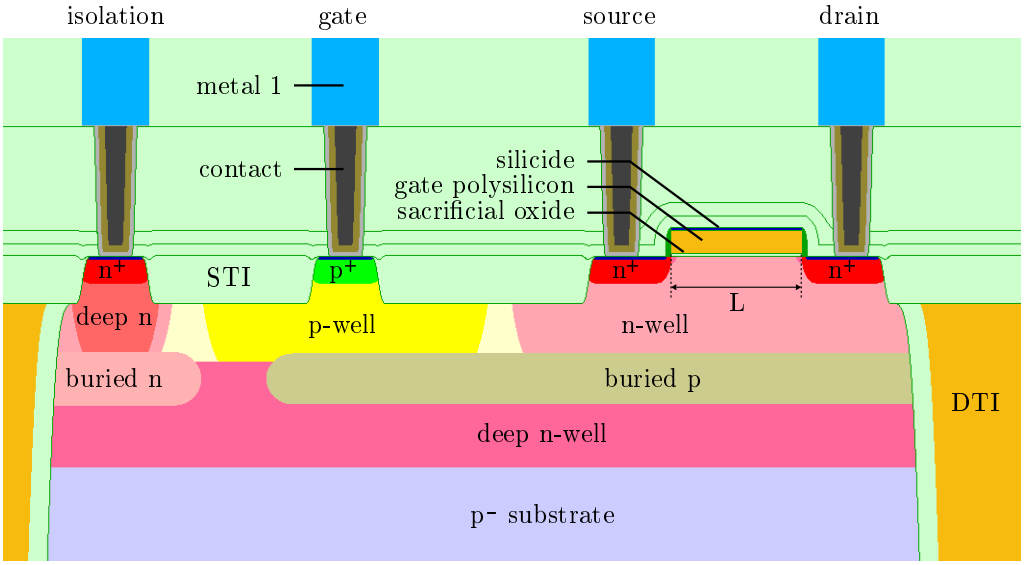


Figure 6.3: Cross-section of the single-gate NJFET structure using an n-well channel. The n- epi variant is created by removing the n-well in the channel.

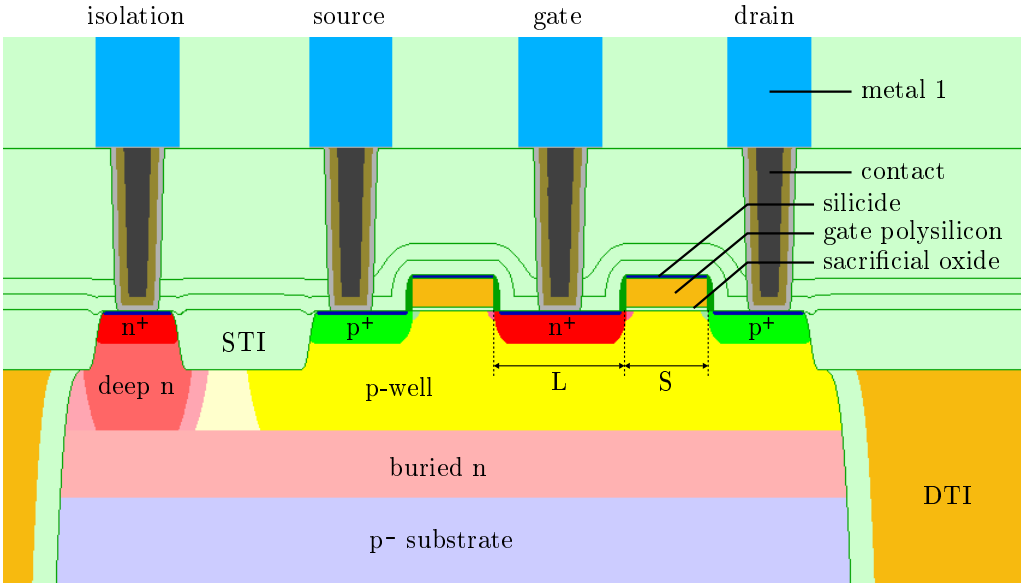


Figure 6.4: Cross-section of the double-gate PJFET structure.

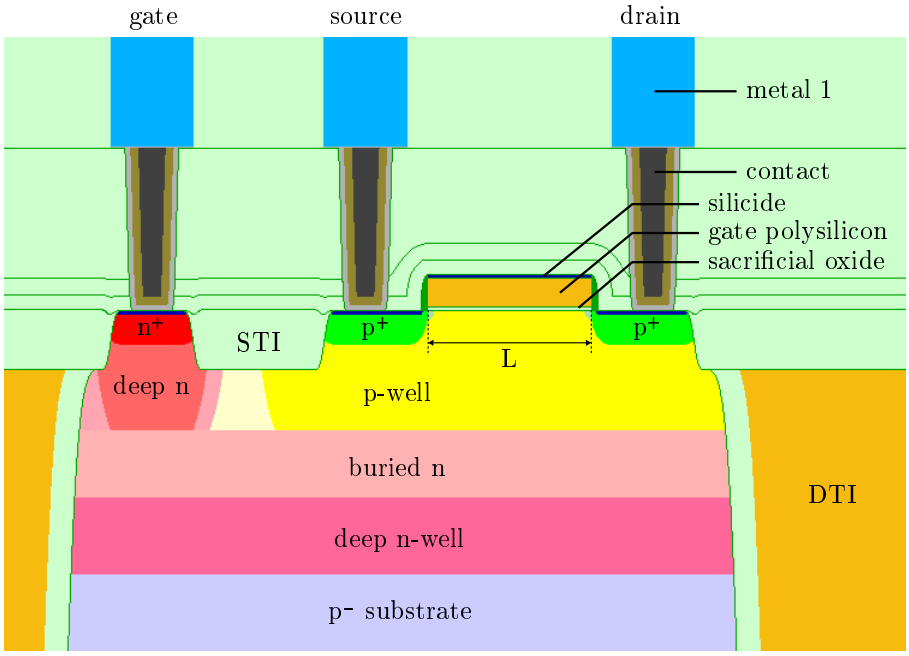


Figure 6.5: Cross-section of the single-gate PJFET structure.

6.2 Varied Parameters of the Improved JFETs

As illustrated in Figures 6.1 to 6.4, geometric variations were made on the JFET structures. The double-gate JFET variations listed in Table 6.1 were included, corresponding to the parameter definitions from Figure 6.2 and Figure 6.4. These are similar to the variations made in the first iteration since no feedback on them was obtained. The double-gate NJFET was implemented with n-well and n- epi, yielding a double amount of variants.

Table 6.1: Varied parameters of the double-gate JFETs, changing only one parameter at at time while keeping the default value (in bold) for the remaining parameters. Each parameter value was created twice: with n-well and with n- epi. This yields 15 variants in total.

Parameter	Value (µm)		
Width (W)	**1.3**	2.9	
Gate length (L)	**0.5**	1	2
Gate-drain distance (D)	**0.5**	1	

The single-gate JFET was not implemented during the first iteration and has different parameters compared to the double-gate JFET. Since the distance between the spacer and the bottom gate is large, a low-doped channel is required. The moderately doped wells were not expected to sufficiently deplete at $|V_{GS}| = 2.5\,V$. Only one geometric implementation is therefore included per well-based type. Both have $W = 1.3\,\mu m$ and $L = 1\,\mu m$, corresponding to Figure 6.3 and Figure 6.5 for NJFET and PJFET, respectively.

Additionally, NJFETs with n- epi channels were implemented. The varied parameters of this n- epi NJFET are listed in Table 6.2 and correspond to the cross-section of Figure 6.3,

but without the n-well drawn.

Table 6.2: Varied parameters of the single-gate n⁻ epi NJFET, changing only one parameter at a time while keeping the default value (in bold) for the remaining parameters.

Parameter	Value (µm)		
Width (W)	**1.3**	2.9	
Gate length (L)	0.5	**1**	2

6.3 Measurements of the Improved JFETs

From all designs mentioned in this chapter, only a single NJFET and single PJFET had drain-source conduction for any gate voltage. These were the single-gate versions with well channels. Both JFETs had an absolute pinch-off voltage over 5 V, making them unsuited for the high-voltage digital level shifter application. In Figure 6.6 and Figure 6.7, the V_{DS}-I_D characteristics of the JFETs are depicted for multiple values of V_G. The pinching effect of the JFETs are clearly visible; the channel conduction decreases for gate voltages closer to the pinch-off voltage.

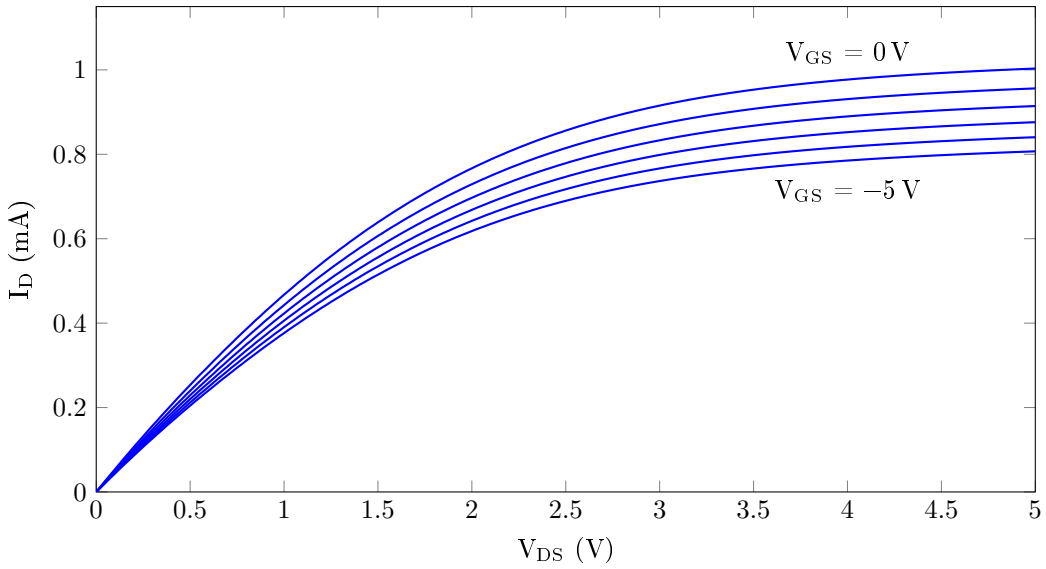


Figure 6.6: V_{DS}-I_D characteristics of the single-gate NJFET with n-well channel for varying V_{GS}. For this device W = 1.3 µm and L = 1 µm.

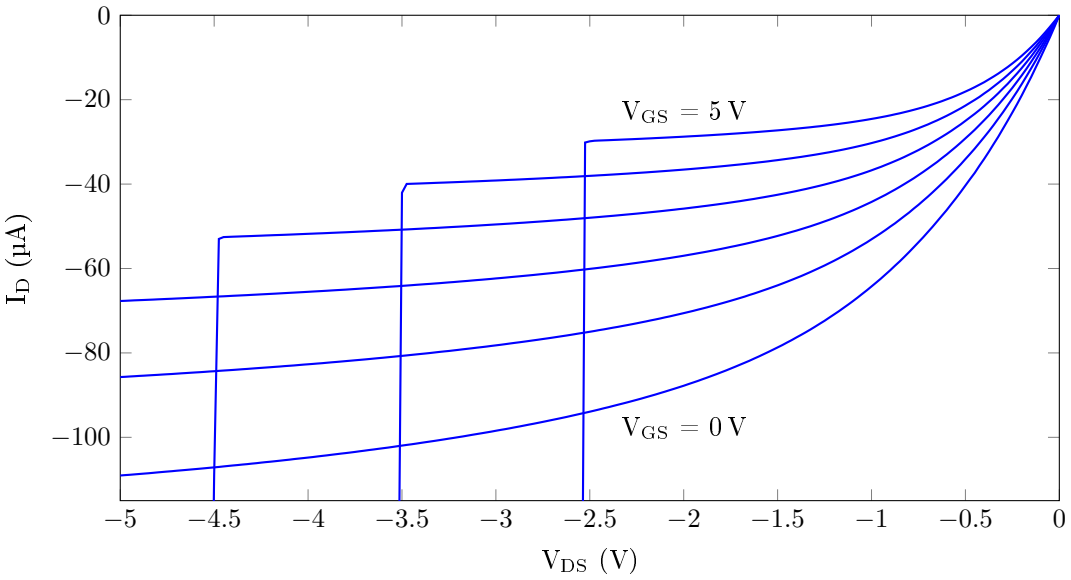


Figure 6.7: V_{DS}-I_D characteristics of the single-gate PJFET with p-well channel for varying V_{GS}. For this device W = 1.3 µm and L = 1 µm.

6.4 Discussion and Conclusion of the Improved JFETs

The fabricated JFETs do not meet the specifications stated in Section 2.3.2 as the absolute pinch-voltage is not close to 2.5 V for any of the investigated configurations. In most configurations, no source-drain conduction was observed for V_{GS} = 0 V. This means that the channel was either totally overdoped by the gates or cut-off was already reached for V_{GS} = 0 V with overly shallow channels. Too high pinch-off voltages were also observed which indicates the channel is too thick.

In Section 5.4 was presumed that the shallow trench isolation above the buried layers did not leave any channel. This can be questioned as similar JFET structures with polysilicon spacers also did not conduct. However, isolating the p-type and n-type regions with polysilicon spacers intuitively enhance transistor performance as it decreases the channel series resistance. Also it enables making single-gate JFETs.

As recommendation, the lateral PJFET with deep n vertical gates can be researched. The distance between the two gates can then be varied to select the pinch-off voltage.

Chapter 7

Double-Diffused MOS Transistors

As described in Section 2.3.3, the JFET-based high-voltage digital signal driver can be improved by implementing DMOS transistors. In this chapter, the working principle of DMOSTs is explained and is used to design n and p-type DMOSTs. Starting from a default layouts, geometric parameters are varied to examine their effects on the DC characteristics. A conclusion on the performance of the fabricated DMOSTs is then stated with proposed improvements for the second iteration.

7.1 Working Principle of the DMOST

Breakdown of MOS transistors is generally from the drain to the gate, as the electric field over the oxide is largest here. In DMOS transistors, the gate oxide is thicker at the drain side, increasing the breakdown voltage. As already illustrated in Figure 2.4 when discussing gate oxide breakdown, a thicker oxide needs more traps lining up to create a conductive path and is thus more robust.

In Section 2.2.1, breakdown due to vertical electric fields over the oxide was discussed as no voltage between source and drain was present. However, with high lateral electric fields in the channel due to drain-source voltage, hot-carriers generate traps in the oxide as well. Hot carriers are electrons or holes, which under the influence of high lateral fields in the channel gain sufficient energy to realize impact ionization. This effectively creates an electron-hole pair. The holes enter the substrate and the electrons enter the gate oxide, which may create traps in the oxide and initiate gate oxide breakdown [12].

Channel hot-carrier trap generation can be reduced by decreasing the maximum lateral electric field in the channel. For a uniformly doped, abrupt junction, the maximum electric field E_{max} is [13]

$$E_{max} = -\sqrt{\frac{2e(V_{bi} + V_R)}{\epsilon_s}\left(\frac{N_a N_d}{N_a + N_d}\right)} \tag{7.1}$$

Here, $V_{bi} = V_t \ln\left(N_a N_d / n_i^2\right)$ is the built-in voltage, V_R is the applied reverse voltage over the junction, ϵ_s is the absolute permittivity of silicon and N_a and N_d are the dopant concentrations of the p and n regions, respectively. The drain-bulk junction of an NMOS can be approximated as a one-sided diode with $N_d \gg N_a$. The depletion region will then primarily stretch under the gate and the maximum electric field can be approximated to

$$E_{max} = -\sqrt{\frac{2e(V_{bi} + V_R)}{\epsilon_s} N_a} \tag{7.2}$$

If the drain contact would be doped similarly to the transistor bulk, say $N_d = N_a = N$, the maximum electric field becomes

$$E_{max} = -\sqrt{\frac{2e(V_{bi} + V_R)}{\epsilon_s} \frac{N}{2}} \tag{7.3}$$

When comparing Equation (7.2) and Equation (7.3), choosing $N_d = N_a$ over $N_d \gg N_a$ reduces the maximum electric field by roughly 30 % when ignoring the change in built-in voltage. If the bulk acceptor concentration N_a is kept constant and N_d is lowered, the built-in voltage will decrease, which decreases the maximum electric field further. The difference between the two cases is illustrated in Figure 7.1. Furthermore, the extended drain diffusion has relatively high resistance, creating a voltage drop over this "drift region". This effectively decreases the channel voltage.

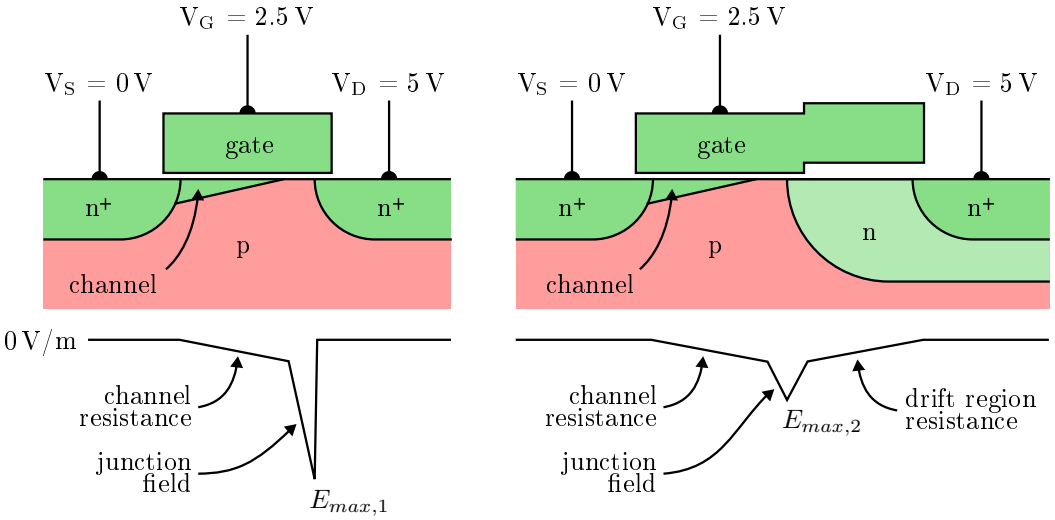


Figure 7.1: Lowering the drain dopant concentration lowers the maximum electric field under the gate for an NDMOST. The p-type substrate is grounded for both cases.

DMOSTs feature a step in gate oxide thickness, being thicker at the drain side. The position of this step is chosen to keep the threshold voltage of the MOS equivalent, yet have thicker oxide where a high drain voltage might occur. To keep the threshold voltage low, all bulk area should be covered by thin oxide. The drain region close to the bulk is depleted in the case that $V_{GS} < V_T$, which protects any small overlap of gate over the drain. Furthermore, the drain region below the gate is depleted, effectively decreasing the voltage drop over the oxide. For the case that $V_{GS} > V_T$, the voltage over the oxide is already limited and is further decreased by the voltage drop over the drift region. Concluding, the gate step position should ideally be at the drain-bulk junction, but can be moved slightly towards the drain.

7.2 Structure of the DMOSTs

The added drain diffusions are less heavily doped than the regular CMOS drain contacts. The silicon just below the gate is n- epi and can be implanted to n-well or p-well or left unaltered. Implementing the NDMOST drain with n- epi is not preferable as lateral diffusion of the more heavily doped p-well bulk then shifts the bulk-drain junction heavily towards the drain. As the n-well and p-well have similar doping concentrations, a well-defined junction location is obtained. Furthermore, the resistance of n- epi is higher than n-well-implanted silicon.

Besides the normal thin gate oxide, a ticker oxide is required to create the step gate. Two thicker oxides are identified in the used BiCMOS technology: the shallow trench isolation (STI) and the sacrificial oxide (SOX). STI is an isolation between active areas and is about 500 nm deep. SOX is 10 nm thick and reduces the ion steering effect during the well implantations. After the implantations, the SOX is removed selectively with a mask that is readily available in the used technology. Therefore, no extra manufacturing costs apply when implementing SOX in the DMOSTs.

Both thick oxides leave a conductive path since the well implantations reach through them. However, STI creates a significant gap in the silicon bulk which increases the drain resistance. SOX is therefore preferred, yet both are investigated experimentally in this study.

7.2.1 Structure of the NDMOSTs

The NDMOS transistors are implemented with an n-well drain and a p-well channel. Buried n is always added under the n-well when converting the design layers to the physical masks. For the first design iteration, no time was left to change these conversion operations. Ideally, the buried n should be removed to increase the breakdown voltage between the drain and bulk.

The thick oxide is implemented with sacrificial oxide in Figure 7.3 and with shallow trench isolation in Figure 7.4. A universal top view is depicted Figure 7.2.

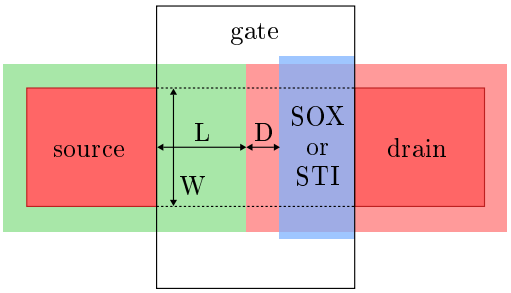


Figure 7.2: Top view of the NDMOS transistor structure.

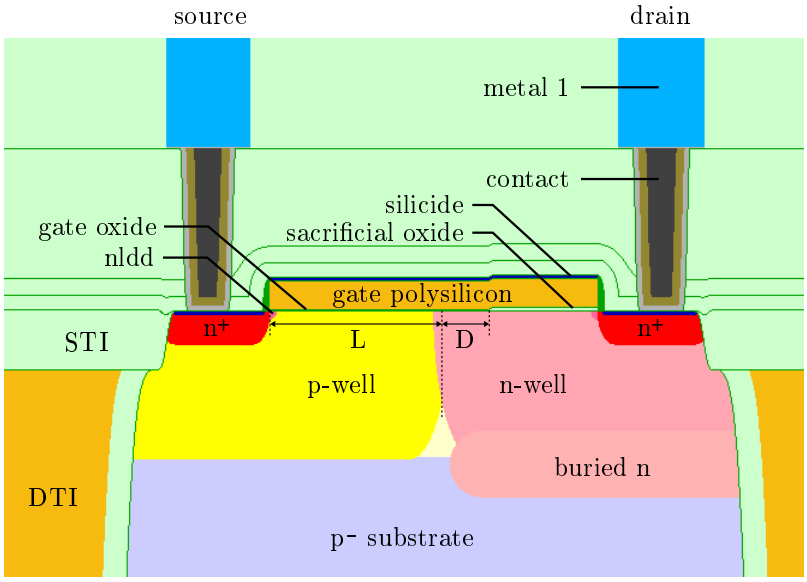


Figure 7.3: Cross-section of the SOX-based NDMOS transistor structure. The channel is located where L is indicated, just below the gate.

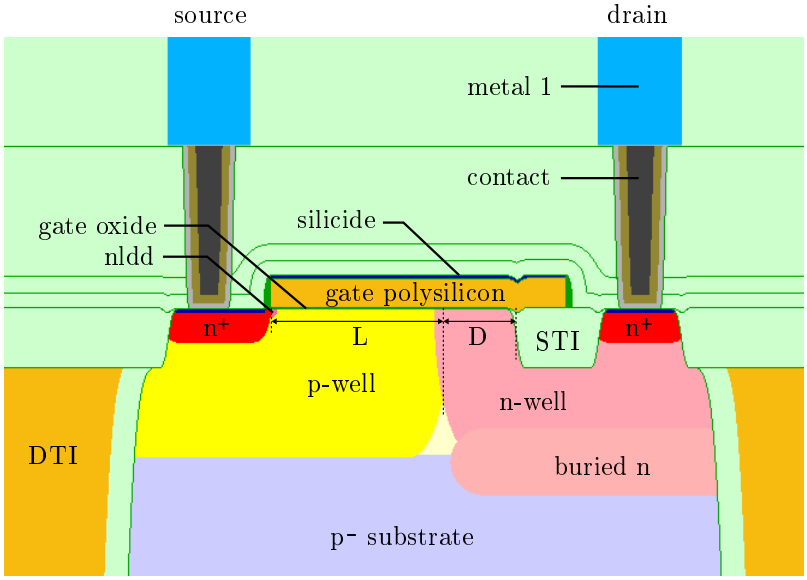


Figure 7.4: Cross-section of the STI-based NDMOS transistor structure. The channel is located where L is indicated, just below the gate.

7.2.2 Structure of the PDMOSTs

Analogous to the NDMOS transistors, the PDMOS transistors can be implemented with SOX and STI as thick oxide. Cross-sections of these SOX and STI-based PDMOSTs are depicted in Figure 7.6 and Figure 7.7 and a universal top view is shown in Figure 7.5.

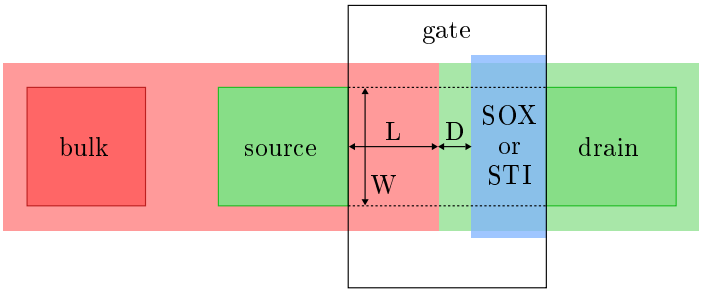


Figure 7.5: Top view of PDMOS transistor structure.

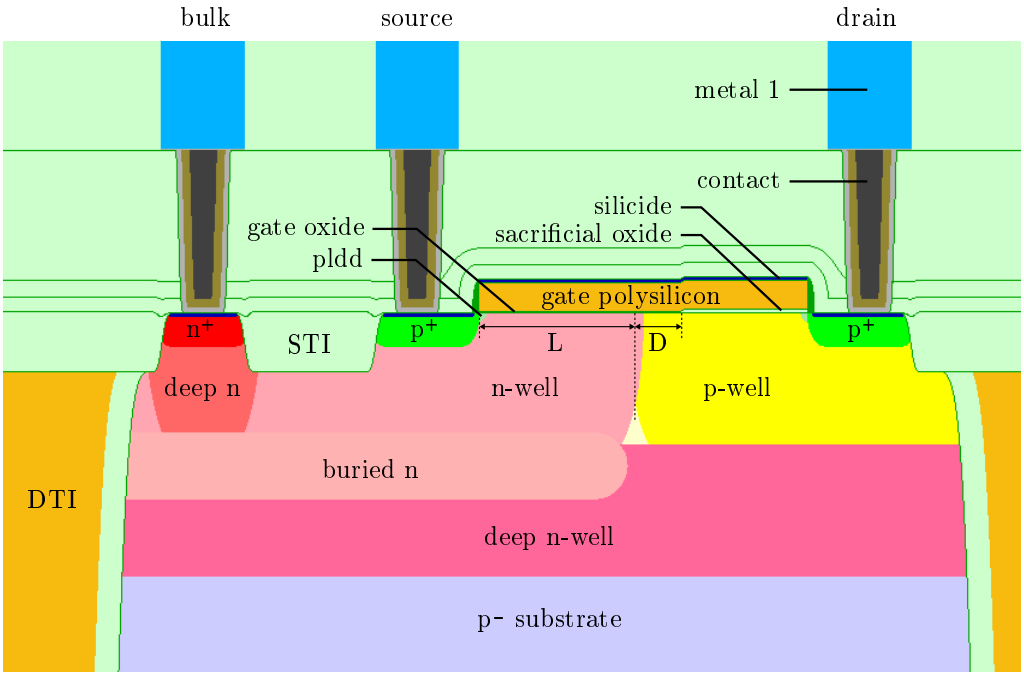


Figure 7.6: Cross-section of the SOX-based PDMOS transistor structure. The channel is located where L is indicated, just below the gate.

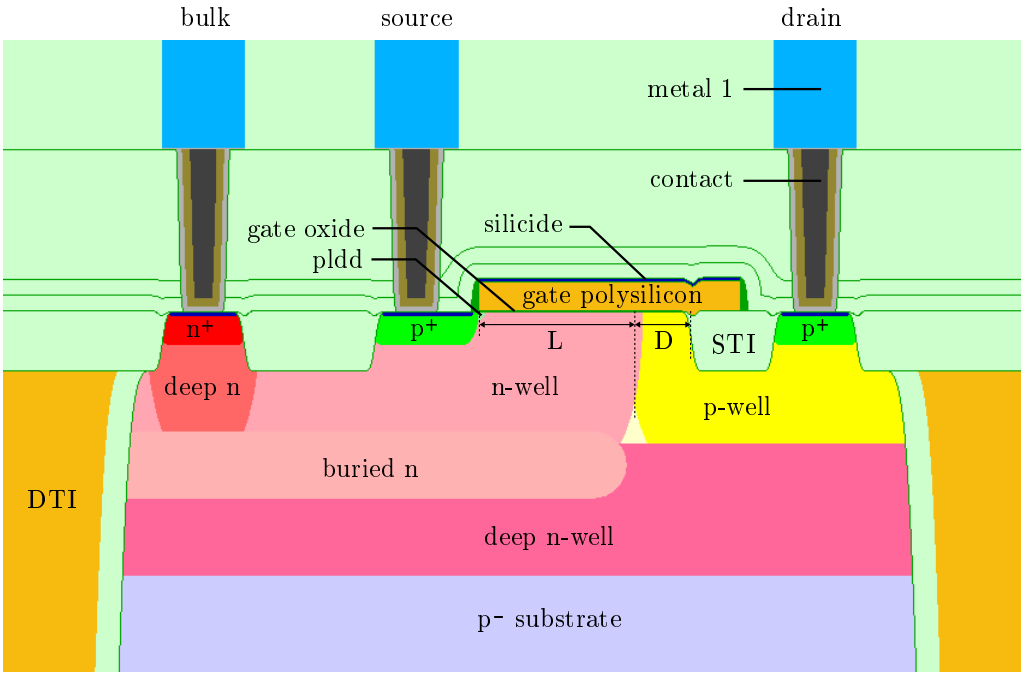


Figure 7.7: Cross-section of the STI-based PDMOS transistor structure. The channel is located where L is indicated, just below the gate.

In contrast to the NDMOSTs, the bulk is not connected to the substrate and is therefore connected separately for the PDMOSTs. Furthermore, between the p-type drain and p-type substrate, an n-type isolation barrier is implemented. Since the substrate is grounded, no positive voltage can forward bias the junction towards the substrate when an n-type layer is added. Analogously, the n-type isolation layer is kept at a higher voltage than the drain. The bulk complies with this voltage requirement and is therefore extended in order to create this isolation layer. The isolation can then be implemented with buried n or deep n-well which are both located under the p-well. Buried n is located closer to the surface than the deep n-well. This leaves less p-well and thus increases the drain resistance. Furthermore, the buried n is doped more heavily than the deep n-well which lowers the drain-bulk breakdown voltage. Therefore, the n-type barrier is implemented with deep n-well.

7.3 Varied Parameters of the DMOSTs

Transistor width (W), gate length (L) and step-gate location (D) are varied in both DMOS transistor types as indicated in Figures 7.2 to 7.7.

Ideally, the transistor's W/L ratio scales the drain current in all operation regions linearly. However, short channel lengths introduce significant channel length modulation and the drain-source breakdown voltage decreases.

The distance D from the bulk-drain junction to the gate oxide thickening is crucial and determines the drain-gate breakdown voltage. Positive values of D refer to gate-step locations more towards the drain from the junction, negative more towards the source. As discussed in Section 7.1, D is ideally slightly positive.

For the STI-based transistors, only positive values of D leave a conductive path between the

inverted channel and the drain. All varied parameters of the STI-based DMOS transistors are listed in Table 7.1 and Table 7.2.

Table 7.1: Varied parameters of the STI-based NDMOST, changing only one parameter at a time while keeping the default value (in bold) for the remaining parameters. This yields 8 variants in total.

Parameter	Value (µm)				
Width (W)	**1.3**	2.9			
Gate length (L)	0.25	0.5	**1**		
Step-gate position (D)	**0.5**	0.6	0.7	0.8	1

Table 7.2: Varied parameters of the STI-based PDMOST, changing only one parameter at a time while keeping the default value (in bold) for the remaining parameters. This yields 6 variants in total.

Parameter	Value (µm)				
Width (W)	**1.3**	2.9			
Gate length (L)	0.25	0.5	**1**		
Step-gate position (D)	0.25	**0.3**	0.4	0.5	0.75

For the SOX-based transistors, both positive and negative values of D are possible. A variety of values were experimented, as listed in Table 7.3.

Table 7.3: Varied parameters of the SOX-based DMOSTs, changing only one parameter at a time while keeping the default value (in bold) for the remaining parameters. This yields 16 variants in total.

Parameter	Value (µm)				
Width (W)	**1.3**	2.9			
Gate length (L)	0.25	0.5	**1**		
Step-gate position (D)	-0.15	0	0.15	**0.3**	0.5

7.4 Measurements of the DMOSTs

The Agilent HP 4155A semiconductor parameter analyzer was to used perform these DC measurements at wafer level. The specifications of all measured DMOSTs are listed in Appendix A.

7.4.1 Measurements of the NDMOSTs

Gate length L, transistor width W and step-gate location D were varied in the default NDMOST geometry.

Effects of the Gate Length on the NDMOST Characteristics

In Figure 7.8, V_{DS}-I_D and V_{GS}-I_D measurements are plotted for the NDMOS transistors. The SOX and STI counterparts have equal characteristics within per-device deviations. The gate length strongly effects the breakdown voltage at which a large current flows from drain to source. Therefore, total channel depletion was presumed.

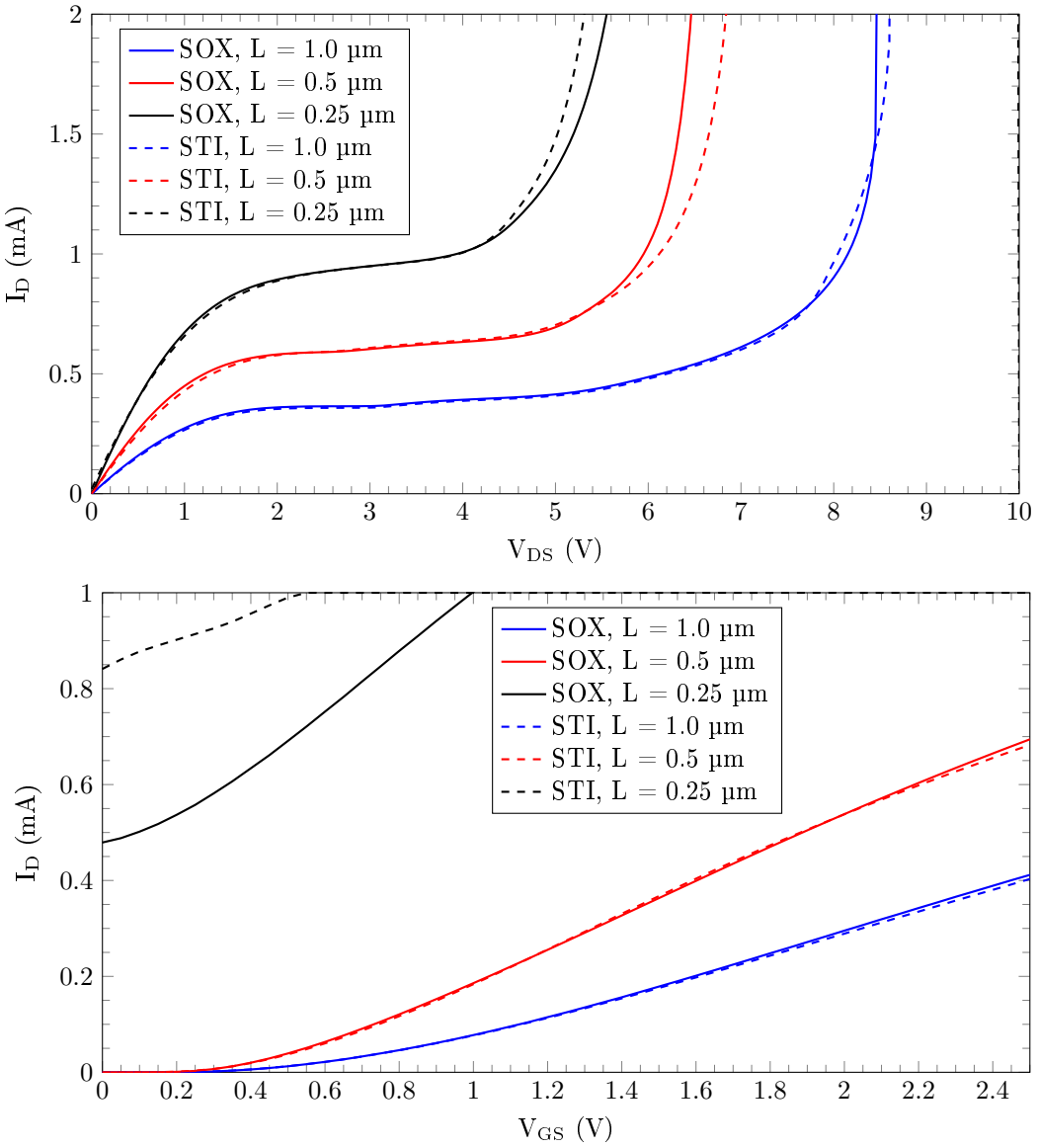


Figure 7.8: V_{DS}-I_D characteristics of NDMOSTs with different gate lengths at V_{GS} = 2.5 V and V_{GS}-I_D characteristics at V_{DS} = 5 V. For all cases W = 1.3 µm and for the SOX-based devices D = 0.3 µm and for the STI-based devices D = 0.5 µm.

Effects of the Transistor Width on the NDMOST Characteristics

The V_{DS}-I_D characteristics of NDMOSTs with different transistor widths are plotted in Figure 7.9. For both SOX and STI-based NDMOS transistors, the breakdown voltage is lowered for the wider device. Further research is required to explain this relationship.

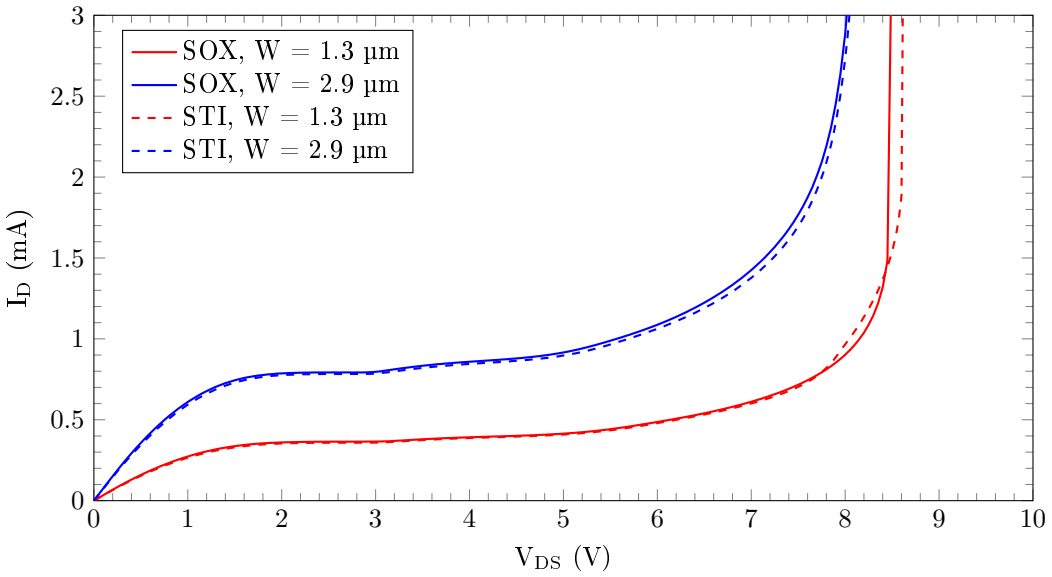


Figure 7.9: V_{DS}-I_D characteristics of NDMOSTs with different widths at V_{GS} = 2.5 V. For the STI-based devices D = 0.5 µm and for the STI-based devices D = 0.3 µm.

Effects of the Gate Step Position on the NDMOST Characteristics

Measurements for different values of D were near identical for both STI and SOX-based NDMOS transistors. As drain-source breakdown occurs before drain-gate breakdown can occur in all variants, no sensible measurements to the effectiveness of the oxide step position could be done in the default measurement setup. To cope with this, the source was left open and a bulk-drain voltage sweep at V_{GB} = 0 V was applied instead. The V_{DB}-I_B characteristics of SOX-based NDMOSTs with different values of D are plotted in Figure 7.10. In all measured NDMOSTs, drain-bulk breakdown starts around 8 V, causing the drain-bulk current to increase exponentially until the approximately 10 kΩ substrate resistance linearizes the curve. A voltage drop over the substrate will then arise, increasing the bulk voltage. When raised sufficiently, the thin oxide near the gate step breaks down as the voltage increases towards the drain.

Additionally, an accumulation layer is created under the gate by raising the bulk voltage, as illustrated in Figure 7.11. For D > 0, the accumulation layer connects to the drain, generating stronger breakdown than the default bulk-drain junction. This explains the difference between the characteristics of the NDMOSTs with D = 0.15 µm and D = −0.15 µm. For D = 0, both breakdowns are visible; first between drain n-well/buried n to bulk p-well, second between the drain n-well and the bulk p-well accumulation layer. A clear transition is visible at 15 V in the V_{DB}-I_B characteristic of the device with D = 0 µm.

The drain-bulk breakdown voltage can be increased by removing the buried n layer. In all measured devices, this was presumed to initiate the breakdown process.

The STI-based NDMOS transistors had near identical characteristics, notably hard oxide breakdown at 15 V.

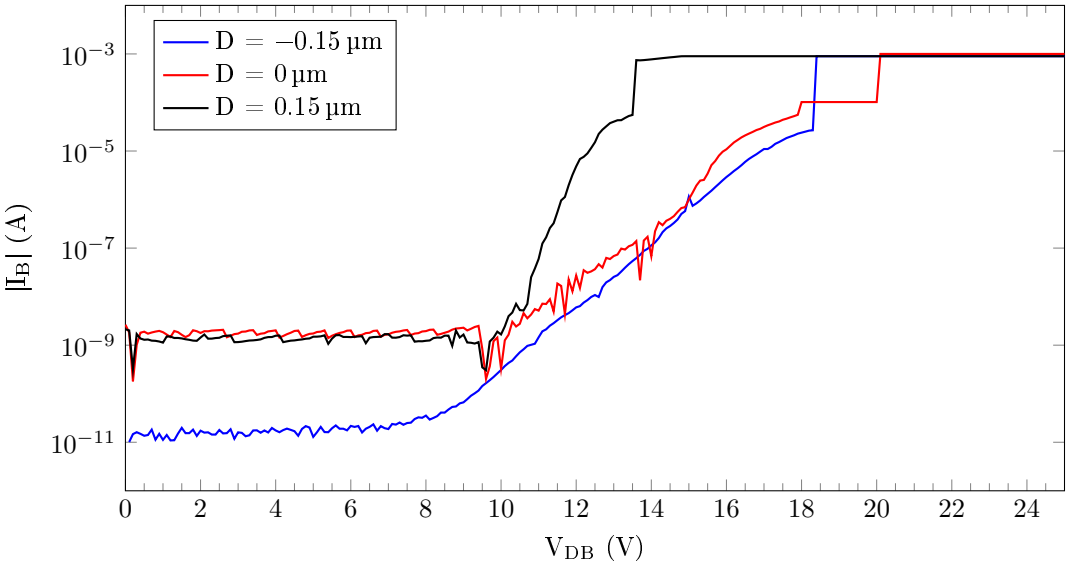
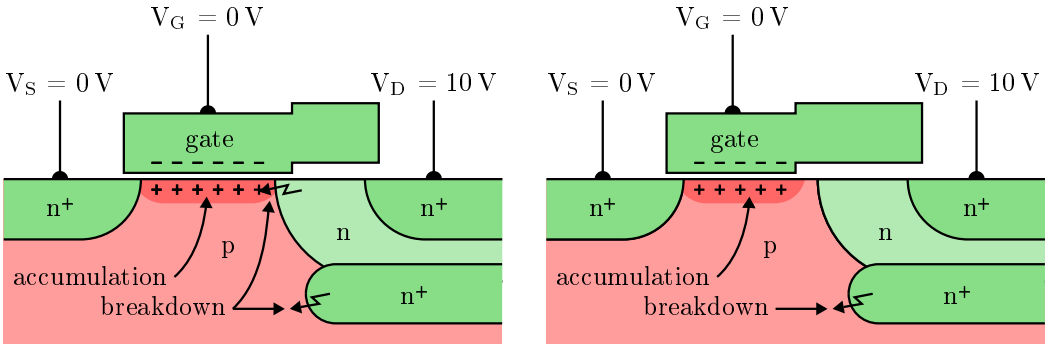


Figure 7.10: V_{DB}-I_B characteristics of SOX-based NDMOSTs with different values of D at $V_{GB} = 0\,V$ and the source left open. For all cases $W = 1.3\,\mu m$ and $L = 1\,\mu m$.



(a) NDMOST with $D > 0$.

(b) NDMOST with $D < 0$.

Figure 7.11: NDMOSTs with positive D (a) break down more heavily towards the accumulation layer in the bulk, whereas DMOSTs with negative D (b) do not.

7.4.2 Measurements of the PDMOSTs

The V_{DS}-I_D and V_{GS}-I_D characteristics of PDMOSTs with different gate lengths are plotted in Figure 7.12. Breakdown starts in the gate-substrate diode at $V_{G,SUB} = 14\,V$, but does not lead to transistor breakdown until the power supply current limit is reached in the measurement setup. This diode protects the gate oxide during fabrication and is always reverse biased during normal operation. No other breakdown effects were found for any variant at lower voltages than the gate-bulk diode breakdown voltage.

The default STI-based PDMOST has abnormal V_{GS}-I_D characteristics for a transistor; the drain current saturates towards a constant value for increasing gate voltage. The default SOX-based PDMOST has significantly higher conduction and does not saturate in the V_{GS}-I_D curve. From the V_{GS}-I_D characteristics of STI-based PDMOSTs with different gate step locations from Figure 7.13 is was found that increasing D clears the saturation effect.

However, the R_{on} of these STI-based PDMOSTs is still considerably higher than of the SOX-based counterparts; 25 kΩ versus 15 kΩ. As a comparison, the SOX and STI-based NDMOST counterparts had near identical characteristics. The main difference is the low-ohmic buried n layer underneath the n-well in the NDMOST. The PDMOST drain p-well has deep n-well underneath and the STI removes a significant portion of the p-well. Consequently, the drain resistance of the STI-based PDMOST is higher than of the SOX-based PDMOST.

The SOX-based PDMOST had near equal characteristics for all step gate location variants.

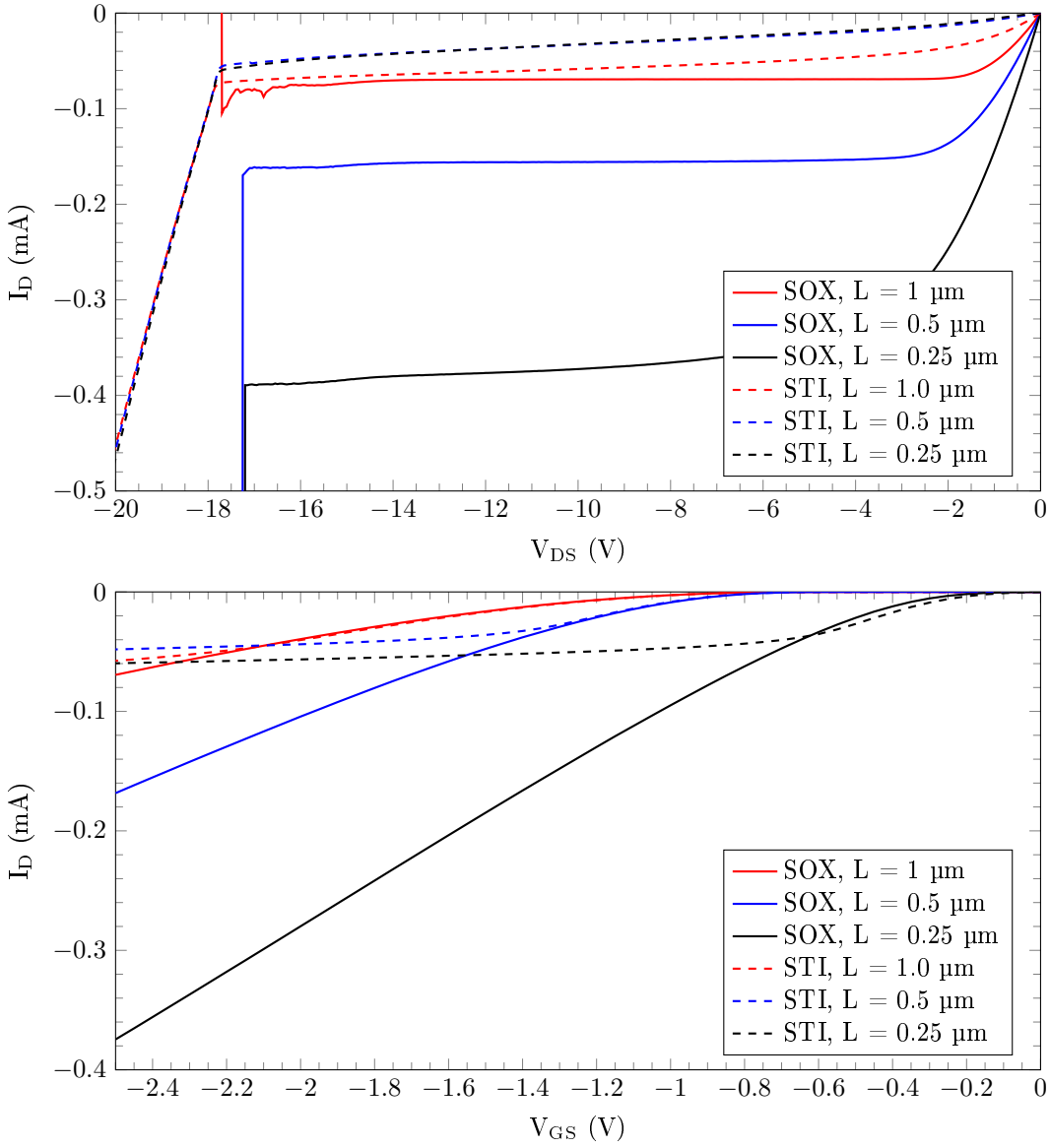


Figure 7.12: V_{DS}-I_D characteristics of PDMOSTs with different gate lengths at $V_{GS} = -2.5\,V$ and V_{GS}-I_D characteristics at $V_{DS} = -10\,V$. For all cases W = 1.3 µm and D = 0.3 µm.

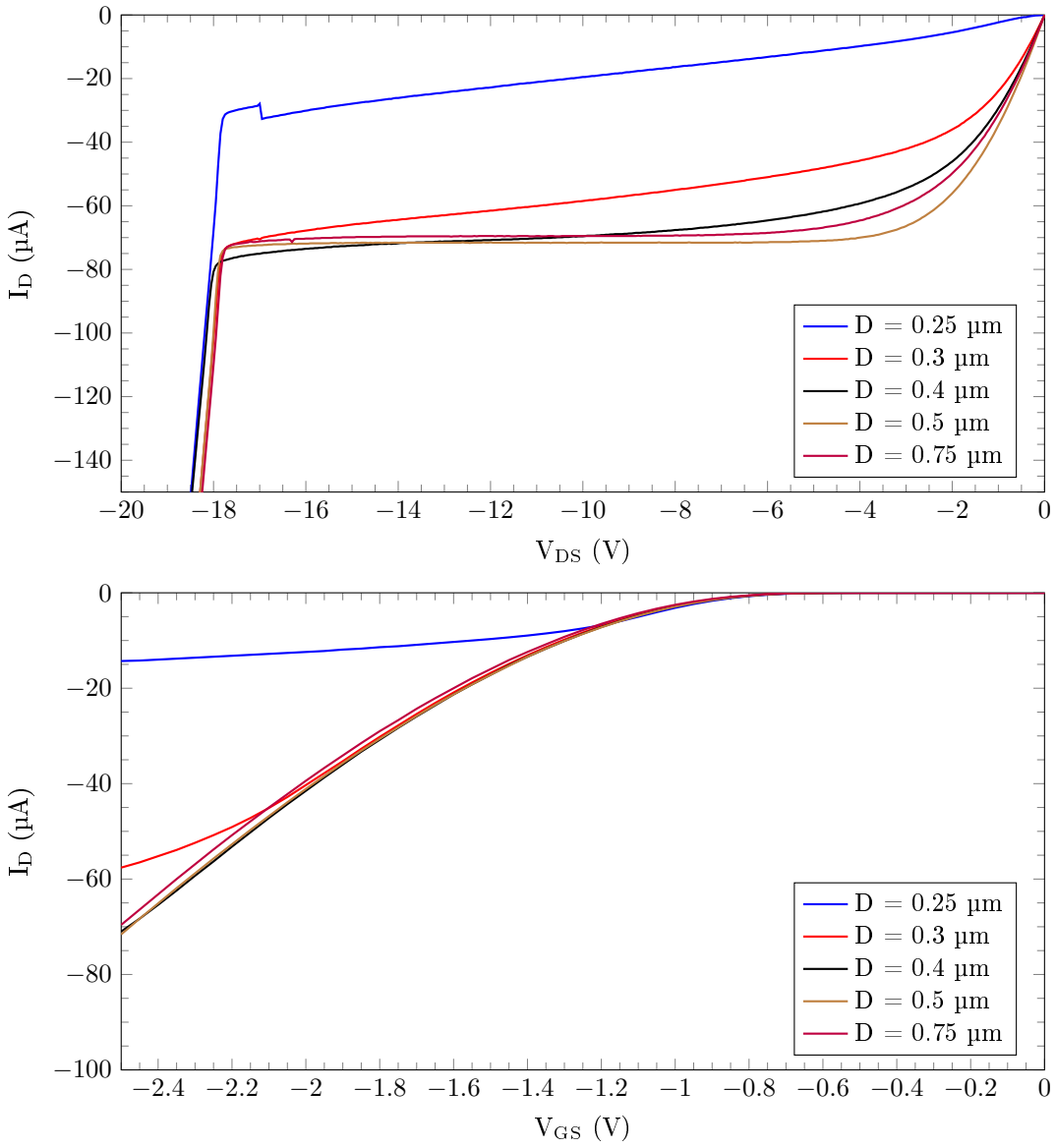


Figure 7.13: V_{DS}-I_D characteristics of STI-based PDMOSTs with different gate step locations D at $V_{GS} = -2.5\,V$ and V_{GS}-I_D characteristics at $V_{DS} = -10\,V$. For all cases W = 1.3 µm and L = 1 µm.

7.5 Discussion and Conclusion of the DMOSTs

DMOSTs were successfully implemented and comply with the minimum 5 V drain-source breakdown voltage without increasing the threshold voltage. The breakdown voltages for DMOSTs with default parameters are listed in Table 7.4. A strong dependence was found between the breakdown voltage of the NDMOST and the gate length. The breakdown is therefore presumed due to a total depletion of the channel, which can be mitigated with longer gates in the second design iteration.

The effectiveness of the step-gate location in SOX-based NDMOSTs was proven by measurements with the source left open. Negative values of D are preferable for SOX-based variants

to obtain a gate oxide breakdown voltage of $V_{DB} = 18\,V$ at $V_{GB} = 0\,V$. In the second design iteration, more negative values of D are proposed to possibly further raise the breakdown voltage and find the point where the threshold voltage changes. Furthermore, by removing the buried n from underneath the drain, the drain-bulk breakdown voltage should increase.

Table 7.4: Breakdown voltages of DMOSTs with $W = 1.3\,\mu m$ and $L = 1\,\mu m$.

	$V_{DS,bd}$	
type	$V_{GS} = 0\,V$	$\lvert V_{GS}\rvert = 2.5\,V$
SOX-based NDMOST	8 V	8 V
STI-based NDMOST	11 V	8 V
SOX-based PDMOST	−15 V	−18 V
STI-based PDMOST	−18 V	−18 V

High breakdown voltages were observed for the fabricated PDMOSTs. The STI-based PDMOSTs had higher drain-source resistances R_{on} than the SOX-based PDMOSTs (25 kΩ versus 15 kΩ). This can be explained by the cutout of the drain p-well by the STI in combination with the bulk deep n-well underneath. A shallow drain connection then remains which imposes a high drain resistance. The difference in R_{on} is less obvious in the NDMOSTs (3.0 kΩ versus 2.9 kΩ) as a low-ohmic buried n layer is present below the drain n-well.

More negative values of D are also proposed for the PDMOSTs as no shift in threshold voltage was observed for the measured devices.

Chapter 8

Improved Double-Diffused MOS Transistors

The DMOSTs designed and measured in Chapter 7 were found to be functional. Improvements on these devices are described in this chapter and were fabricated in the second production cycle. The measurements results are also presented and discussed in this chapter.

Custom mask scripting was available for this design iteration which enabled removing the buried n from underneath the n-well. This was expected to increase the drain-bulk breakdown voltage. The top views, cross-sections and parameter definitions are therefore equal to those from Chapter 7, but the buried n is removed for all configurations.

8.1 Varied Parameters of the Improved DMOSTs

A major improvement for the NDMOST was the gate elongation. Where 1 µm was not found sufficiently long, up to 2 µm was created in this iteration. As depletion region size only scales proportional to the square root of the voltage, sufficient source-drain breakdown voltage was expected with L = 1.5 µm and is therefore chosen as default size. Furthermore, a relation was found between the transistor width and the breakdown voltage in Chapter 7. To further analyze this, a 9.3 µm wide transistor was created.

It was found that higher breakdown voltages are obtained for negative values of D. Therefore, more negative values were created to find the minimum value of D before the threshold voltage shifts. The varied parameters of the SOX-based NDMOST are listed in Table 8.1.

Table 8.1: Varied parameters of the SOX-based NDMOST, changing only one parameter at a time while keeping the default value (in bold) for the remaining parameters. This yields 9 variants in total.

Parameter	Value (µm)				
Width (W)	**1.3**	2.9	9.3		
Gate length (L)	1.25	**1.5**	2		
Step-gate position (D)	**0**	-0.15	-0.25	-0.35	-0.5

The STI-based NDMOST had comparable characteristics as the SOX-based NDMOST, including short gate effects and a correlation between transistor width and breakdown voltage. As the mechanisms driving these effects were presumably equal, less variations were created for the STI-based NDMOST. Variants with lower values of D were created since D = 0.5 µm did not sufficiently protect the gate in the first iteration. The varied parameters of the STI-based NDMOST are listed in Table 8.1.

Table 8.2: Varied parameters of the STI-based NDMOST, changing only one parameter at a time while keeping the default value (in bold) for the remaining parameters. This yields 4 variants in total.

Parameter	Value (µm)		
Width (W)	**1.3**		
Gate length (L)	**1.5**	2	
Step-gate position (D)	**0.3**	0.4	0.5

Both the STI-based and SOX-based PDMOST were found functional and capable of handling high drain-source voltages. The STI-based variations were implemented with the proven parameter set of W = 1.3 µm, D = 0.5 µm and L of either 0.5 µm or 1 µm. The SOX-based variations from Table 8.3 were derived from the SOX-based NDMOST variants.

Table 8.3: Varied parameters of the SOX-based PDMOST, changing only one parameter at a time while keeping the default value (in bold) for the remaining parameters. This yields 8 variants in total.

Parameter	Value (µm)				
Width (W)	**1.3**	2.9	9.3		
Gate length (L)	**0.5**	1			
Step-gate position (D)	**0**	-0.15	-0.25	-0.35	-0.5

8.2 Measurements of the Improved DMOSTs

The Agilent HP 4155A semiconductor parameter analyzer was used to perform these DC measurements at wafer level. The SOX and STI-based variants are compared for the NDMOS and PDMOS transistors. The characterization results of all fabricated transistors are listed in Appendix A.

8.2.1 Measurements of the Improved NDMOST

A general V_{DS}-I_D characteristics comparison between the SOX-based and STI-based NDMOSTs for various gate lengths is given in Figure 8.1.

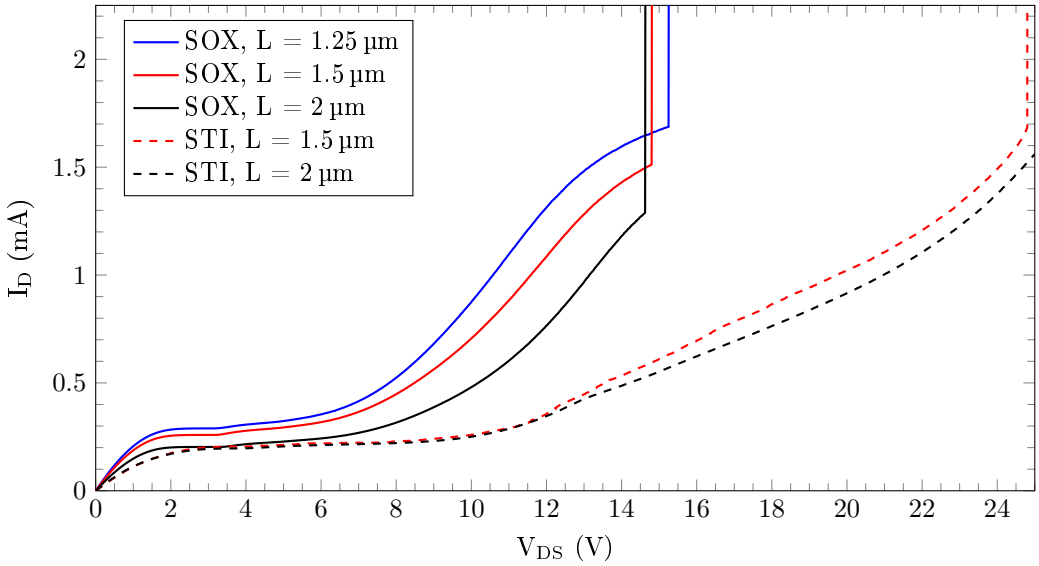


Figure 8.1: V_{DS}-I_D characteristics of NDMOSTs at V_{GS} = 2.5 V. For all cases W = 1.3 µm, D = 0 µm (SOX), 0.4 µm (STI).

Measurements of the Improved SOX-based NDMOSTs

For the SOX-based NDMOST, the gate step location D was varied between 0 µm and −0.5 µm, meaning that the SOX overlaps with the channel. The V_{GS}-I_D and V_{DS}-I_D characteristics of these devices are depicted in Figure 8.2. The device with D = −0.5 µm has an increased threshold voltage compared to the other devices. It changed from the default 0.44 V to 0.65 V which means that the SOX overlaps with the channel too much. The saturation current then changes with the threshold voltage.

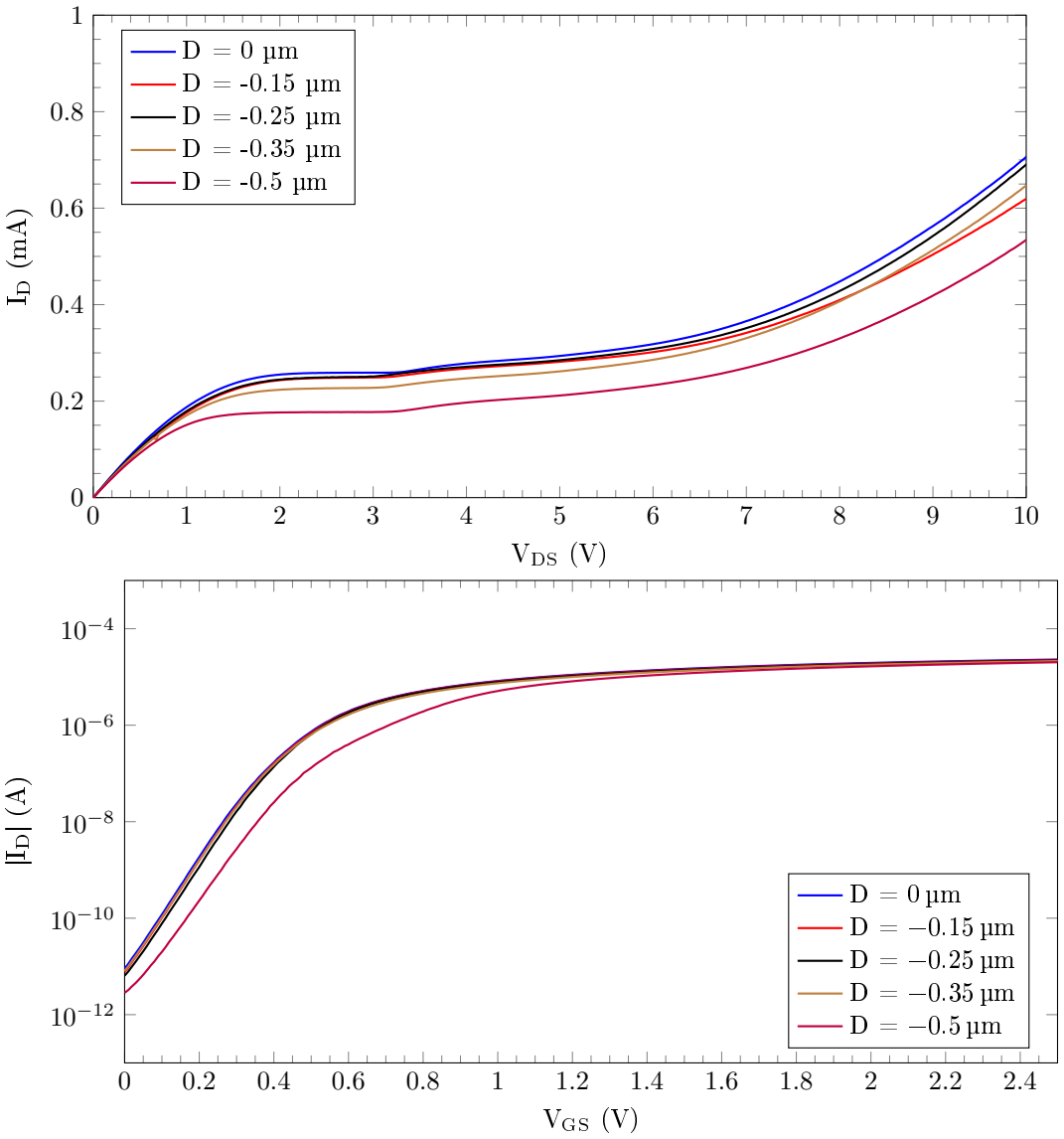


Figure 8.2: V_{DS}-I_D characteristics at V_{GS} = 2.5 V and V_{GS}-I_D characteristics at V_{DS} = 0.1 V of SOX-based NDMOSTs with different values of D. For all cases W = 1.3 µm and L = 1.5 µm.

For higher drain-source voltages, the drain current increases exponentially for all variants, see Figure 8.2. Apart from linear channel length modulation, the drain current in the saturation region remains constant in the standard first-order transistor model. The drain, bulk and gate current curves are plotted in Figure 8.4 and indicate impact ionization in the channel. At the drain side, the electric field is sufficiently high to facilitate the creation of an electron-hole pair. The electron enters the drain, along the strong electric field. The hole is swept to the negatively charged substrate and appears as a substrate current. Due to the high bulk impedance, the bulk voltage increases which lowers the threshold voltage through the body effect. Consequently, the drain current increases as illustrated by the drain current equation in the saturation region of an NMOST from Equation (8.1).

$$I_D = \frac{k_n}{2}\frac{W}{L}\left[(V_{GS} - V_T)^2(1 + \lambda V_{DS})\right] \tag{8.1}$$

Just before hard oxide breakdown, the bulk current is approximately 100 µA and with an estimated bulk impedance of 10 kΩ the bulk voltage becomes 1 V. The bulk-source junction is in forward bias and conducts significant current at this point. This keeps the bulk voltage under 1 V while the largest part of the current flows into the source at high V_{DS}. These current flows are illustrated in Figure 8.3.

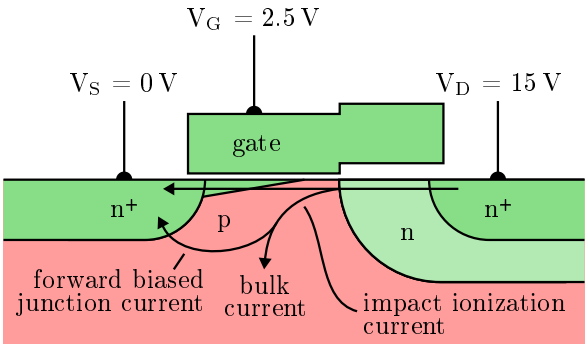


Figure 8.3: NDMOST current flow illustration at $V_{GS} = 2.5\,V$, $V_{DS} = 15\,V$ and $V_{BS} = 0\,V$.

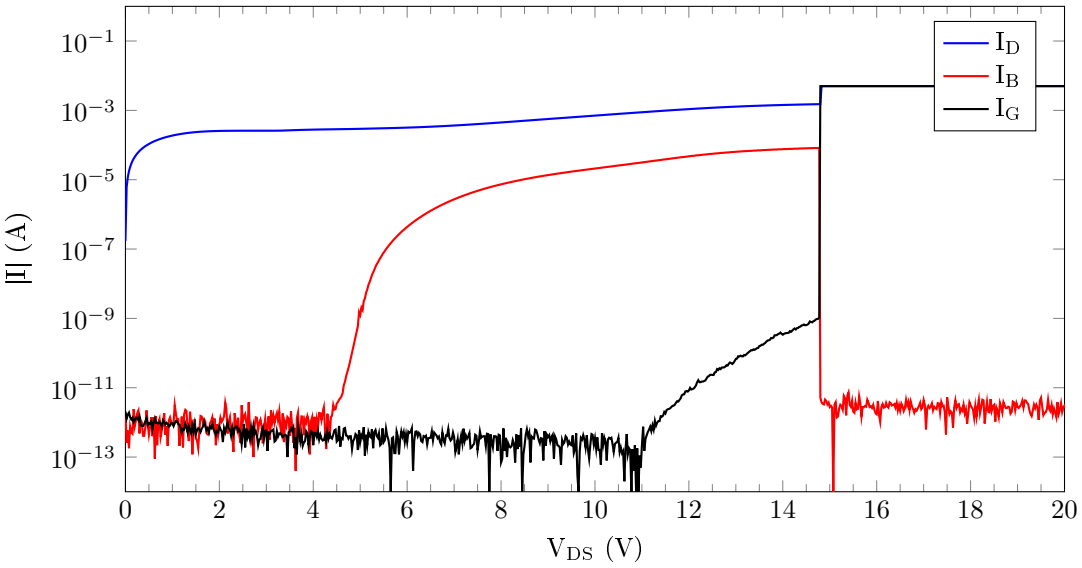


Figure 8.4: Terminal currents over V_{DS} at $V_{GS} = 2.5\,V$ for a SOX-based NDMOST with D = 0 µm, W = 1.3 µm and L = 1.5 µm.

When the transistor is off, e.g. $V_{GS} = 0\,V$, the hard oxide breakdown voltage is lower than at $V_{GS} = 2.5\,V$ in all measured devices. A current from drain to source builds up from $V_{DS} = 4\,V$, without any current through the other terminals. This effect fits drain-induced barrier lowering which lowers the threshold voltage. The V_{GS}-I_D curve for various V_{DS} from Figure 8.6 also indicates strong drain-induced barrier lowering. This short-channel effect can be mitigated with longer gates, but identical results are obtained for L = 1.25 µm, 1.5 µm and 2 µm.

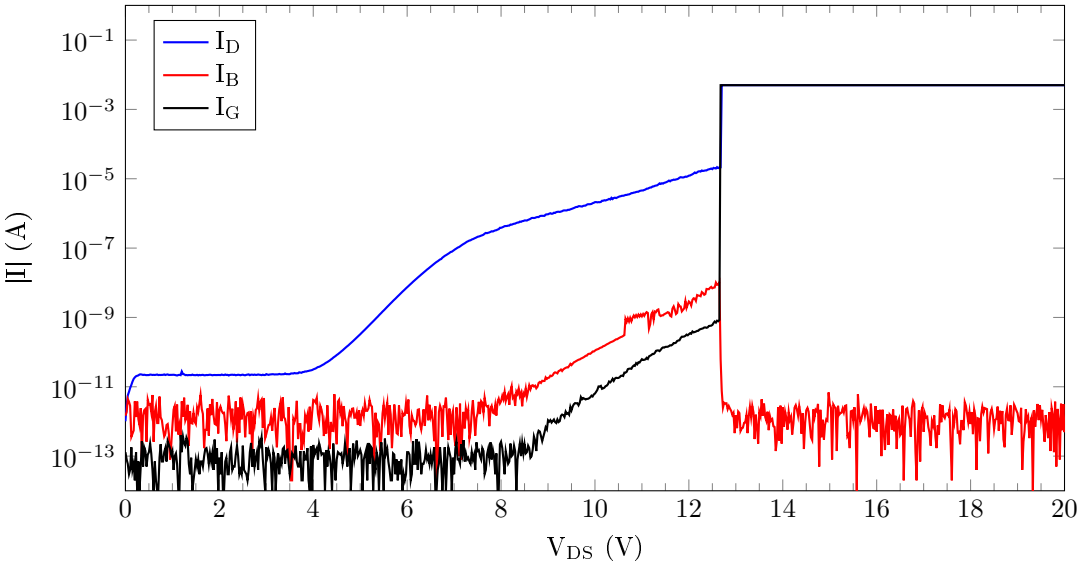


Figure 8.5: Terminal currents over V_{DS} at $V_{GS} = 0\,V$ for a SOX-based NDMOST with $D = 0\,\mu m$, $W = 1.3\,\mu m$ and $L = 1.5\,\mu m$.

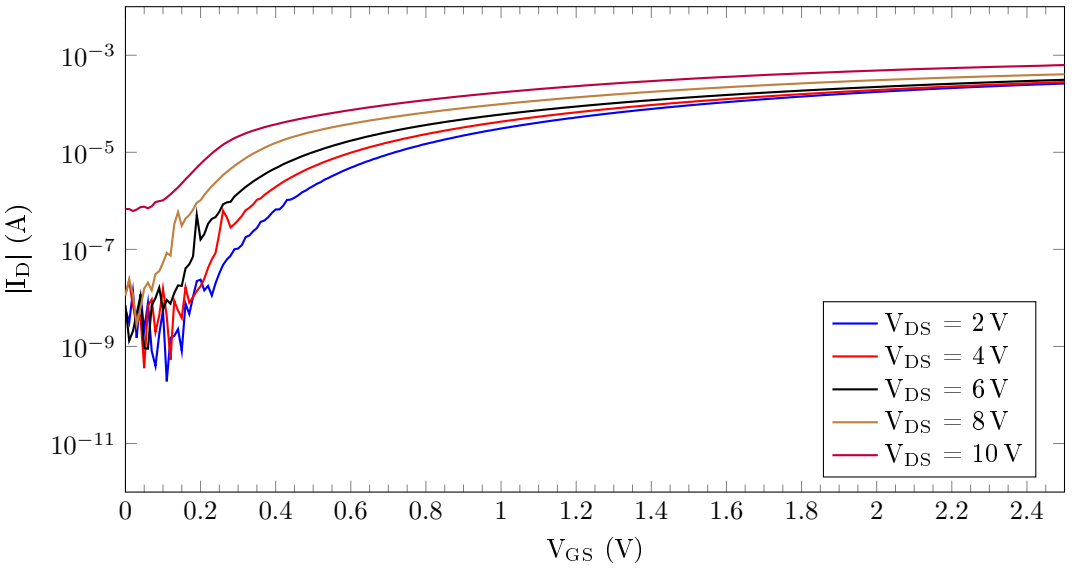


Figure 8.6: V_{GS}-I_D characteristics of a SOX-based NDMOST for varying V_{DS}. Device parameters: $L = 1.5\,\mu m$, $W = 1.3\,\mu m$, $D = 0\,\mu m$.

Measurements of the Improved STI-based NDMOSTs

The V_{DS}-I_D and V_{DS}-I_B characteristics of STI-based NDMOSTs with different gate step locations D are plotted in Figure 8.7. The device with $D = 0.3\,\mu m$ has a high drain resistance as little drain n-well remains between the STI and the p-well channel. The higher drain resistance lowers the voltage over the channel, consequently lowering the electric field too. Impact ionization then occurs at a higher V_{DS} as seen in the V_{DS}-I_B curve from Figure 8.7. However, this does not match the V_{DS}-I_B curve for $D = 0.4\,\mu m$ which shifts without changes to the V_{DS}-I_D curve.

At $V_{GS} = 0\,V$, the drain-source leakage effect observed for the SOX-based NDMOST was not found as severe for the STI-based variants, see Figure 8.8. At $V_{DS} = 14\,V$ only 1 nA of drain current was measured for the variant with $W = 1.3\,\mu m$, $L = 1.5\,\mu m$ and $D = 0.3\,\mu m$.

Abrupt and strong breakdown occurs at $V_{DS} = 18\,V$ between the drain and bulk, but is not initially destructive. Two V_{DS}-I_D sweeps at $V_{GS} = 2.5\,V$ results in identical plots, meaning that no permanent damage occurs at $V_{DS} = 25\,V$ within the millisecond to second time-scale of the measurement.

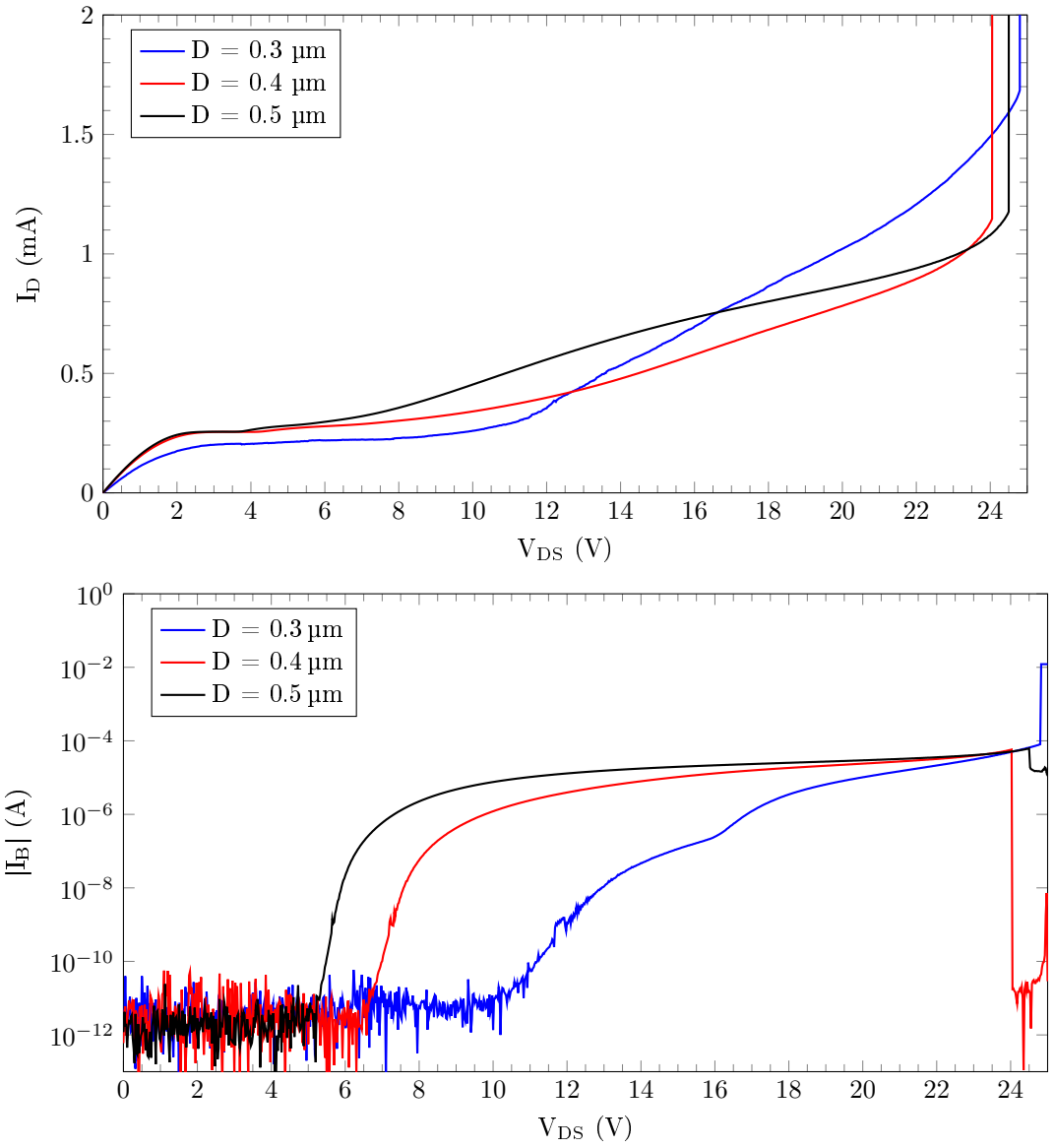


Figure 8.7: V_{DS}-I_D and V_{DS}-I_B characteristics for STI-based NDMOSTs with different values of D at $V_{GS} = 2.5\,V$. For all cases $W = 1.3\,\mu m$ and $L = 1.5\,\mu m$.

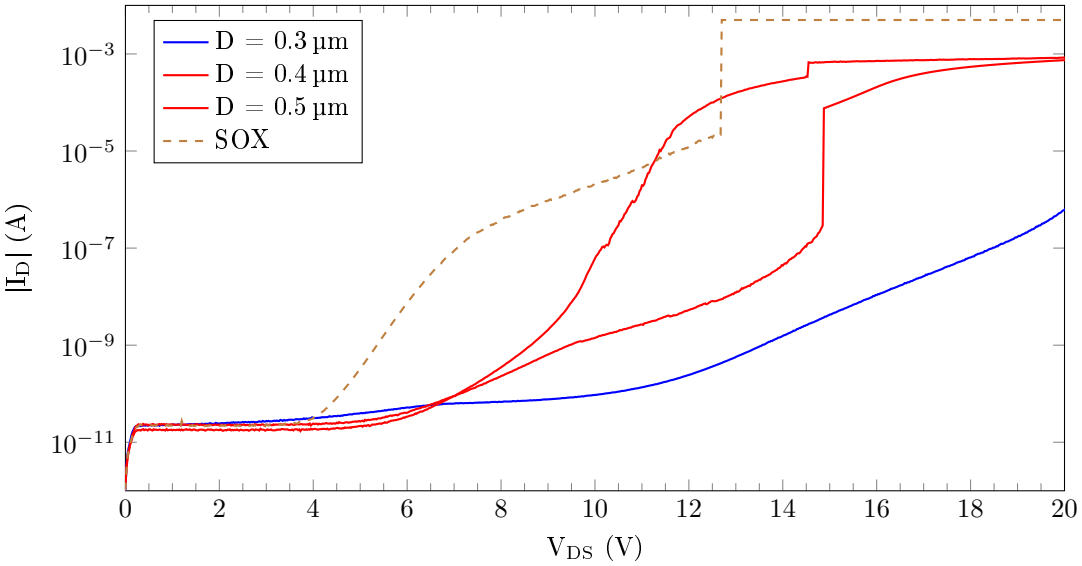


Figure 8.8: V_{DS}-I_D characteristics of STI-based NDMOSTs with different gate lengths at V_{GS} = 0 V. For these devices W = 1.3 µm and D = 0.3 µm. The SOX-based NDMOST with W = 1.3 µm, L = 1.5 µm and D = 0 µm is added as reference.

8.2.2 Measurements of the Improved PDMOSTs

The V_{DS}-I_D characteristics of PDMOSTs with different gate lengths are plotted in Figure 8.9. The drain resistance of the STI-based devices is considerably higher than of the SOX-based devices. The STI and deep n-well cut out and pinch the remaining p-well which results in a relatively high-ohmic connection.

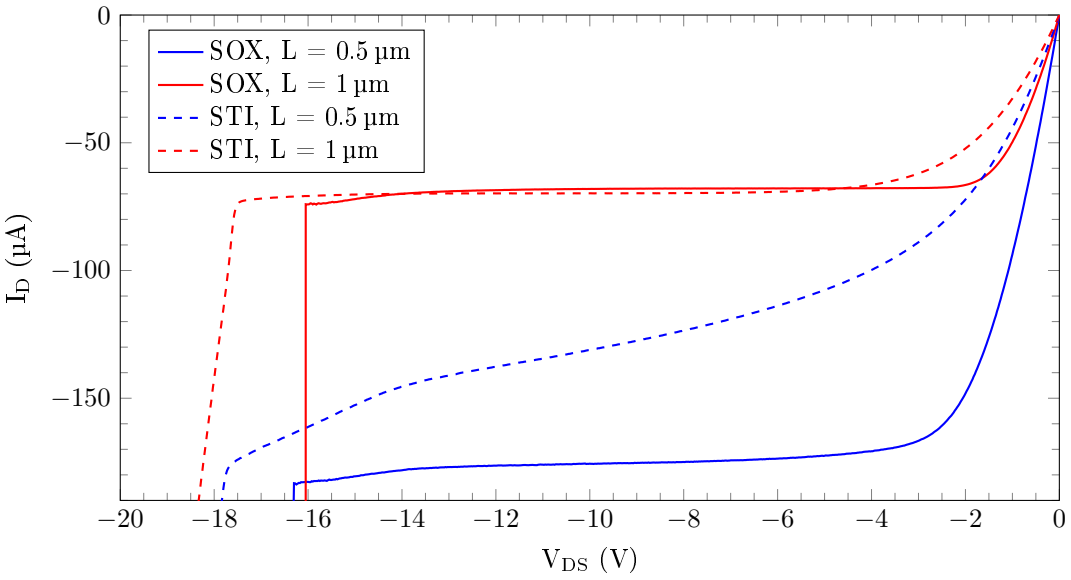


Figure 8.9: V_{DS}-I_D characteristics of PDMOSTs with different gate lengths. For all cases W = 1.3 µm, D = 0 µm (SOX), 0.5 µm (STI).

Measurements of the Improved SOX-based PDMOSTs

The gate step location D was varied in the SOX-based PDMOST layout. The SOX is located up to the drain-channel junction or partially overlaying the channel. From the V_{DS}-I_D and V_{GS}-I_D characteristics plotted in Figure 8.10 can be seen that the saturation current and threshold voltage shift for D = −0.5 µm compared to the other devices. The threshold voltage then changes from −0.66 V to −0.85 V which indicates that the SOX overlaps too much with the channel.

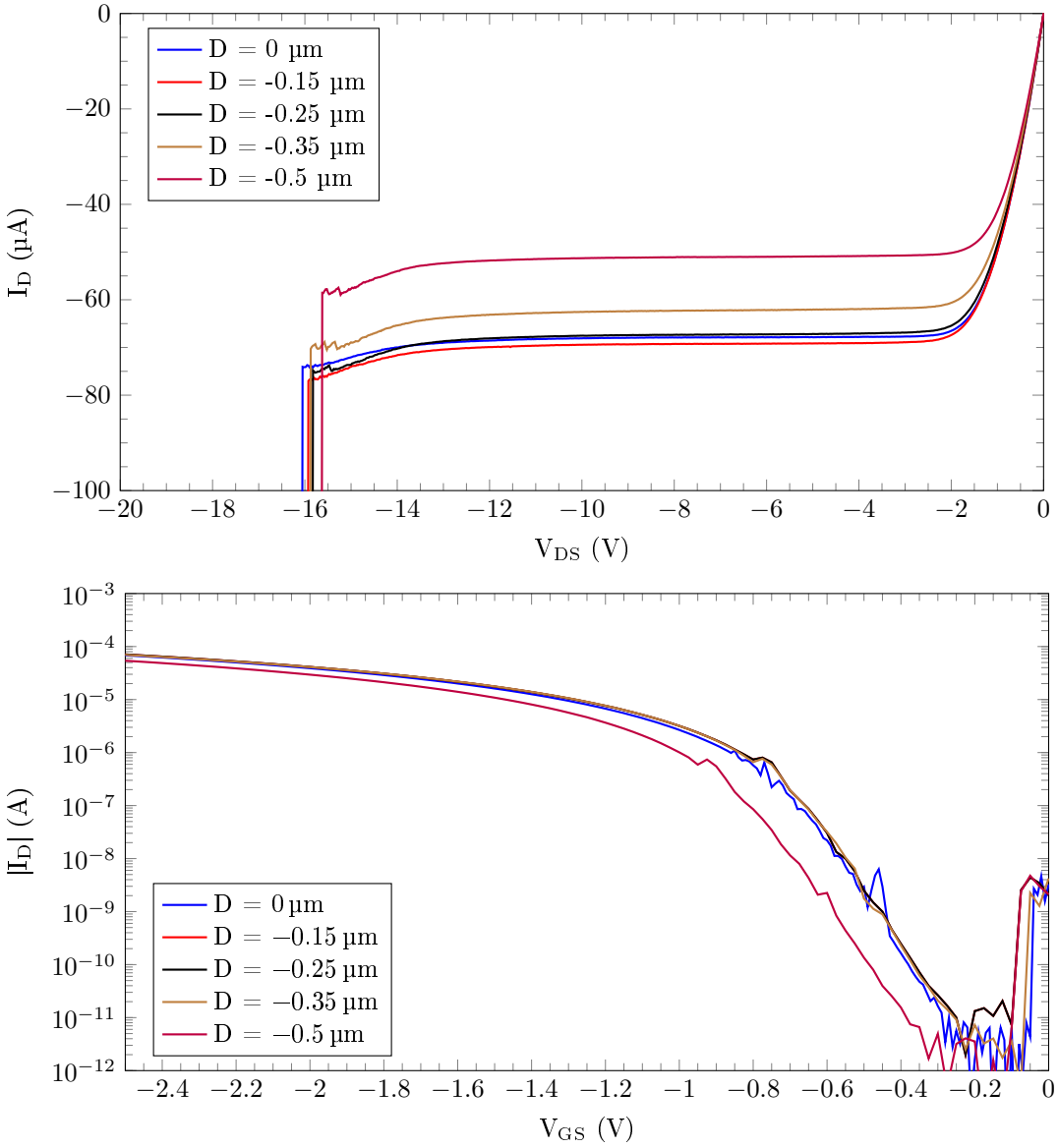


Figure 8.10: V_{DS}-I_D characteristics at V_{GS} = −2.5 V and V_{GS}-I_D characteristics at V_{DS} = −5 V of SOX-based PDMOSTs with different values of D. For all cases L = 1 µm and W = 1.3 µm.

In contrast to the NDMOST V_{DS}-I_D curves, the PDMOST V_{DS}-I_D curves are almost constant in the saturation region as seen in Figure 8.10. Impact ionization occurs in these devices too, see Figure 8.11, but the bulk is connected with a lower impedance which prevents the

bulk voltage from changing.

The V_{DS}-I_B curve at $V_{GS} = 0\,V$ from Figure 8.11 indicates drain-bulk leakage from $V_{DS} = -5\,V$. This leakage is also observed when performing a drain-bulk voltage sweep with source and gate open. The leakage then remains under 1 µA until abrupt breakdown occurs at $-18\,V$. The hard gate breakdown at $V_{DS} = -16\,V$ ($V_{GS} = -2.5\,V$) and $V_{DS} = -13\,V$ ($V_{GS} = 0\,V$) are therefore not expected to be due to drain-bulk breakdown. Instead, direct breakdown of the gate SOX is presumed. Gate leakage starts to increase from $V_{DG} = -8\,V$ to about $I_G = 100\,nA$ at $V_{DG} = -13\,V$ just before hard oxide breakdown for both $V_{GS} = -2.5\,V$ and $0\,V$.

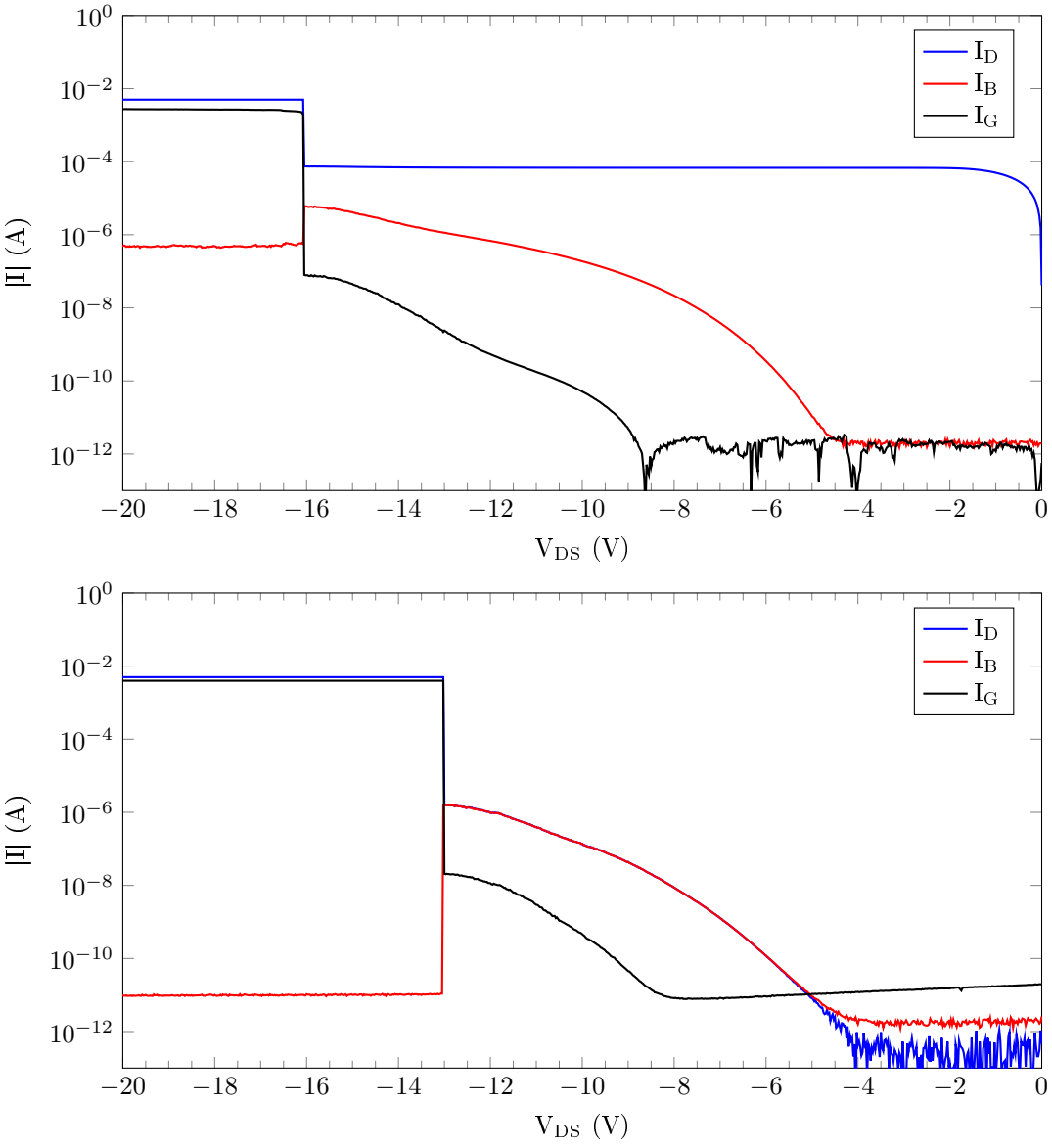


Figure 8.11: Terminal currents versus I_D of the SOX-based PDMOST with D = 0 µm, W = 1.3 µm and L = 1 µm at $V_{GS} = -2.5\,V$ (top) and $V_{GS} = 0\,V$ (bottom).

Measurements of the Improved STI-based PDMOSTs

The breakdown voltage of the STI-based PDMOST is considerably higher than of the SOX-based PDMOST at both $V_{GS} = 0\,V$ and $V_{GS} = -2.5\,V$, see Figure 8.12. Hard gate oxide breakdown did not occur for these V_{DS}-I_D sweeps and the characteristics did not change either. At $V_{DS} = -18\,V$, abrupt drain-bulk breakdown occurs and raises the drain current noticeably.

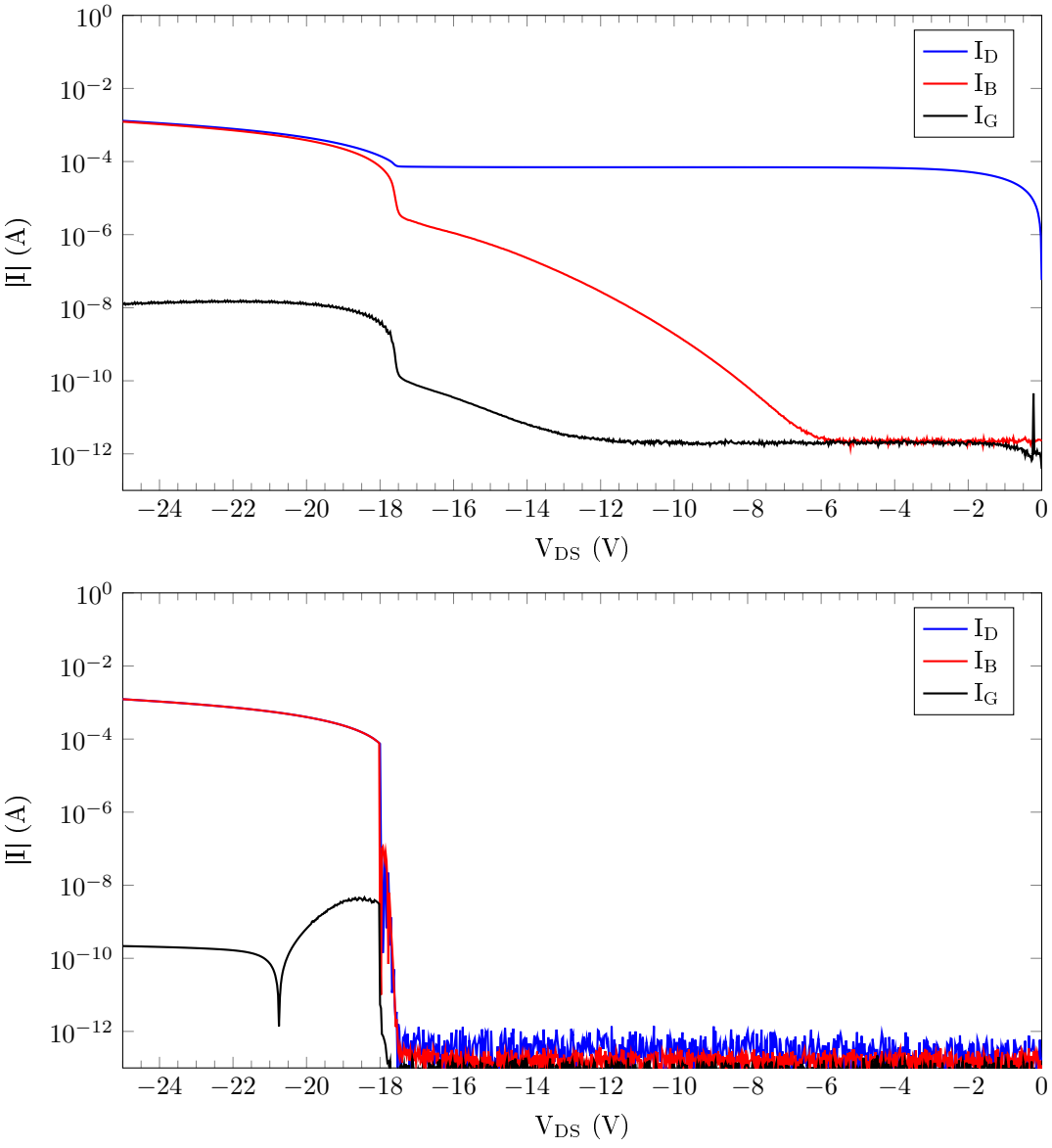


Figure 8.12: Terminal currents versus I_D of the STI-based PDMOST with D = 0.5 µm, W = 1.3 µm and L = 1 µm at $V_{GS} = -2.5\,V$ (top) and $V_{GS} = 0\,V$ (bottom).

8.3 Discussion of the Improved DMOSTs

The breakdown voltages of the STI-based DMOSTs were measured to be higher than of the SOX-based DMOSTs. For the PDMOST it was found to be caused by the breakdown of SOX at $V_{DG} = -13\,V$. This imposes a hard limit to the achievable breakdown voltage of SOX-based transistors. Gate leakage above 10 pA was observed from $V_{DG} = -8\,V$. Additional reliability tests have to be performed to determine the time-dependent dielectric breakdown properties.

The STI-based DMOSTs have higher breakdown voltages as they feature thicker oxide than the SOX-based DMOSTs. As a downside, the drain-resistances are higher for these transistors; $R_{on} = 5.8\,k\Omega$ versus $4.9\,k\Omega$ for $W/L = 1.3\,\mu m/1\,\mu m$ NDMOSTs and $R_{on} = 31\,k\Omega$ versus $16\,k\Omega$ for $W/L = 1.3\,\mu m/1.5\,\mu m$ PDMOSTs.

The drain-bulk breakdown voltage of neither the NDMOST or the PDMOST increased by removing the buried n from underneath the n-well. The drain-bulk breakdown is thus primarily caused by the n-well and p-well. Adding the buried n lowers the drain resistance for the NDMOST and is therefore preferred. The buried p may presumably also be added underneath the drain p-well without reducing the breakdown voltage in the PDMOST. When no buried n would be used for the bulk, lower drain resistance would be obtained without compromising the breakdown voltage.

Due to the high NDMOST bulk impedance, the bulk current caused by impact ionization raises the bulk voltage significantly. By reducing the bulk impedance, the drain current in the saturation region will remain more constant, as demonstrated for the PDMOST. This could be done by creating a bulk connection within the deep trenches.

Thick-oxide transistors can be created by adding SOX to the entire gate oxide surface. When the threshold voltage is sufficiently below 5 V, these transistors can be used in the target application of high-voltage digital signal driver. In the circuit from Figure 2.9, the cross-coupled low-voltage PMOST pair and their cascoding PJFETs can then be replaced with thick-oxide PMOS transistors.

8.4 Conclusion of the Improved DMOSTs

Custom mask scripting enabled removing the buried n from underneath the n-well in the second iteration of DMOSTs. However, this did not noticeably increase the breakdown voltages but increased the drain resistances instead.

For the target application where a 5 V transistor is required, the most suitable devices and their specifications are as follows:

- STI-based NDMOST with $W = 1.3\,\mu m$, $L = 1.5\,\mu m$, $D = 0.4\,\mu m$:
  - $V_{BD} = 14.425\,V$ at $V_{GS} = 0\,V$
  - $V_{BD} = 24.175\,V$ at $V_{GS} = 2.5\,V$
  - $R_{on} = 5.797\,k\Omega$
  - $I_{D,sat} = 250\,\mu A$
  - $V_T = 0.42\,V$
- SOX-based PDMOST with $W = 1.3\,\mu m$, $L = 0.5\,\mu m$, $D = 0\,\mu m$:

  - $V_{BD} = -10.05\,V$ at $V_{GS} = 0\,V$
  - $V_{BD} = -15.75\,V$ at $V_{GS} = 2.5\,V$
  - $R_{on} = 19.968\,k\Omega$
  - $I_{D,sat} = -165\,\mu A$
  - $V_T = -0.62\,V$

When voltage ratings over 5 V should be achieved, the most suitable devices and their specifications are as follows:

- STI-based NDMOST with W = 1.3 µm, L = 1.5 µm, D = 0.3 µm:
  - $V_{BD} = 19.35\,V$ at $V_{GS} = 0\,V$
  - $V_{BD} > 25\,V$ at $V_{GS} = 2.5\,V$
  - $R_{on} = 7.646\,k\Omega$
  - $I_{D,sat} = 197\,\mu A$
  - $V_T = 0.41\,V$
- STI-based PDMOST with W = 1.3 µm, L = 1 µm, D = 0.5 µm:
  - $V_{BD} = -17.8\,V$ at $V_{GS} = 0\,V$
  - $V_{BD} = -18.225\,V$ at $V_{GS} = 2.5\,V$
  - $R_{on} = 30.649\,k\Omega$
  - $I_{D,sat} = -34\,\mu A$
  - $V_T = -0.66\,V$

The majority of the DMOSTs deal with considerable impact ionization. For STI-based NDMOSTs, the impact ionization decreases significantly when the distance from bulk-drain junction to the gate step location decreases. More research is required to find the cause of this phenomenon. Furthermore, the NDMOST may be improved with respect to impact ionization by implementing an n- epi extended drain in future work.

The target application may be realized with only DMOSTs if a SOX-based thick-oxide PMOS transistor can be created. The threshold voltage of this transistor should be sufficiently under 5 V to properly function as cross-coupled PMOST pair.

Chapter 9

One-Time-Programmable Memory Circuits

Measurement results from the first design iteration were used to design OTP memory circuits. The wide, short Zener diodes were found to break down at low forward bias. After breakdown, a low-ohmic connection between the two terminals was reproducibly obtained. Long, silicidized Zener diodes had similar breakdown in reverse bias, but at a voltage outside specifications.

As a target for improving OTP memory, integration with a flipflop was mentioned in Section 1.1.2. The saved OTP memory bit is then saved into the flipflop when the chip starts up, indicated by the POR signal. Setting the flipflop value is performed with the active-low set signal (SN) and active-low reset signal (RN) and are therefore the outputs of the OTP cell. The data and clock signals remain free to incorporate the flipflop in a shift register. The OTP cell has active-low inputs for reading (RDN), programming (PROGN) and data (QN). At active PROGN, the value of the connected flipflop (QN) is programmed into the OTP cell. At active RDN, the programmed value is read and either SN or RN is activated, effectively storing the value into the flipflop. The inputs, outputs and interconnections are illustrated in Figure 9.1 and the read and write signals in Figure 9.2.

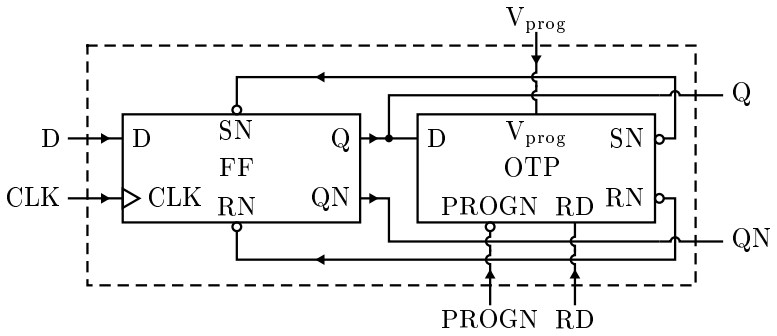
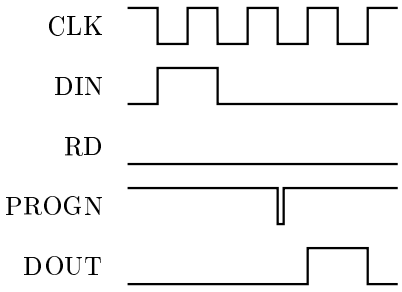
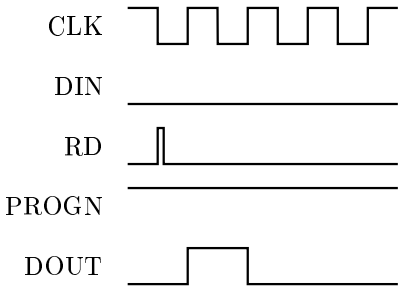


Figure 9.1: Combination of standard flipflop and OTP functionality to create an OTP flipflop.



(a) Write operation of the second OTP flipflop when PROGN is low.



(b) Read operation of all three flipflops when RD is high, this loads the stored value from (a) into the second OTP flipflop.

Figure 9.2: Consecutive signals for write (a) and read (b) operations in a shift register with three OTP flipflops chained. The supply voltage may be turned off between (a) and (b).

Besides the 2.5 V supply voltage V_{DD}, a higher OTP memory programming voltage V_{prog} is required. When not programming the OTP memory, V_{prog} should be connected to either V_{DD} or ground, depending on the OTP memory implementation.

Output glitches on SN and RN are not allowed as that could result in falsely programming the memory bit. This was taken into account when designing the circuit.

9.1 Forward Biased Programmed OTP Memory

The measured 1 µm wide Zener diode had breakdown voltage under 5 V in forward bias. Therefore, the programming transistor was implemented by a 5 V bipolar NPN transistor from the library. This transistor is safe to implement since it is fully characterized and proven, as opposed to the NDMOS transistor. Furthermore, high saturation currents are achieved with these transistors on a relatively small die area. The OTP circuit is depicted in Figure 9.3.

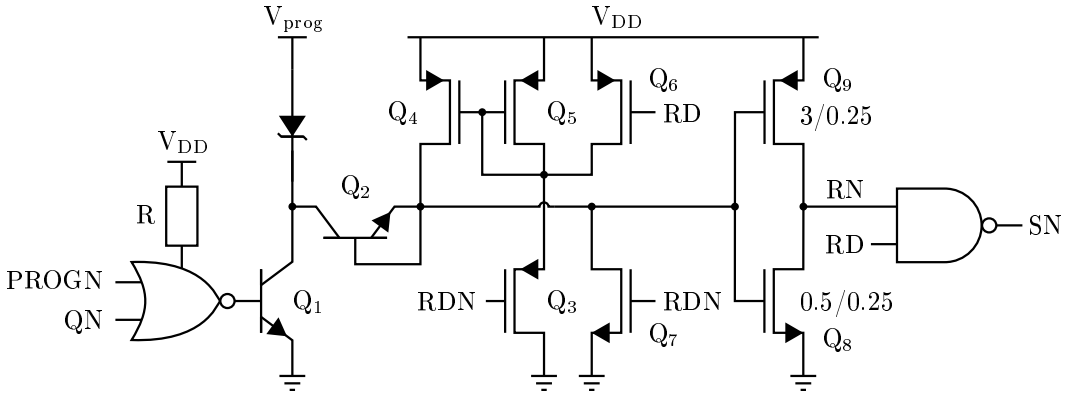
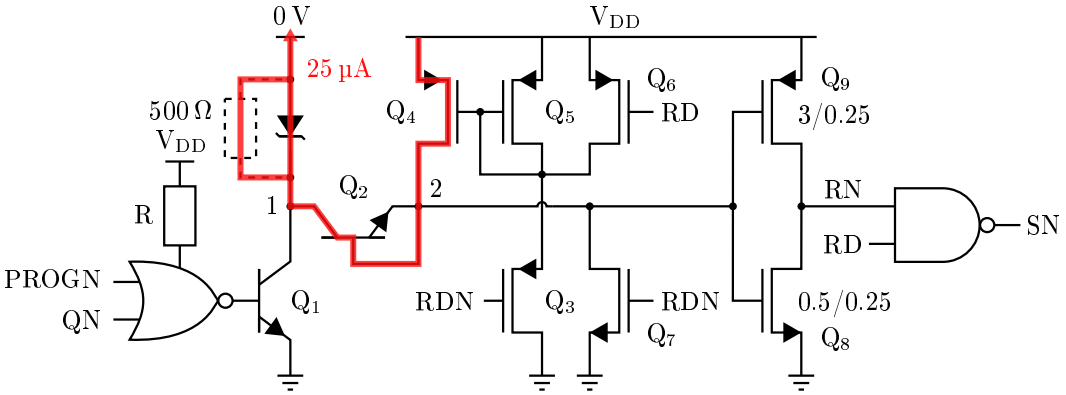
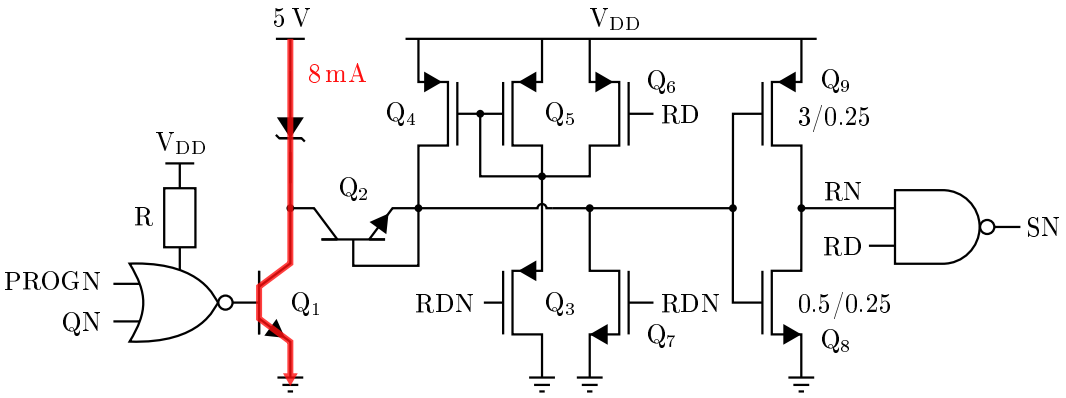


Figure 9.3: OTP circuit for forward biased programming. $V_{prog} = 0$ V while reading.



(a) Read operation when RD is high (and thus RDN low) and $V_{prog} = 0\,V$. After writing the OTP bit, the Zener diode is semi-shorted and can be modeled by adding the $500\,\Omega$ resistor in parallel.



(b) Write operation when PROGN and QN are low and $V_{prog} = 5\,V$.

Figure 9.4: Read (a) and write (b) current paths in the forward biased programmed OTP circuit.

The MOS read circuitry may not be exposed to voltages over 2.5 V, so diode-connected NPN transistor Q_2 and NMOST Q_7 keep the drain node of Q_7 at 0 V outside read mode.

Ideally, the Zener diode is an open or short circuit depending on the memory bit state. This is achieved in reverse bias; negligible current flows at 2.5 V reverse bias by default but after second breakdown, a low-ohmic connection is formed between the two terminals. As programming is in forward bias and reading in reverse bias, the voltage polarity over the diode has to change. Therefore, V_{prog} is connected to ground outside programming mode. The current source consisting of Q_3, Q_4 and Q_5 applies 25 µA into the cathode of the diode in read mode. The voltage drop over the diode then clearly indicates the memory bit state. When programmed, node 1 is at 2.5 V and otherwise nearly 0 V. Diode-connected transistor Q_2 creates a forward voltage drop in the path towards the inverter (Q_8 and Q_9) input at node 2, resulting in a low input state on the inverter that is larger than 0 V. Therefore, NDMOST Q_8 does not turn off entirely in this state, making the output of the inverter smaller than 2.5 V. To minimize this effect, PMOST Q_9 is sized wide compared to Q_8.

9.2 Reverse Biased Programmed OTP Memory

The second breakdown voltage of the Zener diodes was found to exceed 5 V in reverse bias. In addition to the transistors from the library, the newly designed NDMOS transistor was implemented in the OTP circuitry. With small alterations, the NDMOST was estimated to reach a sufficiently high voltage rating for the required reverse biased programming voltage. The OTP circuit is depicted in Figure 9.5.

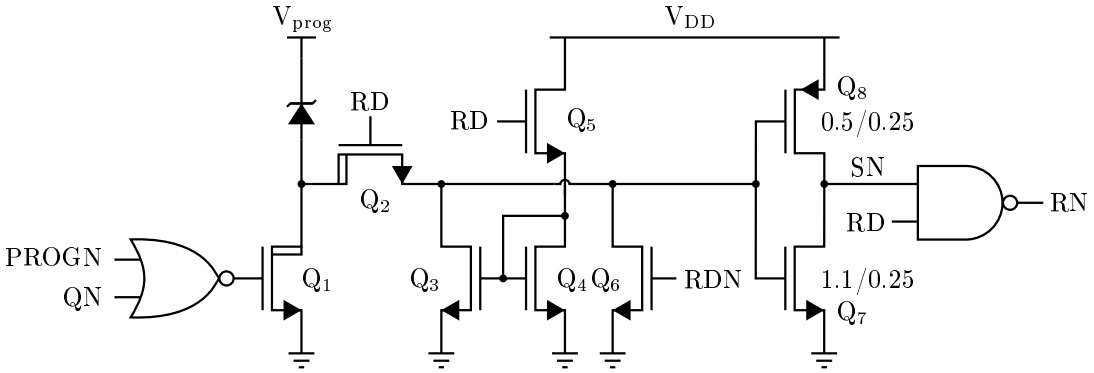
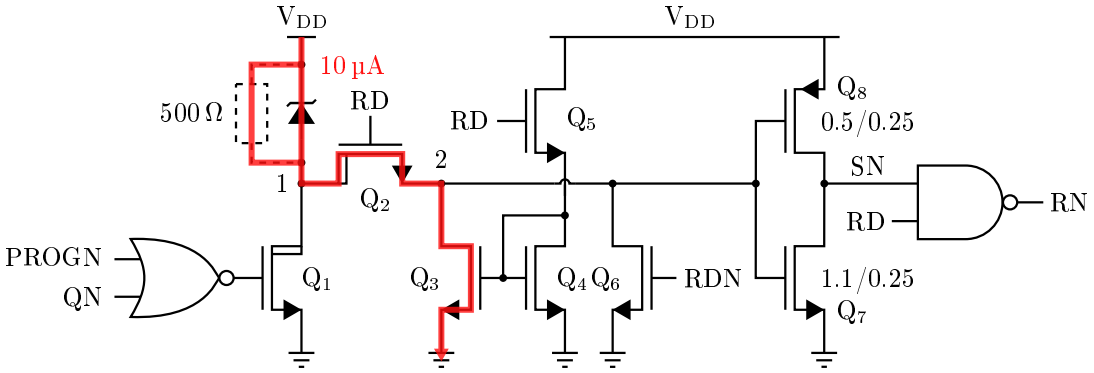
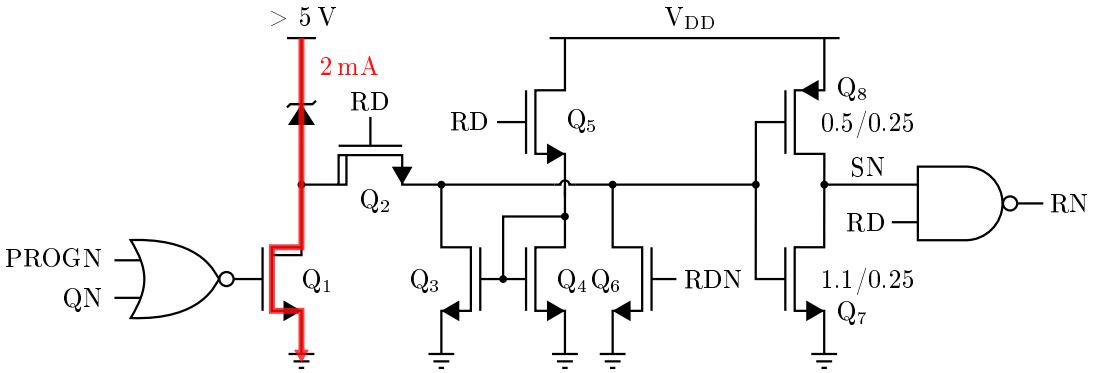


Figure 9.5: OTP circuit for reverse biased programming. $V_{prog} = V_{DD}$ while reading.



(a) Read operation when RD is high (and thus RDN low) and $V_{prog} = V_{DD}$. After writing the OTP bit, the Zener diode is semi-shorted and can be modeled by adding the 500 Ω resistor in parallel.



(b) Write operation when PROGN and QN are low and $V_{prog} > 5$ V.

Figure 9.6: Read (a) and write (b) current paths in the reverse biased programmed OTP circuit.

The currents during read and write mode are illustrated in Figure 9.6. The Zener diode cathode is connected to V_{prog}, which is a high voltage ($> 5\,V$) during programming. The anode is then pulled to ground by the lower DMOST when QN is low. The voltage drop over the Zener diode then exceeds the second breakdown voltage and a high current will flow. To prevent burn-out of the Zener diode, the NDMOST should be properly sized in order to limit the current in the saturation region. The PROGN input pulse length determines the duration of the high-current pulse through the Zener diode.

Outside programming mode, V_{prog} is connected to V_{DD}. Reading is then performed by applying 10 µA into the anode of the Zener diode with the current source of Q_3, Q_4 and Q_5. The voltage drop over the Zener diode then indicates the memory bit value. Before writing the OTP bit, the Zener diode does not conduct in reverse bias, resulting in a voltage of 0 V on node 2. After writing the OTP bit, the Zener diode is semi-shorted which results in a node 1 being around 2.5 V and node 2 around 2 V. Comparable to the circuit of Figure 9.3, the high input state of the inverter (Q_7 and Q_8) is minimally the threshold voltage of DMOST Q_2 lower than V_{DD}. This prevents PMOST Q_8 from turning off entirely, causing SN to never reach 0 V. The effect is mitigated by making Q_7 wide compared to Q_8.

The layouts of the forward and reverse biased programmed OTP flipflops are depicted in Figure 9.7.

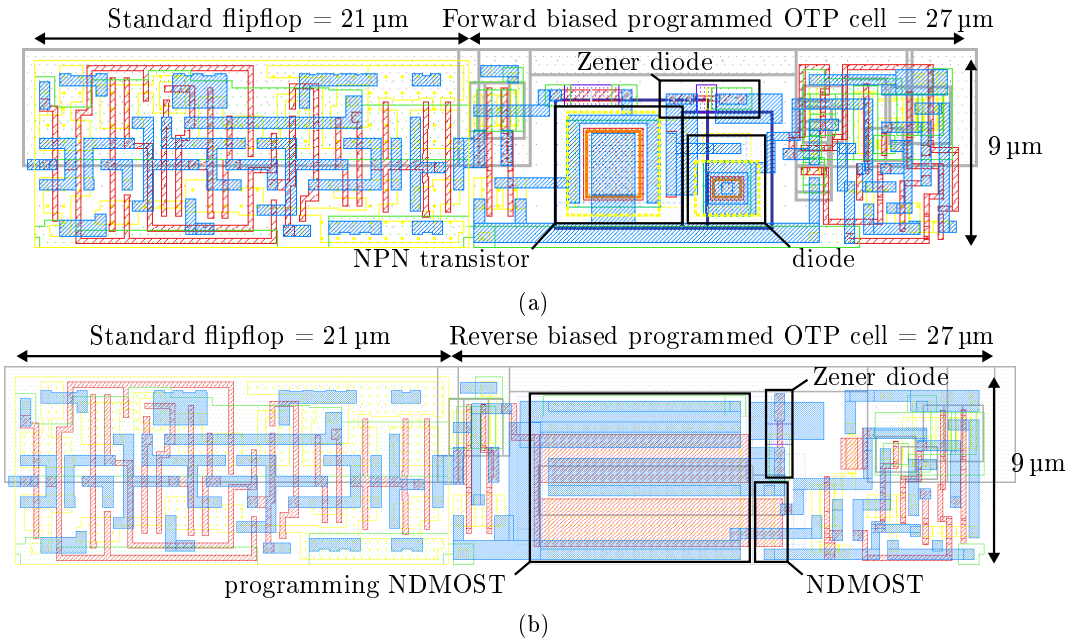


Figure 9.7: Forward (a) and reverse (b) biased programmed OTP flipflop layouts. The high-current variants add 10 µm to the width for both.

9.3 OTP Memory Shift Register

The OTP flipflops are chained in a shift register to reduce the amount of input and output pins. The individual flipflops can be programmed by shifting the desired bit array in and activating the PROGN signal. However, in the test sequence only a single bit is high, effectively programming a single flipflop per PROGN pulse. The current transient can then be measured separately using an oscilloscope and the total current remains limited.

Programming all bits simultaneously would presumably result in unreliable programming due to series resistance in the interconnects.

In Figure 9.8, two OTP flipflops are connected to create an illustrative shift register. The register can be extended indefinitely without clock skew problems. Because the clock propagates in opposite direction to the data, a clock pulse always shifts the register a single flipflop. In the real circuit implementation, longer shift registers with 300 and 396 OTP flipflops are used for forward and reverse biased programming, respectively.

Clocked circuits are known to create current spikes at the clock edges. To prevent the supply voltage from dropping significantly, decoupling capacitors were added distributed over the shift register. Every OTP memory flipflop includes 100 fF decoupling capacitance. Furthermore, Schmitt triggers were placed on the inputs to further mitigate the effects of supply voltage fluctuations.

Buffers were placed throughout the shift register for PROGN, RD and CLK after approximately every 10 flipflops.

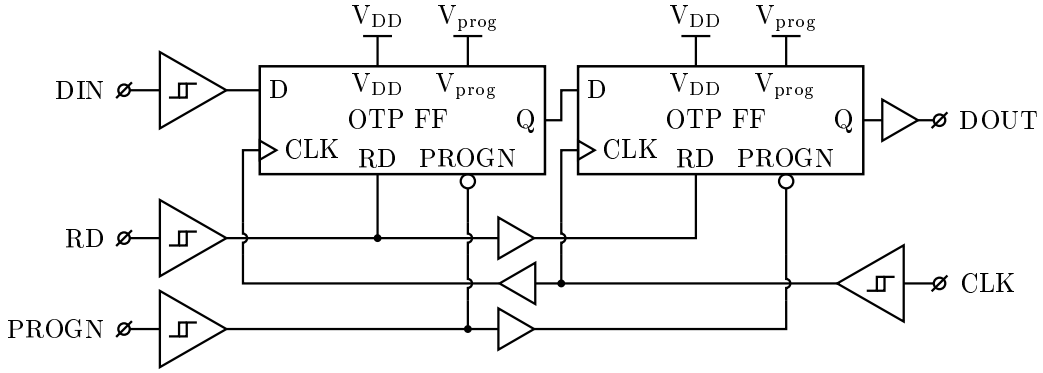


Figure 9.8: Two-flipflop shift register implementing inverted clock propagation direction and signal buffering.

Two OTP flipflop variants were made per Zener variant, a low-current and a high-current version. During and after breakdown, the diodes form a low-ohmic connection, presumably down to 100 Ω during breakdown. The programming transistor should be dimensioned such that it does trigger breakdown in the Zener diode but does not burn it out into an open circuit.

The two OTP cell implementations were implemented in separate shift registers. First, the 5 V forward biased programmed memory should not be exposed to the higher voltage of the reverse biased programmed memory. Second, when a cell is faulty such that the shift register does not work anymore, the other implementation is not affected. Last, it is more convenient for testing to have them accessible separately as the input signals are different.

9.4 OTP Memory Tests

After the wafers were fabricated, measurements were performed at wafer level as well as on packaged dies. In Chapter 4, the improved Zener diodes are described and the wafer-level measurements discussed. These diodes are also implemented in the circuits presented in this chapter and measured after bonding and packaging.

Two OTP memory shift registers were implemented, one being programmed in forward bias

and the other one in reverse bias. A test board was developed to systematically measure the OTP flipflop variants. First, the OTP memory is read and should contain only zeros. Second, the memory is programmed per bit by shifting a single "1" through the register and programming every OTP flipflop it passes. The current is measured and can be traced back to the variant for further investigation. Last, the memory is read again; the bits that were successfully programmed changed from a "0" to a "1". This three-step process is performed for a multitude of I_{lim} to evaluate the minimum programming current.

The National Instruments USB-8452 interface was used as parallel IO port to connect all digital control signals. These signals were generated and read out with custom LabVIEW VIs, see Appendix B. With these VIs, a multitude of read and write operations were available.

9.4.1 OTP Memory Test Setup

A schematic view of the test board is given in Figure 9.9. The packaged chip is placed in a socket on this board and is considered the device under test (DUT). Each DUT contains two shift registers, the forward biased programmed OTP and the reverse biased programmed OTP and can be selected with a switch.

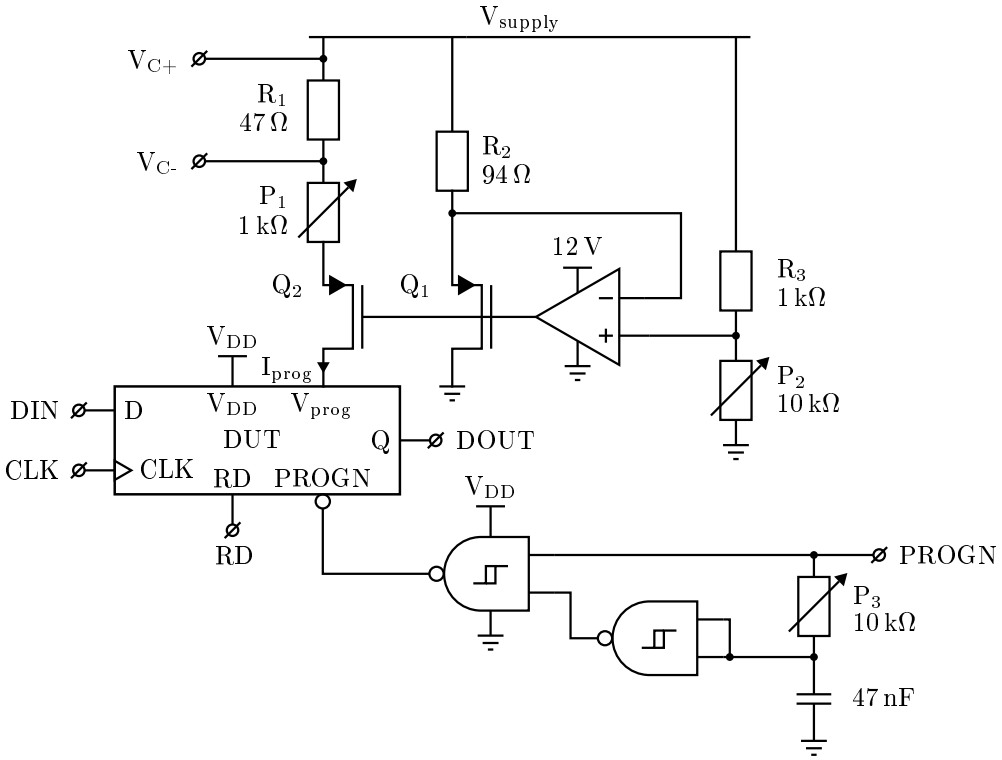


Figure 9.9: Schematic view of the test setup. Only one of the two shift registers is depicted for the DUT.

The USB-8452 cannot create high-frequency digital signals so additional hardware was required to implement the $< 100\,\mu s$ PROGN pulse. By creating a delayed signal with the RC filter, a short pulse is created with the two NAND Schmitt triggers at a rising edge of the PROGN signal from the USB-8452 as described in Section 4.4. The pulse length can be selected with P_3.

The OTP programming supply V_{supply} is limited to a selectable current limit with parallel PMOST pair Q_1 and Q_2 and an opamp. Q_1 is biased by the opamp for a drain current around 10 mA by setting the non-inverting input of the opamp at V_{supply} - 1 V. As the drain of Q_1 is grounded, a maximum for the drain current of Q_2 is also set, but can be linearly scaled with P_1. For every V_{supply}, both potentiometers have to be updated to generate 1 V over R_3 and then the required current limit. When trimming, the V_{prog} connection is shorted to ground to generate the maximum current. The current limit can then be read out as $I_{lim} = (V_{C+} - V_{C-}) / 47\Omega$.

About 2 V is required over Q_2 and the series resistances R_1 and P_1 before the current limit is reached, see Figure 9.10. Therefore, at least 2 V headroom is required for V_{supply} above the breakdown voltage of the Zener diode. During testing, the instantaneous currents can be monitored by an oscilloscope as the voltage drop V_{C+} - V_{C-} over R_1. The test setup is illustrated in Figure 9.11.

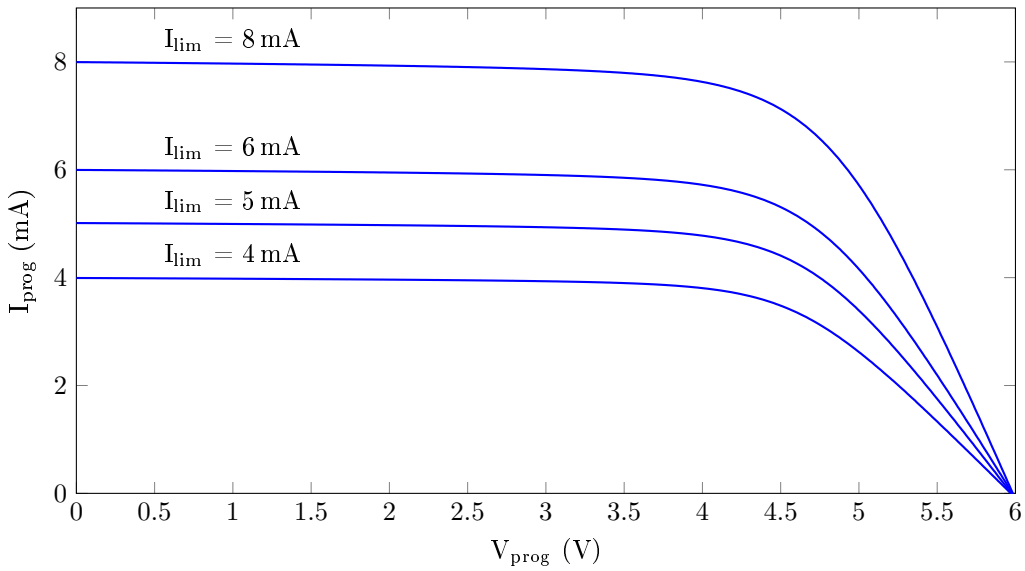


Figure 9.10: Current limiter characteristics of the test board circuit from Figure 9.9 at $V_{supply} = 6$ V for various current limit settings.

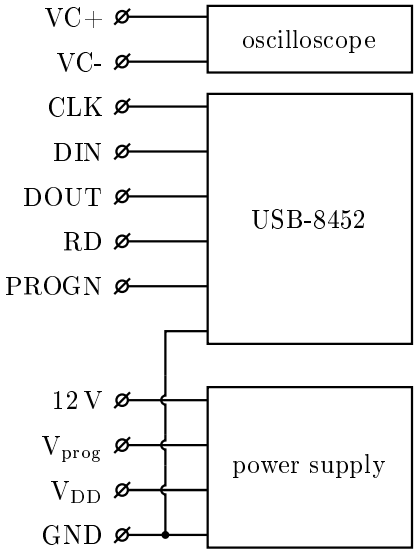


Figure 9.11: Connections from the test board to the digital interface, oscilloscope and power supply.

9.4.2 OTP Memory Tests Results

Before programming memory bits in the shift register, the default values were read. Ideally, all cells output "0" by default, but the cells that implemented Zener diodes with $S \leq 0.4\,\mu m$ occasionally contained "1" when read. Therefore, only cells with $S > 0.4\,\mu m$ were taken into consideration.

After resetting the flipflops to $Q = 0$ by shifting zeros into the shift register, a single "1" was shifted in. At the destination flipflop, PROGN was pulsed, programming a "1" into the single OTP flipflop. To check whether the programming succeeded, a read operation was performed.

Results of the Forward Biased Programmed OTP Memory Tests

Without limiting the programming current it settles at 25 mA at $V_{supply} = 5\,V$. Wider diodes are programmed successfully for this current, but the thinner diodes had unpredictable outcomes as the overly high current burns out the diodes into a semi-open circuit. Therefore, the current limiter from Figure 9.9 was required. The pulse duration was trimmed to 10 µs.

Results for the current limited test setup from Figure 9.9 are listed in Table 9.1. The voltage at the V_{prog} pin and the current through it are captured with an oscilloscope. For a diode with $W = 0.25\,\mu m$, $L = 0.15\,\mu m$, $M = 0.25\,\mu m$ and $S = 0.6\,\mu m$ at $I_{lim} = 7\,mA$ this is plotted in Figure 9.12. Diodes wider than 0.25 µm required higher values of I_{lim} and are therefore not preferred.

Table 9.1: Minimum required current I_{lim} at V_{supply} = 6 V for Zener diodes with W = 0.25 µm and L = 0.15 µm in the forward biased programmed OTP shift register. Current pulse duration was 10 µs.

Middle p- region length M (µm)	Silicide-junction distance S (µm)	I_{lim} (mA)	
		nldd	no nldd
0	0.6	6	6
0	0.8	6	6
0	1	6	7
0.15	0.6	6	6
0.15	0.8	7	5
0.15	1	7	6
0.25	0.6	7	6
0.25	0.8	7	6
0.25	1	6	7

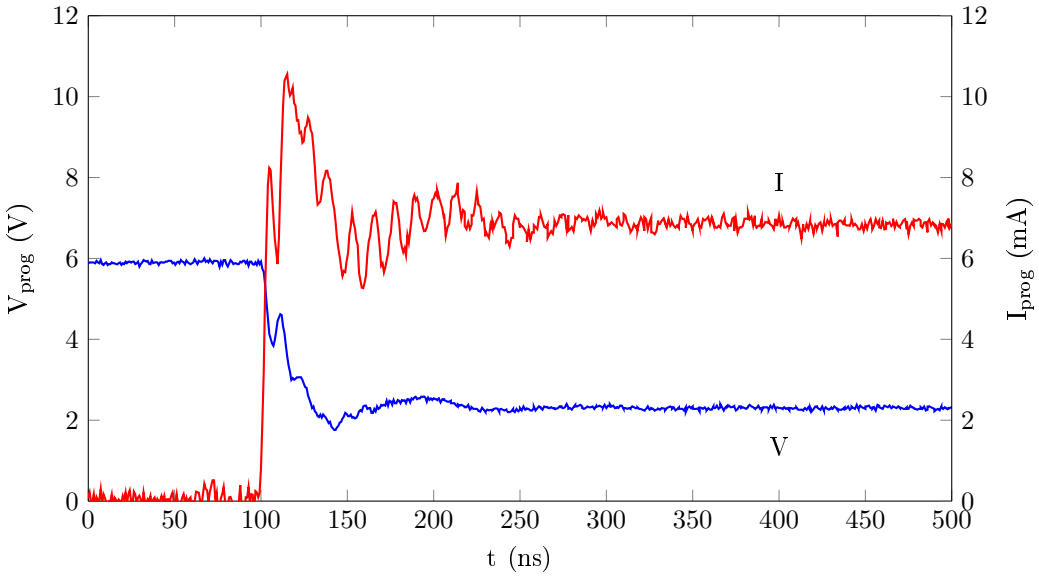


Figure 9.12: Forward biased programming of OTP memory cell with Zener variant W = 0.25 µm, L = 0.15 µm, M = 0.25 µm, S = 0.6 µm.

To better understand the transition to a low-ohmic connection, an additional test was performed on a diode with W = 0.25 µm, L = 0.15 µm, M = 0.25 µm and S = 0.6 µm. The 6 V supply was connected through a 500 Ω resistor to the V_{prog} pin on the chip to limit the current, see Figure 9.13. The voltage over the 500 Ω resistor and the voltage at the V_{prog} pin are measured with an oscilloscope and plotted in Figure 9.14. The transition lasts about 1 µs, in which the first part may be heating and the step at t = 1.5 µs the permanent change in characteristics. A diode with the same layout parameters but without nldd implantation in the cathode was also measured, see Figure 9.15. The breakdown transition is only 200 µs for this diode.

Measurements on variants with W = 0.25 µm, L = 0.15 µm, M = 0.15 µm and S = 0.6 µm

with and without nldd also show this difference.

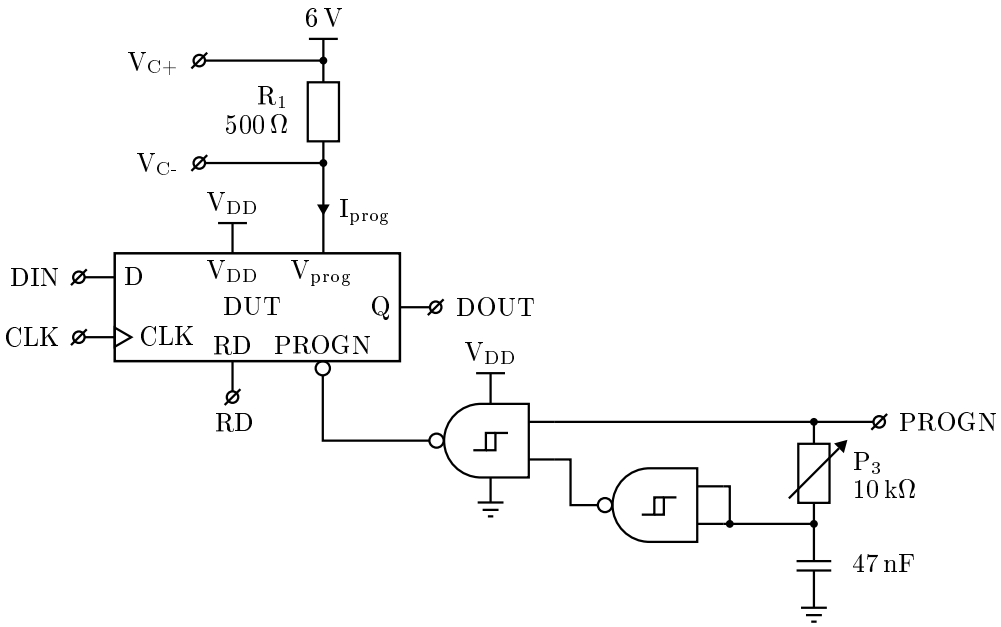


Figure 9.13: Current pulse test setup implementing passive current limiting.

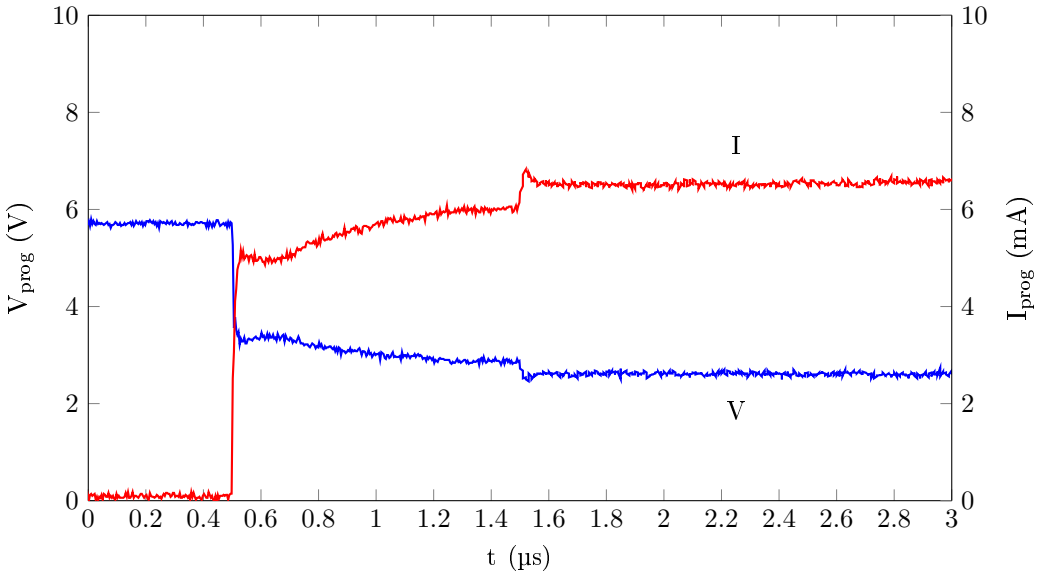


Figure 9.14: Forward biased programming through 500 Ω resistor of OTP memory cell with Zener variant W = 0.25 µm, L = 0.15 µm, M = 0.25 µm, S = 0.6 µm.

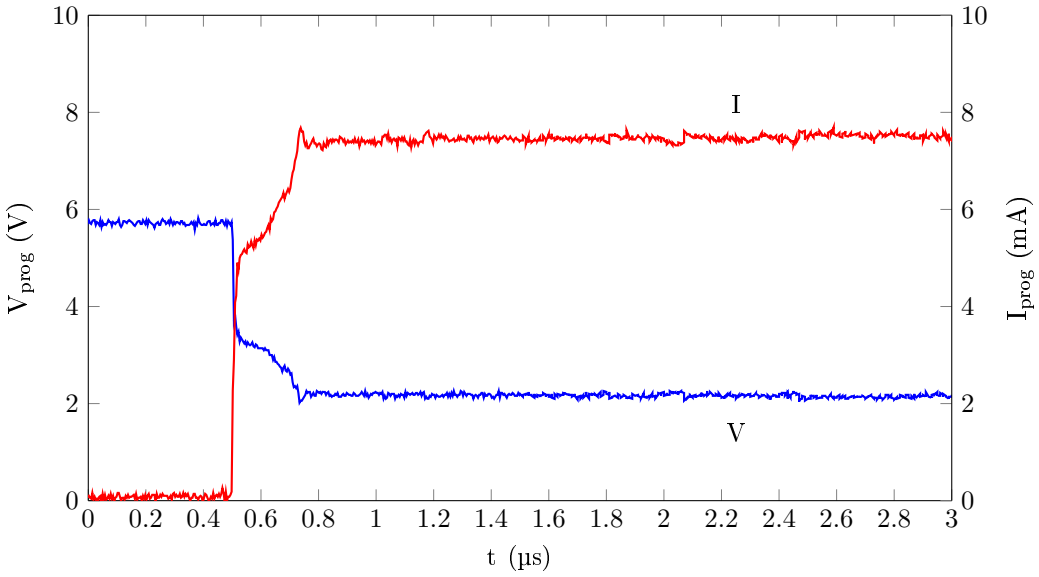


Figure 9.15: Forward biased programming through 500 Ω resistor of OTP memory cell with Zener variant W = 0.25 µm, L = 0.15 µm, M = 0.25 µm, S = 0.6 µm without nldd.

Results of the Reverse Biased Programmed OTP Memory Tests

The reverse biased programmed OTP flipflops contain 9.3 µm or 19.3 µm wide SOX-based NDMOSTs which' drain currents reach a maximum of 2.5 mA or 5 mA when programming, respectively.

In Section 4.3, the reverse breakdown current was found to be constant for 0.25 µm wide diodes so the voltage is varied for these devices without limiting the current. OTP flipflops implementing diodes with S = 0.5 µm and 9.3 µm wide NDMOSTs did not program correctly for 25 µs current pulses at V_{prog} = 7 V. Several OTP flipflop variants with 19.3 µm wide NDMOSTs did program for $V_{prog} \leq 7$ V, see Table 9.2.

Table 9.2: Minimum required V_{prog} without external current limiter for implemented Zener diodes with W = 0.25 µm and S = 0.5 µm in the reverse biased programmed OTP shift register with 19.3 µm wide NDMOST. Current pulse duration was 25 µs.

Silicidized length L (µm)	Middle p- region length M (µm)	V_{prog} (V)	
		nldd	no nldd
0.15	0	7	> 7
0.15	0.15	6.5	> 7
0.15	0.25	> 7	> 7
0.5	0	6.5	6.5
0.5	0.15	6.5	> 7
0.5	0.25	7	> 7
1	0	6.5	6.5
1	0.15	6	6.5
1	0.25	6.5	> 7
2	0	6.5	6.5
2	0.15	6.5	7
2	0.25	6.5	> 7
4	0	6.5	6.5
4	0.15	6.5	7
4	0.25	6.5	> 7
8	0	6.5	6.5
8	0.15	> 7	> 7
8	0.25	7	> 7

9.4.3 Discussion of the OTP Memory Test Results

OTP functionality was successfully added to a standard flipflop. Read and write operations can be performed and the OTP flipflop shift register functioned properly.

In Section 4.3 it was observed that adding nldd to the cathode lowers the lower bound to the minimum forward breakdown current. However, by means of current pulse tests it was found that for 10 µs current pulses the minimum forward breakdown current is similar. The diode breakdown transition did take longer for the nldd-implanted variants.

Diodes with M = 0 µm, 0.15 µm and 0.25 µm had similar results. Only parameter S, the silicide-junction distance, has a significant effect on the required current. As found in Section 4.3.1, smaller values of S minimize the required current. To prevent excessive reverse leakage which causes the OTP cells to dysfunction, S $\geq$ 0.5 µm should be selected.

The larger programming NPN transistor is not required in the forward biased programmed OTP flipflop, but in reverse bias the high-current variant is required. Therefore, the minimum size of the forward biased programmed OTP flipflop is significantly smaller than reverse biased programmed variant. Furthermore, the required V_{prog} supply voltage is over 5 V for the reverse biased variant which imposes additional challenges in terms of reliability.

9.5 Conclusion of the OTP Memory

The targets for improvement stated in Section 1.1.2 are achieved with the implemented forward biased programmed OTP flipflop shift register. The most suited OTP flipflop implements a Zener diode with W = 0.25 µm, L = 0.15 µm, M = 0.25 µm and S = 0.6 µm. This OTP flipflop has specifications as follows:

- 5 V programming voltage
- 8 mA programming current
- 10 µs programming time
- 25 µA read current
- 405 μm^2 die area

This OTP flipflop fits in the digital cell library for easy implementation and usage. As an improvement to this OTP flipflop, the programming NPN transistor may be reduced in size. This both decreases the die area and removes the need for external current limiting.

Reverse biased programming is also possible; a reverse biased programmed OTP flipflop was successfully implemented. However, a programming voltage over 5 V is required to program this OTP flipflop, which is non-compliant with the specifications. Furthermore, more die area is required than for the forward biased implementation.

Chapter 10

Conclusions

A feasibility study was performed to implement Zener diodes, JFETs and DMOSTs in an existing 0.25 µm BiCMOS process without changing any existing or adding additional process steps or masks. Two iterations of lateral polysilicon Zener diodes were fabricated and measured. For the application of OTP memory, these Zener diodes were aimed to change characteristics drastically when a short current pulse is applied. Optimal layout parameters were found to achieve this for forward biased current pulses; the diode width W = 0.25 µm, the silicidized connections to the diode as short as possible with L = 0.15 µm, the middle p^- region length M = 0.25 µm and the distance between the silicide and the junction S = 0.5 µm. Furthermore, when the cathode is implanted with shallow n^+ without nldd, the breakdown transition time decreases which is beneficial. By means of a 10 µs, 8 mA forward biased current pulse, the diode characteristic of the optimal diode changed to a 1 kΩ linear characteristic for both forward and revers bias.

The working principle of the forward breakdown effect in the Zener diodes was observed with TEM/STEM imaging. The silicide and cathode n^+ migrate into the cathode and short the junction to a low-ohmic connection.

Read and write circuitry were designed for the Zener diodes and was combined with an existing flipflop to an OTP flipflop. This flipflop programs its value when the programming signal is made active and 5 V is present on the V_{prog} supply. Outside programming V_{prog} should be grounded. When programming is performed outside normal operation no additional power supply requirements apply. When the read input signal of the OTP flipflop is in active state the reverse characteristic of the Zener diode is read-out with a 25 µA current source and is stored in the flipflop.

The OTP flipflop variants were successfully integrated in the digital cell layout by means of a shift register. Close and easy integration with other digital circuitry is therefore acquired. Furthermore, a functional OTP flipflop was created that is only about double the size of a normal flipflop. Read-out is performed with a current of 25 µA per OTP flipflop. All target specifications from Section 1.1.2 are therefore achieved.

The programming current had to be externally limited to reliably program the 0.25 µm wide diodes. An opportunity to further decrease the size of the OTP flipflop is therefore present.

Programming in reverse bias is also possible but not preferred. A higher programming voltage and more die area are required while the change in diode characteristics are smaller than for the forward biased programmed variant.

A multitude of NDMOS and PDMOS transistors were designed and fabricated. Also two types of thick oxide were experimented; the 10 nm sacrificial oxide and ~500 nm shallow trench isolation. The n and p wells were used to create the lowly doped drain region.

The SOX-based DMOSTs are limited to the hard drain-gate oxide breakdown voltage at $|V_{DG}| = 13\,V$. The STI-based transistors feature drain breakdown voltages up to 18 V but suffer from higher drain resistance than the SOX-based counterparts. As a proposed solution, low-ohmic buried layers may be added underneath the drain for these STI-based transistors. It was found that the drain-bulk breakdown voltage does not decrease when a buried n layer is added to the NDMOST drain.

The DMOST threshold voltages are 0.44 V and −0.66 V up to at least 0.35 µm SOX overlap with the channel and for all fabricated STI-based variants. Impact ionization is dominant in almost all measured DMOSTs; up to 100 µA bulk current was measured and typically starts at $V_{DS} = 4\,V$ for NDMOSTs and −6 V for PDMOSTs. The ~10 kΩ NDMOST bulk impedance then raised the bulk to about a volt. A low-ohmic bulk connection was suggested. The impact ionization was found to shift to over −10 V for the STI-based PDMOST with D = 0.3 µm. More research is required to find the cause of this phenomenon.

Unfortunately, no JFETs were fabricated that had an absolute pinch-off voltage around 2.5 V. One NJFET and one PJFET variant had drain-source conduction at $V_{GS} = 0\,V$, but both could not be pinched off with $|V_{DS}| < 5\,V$. Therefore, no suitable JFETs were found to implement a high-voltage digital signal driver with.

Additional research is required to implement a high-voltage digital signal driver with the DMOS transistors. The fabricated NDMOSTs and PDMOSTs in combination with a proposed SOX-based thick-oxide PMOST could serve the application. Thick-oxide PMOSTs can then be used as cross-coupled PMOST pair to replace the low-voltage PMOSTs and the PJFETs in the circuit of Figure 2.9. However, research has to be performed on the threshold voltage of this thick-oxide PMOST.

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Appendix A

Device Characterization

Two wafer production cycles were performed for this study. The first iteration only featured devices, the second iteration also circuit implementations of the devices. Microscopic photographs of the fabricated dies are given in Figures A.1 and A.2. Per iteration, single devices from a single wafer were measured at room temperature for the DC characterization. The characterization results are listed in Tables A.1 to A.8.

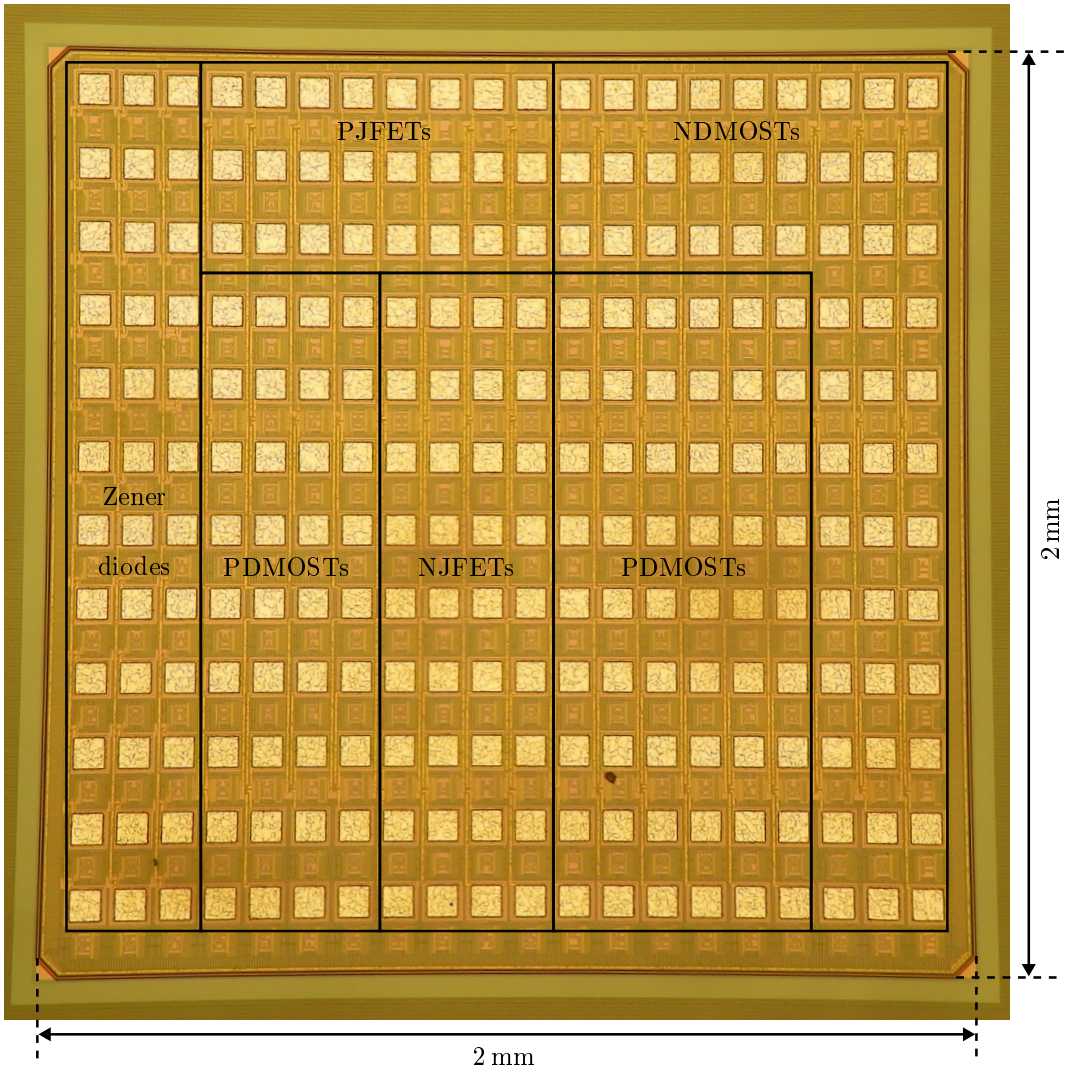

Figure A.1: Microscopic photograph of die from the first iteration with its segments indicated.

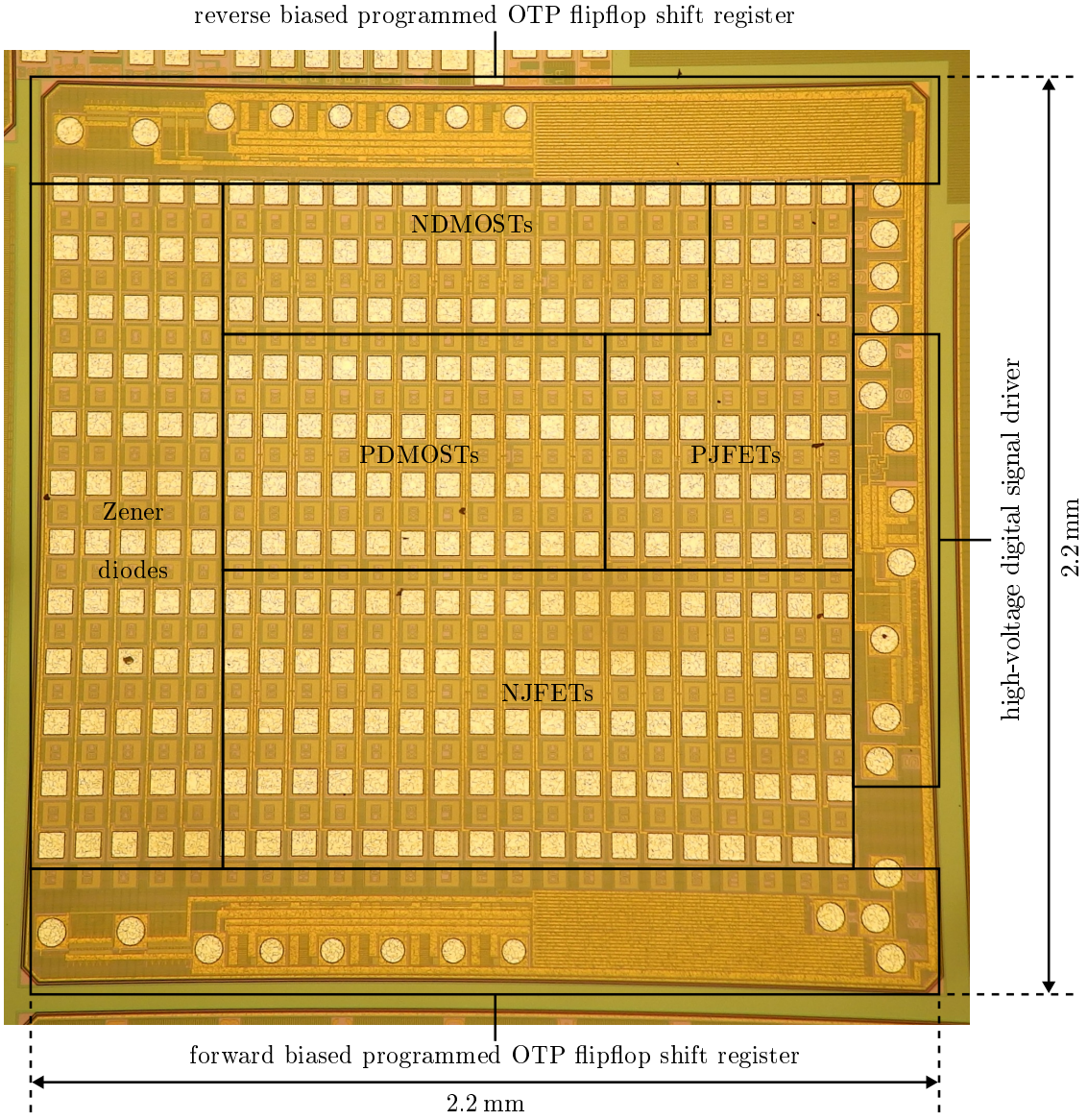

Figure A.2: Microscopic photograph of the die from the second iteration with its segments indicated.

Table A.1: Specifications of Zener diodes in forward bias. R_s is determined by the slope of the V-I curve, averaged over the forward biased voltage range between 2 V and 3 V.

W (µm)	L (µm)	M (µm)	Cathode	V_{BD} (V)	I_{BD} (mA)	P_{BD} (mW)	R_s (kΩ)
0.25	0.5	0.25	n^+	5.31	3.36	17.8	1.461
0.30	0.5	0.25	n^+	5.23	3.99	20.9	1.329
0.35	0.5	0.25	n^+	5.17	4.04	20.9	1.263
0.40	0.5	0.25	n^+	5.12	3.88	19.9	1.107
0.45	0.5	0.25	n^+	4.98	4.42	22.0	0.959
0.50	0.5	0.25	n^+	4.93	4.38	21.6	0.942
0.60	0.5	0.25	n^+	4.82	5.01	24.2	0.783
0.70	0.5	0.25	n^+	4.72	4.77	22.5	0.741
0.80	0.5	0.25	n^+	4.61	5.13	23.7	0.667
0.90	0.5	0.25	n^+	4.50	5.52	24.8	0.596
1.00	0.5	0.25	n^+	4.53	6.08	27.5	0.546
0.25	0.5	0.00	n^+	5.06	4.64	23.5	1.171
0.25	0.5	0.05	n^+	4.94	3.73	18.4	1.089
0.25	0.5	0.10	n^+	5.03	3.75	18.9	1.196
0.25	0.5	0.15	n^+	5.21	3.30	17.2	1.335
0.25	0.5	0.20	n^+	5.21	3.50	18.2	1.419
0.25	0.5	0.30	n^+	5.41	3.46	18.7	1.498
0.25	0.5	0.40	n^+	5.55	2.96	16.4	1.610
0.25	0.5	0.50	n^+	5.83	2.39	14.0	2.067
0.25	0.5	0.75	n^+	6.36	2.14	13.6	2.427
0.25	0.5	1.00	n^+	5.98	1.97	11.8	3.396
0.25	0.5	2.00	n^+	10.18	1.19	12.1	16.052
0.25	0.75	0.25	n^+	6.3	2.61	16.4	2.680
0.25	1	0.25	n^+	7.4	2.60	19.2	3.200
0.25	1.5	0.25	n^+	9.6	2.62	25.1	5.391
0.25	0.5	0.25	n^+, nldd	5.04	3.99	20.1	1.277
0.25	0.5	0.25	nldd	5.23	3.05	15.9	1.461

Table A.2: Specifications of Zener diodes in reverse bias. R_s is determined by the slope of the V-I curve, averaged over the reverse biased voltage range between 6 V and 7 V.

W (µm)	L (µm)	M (µm)	Cathode	V_{BD} (V)	I_{BD} (mA)	P_{BD} (mW)	R_s (kΩ)
0.25	0.5	0.25	n^+	-8.63	-0.851	7.34	4.246
0.30	0.5	0.25	n^+	-8.67	-0.927	8.04	2.588
0.35	0.5	0.25	n^+	-8.24	-0.928	7.65	3.786
0.45	0.5	0.25	n^+	-8.00	-1.126	9.01	2.534
0.50	0.5	0.25	n^+	-7.87	-1.253	9.86	2.261
0.60	0.5	0.25	n^+	-7.70	-1.337	10.29	2.011
0.70	0.5	0.25	n^+	-7.69	-1.579	12.14	1.850
0.80	0.5	0.25	n^+	-7.90	-1.461	11.54	1.825
1.00	0.5	0.25	n^+	-7.64	-1.506	11.51	1.799
0.25	0.5	0.00	n^+	-7.19	-1.121	8.06	2.431
0.25	0.5	0.05	n^+	-7.26	-1.075	7.80	2.697
0.25	0.5	0.10	n^+	-7.50	-0.957	7.18	3.079
0.25	0.5	0.15	n^+	-7.64	-1.105	8.44	3.191
0.25	0.5	0.30	n^+	-9.10	-0.726	6.61	6.387
0.25	0.5	0.40	n^+	-8.89	-0.844	7.50	4.751
0.25	0.5	0.50	n^+	-8.90	-0.959	8.54	4.539
0.25	0.5	0.75	n^+	-10.59	-0.824	8.73	8.496
0.25	0.5	1.00	n^+	-11.40	-0.891	10.16	8.458
0.25	0.5	2.00	n^+	-16.22	-0.831	13.46	17.510
0.25	0.75	0.25	n^+	-9.14	-0.728	6.65	5.945
0.25	1.00	0.25	n^+	-9.38	-1.441	13.52	5.653
0.25	1.50	0.25	n^+	-9.56	-1.309	12.51	6.457
0.25	0.5	0.25	n^+, nldd	-7.33	-1.383	10.14	2.562
0.25	0.5	0.25	nldd	-7.57	-0.944	7.15	2.864

Table A.3: Specifications of improved Zener diodes in forward bias.

W (µm)	L (µm)	M (µm)	S (µm)	Cathode	V_{BD} (V)	I_{BD} (mA)	P_{BD} (mW)
0.25	8	0.25	0.5	n^+, nldd	3.84	4.73	18.1
0.25	8	0.25	0.5	n^+	4.04	4.48	18.1
0.25	4	0.25	0.5	n^+, nldd	3.45	4.89	16.9
0.25	2	0.25	0.5	n^+, nldd	2.97	4.70	14.0
0.25	1	0.25	0.5	n^+, nldd	2.84	4.71	13.4
0.25	0.5	0.25	0.5	n^+, nldd	2.72	4.57	12.4
0.25	0.15	0.25	0.5	n^+, nldd	2.83	5.05	14.3
0.25	0.15	0.25	0.5	n^+	2.81	3.96	11.1
0.25	2	0	0.5	n^+, nldd	2.99	4.80	14.4
0.25	0.15	0	0.5	n^+, nldd	2.97	5.13	15.2
0.25	8	0.15	0.5	n^+, nldd	3.85	4.80	18.5
0.25	8	0	0.5	n^+, nldd	3.88	4.70	18.2
0.5	4	0.25	0.5	n^+, nldd	3.10	6.89	21.4
0.5	4	0.25	0.5	n^+	3.17	6.41	20.3
0.5	2	0.25	0.5	n^+, nldd	2.67	7.15	19.1
0.5	1	0.25	0.5	n^+, nldd	2.50	6.97	17.4
0.5	0.5	0.25	0.5	n^+, nldd	2.46	7.04	17.3
0.5	0.5	0.25	0.5	n^+	2.84	5.45	15.5
0.5	4	0.15	0.5	n^+, nldd	3.37	7.41	25.0
0.5	4	0	0.5	n^+, nldd	3.00	6.91	20.7
1	0.15	0.25	1	n^+, nldd	3.34	6.91	23.1
1	0.15	0.25	1	n^+	4.05	6.36	25.8
1	0.15	0.25	0.8	n^+, nldd	2.91	8.84	25.7
1	0.15	0.25	0.6	n^+, nldd	2.55	11.66	29.7
1	0.15	0	1	n^+, nldd	3.38	6.85	23.2
1	0.15	0	1	n^+	4.01	6.25	25.1
1	0.15	0	0.8	n^+, nldd	2.91	11.14	32.4
1	0.15	0	0.6	n^+, nldd	2.49	10.31	25.7

Table A.4: Specifications of improved Zener diodes in reverse bias.

W (µm)	L (µm)	M (µm)	S (µm)	Cathode	V_{BD} (V)	I_{BD} (mA)	P_{BD} (mW)
0.25	8	0.25	0.5	n^+, nldd	-6.43	-0.88	5.65
0.25	8	0.25	0.5	n^+	-6.68	-0.89	5.94
0.25	4	0.25	0.5	n^+, nldd	-6.07	-0.89	5.40
0.25	2	0.25	0.5	n^+, nldd	-6.28	-0.86	5.38
0.25	1	0.25	0.5	n^+, nldd	-6.34	-0.85	5.41
0.25	0.5	0.25	0.5	n^+, nldd	-5.99	-0.95	5.69
0.25	0.15	0.25	0.5	n^+, nldd	-6.55	-0.91	5.98
0.25	0.15	0.25	0.5	n^+	-6.61	-1.09	7.19
0.25	2	0	0.5	n^+, nldd	-6.14	-0.91	5.57
0.25	0.15	0	0.5	n^+, nldd	-7.19	-0.90	6.46
0.25	8	0.15	0.5	n^+, nldd	-6.27	-0.93	5.82
0.25	8	0	0.5	n^+, nldd	-6.76	-0.81	5.47
0.5	4	0.25	0.5	n^+, nldd	-5.64	-1.20	6.74
0.5	4	0.25	0.5	n^+	-6.69	-1.12	7.51
0.5	2	0.25	0.5	n^+, nldd	-6.04	-1.12	6.77
0.5	1	0.25	0.5	n^+, nldd	-5.65	-1.28	7.21
0.5	0.5	0.25	0.5	n^+, nldd	-5.74	-1.33	7.62
0.5	0.5	0.25	0.5	n^+	-6.75	-1.14	7.69
0.5	4	0.15	0.5	n^+, nldd	-5.80	-1.20	6.98
0.5	4	0	0.5	n^+, nldd	-6.08	-1.06	6.46
1	0.15	0.25	1	n^+, nldd	-6.31	-1.89	11.91
1	0.15	0.25	1	n^+	-7.33	-1.91	13.99
1	0.15	0.25	0.8	n^+, nldd	-6.40	-1.95	12.47
1	0.15	0.25	0.6	n^+, nldd	-5.88	-2.14	12.60
1	0.15	0	1	n^+, nldd	-6.42	-2.03	13.06
1	0.15	0	1	n^+	-6.57	-2.18	14.31
1	0.15	0	0.8	n^+, nldd	-6.05	-1.91	11.56
1	0.15	0	0.6	n^+, nldd	-5.89	-1.88	11.09

Table A.5: Specifications of the first generation NDMOSTs.

type	W (µm)	L (µm)	D (µm)	$V_{DS,bd}$ (V)		R_{on} (kΩ)	$I_{D,sat}$ (µA)
				$V_{GS} = 0\,V$	$V_{GS} = 2.5\,V$		
SOX	1.3	1	-0.15	8	8.25	2.941	371
SOX	1.3	1	0	7.7	8.65	2.985	363
SOX	1.3	1	0.15	11.6	8.6	4.587	178
SOX	1.3	1	0.3	12	8.6	2.941	365
SOX	1.3	1	0.5	10.9	8.175	2.890	362
SOX	1.3	1	0.75	10.9	8.6	2.899	368
SOX	1.3	0.25	0.3	4.8	6.2	1.174	955
SOX	1.3	0.5	0.3	6	6.9	1.739	590
SOX	2.9	1	0.3	11.1	8.1	1.312	793
STI	1.3	1	0.5	11	10.3	3.030	358
STI	1.3	1	0.6	8.1	10.4	2.967	361
STI	1.3	1	0.7	11	11.4	2.985	360
STI	1.3	1	0.8	10	10.9	2.967	361
STI	1.3	1	1	10.9	10.7	2.874	368
STI	1.3	0.25	0.5	4.6	7.9	0.985	960
STI	1.3	0.5	0.5	6.1	9.5	1.866	590
STI	2.9	1	0.5	11.4	9.1	1.372	783

Table A.6: Specifications of the first generation PDMOSTs.

type	W (µm)	L (µm)	D (µm)	$V_{DS,bd}$ (V)		R_{on} (kΩ)	$I_{D,sat}$ (µA)
				$V_{GS} = 0\,V$	$V_{GS} = -2.5\,V$		
SOX	1.3	1	-0.15	-15.5	-17.45	15.176	-68
SOX	1.3	1	0	-15.9	-18.15	15.373	-66
SOX	1.3	1	0.15	-15.6	-17.65	15.439	-69
SOX	1.3	1	0.3	-15.2	-17.75	15.547	-69
SOX	1.3	1	0.5	-15.1	-16.85	15.787	-70
SOX	1.3	1	0.75	-15.8	-17.1	16.686	-69
SOX	1.3	0.5	0.3	-15.8	-17.3	9.816	-154
SOX	1.3	0.25	0.3	-15.3	-17.25	6.318	-346
SOX	2.9	1	0.3	-15.9	-18.15	7.084	-150
STI	1.3	1	0.25	-18.2	-17.95	1041.67	-14
STI	1.3	1	0.3	-16.9	-17.85	33.00	-52.1
STI	1.3	1	0.4	-18.3	-18.1	28.49	-65.5
STI	1.3	1	0.5	-18.3	-18	24.75	-71.6
STI	1.3	1	0.75	-17.8	-17.95	27.10	-68.8
STI	1.3	0.5	0.3	-18.1	-17.8	135.87	-25.5
STI	1.3	0.25	0.3	-18.3	-18	227.79	-24.3
STI	2.9	1	0.3	-18.1	-18	17.99	-83.6

Table A.7: Specifications of the improved NDMOSTs.

type	W (µm)	L (µm)	D (µm)	$V_{DS,bd}$ (V)		R_{on} (kΩ)	$I_{D,sat}$ (µA)	V_T (V)
				$V_{GS} = 0\,V$	$V_{GS} = 2.5\,V$			
SOX	1.3	1.25	0	13.85	15.275	3.897	289	0.44
SOX	1.3	1.5	0	16.20	20.9	4.891	269	0.44
SOX	1.3	2	0	15.5	16.025	5.386	202	0.44
SOX	1.3	1.5	-0.15	14.575	15.15	4.420	255	0.44
SOX	1.3	1.5	-0.25	16.175	14.675	4.687	236	0.44
SOX	1.3	1.5	-0.35	9.875	14.675	5.107	184	0.45
SOX	1.3	1.5	-0.5	12.2	14.8	5.215	162	0.65
SOX	2.9	1.25	0	11.9	14.975	2.052	562	0.48
SOX	9.3	1.25	0	11.375	14.85	0.665	1746	0.53
STI	1.3	1.5	0.3	18.75	24.975	6.108	277	0.41
STI	1.3	2	0.3	19.35	> 25	7.646	197	0.41
STI	1.3	1.5	0.4	14.425	24.175	5.797	250	0.42
STI	1.3	1.5	0.5	18.6	24.575	5.475	252	0.43

Table A.8: Specifications of the improved PDMOSTs.

type	W (µm)	L (µm)	D (µm)	$V_{DS,bd}$ (V)		R_{on} (kΩ)	$I_{D,sat}$ (µA)	V_T (V)
				$V_{GS} = 0\,V$	$V_{GS} = -2.5\,V$			
SOX	1.3	0.5	0	-10.05	-15.75	19.968	-165.44	-0.62
SOX	1.3	1	0	-11.275	-16.575	15.636	-68.27	-0.66
SOX	1.3	1	-0.15	-11.475	-16.3	16.059	-70.21	-0.66
SOX	1.3	1	-0.25	-11.725	-16.25	16.387	-69.02	-0.67
SOX	1.3	1	-0.35	-11.275	-15.95	17.457	-53.89	-0.67
SOX	1.3	1	-0.5	-11.825	-16.85	18.076	-44.47	-0.85
SOX	2.9	1	0	-12.5	-15.5	6.884	-155.88	-0.67
SOX	9.3	1	0	-11.8	-16.6	2.071	-507.37	-0.67
STI	1.3	0.5	0.5	-17.875	-17.675	19.968	-84.94	-0.58
STI	1.3	1	0.5	-17.8	-18.225	30.649	-34.03	-0.66

Appendix B

Circuit Test Setup

The packaged dies were tested with a test board, a NI USB-8452 used as parallel IO port interface and labVIEW software. A schematic overview of the main components and connections is given in Figure B.1. The digital input signals CLK, DIN, RD and the trigger for PROGN are generated with custom labVIEW programs. On the rising edge of this trigger signal for PROGN, the test board generates a short pulse as required for the PROGN signal to the packaged die. The test board also includes a 2.5 V linear regulator to generate the V_{DD} and the current limiting circuit of Figure 9.9. A photograph with indication of subcircuits of the board is depicted in Figure B.2. In Figure B.3, a photograph of the entire test setup is depicted.

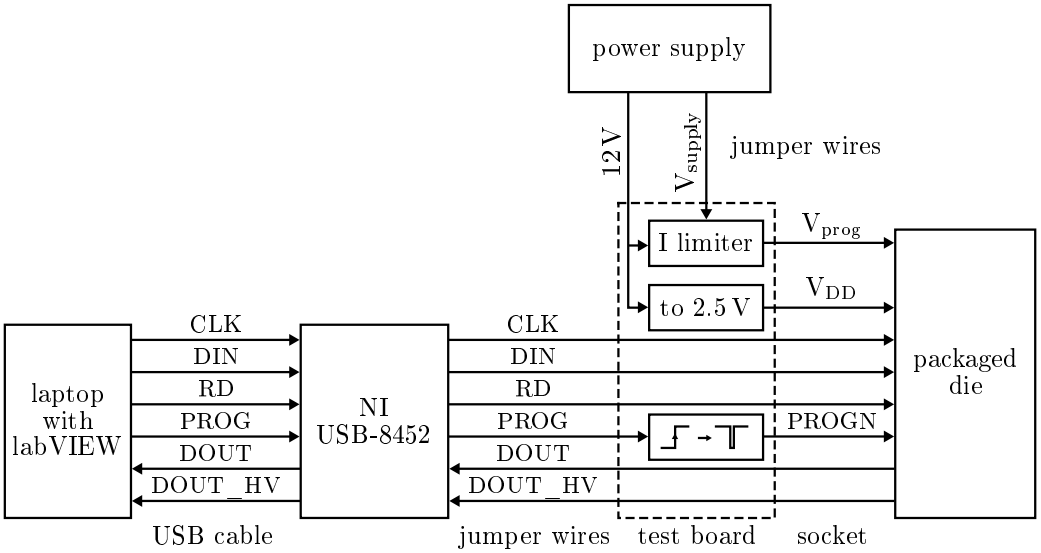

Figure B.1: Schematic view of the circuit test setup.

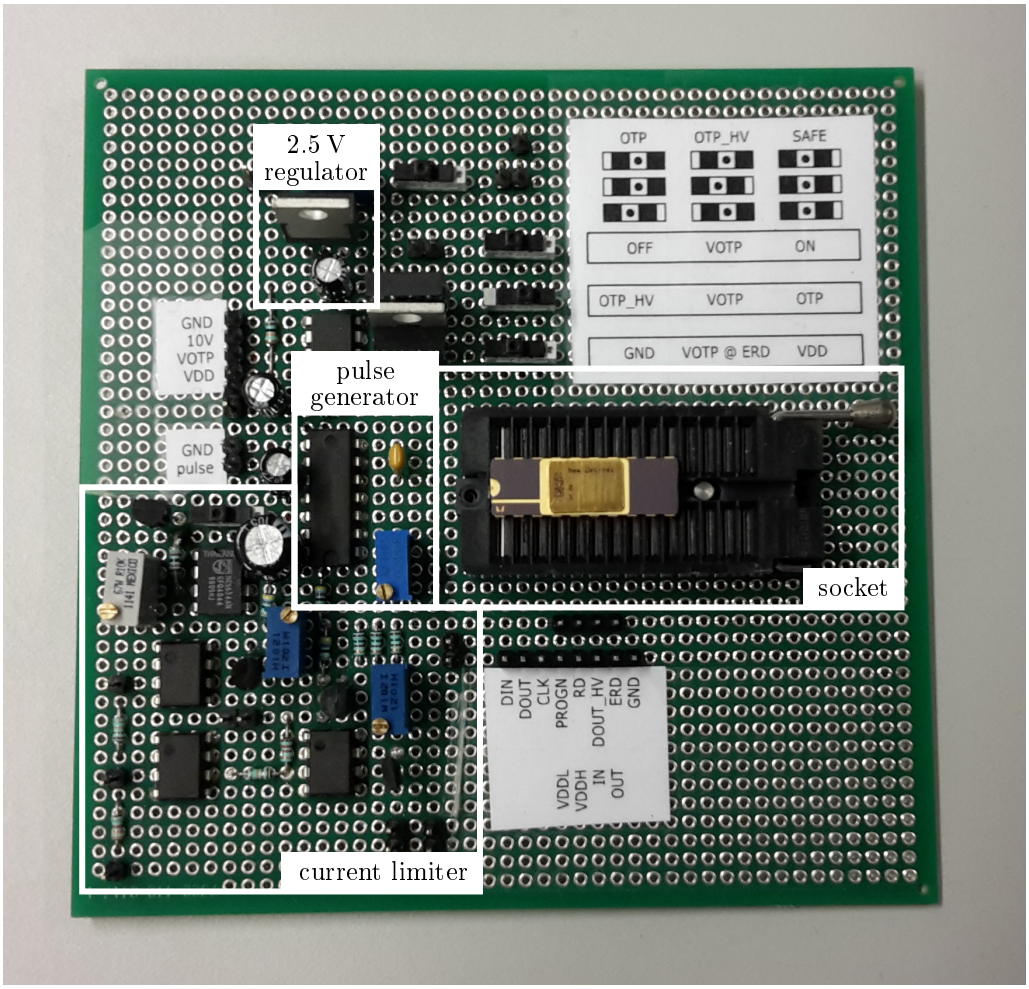

Figure B.2: Test board with subcircuits indicated.

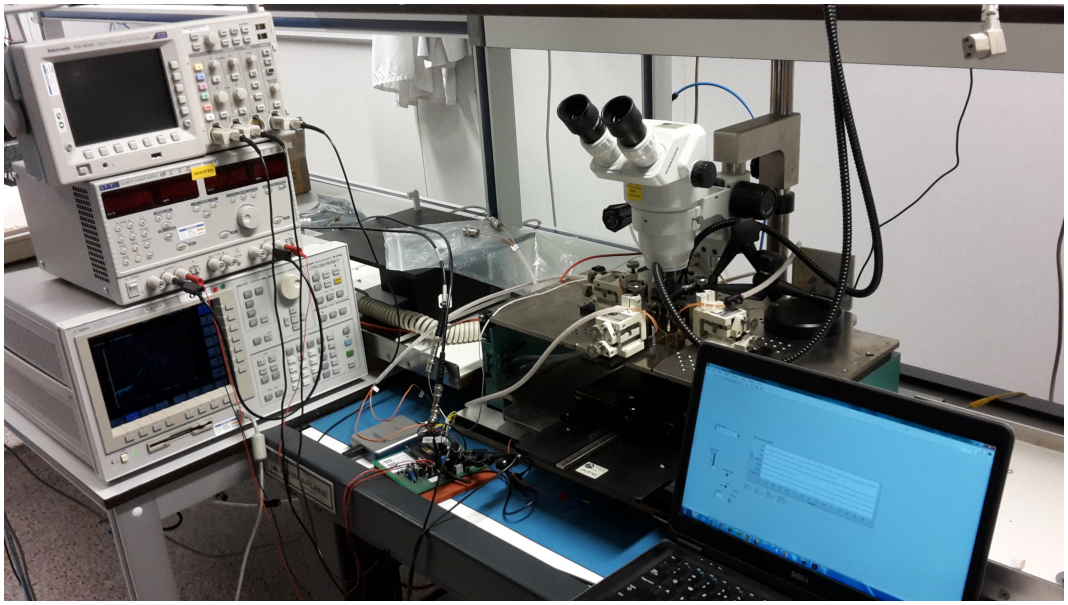

Figure B.3: Photograph of the test setup.

B.1 LabVIEW

A read program and a write program were made in LabVIEW to interface with the packaged dies. As there are two shift registers, one for the forward biased programmed OTP flipflops and one for the reverse biased programmed flipflops. A shift register is selected with settings in the LabVIEW programs and physical switches on the test board.

The read program reads the entire shift register by pulsing RD and shifting the values out. The contents of the next OTP flipflops is then read every clock cycle from DOUT (forward biased programmed OTP flipflops) and DOUT_HV (reverse biased programmed OTP flipflops). This data is interpreted by the program and listed in tables. The LabVIEW block diagram for this operation is depicted in Figure B.4 and its front panel in Figure B.5.

The write program starts with flushing the shift register with "0"s. A single "1" is then shifted into the shift register which then propagates one flipflop per clock cycle. By applying the PROGN pulse, the OTP flipflop that contains the "1" is programmed. The write program has two modes of operation; program all or program one specific OTP flipflop. The LabVIEW block diagram for this operation is depicted in Figure B.6 and its front panel in Figure B.7.

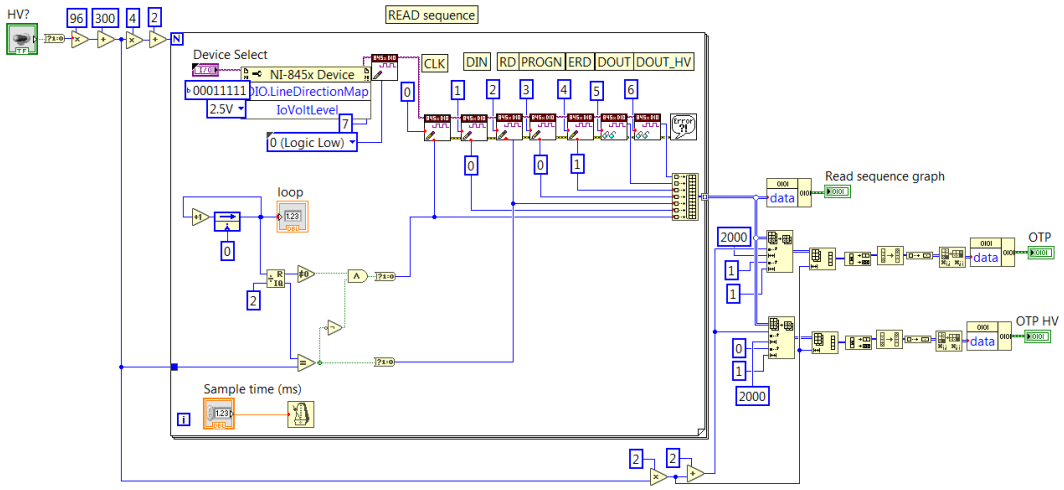

Figure B.4: Block diagram of LabVIEW program to read OTP memory bits.

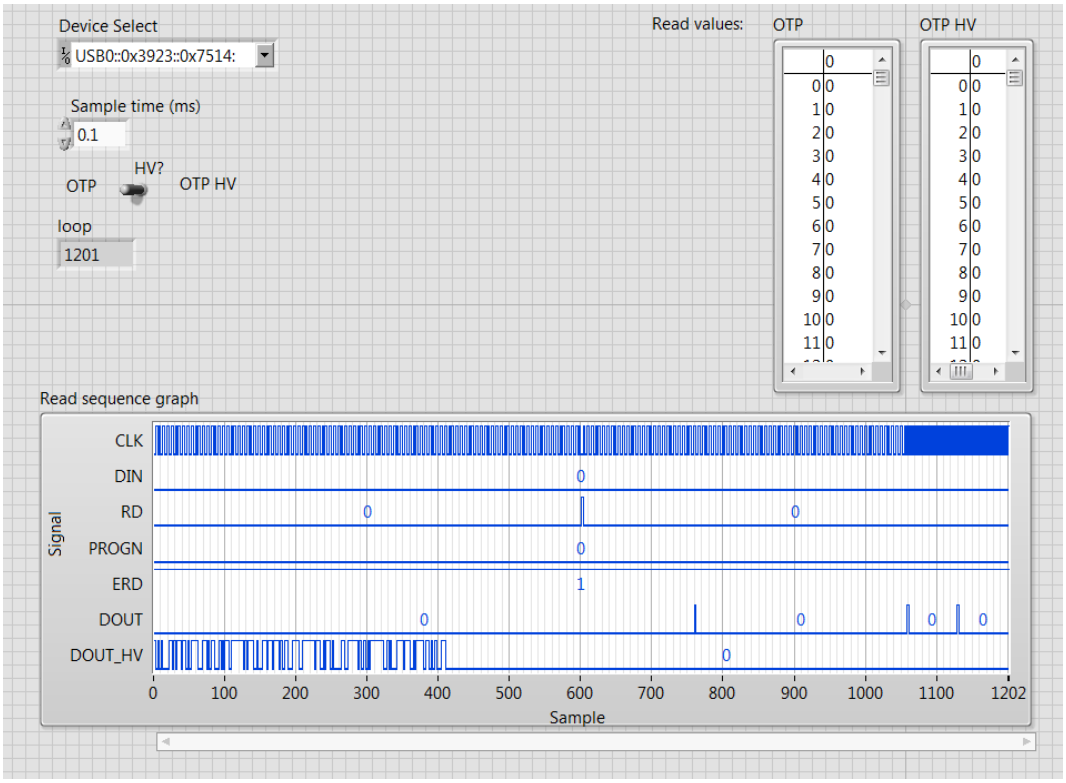

Figure B.5: Front panel of LabVIEW program to read OTP memory bits.

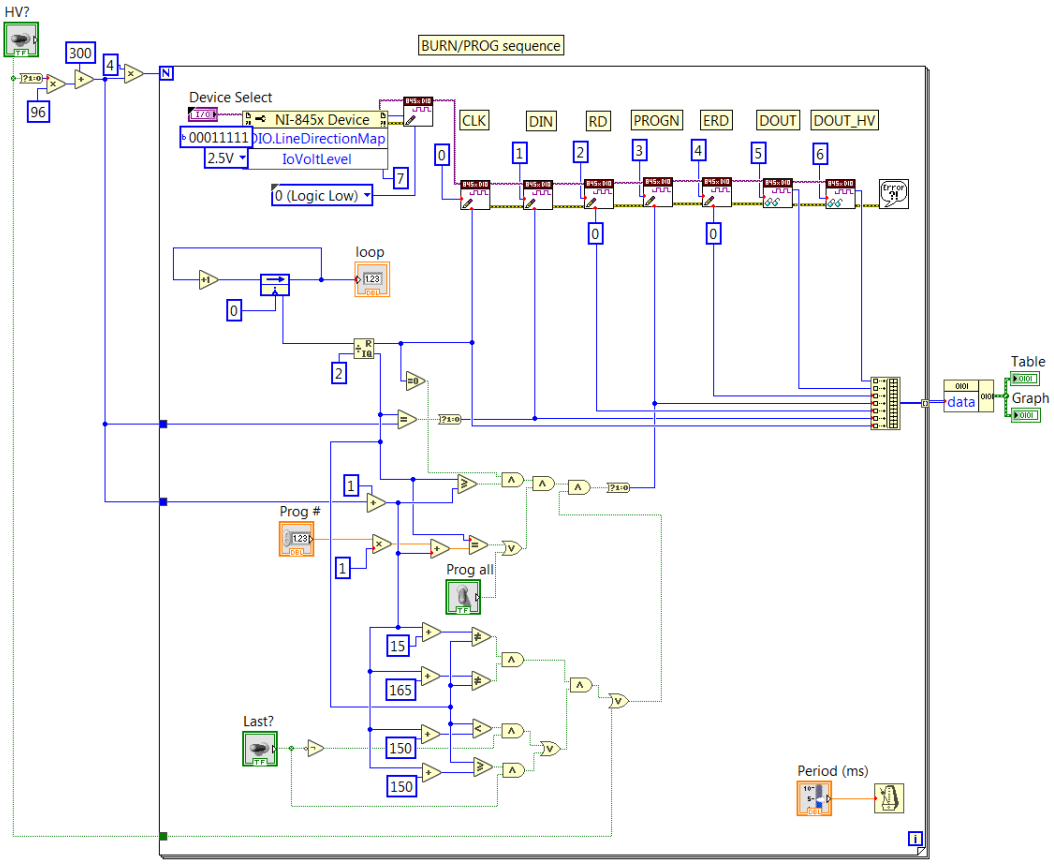

Figure B.6: Block diagram of LabVIEW program to write OTP memory bits.

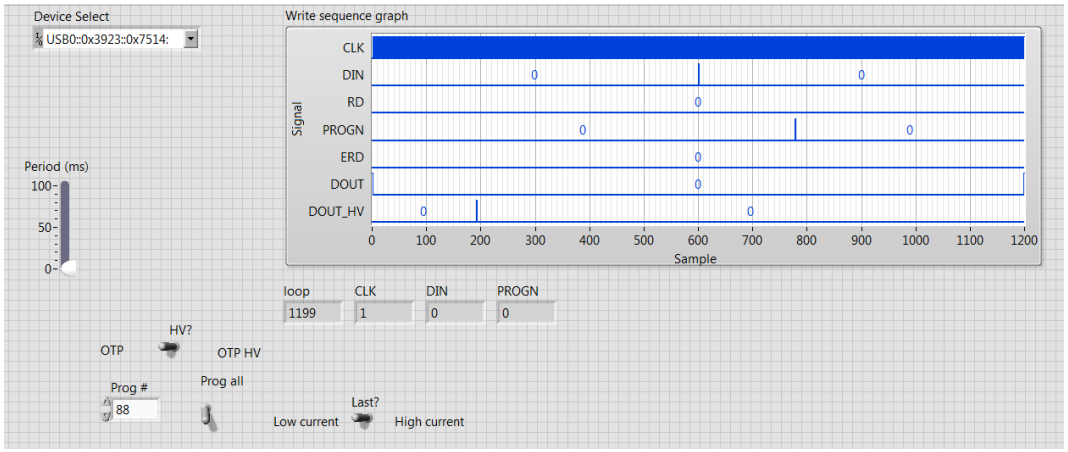

Figure B.7: Front panel of LabVIEW program to write OTP memory bits.