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A Thin-film Reconfigurable SiC Thermal Test Chip for Reliability Monitoring in Harsh Environments

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***Abstract*— Wide bandgap (WBG) semiconductor technologies enable significant progress in the emergence of power modules. Power cycling at elevated temperatures causes crack or delamination failure, especially at the die-attached bonded interface in the long term. Therefore, the in-situ reliability investigation of power modules, materials, and semiconductor packages is of great significance for modern industries. The silicon carbide's higher bandgap energy, intrinsic thermal conductivity, and mechanical strength make it a great candidate for the next generation of semiconductor, designed to operate in harsh conditions. In this study, a thin-film reconfigurable silicon carbide (SiC) thermal test chip (TTC) is designed and fabricated for reliability assessment in harsh environments. The proposed TTC realizes in-situ power/thermal cycling tests at elevated temperatures as well as characterization of novel materials such as nanoparticle-based sintering materials in die-attach technology and high-temperature-compatible epoxy molding compounds. The chip is equipped with thin-film platinum microheaters to realize modular power mappings, and platinum resistive temperature detectors (RTD) to examine the thermal reliability by monitoring the precise changes of the internal junction-to-case thermal resistance.**

Keywords—Wide bandgap semiconductor technology, power modules, die-attach, in-situ reliability investigation, bandgap energy, thermal conductivity, power cycling, nanoparticle-based sintering, resistive temperature detectors, junction-to-case thermal resistance

I. Introduction

Driven by energy transitions, the demand for high power densities and reliable power electronics is soaring [1]. Contrary to conventional silicon (Si) devices, which are limited to an operating temperature of 150 ˚C, wide bandgap (WBG) semiconductor devices can operate at considerably higher temperatures, up to 600 ˚C [2]. Therefore, the WBG technology represents a remarkable advantage in the next generation of power modules [3], [4]. The thermal characteristic evaluation and reliability of WBG semiconductor packages leave crucial issues to be investigated for the next generation of power modules. The increased power densities and potential high operating temperatures are key challenges impeding the reliable thermal management of WBG electronics.

To confront such challenges, new materials and semiconductor packages are being evaluated to alleviate thermal-mechanical health-related issues. For example, power cycling at elevated temperatures causes potential cracks or delamination failures due to a mismatch in coefficients of thermal expansion (CTE). These phenomena deteriorate bonded interfaces such as die-attach joints in long-term operation. Therefore, the in-situ health monitoring and reliability investigation of novel power modules, materials, and semiconductor packages are of prime significance in modern industries. These reliability issues could be further investigated by generating accelerated heat pulses and tracking the junction temperature, as described in Fig. 1.

Recently, a silicon carbide (SiC) thermal test chip (TTC) has been proposed in [5], [6] for online thermal resistance measurement. As shown in Fig. 2, the chip unit cell comprises a single microheater and temperature sensor, developed using Platinum material. The chip provides ON/OFF power switching capability for power cycling tests. However, the designed configuration with a single wire and probe limits the experiment options in terms of power mapping, power uniformity, and thermal map resolution. Moreover, the temperature distribution of the SiC-TEG chip showed approximately 60 ˚C variations over an area of 5x5 mm^2 under active power generation. Therefore, the need to develop a fast and flexible SiC TTC with higher power homogeneity, temperature sensitivity, and thermal map resolution should be addressed for harsh environments.

To this end, a thin-film reconfigurable SiC TTC is designed and fabricated to develop a fast and flexible thermal characteristic evaluation system for harsh environments. The proposed TTC avoids the limiting constraints of conventional Si counterparts [7] owing to the excellent physical features of WBG materials, such as their potential high operating temperatures, intrinsic higher thermal conductivity, and mechanical strength. A SiC TTC is an attractive solution for the next generation of thermal test chips, which are required to operate in harsh testing conditions to investigate novel packages and materials. For example, a SiC TTC could be employed for transient thermal measurements on nano-metallic sintered die-

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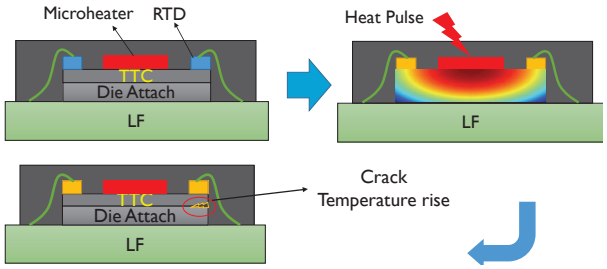

Fig. 1. Reliability investigation of the die-attach layer using a TTC.

attach joints. A similar approach is introduced in [8] using a Si thermal test chip.

II. Design and Methodology

A. SiC TTC Design

The proposed chip is modular in size and enables flexible power mapping. The 4H-SiC wafer layout contains reconfigurable 4x4 mm^2 modules that can be combined monolithically or by post-processing to support larger die sizes and precisely mimic the behavior of larger power modules. To adjust the substrate thickness, mechanical polishing could be performed before dicing.

Each TTC module (4x4 mm^2), illustrated in Fig. 3(a), includes six electrically-isolated microheaters, allowing for uniform, non-uniform, or hot-spot profiles. The active microheaters cover 82.5% of the module area, which enhances power homogeneity and temperature uniformity compared to the state-of-the-art [6]. In addition, three high-precision resistive temperature detectors (RTDs) are added to enable tracking the surface temperature with a high spatial resolution during thermal characterizations and reliability monitoring. The surface temperature represents the junction temperature in an active device. Fig 3(b) shows the structure dimensions, and the optical-laser imaging of a unit cell is provided in Fig. 3(c).

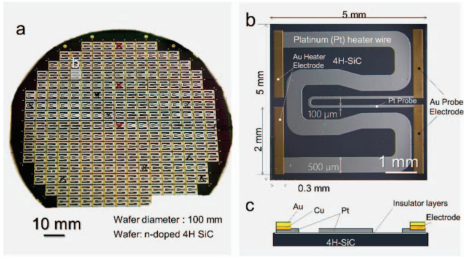

Fig. 2. Schematic diagram of the previously proposed SiC-TEG chip.

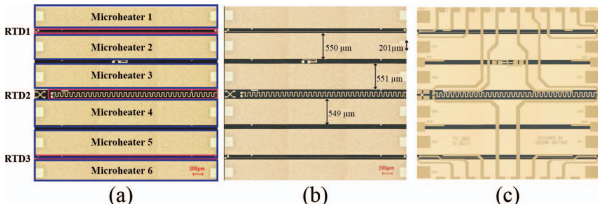

Fig. 3. (a) Schematic diagram of the proposed SiC TTC (b) Microheater dimensions (c) Optical laser imaging of the TTC unit cell.

The TTC layout contains process control modules (PCM) for contact resistance and sheet resistance measurements, as shown in Fig. 4. The microheaters were designed identically over the TTC module. The chip provides 4-point probe measurement capability for tracking the power dissipated through each microheater.

Considering the trade-off between the RTD sensitivity and process dependency, the sensor is designed in two geometries. RTD1 and RTD3 are 5 µm wide in a linear shape and provide higher sensitivity. RTD2 is 15 µm wide and spirally shaped in the center of the module. The latter is less sensitive due to lower initial resistance but less dependent on process variations. Later in the text, RTD1 and RTD3 are referred to as "LRTD" (linear RTD), and RTD2 is referred to as SRTD (spiral RTD). For accurate temperature sensing, 4-point probe measurement is considered for both RTD types. Each TTC module contains three RTDs, which enhances the spatial resolution in thermal mapping. The 2D and 3D optical laser imaging of a SiC TTC module are provided in Fig. 5.

B. TTC Modeling and Simulation

A finite element method (FEM) simulation has evaluated temperature uniformity and power homogeneity. The 3D model of a single TTC module is depicted in Fig. 6(a). The FEM simulation result in Fig. 6(b) shows the distribution of the chip surface temperature under active power excitation of 60 W. The IR thermography of the TTC is demonstrated in Fig. 6(c).

C. SiC TTC Fabrication

The SiC TTC is fabricated in thin-film technology and processed on a 4H-SiC substrate with an initial thickness of 300 µm. Two metallization steps in this process were carried out using electron beam evaporation, and the micro-structuring was correspondingly performed by the lift-off process. First, 500 nm

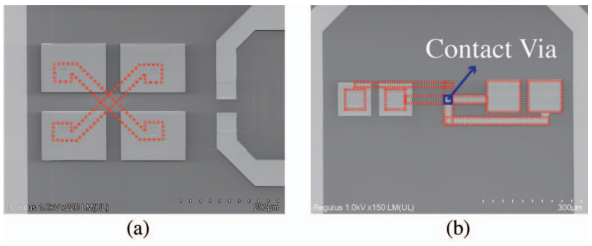

Fig. 4. Process control modules (PCM) for (a) sheet resistance and (b) contact resistance measurement.

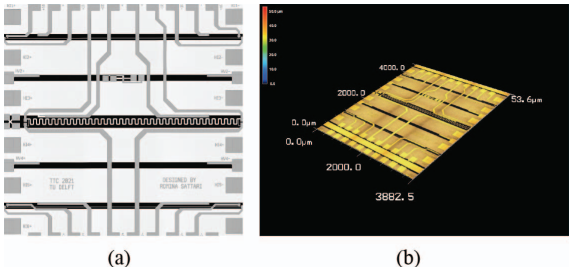

Fig. 5. (a) Optical laser imaging of SiC TTC (b) 3D imaging of a unit cell.

LPCVD TEOS film is deposited as an insulation layer on both sides of the wafer. The purpose of the backside oxidation is to avoid cross-contamination later in the process. Next, the 4H-SiC wafers were coated with 3.5 µm AZ Nlof resist, which was exposed, X-link baked, and patterned for the lift-off process. The layer was then flashed with oxygen plasma to remove organic residues from the surface of the bond pads to improve the Pt adhesion. It will also remove a small percentage of the photoresist masking layer.

Subsequently, 50 nm and 100 nm platinum were deposited using electron beam evaporation. In [9], The properties of Cr, Ti, and Al_2O_3 thin films have been investigated as an adhesion layer between Si/SiO_2 and Pt. Chromium film provides good adhesion at room temperatures. Still, it is less effective at higher temperatures due to its high oxidation rate and in corrosive environments due to the inter-diffusion rate. Titanium adhesion layer is a suitable alternative for corrosive environments, but it starts to form atomic inter-diffusion layers at higher temperatures which deteriorates the adhesion. Therefore, the introduction of Alumina alleviates the challenges discussed above and is proved to efficiently enhance the adhesion. In this study, the poor adhesion between Pt and TEOS has also been improved using a 20 nm Al_2O_3 as an intermediate layer. Therefore, the Pt layer is sandwiched between two thin films of Al_2O_3 with a thickness of 20 nm. Next, the Pt layer was patterned in an ultrasonic lift-off process at 75 ˚C.

The microheaters and RTDs were created on the same layer of Pt with 50 nm and 100 nm thicknesses to target a sheet resistance of 3.5 Ω/sq at 200 ˚C and 1.1 Ω/sq at 25 ˚C, respectively. The physical/chemical properties of Pt meet the requirements for high-temperature operation in harsh conditions.

The Keyence optical microscopy was carried out during the fabrication process to evaluate the linewidth accuracy of the microheaters. The linewidth measurement through the process provides supporting information later to realize the source of calibration errors after real-time resistance or sheet resistance measurements. The optical linewidth measurement is reported in Fig. 7.

Next, 400 nm PECVD TEOS is deposited as a dielectric layer. The contact vias through this layer were chemically etched using BHF 1:7. In this step, the top thin film layer of evaporated Al_2O_3 was also removed by BHF, as expected by the etching rate reported in [10]. Chromium-gold (Cr-Au) was subsequently deposited using electron beam evaporation and patterned by a lift-off process to form interconnects and bonding pads compatible with wire-bonding and flip-chip bumping. Fig. 8 shows the scanning electron microscopy of a single SiC TTC cell and the fab-out processed 4H-SiC wafer. Fig. 9 illustrates the local SEM imaging of the Cr-Au layer, which is uniformly deposited over the wafer.

III. Results and Discussions

Before characterizing the chip, the PCM properties were measured and investigated. Fig. 10 illustrates the sheet resistance measurement results using the VDP structures shown in Fig. 4(a). The Pt/Cr/Au contact resistance was also evaluated using the PCM defined in Fig. 4(b), and the measurement result at room temperature showed a contact resistivity of 1.51×10^{-6} $\Omega.cm^2$.

The microheaters were characterized in Fig. 11 and Fig. 12. The improved uniformity of the resistance distribution over the wafer enhances the calibration error of the microheaters. The total power generated by the TTC is typically calculated by measuring the online voltage of a single microheater due to a limitation in the number of outputs that could be read out simultaneously by the acquisition unit. Therefore, the resistance discrepancies can degrade the accuracy of the thermal resistance measurement due to causing inaccuracy in total power estimation. The resistance uniformity of microheaters is evaluated and reported in Fig. 13.

The sensitivity and accuracy of RTD sensors play a substantial role in reliability assessments. For example, during accelerated power cycling tests, the sensor readout and response time can directly affect the accurate timing of a temperature rise. This temperature rise is an indication of a potential crack

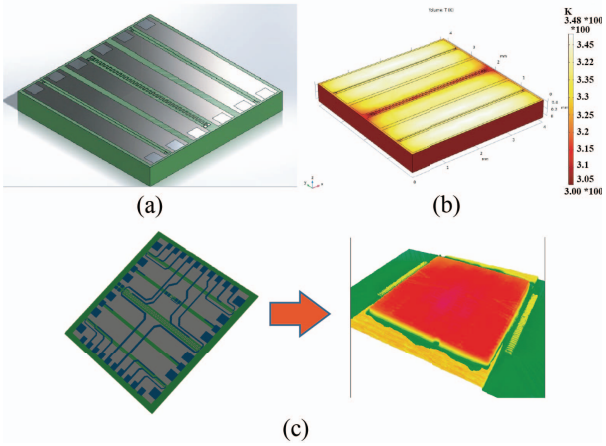

Fig. 6. (a) TTC 3D model, (b) FEM simulation analysis, and (c) IR thermography under 200 W power excitation.

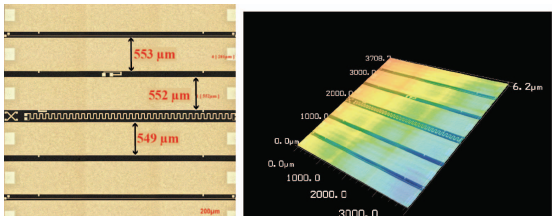

Fig. 7. The Keyence microscopy and microheater linewidth measurement.

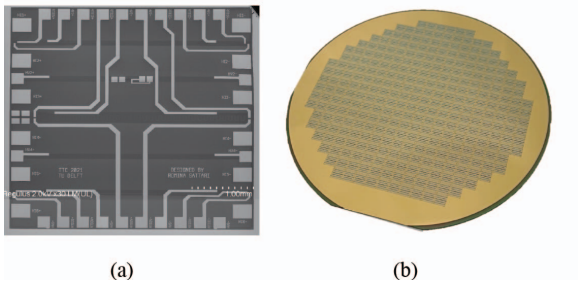

Fig. 8. (a) Scanning electron microscopy (SEM) of SiC TTC module (b) fab-out processed 4H-SiC wafer.

initiation in solder bump fatigue/failure analysis. To this end, platinum RTD sensors have been realized in linear and spiral geometries. Three spots have been dedicated at similar distances to each other to provide a temperature mapping with high spatial resolution, as shown in Fig. 3 (a). The sensors have been characterized within the temperature range of 20 ˚C to 200 ˚C using a semi-automatic probe station. As illustrated in figures 13(b) and 13(d), the central SRTDs showed a linear and stable performance with a sensitivity of 3.5 Ω/K and 1.8 Ω/K in 50 nm and 100 nm thin-film technologies, respectively. Fig. 13(a) and Fig. 13(c) indicate that the LRTDs realize a linear and stable performance with a sensitivity of 4.5 Ω/K and 2.3 Ω/K in 50 nm and 100 nm thin-film technologies, respectively. The fitting error curves confirmed that LRTD provides an improved sensitivity but higher process variation and linearity error. The 100 nm process technology enhances the fitting error due to less process dependency. The maximum temperature of the probe station chuck limited the measurement range to 200 ˚C. Table 1 summarizes the TTC performance compared with the state-of-the-art.

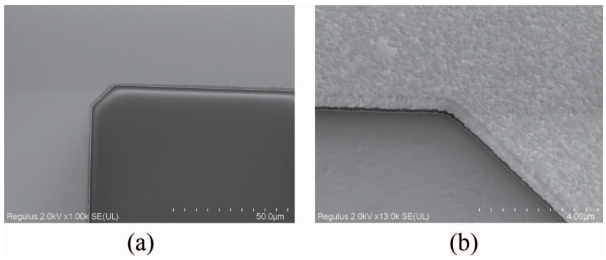

Fig. 9. SEM imaging of Cr-Au interconnects after the lift-off process.

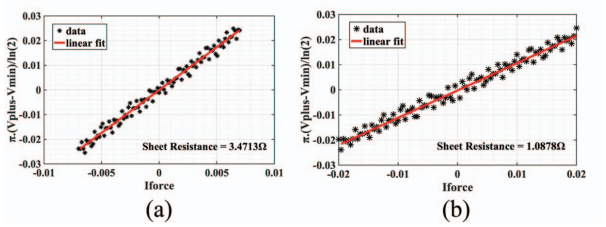

Fig. 10. Sheet resistance measurement (a) 50 nm Pt at 200 ˚C (b) 100 nm Pt.

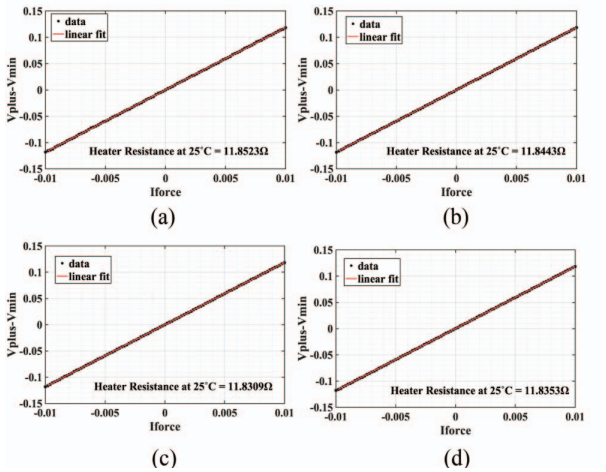

Fig. 11. The IV characterization results of 4 sample microheaters (50 nm Pt).

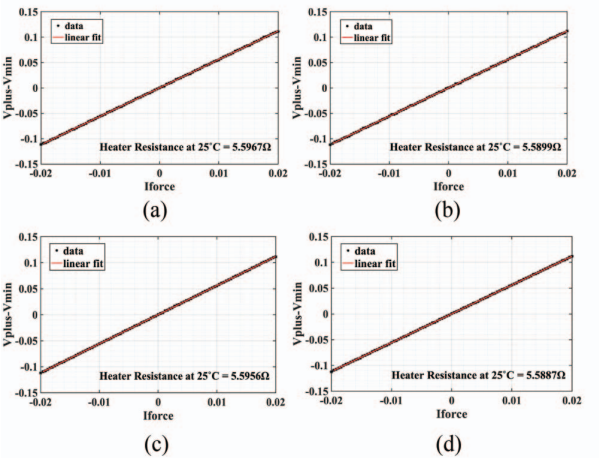

Fig. 12. The IV characterization results of 4 sample microheaters (100 nm Pt).

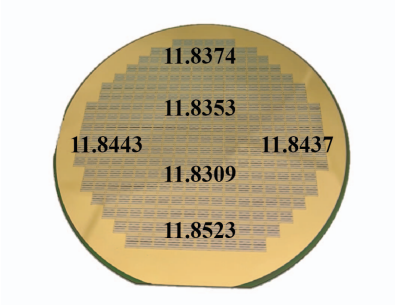

Fig. 13. The resistance distribution of TTC microheaters in 50 nm technology (Ω).

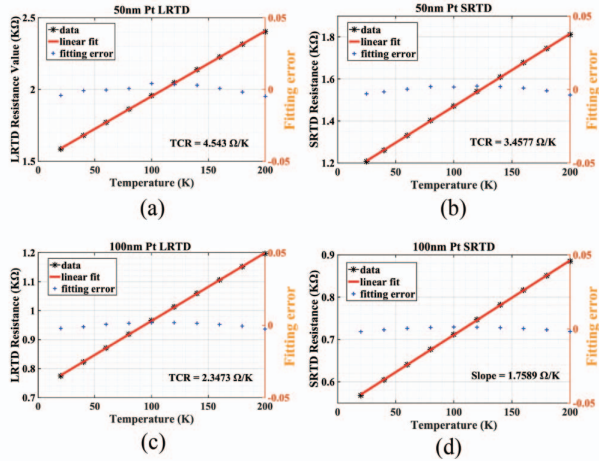

Fig. 14. The RTD sensor characterization (a) 50 nm Pt LRTD (b) 50 nm Pt SRTD (c) 100 nm Pt LRTD (d) 100 nm Pt SRTD.

IV. Conclusion

The proposed SiC TTC, including resistive platinum (Pt) microheaters and temperature sensors, allows for a wide range of in-situ thermal reliability investigations through online monitoring of the internal junction-to-case thermal resistance in harsh environments. The device could serve as a reliable

platform for the further development of power-electronic packages at elevated temperatures. For example, the proposed SiC TTC offers a fast and flexible approach for the transient dual interface test method (TDIM) to characterize and qualify nano-metallic sintered die-attach joints, and monitor the reliability of other novel packaging solutions.

The thin-film SiC TTC is designed in a reconfigurable format with a unit module of 4x4 mm^2, including six electrically isolated Pt microheaters with 12 Ω resistance and three Pt RTD sensors with 4.5 Ω/K sensitivity for tracking the junction temperature in reliability monitoring. The three RTD sensors provide thermal mapping with approximately 1 µm spatial resolution. The Cr-Au lift-off was carried out to realize 200 µm wire-bonding pads around each cell. In addition, the proposed SiC TTC layout can be transferred to other substrates such as GaN or diamond.

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TABLE I. SIC TTC PERFORMANCE COMPARISON

Parameter	*SiC TTC*	*[6]*
Thin-film Technology	50 nm	200 nm
Sensor Type	RTD	RTD
Sensor Precision	> 0.5˚C	N/A
Sensitivity (Ω/K)	4.5	N/A
Heater Type	Resistor	Resistor
Heater Uniformity (3σ)	21 mΩ	N/A
Cell Size (mm^2)	4 x 4	5 x 5
Resistance per Heater	11.84	N/A
Heaters per Cell	6	1
Sensors per Cell	3	1
Active Heater Area	82.5 %	~57 %

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