# Design of Multistandard Adaptive **Voltage-Controlled Oscillators**

Aleksandar Tasić, Wouter A. Serdijn, and John R. Long

Abstract-A multistandard/multiband adaptive voltage-controlled oscillator (VCO) satisfying the phase-noise requirements of both second- and third-generation wireless standards is described in this paper (1.8-GHz DCS1800, 2.1-GHz wide-band code division multiple access, and 2.4-GHz wireless local area network, Bluetooth, and digital enhanced cordless telecommunications standards). The design procedure for the VCO is based on an adaptive phase-noise model. A factor of 12 reduction in power consumption with a phase-noise tuning range of 20 dB is demonstrated by adapting the VCO bias to the desired application. The VCO achieves -123-, -110-, and -103-dBc/Hz phase noise at 1-MHz offset in a 2.1-GHz band at supply currents of 6, 1.2, and 0.5 mA, respectively.

Index Terms-Adaptive circuits, loop gain, multistandard (MS)/multiband (MB) circuits, phase noise, phase-noise tuning, voltage-controlled oscillators (VCOs).

#### I. INTRODUCTION

THE DEMANDS for new telecom services requiring higher capacities and data rates have motivated the development of broad-band third-generation (3 G) wireless systems. The coexistence of second- and third-generation cellular systems requires multimode, multiband (MB), and multistandard (MS) mobile terminals. To prolong talk time, it is desirable to share and/or switch transceiver building blocks in these handsets, without degrading the performance compared to single-standard transceivers.

It is possible to share circuits when different standards do not operate simultaneously. In these situations, considerable power can be saved by using circuits that are able to trade off power consumption for performance on the fly. However, MS frontends typically use duplicate circuit blocks or even entire radio front-ends for each standard. Although this approach is simpler to implement, it is neither optimal in cost, nor in power consumption [1]. For example, a voltage-controlled oscillator (VCO) that is designed to satisfy the most stringent specifications consumes more power than necessary when operating under more relaxed conditions [2].

Selection of the design parameters of an adaptive MS circuit is different from the design for a single standard. Therefore, an adaptive phase-noise model is introduced in this paper that accounts for a number of oscillator operating conditions and required specifications.

Referring to the adaptive phase-noise model, an adaptive second-generation (2 G)/3 G VCO that satisfies the phase-noise requirements of DCS1800, wide-band code division multiple access (WCDMA), wireless local area network (WLAN), Bluetooth, and digital enhanced cordless telecommunications (DECT) standards is described in this paper. Operating from a 3-V supply, a tuning range of 1.8-2.4 GHz is realized. The VCO phase noise at 1-MHz offset in a 2.1-GHz band is -123, -110, and -103 dBc/Hz for power consumption levels of 18, 3.6, and 1.5 mW, respectively. By adapting VCO power consumption to the desired operating scenario, the phase noise of the oscillator can be tuned over a 20-dB range with a factor of 12 reduction in power consumption.

An adaptive VCO is described in Section II. After a thorough examination of the contribution of all noise sources to the phase noise of an oscillator, an adaptive phase-noise model is introduced in Section III. The design procedure of an adaptive VCO is outlined in Section IV, while measurement results and concluding comments are presented in Sections V and VI, respectively.

# II. ADAPTIVE VCO

The quasi-tapped (QT) bipolar VCO [3], shown in Fig. 1, is used to implement the adaptive oscillator. It consists of a resonant LC tank and cross-coupled transconductor  $(Q_1, Q_2)$ , where L is the tank inductance,  $C_V$  is the varactor capacitance, and  $C_A$  and  $C_B$  are the quasi-tapping capacitances. Feedback via tapped capacitors maximizes the voltage swing across the LC tank, while active devices  $Q_1$  and  $Q_2$  remain far from heavy saturation. Moreover, freedom to set the base bias voltage  $V_B$ lower than the supply voltage  $V_{CC}$  allows for a large tank voltage, approaching the voltage swing of CMOS implementation.  $L_{RID}$  is degenerating inductor for the tail-current source (TCS). Degeneration of the current source is necessary to minimize the phase noise contributed by the bias circuit. The oscillation signal is delivered to the measurement equipment  $(50-\Omega \text{ input impedance})$  using an on-chip open-collector buffer and an external transformer balun (TR). Buffering the output from the bases rather than the LC tank allows the buffer to share the base bias voltage, thereby eliminating output coupling capacitors. Gain of the buffer is set by the emitter-degeneration resistance  $R_E$ .

The relationships between the parameters of the oscillator are summarized as

$$G_{TK} = \frac{R_L}{(\omega_0 L)^2} + \frac{1}{2} R_C (\omega_0 C_V)^2$$
  
$$n = 1 + \frac{C_A + C_\pi}{C_B}$$
(1)

Manuscript received April 21, 2004.

The authors are with the Electronics Research Laboratory/Delft Institute of Microelectronics and Submicrontechnology, Delft University of Technology, Delft 2628CD, The Netherlands (e-mail: a.tasic@ewi.tudelft.nl).

Digital Object Identifier 10.1109/TMTT.2004.840648



Fig. 1. QT VCO with open-collector buffer.

$$G_{M,TK} = -\frac{g_m}{2n}$$

$$G_{TK} = \frac{-G_{M,TK}}{k}$$

$$g_m = \frac{I_{TAIL}}{2V_T}$$

$$C_{TOT} = \frac{1}{2} \left( C_V + \frac{C_A C_B}{C_A + C_B} \right)$$

$$f_0 = \frac{1}{2\pi\sqrt{LC_{TOT}}}.$$
(3)

Here,  $R_L$  and  $R_C$  stand for the inductor L and the varactor  $C_V$  series loss resistances,  $G_{TK}$  for the effective tank conductance, n is the quasi-tapping factor,  $G_{M,TK}$  is the small-signal conductance seen by the LC tank,  $g_m$  is the transconductance of the bipolar transistors  $Q_1$  and  $Q_2$ ,  $C_{\Pi}$  is their base–emitter capacitance, k is the small-signal loop gain of the oscillator,  $I_{TAIL}$  is the tail current,  $f_0$  is the oscillation frequency, and  $V_T$  is the thermal voltage.

#### III. PHASE-NOISE MODEL OF AN ADAPTIVE OSCILLATOR

Phase noise of an oscillator is defined as the ratio of the noise power in a 1-Hz bandwidth at a frequency  $f_0 + \Delta f$  and the carrier power

$$\mathcal{L} = \frac{\bar{V}_{N,\text{TOT}}^2}{v_S^2}$$
$$\bar{V}_{N,\text{TOT}}^2 = |Z(f_0 + \Delta f)|^2 \bar{I}_{N,\text{TOT}}^2 = \frac{\bar{I}_{N,\text{TOT}}^2}{(4\pi C_{\text{TOT}}\Delta f)^2}.$$
(4)

 $\overline{V}_{N,\text{TOT}}^2$  and  $\overline{I}_{N,\text{TOT}}^2$  stand for the total voltage and current noise spectral densities at the output of the oscillator (*LC* tank),  $Z(f_0 + \Delta f)$  is the equivalent tank impedance at an offset



Fig. 2. QT-VCO noise sources (without degeneration).

frequency  $\Delta f$  from the resonant frequency  $f_0$ , and  $v_S$  is the amplitude of the voltage swing across the *LC* tank.

The noise sources of the QT VCO, with a TCS without degeneration, are shown in Fig. 2. These are the tank conductance noise  $\bar{I}_{GT}$ , the base-resistance  $(r_B)$  thermal noise  $\bar{V}_B$ , the collector  $\bar{I}_C$  and the base  $\bar{I}_B$  current shot noise, and the equivalent input voltage noise  $\bar{V}_{CS}$  of the current source transistor  $Q_{CS}$ 

$$\bar{I}_{GT}^2 = 4KTG_{TK} \tag{5}$$

$$\overline{V}_B^2 = 4KTr_B 
\overline{I}_C^2 = 2qI_C 
\overline{I}_B^2 = 2aI_B$$
(6)

$$\bar{V}_{\rm CS}^2 = 4KT \frac{1}{2g_{m,\rm CS}} [1 + 2r_{B,\rm CS}g_{m,\rm CS}].$$
 (7)

 $I_C$  and  $I_B$  stand for the collector and base currents,  $g_{m,CS}$  is the transconductance of the transistor  $Q_{CS}$ , and K is the Boltzmann's constant.

For the estimation of the phase noise of the QT VCO, the transfer of the indicated noise sources to the *LC* tank ( $\bar{I}_{N,\text{TOT}}$ ) must be known. Considering the transconductor as a nonlinear voltage-to-current converter (limiter) allows for the inclusion of all the noise-generating mechanisms in the oscillator. Namely, phenomena such as switching of the transconductor noise and the noise of the tail current source, both resulting in the folding of noise, can be understood.

# A. Time-Varying Transfer Function

The nonlinear voltage-to-current transfer function of the transconductor and its equivalent time-varying transconductance in the presence of a large driver signal are shown in Fig. 3 [4]. As long as the limiting of the oscillation  $(v_{\rm IN})$  does not occur, the transfer function of an accompanying small signal has a constant value g. When limiting occurs, the small-signal (e.g., noise) transfer reduces to zero. If the large-signal oscillation period is  $1/f_0$ , the period of a small signal time-varying gain  $g_{\rm IN}$  is  $1/2f_0$ . Considering the transfer from bases to the collectors of the transconductor  $Q_1-Q_2$ , the small-signal gain g is  $g_m/2$ .



Fig. 3. V-to-I and time-varying transfer functions.

Before evaluating the contribution of the various noise sources to the phase noise of the oscillator, let us first estimate the duty cycle d (Fig. 3) of the time-varying gain.

If  $v_{S,B}$  is the voltage swing of the oscillation signal across the bases of the transconductor, and  $\pm 2\alpha V_T$  is the linear region of the limiter, the duty cycle of the time-varying gain can be expressed as

$$d = \frac{2}{\pi} \arcsin\left(\frac{2\alpha V_T}{v_{S,B}}\right). \tag{8}$$

With the aid of (2), the voltage swing across the tank (a product of the tank resistance  $1/G_{TK}$  and the first Fourier coefficient of the current  $I_{TAIL}$ ) equals

$$v_S = \frac{8}{\pi} n k V_T = n v_{S,B}.$$
(9)

Assuming a 100-mV  $(\pm 2V_T)$  transconductor linear region ( $\alpha = 1$ ) and a large loop-gain value ( $k \gg 1$ ), the duty cycle d without loss of generality can be written as

$$d = 1/2k. \tag{10}$$

#### B. Base-Resistance Noise

r

The noise from the transistors  $Q_1$  and  $Q_2$  (both contributions) is switched on/off with the frequency of time-varying gain  $g_{IN}(2f_0)$ . As a consequence, noise folding occurs, i.e., noise from a number of frequencies is converted into the noise at one frequency. The harmonic components of the white base-resistance noise (multiples of  $f_0$ ) and the components of the timevarying gain are shown in Fig. 4.

As a result of the noise folding, the base noise  $(2r_B)$  at odd multiples of the oscillation frequency is converted to the *LC* tank at the resonance frequency, as given by the following:

$$\bar{I}_{TK,VB}^2 = 2\left(g_0^2 + 2\sum_{m=1}^{\infty} |g_{2m}|^2\right)\bar{V}_B^2 \qquad (11)$$

$$\sum_{n=-\infty}^{\infty} |g_{2m}|^2 = \frac{1}{T_2} \int_{-T_2/2}^{T_2/2} g_{\rm IN}^2(t) \, dt.$$
(12)

 $g_{2m}$  are the (complex) Fourier coefficients and  $T_2$  is the period of the transfer function  $g_{IN}(g = g_m/2)$ . With the aid of (2), the transferred noise density equals

$$\bar{I}_{TK,VB}^2 = 4KT \cdot kn^2 r_B G_{TK}^2.$$
<sup>(13)</sup>



Fig. 4. Base-resistance noise folding.

The contribution of the base-resistance noise at the output (*LC* tank) now becomes

$$\frac{I_{TK,VB}^2}{4KTG_{TK}} = nc\frac{k}{2} \tag{14}$$

where  $c = r_B g_{ms-up}$  and  $g_{ms-up}$  is the startup transconductance of the active devices  $Q_1$  and  $Q_2$ . This result is obtained with the aid of the equality

$$r_B G_{TK} = c/2n \tag{15}$$

that is derived from (2).

# C. Transconductor Shot Noise

By splitting the current noise sources, the collector and base current shot noise transform to the resonator as given by the following:

$$\bar{I}_{TK,ICB}^2 = \frac{\bar{I}_C^2}{2}d + \frac{1}{n^2}\left(1 - \frac{d}{2}\right)\bar{I}_B^2.$$
 (16)

The noise sources of both transistors are active for a fraction d of the period  $T_0(1/f_0)$ , whereas for the rest of the period, the noise sources of only one transistor are active. With the aid of (6), (10), and (16), the contribution of the transconductor shot noise becomes

$$\frac{\bar{I}_{TK,ICB}^2}{4KTG_{TK}} = \frac{n}{4}.$$
(17)

The same result would be obtained if switching of the shot noise is considered. Namely, the transconductor shot noise, when both transistors are active, turns on and off with the rate of the transfer function  $g_{\text{IN}}$  (Fig. 2 with g = 1). Referring to (12), this would lead to (17) as well.

#### D. Tail-Current Noise (TCN)

The harmonic components of the equivalent TCN (multiples of  $f_0$ ) and the components of the ideal switcher are shown in Fig. 5.

The noise of the biasing current source is modulated by the oscillator switching action. Therefore, the TCN around even multiples of the resonant frequency is folded back to the



Fig. 5. TCN folding.

resonator noise at the oscillation frequency as given by the following:

$$\bar{I}_{TK,CS}^2 = \frac{1}{4} 2(1-d) \sum_{m=0}^{\infty} |a_{2m+1}|^2 \bar{I}_{CS}^2 \quad \bar{I}_{CS}^2 = g_{m,CS}^2 \bar{V}_{CS}^2.$$
(18)

Here,  $I_{CS}^2$  is the output noise current density of the TCS and  $a_{2m+1}$  are the (complex) harmonic components of the squarewave ( $\pm 1$  ideal switch). To account for the finite switching time, a factor 1 - d is added, as the tail current noise does not contribute to the phase noise when transistors  $Q_1$  and  $Q_2$  are simultaneously active. The factor 1/4 originates from the active transistors load impedance  $(1/2G_{TK})$ .

By combining (7) and (18), and using the well-known weights of the square-wave amplitude components

$$\frac{\pi^2}{8} = 1 + \frac{1}{3^2} + \frac{1}{5^2} + \frac{1}{7^2} \cdots$$
(19)

the transferred TCN density equals

$$\overline{I}_{TK,CS}^2 = KTg_m[1 + 2r_Bg_m].$$
(20)

Finally, with the aid of (2), (15), and (20), the contribution of the TCN to the phase noise becomes

$$\frac{I_{TK,CS}^2}{4KTG_{TK}} \cong \frac{nk}{2}(1+2kc). \tag{21}$$

## E. Oscillator Total Noise

Considered to be uncorrelated, all noise sources, viz., the tank conductance noise, base resistance noise, transconductor shot noise, and TCN add to the equivalent output noise, as given by the following:

$$\bar{I}_{TK,TOT}^2 = \bar{I}_{TK,GT}^2 + \bar{I}_{TK,VB}^2 + \bar{I}_{TK,ICB}^2 + \bar{I}_{TK,CS}^2.$$
 (22)

Now, the noise factor F of the oscillator is

$$F = \frac{I_{TK,TOT}^2}{4KTG_{TK}} = 1 + \frac{n}{4} + \frac{nc}{2}k + \frac{n}{2}k(1+2kc).$$
 (23)

From (23), it can be observed that the contribution of the TCS noise to the phase noise of the VCO (Fig. 1) is larger than all other contributions together [5]–[7]. Denoting the contribution

of the active part noise and the tank resistance noise as  $1 + A_{AP}$ , and the contribution of the TCN as  $A_{CS}$ , we can define the phase-noise difference (PND) as the ratio of the corresponding noise contributions (24) as follows:

$$PND = 1 + \frac{A_{CS}}{1 + A_{AP}}.$$
 (24)

Referring to (24), the PND becomes

$$PND = 1 + \frac{1}{2} \frac{nk(1+2kc)}{1+n/4+nck/2}.$$
 (25)

The PND compares the contributions of the TCN and all other noise sources. If n = 1.4 and c = 0.1 (VCO design data), then for a loop gain, k = 10, PND = 11.2. In other words, the TCS degrades the phase-noise performance of the VCO by 10.5 dB.

## F. Resonant-Inductive Degeneration (RID)

Recognizing that the bias current noise at  $2f_0$  has the largest impact, RID [8] is employed to minimize the TCN contribution. The procedure relies on forming a resonance between the degenerating inductor ( $L_{RID}$ ) and the base–emitter capacitance of the TCS at twice the oscillation frequency.

As the input impedance of an inductively degenerated transistor equals [9],

$$Z_{\rm IN}(f) = 2\pi f_{T,\rm CS} L_{RID} + j \left[ 2\pi f L_{RID} - \frac{f_{T,\rm CS}}{f} \frac{1}{g_{m,\rm CS}} \right]$$
(26)

the imaginary part is set to zero at  $2f_0$  when condition (27) is satisfied as follows:

$$R_{\rm IN}g_{m,\rm CS} = \left(\frac{f_{T,\rm CS}}{2f_0}\right)^2.$$
 (27)

Here,  $f_{T,CS}$  is the TCS transistor transit frequency, and  $R_{IN} = 2\pi f_{T,CS} L_{RID}$  is the real part of the impedance seen at the base of the current source transistor.

Now, the transfer function of the TCS base-resistance noise (i.e., the equivalent transconductance of the RID current–source transistor) to the output current noise of the degenerated TCS at  $2f_0$  equals [9]

$$g_{\rm EQ} \cong -\frac{1}{R_{\rm IN}} \frac{f_{T,\rm CS}}{2f_0}.$$
 (28)

The TCS collector-current shot noise is suppressed, while the base-current shot noise is completely transferred to the output of the current source because at  $2f_0$  the TCS transistor  $Q_{\rm CS}$  operates in a common base-like configuration. Combining these contributions, the total output noise density of the RID TCS becomes

$$\bar{I}_{\text{CS},RID}^2 = g_{\text{EQ}}^2 \bar{V}_{B,\text{CS}}^2 + \bar{I}_{B,\text{CS}} < \left(\frac{2f_0}{f_{T,\text{CS}}}\right)^2 \bar{I}_{\text{CS}}^2 \qquad (29)$$

where  $\bar{V}_{B,CS}$  and  $\bar{I}_{B,CS}$  stand for the TCS base-resistance and base-current noise sources. Equation (29) implies that by applying RID, the contribution of the TCN at  $2f_0$  is reduced by more than a factor of  $(f_{T,CS}/2f_0)^2$ .

Referring to the example of this section, i.e., n = 1.4, c = 0.1, and k = 10, the applied RID results in a factor of 40 TCN suppression (VCO design data). The calculated PND reduces to 1.1 dB after the degeneration, which is an improvement of 9.4 dB. The simulations predict an improvement of 7 dB and PND = 2 dB [see (24)] for this low loop-gain value.

For larger loop-gain values (in the current design  $k_{\text{MAX}}$  = 19) and, accordingly, larger  $f_T$ 's of the transistors, a factor of 100 bias-noise suppression is expected, making the noise contribution of the TCS almost negligible. Therefore, the noise factor of the VCO with RID of the bias TCS reduces to

$$F = 1 + \frac{n}{4} + \frac{nc}{2}k.$$
 (30)

# G. Phase-Noise Tuning Model

When the noise contributed by the bias circuit is negligible, the oscillator phase-noise performance depends on the components in the ac signal path, viz., transconductance cell and resonator. With the aid of (4), (9), (22), and (30), the adaptive phase-noise model becomes

$$\mathcal{L} \propto \frac{1 + n/4 + nck/2}{n^2k^2}.$$
(31)

This model is parameterized with respect to power consumption via loop gain k. Unlike fixed hardware determined design parameters, the loop gain and voltage swing can be varied by changing current  $I_{\text{TAIL}}$ , shown in Fig. 1. This allows adaptation of the oscillator phase noise to different specifications. The phenomenon is named *phase-noise tuning* [10], while the figure-ofmerit describing the oscillator's adaptivity to phase noise is the phase-noise tuning range (PNTR). For a  $k_2/k_1$ -times change in power consumption, the PNTR is defined as

PNTR
$$(k_1, k_2) \propto \frac{k_1^2}{k_2^2} \frac{1 + n/4 + nck_2/2}{1 + n/4 + nck_1/2}.$$
 (32)

Once the minimum and maximum attainable loop gains are known, the ranges of the power-consumption and phase-noise adaptation can be determined. For example, if n = 1.4, c = $0.1, k_{\text{MIN}} = 2$ , and  $k_{\text{MAX}} = 19$  (VCO design data), (32) predicts that 17.4 dB of the phase noise can be traded for a factor of ten savings in power consumption.

#### **IV. DESIGN FOR ADAPTIVITY**

Selection of the design parameters for an adaptive multistandard oscillator is different from the design for a single standard. The design of an adaptive MS/MB VCO (i.e., DCS1800/WCDMA/WLAN–Bluetooth–DECT) will be outlined here.

The phase-noise requirements (decibels relative to a carrier/hertz at 1–MHz offset in receive modes) for five different standards are listed in Table I [11]–[15]. We will refer to the DCS1800 standard as a phase-noise demanding (PN-D) standard, to the WCDMA, WLAN, and Bluetooth standards as phase-noise moderate (PN-M) standards, and to the DECT standard as a phase-noise relaxed (PN-R) standard.

Given the phase-noise requirements listed in Table I, the phase-noise range between demanding (PN-D) and moderate

TABLE I MS/MB VCO REQUIREMENTS

MSVCO	DCS1800	WCDMA	WLAN	Bluet.	DECT
PN@1M	-123	-110	-110	-110	-100

(PN-M) modes is PNTR =  $123-110-20 \log(2.4 \text{ GHz}/1.8 \text{ GHz}) = 11 \text{ dB}$ . Taking into account the relaxed DECT mode (PN-R), the PNTR increases to  $123-100-20 \log(2.4/1.8) = 21 \text{ dB}$ . Therefore, a PNTR of 21 dB is targeted.

Having the effects of the noise from the biasing TCS eliminating by RID (27), the minimum and maximum loop gain kand tail current  $I_{\text{TAIL}}$  can be estimated from (32). Accordingly, the PNTR of 17.4 dB can be realized between the loop gain  $k_{\text{MIN}} = 2$  (safety startup) and  $k_{\text{MAX}} = 19$ . However, if  $k_{\text{MIN}}$ is 1.5, the tuning range extends to PNTR = 21.4 dB.

Once the maximum loop gain is known, the oscillator biasing can be determined. The choice of the base bias potential  $V_B$  is a compromise between a large output voltage swing and saturation of transconductor devices  $Q_1$  and  $Q_2$  (Fig. 1). For the maximum loop gain and lowest phase noise, a voltage swing of  $v_{S,B,MAX} = 1.2$  V is estimated from (9). Further, to avoid saturation of the transistors in the active part of the oscillator,  $v_{S,B}$ should satisfy

$$v_{S,B,MAX} \le 2 \frac{V_{CC} - V_B + V_{BE} - V_{CE,SAT}}{n+1}.$$
 (33)

This worst case condition is derived assuming the largest base and the lowest collector potential and, therefore, insures proper operation of the transistors in the active part *at all times*.  $V_{CC} =$ 3 V is the supply voltage,  $V_{BE}$  is the base–emitter voltage, and  $V_{CE,SAT}$  is the collector–emitter saturation voltage. For a capacitive quasi-tapping ratio n = 1.4, a base potential of  $V_B = 2.1$  V is finally obtained from (33).

The calculations indicate that a factor of ten reduction in power consumption can be realized between the PN-D and PN-R modes of the adaptive VCO under consideration.

### A. VCO Circuit Parameters

Tank inductor L = 3 nH is chosen as a compromise between low power consumption and high quality factor in the 2.1-GHz band. The inductor is fabricated using 4- $\mu$ m-thick aluminum top metal in a 50-GHz SiGe technology. The three-turn inductor has an outer diameter of  $d_{OUT} = 320 \ \mu$ m, a metal width of  $w = 20 \ \mu$ m, and a metal spacing of  $s = 5 \ \mu$ m.

The differentially shielded symmetric inductor uses a ladder metal filling scheme, as shown in Fig. 6 [16]. This improves the peak Q factor by 40%, but has only a minor effect on the inductor self-resonant frequency ( $Q_L = 25$  around 2.1 GHz). It also satisfies the aggressive metal fill restrictions in modern very large scale integration (VLSI) backend technologies without compromising RF performance.

The quality factor of the varactor can also limit the overall tank Q factor in an integrated oscillator. The quality factor of the collector-base varactor is estimated at  $Q_C = 40$  from simulation. The varactor consists of two base-collector diodes with 32 fingers, each 4- $\mu$ m wide and 20- $\mu$ m long.



Fig. 6. Shielded inductor layout (bottom view).



Fig. 7. MS VCO photomicrograph.

For a quasi-tapping ratio of n = 1.4, the metal-insulator-metal capacitances  $C_A = 150$  fF and  $C_B = 600$  fF are chosen. For effective suppression of the TCS noise,  $L_{RID}$  is set to 3.4 nH using the resonant-tuning design method outlined in Section III. The degeneration inductor is realized in the 0.85- $\mu$ m-thick second metal layer, as Q for this inductor is not of concern. The inductor outer diameter is  $d_{OUT} = 140 \ \mu$ m, metal width  $w = 6 \ \mu$ m, metal spacing is  $s = 1 \ \mu$ m, and it has seven turns. Finally, the open-collector output buffer is designed with an  $R_E = 750$ - $\Omega$  linearization resistor and a bias current  $I_B = 1.1$  mA.

## V. MEASUREMENT RESULTS

The chip photomicrograph is shown in Fig. 7. It occupies an area of  $700 \times 970 \,\mu \text{m}^2$  including the bondpads. Wire bonded in a 20-lead RF package, the chip is tested in a metal fixture with filtering on all bias and supply lines, as shown in Fig. 8. On the test board, three-stage low-pass *LC* filters designed remove low-frequency noise originating from the power supply and bias interconnections. Heavy filtering of the supply and bias lines is needed to remove spurs from the VCO output caused by pick-up from the supply and tuning lines. This unwanted interference



Fig. 8. Packaged integrated circuit (IC) on a printed circuit board (PCB) in test fixture.



Fig. 9.  $f_0$ -tuning curve for a 3-V tuning voltage.



Fig. 10. Phase noise at 1-MHz offset in the 2.1-GHz band.

modulates the VCO in both phase and frequency, making accurate phase-noise measurements impossible without the employed filtering on bias lines.

For a 3-V supply, the frequency tuning range of 600 MHz (i.e., output from 1.8 to 2.4 GHz) is measured, as shown in Fig. 9. This frequency range covers all the bands of interest.

Plots of the measured phase noise at 1-MHz offset in the 2.1-GHz mid-frequency band are shown in Fig. 10. Due to the

TABLE II OSCILLATOR PERFORMANCE IN 2.1-GHz BAND

PhaseNoise@1MHz	Loop gain	I <sub>TAIL</sub>
-123dBc/Hz	20	6mA
-108dBc/Hz	3	0.9mA
-103dBc/Hz	1.7	0.5mA

TABLE III POWER-CONSUMPTION AND TUNING-RANGE FIGURES-OF-MERIT

Reference	Process	<i>FOM</i> 1 [dB]	<i>FOM</i> 2 [dB]
[17]	SiGe	178	148
[18]	SiGe	174	148
[19]	CMOS	172	152
[20]	CMOS	183	150
This work	SiGe	178	167

degeneration resistor  $R_E = 750 \ \Omega$  in the output buffer, an output signal in order of  $-20 \ \text{dBm}$  (maximum) is measured in a 50- $\Omega$  system. This results in a noise floor for the phase-noise measurement of  $-130 \ \text{dBc/Hz}$ , as shown in Fig. 10.

The operating conditions accompanying the measurements shown in Fig. 10 are listed in Table II. As can be seen from Table II, by adapting the bias tail current from 0.5/0.9 mA to 6 mA, a PNTR of 20 dB/15 dB is achieved. This satisfies the requirements of five different wireless standards, as desired.

Note that following the measured phase-noise slope in the range 100 kHz–1 MHz, a phase noise better than -133 dBc/Hz at a 3-MHz offset is expected, fulfilling the most stringent DCS1800 requirement (in a receive mode) at this offset as well.

The power-consumption figure-of-merit FOM1 =  $\mathcal{L}(\Delta f_{\text{OFFSET}}/f_0)^2 V_{CC} I_{\text{TAIL}} = 178$  and the tuning-range figure-of-merit FOM2 = FOM1 $(f_0/\Delta f_{\text{TUNE}})^2 = 167$  of the oscillator under consideration are compared with other designs from the recent literature in Table III (modulus: decibels). The adaptive VCO shows a good compromise between phase-noise and frequency-tuning performance. Referring to Leeson's phase-noise formula (34),

$$\mathcal{L} = F \frac{KT}{2P_{\text{SIGNAL}}} \frac{1}{Q_{\text{TANK}}^2} \left(\frac{f_0}{\Delta f_{\text{OFFSET}}}\right)^2 \qquad (34)$$

FOM2 appears to be a useful VCO figure-of-merit. It accounts for the frequency dependency of the phase noise, as well as the power consumption and tuning range of the oscillator, the latter related to the LC tank Q factor.

# VI. CONCLUSION

By sharing functional blocks among different standards, adaptive MB/MS front-end circuits offer reduced complexity, power consumption, chip area, and overall cost.

The adaptive phase-noise model establishes a relationship between the oscillator performance parameters (phase noise, loop gain, voltage swing, and power consumption). A concept of phase-noise tuning is used to design an adaptive oscillator. The 2 G/3 G adaptive VCO, operating in DCS1800, WCDMA and WLAN–Bluetooth–DECT bands, satisfies the phase-noise requirements of these standards at 18-, 3.6-, and 1.5-mW power consumption, respectively.

#### REFERENCES

- J. Ryynanen, K. Kivekas, J. Jussila, A. Parssinen, and K. Halonen, "A dual-band RF front-end for WCDMA and GSM applications," in *Proc. Custom Integrated Circuits Conf.*, May 2000, pp. 175–178.
- [2] D. Wang *et al.*, "A fully integrated GSM/DCS/PCS Rx VCO with fast switching auto-band selection," in *Proc. Radio Wireless Conf.*, Aug. 2002, pp. 209–212.
- [3] A. Tasić, W. A. Serdijn, and J. R. Long, "Multi-standard/multi-band adaptive voltage-controlled oscillator," in *Proc. RF Integrated Circuits*, Jun. 2004, pp. 135–138.
- [4] C. A. M. Boon, "Design of high-performance negative feedback oscillators," Ph.D. dissertation, Delft Univ. Technol., Delft, The Netherlands, 1989.
- [5] J. J. Rael and A. Abidi, "Physical Processes of phase-noise in differential *LC* osillators," in *Proc. Custom Integrated Circuits Conf.*, May 2000, pp. 569–572.
- [6] E. Hegazi et al., "Filtering technique to lower oscillator phase-noise," in Proc. Int. Solid-State Circuits Conf., Feb. 2001, pp. 364–365.
- [7] P. Andreani and H. Sjoland, "Tail current noise suppression in RF CMOS VCOs," in *IEEE J. Solid-State Circuits*, vol. 37, Mar. 2002, pp. 342–348.
- [8] A. Tasić, W. A. Serdijn, and J. R. Long, "Resonant-inductive degeneration of voltage-controlled oscillator's tail-current source," in *Proc. Int. Circuits Systems Symp.*, May 2003, pp. 673–676.
- [9] —, "Matching of low-noise amplifiers at high frequencies," in *Proc. Int. Circuits Systems Symp.*, May 2003, pp. 321–324.
- [10] A. Tasić and W. A. Serdijn, "Concept of phase-noise tuning of bipolar VCOs," in *Proc. Int. Circuits Systems Symp.*, May 2002, pp. 161–164.
- [11] Digital Cellular Communication System, ETSI Standard, 1997.
- [12] UE Radio Transmission and Reception (FDD), 3GPP Standard, 2000. [Online]. Available: http://www3gpp.org.2000.
- [13] Wirelss Local Area Network, IEEE Standard 802.11b-1999, 1999.
- [14] Specifications of the Bluetooth System, ver. 1.1, 1999.
- [15] Digital European Cordless Telecommuncaitions, ETSI Standard, 1999.
- [16] T. S. D. Cheung *et al.*, "Differentially-shielded monolithic inductors," in *Proc. Custom Integrated Circuits Conf.*, Sep. 2003, pp. 95–98.
- [17] J. O. Plouchart *et al.*, "3 V SiGe differential VCO for 5 GHz and 17 GHz wireless applications," in *Proc. Eur. Solid-State Circuits Conf.*, 1998, pp. 332–335.
- [18] M. Soyuer et al., "An 11 GHz 3 V SiGe VCO with integrated resonators," in Proc. Int. Solid-State Circuits Conf., Feb. 1997, pp. 1451–1454.
- [19] A. Mostafa et al., "A sub-1 V 4 GHz VCO and 10.5 GHz oscillator," in Proc. Eur. Solid-State Circuits Conf., 2000, pp. 312–315.
- [20] H. Wang et al., "A 50 GHz VCO in 0.25 µm CMOS," in Proc. Int. Solid-State Circuis Conf., Feb. 2001, pp. 372–373.



Aleksandar Tasić received the M.Sc. (Ir. Engineer) degree in electrical engineering from the University of Nis, Nis, Serbia, in 1998, and is currently working toward the Ph.D. degree at the Delft University of Technology, Delft, The Netherlands.

He was a Research Assistant with the University of Nis until 2000. He then joined the faculty of Electrotechnics, Mathematics and Informatics, Electronics Research Laboratory/Delft Institute of Microelectronics and Submicrontechnology (DIMES), Delft University of Technology. His

research interest includes adaptive and MS RF front-end circuits for wireless communications with an emphasis on adaptive VCOs. His research also includes RF front-end system study, with a particular interest in the optimal distribution of specifications to RF front-end circuit blocks.



**Wouter A. Serdijn** was born in Zoetermeer ("Sweet Lake City"), The Netherlands, in 1966. He received the Ingenieurs (M.Sc.) and Ph.D. degrees from the Delft University of Technology, Delft, The Netherlands, in 1989 and 1994, respectively.

Since 2002, he has been a Workpackage Leader on the freeband impulse project AIR-LINK, which is aimed at high-quality wireless short-distance communication employing ultra-wideband (UWB) radio. He co-edited and coauthored *Research Perspectives* on *Dynamic Translinear and Log-Domain Circuits* 

(Boston, MA: Kluwer, 2000), Low-Voltage Low-Power Analog Integrated Circuits (Boston, MA: Kluwer, 1995), and Dynamic Translinear and Log-Domain Circuits (Boston, MA: Kluwer, 1998). He has also authored or coauthored over 150 publications and presentations. He teaches analog electronics for electrical engineers, micropower analog IC techniques and electronic design techniques. His research interests include low-voltage, ultra-low-power, high-frequency, and dynamic-translinear analog ICs along with circuits for RF and UWB wireless communications, hearing instruments, and pacemakers.

Dr. Serdijn has served as an associate editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART II: ANALOG AND DIGITAL SIGNAL PROCESSING, as tutorial session co-chair for the International Circuits and Systems Symposium (ISCAS'2003), as analog signal processing track co-chair, for ISCAS'2004, and as chair of the Analog Signal Processing Technical Chapter of the IEEE Circuits and Systems Society. He is currently an associate editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART I: FUNDAMENTAL THEORY AND APPLICATIONS, as analog signal processing track co-chair for the International Conference on Electronic Circuits and Systems (ICECS'2004), as Technical Program Committee member for the 2004 International Workshop on Biomedical Circuits and Systems, and as analog signal processing track co-chair for ISCAS'2005.



**John R. Long** received the B.Sc. degree in electrical engineering from the University of Calgary, Calgary, AB, Canada, in 1984, and the M.Eng. and Ph.D. degrees in electronics engineering from Carleton University, Ottawa, ON, Canada, in 1992 and 1996, respectively.

For ten years he was with Bell-Northern Research, Ottawa (now Nortel Networks), where he was involved in the design of application-specific integrated circuits (ASICs) for gigabit/second fiber-optic transmission systems. For five years he was with

the University of Toronto. In January 2002, he joined the faculty of the Delft University of Technology, Delft, The Netherlands, where he is currently Chair of the Electronics Research Laboratory. His current research interests include low-power transceiver circuitry for highly integrated radio applications and electronics design for high-speed data communications systems.

Prof. Long currently serves on the Technical Program Committees of the International Solid-State Circuits Conference (ISSCC), the European Solid-State Circuits Conference (ESSCIRC), the IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM), and GAAS2004 European Microwave Symposium. He was an associate editor for the IEEE JOURNAL OF SOLID-STATE CIRCUITS. He was the recipient of the Natural Sciences and Engineering Research Council of Canada (NSERC) Doctoral Prize, the Douglas R. Colton and Governor General's Medals for research excellence, and the ISSCC 2000 and IEEE BCTM 2003 Best the Paper Awards.