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A Modified PV to Virtual Bus Parallel Differential Power Processing Architecture for Photovoltaic Systems

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***Abstract*—This paper proposes a simplified parallel differential power processing (PDPP) architecture for photovoltaic (PV) systems that reduces hardware complexity by eliminating one dual active bridge (DAB) converter and one intermediate bus capacitor from the previously introduced PV2VB PDPP two-string architecture. In the reference PV2VB PDPP architecture, each PV string is interfaced with its own string-level converter (SLC), comprising a DAB and a bridgeless (BL) converter, for maximum power point tracking (MPPT) and differential power exchange via a shared virtual bus. The proposed topology maintains the use of bridgeless converters for each PV string but replaces the two DAB stages with a single dual-bridge DAB converter, which connects one intermediate bus on one side and the virtual bus on the other. This approach maintains isolation and bidirectional power flow, while significantly reducing the number of magnetic components, switches, and control loops. Simulation results demonstrate that the system can reach and sustain steady-state operation of the virtual bus under various mismatch conditions, validating the effectiveness of the proposed architecture in ensuring power balance and enabling string-level MPPT. The results suggest that the proposed scheme preserves the key benefits of the PV2VB PDPP framework, while simultaneously reducing overall system cost.**

***Index Terms*—Differential power processing (DPP), maximum power point tracking (MPPT), photovoltaic (PV) system, photovoltatronics.**

I. Introduction

Photovoltaic (PV) systems have emerged as a foundation technology in the global transition to renewable energy, thanks to their environmental benefits, long service life, and decreasing cost trends [1], [2], [3], [4], . Traditional centralized PV architectures, while simple and cost-effective, suffer from significant drawbacks including mismatch losses due to shading, soiling, or module aging, which can severely compromise energy yield [5], [6].

To address these limitations, various distributed maximum power point tracking (DMPPT) approaches have been proposed. It can be separated into full power processing (FPP) and differential power processing (DPP) [7]. Despite the fact that FPP is a mature technology, it handles the entire power output generated by the PV strings. Notably, the DPP architectures enable only a fraction of the total power to be processed by converters, thereby enhancing system efficiency and reducing component stress [8], [9]. The two main categories of DPP are: the series differential power processing (SDPP) [10] and the parallel differential power processing (PDPP) [1] architectures, as shown in Fig. 1. SDPP architectures are designed to control the differential current between individual PV modules ($i_{\mathrm{PV}_{Mj}}$) and the string current ($i_{\mathrm{PV}_{Sj}}$), thereby reducing mismatch-related power losses in series-connected photovoltaic elements. However, these architectures fall short in mitigating mismatch losses across parallel-connected PV strings [11]. PDPP has gained attention for its ability to mitigate mismatch losses among PV strings connected in parallel [1], [12], [13], [14], [15].

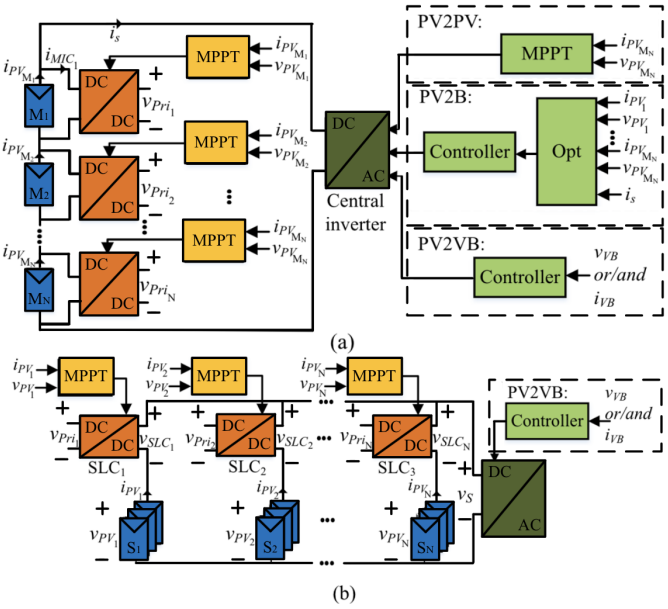


Fig. 1: PV systems using different differential power processing approaches: (a) series DPP, (b) parallel DPP [15].

In this context, the PV to Virtual Bus (PV2VB) PDPP architecture introduced by [1], [12], [13], represents a significant advancement. By replacing the traditional high-voltage bus with a virtual low-voltage bus, and employing dual-

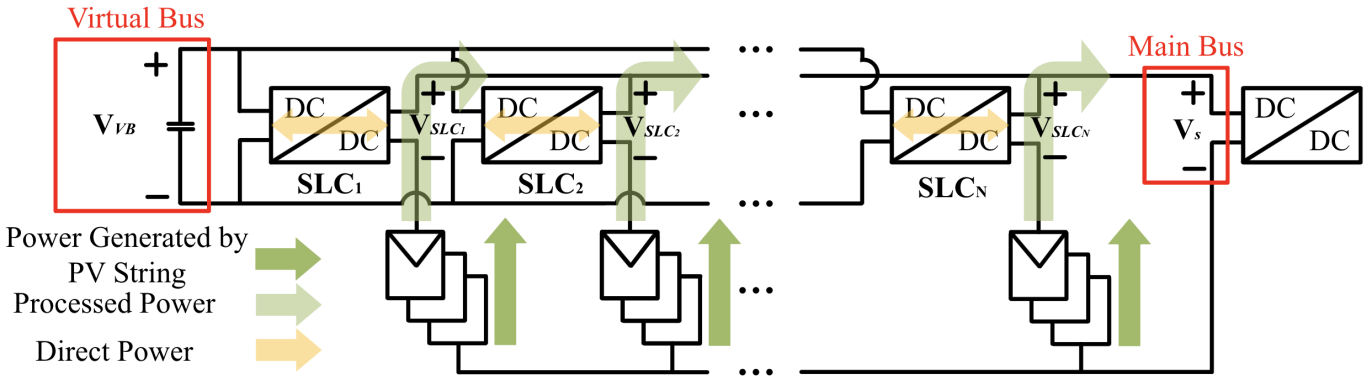


Fig. 2: PV systems using the proposed PV2VB PDPP architecture [1].

active bridge (DAB) converters followed by bridgeless (BL) converters as string-level converters (SLCs), the architecture achieves both improved scalability and reduced converter voltage ratings. The system processes only the differential power between PV strings and the virtual bus, enabling string-level MPPT with converter efficiencies between 96.4% and 99%.

Building on this architecture, this paper proposes a simplification by eliminating one of the DAB converters in one of the SLCs and one of the intermediate bus capacitors. The proposed architecture reduces system complexity and potential cost while maintaining the core benefits of the PDPP approach.

II. Overview of the PV2VB PDPP Architecture

References [1], [12], [13] provide all the necessary information regarding the architecture. As shown in Fig. 1, the proposed PV2VB PDPP system connects the inputs of the SLCs to a common, isolated DC line called the virtual bus. To keep the system running smoothly and avoid voltage changes on the virtual bus, it's important to maintain a balance of power over the virtual bus. This means that while some PV strings send power into the virtual bus through the SLCs, others must take power from it. The system has two main goals: (i) keeping the virtual bus voltage stable, which is managed by the central converter, and (ii) allowing each PV string to track its maximum power point (MPP) on its own, which is handled by the SLCs.

The broad scheme is the implementation of more than 2 PV strings. Therefore, a central converter, a virtual bus, and the full SLCs are needed to achieve the required connection [15], [16], [17]. In many industrial applications, there are two MPPT inputs for connecting two PV strings. In the previously introduced PV2VB PDPP, two DAB converters followed by two BL converters are required. DAB converters contain many passive elements, which increase the complexity of the system. This paper investigates removing one of the DAB converters and one intermediate bus capacitor. The new architecture should produce the same steady-state at the virtual bus, as well as the MPP tracking at the PV strings. The next subsections will explain the initially proposed architecture, along with its significant components, and finally demonstrate the modified and final version.

A. Conventional PV2VB PDPP Configuration.

I. Central Converter

In the PV2VB PDPP system, the central converter controls the main bus voltage (v_S) by adjusting its duty cycle. Its main purpose is to maintain a stable virtual bus voltage (v_{VB}). For simplicity, the system is assumed to use ideal (lossless) converters, and the capacitive virtual bus is considered the primary energy storage element. The power balance in the system is given by:

$$P_{VB} = P_{\text{out}} - P_{\text{in}} \tag{1}$$

where P_{VB} is the virtual bus power, P_{out} is the power delivered to the main bus, and P_{in} is the power drawn from the PV strings. These terms are expressed as:

$$P_{VB} = C_{VB} \cdot v_{VB} \cdot \frac{dv_{VB}}{dt} \tag{2}$$

$$P_{\text{out}} = v_S \cdot i_S = v_S \cdot \sum_{j=1}^{N_{PV}} i_{PV_j} \tag{3}$$

$$P_{\text{in}} = \sum_{j=1}^{N_{PV}} v_{PV_j} \cdot i_{PV_j} \tag{4}$$

Here, C_{VB} is the virtual bus capacitance, N_{PV} is the total number of PV strings, and v_{PV_j} and i_{PV_j} are the voltage and current of the jth PV string, respectively. Substituting equations (2)–(4) into equation (1), the complete power balance becomes:

$$C_{VB} \cdot v_{VB} \cdot \frac{dv_{VB}}{dt} = \sum_{j=1}^{N_{PV}} v_{PV_j} \cdot i_{PV_j} - v_S \cdot i_S \tag{5}$$

The main bus current is naturally equal to the sum of the individual PV string currents. As a result, since PV strings' current and voltages are controlled by SLCs to make PV strings operate at their MPPs, the main bus voltage (v_S) becomes the only control variable available to regulate the virtual bus power and, therefore, the virtual bus voltage (v_{VB}).

When the average power of the virtual bus is zero, the steady-state condition can be expressed as:

$$P_{VB} = 0 \quad \Rightarrow \quad V_S^* = \frac{\sum_{j=1}^{N_{PV}} V_{PV_j} \cdot I_{PV_j}}{\sum_{j=1}^{N} I_{PV_j}} \qquad (6)$$
$$V_{VB} = \text{const}$$

Here, V_S^* represents the equilibrium main bus voltage that maintains a constant virtual bus voltage. Note that capital letters indicate steady-state quantities. By combining equations (5) and (6), the time derivative of the virtual bus voltage can be expressed as:

$$\frac{dv_{VB}}{dt} = \frac{\sum_{j=1}^{N_{PV}} V_{PV_j} \cdot I_{PV_j}}{C_{VB} \cdot v_{VB}} \cdot \left(1 - \frac{v_S}{V_S^*}\right) \qquad (7)$$

Equation 7 describes the dynamic behavior of the virtual bus voltage in response to deviations of the main bus voltage from its steady-state value. Specifically, the virtual bus voltage increases when v_S is lower than the equilibrium voltage V_S^*, and decreases when v_S exceeds V_S^*.

In this work, a boost converter is selected as the central converter topology due to its suitability for regulating the virtual bus voltage. The control is achieved indirectly by adjusting the converter's input voltage, which corresponds to the main bus voltage. This approach allows the central converter to maintain virtual bus stability by tracking variations in the main bus.

II. SLCs

In the PV2VB PDPP architecture, the primary role of the SLC is to ensure that each PV string operates at its Maximum Power Point (MPP). To achieve this, the SLC must also manage the bidirectional flow of power between the PV strings and the virtual bus [1]. As SLC, a DAB with a BL converter was utilized, since this topology meets three essential criteria: it operates in both the first and fourth quadrants of the voltage-current (V–I) characteristic, it behaves as voltage-source converters to interface with the virtual bus, and it provides electrical isolation from the virtual bus [1], [18], [19], [20]. The output voltage of the jth SLC can be written as:

$$v_{\text{SLC}_j} = v_S - v_{PV_j} \qquad (8)$$

Substituting (8) into the steady-state virtual bus power equation (5), we obtain:

$$P_{VB} = \sum_{j=1}^{N_{PV}} v_{\text{SLC}_j} \cdot I_{PV_j} = \sum_{j=1}^{N_{PV}} P_{\text{SLC}_j} = 0 \qquad (9)$$

This equation implies that, under steady-state conditions, the total power delivered by all SLCs to the virtual bus is zero. As a result, the SLCs have only one purpose, which is to redistribute energy among themselves. Given that I_{PV_j} is always positive, this condition indicates that some SLCs generate negative output voltages while others generate positive ones, depending on the power exchange required to regulate the virtual bus voltage.

The SLC duty cycle (d_{BL_j}) is determined by the MPPT algorithm. During the ON state of the switches, the voltage polarity before the j^{th} LC output filter ($v_{\text{SLC}_{BF_j}}$) aligns with the j^{th} intermediate bus voltage (v_{IB_j}), leading to the intermediate bus capacitor discharge with power equal to:

$$P_{\text{C}_{\text{IB}_{j_1}}} = v_{\text{IB}_j} \cdot i_{\text{PV}_j} \qquad (10)$$

When the switches are OFF, the BL converter inverts the intermediate bus voltage, and the capacitor is charged:

$$P_{\text{C}_{\text{IB}_{j_2}}} = v_{\text{IB}_j} \cdot (-i_{\text{PV}_j}) \qquad (11)$$

By considering (10) and (11), the average power processed by the intermediate bus capacitor over a switching period T_{sw} can be expressed as:

$$P_{\text{C}_{\text{IB}_j}} = \frac{1}{T_{\text{sw}}} \int_0^{d_{\text{BL}_j} T_{\text{sw}}} P_{\text{C}_{\text{IB}_{j_1}}}\, dt + \frac{1}{T_{\text{sw}}} \int_{d_{\text{BL}_j} T_{\text{sw}}}^{(1-d_{\text{BL}_j})T_{\text{sw}}} P_{\text{C}_{\text{IB}_{j_1}}}\, dt$$
$$= (2d_{\text{BL}_j} - 1) \cdot V_{\text{IB}_j} \cdot I_{\text{PV}_j} = V_{\text{SLC}_j} \cdot I_{\text{PV}_j} \qquad (12)$$

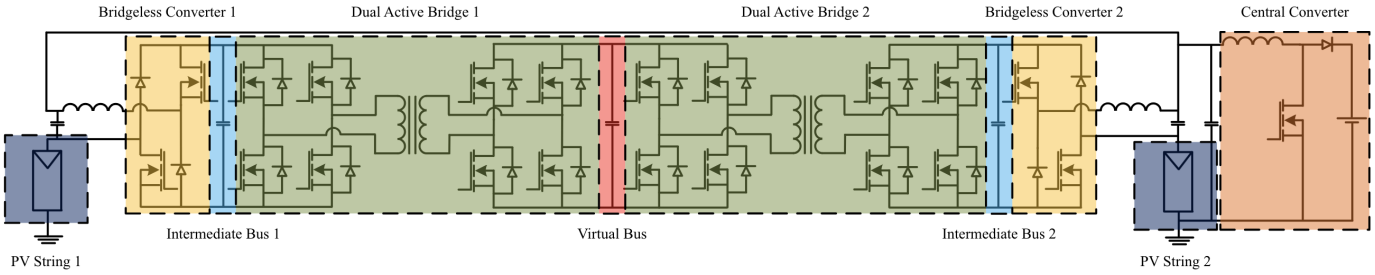
Here, $P_{\text{C}_{\text{IB}_j}}$ denotes the net power exchange between the intermediate bus and the PV string. To ensure positive power transfer from the virtual bus to the string—equivalent to applying a forward bias—it is necessary for the BL converter duty cycle d_{BL_j} to remain above 0.5. If the duty cycle drops below this threshold, the power direction reverses, causing energy to flow from the string back toward the virtual bus. This corresponds to a negative voltage being applied to the PV module [8], [15], [16].

B. Modified PV2VB PDPP Architecture for a PV System with Two PV Strings

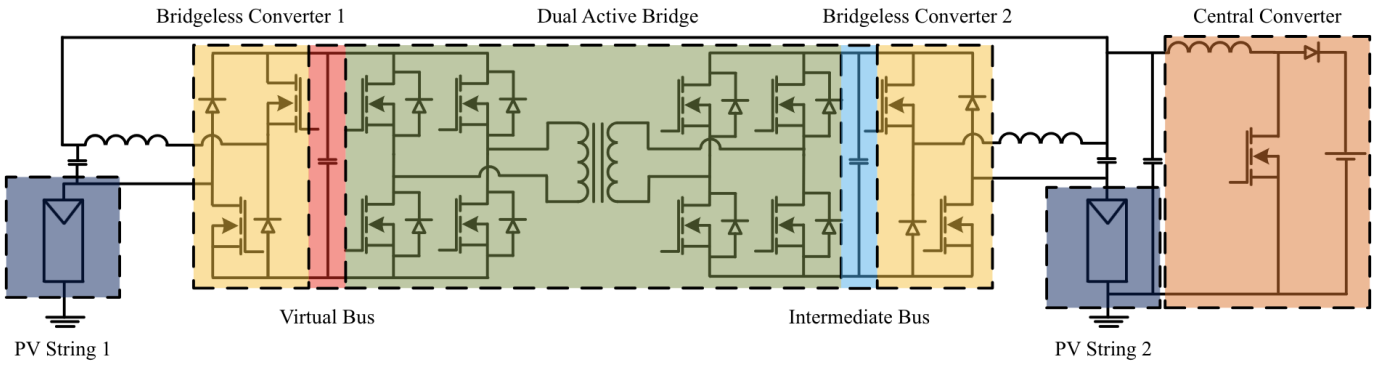
As illustrated in Fig. 3a, the original PV2VB PDPP architecture consists of two PV strings, two BL converters, DAB converters, two intermediate buses, a central boost converter, and a virtual bus connecting the two DAB converters. While this configuration effectively facilitates differential power processing and mitigates mismatch losses, it introduces additional system complexity and cost due to the presence of two DABs and two intermediate bus capacitors.

A simplified architecture is proposed in Fig. 3b, where one DAB converter and one intermediate bus capacitor are removed. The modified system retains the functional objectives of the original design while reducing the component count. In this architecture, a single DAB converter is used to perform bidirectional power exchange between the remaining intermediate bus and the virtual bus. The governing control principles remain consistent with the original architecture.

In this architecture, there are four main control objectives: (1) and (2) to track the Maximum Power Point (MPP) of the PV strings, and (3) and (4) to maintain the virtual bus and intermediate bus voltages at constant levels. To achieve these goals, four actuators are utilized—two BL converters, one DAB converter, and a central converter. The BL converters are responsible for tracking the MPP of their respective PV strings using a Perturb and Observe (P&O) algorithm. Meanwhile, the



(a)



(b)

Fig. 3: Proposed modification to the existing 2 PV-string architecture. (a) Conventional architecture using two DABs, two intermediate buses, and a virtual bus in the middle, (b) New architecture using one DAB, one intermediate bus on the right side, and a virtual bus on the left side.

virtual and intermediate bus voltages are regulated by closed-loop Proportional-Integral (PI) controllers.

Equation (12), which describes the power exchange between the intermediate bus and PV string 2, can be simplified as:

$$P_{C_{IB}} = (2 \cdot d_{BL_2} - 1) \cdot V_{IB} \cdot I_{PV_2} \tag{13}$$

On the virtual bus side, the dynamic power behavior remains defined by:

$$P_{VB} = C_{VB} \cdot v_{VB} \cdot \frac{dv_{VB}}{dt} \tag{14}$$

This revised architecture maintains the core advantages of the PV2VB PDPP system, including mismatch loss reduction and per-string MPPT, while achieving lower hardware complexity and improved implementation efficiency.

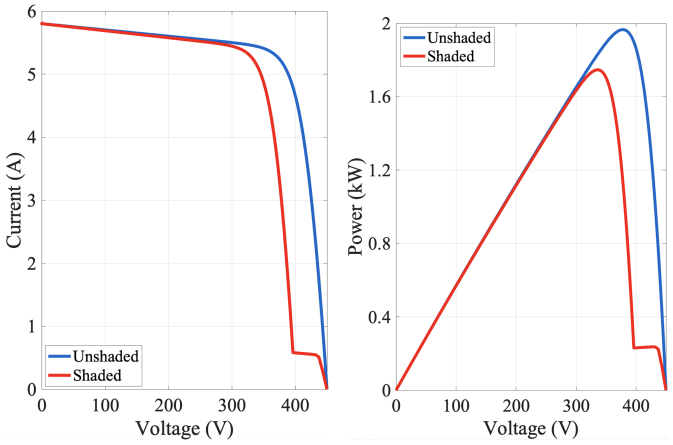
III. Results

This section demonstrates the capability of the proposed architecture to achieve MPPT at the string level without processing the full power generated by the PV strings. It also validates the ability of the system to maintain a regulated virtual bus voltage using fewer components compared to the previously introduced PV2VB PDPP. The electrical specifications and component values used for the simulation are summarized in Table I. The PV string behavior under different irradiance conditions is illustrated in Fig. 4, showing the current-voltage and power-voltage characteristics for shaded and unshaded conditions. The shaded case represents a partially shaded PV string consisting of nine modules connected in parallel, while the unshaded case represents an identically sized, fully illuminated string.

TABLE I: System Specifications and Component Parameters

Category	Parameter	Value
Electrical specifications	PV system rated power (P_{sys})	3.9 kW
	Virtual bus voltage (V_{VB})	200 V
	Nominal MPP voltage (V_{MPP})	378 V
	Nominal MPP current (I_{MPP})	5.2 A
	BL rated current (I_{SLC})	5.2 A
	BL rated voltage (V_{SLC})	200 V
	Number of PV strings (N_{PV})	2
	Switching frequency (f_{sw})	100 kHz
	Virtual Bus Capacitance (C_{VB})	12 mF
Components parameters	BL inductance (L_{BL})	660 μH
	BL capacitor (C_{BL})	100 μF
	DAB leakage inductor (L_{DAB_leak})	22 μH
	Boost inductor (L_S)	510 μH
	Bus capacitor (C_S)	7 μF

Two test cases were evaluated. In both cases, PV String 1 remains unshaded throughout, while PV String 2 changes conditions at t = 0.1 sec. In Scenario I, PV String 2 transitions from the unshaded to the shaded condition. In Scenario II, it begins in the shaded condition and transitions to the unshaded case at the same time.



(a) I-V Characteristics of PV Strings (b) P-V Characteristics of PV Strings

Fig. 4: Current-Voltage and Power-Voltage curves of PV strings under different shading conditions.

Figure 5 presents the simulation results for Scenario I. Prior to the transition, both PV strings operate near their nominal MPP voltages of approximately 378 V. At t = 0.1 s, PV String 2 becomes shaded, resulting in a sudden drop in its voltage to approximately 335 V. This causes a temporary imbalance in power between the strings, leading to a momentary 7V drop in the virtual bus voltage. However, the central converter responds quickly, and the virtual bus voltage recovers to the reference value of 200 V within approximately 0.7 s.

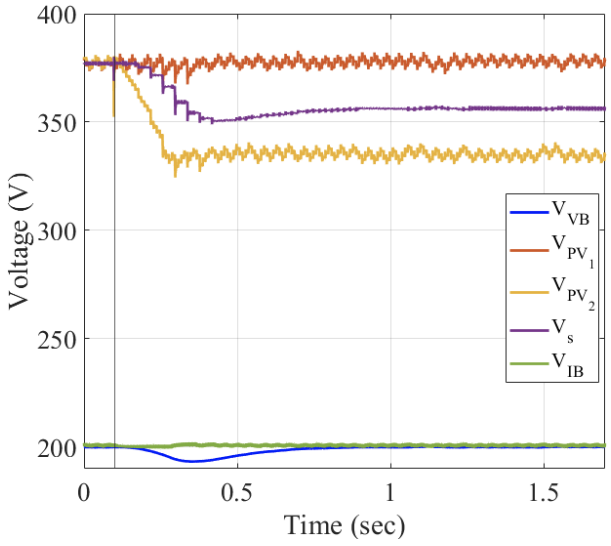


Fig. 5: Voltage waveforms. Scenario I: PV String 1 stays at unshaded curve, and PV String 2 transitions from I-V unshaded to shaded curve 2 at 0.1 sec.

The PV strings' voltages exhibit oscillations even in steady state due to the inherent behavior of the P&O algorithm. Additionally, the main bus voltage V_S displays discrete changes during transients, which result from the use of a discrete-time Proportional-Integral (PI) controller. To prevent interference between the central controller and to enable the MPPT algorithms to autonomously seek the MPP of the PV string, it is preferable to increase the sampling time of the central PI controller to minimize its interference with the MPPT algorithm as follows:

$$T_{VB} = 4 \cdot m \cdot T_{MPPT} \qquad \text{where } m = 1, 2, \ldots \tag{15}$$

where T_{VB} and T_{MPPT} represent the sampling time of the central PI controller and the perturbation period of the MPPT algorithm, respectively. Here, a 10ms perturbation period is selected for the P&O algorithm, and 40 ms for the sampling time of the central PI controller. It should be noted that there is no specific requirement for the sampling time of the PI controller for the DAB converter, which regulates the intermediate bus voltage. Therefore, its sampling time is chosen to match the switching frequency to avoid phase lag.

In Scenario II (Fig.6), PV String 2 starts under shaded conditions and transitions to the unshaded state at t = 0.1 s. This causes an immediate increase in PV string 2 voltage from 335 V to 378 V to track its MPPT. It causes the virtual bus voltage to temporarily overshoot by approximately 7V, followed by a smooth recovery within the same 0.7 s interval. Again, the control loops respond appropriately: the central converter increases its output to absorb the excess energy, and the MPPT algorithms stabilize both PV string voltages near their respective MPPs.

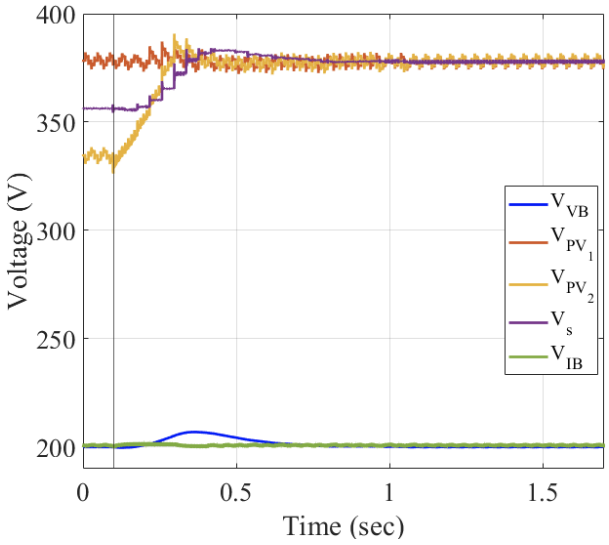


Fig. 6: Voltage waveforms. Scenario II: PV String 1 stays at unshaded curve, and PV String 2 transitions from I-V unshaded to shaded curve 2 at 0.1 sec.

In both scenarios, the virtual bus voltage remains within a tightly controlled range around the 200 V reference, verifying the effectiveness of the simplified control scheme. Additionally, the PV string voltages track their MPP targets accurately despite changes in shading conditions, and without centralized

full-power processing. The intermediate bus voltage (V_{IB}) remains relatively constant, further confirming the success of the decoupled architecture and power balancing mechanism.

IV. Conclusion

The article presented a modified version of a novel PV2VB PDPP architecture designed specifically for string-level MPPT for PV systems with two PV strings. The innovation of this project is the size reduction of the system compared to its predecessor, while it exhibited similar behavior. By removing one of the DABs and one intermediate bus capacitor, the system was able to find the MPP voltage at the BL converter level and regulate the virtual bus voltage at the desired value.

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