High voltage generator for eco-friendly plasma-disinfection of seeds

Subgroup thesis report, Bachelor Graduation Project

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Abstract

In a world where global warming is a growing issue, new solutions need to be found to reduce the carbon footprint. The same is true for the seed breeding industry, which uses energy inefficient ways of disinfecting seeds using hot water baths. A more eco-friendly solution would be the use of cold plasma treatment. This thesis proposes two designs for high voltage generators to achieve this goal. These include the supercascode switch for high voltage pulsed DC operation and the high voltage transformer driven by a ZVS driver to create high voltage AC. Simulations were performed from which it was verified that the supercascode circuit could switch an input DC voltage of 10 kV at 20 kHz. The ZVS driver-transformer combination was shown to be able to generate up to 10 kV peak with a frequency up to 22 kHz depending on the load. Experiments were conducted with the ZVS driver and transformer which was able to match the simulations. However, the transformer turned out to have a coupling coefficient of 87%, which was not enough to be able to generate plasma, as a coupling of around 95% would be required.

Acknowledgements

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Contents

1 Introduction

1.1 Project objective

Ever since humans started cultivating crops, we have been on a mission to grow more food. Farmers have always looked for ways to improve their crops, like adding nutrients to the soil, giving plants the right amount of water, and making sure they get enough sunlight. But as the agricultural industry has grown, so has the hazard that plant diseases pose. This means farmers need more high-tech solutions, like specialised seed treatments and new ways of disease prevention, to keep their crops healthy [1].

Contemporarily, the technology of growing seeds has its own industry. Extremely specialised and all about making seeds that are tough, easy to store, and sprout quickly. But even with all the intricate breeding techniques, there is still the problem of seed diseases. The old ways of cleaning them, like using harsh chemicals or hot water baths, are not always the best. They can be wasteful on energy, bad for the environment, and even harm the seeds themselves. As a result, there's a growing interest in finding new and eco-friendly disinfection methods [1] [2] [3].

One promising option is cold plasma. This is essentially an ionised gas filled with reactive particles that can kill micro-organisms. Cold plasma has several advantages over older methods: it is better for the environment, uses less energy, and can disinfect seeds effectively without harming them [1] [4] [5].

This thesis focuses on constructing a high-voltage (HV) generator, proving either pulsed DC or AC waveforms, for a system that uses cold plasma to disinfect seeds in an eco-friendly way. The core of this system is a special chamber called a fluidized bed reactor. Here seeds get suspended in a swirling air flow and exposed to the cold plasma. This plasma is created using a technique called dielectric barrier discharge (DBD) which involves creating plasma between electrodes on circuit boards as a result of a large applied potential difference. We want to make sure the system can be scaled up for large-scale use in the seed industry, that it does not waste too much energy and remains relatively affordable [1] [6].

This project is done with support from our sponsor: Bejo Zaden B.V., an industry leader in collecting, disinfecting and distributing seeds.

1.2 State-Of-The-Art Analysis

The seed industry contemporarily largely relies on hot water baths as the primary method for seed disinfection. This method is simple yet effective in removing pathogens from seeds and is performed by submersing seeds in 50 to 60°C water for a typical span of 10 to 30 minutes [7]. Through the hot water baths pathogenic protein structure denatures resulting in compromised cellular structure, effective in eradicating hard to kill fungal pathogens such as Verticillium dahliae and Cladosporium variabile [8]. As such, the industry widely uses hot water baths to disinfect a variety of fruit and vegetables. Hot-water baths do not use harmful chemicals and therefore are not harmful to the environment, it furthermore does not rely on expensive or hard to maintain technologies [2].

Seed disinfection remains a critical aspect of modern agriculture. Conventional methods, like chemical treatments and hot water baths, have limitations. These can negatively impact the environment, consume excessive energy, and potentially damage the seeds themselves. Hence, there is growing interest in identifying alternative eco-friendly disinfection approaches [2].

Several emerging technologies are starting to take shape in the industry, one of which is Ultraviolet (UV) treatment of seeds. Particularly UV-c (200 - 280 nm) is a promising germicide. Electromagnetic (EM) radiation of this frequency is ionising and penetrates deep into the cells of microorganism, causing damage to the pathogens DNA structure, leading to cell death and/or halted reproduction. UV-c is effective for surface sterilization of seeds, grains, and other agricultural products. Being chemical free, means it leaves no residue, isn't harmful to the environment, has minimal impact on seed vitality and since it makes use of energy efficient diodes doesn't adversely contribute to global carbon emissions [9]. However UV-c is a surface level treatment of seeds, the EM waves can't penetrate to lower layers on the surface of the seeds and is thus ineffective against pathogens more deeply embedded within the seeds. Furthermore UV-c treatment is difficult to scale, requiring large surface areas for effective treatments [9].

Another promising emerging technology, one where this thesis report delves into, is cold plasma treatment of seeds. Cold plasma or non-thermal plasma (NTP) is a form of ionised gas characterised by generation of:

- charged particles such as hydroxide ions (HO^-) and superoxide anions (O_2^-) [10]
- reactive species such as reactive oxygen species such as hydroxyl radicals ($HO^\bullet$) [10]

These reactive species disrupt pathogenic cellular structures, deactivating or destroying the pathogens nested on the seeds, at room temperature with minimal effect on the seed vitality [11].

Cold plasma offers a particularly attractive alternative compared to traditional methods due to its combined advantages in energy efficiency and effectiveness. Hot water treatment requires maintaining high water temperatures (50-60°C) for an extended period, which is energy-intensive and contributes to higher carbon emissions [12]. Similarly, while UV-C treatment is relatively energy-efficient due to the use of LEDs, it faces limitations in terms of scalability and effectiveness against pathogens embedded within seeds. In contrast, cold plasma operates at room temperature, significantly reducing energy consumption and environmental impact. Additionally, its ability to generate reactive species allows it to target both surface and embedded pathogens, overcoming the limitations of both hot water and UV-C treatments.

1.3 Thesis Outline

This thesis presents a proof-of-concept analysis for two HV power supply designs intended for DBD plasma seed disinfection. A Program of Requirements (PoR) outlines customer needs, power supply requirements, and justifies design choices through a trade-off matrix. Subsequent chapters detail the working principles, driving outputs, and key design considerations for each HV power supply implementation. Simulation and testing chapters present and discuss results, validating each design's functionality. Finally, the thesis concludes by summarising key findings, highlighting design strengths and limitations, and exploring future research directions for HV generation applied to DBD plasma seed disinfection technology.

2 Program of Requirements

This Program of Requirements outlines the design specifications for the desired high-voltage power supply for DBD plasma seed disinfection. A well-defined PoR is essential for any design process, guiding our decisions and establishing criteria for selecting the optimal approach.

As this project is commissioned by Bejo Zaden, the target customers for this design are seed producers and large seed manufacturers. Within this section, a set of user stories (US) is defined. These are concise descriptions of what the target users want to achieve with the product. From these user stories, a set of design requirements are established. These are further categorized into mandatory requirements, which an implementation must fulfill, and trade-off requirements used to select between remaining viable implementations. By evaluating all implementations meeting the mandatory requirements, a requirement matrix to identify the most suitable design solution can be constructed.

2.1 User Stories

US-1: As a seed-producer I require a plasma disinfection system that offers superior seed disinfection capabilities compared to existing methods.

US-2: As a seed-producer I require a reliable seed plasma disinfection system with a low rate of failure.

US-3: As a seed-producer I require an affordable plasma disinfection system without significantly trading in effectiveness or efficiency.

US-4: As a seed-producer I require a plasma disinfection system that is safe to operate.

US-5: As a seed-producer I require a plasma disinfection system that offers lower power-consumption compared to existing methods.

US-6: As a seed producer, I require a plasma disinfection system with readily maintainable components to minimise repair costs.

2.2 List of Requirements

2.2.1 Mandatory Requirements (MR)

MR-1: Affordability: The prototype implementation must be affordable and shall not exceed €800. (This prioritizes cost as a key factor)

MR-4: Component Availability: The prototype implementation shall be constructed of easy to obtain, off-the-shelf components. (Focuses on readily available parts for ease of construction)

MR-2: Power Output: The prototype implementation must be capable of providing at least a power of 100 W. (Defines the minimum power requirement)

MR-7: Driving Waveform: The prototype implementation must drive the DBD electrodes with an alternating voltage waveform, either pulsed DC or AC. (Specifies the type of electrical output)

MR-3: Voltage Output: The prototype implementation must be capable of driving 10 kV of potential difference across the DBD electrodes. (Defines the voltage requirement)

MR-5: Reliability and Durability: The prototype implementation shall be robust, surviving for a large number of 30-minute disinfection cycles. (Focuses on the system's longevity)

MR-6: Safe Connections: The prototype implementation shall utilize safe and easy-to-use terminals to connect to a multitude of DBD electrodes. (Addresses safety and connection flexibility)

2.2.2 Trade–off Requirements (TR)

TR-1: Output Voltage Control: The prototype implementation *should* have the capability to control the output voltage within a range of 0 to 10 kV

TR-2: Output Power Flexibility: The prototype implementation *could* offer the capability to adjust the output power beyond the minimum requirement of 100 W.

TR-3: Output Waveform Frequency Adjustment: The prototype implementation *could* have the capability to adjust the frequency of the output waveform.

TR-4: System Efficiency: The prototype implementation *should* achieve a power efficiency from input to output of at-least 80%.

TR-5: Output Waveform Frequency Range: The prototype implementation *should* have a minimum broad bandwidth with a center frequency around 20 kHz.

TR-6: Implementation Complexity: The prototype implementation *should* ideally be designed for simplicity in construction.

TR-7: Plasma Generation Efficiency: The prototype implementation *should* be evaluated on the efficiency of the output power that can be utilized for plasma generation.

TR-8: Affordability of the System: The total cost of the prototype implementation *should* minimise the total cost of components.

TR-9: Reliability of the System: The prototype implementation *should* be designed with a high level of reliability to minimise component failures during operation.

2.3 Trade-off matrix: Implementation selection

From the literature a select four implementations, which satisfy all mandatory requirements, are identified, these are:

- **Zero Voltage Switching (ZVS) circuit**: A Zero Voltage Switching (ZVS) circuit is a driver circuit that uses inductor-capacitor (LC) oscillations to drive the gates of MOSFETs. It generates a sinusoidal AC voltage, with its frequency determined by the values of the connected inductors and capacitors. This AC voltage is then fed into a transformer to produce a high voltage sinusoidal output [13].
- **Series Transistor Switching (STS) circuit**: A STS circuit is a type of (half wave- or full wave) inverter that transforms a high voltage input DC voltage to square wave output (Pulsed DC for a half wave, square wave AC for a full wave) by utilizing MOSFETs in series to spread a high blocking-voltage [14].
- **Supercascode Switching (SCS) circuit**: similar to the STS circuit but instead of utilizing series MOSFETs, the SCS circuit spreads the blocking-voltage over series connected JFETs, whose switching behaviour is determined by a series connected MOSFET [15].
- **Marx Generator**: A Marx Generator circuit is a type of high-voltage pulse generator that uses a series of capacitors charged in parallel and then discharged in series. This configuration allows the circuit to produce short high voltage pulses from a relatively low voltage DC input. The capacitors are charged simultaneously through resistors and then rapidly discharged through spark gaps or solid-state switches, resulting in a high voltage output pulse [16].

These circuits are assessed for each TR, being in accordance with the MoSCoW requirement priority grading [17]:

- **1: Inadequate** performance for this metric, the implementation does not meet the minimum condition for this metric

- **2: Subpar** performance for this metric, the implementation barely meets the minimum condition for this metric
- **3: Acceptable** performance for this metric, the implementation meets a satisfactory condition for this metric, though better implementations exist for this metric
- **4: Exemplary** performance for this metric, the implementation is a good fit for this metric
- **5: Outstanding** performance for this metric, the implementation easily meets all conditions set for this metric
- **N/A:** the performance metric is not suitable to describe this implementation

The switch based SCS and STS circuits only require a variable DC source to meet TR-1. ZVS circuits, requiring a minimum input voltage for oscillation, have a minimum output voltage and cannot fully comply with TR-1. Marx Generators, while offering input voltage regulation, cannot adjust it during operation due to the multi-stage capacitor charging process, limiting TR-1 compliance.

ZVS, STS and SCS implementations can fully comply with TR-2 if the driving source can supply the required power. Marx Generators utilise low duty cycle DC pulses, there is no real continuous power usage making TR-2 unsuitable to describe this implementation.

The operating frequency for the STS and SCS circuits can be adjusted during operation, fully complying with TR-3 and TR-5. The Marx Generator and ZVS circuit, due to the nature of their topology can't offer this freedom and such are ill suited to TR-3 and TR-5.

The efficiency of all implementations is largely dependent on the efficiency of the source driving the generator. STS, SCS, and Marx Generator circuits do not contain components with a direct, significant impact on system efficiency, making them well-suited for TR-4. However, the ZVS circuit exhibits a potential decrease in output efficiency when the transformer is not ideally designed, affecting its suitability for TR-4.

The STS, SCS and Marx Generator designs requires a great plethora of components driving up the implementation cost, making these less suitable for TR-8. Furthermore the STS design demands complex gate-driver synchronisation for proper operation and the SCS has a complex interconnected circuit topology making these less suitable for TR-6 and TR-9. The ZVS circuit on the other hand requires no separate gate-driving mechanisms and is topographically less complex than the other implementations making it a good fit for TR-6 and TR-8 and TR-9.

As noted by Williamson (2006) [18], the characteristics of the applied voltage waveform on DBD electrodes significantly impact plasma generation efficiency. Their study suggests that a higher applied waveform frequency results in a higher average power deposited for plasma generation. Nanosecond pulsed DC discharges, with a waveform similar to Figure 2.1(D), offer a distinct advantage in this regard. This rapid energy delivery, as supported by Williamson (2006) [18], significantly energizes electrons within the plasma, creating a highly non-equilibrium state. Additionally, research suggests that these pulses primarily influence the intensity and width of the generated plasma region. In contrast, sinusoidal wave-forms like those generated by a ZVS topology, as shown in Figure 2.1(A), have a comparatively low portion of the active period that delivers useful power for plasma generation. This characteristic makes the ZVS topology less suited for achieving high plasma generation efficiency (TR-7). On the other hand, wave-forms like those in Figures 2.1(B), (C), and (D) dedicate a larger portion of their active period to a region where power is actively utilized for plasma generation. Combined with the previously mentioned findings on frequency capabilities, this suggests that SCS, STS, and Marx generator circuits might be a good fit for TR-7.

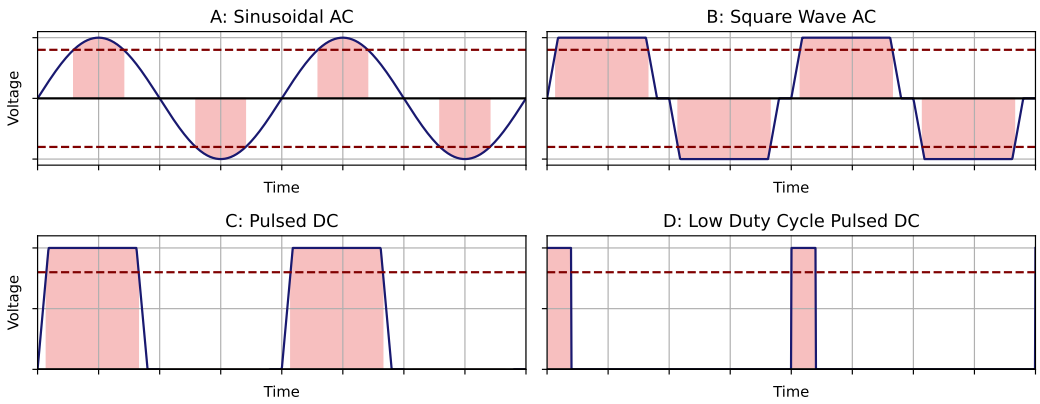


Figure 2.1: Output voltage characteristics for different wave-forms, the dotted horizontal lines indicate the minimum voltage needed for plasma generation and the shaded regions is the part of the period where useful power is available for plasma generation.

In subsection 2.2 a set of requirements and specifications was set up. Each requirement/specification is attributed with a weighting factor (being either '1', '3' or '5'), in accordance with the MoSCoW prioritisation labels [17]. The implementation are assessed for these requirements in the requirements table listed in Table 1. Where each requirement is given a rating with each rating indicating:

- **1: Inadequate** performance for this metric, the implementation does not meet the minimum condition for this metric
- **2: Subpar** performance for this metric, the implementation barely meets the minimum condition for this metric
- **3: Acceptable** performance for this metric, the implementation meets a satisfactory condition for this metric, though better implementations exist for this metric
- **4: Exemplary** performance for this metric, the implementation is a good fit for this metric
- **5: Outstanding** performance for this metric, the implementation easily meets all conditions set for this metric
- **N/A:** the performance metric is not suitable to describe this implementation

Table 1: Trade-off matrix for the various implementations, *: denotes that the score was calculated based on a fill in value of '3'

	TR-1	TR-2	TR-3	TR-4	TR-5	TR-6	TR-7	TR-8	TR-9	Score
Metric weight	5	5	1	3	5	3	5	5	5	
ZVS	3	5	2	3	4	5	2	5	4	141
STS	5	5	5	4	4	1	4	2	3	135
SCS	5	5	5	5	4	2	4	3	2	141
Marx Generator	3	N/A*	2	4	1	4	4	3	4	116

Based on Table 1, the zero voltage switching circuit and the supercascode switching circuit both appear to be the most ideal implementations. However an implementation based on square wave voltage generation is seen as more desirable for plasma generation due to the aforementioned higher plasma generation efficiency, that said the low cost of the ZVS circuit makes it an attractive and interesting option in developing a power-supply for DBD. It was thus decided upon to implement both the SCS and ZVS topologies.

3 Implementation design description

This section will go over the two implementations considered for the high-voltage generation over the DBD electrodes. First this section discusses the general principles of each design, it then looks at the design considerations that need to be considered and finally presents the component choices and prototype specifications.

3.1 Supercascode switching circuit

This subsection details the design considerations for the supercascode circuit, in Appendix B the working principle of the supercascode is explained in detail.

3.1.1 General principle

A standard half-wave inverter utilises two MOSFETs, each in-turn blocking the supply voltage during operation. Though this comes with a budget problem, standard SiC transistors can have at most a blocking voltage of 4.5 kV whilst transistors with a blocking voltage above 4.5 kV aren't readily commercially available [15]. The limitations for high blocking-voltage transistors can be circumvented by spreading the 10 kV drain to source voltage over multiple lower blocking-voltage transistors. The supercascode design achieves this by utilising an $n-$ series cascade of SiC normally-on JFETs (S_{n+1} to S_2) terminated with a NMOS transistor (S_1). This design is illustrated with the circuit schematic shown in Figure 3.1, the schematic here serves to represent the component composition of the switches in Figure B.1b.

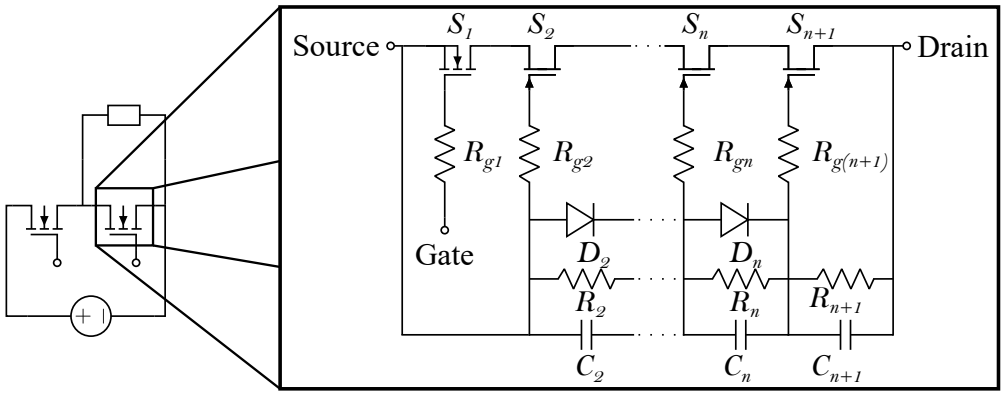


Figure 3.1: Schematic for implementing a high blocking-voltage transistor using a cascade of normally on JFETs terminated with an NMOS transistor

The switching behaviour of the supercascode is determined by the gate to source voltage (V_{GS}) of the terminating NMOS (S_1). The blocking voltage should be spread as evenly as possible over the n JFETs (S_2 to S_{n+1}), the blocking voltage is clamped by the diodes (D_2 to D_n) and the dynamic and static voltage balancing is provided by the capacitors (C_2 to C_{n+1}) and the resistors (R_2 to R_{n+1}) respectively [19].

3.1.2 Design considerations

The amount of stages determines the voltage division over the JFETs. The ideal blocking voltage over each JFET with a supply voltage V_G and number of stages n becomes

$$V_{S_i} = \frac{V_G}{n}$$

High voltage source considerations:
There are various methods of obtaining a high-voltage DC source for the supercascode. From the literature three main types of sources were found:

- A Cockroft Walton Voltage Multiplier can turn a low Voltage AC input to a high voltage DC output, this circuit has a few drawbacks:
  - High cost, roughly €500
  - Large voltage ripples, these add higher frequency elements which contribute to heat generation on the electrodes [20]
  - Voltage level clipping, large number of stages give diminishing returns. High voltage can't be reached with low voltage components [21]
  - No protection circuitry such as over-current protection
- A transformer coupled with a rectifier can achieve a 10 kV output voltage, by regulating the input voltage one can regulate the output voltage. This implementation has the drawback of requiring a rectifier to be used for square wave generation. This rectifier in turn requires a high voltage and high capacitance capacitor, which can be quite expensive. Furthermore this implementation would need to include separate protection circuitry to guarantee longevity.
- A commercially available DC source, these can be inexpensive and can come included with protection circuitry. Commercial available sources also enjoy the benefit of higher efficiency, though some may find themselves having limited output voltage ranges.

JFET considerations:
The selection of the JFETs have to meet several design requirements. It is imperative that the drain to source on resistance R_{DSon} is kept minimal, this is to minimize conduction losses induced by stacking the JFETs in a pseudo-series ladder, to minimise loss in output power. Furthermore the JFETs must turn on and off synchronously, imperative to properly balance the voltage across the transistors. To improve the synchronisation a low gate charge (Q_G) is desired, which also minimises the switching losses of the supercascode circuit. To further ensure minimal power dissipation a transistor must be selected with a low drain to source leakage current (I_{DSS}), the I_{DSS} results in a power dissipation during the off-state of the switch, the efficiency of the switch will improve by selecting a transistor with small leakage current [22].

NMOS considerations:
The NMOS transistor controlling the switching circuit follows similar design requirements as the JFETs. However, since the NMOS controls multiple interconnected semiconductors, each contributing to a parasitic inductance and capacitance, forming so called resonant tanks throughout the supercascode. These resonant tanks can couple energy back to the gate of the NMOS. This phenomena can lead to unwanted turn-ons of the supercascode or even unwanted continuous operation of the supercascode. In the worst case scenario this leads to device failure [23]. Thus it becomes imperative to select an NMOS transistor with a high threshold voltage, in order to prevent these resonant tank effects. Another requirement which is needed for the NMOS is the ability to withstand rapid transitions occurring within the system. A large avalanche voltage is required as a result, such to clamp the voltage across the transistor [22]. Finally the transistor should be capable of switching at 20kHz, as per the design requirements.

Balancing diodes considerations:
Balancing diodes are used to define the maximum static blocking voltage that each JFET must endure, these diodes will face repeated avalanche conditions and must do so without degradation. According to Jimenez et. al. (Arizona, 2024) the preferred choice for these balancing diodes are either avalanche or zener-diodes

due to their ability to clamp a voltage level. This principle is illustrated in Figure 3.2, where in reverse bias at the avalanche voltage for any change in current the voltage drop across an avalanche diode remains relatively stable, the voltage is 'clamped' by the diode. Since the diodes are used to define the maximum blocking voltage, it is imperative to select diodes with an avalanche voltage below that of what the JFETs are rated for, such to reserve meaningful headroom for overshoot of the voltage across the JFETs. According to Jimenez et. al. (Arizona, 2024) a good rule of thumb is to select diodes with an avalanche voltage of: $V_{\text{D-av}} = \frac{2}{3}V_{\text{JFET-rated}}$. As with previous components the diodes should have small leakage currents to keep losses in the supercascode small [22].

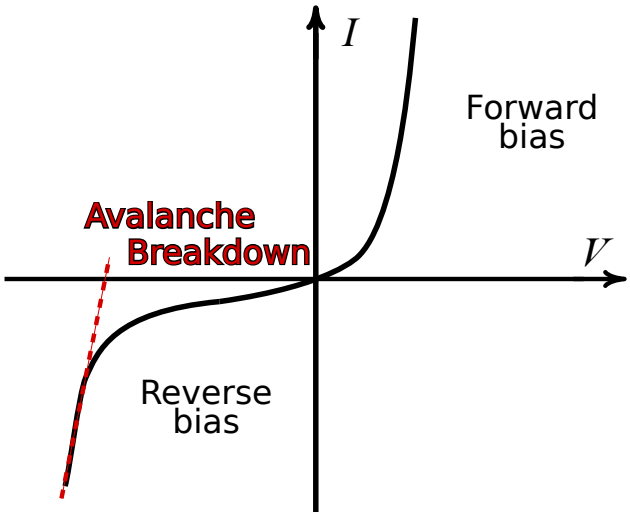


Figure 3.2: *I-V* characteristic of an avalanche diode, the avalanche behaviour is highlighted with a dashed line.

Balancing capacitors considerations:
The dynamic balancing capacitors must ensure that the charge on gates of the JFETs remains stable during switching. Capacitors resist large changes in applied voltage due to the capacitors current dependence on the rate of change of applied voltage, see Equation 14. Keeping an applied voltage level relatively stable. By utilizing a first order approximation given in [24] one can find Equation 1, which gives the values for the balancing capacitor per stage.

$$C_i = (n - (i-1))\frac{Q_G - Q_D}{V_{\text{D-av}}} \tag{1}$$

where n is the number of stages, i is the stage index counting from the NMOS, Q_G is the nominal gate charge of the JFETs, Q_D is the diode charge and $V_{\text{D-av}}$ is the voltage per stage. Finding the diode charge however, requires in-depth analysis, a more simplified approach where the diode charge is omitted is given by [15]. There the capacitance difference per stage is given by Equation 2.

$$\Delta C = (C_{gs} + C_{oss})\frac{V_{p-o}}{V_{\text{D-av}}} \tag{2}$$

$$C_{gs} = C_{iss} - C_{gd} = C_{iss} - C_{rss} \tag{3}$$

V_{p-o} represents the pinch-off voltage of the JFET, C_{oss} is the output capacitance of the JFET, C_{gs} is the JFET gate source capacitance, C_{iss} is the input capacitance of the JFET and C_{gd} represents the gate drain capacitance. Equation 3 indicates how to find the gate source capacitance, given in chapter III of [25]. To maximise the life expectancy of the supercasocode [22] recommends to obtain capacitors with a rated voltage twice that of the stage voltage [22].

Balancing resistors considerations:
The balancing resistors are utilised for static voltage balancing, they evenly distribute the nodal voltages between the gates of each JFET, each balancing resistor must therefore have the same resistance. Selection for these resistors need to fulfill two requirements: low power dissipation, which can be obtained by high resistance values and a voltage rating of at least twice the stage voltage [22].

Gate resistor considerations:
The resistors placed at the gates of the JFETs, indicated by R_{g2} to $R_{g(n+1)}$ serve as current limiting resistors and attenuate unwanted oscillations on the gate of each JFET. The resistors should be capable of dealing with surge currents and should be capable of evenly distributing heat to increase longevity of the system [22]. Furthermore a current limiting resistor R_{g1} should be placed at the gate of the MOSFET. It is imperative that for this gate resistor the following criteria is satisfied to prevented unwanted back-oscillations to the JFET gates:

$$R_{g1} \neq R_{gi}, \quad i \in \{2,\ 3, ..., n+1\}$$

Gate driving considerations:
A further consideration one must account for is the driving of the NMOS transistor. Traditional gate-driving mechanism won't be applicable due to the high offset voltage at the source of the NMOS. To account for this one would need to achieve two objectives. Firstly there is need for isolation between the driving signal and the gate, this can be achieved by means of an opto-coupler. Secondly there is need for isolation between the power source and the output of the gate driver, this can be done by means of an isolated DC/DC converter. Figure 3.3 shows one such implementation.

The capacitors C_1 and C_1 decouple noise from the 15 V and -5 V lines to the offset voltage line (denoted as '0V'), the bipolar junction transistor (BJT) B_1 applies 15 V to the node between R_3 and D1 (V_J) when the driving signal through the opto-coupler is high. When the signal is low B_2 starts conducting and drives V_J down to the offset line. R_1 and R_2 limit the currents to B_1 and B_2. R_3 limits the current flowing to the gate of the NMOS and R_4 provides a discharge path from the gate to the source node. R_3 and R_4 create a voltage division to the gate, this is given by Equation 4. Letting $R_4 >> R_3$ minimises this effect. The Zener-diodes D_1 and D_2 clamp the voltage level at the junction with voltage V_J, these should have a reverse bias rating higher than the desired drain to source voltage. The sync input is not utilised and can be coupled to the 'Vin-' input with a capacitor to reduce noise. The opto-coupler is inputted with a signal source, generating the desired gate driving signal.

$$V_{GS} = \frac{R_4}{R_3 + R_4} V_J \tag{4}$$

3.1.3 Component selection

The high-voltage DC power-supply to drive the supercascode switch was selected to be a 300W 8-16 kV power-supply obtained from Maxgeek, it can be seen in Figure 3.4b. The selected variant is in theory capable of driving the rest of the circuitry with 300 W of power. The output voltage characteristic are two DC voltage lines, one voltage line is at 4 to 8 kV with respect to ground, the other at -4 to -8 kV with respect to ground. When both lines are inputted to the cascode the combined voltage drop can be 8 to 16 kV. This source was selected for it's relative low price of €55 and for being equipped with various circuit protection elements such as a short-circuit-, over-current- and flash-over protection system. Making it a viable, safe and low-cost alternative to building our own source. It works on the principle shown in Figure 3.4a. The input signal from the mains is rectified and then fed into an inverter with a higher than mains frequency, this inverter signal is then fed to a flexible transformer with adjustable tabs to determine

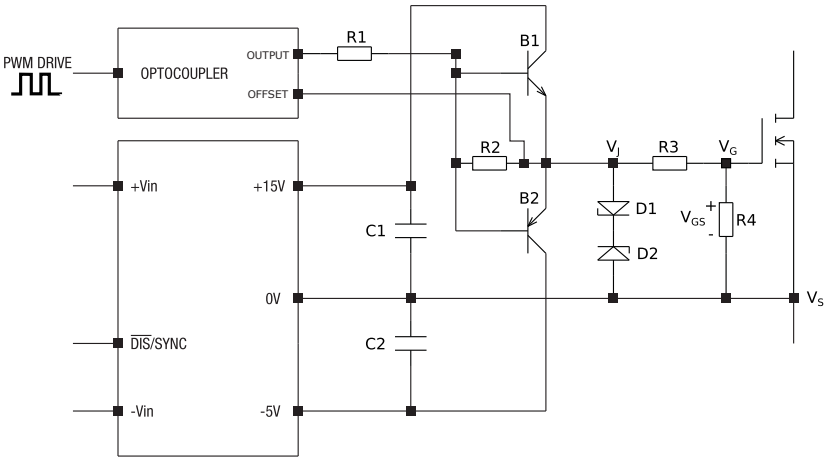


Figure 3.3: Gate driver implementation for NMOS device utilising a DC-DC converter with a driving signal inputted through an opto-coupler [26]

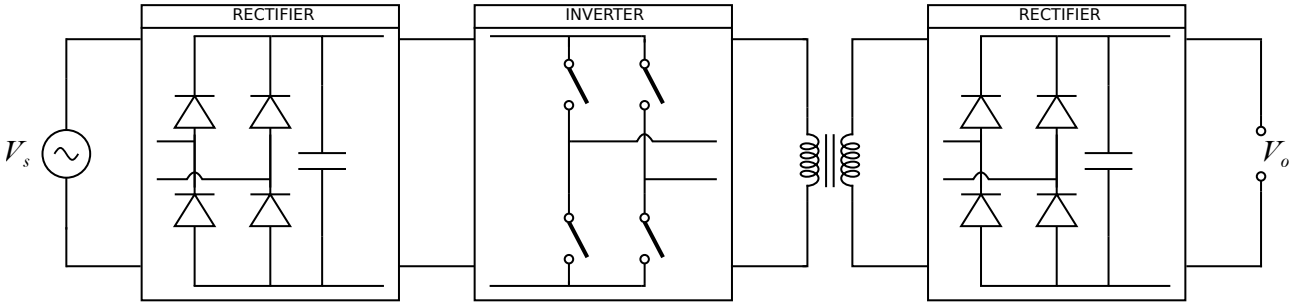
the voltage amplification. The voltage from the transformer is subsequently rectified and presented at the output.

The number of stages was selected to be 11, such that each stage carries less than 1 kV, the ideal stage JFET voltage is then ~ 910 V. This allows for the selection of the VISHAY SF4007 avalanche diode with a repetitive peak reverse (avalanche) voltage of 1 kV. The voltage selection for the JFETs should ideally be 1.5 kV. However, these aren't standard obtainable JFET rated voltage values, as such it was opted to select the 1200 V United SiC UJ3N120070K3S instead. Here voltage headroom was traded in for availability and budgetary reasons. Additionally the ROHM SCT2080KEGC11 NMOS transistor was selected to control the switching behaviour of the circuit. This transistor has a blocking voltage of 1.2 kV, a low drain-to-source resistance of 80 mΩ and a high gate-to-source threshold voltage of 4 V.

Using Equation 3 and [27] a value of $G_{gs} = 890$ pF, further utilising Equation 1 a value of $\Delta C = 128.52$ pF was obtained. Starting from a value of 200 pF Table 2 indicates which capacitor values were allocated for each stage, each capacitor has a tolerance of $\pm 5\%$ and were obtained from VISHAY. It can be noted that most stages utilise 4 capacitors to achieve the desired value, this is due to the rated voltages of the sourced capacitors. The capacitors that were sourced could only be rated for 1 kV, to reach the 2 kV rated voltage level one would need to evenly divide 500 volts over each capacitor. This can be achieved by placing two capacitors in series and placing the 2 sets of series connected capacitors in parallel. The nominal capacitance remains the same. However, the voltage carried by each capacitor is now half of what a single capacitor would carry. A notable issue would be that the tolerances of series and parallel connected components would be worsened, for a prototype this effect is tolerable. However, for a finalised product one would need to source a single capacitor capable of carrying the desired rated voltage with a low tolerance.

For static voltage balancing it was selected to use 75 MΩ resistors with tolerances of $\pm 1\%$, the low tolerance and high resistance values provide a stable and fairly even static voltage division over the cascode. For limiting current to the JFET gates it was selected to use 50 MΩ thick-film anti-surge resistors with tolerance of $\pm 5\%$, these were selected for their ability to withstand short-term current surges with minimal dissipation of energy form the system. For the

The gate driving circuit was designed in accordance with Figure 3.3, here the OPTEK TECHNOLOGY



(a) Blockdiagram for the DC voltage source obtained from Maxgeek, V_s is the main-voltage and V_o the output voltage

(b) Image of the Maxgeek power-supply

Figure 3.4: Commercial voltage source utilised to drive the supercascode

OPI1268S 20 kV isolation opto-coupler was utilised due to it's high isolation voltage. The DC-DC converting providing power to the gate driver circuitry is the Murata Solutions MGJ6D052005WMC, having a 15 V and -5 output line capable of fully turning the cascade fully on or off. Furthermore 20 V zenerdiodes were selected to limit the maximum gate-to-source voltage to 20 V. In Figure 3.3 R_1 and R_3 were selected to be high wattage carbon resistors of 10 Ω, R_2 was selected to be 150 Ωand R_4 100 kΩto guarantee that virtually the full V_J is over the gate-to-source. Finally 22 nF decoupling capacitors were used in accordance with [26].

3.1.4 Prototype construction

The prototype was built on multiple 1.6 mm thick circuit boards. Screw terminals were installed for easy electrical connections between sub-circuits. To ensure rigidity and high voltage isolation, the boards were coated with an epoxy layer. Appendix D images of the prototype are provided.

3.2 ZVS driver with a transformer

The other implementation that was decided upon is the Zero Voltage Switching (ZVS) driver for a high voltage transformer. Such drivers are often used for induction heating coils [28] and high voltage flyback transformers to create plasma [29]. By switching MOSFETs when the drain to source voltage is zero, no voltage occurs at the transistor. This leads to little to no switching losses and EMI can be reduced [30].

Table 2: Realised capacitor values for the supercascode

JFET	Required Capacitor Value (pF)	Realized Value (pF)	Achieved With (pF)
S_{12}	200	200	4x 200
S_{11}	330	330	4x 330
S_{10}	460	470	4x 470
S_9	600	600	1x 1000 in series with 1x 1500
S_8	730	750	2x 1500 in series
S_7	870	860	4x 390 in parallel with 4x 470
S_6	990	1000	4x 1000
S_5	1130	1120	4x 1000 in parallel with 4x 120
S_4	1250	1250	4x 1000 in parallel with 4x 250
S_3	1380	1380	4x 560 in parallel with 4x 820
S_2	1510	1500	4x 1500

3.2.1 ZVS driver

One popular ZVS driver implementation is the Mazzilli driver [30]. This driver is popular for its simplicity and robustness. As can be seen in Figure 3.5, this driver consists of 2 N-channel MOSFETS, which turn on in an alternating fashion because of the oscillating voltage brought on by the resonance between capacitor C1 and the transformer. Inductor L1 functions as a choke. It blocks high frequency AC voltage at the transformer from interfering with the DC rail. Without it, there would be a short circuit when the AC crosses zero volts.

It is possible to build such a ZVS driver from separate components. However, these kinds of ZVS driver are popular circuits so they can be ordered pre-assembled for less cost than the individual components. That is why it was decided to order a ZVS driver instead of building it. The specific driver can be seen in Figure 3.6a. This driver differs slightly from the Mazzilli driver, as it contains 2 choke inductors which means that the transformer primary coil does not need a centre tap.

When the circuit starts oscillating, the output peak voltage will rise to π times the input voltage,

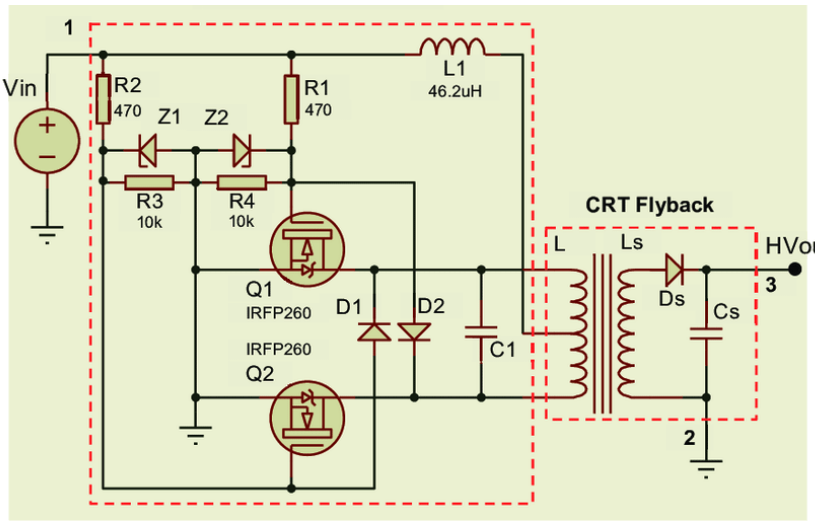
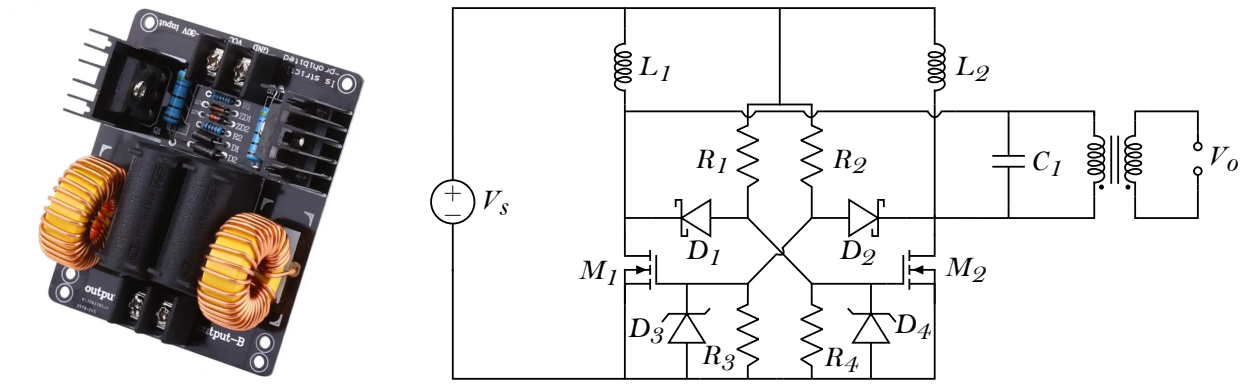


Figure 3.5: Mazzilli ZVS driver with flyback converter [30]



(a) The ZVS driver circuit.

(b) Circuit diagram of the ZVS driver driving a transformer.

Figure 3.6: The modified Mazilli ZVS driver.

3.2.2 High voltage transformer

In order to create the high voltage AC, a transformer is needed. A transformer uses coupled inductors to transfer power using magnetic fields. A simplified model of a transformer can be seen in Figure 3.7. There are a handful of properties that need to be taken into account when designing the transformer:

1. Turn ratio
2. Core material
3. Self inductance of the coils
4. Coupling coefficient

The turn ratio ultimately governs the voltage step up ratio. And considering that the output peak voltage of the ZVS driver is πV_{in}[1], a calculation can be made to determine this turn ratio. The relation between

[1]This value can be found mathematically as it comes from the fact that the resonance creates a sinusoidal voltage. The

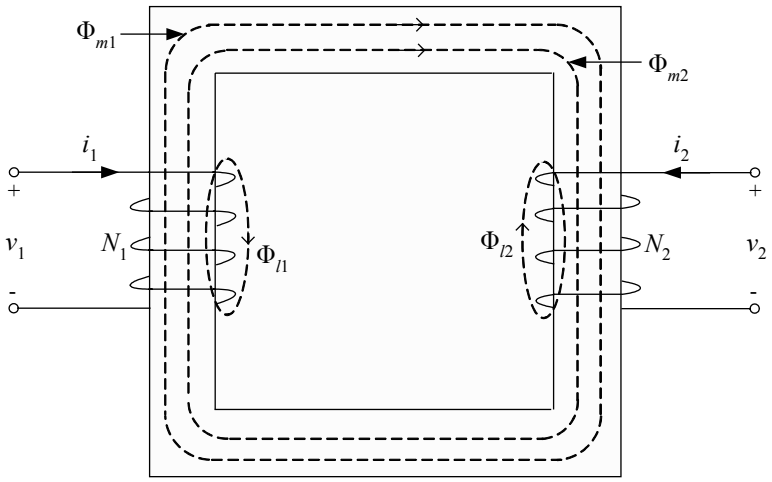


Figure 3.7: A simplified view of the magnetic circuit of a transformer. [31]

voltages and winding turns is

$$\frac{N2}{N1} = \frac{V_2}{V_1} \tag{5}$$

where N is the number of turns and V is the voltage. 1 and 2 denote the primary and secondary side respectively.

The ZVS driver is able to output a peak voltage of roughly 40 to 80 V when varying the voltage between 12 and 14 V. If a peak output voltage of 10 kV is to be achieved, it is possible to calculate the required turn ratio using Equation 5:

$$\frac{N2}{N1} = \frac{V_2}{V_1} = \frac{10000}{80} = 125$$

This means that the secondary winding needs 125 times as many turns as the primary.

Next, a decision needs to be made for the material of the core. Since a high coupling is desired, an air core transformer is not suitable. Considering the frequency that will be required is relatively high, it was decided to use a ferrite core. This material has a high resistivity, which limits losses in the core due to eddy currents. Cores of this material are also affordable and commonly available, which also influenced the decision.

There is a minimum number of turns a transformer winding can have for a given voltage as the mate-

Table 3: The relevant parameters for the ferrite core. [32] [33]

Symbol	Parameter	Value
A	Effective Area	171.0 mm^2
μ_r	Relative Permeability	2500
B_{max}	Saturation Flux Density	470 mT

rial of the core has a maximum magnetic flux density it can support before saturating. This constraint is

derivation is outside of the scope of this project however.

given by the universal EMF equation for sinusoidal voltages [31]:

$$V_{rms} = 4.44 f N A B_{max} \tag{6}$$

where V_{rms} is the effective voltage over a winding, f is the frequency of this sinusoidal voltage, A is the effective area of the core and B_{max} is the maximum magnetic flux density of the core material. This equation can be rewritten to obtain the minimal number of turns:

$$N = \frac{V_{rms}}{4.44 f A B_{max}} \tag{7}$$

Using the data in Table 3, and taking into account that the RMS voltage is the peak voltage over $\sqrt{2}$, the minimum number of turns for the primary can be calculated:

$$N = \frac{80}{\sqrt{2} \cdot 4.44 \cdot 20000 \cdot 171 \cdot 10^{-6} \cdot 0.470} \approx 8$$

At least 8 turns would be required as to not saturate the core. As variance in either the frequency or the saturation flux density could lead to a higher number, it was decided to take into account a margin of 3 turns, meaning the primary winding of the transformer has 11 turns. The secondary will thus have about 125 times as many turns, which is around 1375 turns.

The resonant frequency of the LC circuit is dependent on the capacitor in the ZVS driver and the primary side self inductance. The frequency can be calculated as follows:

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{8}$$

which can be rewritten into

$$L = \left(\frac{1}{2\pi f \sqrt{C}} \right)^2 \tag{9}$$

Filling in the relevant parameters in Equation 9, a target primary inductance can be determined.

$$L_1 = \left(\frac{1}{2\pi \cdot 20000\sqrt{0.6 \cdot 10^{-6}}} \right)^2 = 105.5 \ [\mu H]$$

Now it is possible to determine the self inductance of the windings. The wires will be wound around a cylinder (bobbin), so the windings can be approximated as a solenoid. The inductance of a solenoid can be calculated with the following expression:

$$L = \frac{\mu_0 \mu_r N^2 A}{l} \tag{10}$$

where μ_0 is the permeability of vacuum, μ_r is the relative permeability of the core material, N is the number of turns, A is the area of the core and l is the length of the solenoid. The bobbin is 25 mm long for both the primary and secondary. Now Equation 10 can be used to approximate the self inductance:

$$L_1 = \frac{4\pi \cdot 10^{-7} \cdot 2500 \cdot 11^2 \cdot 171.0 \cdot 10^{-6}}{0.025} = 2.60 \ [mH]$$

$$L_2 = \frac{4\pi \cdot 10^{-7} \cdot 2500 \cdot 1375^2 \cdot 171.0 \cdot 10^{-6}}{0.025} = 40.62 \ [H]$$

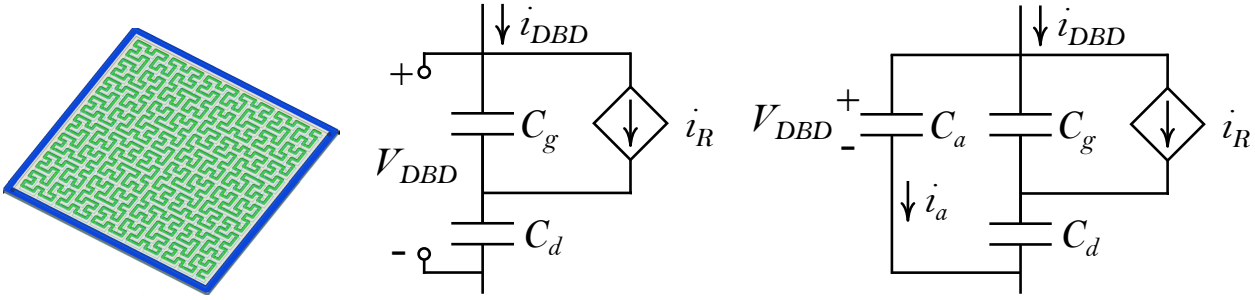
The inductance of the primary is larger than the target of around 100 μH, so an air gap should be introduced in the core to drop the inductance. In the final design, a layer of tape was added to separate the two halves of the core. This yielded an inductance for the primary winding of 92.5 μH, which is close to the target of 100 μH, which will yield a frequency of 21.3 kHz.

4 Simulations and validation

The following section will delve into the simulation results obtained for the supercascode and zero voltage switching circuits and will attempt to validate the chosen implementations. The simulation tool utilised for this purpose is LTSpice.

4.1 DBD load model

Before any simulation can be established a lumped element circuit model of the DBD load should be established. Figure 4.1a shows a model of the electrode in question for which a load model should be established. By referencing [34] one can find a circuit model for the electrode, this is presented in Figure 4.1b.



(a) Render of the dielectric barrier discharge electrode, utilising a 4^{th} order Hilbert fractal to define the traces on a copper coated plate

(b) Lumped element model for the electrode

(c) Lumped element model for the electrode utilised in LTSpice

Figure 4.1: Dielectric barrier discharge electrode and lumped element model

Here C_g is the equivalent capacitance of the discharge gap on the electrode and C_d the equivalent dielectric capacitance of the electrode. The controlled current source i_R represent the discharge current during plasma generation on the electrodes. The values for these elements are given by Equation 11, Equation 12 and Equation 13 [35].

$$C_g = \epsilon_0 \frac{A}{d_g} \tag{11}$$

$$C_d = \epsilon_r \epsilon_0 \frac{A}{d_d} \tag{12}$$

$$i_R(t) = \left(1 + \frac{C_g}{C_d}\right) i_{\text{DBD}}(t) - C_g \frac{dV_{\text{DBD}}(t)}{dt} \tag{13}$$

where d_d is the dielectric barrier thickness, d_g the thickness of the discharge gap, A the discharge area, ϵ_r the relative permittivity of the medium and ϵ_0 the permittivity of free space.

Whilst LTSpice is capable of modeling a current controlled current source, it is unable to model a source dependent on the time derivative of either element currents or voltages. A workaround to this is to apply a capacitor across the terminals of the lumped element model. This is shown in Figure 4.1c. Here the analysis capacitor C_a is chosen to be orders of magnitude smaller than the series connection of C_g and C_d, as such the current through the capacitor $i_a(t)$ is orders of magnitude smaller than the current $i_{\text{DBD}}(t)$.

Therefore the impact that C_a has on the circuit simulation can be minimised, then by utilising the well known current-voltage relation of a capacitor, namely Equation 14 one finds Equation 15.

$$i_c = C\frac{dV_c}{dt} \tag{14}$$

$$\frac{dV_{\text{DBD}}(t)}{dt} = \frac{i_a(t)}{C_a} \tag{15}$$

Now using the circuit shown in Figure 4.1c $i_R(t)$ can be represented in LTSpice though Equation 16 by two parallel current dependent current sources, one proportional to the input current $i_{\text{DBD}}(t)$ and the other proportional to $i_a(t)$.

$$i_R(t) = \left(1 + \frac{C_g}{C_d}\right) i_{\text{DBD}}(t) - \frac{C_g}{C_a} i_a(t) \tag{16}$$

4.2 Supercascode

Two transient analyses for the supercascode were performed in LTSpice as presented in Figure B.1a and Figure 3.1. In the first analysis simulates the generator with a 10 kV DC voltage source, which ramps from 0 to 10 kV in 100 µs to prevent sudden current spikes at $t = 0$. The second analysis supplements the 10 kV voltage source with a random noise source, assuming the source of the cascode to have a tolerance of ±5%, ($V_{\text{n-RMS}}$ = 500 V) simulating sudden potential spikes in the network. The supercascode switch is supplemented with Spice models for the SF4007-TR avalanche diode, SCT2080KE NMOS and UJ3N120070K3S JFET were utilised, which were obtained from: [36], [37] and [27]. Furthermore values were selected for the resistors R2 to R12 which are 75 MΩ with a tolerance of ±1% and the resistors Rg1 to Rg12 were set to 50Ω with tolerance of ±5%. The gate drivers were modeled with a pulse source ranging from -5 V to 20 V with a frequency of 20 kHz and a rise/fall time of 1 µs for analysis 1 and 2. For analysis 3 the gate drivers were simulated with the same voltage levels with a frequency of 2 kHz and a rise/fall time of 10 µs. The square wave generator was connected from its output to a modeled DBD load, as was presented in Figure 4.1c.

Table 4: Values for the co-planar electrode, which were obtained from the DBD electrodes sub-group, to be utilised for the supercascode based switching circuit simulations [38]

Quantity	Symbol	Value
Discharge area	A	41 cm^2
Discharge gap width	d_g	0.7 mm
Dielectric barrier thickness	d_d	0.8 mm
Dielectric relative permittivity	ϵ_r	3.5
Discharge gap capacitance	C_g	51.86 pF
Dielectric capacitance	C_d	158.82 pF

Co-planar electrode values were obtained from the most promising developed electrode, these are presented Table 4. For the transient analysis a value of 1 fF was used to model C_a. The naming convention for the supercascode element follows that presented in Figure 3.1 with an 11 stage supercascode. The result of the transient analyses are presented in the following subsections.

4.2.1 Analysis 1: Static source

In section C the simulation results for the voltages and instantaneous power dissipation for the JFETs: S12, S6 and S2 can be found. In these figures it is found that the largest voltage drop and power dissipation occurs with transistor S2.

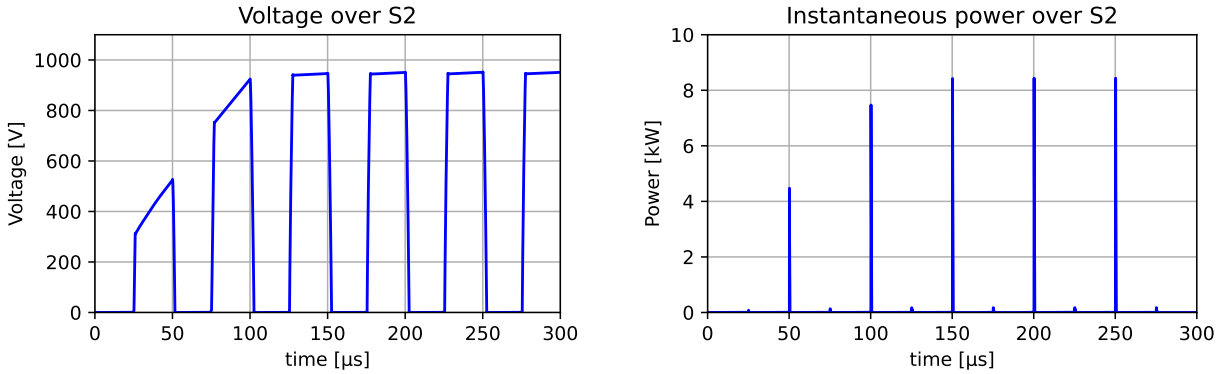
Figure 4.2a illustrates the voltage over the JFET S_2, additionally the voltages over S_6 and S_{12} can be found in Figure C.1. One can observe that the on voltage for JFETs S6 and S2 is about 920 V, for S12 this is slightly below 900 V. This indicates that good voltage balancing can be achieved by this circuit over the JFETs. Ideally Each JFET should carry $\frac{10\text{ kV}}{11} = 909$ V per JFET.

Figure 4.3 shows the drain to source voltages over the high voltage side NMOS, the low voltage side NMOS and the DBD load voltage. The MOSFETs are rated for 1.2 kV, they are well within their blocking voltage specifications with occasional voltage spikes up to 80 V. Due to an immediate drain to source voltage being applied when the cascode switch disconnects the source from the load.

Figure 4.2b shows the instantaneous power dissipation by the JFET S_2, additionally the dissapations by S_6 and S_{12} are shown in Figure C.2, with a load drawing 10 mA at 10 kV and switching at 20 kHz. These JFETs are rated for 254 W. Average power dissipation can be found with Equation 17, where T is the period of the time periodic power signal $p(t)$ and t_0 is some arbitrary starting point. The maximum power over a JFET during switching is about 31 W indicating that for this type of load with a non-varying source they're well within their power dissipation specifications.

$$P_{av} = \frac{1}{T}\int_{t_0}^{t_0+T} p(t)dt \tag{17}$$

In Figure 4.4 the pulse shape is analysed, the input signal is a DC pulse train at a frequency of 20 kHz with a rise and fall time of 1 ns. The pulses at the output are also DC pulses with a rise time of 1.691 µs, a fall time of 1.689 µs and an on time of 24.96 µs. These are close to the rise and fall times of the simulated gate driver source, indicating that the network adds a minimal delay.



(a) Voltage over high-side JFET S_2

(b) Instantaneous power dissipation of high-side JFET S_2

Figure 4.2: Analysis 1 simulation results for the voltages and power dissipation in stage 2

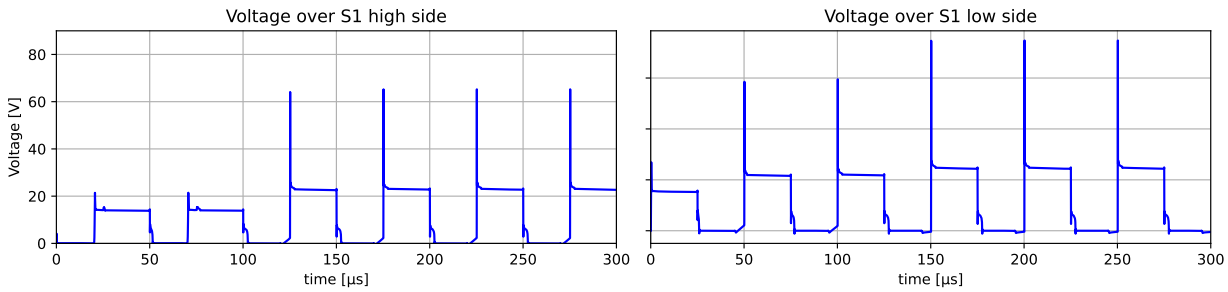


Figure 4.3: Simulated voltage values over the two NMOS transistors with a 10 kV DC source

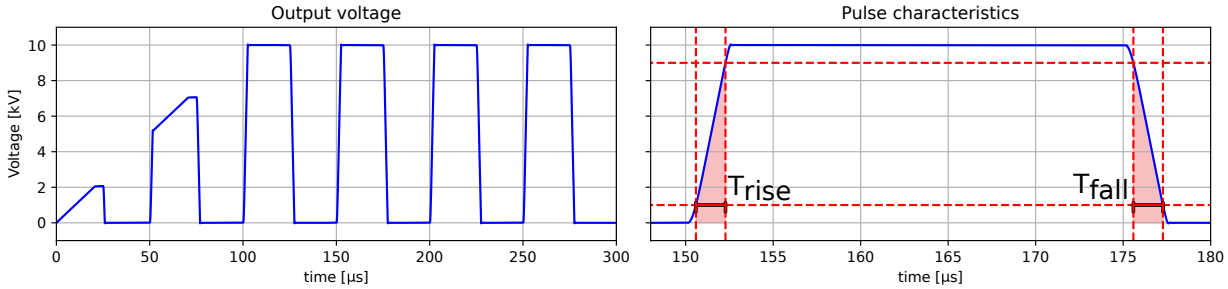


Figure 4.4: Simulated output voltage applied to the DBD load and an analysis of the pulse shape of this output voltage

4.2.2 Analysis 2: Noisy source

For analysis 2 a white noise source (element 'bv' in LTSpice) is supplement to the DC source already present, this noisy source has an RMS voltage value of 500 V (5% of the source voltage), this is meant to model a particularly bad fluctuating source, to verify whether under these conditions the circuit is still functional.

Figure Figure C.3 shows the voltage over each of the analysed JFETs and Figure 4.5a specifically for S_2, the noisy source does appear to push the voltage level of S_2 to the 1 kV, however there's still a good separation ($\sim$ 200 V) between its rated voltage and the voltage applied over the transistor.

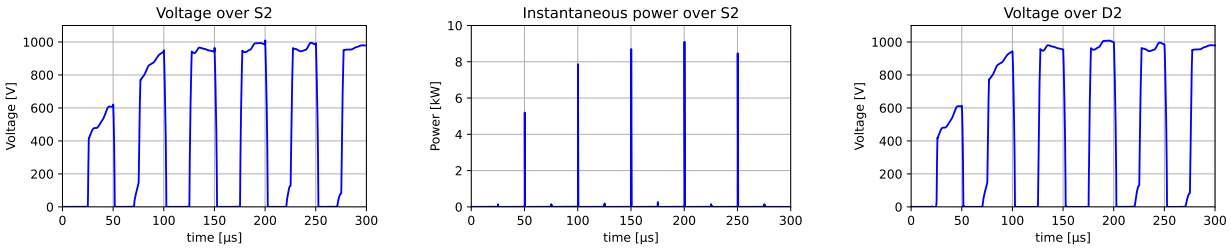
Figure C.4 and Figure 4.5b illustrate the power induced as a result of this fluctuating noise source, it can be observed that the instantaneous power dissipation of the JFETs is practically unchanged. From analysis with LTSpice it was found that the maximum average power dissipation is 52 W, well within the 254 W power rating.

Likewise no significant change can be observed of the voltage over the NMOS transistors, only noting that due to the dynamic effects the voltage over the transistors is slightly higher but well below the specifications.

The dynamic voltage over the balancing diodes D_{11}, D_6 and D_2 and conversely also the corresponding balancing resistors and capacitors can be seen in Figure C.5 and for D_2 specifically in Figure 4.5c. It can be observed that the voltage profile is very similar to that of the JFETs, illustrating the effect of the balancing elements to the voltage over the JFETs.

Finally in Figure 4.7 the output voltage characteristic is observed, it can be seen that the dynamic input results in a dynamic output, with oscillations visible during the on-time. The pulse shape remains

relatively unchanged with the same rise and fall times.



(a) Voltage over high-side JFET S_2 **(b)** Instantaneous power dissipation of high-side JFET S_2 **(c)** Voltage over high-side avalanche diode D_2

Figure 4.5: Analysis 2 simulation results for the voltages and power dissipation in stage 2

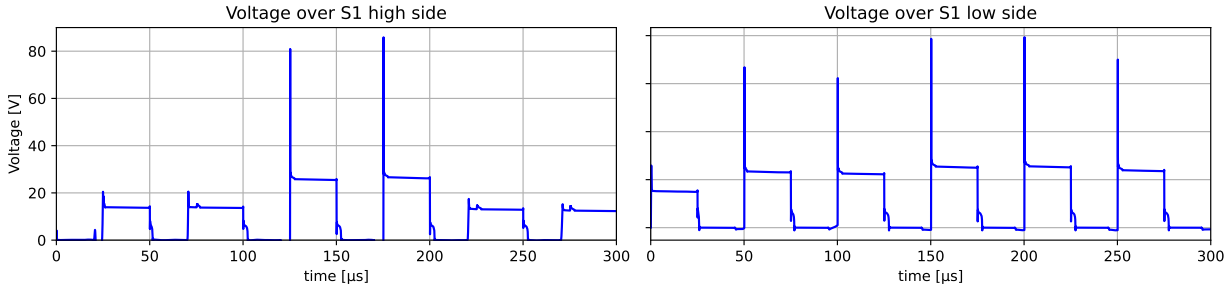


Figure 4.6: Simulated voltage values over the two NMOS transistors with a 10 kV DC source

Analysis 1 confirms that during the static condition with a 10 kV source the supercascode design is within specifications and generates the desired square wave potential difference over the DBD load. Analysis 2 confirms that with a relatively poor source device, the supercascode circuit still manages to remain within specifications.

4.3 ZVS driver and transformer

To simulate the effects of the ZVS driver, the circuit was entered in LTspice. The coupling coefficient that was chosen for this was 95%, as a perfect coupling of 100% is impossible to achieve. The simulation command contained the "startup" directive, which steps the 24 V DC source which is required for the driver to start oscillating. Spice models for the exact semiconductor components used were not available, so they were replaced with models with similar ratings. Transient behaviour was disregarded as interest lies in the steady state behaviour and these transients were not able to be validated using measurements.

4.3.1 Analysis 1: No load

The first simulation was made to determine the output voltage of the system when no load is connected. This should verify if the target output voltage and frequency are as expected. As can be seen in Figure 4.8, the output voltage is around 9.2 kV when the input voltage of the transformer is at 75 V, which is a voltage ratio of 123. This lines up with the calculations for a transformer with a 1:125 turn ratio. It is possible to determine the frequency of the sinusoidal wave from the plots by measuring the time between a number of periods. This yields a frequency of about 22 kHz, which is similar to the expected frequency of 21.3 kHz.

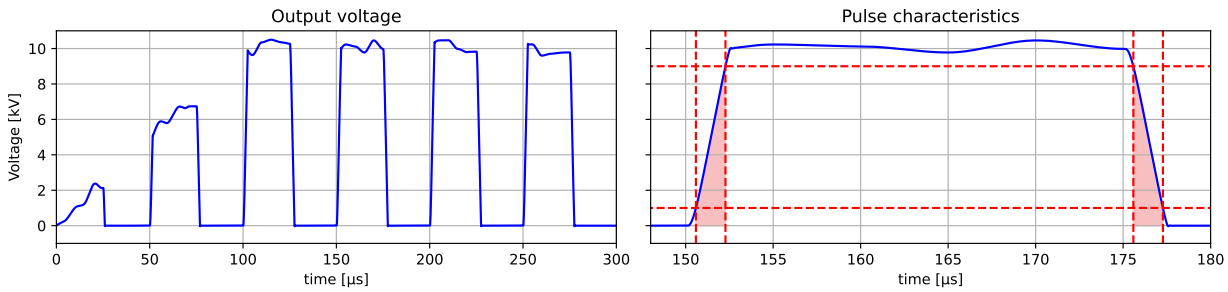


Figure 4.7: Simulated output voltage applied to the DBD load and an analysis of the pulse shape of this output voltage

When looking at the current in the primary coil, it can be noted that it is relatively high at 6 A peak. In order to minimise copper losses, the wire that is used for the primary winding needs to be thick enough to handle this current. It can also be noted that the current flowing through the primary winding is significantly higher than the current in the source. Resonance causes the current to rise and it does not require much energy to sustain this resonance. Most of the power that is used can be attributed to the several resistors and diodes in the circuit and the on-resistance of the MOSFETS.

From these simulation results it can be deduced that this high voltage generator works as expected when no load is connected, with a relatively low power draw from the source.

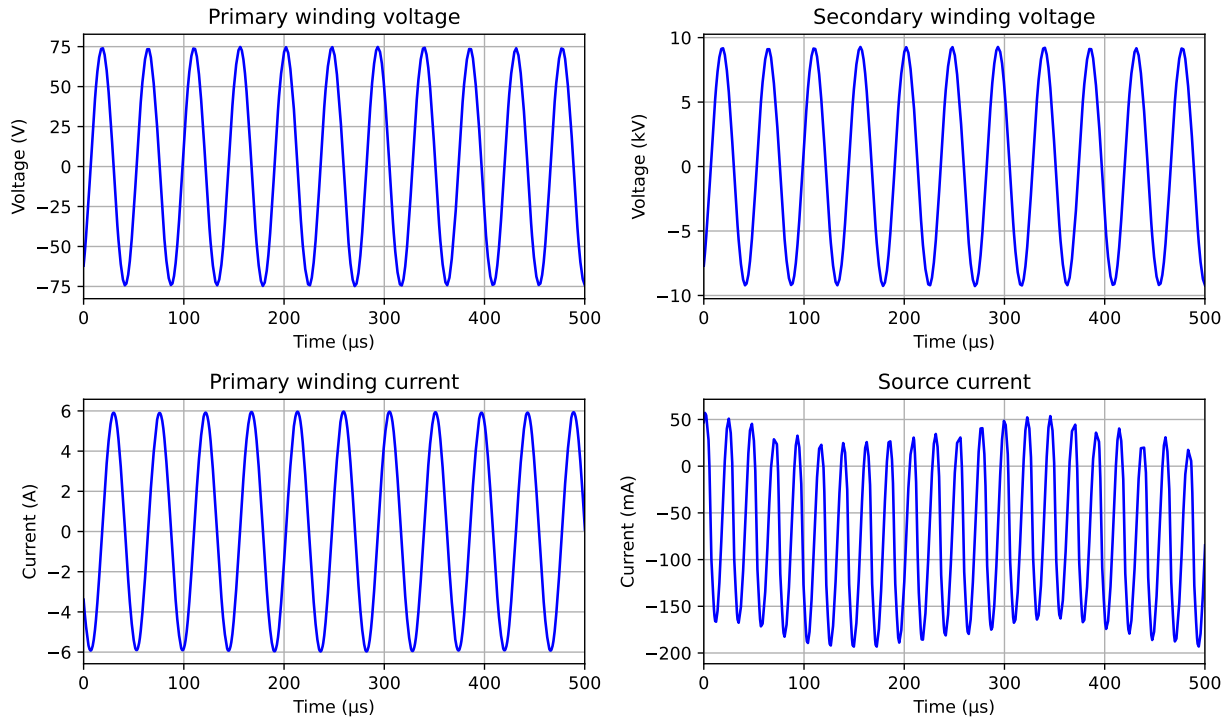


Figure 4.8: Simulation results for the ZVS driver and transformer with no load.

4.3.2 Analysis 2: DBD load

For the second simulation analysis, the DBD load model from subsection 4.1 was connected to the output of the transformer. This will show the behaviour of the system under load and if plasma can be generated. Figure 4.9. The maximum voltage that is generated now is 10 kV at 9 kHz. The change in frequency is due to the capacitance of the DBD load. This capacitance can be referred to the primary side, which will add to the capacitance in the ZVS driver. Considering the requirement of the frequency having to be higher than 5 kHz, this is not a showstopper. However, this phenomenon could limit the amount of DBD elements that can be connected, while still generating plasma.

Looking at the simulation results with 3 loads connected in Figure 4.10, it can be seen that the distortion in the current through the primary is increased compared to having one load. The peak current has also been reduced compared to previous simulations. The frequency has also dropped to 5.4 kHz. The simulations indicate effects of saturation, which could be true as more power is required for the generation of plasma. From this it can be concluded that three electrodes can be connected to a ZVS-transformer combination for plasma generation. However, it should be addressed that these simulations do not take into account different parasitic effects, core losses among others, so the real performance can deviate from the simulations.

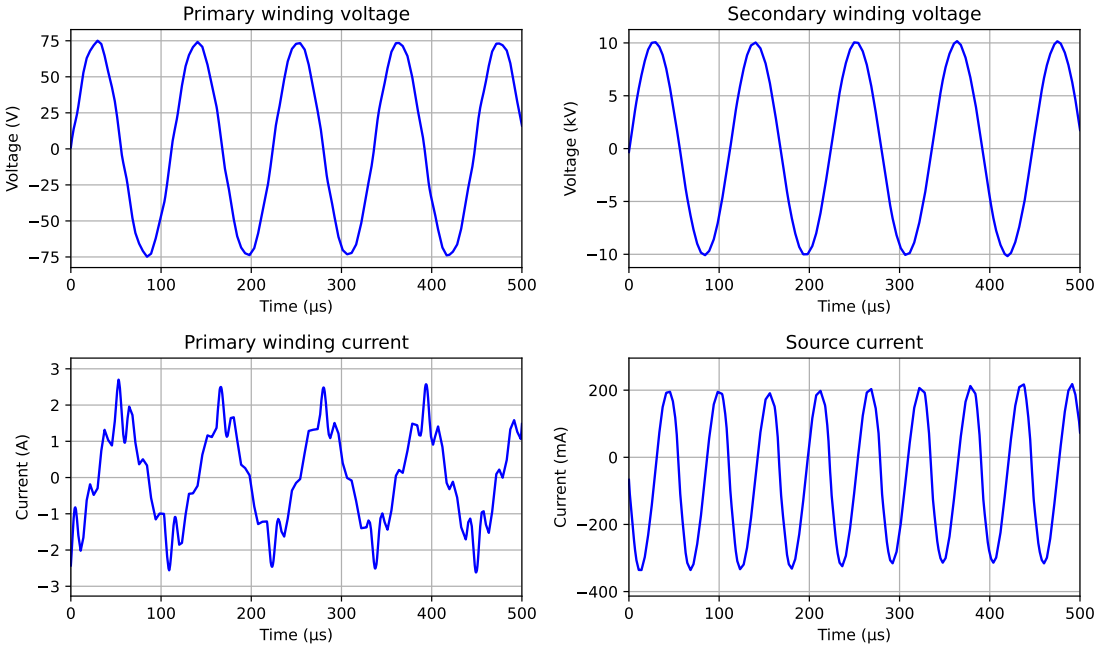


Figure 4.9: Simulation results for the ZVS driver and transformer with 1 DBD load.

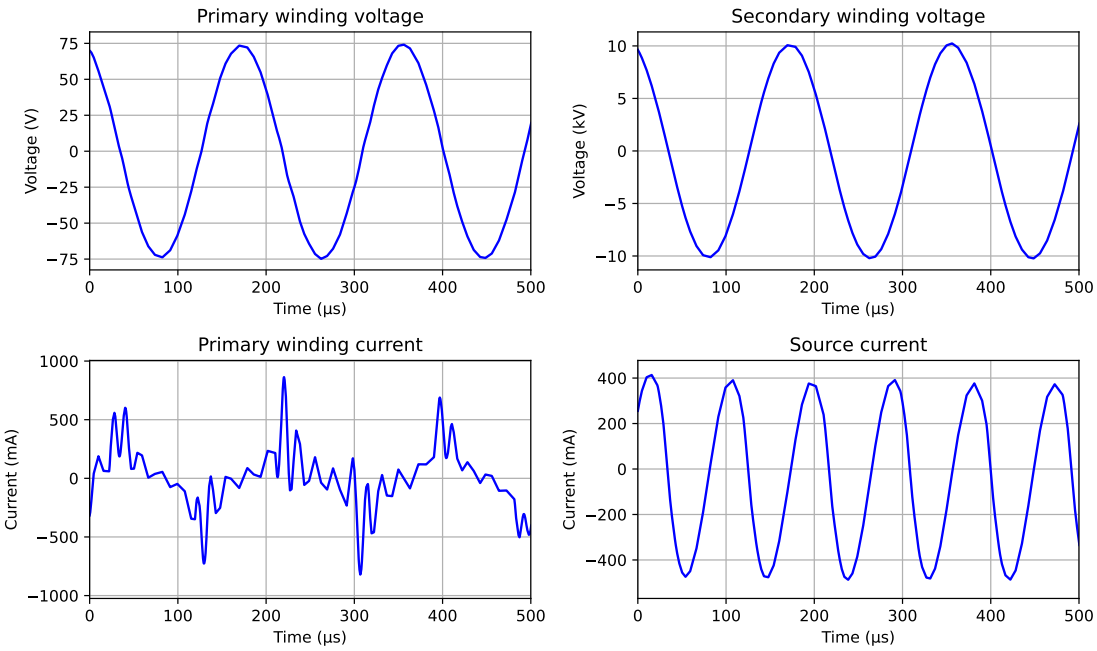


Figure 4.10: Simulation results for the ZVS driver and transformer with 3 DBD loads.

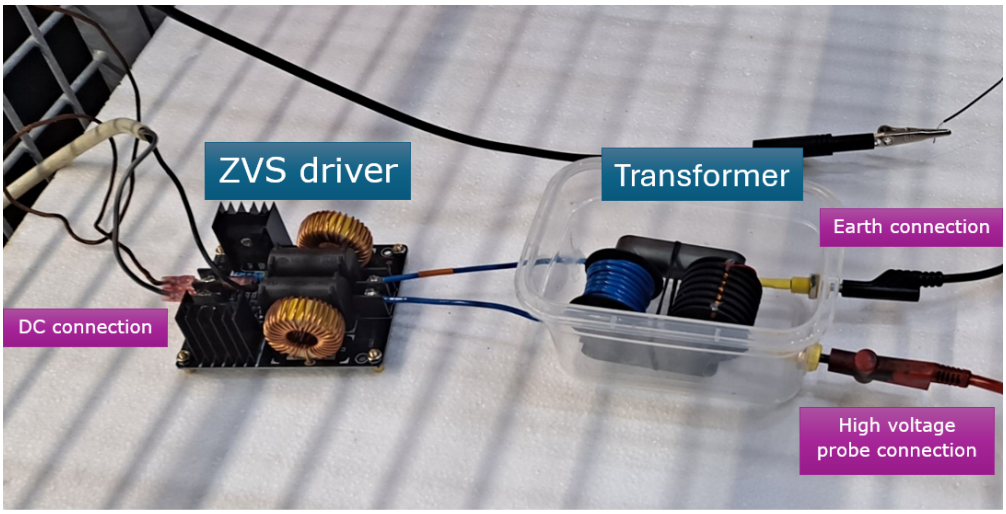


Figure 5.1: The testing setup for the ZVS driver and transformer

5 Testing and results

The following chapter will discuss the experiments and test that were conducted to verify the design requirements. Due to difficulties sourcing the components and shipping delays, it was not possible to test the supercascode circuit. For safety, these tests had to be done in the High Voltage Lab with the components safely residing in a closed cage for safety.

5.1 ZVS and transformer

5.1.1 No load test

To test the ZVS driver with high turn ratio transformer it was decided to make measurements of the output voltage when varying the input voltage between 4.0 and 12.0 V. It was decided not to go higher without a load in case it would destroy the driver due to large currents. The testing setup can be seen in Figure 5.1. The high voltage probe was connected to an oscilloscope to capture the waveform of the output which can be seen in Figure 5.2. The output is close to a sinusoid. The frequency of the wave is measured to be 19.5 kHz, which is close to the theoretical value of 21.3 kHz and the target of 20 kHz. The waveform did not change when the input voltage was varied, apart from the change in amplitude.

The input and output voltage levels were noted down in Table 5 and plotted in Figure 5.3. From the data it can be determined that the effective voltage step up ratio is 100, which is lower than the theoretical 125.

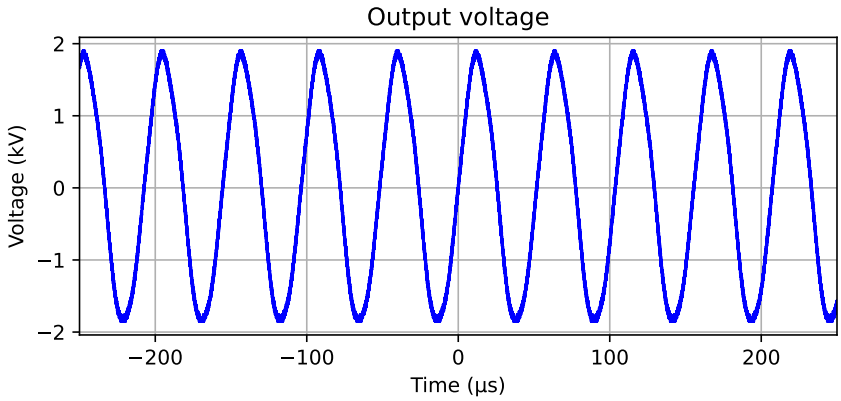


Figure 5.2: Oscilloscope output of the transformer at a DC input voltage of 6V.

Table 5: Measurement results of the no load experiment

DC input voltage [V]	4.0	5.0	6.0	7.0	8.0	9.0	10.0	11.0	12.0
AC output peak voltage [V]	1.3	1.6	1.9	2.2	2.5	2.9	3.1	3.5	3.7

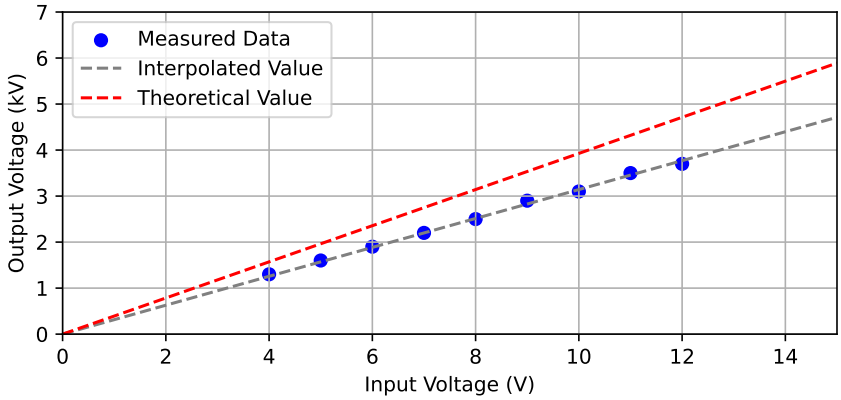


Figure 5.3: Measured input-output behaviour compared to simulation.

5.1.2 DBD load test

For the next experiment, the same setup was used as in the no load experiment, but with an added DBD electrode. When the system was enabled, it was quickly apparent that the output voltage was significantly lower than expected. The relation between input and output voltage was still linear, but now it was with a step up ratio of 16. This meant that the output voltage was too low to be able to generate any plasma. Furthermore, the frequency of the rose to over 50 kHz, which could be outside the bandwidth of this transformer.

The reason this happened is because the coupling coefficient of the transformer is not high enough. Using an LRC (Inductor, Resistor and Capacitor) meter it was possible to determine a coupling coefficient of 87%. Initially it was believed that this value would be enough to generate high voltage under a small load, but it appeared that the effects of leakage inductance were underestimated.

6 Conclusion

Two designs for high voltage generators used for eco-friendly disinfection of seeds using plasma were proposed. The theory and importance behind the idea was explained in detail. Design requirements were set up using the MoSCoW method. Care was given to developing measurable and verifiable requirements. Four different implementations of high voltage generators were considered, and the two most promising concepts were selected to be worked out. These concepts were the supercascode and ZVS driver circuits.

Designs for the two concepts were explained in detail and finalised. These designs were verified using spice simulations which came out positive. Due to sourcing and delivery issues, it was not possible to test the designs on all the requirements. The supercascode was not able to be verified and the ZVS driver circuit was not behaving as desired due to an imperfect high voltage transformer. However, these designs did show promise and could lead to a working product in the future.

7 Discussion and future prospects

7.1 Discussion

As touched on in section 5, it was not possible to test the supercascode circuit due to shipping delays. But even without these delays, it would still not have been able to be tested because the opto-couplers that are rated for 20 kV did not function as expected. This was only noticed late in the project and no alternative could be found in time to do tests on low voltage. If this project were to be done again, it would be recommended to build a similar design using cheap, low voltage components, as this would still make it possible to prove the idea of the supercascode circuit, albeit not for generating plasma.

Faculty regulation forbids the use of high voltage (over 50 V) circuitry in the lab. Tests with high voltage had to be done in the High Voltage Lab under supervision. This severely limited the possibility of rapid iteration of the prototypes as the testing sessions had to be planned out in front. And if there were unexpected results, the day ended there. There is no real solution to this problem, as safety is extremely important.

7.2 Future prospects

In the future, these design could be iterated upon as the literature and simulations show that the concept is feasible. As for the project, there are a handful of elements that could be explored further.

New high voltage transformer: The high voltage transformer that was built utilised 2 bobbins on which the wires were wound. These bobbins were placed on different legs of the transformer core. Also, to reduce the chance of flash-over between the two winding through the core, these bobbins were made to have an inner wall thickness of 2 mm and the inner diameter of the bobbin was made to be 1 mm larger than the outer diameter of the core leg. These distances introduce leakage, which will deteriorate the coupling factor. In the future, a new transformer could be made using a thinner bobbin or possible with the wire of the primary wound directly on the core to improve the coupling factor, which could lead to better power transfer and plasma generation. Another option is to make a transformer with the primary and secondary on the same leg. With this option, extra will have to be taken to avoid flash-over between the wingdings. This could be done by potting the transformer in epoxy resin or silicone.

High voltage DC source using ZVS driver: For the current implementation of the supercascode circuit, an external HVDC supply is required. Instead of using a commercial driver, it is possible to use the ZVS driver with a flyback transformer, which is a transformer with an integrated rectifier on the output in order to create high voltage DC. This implementation could be more economical and versatile than the commercial source which use similar circuitry.

Disinfection capability comparison: An experiment that was originally planned was a comparison between the plasma disinfecting capabilities of AC and pulsed DC. To test this out, one could prepare a batch of seeds infected with a known fungus (yeast). These seeds could then be grown in petri dishes after different treatments. This way, the effect of the different types of plasma generation, intensity and duration could be compared and a definitive implementation can be chosen.

Control system: An idea that was proposed was a control system to control ozone concentration. Another subgroup in our project worked on a sensor system which had sensors for ozone concentration. This data could be sent to a micro-controller, which could then control the input voltage. This idea is promising and seems feasible, as the input voltage for the ZVS driver could be electronically regulated using a DC-DC converter.

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Appendices

A Nomenclature

Below you can find a list of abbreviations and symbols.

Abbreviations

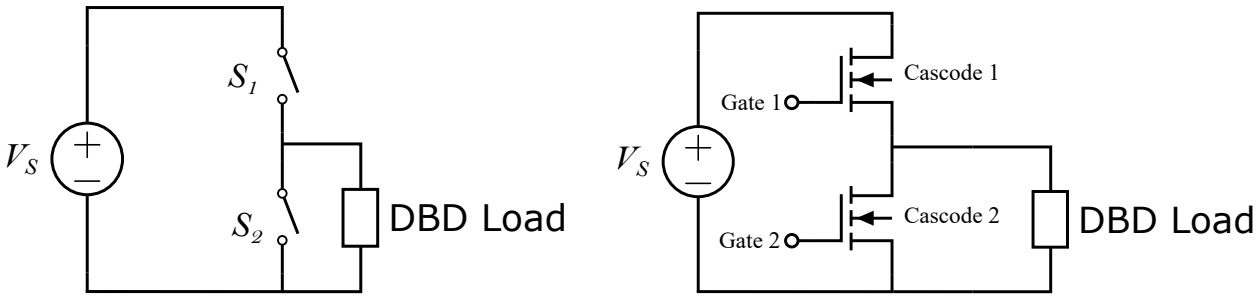
Abbreviation	Definition
DBD	Dielectric Barrier Discharge
NTP	Non-Thermal Plasma
HV	High Voltage
ZVS	Zero Voltage Switching
SCS	Supercascode Switch
SiC	Silicon Carbide, a type of material used in the semiconductor industry
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
NMOS	N-type metal–oxide–semiconductor, MOSFETs where the majority charge carriers are dominated by electrons
PMOS	P-type metal–oxide–semiconductor, MOSFETs where the majority charge carriers are dominated by holes
JFET	Junction Field-Effect Transistor
BJT	Bipolar Junction Transistor
NPN	Negative-positive-negative doped BJT
PNP	Positive-negative-positive doped BJT

Symbols

Quantity	Definition	Unit
V	Voltage DC	[V]
$v(t)$	Voltage AC	[V]
U	Potential	[V]
I	Current DC	[A]
$i(t)$	Current AC	[A]
C	Capacitance	[F]
L	Inductance	[H]
P	Power	[W]
$p(t)$	Instantaneous power	[W]
ϵ_0	Free-space permittivity	[F m^{-1}]
ϵ_r	Relative permittivity	Dimensionless
μ_0	Free-space permeability	[H m^{-1}]
μ_r	Relative permeability	Dimensionless
N	Number of turns	Dimensionless
B	Magnetic flux density	[T]
f	Frequency	[Hz]

B Working principle of the Supercascode Switching Circuit

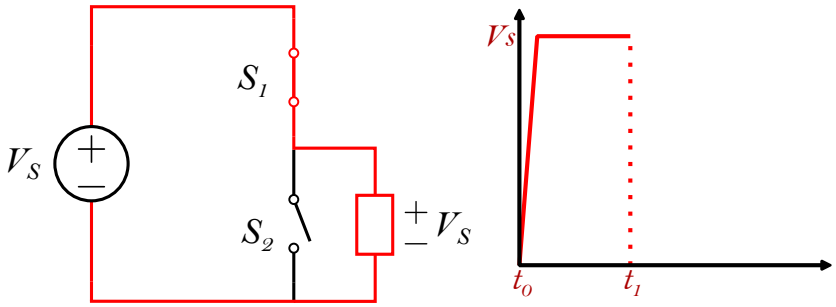
Switches are used to generate a square wave output signal from a DC source. Figure B.1a illustrates the design principle, here a half wave inverter circuit is illustrated. This principle uses two switches (S_1 and S_2) which engage in sequence. At a certain time t_0 S_1 engages and S_2 disengages, the source now applies a potential difference across the load, as can be seen in Figure B.2a. When S_2 is being engaged and S_1 is being disengaged at a certain time t_1, see Figure B.2b, the load loses the applied potential difference.



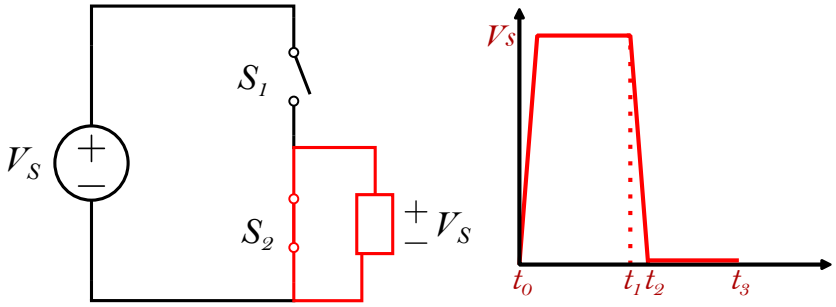
(a) General principle with generic switches

(b) Principle utilising the supercascodes as switches

Figure B.1: Switch schematic illustrating the basic principle of pulsed DC voltage generation utilising a half wave inverter



(a) Engaged S_1 and disengaged S_2 applies the source voltage over the load



(b) Engaged S_2 and disengaged S_1 applies 0 V over the load

C Additional plots

Figures for SCS simualtion

Analysis 1: Static source

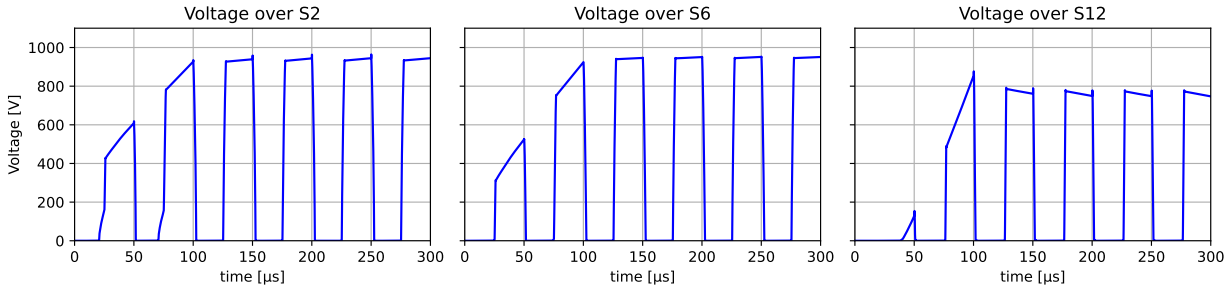


Figure C.1: Simulated voltage values over the JFETs S2, S6 and S12 with a 10 kV DC source, the voltage between 0 and 100 µs is determined by the ramping behaviour of the source

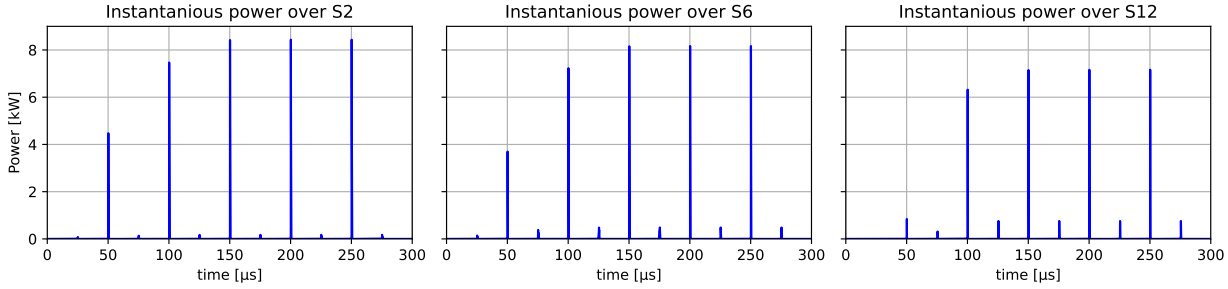


Figure C.2: Simulated power dissipation by the JFETs S2, S6 and S12 with a 10 kV DC source

Analysis 2: Noisy source

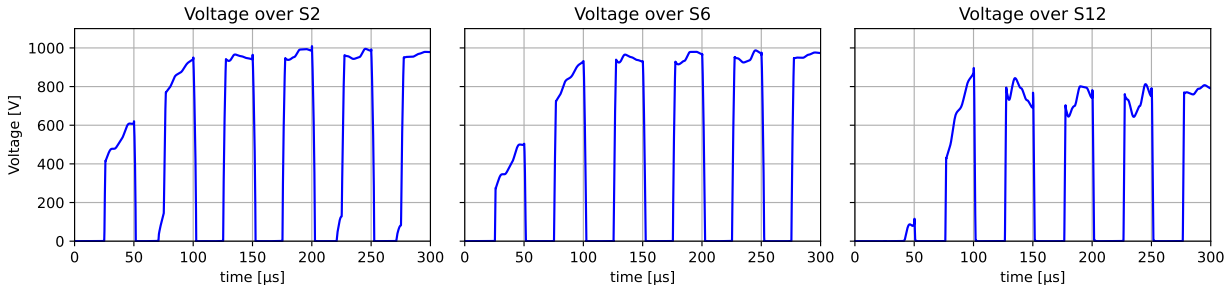


Figure C.3: Simulated voltage values over the JFETs S2, S6 and S12 with a 10 kV DC source, the voltage between 0 and 100 µs is determined by the ramping behaviour of the source

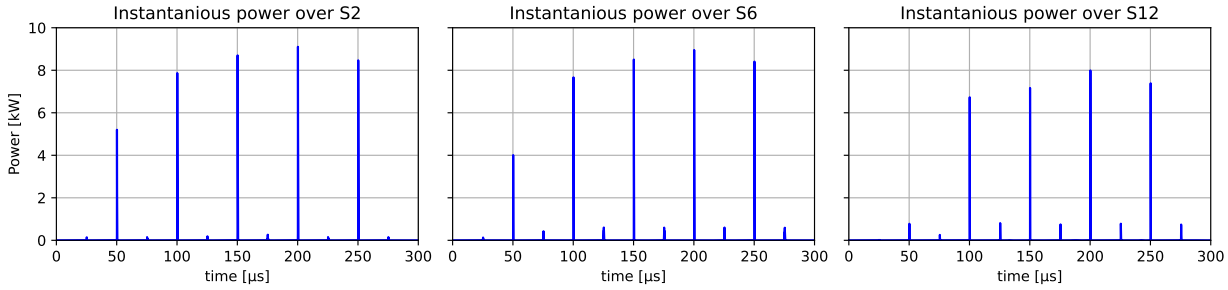


Figure C.4: Simulated power dissipation by the JFETs S2, S6 and S12 with a 10 kV DC source

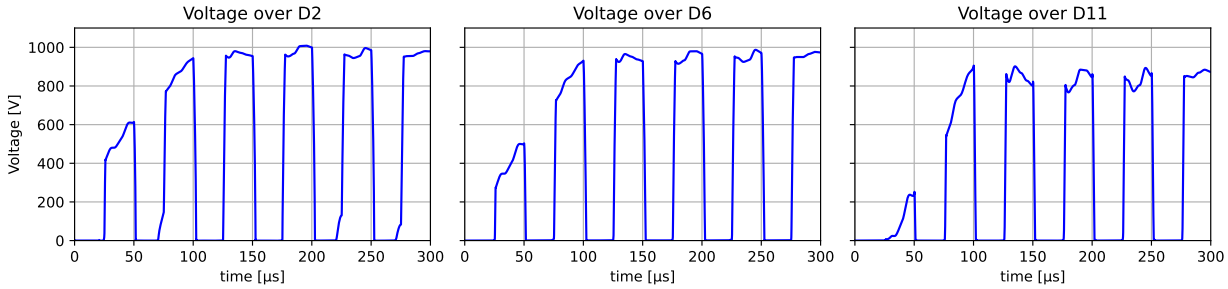


Figure C.5: Simulated output voltage over the balancing diodes D11, D6 and D2, conversely also the voltage over the corresponding balancing capacitors and resistors

D Prototype gallery

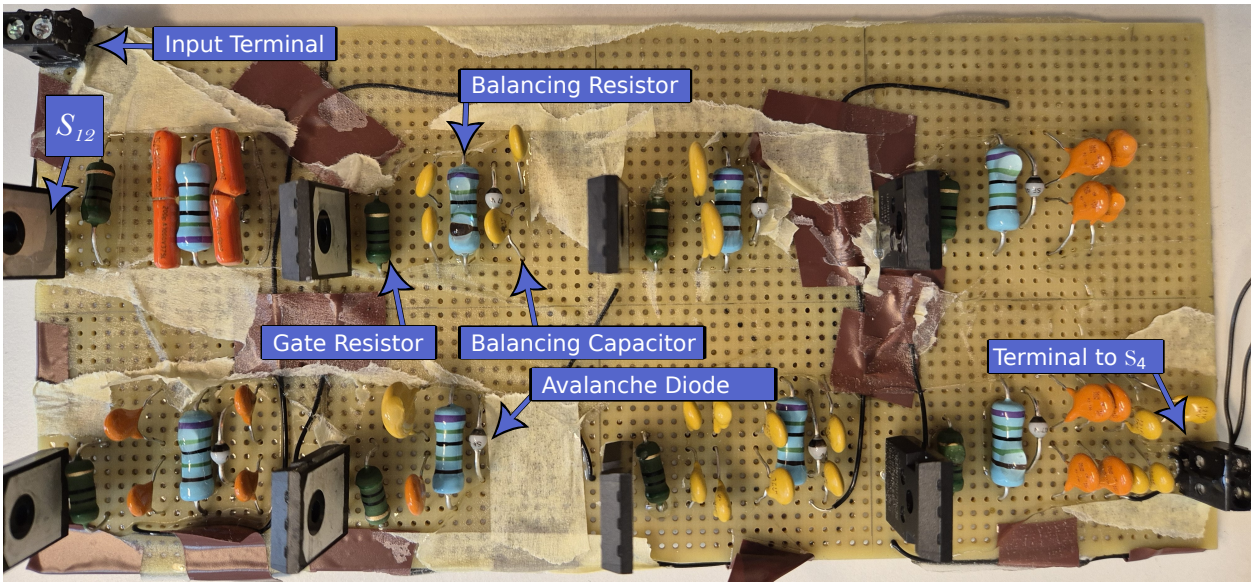


Figure D.1: Image of the top-side of the supercascode prototype, featuring S_{12} to S_5

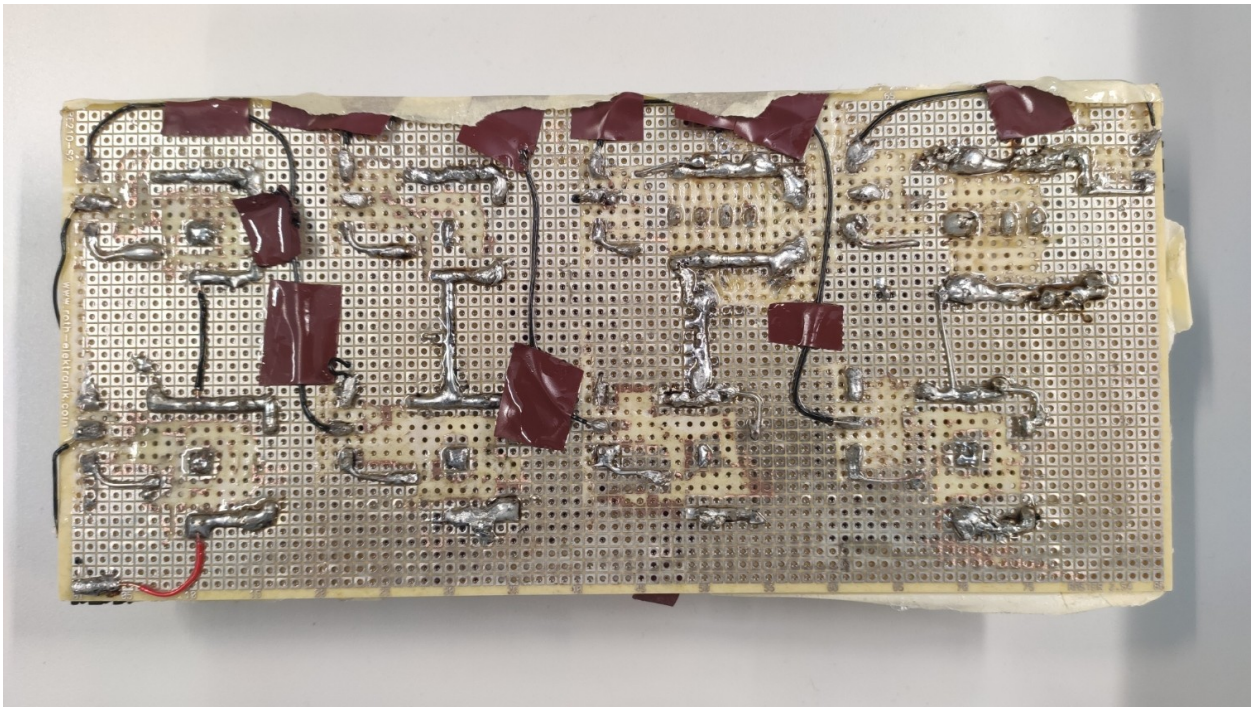


Figure D.2: Image of the epoxy coated bottom-side of the supercascode prototype, featuring S_{12} to S_5

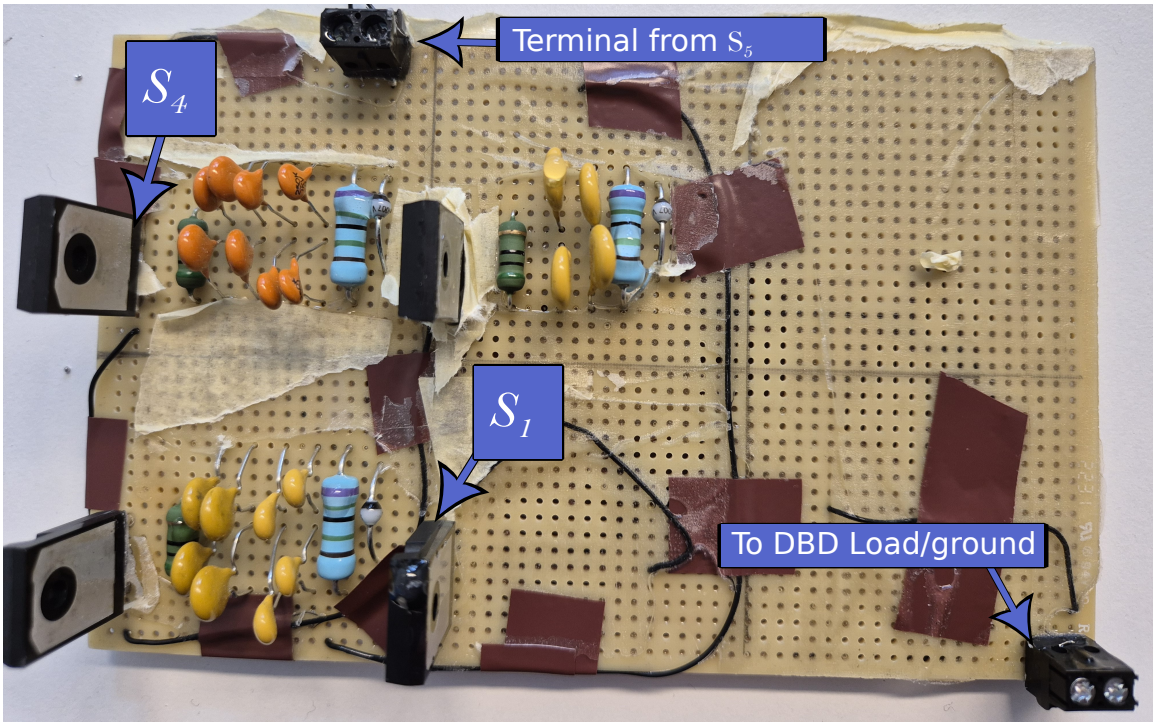


Figure D.3: Image of the top-side of the supercascode prototype, featuring S_4 to S_1

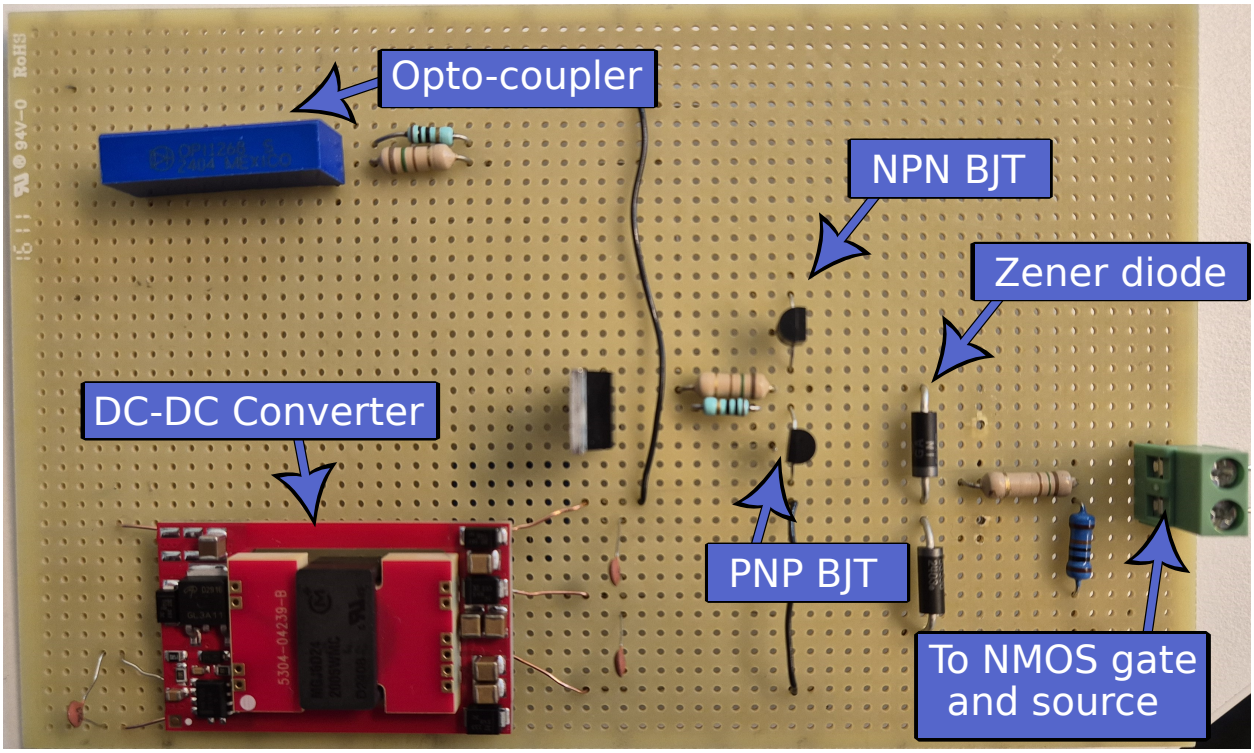
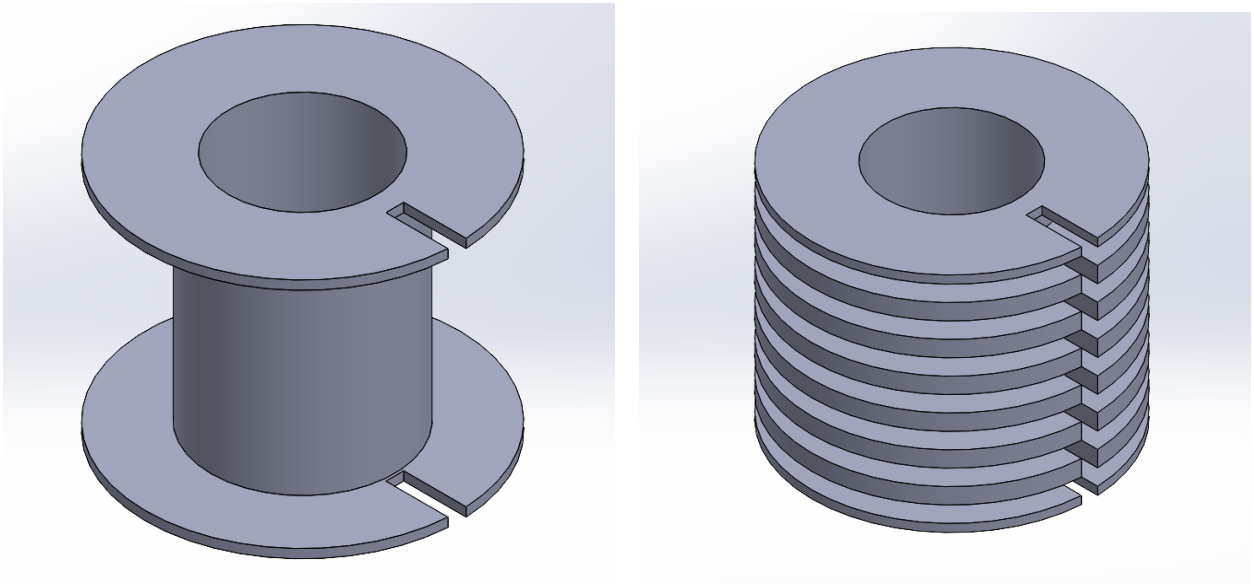


Figure D.4: Image of the top-side of the gate-driver sub circuit for the supercascode

Figure D.5: The ferrite core with added tape "air gap" to reduce inductance.



(a) Primary bobbin. **(b)** Secondary bobbin.

Figure D.6: 3D models of the transformer bobbins.

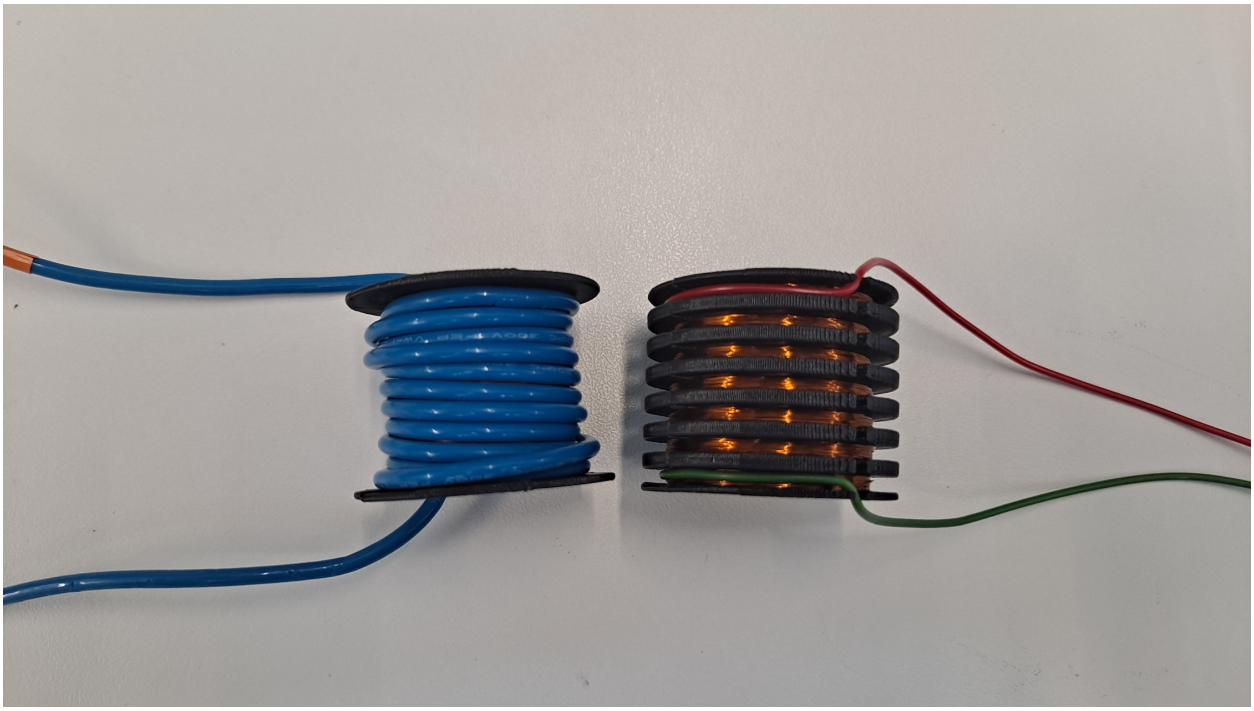


Figure D.7: The completed primary (left) and secondary (right) windings.

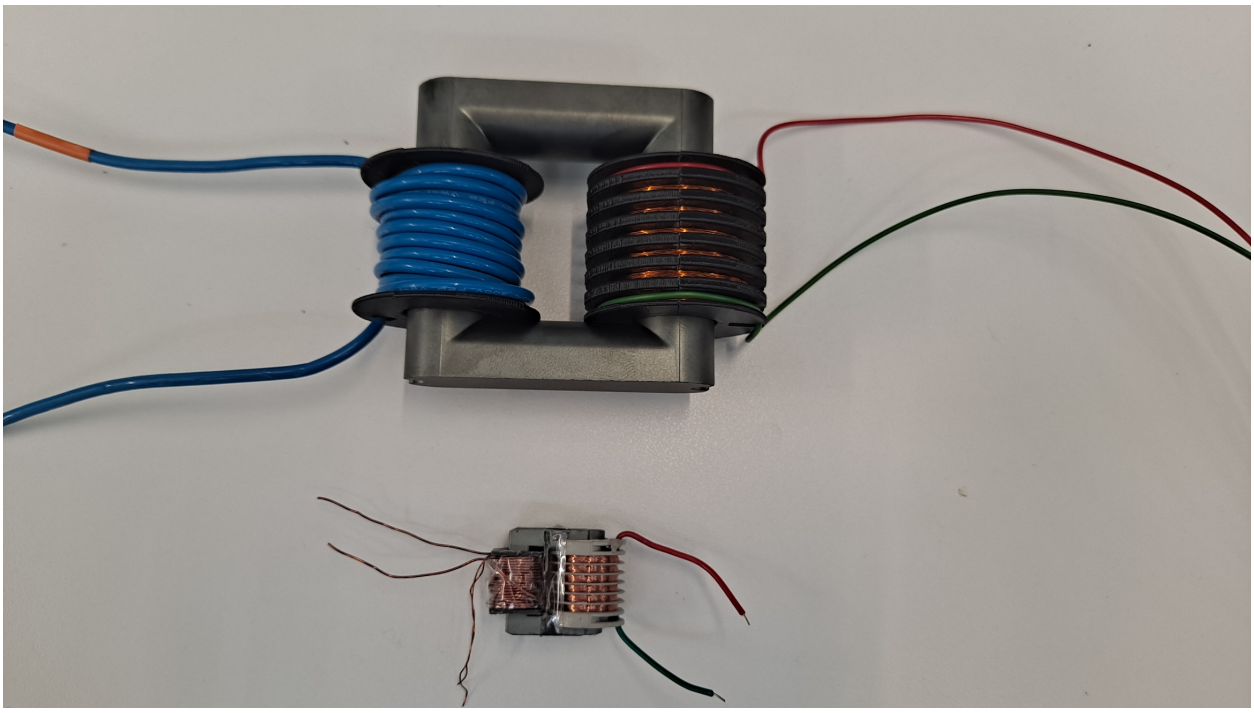


Figure D.8: The hand made transformer (top) with a commercial high voltage transformer (bottom).