Texturing approaches for the fabrication of nc-Si:H/c-Si tandem devices

by

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to obtain the degree of Master of Science in

Sustainable Energy Technology

at the Delft University of Technology,
to be defended publicly on Friday October 11, 2019 at 13:30 PM.

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Acknowledgment

Hereby, I would like to express my gratitude for everyone who helped indirectly or contributed directly to this work. Some of which I would like to name them personally. First, I would like to thank my daily supervisor Thierry de Vrijer for always being supportive and reachable whenever I need him. The constructive discussions we had on weekly basis and the freedom I had motivated me to overcome all challenges throughout my thesis work. I would like to express my gratitude to Prof. Arno Smets who inspired me to enter the world of Photovoltaics through the passion he showed in his lectures and his continuous personal support during my study period in Delft. Finally, I would like to thank Gianluca Limodio and Yifeng Zhao for the help they offered in some of the lab sample's preparation. Special thanks to the staff of Else-Kooi laboratory for their cooperation and the users for their solidarity. I would like to take this opportunity to thank the board members of the graduation committee for their effort and time to evaluate my thesis work. Special thanks to my friend Mamdouh ellamie for motivating me to finish writing my thesis report. Last but not the least, My parents and siblings for their love and support.

Abstract

This thesis is dedicated to the fabrication of a novel silicon based tandem cell which combines hydrogenated nanocrystalline silicon (nc-Si:H) thin film (TF) photovoltaic (PV) technology and silicon heterojunction (SHJ) c-Si based PV technology. As a matter of fact, the growth of nc-Si:H on a flat c-Si substrate is not uniform as it irregularly peels off after deposition using the plasma enhanced chemical vapor deposition (PECVD). On the other hand, the growth of the nc-Si:H TF layers on the standard alkaline textured c-Si substrate with sharp pyramidal structures results in defective regions in the bulk of nc-Si:H grown material. A nc-Si:H layer with high defect density reduces the voltage and the fill factor (FF) of the tandem device. In order to minimize the defect density in the nc-Si:H absorber layer, different texturing approaches (TA) were developed for the c-Si wafer to facilitate better growth of the nc-Si:H absorber. The surface morphology of the textured c-Si wafers for all TA's at different etching time steps were investigated. Prior to TF layer deposition for the SHJ and the tandem devices, various cleaning approaches were investigated to improve the surface passivation of the textured c-Si wafers. The investigation of the grown nc-Si:H layer using different TA's showed that smoothening of the sharp pyramidal structures significantly improved the nc-Si:H grown bulk as it helped in better growth of nc-Si:H with no significant defects. Finally, the current density-voltage (J-V) measurements were investigated for all TA's for the SHJ and the tandem devices. The best performing tandem cell has an open circuit voltage (V_{oc}) of 1.02 V , short current density (J_{sc}) of 13.34 mA/cm-2 and a FF of 0.44. It is expected that optimizing the tunnel recombination junction (TRJ) will further improve the electrical performance of the tandem devices for all TA's.

Contents

List of Figures

List of Tables

1 Introduction

1.1. Motivation

Up until now, the global energy demand is mainly met by fossil fuels. In 2015, global power consumption has reached 17.4 terawatts [21]. The global population is expected to grow by 2.5 billion over the next decades. As a result, the global energy demand will likely increase by more than 30% before the end of 2040 [22]. According to The British petroleum Energy Review for 2017 [1], it is stated that the global primary energy generation is still dominated by fossil fuels by 85% despite the depletion of conventional fossil fuel energy sources. The main threat of burning fossil fuels is the increase of greenhouse gas emissions that cause global warming which will further lead to irreversible damages as a result of climate change. In order to meet the continuous increase in the energy demand, while reducing greenhouse gas emissions, a transition towards clean and renewable energy generation is required.

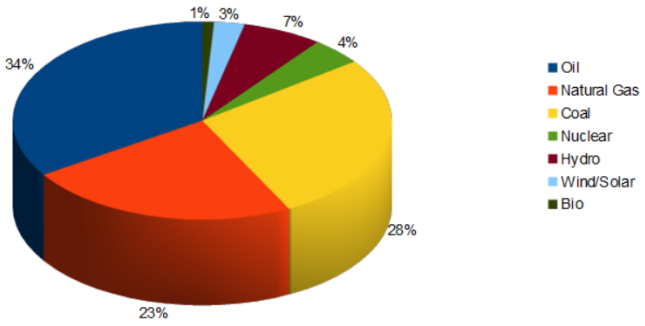


Figure 1.1: Global primary Energy Generation 2017 [1]

Photovoltaics (PV) is a promising clean sustainable technology which converts sun light energy into electricity. Over the last decades, crystalline silicon (c-Si) based cells, also known by first generation solar cells have shown high reliability in the PV market with a production share of 95% in 2017 [23]. Silicon is a cheap, non-toxic semiconductor material and it is the second most abundant element in earth's crust. C-Si based cells are mainly used for terrestrial applications. Seeking higher efficiencies led to the investigation of multi-junction solar cells. Second generation solar cells were further developed to lower the price of the bulk crystalline cells by depositing semiconductor layers as thin films on substrates such as glass, roof sheets and plastics. Amorphous silicon (a-Si) is a non-crystalline form which is used as an absorber layer in thin film PV technology. Apart from a-Si, other absorber materials have been established with higher efficiencies than a-Si based cells. These materials include cadmium telluride (CdTe) and copper indium gallium diselenide (CIGS). Despite high efficiencies of CdTe and CIGS based solar cells, scarcity of In,Ga and Te elements and the complex deposition techniques made them not sustainable for industrial large scale production.

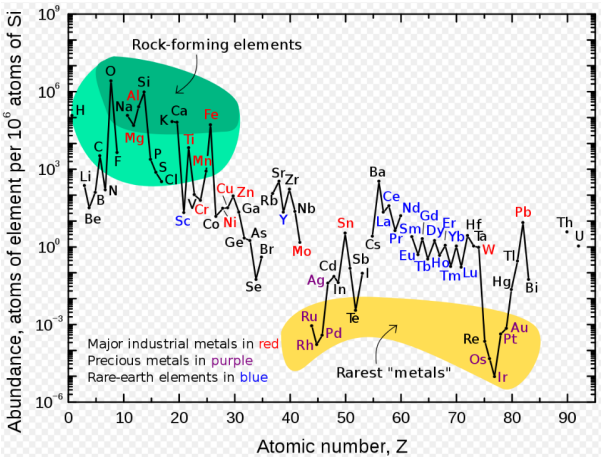


Figure 1.2: Abundancy of elements in earth's crust [2]

1.2. Solar radiation

The sun is the by far the most powerful source of energy for life on the earth. Around 150 million kilometers away from the earth, the sun emits electromagnetic radiation that is incident to the earth. A photon represents a quantum of light. The energy of a photon E_{ph} is proportional to the radiation frequency and is expressed by:

$$E_{ph} = \frac{hc}{\lambda} \tag{1.1}$$

where E_{ph} is the energy of the photon, h is the Planck constant, c is the speed of light in vacuum and λ is the wavelength of the incident photon [24]. As stated, by equation 1.1, photons with the shortest wavelengths have the highest energies. Depending on their wavelength, electromagnetic waves are classified into different ranges starting from short gamma waves up to extremely long radio waves. The ranges of the electromagnetic waves are depicted in Figure 1.3. The visible light range is approximately between 400 nm and 700 nm. All ob-

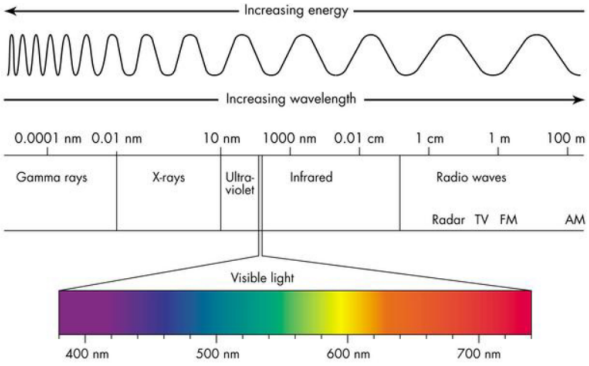


Figure 1.3: Electromagnetic spectrum-the ranges [3]

jects (with T>0K) emit radiation. Their spectral radiation depends on their temperature. Black body radiation demonstrates the relationship between the temperature of an object and the frequency of the electromagnetic radiation. An ideal black body absorbs all electromagnetic radiation received and then emits it back in a non-continuous spectrum. At the chromosphere, the outer surface of the sun, the temperature is approximately 5800 degrees kelvin(K). Due to the far distance between the sun and the earth and reflection losses, not all electromagnetic radiation is absorbed by the Earth. Just above the atmospheric layer surrounding the earth, the incident power density from the solar radiation is about 1353 $W.m^{-2}$ at Air mass zero (AM0). Air

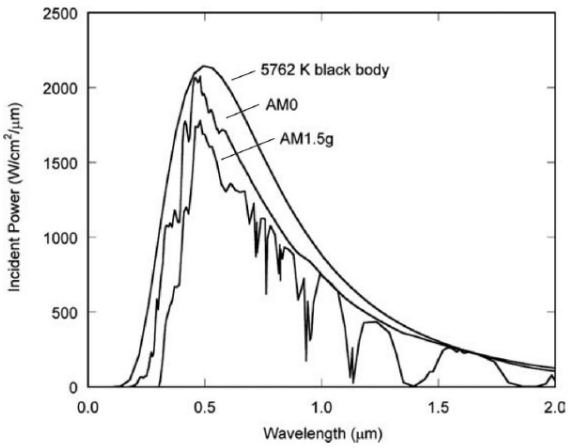


Figure 1.4: Spectral radiation for a blackbody at T=5762K., the AM0 spectrum and the AM1.5 spectrum [4]

mass is a relative measure of the optical length of the atmosphere. It can be used to determine the solar radiation incident on the earth after passing through the atmosphere. Equation 1.2 expresses the air mass as function of the incident angle θ.

$$AirMass = (\cos\theta)^{-1} \tag{1.2}$$

At θ= 0 ° (degree), the sun is positioned directly overhead and is referred as AM1. In order to analyse the performance of the solar cells, the solar modules are tested under standard test conditions at AM1.5 with incident angle of 48.2 °, normalized power density of 1000 W.m^{-2} and a module temperature of 25 C °. Figure 1.4 shows the spectral radiation for a black body, AM0 and AM1.5 as a function of wavelength. Depending on the solar cell technology, only incident photons with sufficient energy will be absorbed by a solar cell. Low energetic photons will not contribute to the generation of electric charge carriers. To further understand which photons contributes in the current generation, basic operational principles of Photovoltaic Solar Cells will be explained in the next section.

1.3. Basic operational principles of Photovoltaic Solar Cells

Solar cells are electrical devices that generate electricity upon exposure to the sunlight. This process is the photovoltaic effect. It entails generation, separation and collection of charge carrier upon absorption of a photon. A single junction silicon solar cell is composed of p-type and n-type region forming a p-n junction. Silicon as an intrinsic material without added impurities is a semiconductor material that has 4 electrons in the valence band. It has an intermediate conduction property between a conductor and an insulator. Electrons flow freely in the conductors while for the insulators, it requires extremely high amount of energy to excite the electrons which are strongly bounded in the valence band. On the other hand,the flow of electrons in the semiconductors can be conducted under certain conditions. In order to excite the electrons from

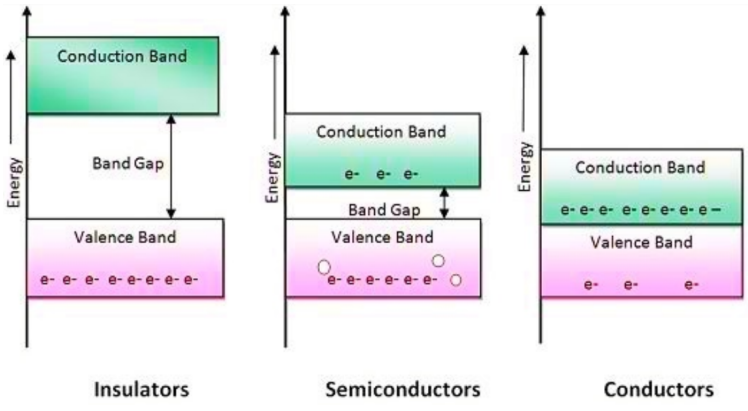


Figure 1.5: Energy band diagram for insulators, semiconductors and conductors [5]

the valence band to the conduction band where the electrons can move freely, certain amount of energy is required namely the Binding energy. Figure 1.5 shows the energy band diagram for the three different materials. Band gap is the set of energy levels between the valence band and the conduction band. Insulators have a very wide band gap between the valence band and the conduction band compared to semiconductors, while conductors have no band gap. Regarding the semiconductors, E_p larger than the binding energy will excite an electron from the valence band to the conduction band. When an electron is excited to the conduction band, a hole replaces the position of the excited electron. A hole is a virtual positive charge carrier that also contributes in generating the current. However, separation and collection of generated charge carriers at different terminals is required. As aforementioned earlier in this section, a solar cell is based on a p-n junction.

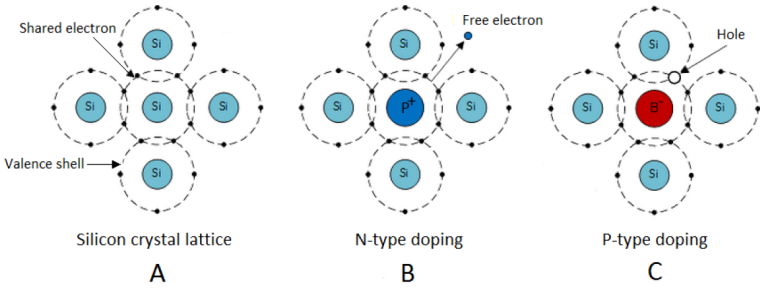


Figure 1.6: A) Crystalline structure of intrinsic silicon B) N-type doped silicon and C) P-type doped silicon [6]

Intrinsic silicon is doped with phosphorus and boron atoms forming n-type and p-type layers respectively. Phosphorus has 5 valence electrons. Doping silicon with phosphorous atoms will add an extra electron to the n-type layer for each added atom. This occurs since silicon atom requires only 4 electrons to become stable. On the other side, for the p-type layer, boron atom has only 3 valence electrons. Doping silicon with boron will leave a hole vacancy for each boron added atom. Introducing such impurities form a n-type layer with majority of electron charge carriers and a p-type layer with majority of hole charge carriers. Due to the charge carrier concentration difference in the p-n junction, electrons diffuse from the high concentration n-type region to the low concentration p-type region, whereas holes diffuse in the opposite direction from the p-type region to the n-type region. Transferred Electrons and holes as minority carriers will recombine with the opposite majority charge carriers in the p-type and n-type respectively. This flow creates an internal electric field in the depletion region triggered by the charged ions of the dopants.

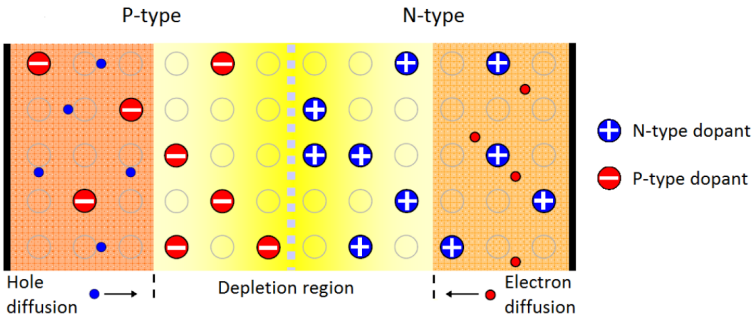


Figure 1.7: P-N junction at equilibrium [7]

Figure 1.7 shows the p-n type junction at equilibrium. Under illumination, the incident E_{ph} greater than the band gap will generate an electron-hole pair. Generated minority carriers in the p-type and n-type region will diffuse towards the depletion region as a result of the concentration gradient. The internal electric field in the depletion region will drift the generated electrons to the n-type region and holes to the p-type region. After the separation of the generated electron-hole pair, charge carriers are collected using high conductive metal electrodes.

1.3.1. Solar cell external parameters

External parameters are used to determine the performance of a solar cell. These parameters are the short circuit current density (J_{sc}), the open circuit voltage (V_{oc}), the maximum power point (MPP) and the fill factor

(FF). The conversion efficiency of a solar cell is determined using the above-mentioned parameters which

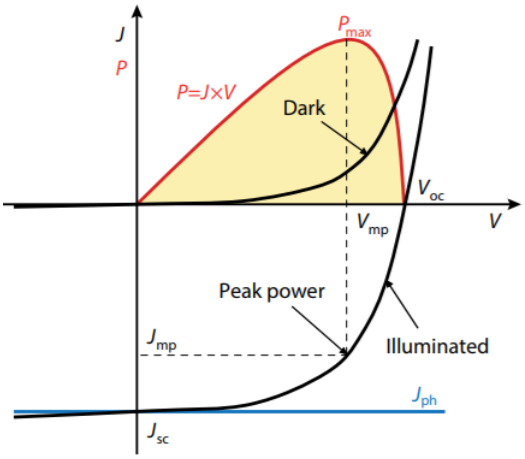


Figure 1.8: J-V characteristics of a p-n junction in the dark and under illumination [8]

are illustrated in figure 1.8. The J-V measurements for a solar cell are performed under the standard test conditions of the AM1.5 spectrum, a power density of 1000 W.m^{-2} and a temperature of 25 C°.

- J_{sc} is defined as the current per unit area flowing through an external circuit when the two metal electrodes of the cell are short-circuited. In the ideal case, assuming uniform generation of charge carriers and no surface recombination, photo-generation current (J_{ph}) will be equal to J_{sc}.

- V_{oc} is defined as the voltage measured when no current flows through the external circuit. It is the maximum built up voltage a solar cell can deliver. V_{oc} can be derived as shown in equation 1.3.

$$V_{oc} = \frac{K_B T}{q} \ln\left(\frac{J_{ph}}{J_o} + 1\right) \tag{1.3}$$

  Where K_B is Boltzmann constant, temperature T, unit charge q, and J_0 is the saturation current density.

- **MPP** is defined as the operating point at which the delivered power of the solar cell is maximum. Power is the product of the voltage and the current. V_{mp} and J_{mp} are the (x,y) coordinates of the maximum power point.

- **FF** is defined as the ratio between the maximum power that can be generated by a solar cell and the product of V_{oc} and J_{sc} expressed in equation 1.4.

$$FF = \left(\frac{V_{mp} J_{mp}}{V_{oc} J_{sc}}\right) \tag{1.4}$$

  The conversion efficiency η of a solar cell is the ratio between the generated power to the incident power Pin expressed in equation 1.5.

$$\eta = \left(\frac{J_{sc} V_{oc} FF}{P_{in}}\right) \tag{1.5}$$

1.3.2. Limits of photovoltaic silicon solar cell

There are some limitations for PV cells for the power produced relative to the incident power. As aforementioned in section 1.3.1, not all light photons contribute in the current generation. Figure 1.9 shows the energy of the AM1.5 spectrum that can be utilized by a single junction c-Si solar cell with a bandgap energy of 1.1 electron volt (eV). In one hand, Spectral losses, indicated by the grey area in figure 1.9, are the main loss mechanisms in solar cells which account for approximately 50% of the power losses. Only photons with energy higher than the band gap of the absorber layer will excite electrons from the valence band to the conduction band. Excess energy of the band gap will be lost as a form of heat where electrons will settle back to the bottom of the conduction band. This process is called thermal relaxation. Photons with lower energy

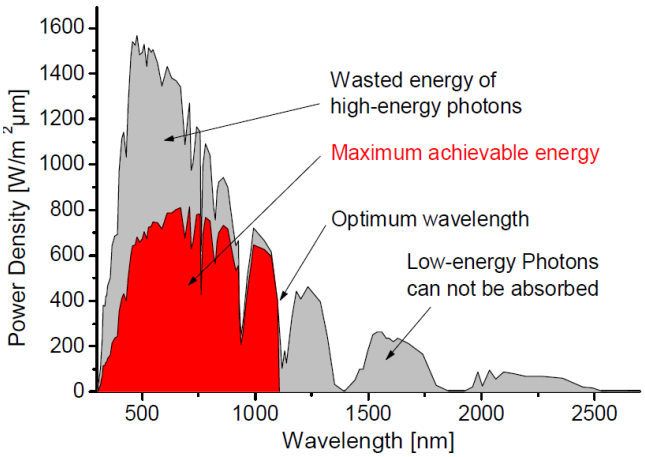


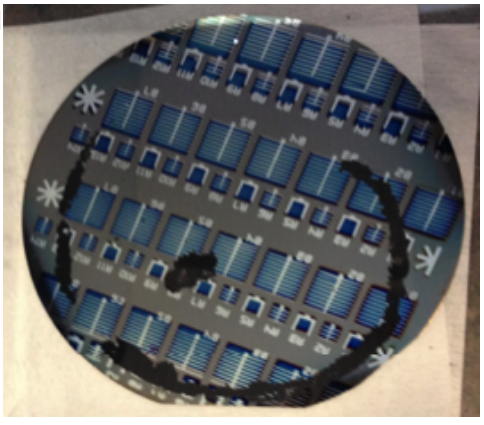
Figure 1.9: Spectral losses and the maximum achievable energy for c-Si solar cell of AM1.5 spectrum [9]

than the band gap beyond the optimum wavelength (c-Si bandgap) will not be absorbed. The red area indicates the maximum achievable energy that can be utilized by a c-Si solar cell. On the other hand, there are other loss mechanisms that limit the conversion efficiency of PV cells. These losses include charge carrier recombination of the generated charge carriers and radiation emitted by solar cell itself. According to Shockley-Queisser limit, the maximum theoretical conversion efficiency for a single p-n junction is 30% at band gap of 1.1 eV. Under the standard test conditions of AM1.5 and on laboratory scale, single junction c-Si solar cells have reached a V_{oc} up to 0.72 V and a maximum achievable J_{SC} above 42 mA.cm^{-2} [25].

1.4. Research question and outline of the thesis

As aforementioned in the previous section, single junction c-Si solar cells deliver an open circuit voltage (V_{oc}) of up to 0.72 V on laboratory scale. Achieving higher voltage from Si based cells can be obtained by developing multijunction solar cells. The purpose of this thesis is to fabricate a Si based tandem cell that combines c-Si wafer technology and Thin film (TF) technology that can be used for high voltage stand-alone systems. For this purpose, a tandem cell is chosen with a Silicon heterojunction (SHJ) as the bottom cell and a thin film hydrogenated nano-crystalline (nc-Si:H) as the top cell. In fact, nc-Si:H cannot grow properly on a flat smooth silicon wafer as it will peel off right after deposition. It can attach much easier to a surface with a rougher morphology. Standard Alkaline texturing of c-Si wafers give rise to large sharp pyramidal structures of over a few microns. Depositing thin layers on top of this texture profile results in a defective nc-Si:H grown bulk material full of cracks.

[(a)]



[(b)]

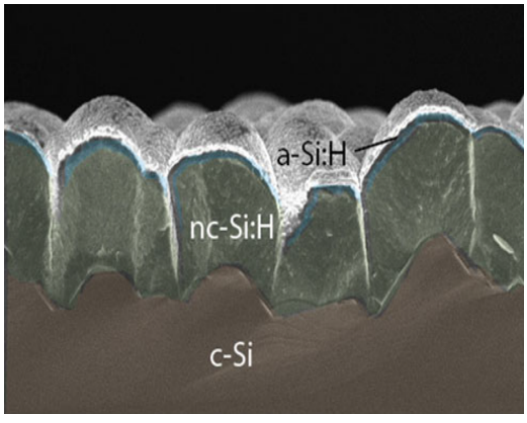


Figure 1.10: a) Growth of the nc-Si:H on a flat c-Si wafer[Photo courtesy of P. RODRIGUEZ] and b) SEM image of the nc-Si:H growth on standard pyramidal structures of textured c-Si wafers [10]

The aim of the thesis is to develop a texturing approach (TA) to optimize a surface texture for the c-Si sub-

strate for better growth of the nc-Si:H bulk on the c-Si surface. The main research question is whether these TA's can improve the surface morphology of the c-Si absorber layer of the bottom cell. This improvement will facilitate better deposition of nc-Si:H top cell which will enhance the performance of the tandem cell. In this paper, three TA's are developed which will be further explained in chapter 2. The processing tools which are used for the fabrication of the tandem cell and the characterization equipment will be covered in chapter 3. The obtained results of nc-Si:H/SHJ tandems using the three different TA's are presented in chapter 4. Finally, the conclusion of the most important findings of this thesis and recommendations for the future research work are presented in chapter 5.

2

Theoretical background

This chapter is divided into three sections. The first section provides information regarding the developed wet texturing approaches (TA) in this thesis work. The second section explains different cleaning techniques that were used to clean the textured wafers before the deposition of thin film layers of the solar cells. Finally, the design of SHJ and tandem cells will be illustrated in the third section.

2.1. Texturing approaches

Wet chemical etching is widely used in the solar cell industry for the surface texturization of the c-Si solar cells. The resulting morphology of the surface texture is highly dependent upon the type of the chemical etchant, specifically upon the isotropy or the anisotropy of the chemical etching. Alkaline etchants such as sodium hydroxide (NaOH), potassium hydroxide (KOH) or tetra-methyl-ammonium hydroxide (TMAH) are anisotropic etchants. On the other hand, Acidic etchants which are for instance based on hydrogen fluoride (HF) and Nitric acid (HNO_3) are classified as isotropic etchants. In this section, an overview of the three developed TA will be presented.

2.1.1. TA1

In this texturing approach, two different wet chemical etching techniques were used namely alkaline and acidic etching respectively. In alkaline etching, the main ion involved in etching the silicon is the hydroxyl ion (OH^-), that attacks the silicon atom [26]. The reaction of OH^- with silicon is expressed as follows:

$$Si + 2OH^- \rightarrow Si((OH)_2)^{2+} + 4e^- \tag{2.1}$$

The ions of the silicon crystal react with H_2O in the alkaline solution. Simultaneously, H_2O breaks down and produces hydrogen gas as shown in the equations 2.2 and 2.3 [27, 28, 29]. The continuous regeneration of OH^- ions maintains the chemical etching of silicon in which the OH^- ions attack again the neutral silicon atoms .Isopropyl alcohol (IPA) is added to control the etch rate and to prevent the explosive reaction between silicon atoms and the OH^- ions [30].

$$4H_2 + 4e^- \rightarrow 4H_2O^- \tag{2.2}$$

$$4H_2O^- \rightarrow 4OH^- + 2H_2 \tag{2.3}$$

In case of (100) oriented silicon wafer, the alkaline chemical etching results in forming random pyramids on the surface. Such pyramids are formed by anisotropic etching in which the etching rate depends on the crystallographic orientation of the silicon atoms. The difference in the etching rate is related to the different plane densities in (100) and (111) directions [31]. Figure 2.1 shows (111) and (100) c-Si planes and the bond configuration of silicon atoms for both orientations.

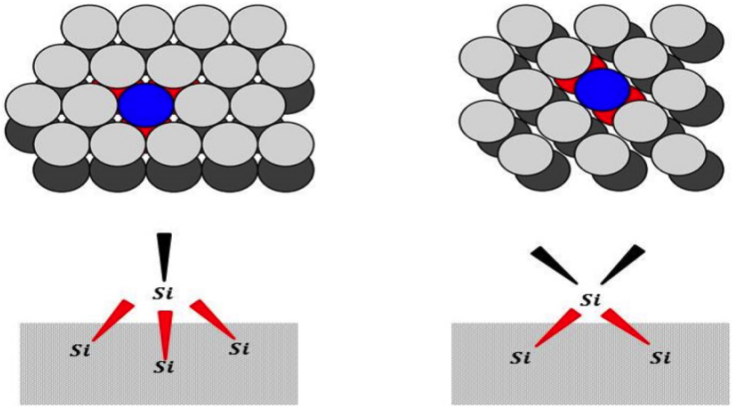


Figure 2.1: (111) and (100) c-Si planes and the bonding configuration of silicon atoms in both orientations [11]

Silicon atoms in the (111) orientation has higher density than the silicon atoms in (100) orientation. The difference in the silicon atomic density is attributed to the dangling bonds in each orientation. In (111) orientation , Si atom is bonded to 3 (Si-Si) back bonds (shown in red) and 1 dangling bond (shown in black). While in (100) orientation, Si atom is bonded to 2 (Si-Si) back bonds with two dangling bonds. During etching , three OH^- ions are required to break down 3 (Si-Si) back bonds in (111) orientation rather than 2 OH^- ions in the (100) orientation [32, 33]. As a result, the etch rate will be much faster in (100) direction than in (111) forming a pyramidal structure of (111) facets. At low concentrations of the alkaline etchant, the formed pyramids on the surface of the (100) oriented c-Si wafers are up to 10 µm in height depending on the etching time and the temperature of the etching process [34].

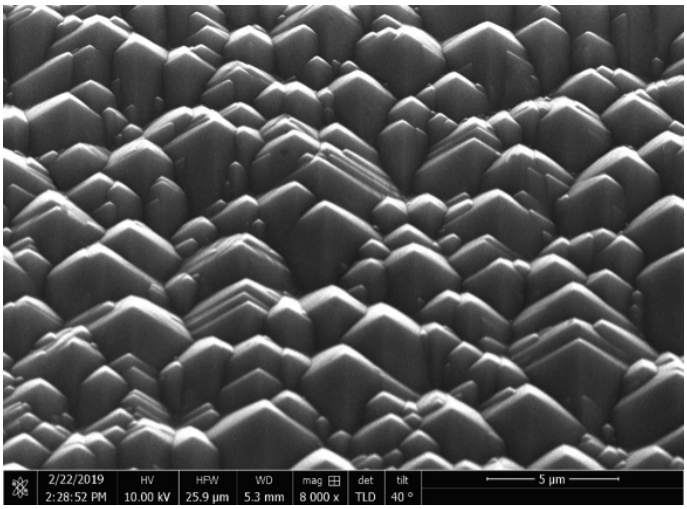


Figure 2.2: SEM Image of the pyramidal textures of alkaline etching at low TMAH concentration for 7min[courtesy of T.de vrijer]

After the formation of the pyramidal textures, acidic etching is employed to isotopically smoothen the sharp pyramidal features into smoother textures. In contrary to the anisotropy of the alkaline etching, the isotropic etching rate is to a large extent orientation independent. The fundamental mechanism of the HF:HNO_3 acidic etching is based on an oxidization-reduction reaction [34]. As expressed in equations 2.4 and 2.5, silicon is oxidized by HNO_3 and Nitrous acid (HNO_2), meanwhile, the formed silicon oxide is removed by HF.

$$HNO_3 + Si \rightarrow SiO + HNO_2 \tag{2.4}$$

$$2HNO_2 + Si \rightarrow SiO_2 + H_2O + 2NO \tag{2.5}$$

In fact, HNO_2 is the active species in the oxidation reaction. It is formed by two steps process. Firstly, HNO_2 reduces the undissociated HNO_3 which is the rate determining step. In the second step, HNO_2 is generated much faster from the resulting reaction products.

$$HNO_2 + HNO_3 \leftrightarrow N_2O_4 + H_2O \tag{2.6}$$

$$N_2O_4 + 2NO + 2H_2O \leftrightarrow 4HNO_2 \tag{2.7}$$

The reduction reaction of the formed oxide is rate limited by the oxidation step by HNO_3, whilst in the regions with higher ratios of HNO_3 to HF, the diffusion of the HF is the rate limiting factor for etching the formed oxide. The etch rate can be further lowered by adding a diluent [12]. H_2O or Acetic acid (CH_3COOH) is commonly used as a diluent for the HF:HNO_3 oxidation-reduction reaction. Figure 2.3 shows the etch rates as a function of the etch composition of a diluted HF:HNO_3 system. As the proportion of the HF increases in the HNO_3 rich regions, approximately past the ratio of 20:80 (region C), the etching rate increases significantly, up to an etch peak at region A. Up to a critical value, the addition of a diluent lowers the etch rate as the oxidizing rate in the solution is reduced.According to [34], the dilution of CH_3COOH up to 40% barely affects the etch rate for high HNO_3 rich regions. Therefore, lowering the etch rate requires diluent proportion beyond 40%.

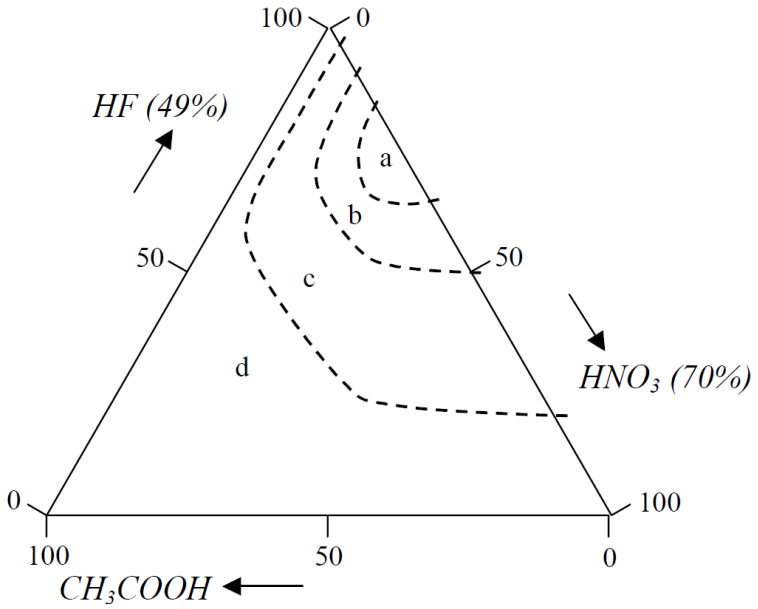


Figure 2.3: Etch rates as a function of the etch composition HF:HNO_3:CH_3COOH system using triangular coordinate system. Etching rate at region (a) > 1000 µmin^{-1}, (b) > 500 µmin^{-1}, (c) > 50 µmin^{-1}, and (d) 0-50 µmin^{-1} [12]

2.1.2. TA2

In this texturing approach, alkaline isotropic etching is applied on a (100) oriented c-Si wafer. The main aim of this TA is to the increase the surface roughness by forming small pyramidal features on the flat surface of the wafer. As previously mentioned, at low concentration alkaline etching , pyramids up to 10 µm are formed based on the etching parameters of the process. Figure2.4 visualizes the development of the pyramidal structures. The etching process starts with random nucleation of the pyramids on the wafer surface[25]. During the etching procedure, the number of the nucleated pyramids sporadically increases as well as the size of the formed pyramids increases with time. As a result, the surface is gradually covered with pyramidal structures. In this thesis work, surface textures at the early stages of this etching process will be investigated.

2.1.3. TA3

For this texturing approach, a sacrificial layer of silcon oxide (SiO_x)/poly silicon was first deposited on the c-Si wafers. Using an ultraviolet (UV/O_3) excimer source, an ultra-thin (SiO_x) layer, approximately 1.5nm, was dry-chemically grown. Subsequently, a 15 to 20 nm thick layer of a Boron doped a-Si was deposited on both sides by Plasma enhanced chemical vapor deposition (PECVD). The wafers were then subjected to

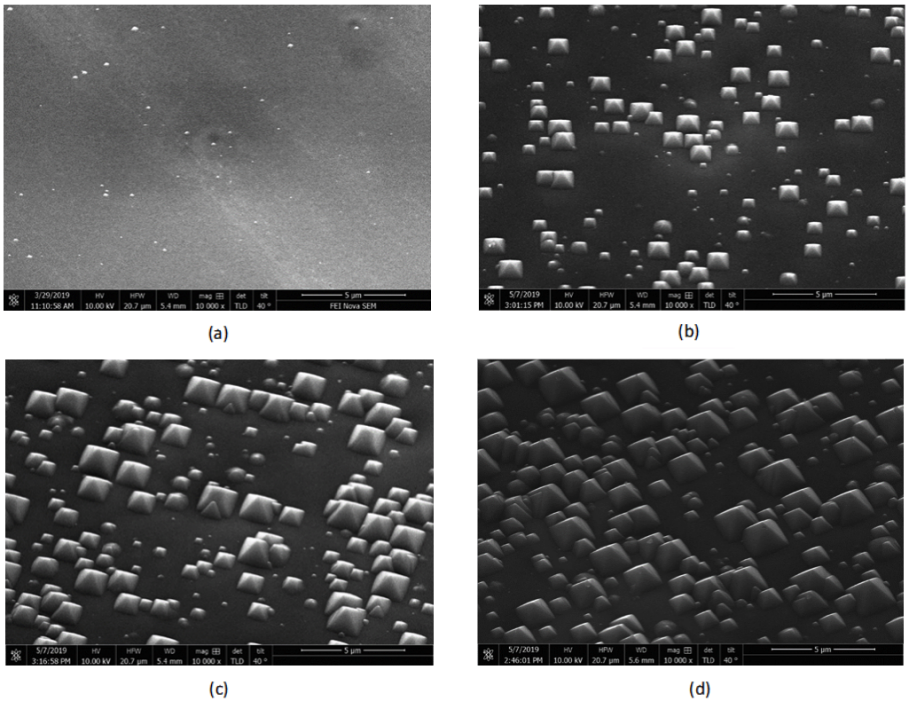


Figure 2.4: SEM Images for the Development of pyramidal texture at low TMAH concentration for the surface of (100) c-Si wafer after a) 30sec , b) 60 sec, c) 2 min and d) 3 min of etching.[photos courtesy of T. de Vrijer]

high-temperature furnace anneal at 950 °C for 3 minutes under nitrogen atmosphere to activate the dopants. Annealing at 900 °C or above changes entirely the a-Si layers to a poly-crystalline structure [35, 36]. After the deposition of the sacrificial layer, the wafers were isotopically etched to completely remove the sacrificial layer. During the etching process, the etch rate differs from one region to another. The etch selectivity of this TA is due to the grain boundaries between the poly-crystalline structure of sacrificial layer and the mono-crystalline structure of the c-Si wafer. When the sacrificial layer is completely etched away, a concave pit structure is formed.

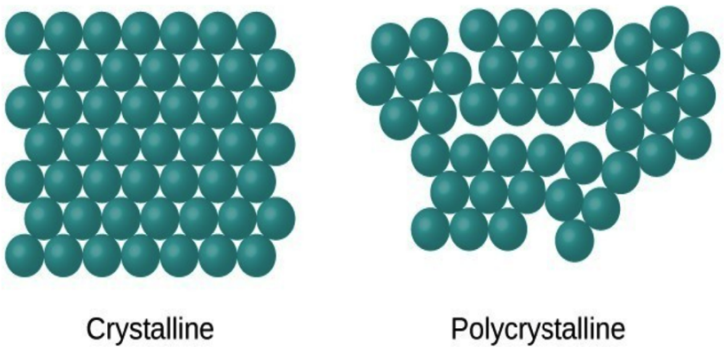


Figure 2.5: Atomic structure of monocrystalline and polycrystalline silicon [13]

2.2. Cleaning techniques

After texturing the c-Si wafers, a pre-cleaning step is performed before proceeding to the thin films deposition procedure by PECVD. The textured samples were cleaned to remove the surface contaminants and the native oxides for better surface passivation. Nitric acid oxidation cycle (NAOC) is a wet cleaning method that is commonly used for cleaning the c-Si wafers. NAOC entails oxidation-reduction reaction using HNO_3 and HF respectively. The main concern of using this method is that it may influence the surface morphology for some of the textured wafers. For this reason, different cleaning approaches (CA) were investigated using wet and dry-cleaning methods. In this work, two wet cleaning methods were used namely the Radio Corporation of America (RCA) and the NAOC. In addition, a dry-cleaning method, hydrogen plasma dry cleaning (HPDC) was investigated which will be further explained in this section.

2.2.1. NAOC

NAOC is a wet cleaning method that entails oxidation-reduction reaction using HNO_3 and HF respectively. Firstly, c-Si textured Wafers are immersed for 10 minutes in a 99% HNO_3 at room temperature. Subsequently, the samples were immersed for 10 minutes in a 69.5% HNO_3 at 100 °C. As a result, a silicon oxide layer is formed with a thickness of 1-2 nm. In between the cleaning steps, the samples were rinsed in high purity Deionized water (DIW). Afterwards, the samples were immersed in a 0.55% HF at room temperature for 4 minutes to strip away the formed silicon oxide.[19] It is reported that repeating NAOC up to three cycles provides best passivation for the cleaned samples.

2.2.2. RCA

RCA is another wet cleaning method which is divided into two main steps, namely standard cleaning (SC1) and (SC2). The role of SC1 is to remove the organic contaminants by continuous oxidation-reduction reaction using ammonium hydroxide (NH_4OH) and hydrogen peroxide (H_2O_2) respectively [37]. A mixture of ammonium hydroxide (NH_4OH), hydrogen peroxide (H_2O_2) and di-ionized water (DIW) with a ratio 1:1:5 is used at temperature of 75 °C. The samples are immersed for 10 minutes in the mixture and then rinsed in DIW. The second step is SC2 which is designed to remove the metal contaminants [38]. A mixture of hydrogen chloride (HCl), H_2O2 and DIW with a ratio 1:1:5 is used at a temperature of 75 °C. the samples are immersed for 10 minutes in this mixture and subsequently, rinsed in DIW. After rinsing the samples in DIW, samples are immersed in a 1%HF at room temperature to remove the formed thin oxide layer on the surface of the textured samples [39].

2.2.3. HPDC

In this dry-cleaning method, firstly, a sacrificial layer of a-Si:H with a thickness of 4 nm was deposited on both sides of the textured wafers using PECVD. Subsequently, the sacrificial layer was completely etched away using a hydrogen plasma process. The deposition and the etching conditions with gas flows ($cm^3 s^{-1}$ expressed as sccm) used in this dry-cleaning step are given in Table 2.1. In order to determine the etching rate of the hydrogen plasma, firstly, a-Si:H layer was deposited on a clean glass substrate. The glass substrate was cleaned in an ultrasonic bath of acetone for 15 minutes, followed by 15 minutes in IPA. Subsequently, the hydrogen plasma was applied for 10 minutes. Finally, the thickness of the glass substrate was measured using spectroscopic ellipsometry.

Table 2.1: PECVD parameters for hydrogen plasma dry cleaning method(HPDC)

PECVD Parameters	**Silane** (sccm)	**Hydrogen** (sccm)	**Power** (W)	**Pressure** (mbar)	**Duration** (s)
a-Si sacrificial layer	40	-	2.8	0.7	29
Hydrogen plasma etching	-	200	6	2.8	45

2.3. Solar cell design

As aforementioned earlier in chapter 1, The design of tandem solar is composed of SHJ device as the bottom cell and a thin film nc-Si:H as the top cell. in this thesis work, a standard recipe is used to design the SHJ and

the tandem devices which are shown in figure2.6(a) and figure2.6(b) respectively [40]. As single junctions, The SHJ bottom cell has a V_{oc} of 0.69 V ,J_{sc} of 30.7 mA.cm^{-2} and FF of 0.64, whilst the nc-Si:H has a V_{oc} of 0.51 V, J_{sc} of 17.7 mA.cm^{-2} and FF of 0.61 [41].

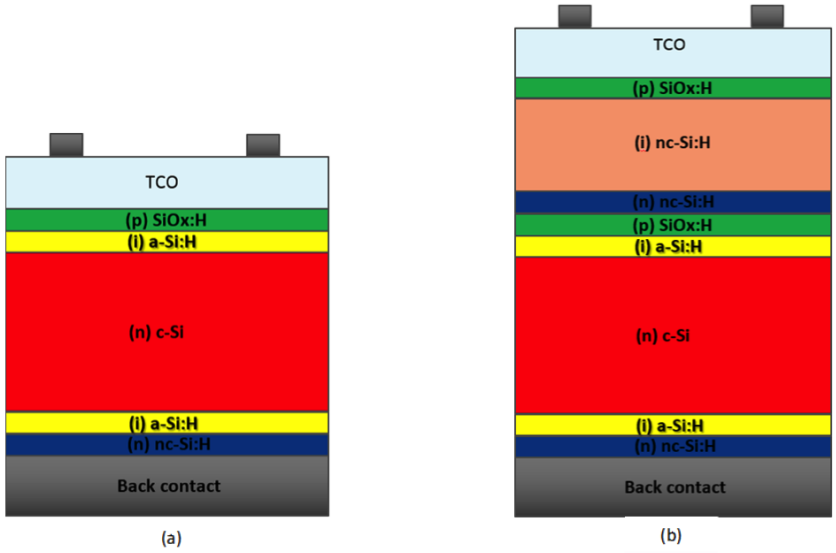


Figure 2.6: Schematic of a) SHJ solar cell and b) SHJ/nc-Si:H tandem solar cell (Schematics are not drawn to scale).

SHJ solar cell is composed of a n-type c-Si absorber layer with a thickness of 280 ± 20 µm. The c-Si absorber layer is passivated by a thin intrinsic a-Si:H layer of 30nm. At the front side, a p-type doped hydrogenated silicon oxide (SiOx:H) layer of 20nm is deposited which acts as an emitter to lower the recombination of the minority carriers at the front contact. On the back side, a n-type highly doped nc-Si:H layer of 30nm is deposited which creates a Back-surface field (BSF).The BSF creates a barrier to the minority carriers flow to the rear surface. Concerning the tandem solar cell, the top cell is based on three layers in a n-i-p configuration. The n and p layers are thin layers of approximately 30nm and 20nm respectively. The thickness of the intrinsic nc-Si:H absorber layer is rather thicker of about 2.5 µm.Concerning the tandem cell, the top and the bottom cell are monolithically connected in series via a tunnel recombination junction (TRJ) at the interface [42].TRJ ensures efficient recombination of electrons flowing from the n-type layer of top cell and the holes flowing from the p-type layer of the bottom cell at this junction. In addition, it creates an effective barrier for the generated minority carriers of both cells. As a result, the recombination losses are minimized.

3

Experimental methodology

This chapter is sub divided into 3 sections based on a chronological order in which experiments were carried out. The first section describes the cleaning and texturing procedure for the c-Si wafers. The second section shows the tools used in the fabrication process of the SHJ and the tandem devices. The third section presents various characterization techniques which are used in this thesis work.

3.1. Texturing and cleaning of the c-Si wafers setup

In this work, three texturing approaches (TA) were developed for the c-Si absorber layer in the SHJ bottom cell. All TA's were applied on a (100) oriented n-type float-zone silicon wafers from SIEGERT and Topsil with a thickness of 280 ± 20 µm, a resistivity of 1 - 5 ohm.cm and a double side polished surface finish. The texturing procedure for the wafers was carried out in the MEMS lab. For the Alkaline etching, the TMAH setup was used to anisotropically etch the wafers. The samples were immersed in an aqueous alkaline mixture which consists of deionized water (DIW), TMAH and Alkatex with the ratio of 1:5:10 respectively. Alkatex was used instead of IPA which serves as a surfactant that stabilizes the etching process. During the etching procedure, the mixture was continuously stirred at a speed of 100 RPM and the temperature was kept at 80°C. For the acidic etching, an undiluted and diluted HF:HNO_3 systems were experimented to isotropically etch the c-Si wafers. Both mixtures were prepared in a Teflon beaker at room temperature. The concentrations of the HF and HNO_3 that were used are 40% and 69% respectively. For the undiluted system, an aqueous mixture of HF: HNO_3 was prepared with a ratio 1:70 (poly-etch recipe). For the diluted HF:HNO_3 system, CH_3COOH was used as a diluent. Various ratios of HF:HNO_3:CH_3COOH were experimented which are shown in table 3.1.

Table 3.1: Diluted HF:HNO_3 mixture composition

	Recipe					
	1(a)	1(b)	1(c)	2(a)	2(b)	2(c)
Volume ratio (CH_3COOH :(HF-HNO_3))	40:60	40:60	40:60	70:30	70:30	70:30
Volume ratio (HF:$HN0_3$)	1:4	1:1	4:1	1:4	1:1	4:1

After the texturing procedure, the c-Si wafers were cleaned with 4 different cleaning approaches (CA) using dry and wet cleaning methods that are explained earlier in section 2.2. The standard cleaning steps SC1 and SC2 of RCA cleaning method were prepared in the Special application lab (SAL).The NAOC cleaning method was applied using the HF and HNO_3 bath setup in cleanroom100 in the Elsekooi lab. Finally, the HPDC was carried out using the Amor PECVD cluster tool.

Table 3.2: cleaning approaches

Cleaning approaches	Cleaning methods	Cycle(s)
CA1	RCA	1
CA2	RCA + NAOC	1
CA3	NAOC	3
CA4	(a-Si:H - H_2)	1-3-5

3.2. Processing tools

This section presents the main steps used in the fabrication of silicon heterojunction (SHJ) and the tandem solar cells. After texturing and cleaning of the c-Si wafers, the thin film layers of the designed solar cells are deposited using the PECVD. Subsequently the transparent conductive oxide (TCO) is deposited using magnetron sputtering. Finally, the front and back metal contacts are processed using physical vapor deposition (PVD).

3.2.1. Plasma enhanced chemical vapor deposition (PECVD)

The deposition of the different thin film layers of SHJ and the tandem cells is processed using PECVD cluster tool. Figure 3.1 shows a schematic diagram of a PECVD chamber. The chamber consists of two electrodes. The substrate is mounted at the top electrode which is electrically grounded. The bottom electrode is connected to radio frequency (RF) generator. The applied excitation frequency across the electrodes is 13.56 MHz for (RF-PECVD) and 40 MHz for very high frequency (VHF) PECVD [18]. The deposition procedure in the chamber is maintained at high vacuum and the temperature is controlled by heating elements. The precursor gases are introduced into the chamber. An alternating current (AC) voltage is applied across the bottom electrode and the plasma is ignited. The plasma facilitates the dissociation of molecules of the gases which produces neutral radicals and reactive ions. The neutral radicals diffuse to the substrate and adsorb to the substrate. The reactive ions also contribute in the growth of the deposited layer by ion bombardment of the substrate. There are multiple chambers used in the deposition of different layers to avoid cross-contamination of the gases.

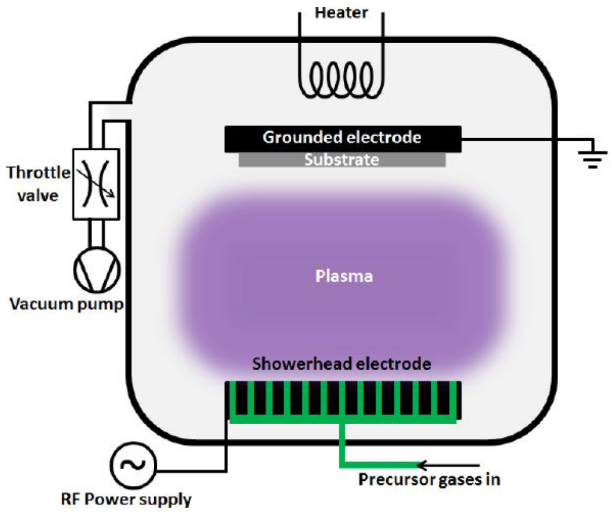


Figure 3.1: Schematic diagram of a PECVD chamber [14]

In this work, Amigo and Amor PECVD cluster tools by Elettrorava S.p.A were used in the deposition of the thin film layers [43]. Amor was used to deposit the passivation layers of a-Si:H on both sides. It has a rotation mechanism in which the deposition of the passivation layers can be applied on both sides without a vacuum break. Amigo was used to deposit the thin layers of the SHJ and the tandem cell.

3.2.2. Radio-frequency magnetron sputtering

The transparent conductive oxide (TCO) was deposited using RF magnetron sputtering. In this work, Tin doped Indium oxide (ITO) was used as it has high electrical conductivity and it is highly transparent in the visible light spectrum. RF magnetron sputtering is a physical vapor deposition (PVD) method. Figure 3.2 shows a RF magnetic sputtering chamber.

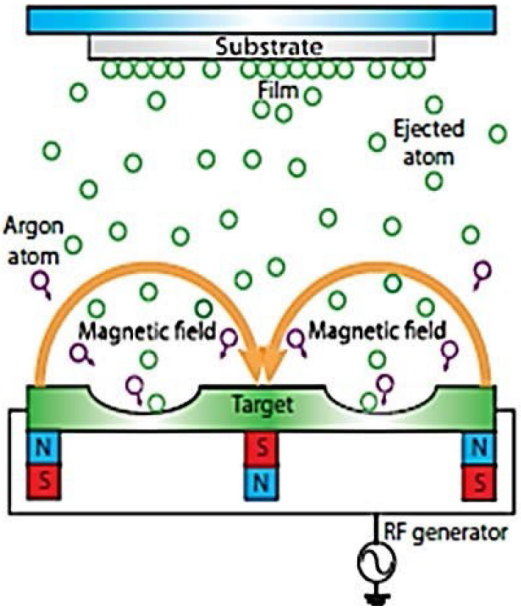


Figure 3.2: Schematic diagram of a RF magnetron sputtering chamber [15]

The deposition chamber consists of two electrodes. The substrate is mounted at the top electrode (anode) whereas, the bottom electrode (cathode) contains the target material. The deposition process occurs in vacuum chamber. An Argon plasma is ignited due to the oscillating RF magnetic field across the two electrodes. The generated positively charged argon ions bombards the target material. As a result, ITO atoms are ejected from the target. The released atoms diffuse to the substrate to facilitate the growth of the ITO [44]. In this work, the depositions of the ITO were carried out in magnetron sputtering cluster unit (Zorro) by Kurt J.Lesker Company. The ITO target material is composed of 10% SnO_2 and 90% of In_2O_3. The ITO deposition is followed by metal contact deposition.

3.2.3. Metal evaporation

The front and back metal contacts of the solar cells were processed using a physical vapor deposition. Figure 3.3 shows a schematic diagram of PROVAC, a metal evaporation unit. There are two means of metal evaporation, either by thermal evaporation or electron beam evaporation. In both means of evaporation, the target material starts to evaporate to the substrate when the melting point of the metal is reached. On one hand, the thermal evaporation involves resistive heating of the target material in the boat [44]. On the other hand, the electron beam evaporation involves heating of the target material in the crucible by an intense electron-beam.

Silver evaporates using thermal evaporation while aluminum and chromium evaporate using e-beam evaporation. The evaporation process is carried out in vacuum to reduce the formation of an oxide in the metallic film. The substrates are mounted at the rotating stage which rotates at a low speed of 10 RPM to enhance the homogeneity of the metal deposition [45]. The metal contacts are composed of 500 nm aluminium (Al), 30 nm chromium (Cr) and 300 nm silver (Ag). For the fabricated SHJ and tandem devices, the back contact is deposited on full area of the c-Si wafers which acts as back reflector for the solar devices. For the front contacts of the solar devices, a shadow mask is used to deposit the metal contacts which is shown in figure 3.4. Metal grids are deposited on the front contacts to collect the generated charge carries. All J-V measurements (section 3.3.4) were carried out for areas of (4x4 mm^2 or 1x1 cm^2) indicated by A_1 and A_2 respectively.

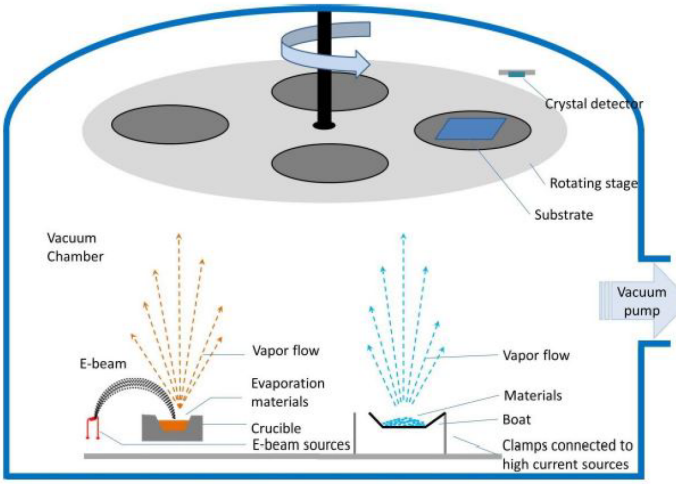


Figure 3.3: Schematic diagram of a metal evaporation chamber [16]

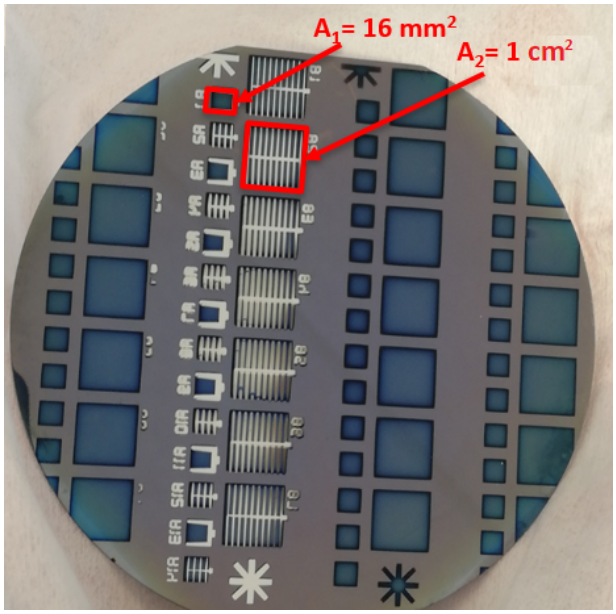


Figure 3.4: Front contact with the metal girds for the fabricated SHJ and tandem devices

3.3. Characterization measurements

In this section, the characterization techniques that were used in this thesis work are presented. These techniques were used to characterize the properties of different layers and to analyze the performance of the SHJ and the tandem devices. Specifically, the Atomic force microscopy (AFM) was used to characterize the surface morphology of c-Si textured wafers. The optical properties of the textured c-Si wafers were determined using Spectrophotometry. The minority carrier effective lifetime of the textured c-Si wafers was determined using photoconductance decay measurement. The J-V measurements of the SHJ and the tandem devices were determined using (Wacom) solar simulator. Finally, scanning electron microscopy (SEM) was used to visualize the quality of the grown nc-Si:H bulk on the SHJ bottom cell.

3.3.1. Atomic Force Microscopy

In this work, atomic force microscopy (AFM) was used to analyze the surface morphology of the textured c-Si wafers and to provide a quantitative data for the measured surfaces. Figure 3.5 shows a schematic diagram of an AFM setup.

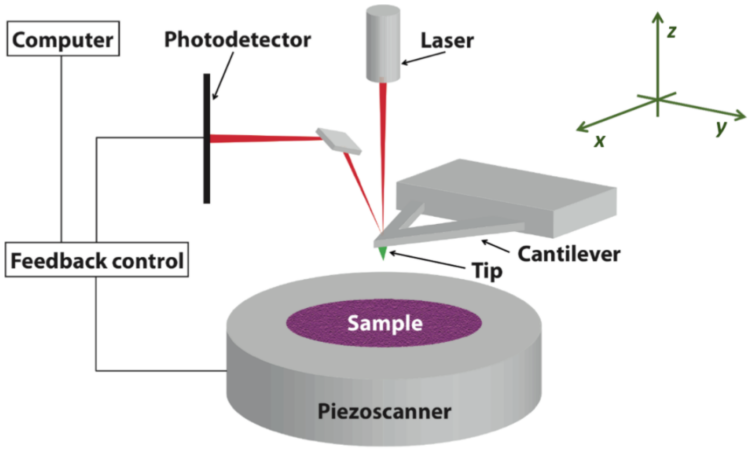


Figure 3.5: Schematic diagram of an AFM setup [17]

The sample is mounted on a piezoelectric scanner that can move in x,y and z directions. The surface of the sample is scanned by a sharp metallic tip which is attached to the cantilever. During the scanning process, the piezoelectric scanner moves while the tip remains in a fixed position. The incident laser beam on the top side of the tip is reflected onto a photodetector. When the tip tapes the surface of the sample, the forces between the tip and surface deflect the cantilever which shifts the reflection of the laser beam on the photodetector [46]. The average distance between the tip and the surface of the sample is kept constant using a closed loop system. The feedback control moves the piezoelectric scanner in the z direction, based on the displacement of the reflected laser beam on the photodetector.

In this work, the surface morphology data was obtained from a Ntegra NT-MDT atomic force microscope [47] with a polysilicon tip with a radius of 10nm and a cone angle of 30°. The AFM was used in semi-contact mode. The frequency and the speed of scanning was kept below 1 Hz and 50 µm. s^{-1} respectively. The quantitative data files obtained from the AFM scan consist of a total of 256 x 256 measured data points, and a scan area used for the samples was 10 x 10 m². The AFM data were analyzed using Gwyddion V2.52 software [48] in which the root mean square (RMS) surface roughness (σ_{rms}) and the slope distribution data of the textured features are obtained.

3.3.2. Spectrophotometry

The optical characterization of the of the textured samples was carried out by means of spectrophotometry. Spectrophotometry measures the intensity of light as a function of wavelength. In most spectrophotometers, light from halogen or deuterium light source is converted to a monochromatic beam via mirrors and diffraction grating. The converted monochromatic beam passes first through the mounted sample and then to an optical detector [18]. The measured signal that is coming from the optical detector is compared to the reference signal.Figure 3.6 shows a schematic diagram of the transmittance and the reflectance measurements in an Integrating Sphere (IS). According to the positioning of the sample, the transmittance or the reflectance of the mounted sample is expressed in relative terms of the reference beam. In this thesis work, Lambda 950 by Perkin Elmer was used to carry out the Reflectance measurements for the textured samples.

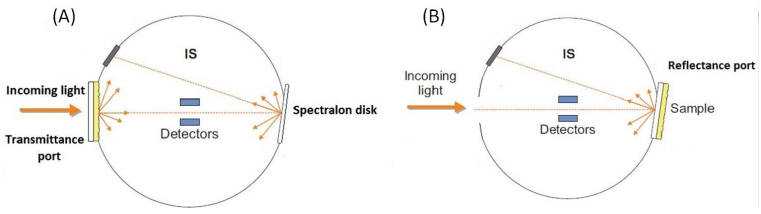


Figure 3.6: Schematic diagram of the transmittance and the reflectance measurements in (IS) [18]

The calculated reflectance is expressed as follows:

$$R = \frac{(R_{measured} - R_{dark})R_{Ref}}{R_{Ref} - R_{dark}} \tag{3.1}$$

3.3.3. Minority carrier lifetime measurement

Photoconductance decay measurements are used to determine the lifetime of the minority carriers of the textured c-Si wafers. In this work, the lifetime of the minority carriers was measured using a Sinton WCT-120 Photoconductance Lifetime tester. These measurements assess the quality of the a-Si:H/ c-Si interface of the SHJ solar cell after applying different cleaning approaches. The lifetime of the minority carriers is directly related to the V_{oc} of the solar cell. Short lifetime of the minority carriers indicates high defect density and poor surface passivation. Higher defect density implies a higher recombination of the minority carriers, thus lowering the V_{oc}. The effective carrier lifetime (τ_{eff}) can be expressed as follows:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{1}{\tau_{surface}} \tag{3.2}$$

Where τ_{bulk} and $\tau_{surface}$ are the lifetimes related to the bulk and the surface recombination processes respectively. Figure 3.7 shows a schematic diagram of the photoconductance decay measurement setup.

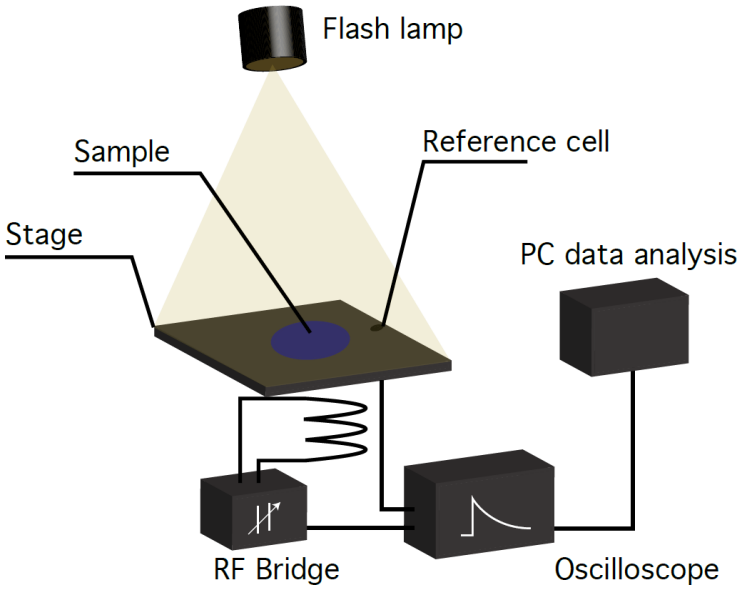


Figure 3.7: Schematic diagram of the photoconductance decay measurement setup [19]

The wafer sample is placed on the stage with a coupled coil that is connected to a RF bridge. Afterwards, the sample is illuminated by a flash lamp by which the decay time constant can be adjusted. Flashing of the wafer samples results in the generation of excess carriers. The change in the photoconductance of the sample is used to determine the effective carrier lifetime (τ_{eff}). The measured τ_{eff} can be expressed as follows:

$$\tau_{eff} = \frac{\Delta p}{G - \frac{\partial \Delta p}{\partial t}} \tag{3.3}$$

Where p is the excess minority carrier concentration and G is the photogeneration rate of the charge carriers. Photoconductance decay measurements can be carried out either in transient or steady-state mode [19]. Short light pulses imply to the transient mode whereas, long light pulses imply to the steady-state mode. In this work, transit mode is used. Generally, steady state mode is used for samples with $\tau_{eff} < 100$ µs. Both modes require to have an illumination source with much larger decay than the of the sample to ensure no photo generation of charge carriers.

3.3.4. Illuminated Current Density-Voltage (J-V)

As clarified before in section 1.3.1, the performance of the solar cells is determined by the external parameters. In this work, the illuminated current density- voltage (J-V) measurements are performed to determine the V_{oc}, J_{sc} and FF of the SHJ and the tandem devices.

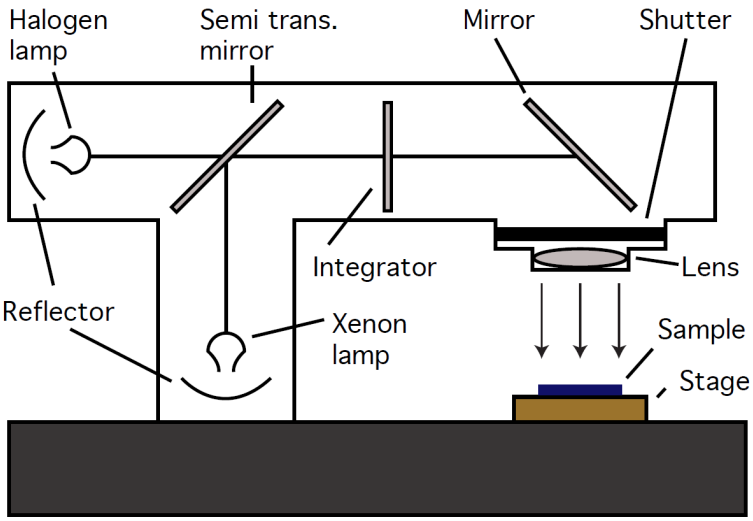


Figure 3.8: Schematic diagram of a AAA class Wacom WXS-156S-L2 solar simulator [20]

Figure 3.8 shows a schematic diagram of a AAA class Wacom WXS-156S-L2 solar simulator which was used for J-V measurements. Under illumination, the current density of the solar cells is measured as a function of the applied voltage. During the measurement, the solar cell is connected to a load in which the load is varied and the current produced is plotted. The measurements for the solar cells are performed under the standard test conditions of the AM1.5 spectrum, a power density of 1000 $W.m^{-2}$ and a temperature of 25 °C. Xenon and halogen light bulbs are used to stimulate the AM1.5 spectrum. The temperature of the measuring stage is temperature-controlled in which the solar cell is mounted.

3.3.5. Scanning electron microscope (SEM)

Scanning electron Microscope (SEM) is mainly used to investigate the surface textures. SEM can provide a precise qualitative analysis with a limited quantification of the surface morphology. It builds an image of a sample by scanning the surface with a focused beam of high energy electrons. The electrons interact with the atoms of the sample, generating various signals that reveals information about the surface topography. In this work, SEM XL-50 by Philips is used. SEM XL-50 microscopy uses acceleration voltages of 15 kV with a magnification up to 150K. The obtained images were generally taken from the cross-section of the tandem cell to visualize the quality the nc-Si:H bulk of the top cell which is grown on the textured c-Si layer of the SHJ bottom cell. The cross-section images of the tandem cell were taken with a tilt angle of 90°. In this work, the samples were broken by hand rather than polishing to minimize the damage of the texture profile.

4

Results and discussion

This chapter presents the obtained experimental results using the three developed texturing approaches (TA) which were earlier discussed in chapter 2. Using the characterization techniques which are explained in the previous section, firstly, a quantitative surface morphology analysis and the optical characterization of the textured c-Si wafers are presented for each TA at different etching times. Based on the quantitative surface morphology analysis , one c-Si wafer sample is chosen for each TA to process the SHJ and the tandem devices. Secondly, the results of applying different cleaning approaches (CA) on the textured wafers of TA1 are investigated. Later in this section, the J-V measurements of the SHJ and the tandem cells are illustrated. Finally, the cross-sectional images of the SHJ/nc-Si:H interface of the tandem cells for each TA are presented.

4.1. Surface morphology characterization

This section shows the resulting surface morphology of c-Si textured wafers for the three TA's at different etching times. In addition, the quantitative analysis for the textured samples are presented. Due to the lack of deposition time, only one c-Si wafer sample is chosen for each TA to process the SHJ and the tandem devices.

4.1.1. TA1

As aforementioned in the experimental setup for TA1, the c-Si wafers were anisotropically etched using TMAH alkaline etching. After 7 min of etching, sharp pyramidal structures of 2 μm in height are formed. Afterwards, diluted and undiluted HF:HNO_3 acidic mixtures with different concentrations were used to isotropically smoothen the large sharp V-shaped pyramidal structures into U-shaped valley structures. A range of diluted HF:HNO_3 mixtures were used to texture c-Si wafers for 10 s up to 1 min with a 10s-time step.

Applying these recipes resulted in etching away the pyramidal features of the c-Si textured wafers. As explained before in section 2.1.1, HF is the rate limiting factor for the oxidation-reduction reaction. High concentration of HF results into fast etching rate ,thereby faster smoothening of the textured features. The addition of CH_3COOH up to 70% barely affects the etching rate for HF:HNO_3 ratios of 50:50 and 80:20. Moreover, at HNO_3 rich regions, specifically for HF:HNO_3 ratio of 20:80, the effect of the diluent up to 70 was even not sufficient to lower the etch rate to the desired rate. For this reason, the undiluted HF:HNO_3 mixture with a ratio 1:70 was employed instead to smoothen the pyramidal features. Due to the low HF proportion in this acidic mixture, c-Si wafers were textured for longer etch time starting from 5 min up to 40 min with a 5 min time step. Figure 4.1 shows the surface morphology of the c-Si textured wafers for different etching time steps.

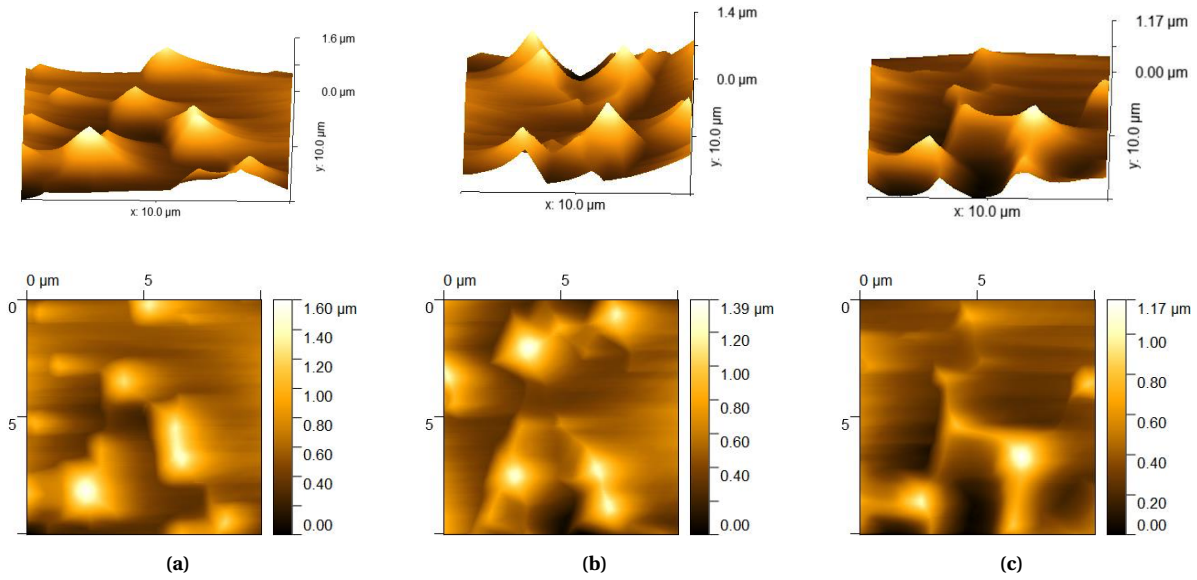


Figure 4.1: surface morphology of textured c-Si wafer using TA1 at etch time of a) 25min , b) 30min and c) 40min.

Table 4.1 shows the quantitative analysis for textured c-Si samples for different etching time steps. As the etch time increases for the textured samples, the height of the pyramidal structures decreases, the Rms surface roughness (σ_{rms}) of the microscopic peaks of the pyramidal structures decreases and the mean slope (S_M) of the pyramidal structures decreases. According to the statistical quantities and the visual inspection of the surface morphology of the textured samples at different etching times, it is concluded that Applying isotropic etching on the TMAH textured samples has met our expectation for etching the sharp pyramidal features into smoother pyramidal features with less steeper slopes. For this TA, samples with sharp pyramidal structures of 5 min etch time have an σ_{rms} of approximately 235 nm and S_M of 30°, while smoothened samples of 40 min etch time have an σ_{rms} of 159 nm and SM of 13 °.for this TA, an etch time of 30 min with an intermediate σ_{rms} of 201 nm with relatively less steeper pyramidal features (S_M =18 °) is chosen to texture the c-Si wafer of the SHJ bottom cell.

Table 4.1: AFM quantitative surface parameters for TA1

Statistical quantities	Etching time		
	25 min	30 min	40 min
Rms Surface roughness (nm)	217.63	200.92	158.53
Maximum height (µm)	1.60	1.39	1.17
Mean slope (°)	19.13	17.86	13.38

4.1.2. TA2

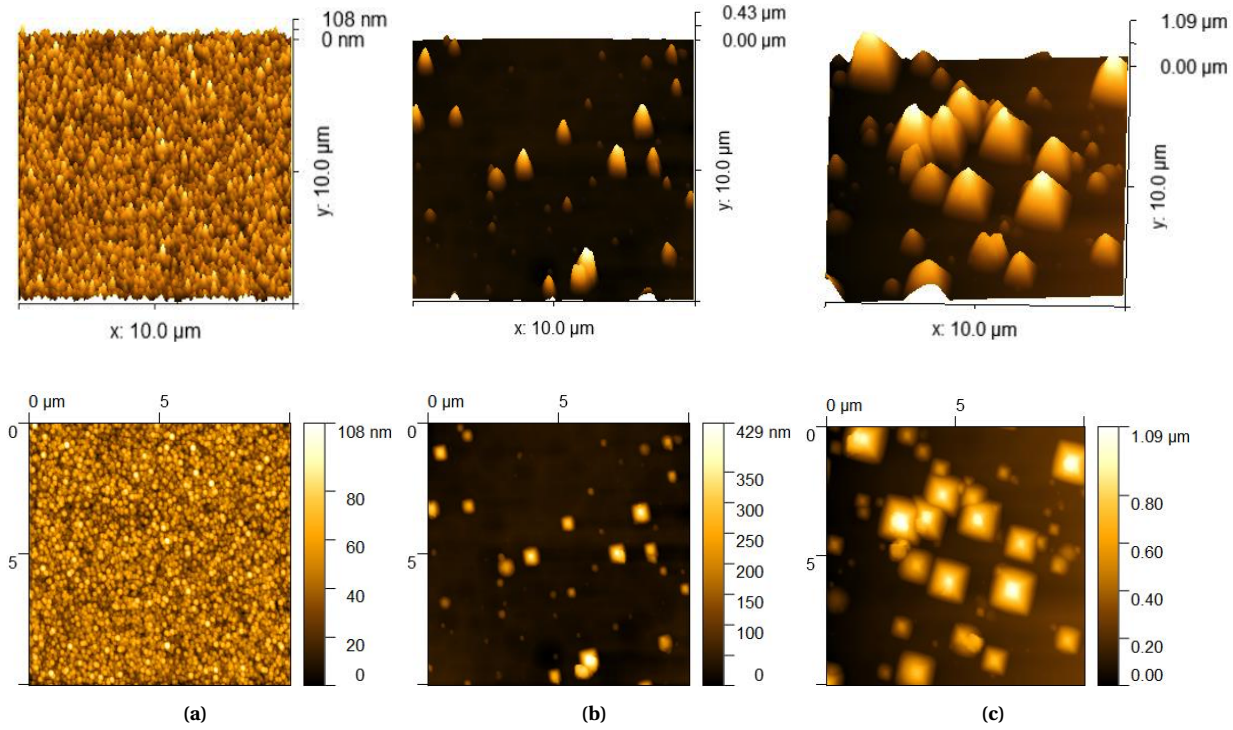


Figure 4.2: Surface morphology of textured c-Si wafer using TA2 at etch time of a) 30s , b) 60s and c) 120s.

In this texturing approach, c-Si wafers were anisotropically etched using an alkaline TMAH solution. Figure 4.2 shows the surface morphology of the c-Si samples for different etching times. The main purpose of this TA was to introduce surface roughness by forming small pyramidal features. The samples were textured for 30 s up to 2 min with a 30s-time step. Table 4.2 shows the quantitative analysis of these samples. During etching, sporadic nucleation of pyramids are formed in which the size of the pyramidal structures increases with time. As a result, the surface roughness and the mean slope of the pyramidal features both increase with the etching time. For this TA, an etch time of 60s is chosen to texture the c-Si wafer of the SHJ bottom cell. These textured samples have a σ_{rms} of 39.44 nm which is higher than the surface roughness of a flat c-Si lapped wafer of approximately of 17 nm and small pyramidal features with a height of 0.43µm.

Table 4.2: AFM quantitative surface parameters for TA2

Statistical quantities	Etching time		
	30 s	60 s	120 s
Rms Surface roughness (nm)	13.18	39.44	199.43
Maximum height (µm)	0.11	0.43	1.09
Mean slope (°)	11.18	14.21	18.71

4.1.3. TA3

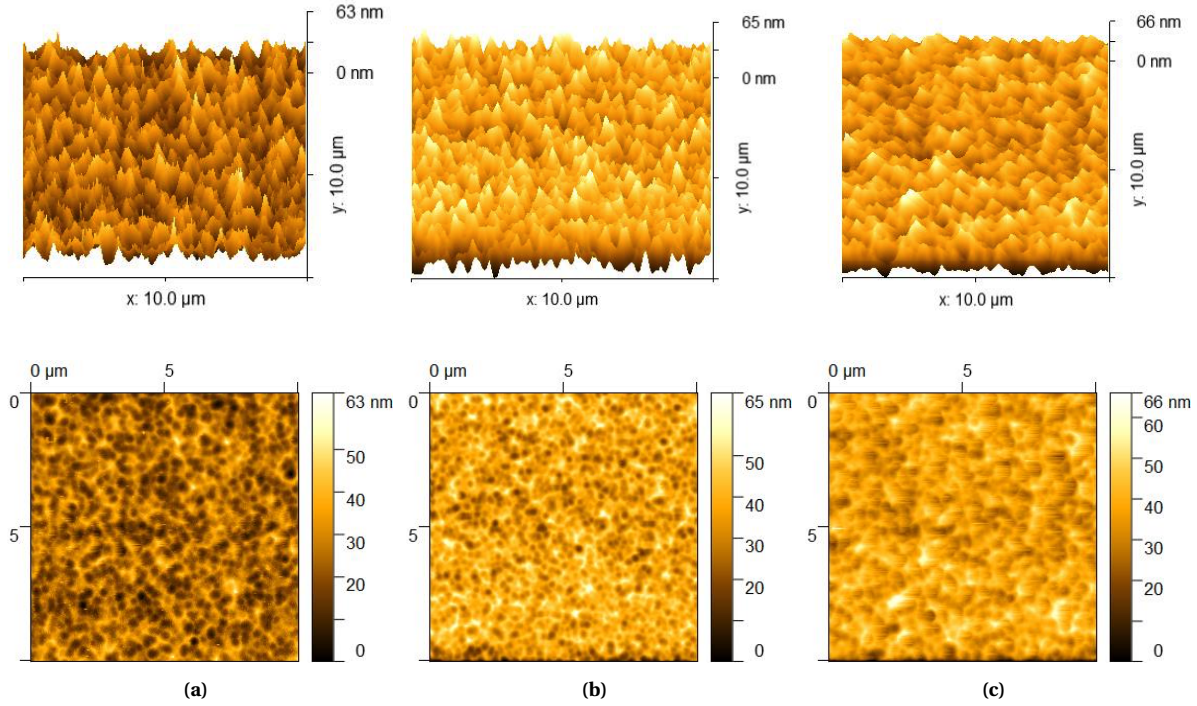


Figure 4.3: surface morphology of textured c-Si wafer using TA3 at etch time of a) 9min, b) 10min and c)12min

As previously discussed in section 2.1.3, a poly-Si layer is deposited on the c-Si wafers. For this TA, the poly Si/c-Si wafers were etched using HF:HNO3 acidic mixture with a ratio of 1:70. During the etching procedure, the samples were anisotropically etched due to the grain boundaries between the poly-Si layer and the c-Si surface. As shown in Figure 4.3, random nanoscale pit structures are formed at different etching times after the removal of the poly silicon layer. When the poly Si layer is completely etched, the surface of the c-Si samples is isotropically etched. As shown in table 4.3, at 9 min etch time, nano pit structures are formed with a σ_{rms} of approximately 7 nm. Further increase in the etching time up to 12 min leads to smoothening of the texture profile to a σ_{rms} of 6.61 nm due to the isotropic etching of c-Si wafer's surface. For this TA, an etch time of 9 min is chosen to texture the c-Si wafer of the SHJ bottom cell.

Table 4.3: AFM quantitative surface parameters for TA3

Statistical quantities	Etching time		
	9 min	10 min	12 min
Rms Surface roughness (nm)	7.09	7.45	6.61
Maximum height (nm)	63.2	65.1	65.9
Mean slope (°)	3.94	4.61	2.83

4.2. Optical characterization

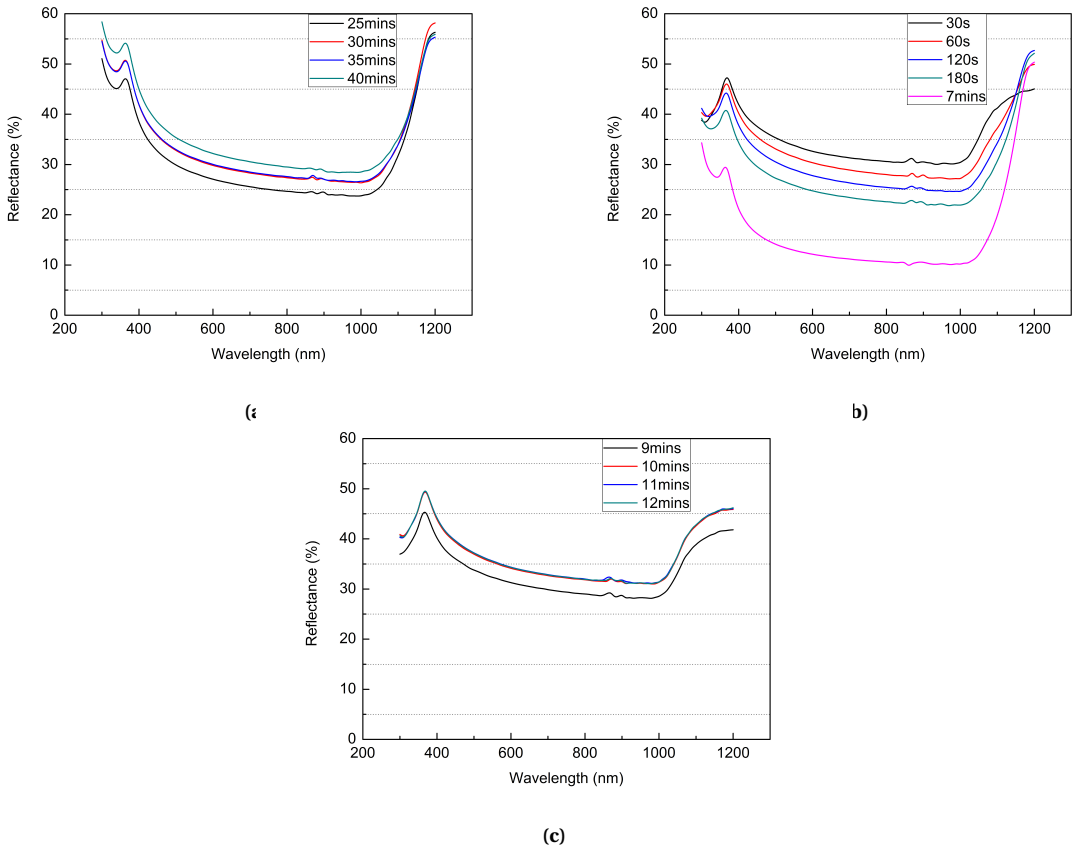


Figure 4.4: Reflectance measurements of textured c-Si wafers at different etching time for a)TA1 , b) TA2 and c)TA3

In this thesis work, the primary concern of texturing the c-Si wafers is to optimize a texture profile for better growth of the nc-Si:H on the the c-Si substrate. However, smoothening of the textured profiles increases the light reflectance and as a result, the delivered current of the solar cells is reduced which will lower the overall delivered power. For a flat polished c-Si wafer, the average reflectance is approximately 30% of the incident light in the visible spectrum [26], whereas, for the industrial standard fully textured sharp pyramids of 10µm in size, the average reflectance is lowered to 10% in the visible and the near infrared spectrum range[49]. Figure 4.4 illustrates the measured optical reflection of the textured c-Si wafers for the three TA's at different etching times. for TA1 , the reflectance of textured samples increases with the etching time as the steepness of the pyramidal features is reduced. For the etch time range of 25-40 min, the measured average reflectance increases with the etch time from 26.8% to 31.4%. Regarding TA2, the reflectance decreases with the etching time, reaching the lowest reflectance for the fully textured sharp pyramids at 7 min with an average reflectance of 12.7%. Finally, for TA3, at 9 min, after the removal of the poly Si layer, the reflectance is the lowest with a value of 31%. Longer etching time results in smoothening of the wafers and as a result, the reflectance increases to approximately 34%.

4.3. Surface passivation-life time measurement

After texturing the c-Si wafer of the SHJ bottom cell, 4 different cleaning approaches (CA) were employed to remove the native oxides and the surface contaminants. Regarding the CA, two wet cleaning methods namely nitric acid oxidization cycle (NAOC) and Radio corporation of America (RCA) were employed to clean the c-Si textured wafers using oxidation-reduction reactions. In addition, hydrogen plasma dry cleaning (HPDC) is investigated to clean the wafers by depositing an a-Si:H layer on both sides and etching the sacrificial layer by hydrogen plasma using Amigo PECVD cluster tool. In this section, the effect of the CA's is investigated by measuring the effective carrier lifetime (τ_{eff}) of the c-Si textured wafers. Due to the time constraints, the

four CA's were only tested on TA1 samples. After the cleaning treatment of the TA1 textured wafers, an a-Si:H layer of 10 nm is deposited on both sides to passivate the textured features of the c-Si wafers. Afterwards, the samples were annealed to improve surface passivation by thermal relaxation as it relieves the strain due to the lattice mismatch between the c-Si/a-Si:H interface [50]. However, annealing at high temperature for prolonged time can damage the grown a-Si:H layer. For each CA, the annealing time and temperature were optimized and are illustrated in Appendix A. Figure 4.5 shows the effect of annealing temperature on the τ_{eff}. The τ_{eff} is measured with excess minority carrier density at injection level of 10×10^{15} cm^{-3}.

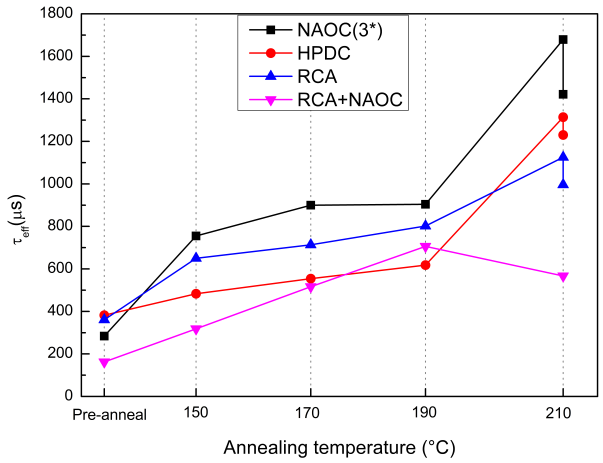


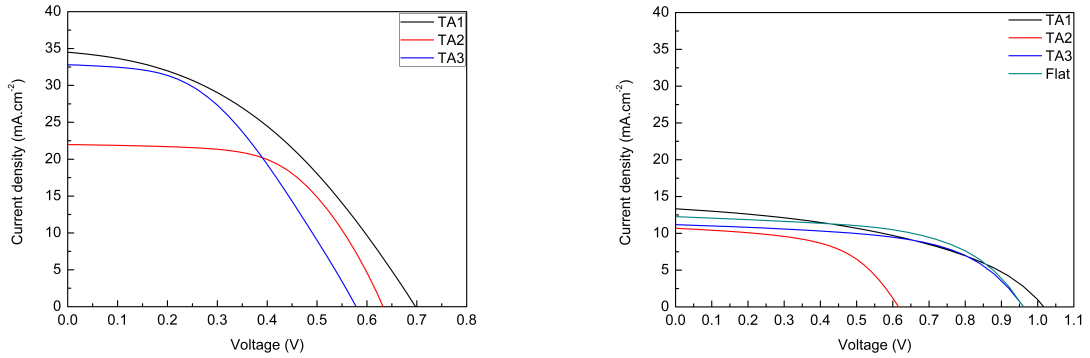
Figure 4.5: Carrier Lifetime measurement for c-Si wafer using TA1 (30min) for different cleaning approaches

As shown in Figure 4.5, annealing had a significant effect on τ_{eff} for all CA's. In the Pre-anneal stage, the measured τ_{eff} ranged between 162 µs for (RCA+NAOC) up to 382 µs for HPDC. After annealing, the measured τeff was tripled and quadrupled at the optimized annealing time and temperature until failure in which the τ_{eff} starts to deteriorate for all CA's. Regarding the Wet CA's, applying NAOC(3*) provided the best surface passivation for the TA1 sample with an τ_{eff} of 1679 µs. For the dry cleaning method, a relatively high τ_{eff} was obtained for HPDC with a τ_{eff} of 1314 µs. Applying HPDC for 3 and 5 cycles resulted in a damaged surface with poor τ_{eff} of 33 µs. It's suggested that the poor τ_{eff} of applying HPDC for multiple cycles might be due to the multiple ion bombardment of the hydrogen plasma which increases the defect density of the surface. Another reason of this damage could be due to the difficulties of matching the a-Si growth rate and the etching rate of the hydrogen plasma. Based on this CA's investigation, NAOC(3*) is chosen for cleaning the c-Si wafers for TA2 and TA3.

4.4. J-V characterization

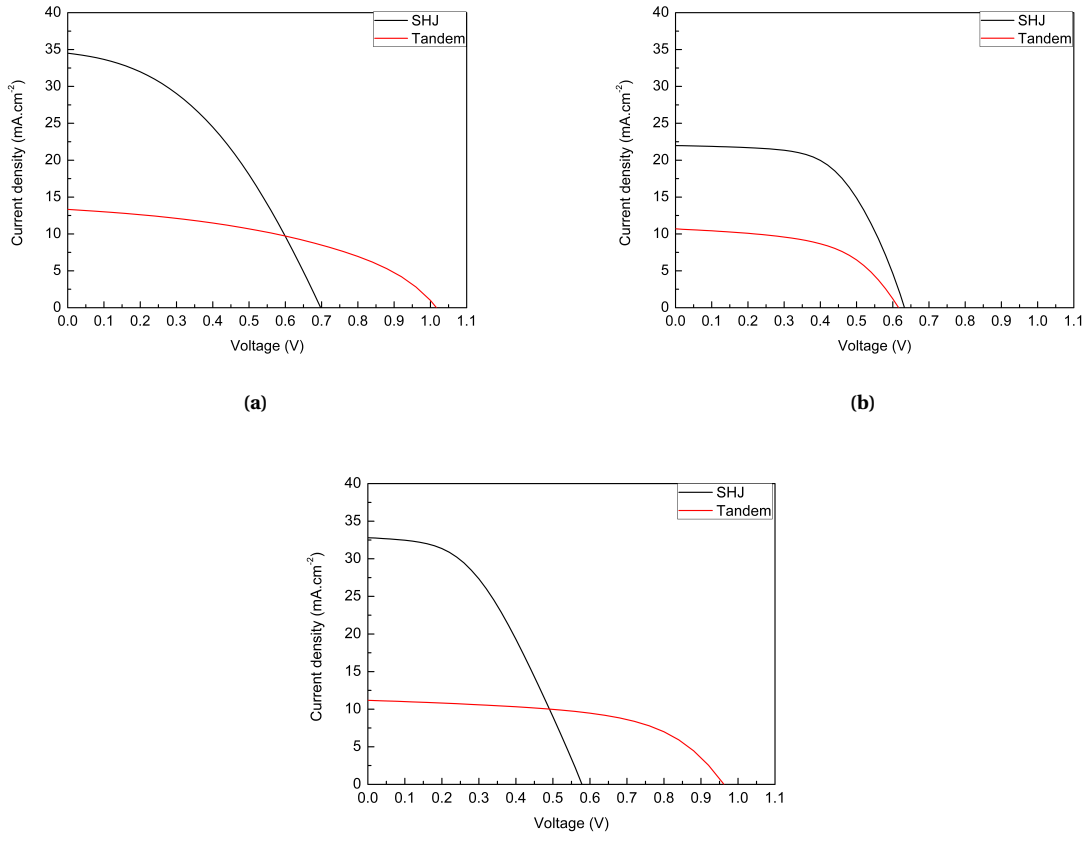
After the cleaning treatment of the textured c-Si wafers for the three TA's, SHJ and tandem devices were fabricated using the processing tools discussed earlier in section3.2. Using the Wacom solar simulator, the performance of the SHJ and the tandem cells were determined. Figure 4.6 and 4.7 show the J-V characteristics of the fabricated devices.

According to the J-V measurement of the SHJ cells, it can be concluded the electrical behavior is texture dependent. It is observed that the smoothened pyramidal features of TA1 textured wafer is well passivated in which ,high V_{oc} of 0.69 V and FF of 0.5 is obtained. For TA2, the few small random pyramids (low pyramidal coverage) of the c-Si wafer were likely not passivated properly. This might be due to the poor quality of the c-Si/a-Si interface since the a-Si growth quality is reported to be texture dependent [51]. While for TA3, textured wafers with nano pit structures have slightly lower V_{oc} and FF of 0.578 V and 0.43 respectively.



(a) **(b)**

Figure 4.6: J-V measurements for a) SHJ and b) tandem devices for all texturing approaches



(a) **(b)**

(c)

Figure 4.7: J-V measurements for SHJ and tandem devices using a) TA1 , b) TA2 and c) TA3

According to Figure 4.6b) and Figure 4.7,TA1 tandem cell is the best performing fabricated cell with a measured V_{oc} of 1.02 V, J_{sc} of 13.34 mA.cm^{-2} and FF of 0.44. high delivered J_{sc} is attributed to better optical utilization of the texture profile of TA1 tandem device. For TA2, TRJ didn't work well for the tandem cell where the V_{oc} obtained for tandem cell is <0.65 V with a FF of 0.54. While for TA3 tandem cell, a V_{oc} of 0.962 V and FF 0.56 is obtained which is likely comparable to the FF and the V_{oc} of the flat tandem cell. As mentioned before in section 2.2.3, in this work, the tandem cells were processed using two single junctions for SHJ bottom cell and nc-Si:H top cell for all TA. Due the time constraints, the TRJ for fabricated tandem devices were not

optimized. It is believed that Improving the TRJ will further lower the voltage losses and enhance the FF of the tandem cells for all TA's. It is suggested that the defect density in the nc-Si:H bulk could be still a dominant factor that influence the overall delivered voltage of the tandem devices. High defect density will increase the recombination rate of the generated charge carriers and thereby, the delivered Voc is lowered. The main goal of this thesis work was to develop a texturing approach to facilitate better growth quality of nc-Si:H bulk on the c-Si substrate. As aforementioned, nc-Si:H does not grow uniformly on flat c-Si wafer due to internal stresses accompanied by poor adhesion to a flat substrate. On the other hand, growth of nc-Si:H on sharp and steep pyramidal structures results in cracks in the grown nc-Si:H bulk. In this work, different TA's were developed to facilitate better growth nc-Si:H on c-Si substrate. Figure 4.8 visualizes the cross section of c-Si/nc-Si:H interface for the fabricated tandem devices using the developed TA.

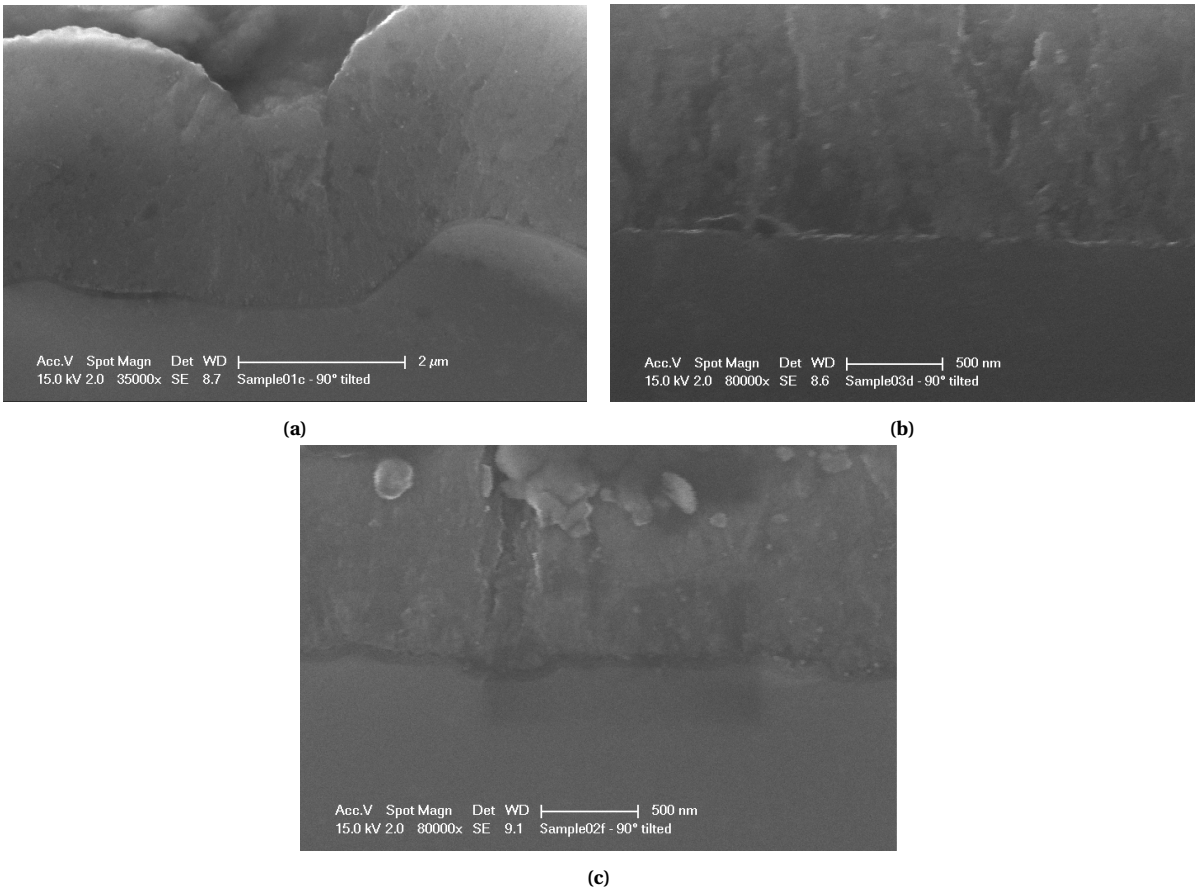


Figure 4.8: SEM cross-section image of the (c-Si/nc-Si:H) interface at 90 ° tilt of the tandem cells using a) TA1, b)TA2 and c)TA3

It can be concluded that nc-Si:H was successfully grown on the c-Si surface for all TA. Regarding TA1, it is observed that smoothening of the large sharp pyramidal features into U-shaped valleys results in a better growth of nc-Si:H bulk material on the c-Si textured wafer without significant cracks[1]. On the other hand, concerning TA2 and TA3, there were no visible defects observed in the c-Si nc-Si:H interface as the nc-Si:H top cell was grown nearly on a flat surface morphology of the c-Si wafer in the SHJ bottom cell.

[1] More SEM images are provided in Appendix B

5

Conclusions and Recommendations

In this thesis work, various aspects regarding the fabrication of nc-Si:H/SHJ tandem cells have been discussed. Different texturing approaches (TA) were developed to facilitate better growth of nc-Si:H on SHJ c-Si based cells. Subsequently, the effect of different cleaning approaches (CA) on improving the surface passivation of the c-Si wafers is discussed. Finally, the J-V measurements for the tandem cell and the cross section of nc-Si:H/SHJ interface for all TA's were presented. This chapter concludes the most important findings for this thesis and gives recommendations for future research work.

5.1. Conclusions

After applying the three different texturing approaches on the c-Si wafers of the SHJ bottom cell, it's concluded that smoothening of the sharp pyramidal structures of the standard alkaline etching results in a promising nc-Si:H/SHJ interface with a better grown nc-Si:H layer. for this TA, a V_{oc} of 1.02 V, J_{sc} of 13.34 mA.cm^{-2} and FF of 0.44 is obtained for the nc-Si:H/SHJ tandem cell. For TA2, anisotropic etching for short time of 60s resulted in low coverage of small pyramidal structures. It is suggested to investigate nc-Si:H/SHJ interface for longer etch time of 90s. For TA3, the smoothness of nanoscale pit structures of the textured wafers resulted in the same J-V measurements as for the flat tandem cell.

Cleaning the c-Si textured wafers before thin films deposition is an essential step in removing the native oxide layer and particulate surface impurities which reduces the V_{oc} and the FF. Different cleaning approaches (CA) were investigated for the textured wafers of TA1. The efficiency of the CA's was analyzed by measuring the minority carrier effective lifetime (τ_{eff}) of the c-Si/a-Si:H passivated wafers. The oxidation of HNO_3 and the subsequent stripping of the formed oxide provided the best passivation for the textured c-Si/a-Si:H wafers in comparison to all other CA's.

According to the cross-section SEM images for nc-Si:H/SHJ interface using TA1, it is concluded that smoothing of the sharp V- Shaped pyramidal structures into U shaped valleys resulted in promising nc-Si:H/SHJ interface with no significant cracks. It successfully facilitated the growth of nc-Si:H on top of SHJ bottom cell and hence, promising Voc and FF can be obtained for the future optimized nc-Si:H/SHJ tandem devices.

5.2. Recommendations

In this thesis work, due to time constrains, it was not possible to optimize all aspects regarding the fabrication of the nc-Si:H/SHJ novel tandem device. The following recommendations can be applied for further research work.

- Fabrication of nc-Si:H/SHJ tandem device using TA1 for different etching time in the range of 25-40min. The variety of the fabricated nc-Si:H/SHJ interfaces will show the trend of the growth quality of the nc-Si:H top cell with the surface roughness and the steepness of the texture profile of the c-Si wafer of the SHJ bottom cell.

- Hydrogen plasma dry cleaning (HPDC) might be a future good candidate for cleaning the textured wafers in comparison to the wet cleaning methods. The main advantage of using this method is that

the thin film layers of the SHJ bottom cell can be deposited using AMIGO PVMD cluster tool without a vacuum break. Further Optimization of the deposition a-Si:H sacrificial layer and the plasma etching parameters is required.

- Optimization of the Deposition parameters of the PECVD for Thin film layers of the nc-Si:H/SHJ tandem device is required [51, 52]. It can further improve TF layers growth quality of the nc-Si:H thin film layers on the textured c-Si wafer of the bottom cell.

For this thesis work , standard recipes for the SHJ bottom cell and nc-Si:H top cell were used to fabricate the nc-Si:H/SHJ tandem devices. Therefore, there is still a wide room to further improve the external parameters of the various interfaces of the tandem device. It is expected that optimization of the TRJ intermediate layer will improve the charge carrier flow between the top and bottom cell and hence, it will further enhance the overall performance of the tandem cell.

A

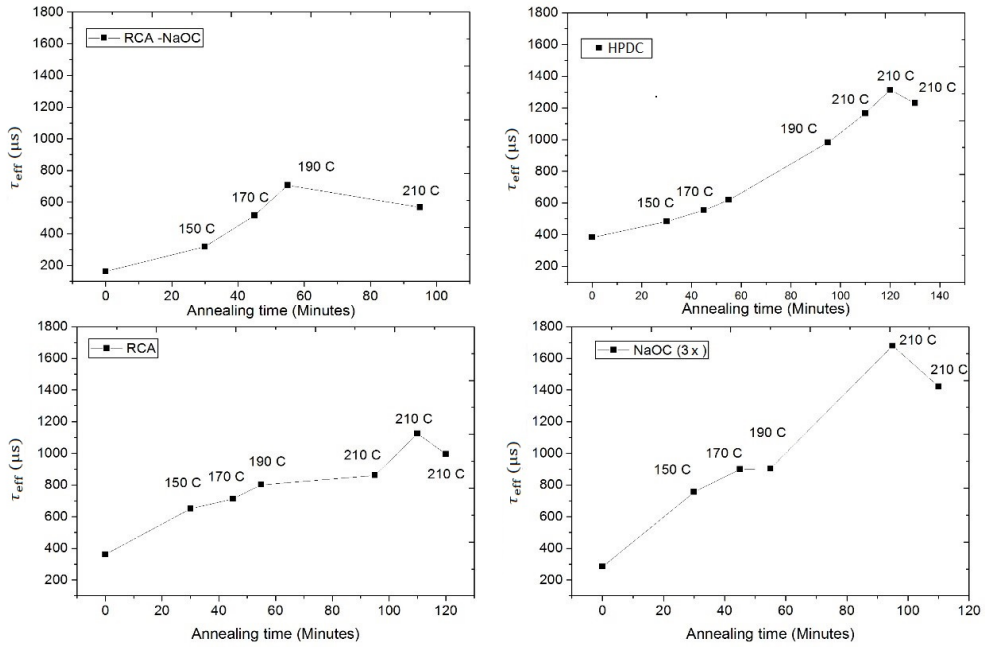


Figure A.1: Optimization of the annealing time and temperature of the carrier lifetime measurement for the TA1 (30 min) samples after applying different cleaning approaches

B

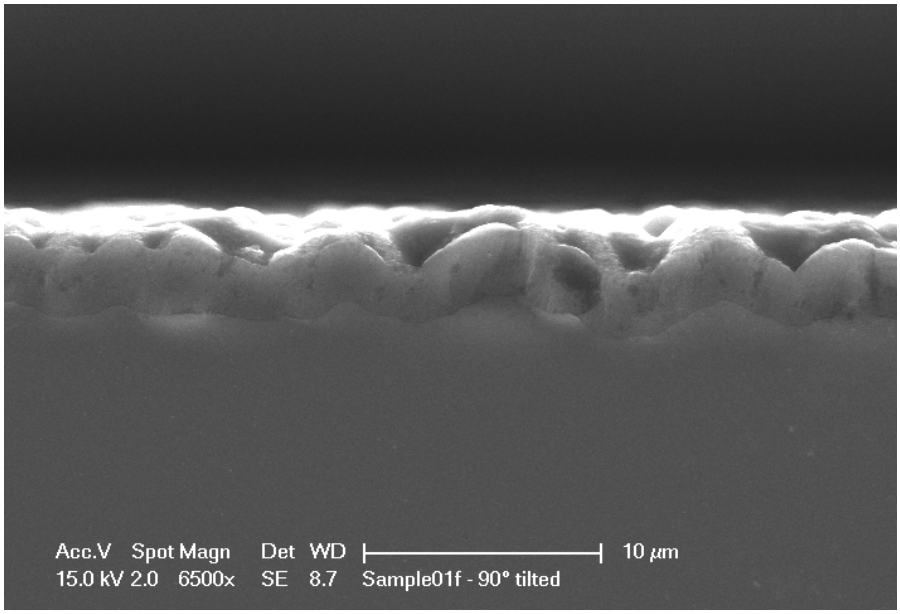

Acc.V Spot Magn Det WD 10 µm
15.0 kV 2.0 6500x SE 8.7 Sample01f - 90° tilted

Figure B.1

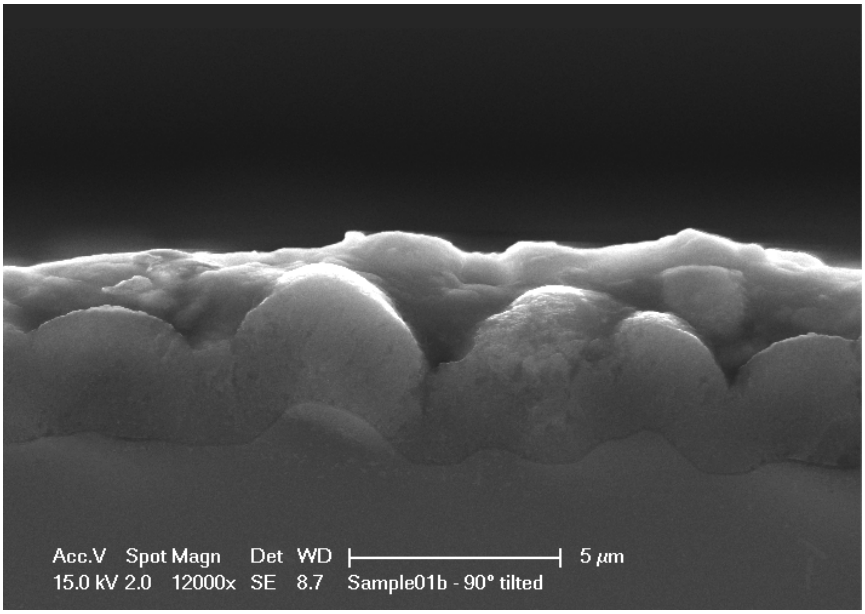


Figure B.2

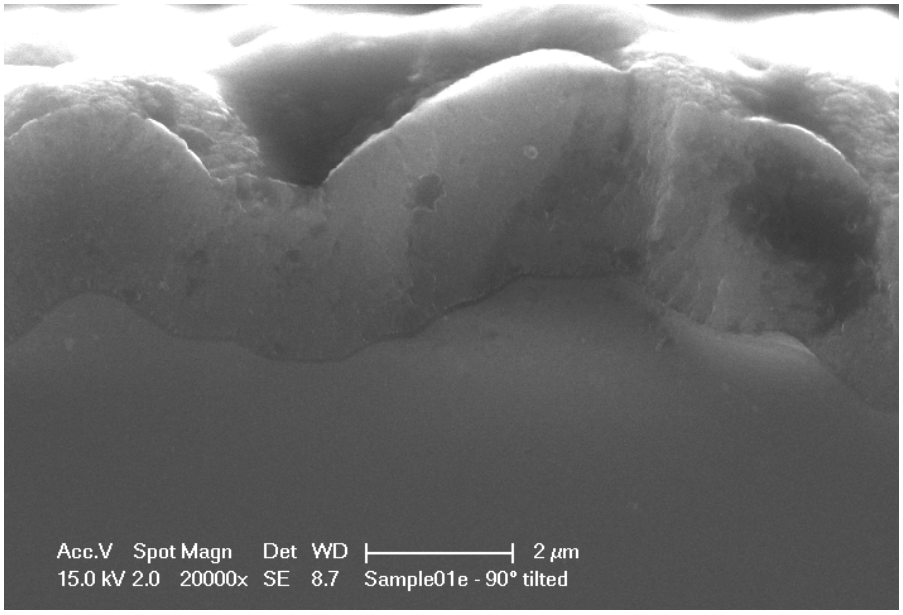


Figure B.3

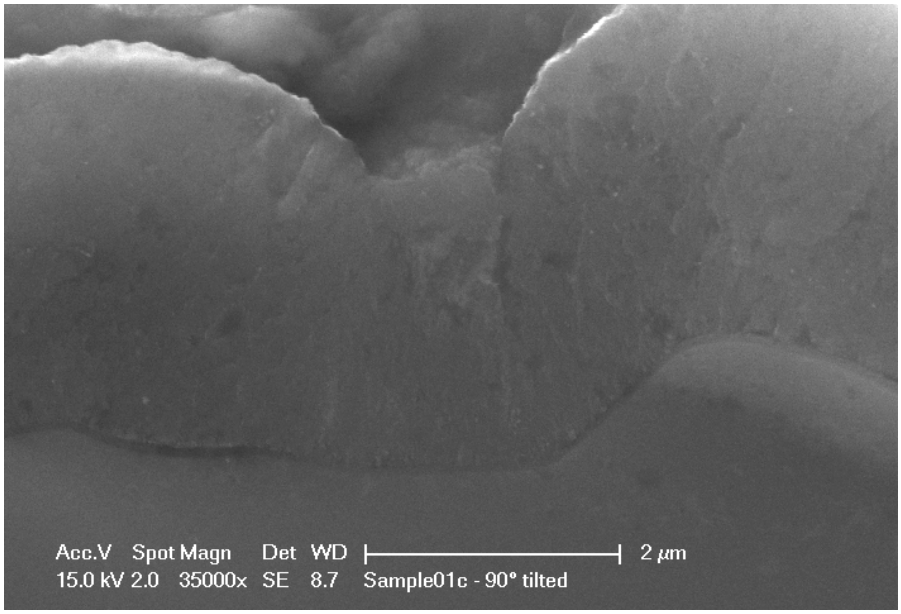

Acc.V Spot Magn Det WD 2 μm
15.0 kV 2.0 35000x SE 8.7 Sample01c - 90° tilted

Figure B.4

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