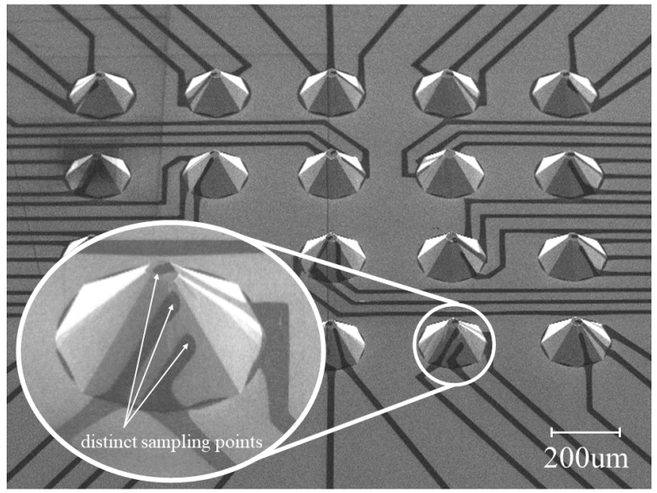

Master Thesis

A 3D microelectrode array to record neural activity at different tissue depths

T.M. de Rijk, MSc.

Measuring neuronal responses along all three spatial dimensions is the next step, beyond the capacity of established 2D microelectrode arrays (MEAs), to record electric activity inside tissues with highly accurate spatial resolution. We present silicon-based planar arrays of 3D microelectrodes, whereby each microelectrode supports multiple, independent and vertically stacked TiN sampling points. The microarrays were manufactured by wafer-scale micromachining and assembled onto PCBs conforming to MEA readout standards.

T.M. de Rijk, MSc.
Delft 15-05-2020

TU Delft

A 3D microelectrode array to record neural activity at different tissue depths

by

T. M. de Rijk, MSc.

to obtain the second degree of Master of Science
at the Delft University of Technology.
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Track:	Microelectronics
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Abstract

Measuring neuronal responses along all three spatial dimensions is the next step, beyond the capacity of established 2D microelectrode arrays (MEAs), to record electric activity inside tissues with highly accurate spatial resolution. This research presents silicon-based planar arrays of 3D microelectrodes, whereby each microelectrode supports multiple, independent and vertically stacked TiN sampling points. The microarrays were manufactured by wafer-scale micromachining which can be assembled onto PCBs conforming to MEA readout standards.

The study entails multiple fabrication processes in order to find the most promising recipe for manufacturing arrays of truncated pyramids. Results show clear differences between alkaline etching solutions (KOH and TMAH) and the effects of surfactants. Material properties and corner compensation techniques allow for precise control over the final shape of the truncated pyramid structures which are used as a base for the electrodes. Sidewall lithography techniques are investigated and results are shown to prove the viability of patterning high resolution spatial details on 3D structures.

Final microelectrode arrays were fabricated on 4" Si wafers. The truncated micro-pyramids were obtained by timed anisotropic wet etching (25% TMAH + Triton) solution of the Si substrate using lithographically defined hard masks that allowed precise selection of crystallographic directions. After thermal growth of a 270 nm-thick SiO2 passivation layer, a 40 nm/200 nm-thick Ti/TiN layer was sputtered and lithographically patterned to define the electrically independent electrodes. On each pyramid, vertically stacked and distinct sampling points were defined at the tip of each electrode by lithographic patterning of a thin oxide passivation layer. The smallest metal tracks patterned on the slanted facets were 15 um-wide with minimal inter-track gap of 5 um. By virtue of these innovative 3D MEAs biologists expect to be able to measure responses of 3D neuronal networks from hiPSC-derived cortical neurons cultured within biogel matrices or as brain organoids.

Preface

This thesis is part of the Master Graduation Project for the Master Electrical Engineering at the TU Delft. A three month literature study was conducted before this work and its relevant parts are included in this thesis. The two year curriculum ME-EE Microelectronics consists out of 60 ECTS; one full year of specialist courses, with a 60 ECTS Thesis Graduation project, consisting out of a literature study and this thesis. All parts have to be successfully finished before one can finish the master program.

A research proposal was defined by dr. M. Mastrangeli from the Technical University Delft. The project is in collaboration with the Leiden University Medical Center and Erasmus MC in Rotterdam. The project consists of designing and manufacturing, in the EKL cleanroom of TU Delft, a 3D neuronal microelectrode array that could be directly implemented in current MEA structures for reading out the responses of neuron clusters. An additional feature of being able to measure the responses on three different height levels was defined from the medical universities. This thesis focuses on two major developing challenges:

Manufacturing small truncated (<10um top base sizes) pyramid structures with a height between 80 to 100um in a dense matrix formation.

Sidewall lithography: Patterning titanium nitride interconnect on the slopes of the earlier constructed micro-structures

I want to express my gratitude to Dr. M. Mastrangeli for giving me the possibility to do my master thesis within the ECTM group, and providing me with guidance, feedback and help throughout this project. The freedom given to me in this project gave me the chance to work on my own schedule and pursue my interests, resulting in a great working atmosphere. Special thanks goes out to Prof. dr. P.M. Sarro, with whom I could brainstorm ideas and discuss plans and results. Another thanks goes to Henk van Zeijl for all his ideas, tips and reticle design help. All EKL staff was extremely friendly and helpful in and around the cleanroom, with a special note to Robert Verhoeven, Johannes van Wingerden, Hitham Mahmoud. All named (and not specifically included) colleagues, friends and staff gave insight and motivation to end this one-year project successful.

T.M. de Rijk, MSc.
Delft, May 2020

Contents

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List of abbreviations

CP	Conductive Polymer.
CZ wafer	Czochralski wafer.
DRIE	Deep Reactive Ion Etching.
FZ wafer	Float-zone wafer.
IPA	Isopropyl alcohol.
iPSC	Induced Pluripotent Stem Cells.
KOH	potassium hydroxide.
MEA	Microelectrode Array.
MEMS	Micro-ElectroMechanical Systems.
MP	Micropyramidal.
MPS	Microphysiological system.
MSI	Multi-Step Imaging.
MTF	Muscular Thin Film.
OoC	Organ-on-Chip.
PCB	Printed Circuit Board.
PDMS	Polydimethylsiloxane.
RIE	Reactive Ion Etching.
SEM	Scanning Electrom Microscope.
TMAH	Tetramethylammonium hydroxide.

1 Organ-on-Chip

1.1. The need for more accurate biological models

Humans are able to grow and replicate countless cells and diseases in petri dishes, enabling to study drug efficacy, disease progression and much more. However, current *in vitro* 2D cell cultures fail to mimic the 3D microenvironment and other key cell functions. It appears that cell-cell interactions differ greatly between patients and 2D cell cultures [60]. Several other often mentioned differences are surface topography, surface stiffness, mechanical loading and biochemical composition [15] [23].
Similar to animal studies, 2D biological models often do not fully represent the human physiology and its response. Clinical trials often fail due to the lack of proper models and methods for detecting adverse reactions early on [24] [39].

Current methods for cell culturing lack crucial functions to keep the cells alive and healthy. Some examples are insufficient perfusion of nutrients [73], failure to maintain differentiation and expression of tissue-specific functions, and mechanical stimulation. An important aspect is the need for a model to recreate the active tissue-tissue interface. Mechanical microfluidic devices (Organ on Chip, OoC) can mimic this tissue-tissue interfaces and expand on the capabilities of current cell cultures and animal models [24] [40] [75].

Animal tissues and physiology are not very representative for modeling the human physiology responses. Just like that human tumor-derived cell lines,(e.g. Hela line), are also not representative for normal healthy tissue [11]. This is partly due to the fact that these cell lines are extremely resilient, hard to kill, and not an accurate model when subtle cell responses are wished to be modeled. It has been reported that over 11.5 million animals per year are used for experiments in the EU alone. The largest contributors to this are the industry for fundamental biological research and human medicine [39].

The costs for developing new drugs has been rising steadily over the last decades. In the early 1970's, on average, a newly successful released drug cost about 179 million dollars. This number increased exponentially to the 2.6 billion dollars in the year 2012 (see Figure 1.1) [39] [40]. It roughly takes 12.5 years to develop and FDA approve a new drug, and the number of approved drugs has kept dropping in the last decades [14] [40]. Figure 1.2 shows a typical drug development process for all stages. Researchers start with a large amount of different compounds and mixtures for a drug. After numerous testing stages, the number of compounds decreases. Unfortunately, in vitro testing gives poor predictions of the drug responses. And animal testing is often obligatory, which makes the testing phase even more expensive [11] [33].
The failure rates of clinical trials clearly indicate the need for more physiologically relevant human models. The clinical and animal trials are often one of the most expensive phases for the companies, with relatively high fail rates [40]. Reported clinical trial failure rates from the FDA are 48-64% for phase 1, 29-31% for phase 2, and 60-67% for phase 3 [39]. The prime contributors of failing the clinical trials are damaging drug responses on cardiac muscle and liver toxicity [39]. These numbers clearly show the need for better models to test the effects of drugs in the early stages. Current animal models are often a poor representative to indicate possible effects in humans [40].

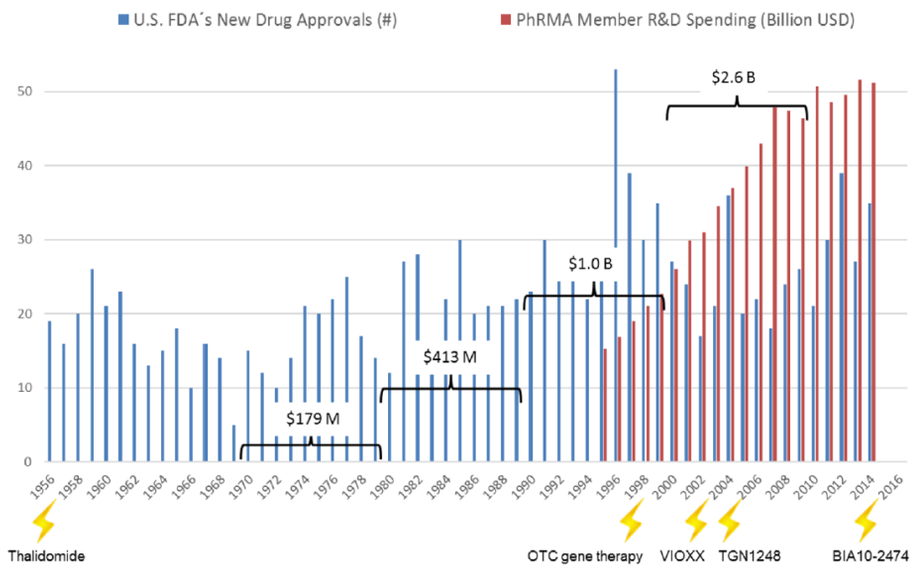


Figure 1.1: Number of drugs approved in the US by the FDA and the corresponding costs. The lightning bolts indicate drug or substance failures which resulted in human harm. Image reproduced from Marx et al. (2016) page 73 [39].

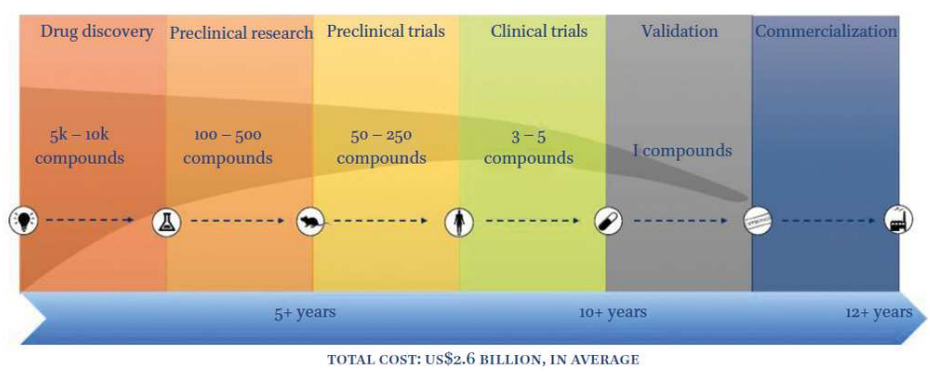


Figure 1.2: Typical drug development process. Image reproduced from Clerk et al. (2017) page 1 [11].

Another disadvantage of current models is the fact that they are not patient specific. Models are often grown from animal cells, where patient specific responses cannot be tested very accurately. Each patient reacts different, for which current methods cannot differentiate for. Nowadays, the drugs are administered to the patients in the hospitals without exactly knowing whether medicine is actually working properly and efficient. Some people do not react or have an adverse reaction to the drugs, which then will only worsen their condition. OoC devices could help improve this situation by mimicking the human body on a series of lab-on-chips that can show the individual response of a drug on different organs without actually administrating the drugs to the patient.

A summary of the advantages of the Organ-on-Chip technologies over the current standards of cell culturing is given below [11] [24] [39] [40] [75]:

- The use of human cells in contrast to often used animal cells can give a more precise and accurate model.
- Connect multiple organs together.
- Ability for long-term cultures (oxygen/nutrients perfusion). To investigate long term exposure or repeated drug exposure effects.

- Provide mechanical and/ or electrical stimulation with active MEMS structures to mimic the cells natural environment, for example heart or lung cells. The primary cells taken from humans are effectively immature. The cells need to age and 'exercise' to become a good representation of the organs they represent.
- Provide a platform for testing patient specific drug responses on multiple organs. The drug response can be tested on the organs but outside the human body. Cells from the patient can be taken and grown on the multiple OoC devices, on which the drugs can be tested.
- Drug developments become more efficient due to the fact that early trials can be performed to detect any adverse and or toxic effects on human tissues. The clinical trials normally take a long time and often result in adverse effects, resetting the whole development phase.

1.2. From single cell cultures to Organs-on-Chip

The development of cell culturing has been steadily increasing during the last decades. Each improvement tries to act and improve on the limitations of its previous generation. This process is shown in Figure 1.3.

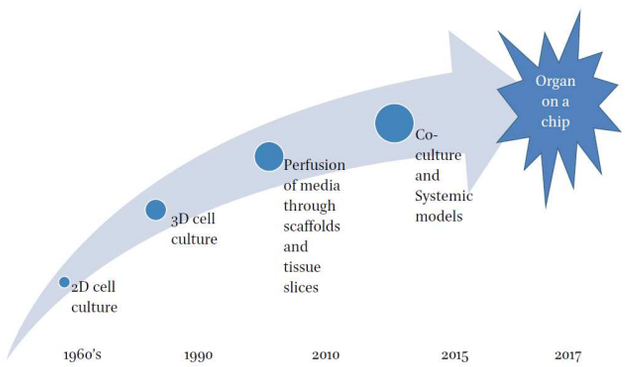


Figure 1.3: Timeline of different cell culture developments. Image reproduced from Wilkinson et al. (2019) page 1 [73].

Petri dish cell cultures have one side touching the base wall (often glass or plastic from the petri dish), and the other side in contact with the media. Therefore, cell-to-cell interaction is highly limited [73]. The cells are often grown in a different environment than they are supposed to (their native environment). The cells are not regularly perfused with oxygen and/or nutrients as they are in healthy tissue. There is no communication between other organ cells (metabolic signaling between tissues [73]) and the mechanical and electrical stimulation is absent [39]. All these factor play a role in as to why current cell cultures and models do not yield the expected results when developing new drugs. The third dimension in cell culturing proved to be extremely useful as 3D tissues are much closer to the human physiology. This gives an advantage when performing toxicity tests or drug discovery [46]. 3D cell cultures use a (soft or rigid) structure, for example a scaffold, to enable cells to grow in a 3D fashion. However, one large disadvantage is that when cells cluster together, they can become necrotic in the absence of perfusing vessels [73].
To mimic the environment of human physiology, more reliable data can be acquired from cells that exhibit the same behavior and do not differentiate between the environment on the so-called lab-on-a-chip and their human organ.
To properly formulate the goal of the Organ-on-Chip (OoC) research initiative, the following definition was formulated by Mastrangeli et al. [40]:

A fit-for-purpose microfluidic device, containing living engineered organ substructures in a controlled micro environment, that recapitulated one or more aspects of the organ's dynamic functionality and (patho)physiological response in vivo under real-time monitoring.

To simplify this definition into a more easily understandable concept, the goal for OoC is:

To simulate the body, outside the body.

1.3. What is Organ-on-Chip?

The name Organ-on-Chip amplifies the main purpose of this research field. It tries to recreate a system (human body) with multiple sub-systems (organs) in a laboratory setting where these sub-systems can be individually monitored, connected and stimulated. The so-called ' organs' are microfluidic cell culture systems that recapitulate the structure, function, physiology and pathology of living humans [53]. The reader should be reminded that this does not imply actual organs are placed in these microfluidic devices. Clustered cells are used that can grow and inhibit organ intrinsic properties like pulsating heart muscle, or gas exchange through different cell layers like in the human lungs.

The following sub-sections briefly show some of the largest and well-known OoC target organs and can give the reader a general feeling on how these cultured 'organs' currently look like. An overview of an extensive *Human-on-Chip* is shown in Figure 1.4, which clearly shows the general goal of replicating the major organs and their connections.

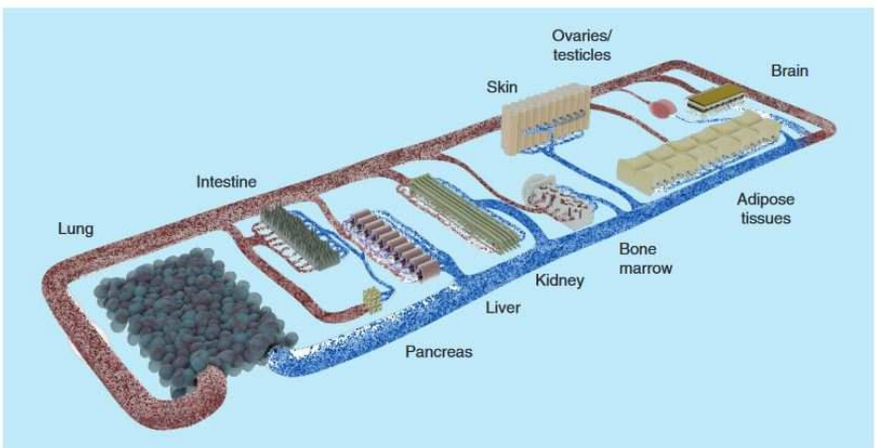


Figure 1.4: Human(-body)-on-Chip concept consisting out several major organs and their interconnect. Image reproduced from Dehne et al. (2017) page 12 [13].

1.3.1. Lung-on-Chip

It is estimated that more than one million people suffer from Pulmonary thrombosis in the United States, with more than 100.000 to 200.000 of these fatal [63]. However, as of now there is no effective *in vitro* model available that simulates the thrombi formation in human lung microvessels [25]. The so-called alveolus-on-chip can be a first step in modeling the alveolar epithelium and endothelium interface. This OoC can, in contrast to ordinary animal models, try to mimic the altered hemostasis and complexity of human lungs [25] [69].

The proposed device features two parallel rectangular microchannels separated by a flexible PDMS membrane coated with extracellular matrix [25]. The bottom part was covered in human umbilical vascular endothelial cells (HUVECs). The function of these cells was to create a micro-vessel that prevents the contact of blood to its surrounding. The top part was lined with primary human alveolar epithelial cells. This method successfully recreated the alveolar-capillary interface [25]. The process is depicted schematically (and simplified) in Figure 1.5.

Another research project from D. Huh et al. in 2010 showed by a similar method the possibility to recreate the alveolar-capillary interface of the human lung. This OoC device was able to reproduce integrated organ-level responses to bacteria and inflammatory cytokines [24]. The method of thinking of this project seems very similar to the earlier discussed method from A. Jain et al. [25]. However, the major difference is the addition of pulmonary movement caused by adding the two side chambers. The device consists out of three main parallel compartments, with the alveolar-capillary interface in the middle. Continuously changing the pressure in the outer chambers mimics the movement of the lungs, and stretching the cells/tissue (just like in normal human lungs). The designs are shown in Figure 1.6.

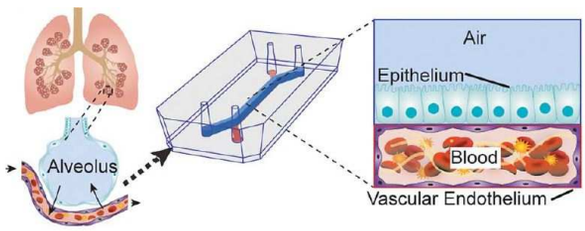


Figure 1.5: Concept design of a Lung on Chip device. Image reproduced from Jain et al. (2018) page 1 [25].

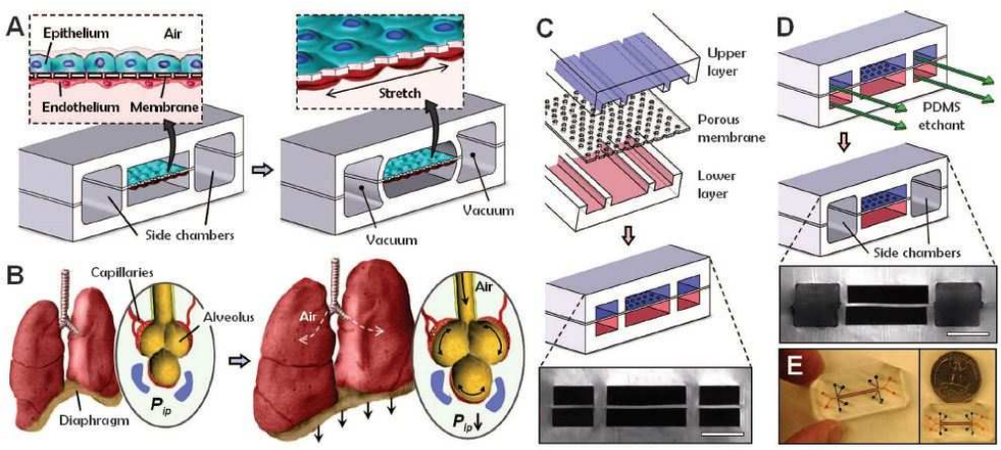


Figure 1.6: Concept design of a Lung on Chip device with pulmonary movement. Image reproduced from Huh et al. (2010) page 2 [24].

1.3.2. Heart-on-Chip

The heart muscle is a complex system that maintains homeostasis in the human body. Experts have been trying for years to mimic the cardiac tissue interface for drug discovery or tissue regeneration applications [1] [79]. However, it is difficult to measure both contractility and electrophysiology [22]. Recent studies show that cardiac cells may behave differently when in small or large complex anisotropic structures [22]. This means that current models fail to accuratetly describe the human heart muscle interface due to the fact that the single monolayers propagate the action potentials and contractile stresses differently than *in vivo*.
A major advantage of heart-on-chip systems is the ability to create personalized *in vitro* heart models instead of the less accurate animal models [79]. However, it is challenging to create functional heart tissue due to the fact that mature cardiomyocytes exhibit limited proliferation potential [79], meaning the cells are not able to recover from certain damage like other cell organs can. Due to the lack of accurate models for the human heart, lots of new drugs fail clinical trials or even at earlier stages of drug development. It is said that almost half of the cardiac drugs fail due to safety issues directly related to inaccurate testing models [79].

Current models often use simple 2D cultures without any mechanical stimulation or proper microfluidic flow to let the cells feel as 'close to home' as possible. Realistic (Heart-on-Chip) models with integrated microfluidic vasculature structures can greatly increase the effectiveness of models and help improving the testing phases of new drugs. When using embryonic stem cells, the mechanical motion and shear stress can 'exercise' the cells and promote maturation [79]. These models would be patient specific and not generic models, which would make them even more valuable and suitable for personalized medicine.
A study from 2007 showed that single cell studies or isotropic monolayers cell studies of cardiac myocytes are not representative and accurate models for toxicology studies [27]. Anisotropic layers of cardiac cells mimic more closely the response of *in vivo* heart muscle. 2D bilaminate cardiac cells were constructed (out of anisotropic tissue from heart muscle cells [22]) and the contractile stresses were measured by the Muscular Thin Film (MTF) [1]. The muscular film was cultured on a deformable film which enabled free movement of the cells. The MTF chip was placed in an aluminum well which allowed additional optical readout of contractility of the tissue. The entire device was manufactured as a microfluidic device. Results showed diastole and systole peaks and revealed free contraction by external applied stimulation. This method allowed for measuring contractile responses to cardiac drugs and *in vitro* drugs testing studies [1].

1.3.3. Brain-on-Chip

The brain is an enormous complex machine that is key to our life as we know it. Before explaining the reader the concept of Brain-on-Chip, it is worth producing a notable quote from Paul Allen and Francis Collins [57]:

Neuroscience today is like chemistry before the periodic table: People knew about elements and compounds but lacked a systematic theory to classify their knowledge.

It is estimated that the human brain consists out of 85 billion neurons, 100 trillion synapses, and 100 chemical neurotransmitters [2] [57]. Deciphering the vast complexity of the human brain and being able to monitor certain reactions and responses could be a major advantage for detecting, preventing and even curing diseases. Current models lack the predictability for drug efficacy and are not a full representation of the human brain [46]. Microphysiological systems (MPS) can improve current 2D models and combine different cell types in 3D configurations and simulate complete brain functions [46]. Drug responses, toxicology effects and medicines can all potentially be tested on these MPS systems and decreasing the number of failed clinical trials.
2D monolayers cannot mimic the complex cell-to-cell interactions within the neurite networks. Advances have been made by using 2D co-cultures compared to cultures with a single cell type [46]. However, 3D systems are more likely to mimic the complex cell-to-cell behavior, differentiation and interaction even better. Human embryonic stem cells became a powerful tool for growing cell cultures. However, due to the ethical issues, other methods were explored and found to obtain cells pluripotent stem cells (iPSC) from adult humans, eliminating the ethical concerns. Small differences are reported between Embryonic stem cell (ECS) and iPSCs, however the impact on cell developments are still unknown [46]. The iPSCs can be differentiated into neuronal and glial cells, which can be used for MPS models. A simplified schematic overview of a proposed Brain-on-Chip is shown in Figure 1.7. The somatic cells can be extracted from a patient and reprogrammed to HiPSC cells. These cells grow and differentiate into neuronal and glial cells that form the MPS system. After this step, interaction and monitoring of the MPS system is possible.

This report will continue with the Brain-on-Chip and start evaluating different electrodes fabrications. Different types of electrodes exist, and this research focuses specifically on the fabrication of microelectrodes.

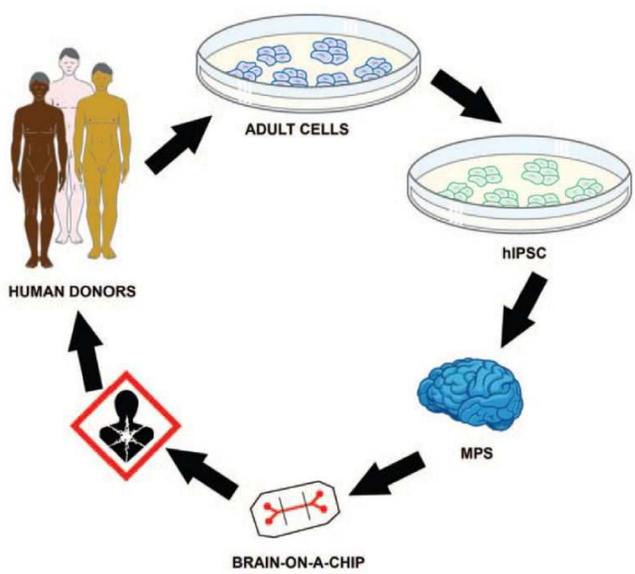


Figure 1.7: Simplified Schematic overview of proposed Brain-on-Chip diagnostic loop.
Image reproduced from Pamies et al. (2014) page 21 [46].

1.4. Current 2D and 3D neuronal recordings

Neurons are the nerve cells that transmit and relay signals in the body. The largest concentration of neurons is located in the central nervous system of the body. A large misconception is that neurons are only located in the brain [48]. It is estimated that 100 billion neurons are interconnected in the human brain that allows us to function as we are [38]. A schematic representation of a 'typical neuron' is shown in Figure 1.8. For this research project it is important to find structures that are suitable for cells/neurons to grow on. Materials should be biocompatible and sharp edges that can puncture the neurons membrane should be avoided for extracellular measurement setups (except for juxtacellular recordings). Intracellular measurements will be performed inside the cell, where the membrane has to be punctured. Therefore, neuron measurement setups can be classified in two different techniques: extracellular and intracellular.
This project will focus on the fabrication for extracellular microelectrodes. This technique targets a group/network of neurons (extracellular) with the goal of tracking and recording, in 3D, the signal propagation/communication between neurons.

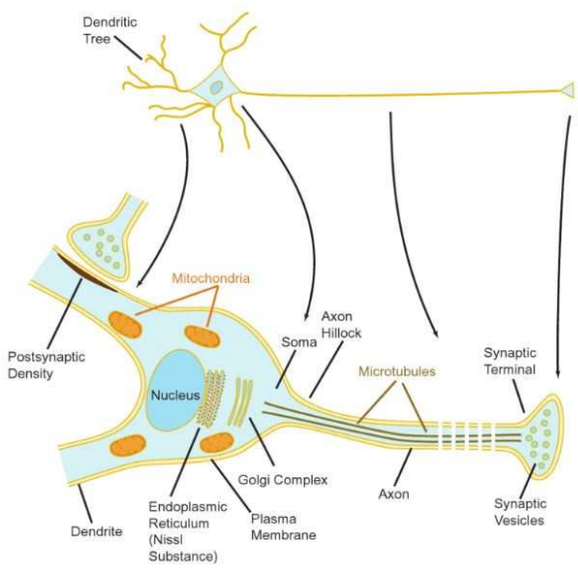


Figure 1.8: General neuron structure.
Image reproduced from "The neuron: cell and molecular biology" (2015) [38].

Microelectrode arrays (MEA)

The designed system will be compatible with current MEA (from Multi Channel Systems [64]) standards to ensure proper read-out possibilities. The maximum number of output connections is therefore limited to 60 (or possibly 120), which limits the number of electrodes (especially if each structure has multiple conductive electrodes). Future designs could utilize active multiplexing of signals to increase the number of electrodes. For now, the MEA device already enables for higher throughput, parallel and low cost cell measurements, in contrast to other methods like the patch clamp system [65].

1.5. Current 3D electrodes

My first master thesis dealt with the fabrication of a flexible epiretinal implant to help restore the vision of visually impaired people. The structure was constructed from a flexible silicon chip with 3D-microelectrodes and a flexible transparent thin polyimide film. To continue to design and fabricate 3D microelectrodes for brain tissue is a challenging next step.

The disadvantage normally is that, when increasing the number of electrodes in a certain area, the 2D electrodes become smaller and concurrently their electrode impedance increases due to this area reduction. This increase in impedance naturally decreases the injection current amplitude of the electrodes [8] [29]. To overcome this problem, a switch to 3D microelectrodes, where the surface area is increased, can lead to a new era

1

of stimulating microelectrodes. With the LIGA process a resist (for example PMMA) is exposed by an X-ray source and can develop structures with an aspect ratio over 50 with heights up to 1 mm [71]. However, this process utilizes an expensive synchrotron source (electromagnetic radiation emitted from a charged particle moving at almost the speed of light [20]), which enforces the reason for a cheaper UV based resist like SU-8 [71].

Therefore, this research will focus on the fabrication of 3D microelectrodes using UV lithography and will show proof-of-concept designs for this. The main purpose for this chapter is to research possible fabrication methods for 3D microelectrodes that can be later be upgraded to measuring neuronal responses on different heights.

The upcoming sub-sections show several methods for creating (high-aspect-ratio) microelectrodes. Several materials, processes and shapes are mentioned to indicate the possibilities and ' outside of the box thinking' to create certain less common structures.

Mushroom-shaped microelectrodes for intracellular neuron recordings

Instead of puncturing the neurons for intracellular recordings, a so-called mushroom shaped electrode was fabricated by [44]. The cell engulfs the structure (or multiple) and the gold covered electrodes can record its signals. Different small mushroom shapes (between 1 and 5 um) were fabricated and engulfed by the neurons. A conductive gold (gMuPs) layer was deposited over the electrodes. A Scanning Electron Microscope (SEM) image of the gold mushroom-shaped electrodes is shown in Figure 1.9 and Figure 1.10 shows a hippocampal neuron engulfing the structure.

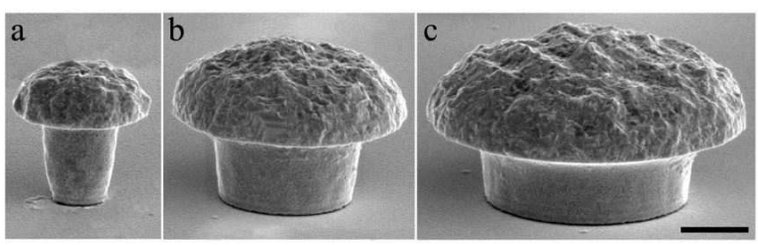


Figure 1.9: Gold covered mushroom shaped electrodes with different sizes.
Image reproduced from Ojovan et al. (2015) page 3 [44].

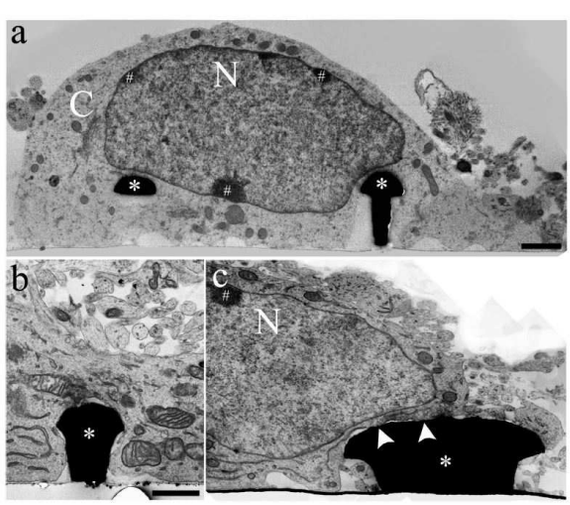


Figure 1.10: Hippocampal neuron engulfing a mushroom shaped electrode.
Image reproduced from Ojovan et al. (2015) page 4 [44].

32-site fork-like electrode array

In 2002, a study showed a fabrication method for creating a 32-site recording electrode array [43]. The long sharp fork-like structures were made horizontally on wafers and formed by double-side DRIE etching with silicon oxide as an etch stop layer. The results showed an electrode impedance of 1 MΩ at 1 KHz, which is similar to other neurophysiological recordings according to [43]. This method for creating electrodes with multiple conducting paths circumvents the need for sidewall lithography but it is not compatible for a 2D array of 3D electrodes suitable for the MEA device.

Electrode impedance reduction for higher SNR recordings

Another paper from 2010 [56] showed a 25-fold reduction of the electrode impedance to 30kΩ, stating that low impedance provides a superior SNR for detecting neural activity. Some materials mentioned to improve the electrode impedance are titanium nitride, porous silicon or other conductive polymers. Platinum black electrode coatings are also used but they lack deposition reproducibility and durability [56]. Seker et al. 2010 proposed nanoporous gold (np-Au) as a new approach for creating a conductive coating on electrodes to improve its impedance.

Neural and retinal sharp tipped electrodes

A study from R. Bhandari et al. 2007 [3] showed a fabrication process for neural and retinal prostheses with sharp tipped electrodes. A thick wafer (2mm) was diced with various depths and filled with glass as an isolation layer. After removing the backside of the wafer, the sharp tips were created by wet isotropic etching in HF 49% + HNO3 69% solution. After deposition of a conductive material for the electrodes, the array was encapsulated with Parylene-C. An interesting method for deinsulating the electrode tips after the Parylene-C deposition is spin-coating the photoresist everywhere and freeing the tips with RIE etching in oxygen plasma [3].

3D arrowhead-shaped microelectrodes

This method proposed to Deep Reactive Iron Etch (DRIE) deep cylindrical 'tunnels' in a regular silicon wafer and stop at a predetermined depth. Due to the crystal structure of silicon and the selectivity of wet etching to different crystal orientations, a triangular tip can be created with anisotropic wet etching. After this, the complete chamber is filled with gold using standard Ti/Au electroplating method which was discussed in detail in my first thesis [12]. After spin coating and patterning a polyimide layer and backside DRIE for removing the substrate, the gold electrodes were created on the optically transparent polyimide. Figure 1.11 shows the fabrication process.

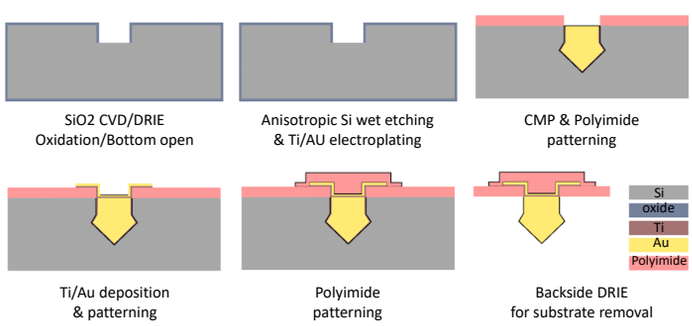


Figure 1.11: Fabrication process of the arrowhead microelectrodes [36].

One aspect that has to be taken into account is the so-called microloading effect or the RIE lag [29]. When using DRIE to etch long bars in the silicon, by decreasing the openings of the bars, the etch rate decreases. Therefore, the height of the arrowhead shape can be determined by the width of the opening. The smaller the opening, the smaller the height of the tip. For clarification, this is graphically shown in Figure 1.12.
The paper from Koo, Kyo-in, et al. [29] uses alkaline wet etching to open up the bare silicon and reveal a negative arrowhead. The subsequent steps follow the same method of thinking, and an example of the results is shown in Figure 1.13.

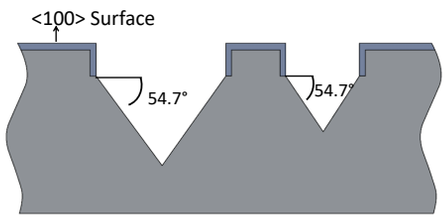


Figure 1.12: The DRIE opening determines the arrowhead height.

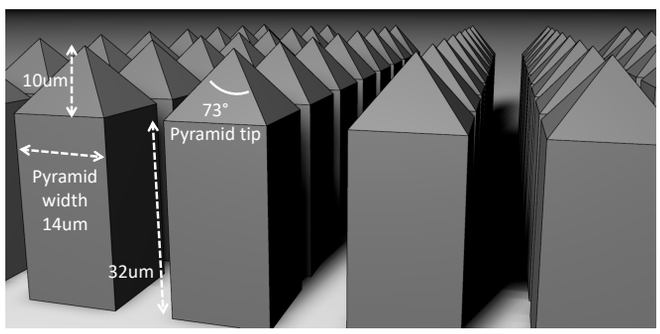


Figure 1.13: Sketch of fabricated arrowhead micro-electrode arrays, with DRIE and wet etching.

Conducting Polymer 3D microelectrodes

The paper from Sasso et al. [54] mentions the need for high signal-to-noise 3D microelectrodes is large due to the fact that currently most planar electrodes measure neuronal responses up to only 0.5 mV. In contrast to the 60-100 mV intracellular responses, this is extremely low. Key advantages for 3D microelectrodes, compared to 2D, are listed below.

- The 3D electrodes can penetrate the neurons and achieve higher signal levels, increasing SNR.
- The 3D electrodes can penetrate the first dead cells of a cell culture.
- Even when not penetrating the cells, a higher SNR can be achieved due to the fact that the surface area is increased, which translates directly to a lower impedance.

High aspect ratio pillars can be fabricated using several methods, including dry etching. However, a problem arises when these pillars need to be electrically active. A metallic layer can be deposited using several methods like electrochemical deposition, e-beam evaporation and sputtering. Unfortunately, these methods are unable to cover the complete vertical sidewalls of the high aspect ratio pillars with metal. The angle of incidence of the metal ions is too narrow to reach the bottom of the vertical sides [54]. It was found that around the range of 70 um pillars, the sputtering methods were unable to deposited a uniform layer of conductive material over the vertical structure, isolating the microelectrode. This is shown in Figure 1.14.
To overcome this problem, the metalisation step was replaced by a conductive polymer (CP) deposition to guarantee the conductivity of the electrodes to its substrate. The process steps are shown in Figure 1.15, which clearly shows the ability to ensure the electrode electrical conductivity to its base.

Mechanically sawed microelectrodes

An interesting technique already proposed in 1992 by [26] showed that pillars can be easily sawed in the silicon wafer, after which the damages could be removed (and the thickness of the pillars could be regulated) by acid etching. This method showed the possibility to develop high aspect ratio pillars with smooth surfaces, using a controversial but relatively simple method. The two process steps are shown in Figure 1.16.

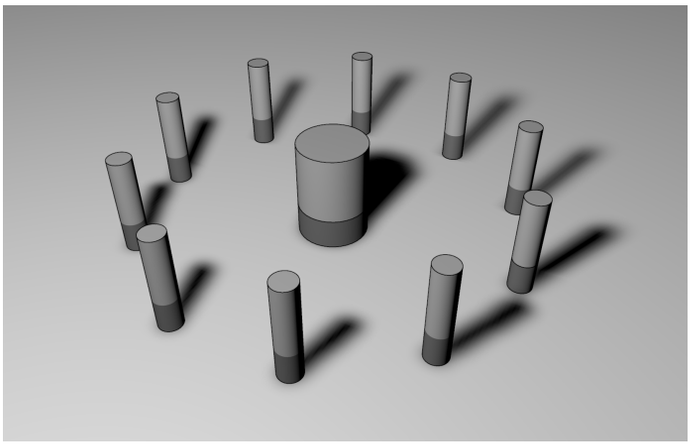


Figure 1.14: Sketch showing the effect of sputtering high aspect ratio structures.

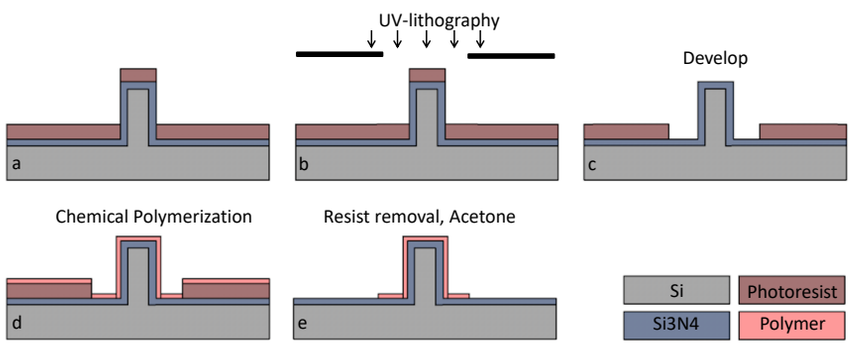


Figure 1.15: Process flow for depositing a conductive polymer (CP) over high aspect ratio pillars [54].

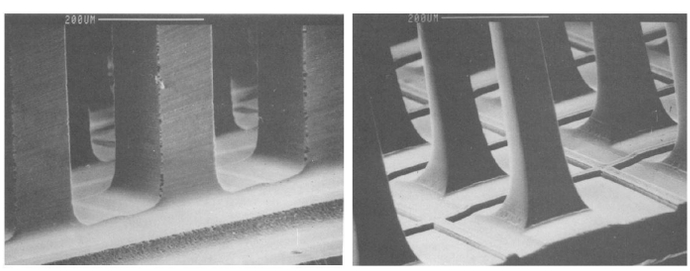


Figure 1.16: SEM image from sawed silicon high aspect ratio pillars. Left: Before etching. Right: After acid etching. Image reproduced from Jones et al. (1992) page 5 [26].

Backside UV exposure SU-8 electrodes

This research study focuses on fabricating pillars as high as 100 um. To realize this, thick resist profiles are needed which give rise to several difficulties. UV exposure becomes more difficult when exposing thicker resist layer. The effective dose along the layer thickness is different, resulting in smaller exposed area at the bottom and larger at the top [34]. Figure 1.17 shows how to use this property to an advantage and create cone-shaped high aspect ratio electrodes from SU-8. By spincoating a thick layer of SU-8 on a transparent substrate like glass, and then applying a select layer of SU-8, the pillars can be manufactured. Due to the fact that the UV dose (through the backside of the wafer) decreases slowly when going deeper into the polymer, the bottom parts can be under-exposed. When developing the structures, the pillars with inclined vertical sidewalls remain.

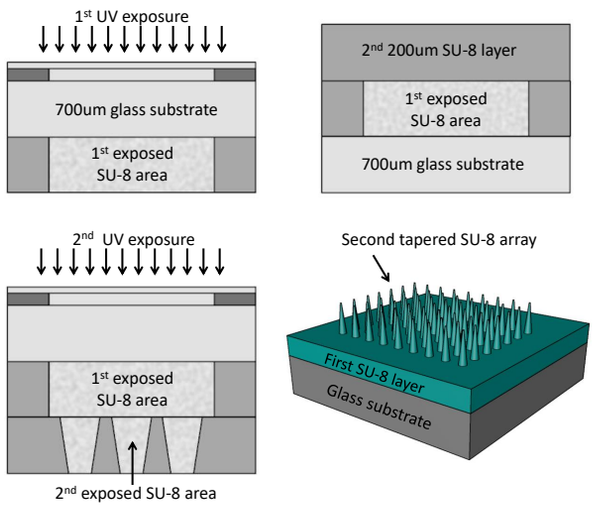


Figure 1.17: Process steps to create cone-shape electrodes by back-side UV lithography.

Extremely high aspect ratio microneedles

A brief technique worth mentioning due to the fact that it utilizes a completely different approach to create high aspect ratio needles is so-called SU-8 drawing lithography [34] [35] [74].
An array of stainless steel pillars were fabricated and placed into contact with soft-baked SU-8. After contact was initiated, the pillars were pulled back in the opposite direction and the polymer stretched out of plane, following the stainless steel pillars up to a length of 3200 um. The pulling rate and temperature are key factors for controlling the so-called 'drawing'. The microneedles can be processed further with regular IC process steps. In this case the pillars were electroplated with Ni and the SU-8 was removed by curing and hollow ultra-high metallic hollow microneedles remained [35].

KOH etched electrode array

When high aspect ratio structures (and steep slopes) are not necessary, it is possible to use anisotropic etching for fabricating the electrodes. Due to the selectivity of certain wet etchants to silicon crystal orientations (see Chapter 2.8), 3D MEMS structures can easily be fabricated (or in other crystalline materials). Due to the higher density, the ⟨111⟩ crystal plane is attacked much slower then the other planes, resulting in numerous possibilities for creating 3D structures [37]. However, all angles and slopes are fixed due to the crystal orientation of silicon. The speed of the etching process is highly depended on the concentration of the etchant and the temperature, as can be seen in Figure 1.18. Where as dry etching mainly gives vertical sidewalls, wet etching can be used to create a whole different variety of structures. This technique, where the structures are fabricated using KOH/TMAH etching, will be taken further in the following Chapters, where the sidewalls are patterned, providing the first step of fabricating multi-level electrodes on a single truncated pyramid.

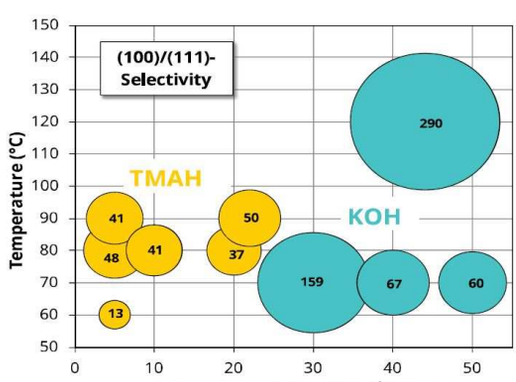


Figure 1.18: Wet etching rates. Image reproduced from Microchemicals (2019) [42].

1.6. Research Proposal

This master thesis will focus on the fabrication of 3D microelectrodes, which can be used for Organ-on-Chip applications. The research proposal is given as:

Development of three-dimensional microelectrodes able to sample electric tissue activity at multiple, distinct and vertically resolved points.

Multiple different types of alkaline etching solutions and concentrations/temperatures are experimented with to find the most suitable structure characteristics. Corner compensation methods are investigated and intensively tested and evaluated to find the most promising procedure and repeatable construction of 3D micro-electrode arrays. The two major parts of this thesis are mentioned below:

[1] Manufacturing small truncated (<10um top base sizes) pyramid structures with a height between 80 to 100um in a dense matrix formation. Silicon crystal properties and corner compensation methods are used to create convex angled pyramid structures with different slope angles.

[2] Sidewall lithography: Patterning aluminum pads and titanium nitride interconnect on the slopes of the earlier constructed micro-structures.

A general overview of how the ideal fabrication process will look like is given in Figure 1.19 on the next page. This should give the reader a more clearer picture of what the end result should look like before the in-depth fabrication processes are explained.

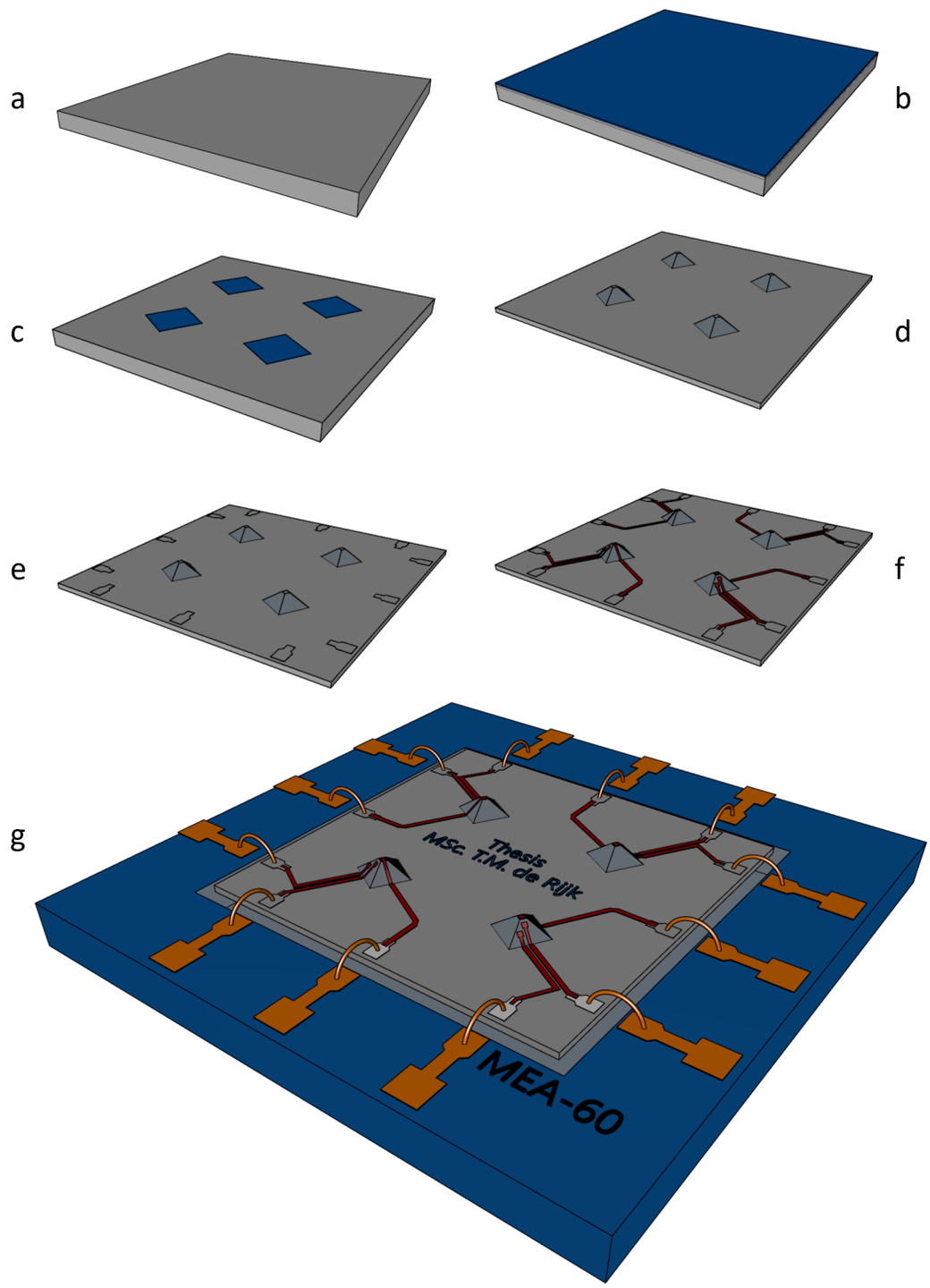


Figure 1.19: Sketch of proposed 3D electrode fabrication process. (a) silicon (100) wafer. (b) SiN hard mask. (c) Etched masks. (d) etched truncated pyramids. (e) Aluminium pads. (f) TiN interconnect. (g) PCB design and wire-bonding.

2 Monocrystalline silicon etching

Mono-crystalline silicon is the base material for almost all integrated circuits and technology. The crystal orientation of the silicon is indicated by the Miller indices *hkl*. This thesis will handle the following convention:

- (hkl): wafer orientation
- ⟨hkl⟩: crystal orientation

There are two types of wafer fabrication methods. The Czochralski (CZ) and the Float-zone (FZ) silicon wafers. The first type of wafers are formed from a single-crystal silicon seed that is being drawn upwards from molten silicon. During the process the quartz crucible (SiO_2) dissolves, releasing large quantities of oxygen. It was determined that more than 99% of the gas is evaporated but the rest stays trapped in the crystal [41].

An alternative method of growing high purity silicon is the so-called FZ process. A high-purity polycrystalline rod and a monocrystalline seed crystal are placed on top of each other. Both parts are slowly melted with a specific radio frequency and the seed crystal is slowly pulled away from the rod [41]. This process has less trapped oxygen and carbon, making them more ideal for long wet etching due to the lower chance of SiO_2 micromasking. Unfortunately, this type of wafers with higher purity and higher resistivity than CZ wafers are also more expensive.
Figure 2.1 shows the notation of the silicon crystal, where $h = 1/a, k = 1/b$ and $l = 1/c$ [78]. Figure 2.2 illustrates the most common crystal orientations used in this project, in which Table 2 indicates the crystal angles and their corresponding angles.

Table 2.1: Silicon crystallographic planes and their respective angles toward the vertical ⟨100⟩ direction [80].

Direction (hkl)	**(100)**	**(110)**	**(210)**	**(310)**	**(410)**
Angle toward ⟨110⟩	45°	0°	18.43°	26.57°	30.96°
Angle toward ⟨100⟩	⟨100⟩ 90° ⟨110⟩ 45°	⟨111⟩ 54.73°	⟨221⟩ 48.18° ⟨211⟩ 65.9°	⟨331⟩ 45.87° ⟨311⟩ 72.45°	⟨441⟩ 45.87° ⟨411⟩ 76.37°

2.1. Etch properties

Etching MEMS devices into silicon often occurs with wet anisotropic etching. Crystal orientations are selectively removed due to differences in activation energies, causing the etching to be an-isotropically [58]. The sidewalls and shapes are determined by the slowest etch rates of a certain crystal plane. For silicon, the slowest etch rate belongs to the ⟨111⟩ plane, giving the characteristic inverted pyramid shape. When concave corners are etched, perfect square shapes can be obtained. However, with convex corners, a phenomena called undercutting plays a large role. The results of etching an inverse pyramid with concave corners is shown in Figure 2.3, and the effect of convex corners is shown in Figure 2.4.

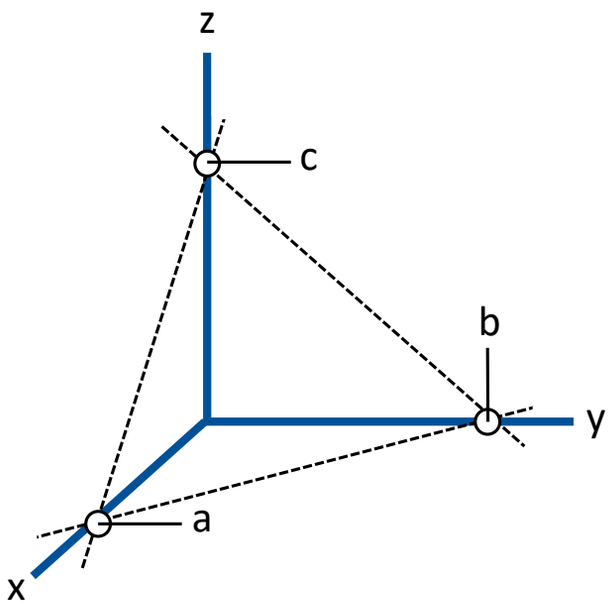


Figure 2.1: Crystal notation.

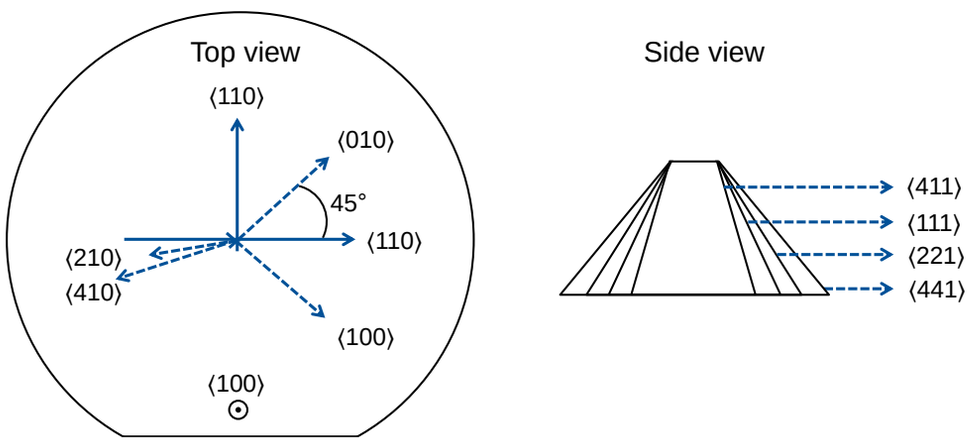


Figure 2.2: (100) silicon wafer crystal orientation.Left: top view. Right: side view of etched truncated pyramid.

Multiple methods are investigated for compensating the undercutting effect of convex corners, of which corner compensation is the best known. However, this method features several difficulties and problems and therefore another method is also proposed. This method features the silicon crystal properties to remove the need for compensation structures completely.

2.1.1. Corner compensation

This method adds additional structures to protect the fast etching planes. These structures become large with increasing etch depth, meaning a large area is needed to make the structures. Precise control of the etch rate of different planes is still not understood fully [45], which makes it difficult to create perfect convex corners with wet anisotropic etching. Several shapes to protect the convex corners are shown in Figure 2.5. The etch process of the double square corner compensation on the right part of Figure 2.5 was confirmed by a SEM image shown in Figure 2.6.

The star-shape uses the property that the KOH or KOH + IPA wet etchants attack the crystal planes differently. Therefore, the shape should be oriented along the ⟨130⟩ plane for KOH etching, and ⟨120⟩ for KOH + IPA [45]. P. Pal et al. determined mathematically after several tests the etch rates of the crystal planes and determined relations of the compensating structure size versus etch depth.

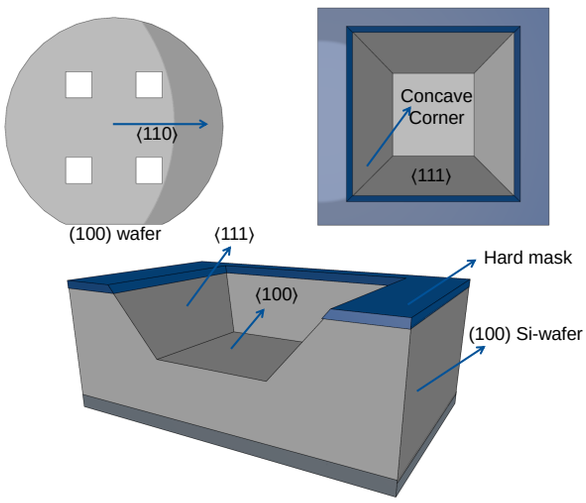


Figure 2.3: 100 wafer wet anisotropic etching, concave corners.

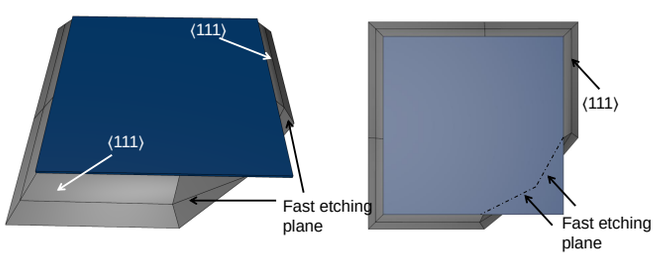


Figure 2.4: Undercutting convex corners with wet etching.

To give the reader a general feeling of the size of these structures (and that they become really large), the relations are given below where *d* is the relative dimension given in Figure 2.5 [45]. The mentioned values are for KOH + IPA etchants, which differ from pure KOH etching. With pure KOH etching, the undercutting is more extreme and the structures need to be even larger (up to a factor of 3). If small micrometer structures with a depth of 100 um need to be fabricated, the structures that need to be added at each convex corner surpasses the structure area by a factor of 10 or more. This clearly shows the high area usage of this kind of corner compensating.

- d = -1.7 + 1.16H (triangular)
- d = -5.3 + 1.24H (Star shape)
- d = -10 + 1.33H (rectangle)

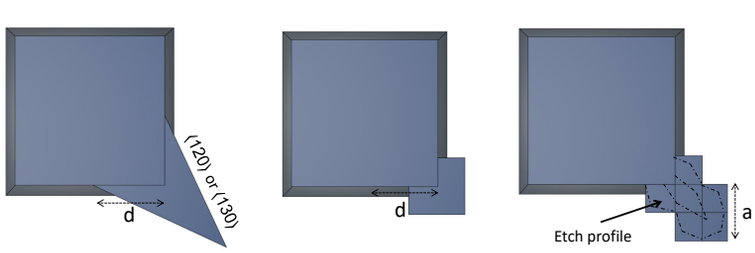


Figure 2.5: Corner compensating structures for KOH etching. Structures based on [18] [49].

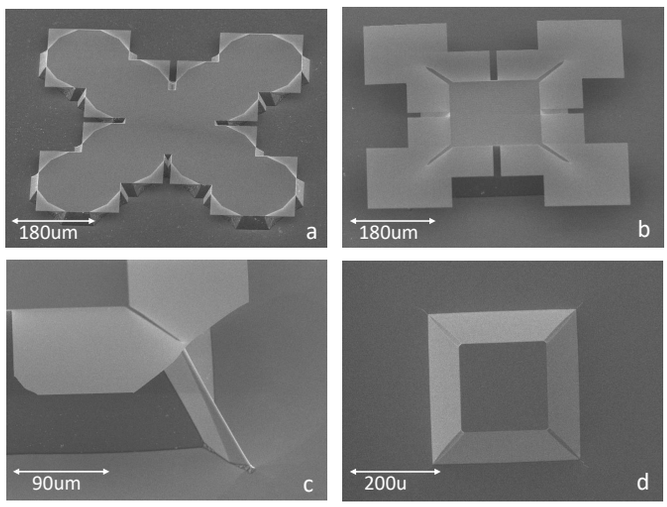


Figure 2.6: Pictures evidencing the effect of corner compensation. Convex corners are protected by slowly removing the compensating structures when etching, until the structures are gone and a perfect pyramid remains.

2.1.2. Aligning to crystal planes to protect convex corners

Another method is trying to use the property of fast etching planes. It is well known that a square mask aligned to the ⟨110⟩ plane will have large undercutting of its convex corners. Rotating the structures to align with the ⟨h10⟩ plane (with h > 1), will decrease this destructive undercutting due to the smaller differences of etch rates [61] [62]. Increasing the rotation from the ⟨210⟩ plane to ⟨310⟩ plane shows even less undercutting and the advantage is that the structure keeps its shape during further etching. Results from [62] are shown in Figure 2.7 where the top part clearly shows undercutting of the convex corners when the structure is aligned to the ⟨110⟩ plane. Rotating the structure along other crystal planes shows that the undercutting becomes less rough and severe. Increasing this to the ⟨310⟩ plane improves this a lot, with an even smoother surface when rotating to the ⟨510⟩ plane as shown in Figure 2.7.

The major advantage for this technique is that no large additional corner compensating structures are needed. Therefore, more structures can be manufactured on the same area. Also the structures are independent on the etch depth. After a certain while, the 3D structure will not change its shape during further etching [62]. However, very precise knowledge and control of the silicon crystal structure is necessary to ensure correct working of this method.

2.2. Etch selectivity

To ensure accurate wet etching of (100) silicon, the structures need to be perfectly aligned to the ⟨h10⟩ planes. A slight misalignment can cause undercut during the anisotropic etching. This effect leads to uneven structures where the square shapes become deformed, potentially causing crucial errors in many IC processes. The wafer is cut from an ingot where the crystal structure is precisely determined by X-ray diffraction, after which the flat is cut into the silicon. If the crystal orientation is not exactly as the flat suggests, it is difficult to achieve perfectly smooth sidewalls of the KOH etched MEMS devices [72]. This is due to the fact that the KOH removes the ⟨100⟩ planes faster than the ⟨111⟩ planes. Therefore, a (100) wafer with a wafer flat accuracy around 1 degrees, could make MEMS fabrication processes more difficult.

The wafer stepper ASML 5500 available in TU Delft's Else Kooi Laboratory (EKL) aligns the wafers following the Edge Sensor Repro procedure. The wafer is rotated and the border of the wafer is mapped and the center and flat are determined. In 2010, a series of tests were performed to see the alignment error of the wafer stepper. The average results of the 15 processed wafers were -41.09 urad rotation error with a standard deviation of 23.51 urad. Converting this to degrees results in an error less than 0.003 degrees. This means that the zero layer will have a very small misalignment (compared to the wafer-flat).

To minimize the rotation error (the difference between the wafer flat and actual silicon crystal ⟨110⟩ plane) , one wafer of a batch can be used for determining the misalignment of the processed layer. Knowledge of the wafers rotation error, can be used to process further wafers with this given rotation offset, given they are from the same ingot and therefore have the same flat to crystal orientation.

Several structures can be created to detect the crystal orientation. The most common and intuitive structure is a set of rectangles rotated around the ⟨110⟩ direction of the (100) wafer. If the ⟨110⟩ crystal orientation is exactly 90° to the wafers flat, the middle structure without a rotating offset will be etched perfectly homogenous. If the wafer is misaligned, one side of the bar will be etched differently. The structure that is etched without undercut shows the crystal orientation. J M Lai et al. states that an accuracy of 0.01 degrees is possible to determine the ⟨110⟩ crystal orientation on (100) silicon wafers. The principle is shown in Figure 2.8.

Another alignment structure is shown in Figure 2.9. If this structure is perfectly aligned on the ⟨110⟩ plane, the etching will be symmetrical. A misalignment can be detected when both sides are not removed in the same way. The top part of the structure will be etched differently than the bottom part, resulting in uneven underetched regions. These regions, due to the tip-shaped form, can be easily detected with a microscope.

To be able to precisely detect the crystal orientation, the aforementioned structures were rotated along the ⟨110⟩ plane with increments of 0.002 to 0.1 degrees. In literature [32] [70] [59] it was found that the structures are able to detect crystallographic orientation with an accuracy up to 0.05 degrees.

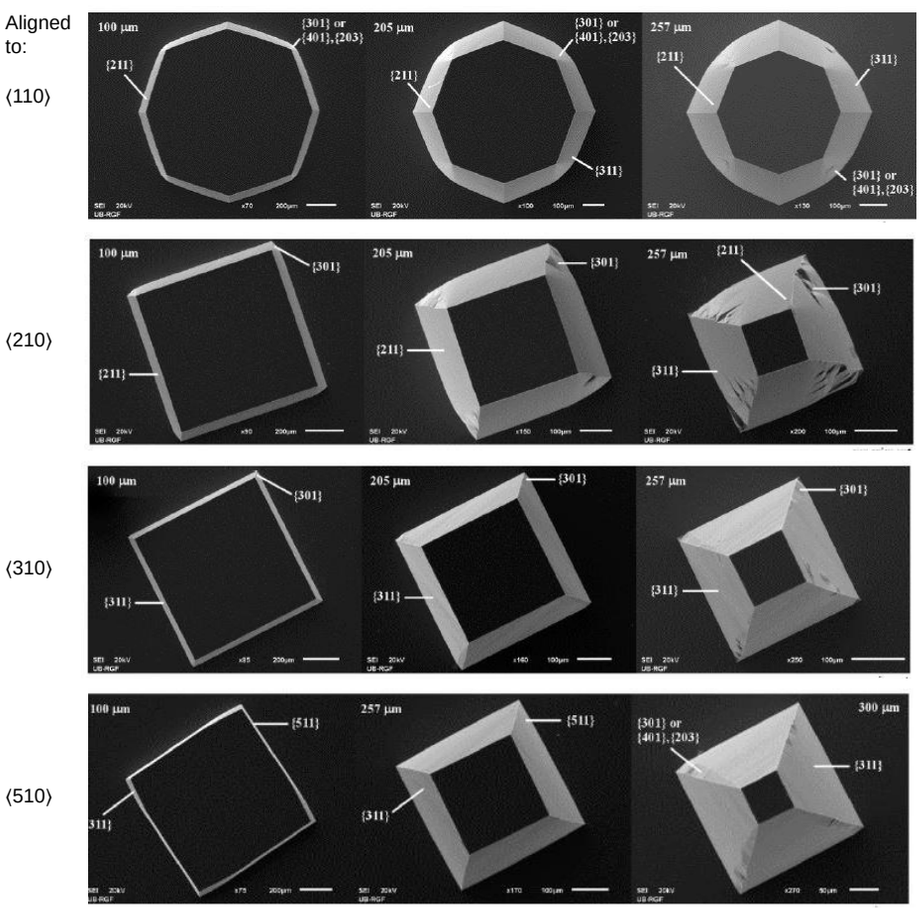


Figure 2.7: Wet etching a squares aligned to the ⟨h10⟩ planes in 25% TMAH. Smoother surface occur with higher order crystal rotations. Image reproduced from Smiljanic et al. (2019) page 5-8 [62].

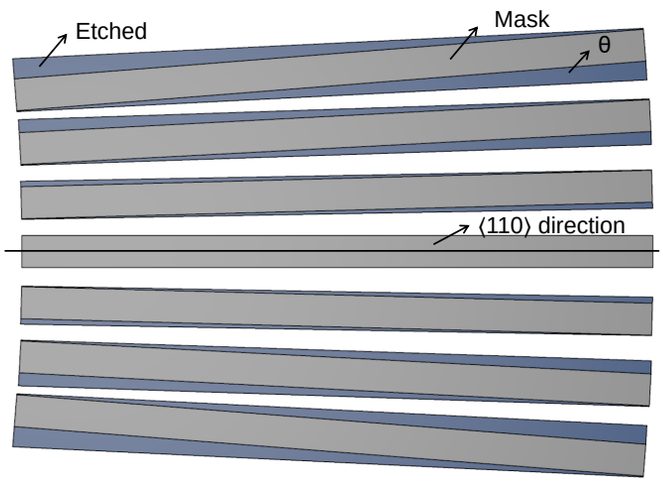


Figure 2.8: Rotation misalignment structures.

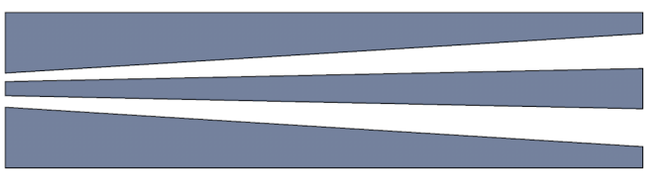


Figure 2.9: Alignment fork structure.

2.3. Etch solutions

Alkaline solutions are most often used to etch crystalline silicon. Potasium hydroxide (KOH) and Tetramethylammonium hydroxide (TMAH) are commonly used solutions (how the solutions are prepared is explained in Appendix C). In both cases, the silicon reacts with the OH^- in the solution and forms a soluble $SiO_2(OH)_2^{2-}$. The reaction creates hydrogen bubbles which leave the solution. The complete reaction equations are given in Equations 2.1 to 2.4 [42] [77].

The oxidation starts when the hydroxyl groups react with the silicon surface. The reaction forms the so-called silicate. Figure C.1 in Appendix C shows interesting creations on the wafers surface. When etching only a partially submerged wafer, the reaction products form a cracked silicate layer where air meets the etching solution.

$$Si + 2OH^- + 4h^+ \rightarrow Si(OH)_2^{++} \tag{2.1}$$

Then the H_2O reacts to produce hydroxide and hydrogen.

$$4H_2O \rightarrow 4OH^- + 2H_2 + 4h^+ \tag{2.2}$$

The formed silicate will react further with the hydroxyls to form a soluble.

$$Si(OH)_2^{++}4OH^- \rightarrow SiO_2(OH)_2^{2-} + 2H_2O \tag{2.3}$$

The final redox reaction of hydroxide etching with alkaline solutions is given below.

$$SI + 2OH^- + 4H_2O \rightarrow Si(OH)_2^{++} + 4OH^- + 2H_2 \tag{2.4}$$

In literature, the etchant is often mentioned by either molar- or percentage concentration. 1 mole of KOH has 59 grams of KOH in one liter of water. To give the reader a clearer picture of how the two concentrations are related, the relation between molar and percentage concentrations (for KOH) are given in Table 2.2.

Table 2.2: KOH Molar concentration to % concentration conversion table.

Molar Concentration [M]	1	3	5	7	9	11
Concentration [%]	5.9	17.7	29.5	41.3	53.1	64.9

2.3.1. KOH etching

Looking at Equation 2.1 it can be seen that only the OH^- part of the potassium hydroxide is used in the reaction. The K^+ is left in the equation and the charge balance is kept by the fact that the soluble part $SiO_2(OH)_2^{2-}$ has a charge of −2, which balances out the $2K^+$.
Equation 2.2 also clearly shows that the H_2O is part of the reaction process. Not enough water molecules cause the reaction to slow down. Two etch properties can be formulated that are true for KOH etching:

1. Low KOH concentration -> low OH^- concentration -> low etch rate.
2. High KOH concentration -> low H_2O concentration -> low etch rate.

This property already shows that silicon etch rates behaves not linearly with the KOH concentration. For more information the reader can find different KOH and KOH + IPA etch rates in Appendix B, clearly showing the non-linear behavior of etch rate versus concentration.

The KOH solution is etching the ⟨100⟩ planes fast and is almost not attacking the ⟨111⟩ planes. This is how the characteristic 'KOH' etch holes in (100) silicon wafers are made with roughly 55° slopes. However, the hydroxide part of the KOH is highly active and therefore the solution attacks other crystal orientations as well. The ⟨110⟩ planes are removed roughly twice as fast than the ⟨100⟩ direction (See Appendix B Figure B.2 for etch rates of different crystal planes). This means that a structure etched to a depth of 100 um (thus in the ⟨100⟩ plane) will also be etched laterally up to 200um. This lateral etching is called under-etching or undercutting and can give rise to serious problems when small high aspect ratio structures are wished for. Possible remedies to minimize this undercutting effects will be discussed in later sections in this Chapter.

2.3.2. TMAH etching

Another common anisotropic etchant is Tetramethylammonium hydroxide (TMAH). The advantage of TMAH to KOH is its organic nature and therefore compatibility with current CMOS processes. TMAH is an organic alkaline solution that is able to etch (compared to KOH surface roughness sdr 0.010) less rough planes (See Table 2.3 for measurement results) due to the active OH^- bonds and the lower surface tension of the solution [30]. The liquid can be seen as a soap-like solution, where the TMAH is able to maneuver and etch the silicon more easily than with KOH. Once again, this results in fast etching of the ⟨110⟩ planes, which makes it difficult for small pitch electrode arrays. However, hillocks are still observed with TMAH etching. Similar as with KOH, the hillocks are bounded by the ⟨111⟩ planes and most often in an octagonal shape. It was thought that the formation of hillocks was contributed due to the trapped oxygen particles in the silicon wafers. FZ wafers probably could minimize the chance of random hillocks even further [9].

In contrast to KOH etching, the etch rate is linear with TMAH concentration (See Appendix B Figure B.3). With TMAH, lower concentrations are needed (5-40% TMAH, instead of 30-70% in KOH). The etch rate of KOH, at the same temperature is higher than that of TMAH [66] [82].

2.3.3. Influence of Isopropyl alcohol

To be able to manufacture small pitch electrode arrays, high lateral etch rate of the ⟨110⟩ planes have to be minimized. A well documented solution for this is adding Isopropyl alcohol (IPA) to the KOH solution. As mentioned before, the small KOH molecule (compared to TMAH) has highly active OH^- groups that etch the ⟨110⟩ planes very fast. Introducing IPA to the solution 'blocks' the highly active KOH bonds with its less active free OH^- groups. The relative large molecule with its 'slow' OH^- groups will slow down crystal plane specific reactions with the silicon surface, reducing the lateral undercut (for example the ⟨110⟩ plane). The effect of IPA is demonstrated in Figure 2.10, where the same structure with large compensating structures is etched to a depth of 100 um with and without IPA.

The cause for the slower reaction rate on specific crystal planes has to do with the fact that the alcohol molecules are absorbed on the silicon surface with their hydrocarbon chains by van der Waals forces. The hydroxyl groups are oriented towards the solution (away from the silicon surface), effectively blocking the access to the silicon [52]. This is schematically shown in Figure 2.11 for TMAH (same principle applies for KOH).

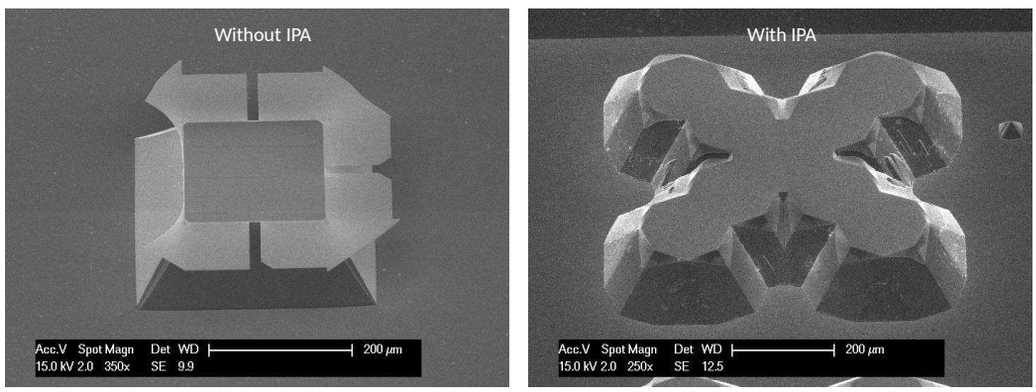


Figure 2.10: KOH etching with and without IPA. Clear reduction in lateral undercut is visible with added IPA. Etch depth is 100um.

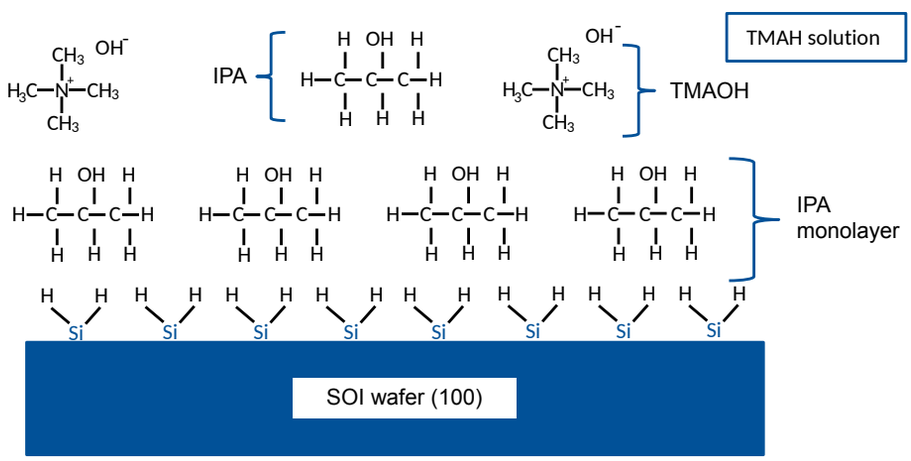


Figure 2.11: IPA monolayer blocking the silicon surface [83] [77].

The etch rate of KOH with IPA added into the solution can be seen in Figure B.1. However, due to the fact that organic IPA is very soluble in TMAH (which is also organic), its effect with respect to lateral etch rate, is small.

TMAH has the ability to create even smoother etch surfaces than KOH, as shown in numerous studies ([6] [7] [30]). Adding IPA/Triton to the solution of both KOH and TMAH, can create even smoother etch planes and reduces the micro pipes on the silicon (See Table 2.3). But, as will be shown extensively in the next Section 2.8, this is not the case for all etch planes.

2.3.4. Influence of Triton-x-100

Adding Triton to the TMAH solution can greatly reduce the convex corner under-etching [50]. Studies ([21] [30] [50] [68] [67]) show that adding Triton keeps the ⟨100⟩ etch rate relatively constant but it greatly reduces the ⟨110⟩ etch rate, making it extremely useful for creating convex cornered free-standing structures in (100) wafers. Another advantage is that it lowers the surface tension and creates even smoother etch surfaces. Triton, with its large molecule, functions as a blockade to crystal specific planes and reduces their respective etch rates. Therefore, it has basically the same effects as adding IPA to a KOH solution: lowering the lateral etch rates and decreasing the surface roughness of certain crystal planes.

2.4. Hard masks

To etch deep structures in the silicon ⟨100⟩ surface, a suitable hard mask is needed that is not affected by the etchant. As KOH/TMAH is hardly affecting silicon nitride (Si_3N_4), this material was chosen. The material is easily deposited and also removed afterward by either dry or wet etching. Silicon nitride thicknesses of 100 to 500 nm were experimented with to determine the combination of hard mask that is easily and quickly removed, and is still thick and firm enough to minimize the risk of bending/breaking of the mask during rinsing steps. Figure 2.12 shows three different hard mask thicknesses. It clearly shows that the 104 nm thick layer (Figure 2.12c,d) is not strong enough to keep its original position when the mask is almost freestanding. The layer is so thin it bends and falls on the silicon substrate, shielding unwanted parts of the structures. The 230 nm layer (Figure 2.12b) shows similar results as with the 500 nm. The layer is strong enough to hold itself over large free floating areas. All masks slightly damage when rinsing the wafers after etching. With careful rinsing this effect is minimized but future problems are not expected because then, ideally, the wafers will not be etched and rinsed repeatedly. Now for testing purposes, the same wafers see several rinsing steps. When the proper etch parameters are found, the etching will be performed in a single process, after which the breaking of the nitride layer during rinsing is not an issue anymore.

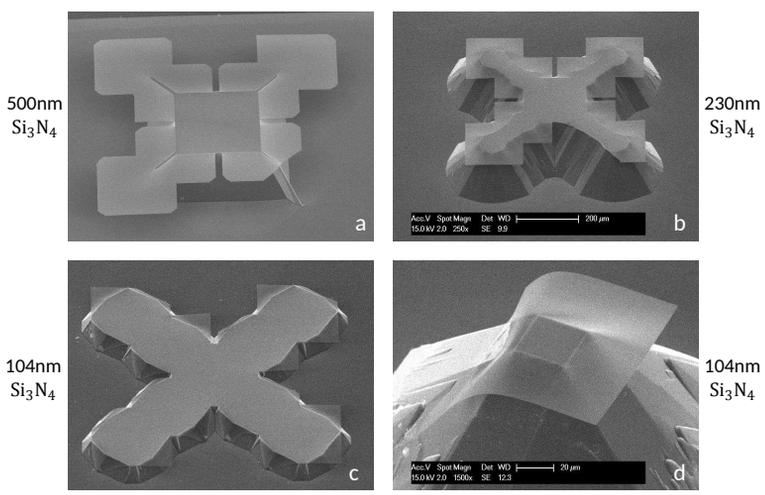


Figure 2.12: Different silicon nitride hard mask thicknesses.

2.5. Etch contamination

Particles in the etching solution or on the wafers surface can cause unwanted etch effects. Preventive measures have to be taken to minimize the risk of contamination. Several procedures, causes and effects will be addressed below.

2.5.1. KOH contamination

As potassium particles can contaminate further and other CMOS processes in the cleanroom, cleaning is an important next step. After etching, the wafer is submerged in four different distilled water baths for several minutes, after which the wafers go through the complete standard cleaning line of EKL (HNO_3 69% and heated 99%HNO_3 and rinsing). It was found that residual KOH flakes will dissolve when cleaning steps are performed long enough. Figure 2.13 shows a wafer with numerous KOH flakes on the surface of the water, which were removed after several additional cleaning steps. The crystalline shape of the crystals and the possibility to remove it in the distilled water and HNO_3 baths indicates a high probability that the solid residues were of KOH origin. These particles form when the soluble solution evaporates, leaving the potassium to solidify on the wafer again. Figure 2.13 shows several KOH particles on a silicon surface. After additional cleaning steps, almost all particles were removed.
Contaminating other wafers and processes aside, other problems can arise when the wafers or solutions are not cleaned/refreshed enough. Contaminating particles can also cause micromasking, affecting the surface quality of the etching [19].

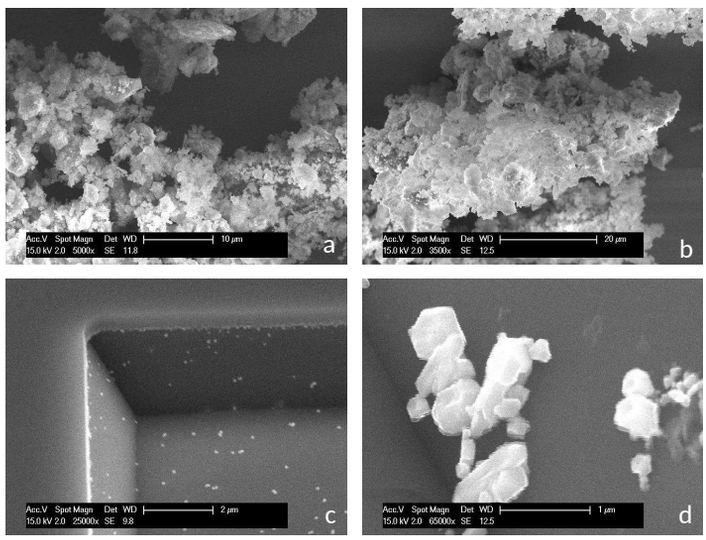


Figure 2.13: KOH insolubles on the silicon surface.

2.5.2. Effect of oxygen precipitates

Another often mentioned cause for rough surfaces and so-called hillocks (small pyramidal shaped structures, most often found on the ⟨100⟩ planes) is SiO_2 contamination. Trapped oxygen in the silicon wafer can cause unwanted micromasking due to the formed SiO_2 particles on the surface. Figure 2.14 shows how this can occur. FZ-wafers contain less trapped oxygen and should minimize the possibility for this type of contamination, if this would really become a contamination issue.

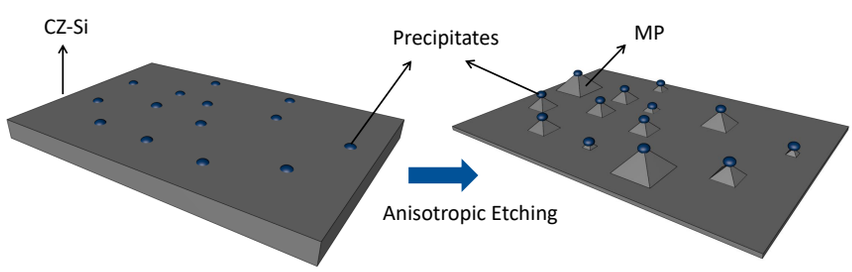


Figure 2.14: Micropyramidal hillock formation (MP) due to silicon dioxide precipitates.

After determining that the flakes on the silicon surface were of KOH origin, it was chosen not to pursue and improve the SiO_2 contamination. The wafers were etched in a solution of 0.55% HF for 4 minutes to remove the native oxide before starting the KOH/TMAH etching, which was found to be sufficient. This dip is crucial because the selectivity of KOH is relatively high for (100)-Si/SiO_2 = 200/2000 [42].

2.5.3. Effect of hydrogen precipitates

Equations 2.1 - 2.4 show that hydrogen is released from the etching reaction with alkaline solutions. If the H_2 bubbles are not removed quickly enough from the wafers surface (dwell time of the H_2-bubbles is too long), this can cause plateau generation on the ⟨100⟩ surface. This effect was schematically shown in 1999 by Schroeder et al [55] in Figure 2.15 and 2.16 and was also found in this research, shown in Figure 2.17. The plateau forming was especially bad if multiple wafers were placed close to each other in the same etch bath, blocking a large part of the liquid circulation. Due to this, it is thought that the released H_2 bubbles were longer 'trapped' against the silicon surface, causing these masking effects [5]. This effect was remedied by only etching single wafers with a large magnetic stirrer and with a higher rotation speed (250 RPM).

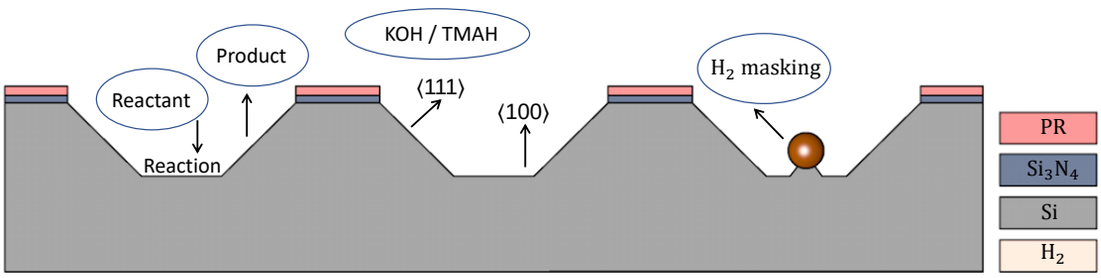


Figure 2.15: 2D drawing of plateau generation/masking due to H_2 bubbling on ⟨100⟩ surfaces.

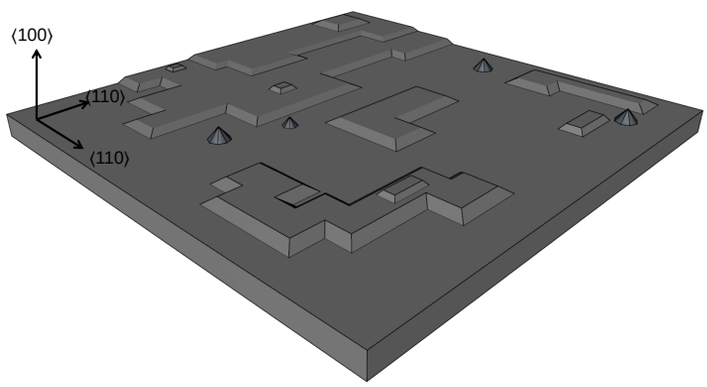


Figure 2.16: Schematic representation of plateau forming on the ⟨100⟩ surface due to H_2 bubble forming. The pyramid hillock formation is also shown.

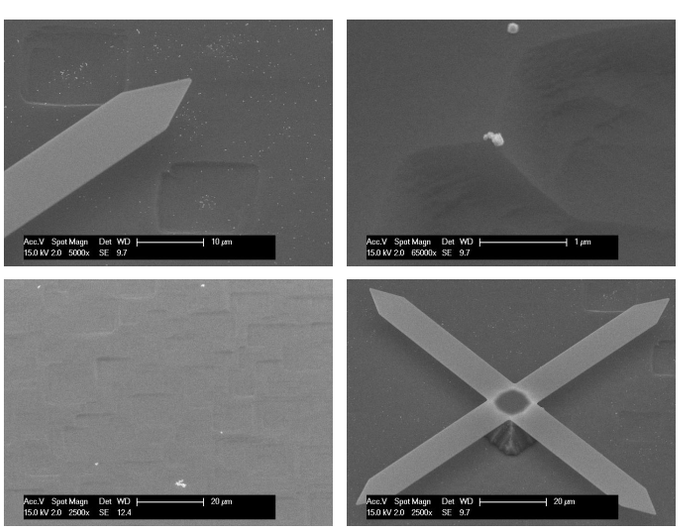


Figure 2.17: Plateau forming due to h_2 bubbling.

Another method to minimize the effect of trapped H_2 bubbles is ultrasound agitation.. The ultrasound waves can detach possible H_2 bubbles form the surface and combined with magnetically stirring the solution, smoother etching can be achieved [7] [76]. The effects of the ultrasound agitation are clearly depicted in Figure 2.18.

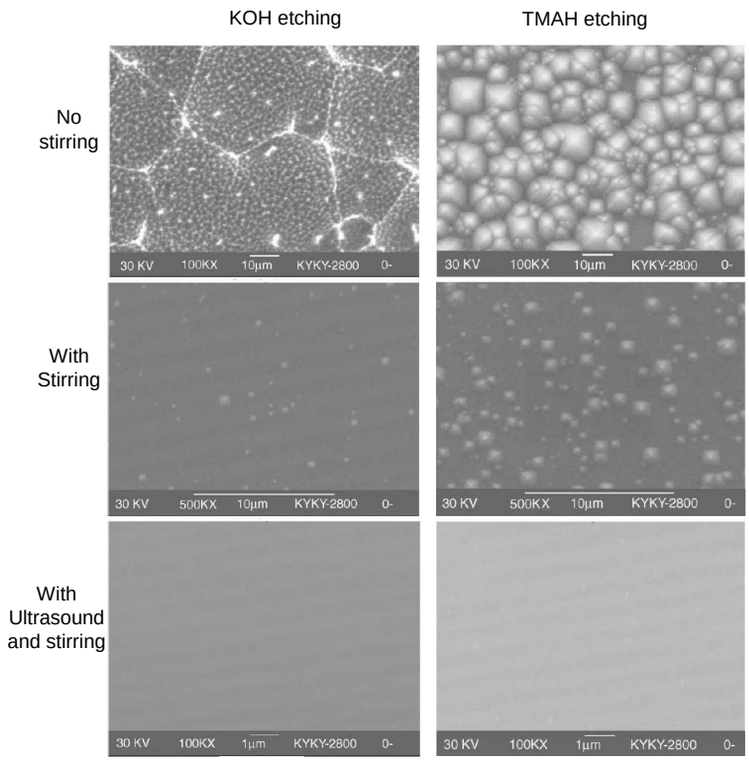


Figure 2.18: Silicon surface roughness with and without ultrasound agitation.
Image reproduced from Chen et al. (2002) page 3 [7].

2.6. Etch concentration and surface roughness

Literature ([19] [55] [66] [82]) shows large differences in surface roughness with different etch concentrations. Low KOH concentrations cause high surface roughness on the ⟨100⟩ planes due to the lack of active OH^- groups [82]. Increasing the concentration gives smoother ⟨100⟩ surfaces, as shown in Figure 2.19. The same is true for TMAH etching. A concentration too low causes hillock forming and rough surfaces on the etch planes [66], which is shown in Figure 2.20.

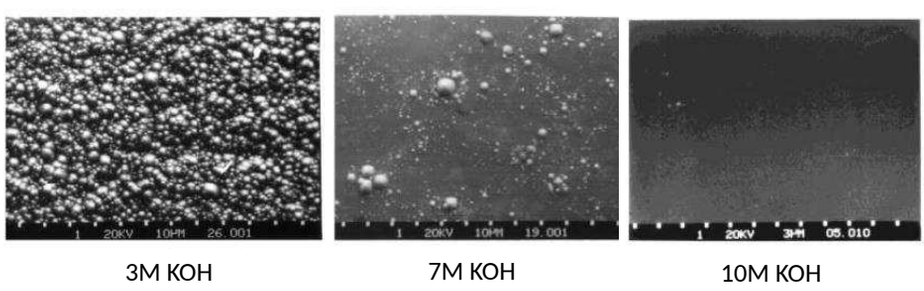


Figure 2.19: KOH surface roughness with different concentrations.
Image reproduced from Zubel et al. (2001) page 5 [82].

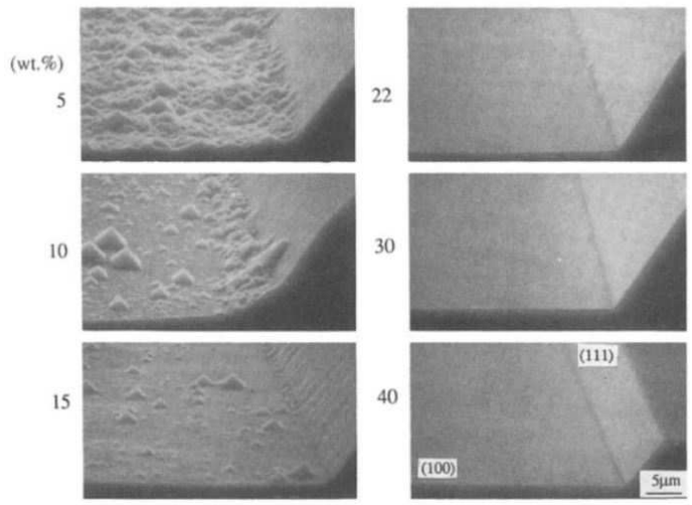
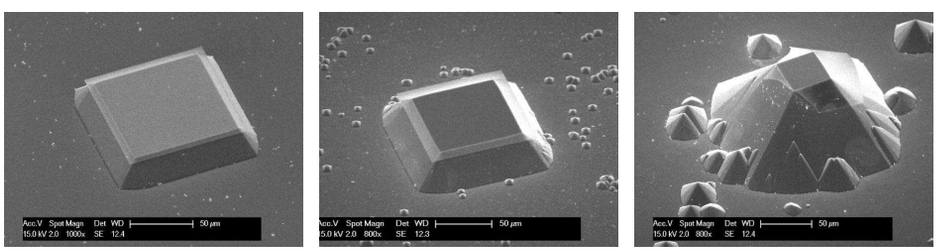


Figure 2.20: TMAH surface roughness with different concentrations.
Image reproduced from Tabata et al. (1992) page 3 [66].

This so-called hillock forming at low concentrations was also confirmed by etching several wafers at differences depths. From the results, it can be confirmed that etching to small depths, the hillock forming is still very small and hardly noticeable. Etching deeper, damaging hillocks start forming (see Figures 2.21 and 2.22). It appears, once again, that the micropyramid hillocks and triangular hillocks favor the ⟨111⟩ plane.



21 um etched 30 um etched 75 um etched

Figure 2.21: Hillock forming on the silicon surface at different etch depths with <7.5M KOH.

Surface roughness measurements (arithmetical mean height sa[1] and developed interfacial area ratio sdr[2]) were performed on each etched wafer to give more insight of the ⟨100⟩ surface after different etch solutions. The results agree with the literature and show that KOH + IPA and TMAH + Triton results in the most smooth ⟨100⟩ surfaces (see Table 2.3 for measured surface roughness's in this research). SEM results of the surface are shown in Figure 2.23.

Table 2.3: Surface roughness measurements. Measured with Keyence Microscope, averaged results.

	KOH	**KOH + IPA**	**TMAH**	**TMAH + Triton**
sa	0.098	0.076	0.090	0.016
sdr	0.010	0.005	0.009	0.001

[1] arithmetical mean height: it expresses, as an absolute value, the difference in height of each point compared to the arithmetical mean of the surface [28].

[2] Developed interfacial area ratio: expressed as the percentage of the definition area's additional surface area contributed by the texture as compared to the planar definition area [28].

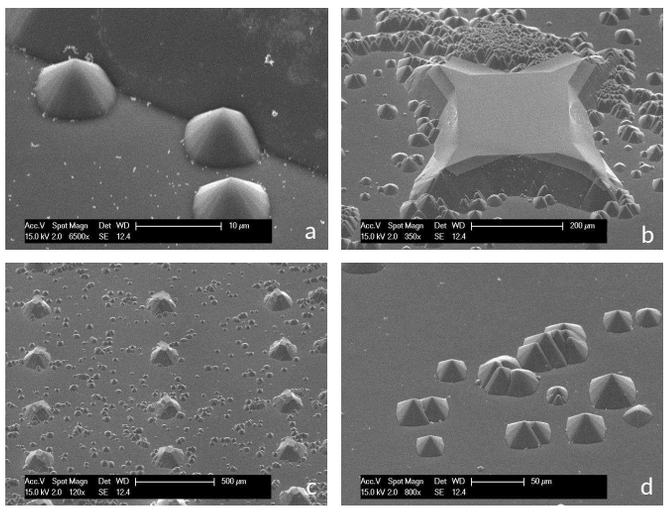


Figure 2.22: Large hillocks oriented in the ⟨111⟩ plane due to low KOH concentration.

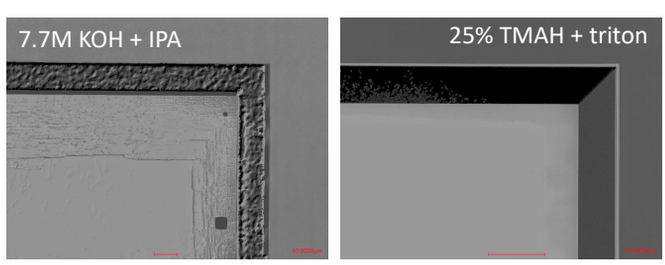


Figure 2.23: Differences in ⟨100⟩ surface roughness KOH + IPA and TMAH + Triton.

2.7. Additional TMAH etch to reduce surface roughness

Due to the high lateral etch rates of TMAH in (100) silicon wafers, this solution without any additives is unpractical for etching deep small pitch micro-structure arrays. However, the high etch rate can be taken as an advantage to remove the ⟨111⟩ favored hillocks that are formed after long KOH/ KOH+ IPA etching. Due to the high lateral etch rate, it was thought that a quick dip in the TMAH solution could result in 'smoothing' of the crystal planes. Etching the wafer longer in TMAH will result in deformation of the pyramid structures to due the different etch planes/rates. Therefore, it was chosen to only etch to a maximum of 10 minutes in the TMAH solution, which already showed very promising results (See Figure 2.24).
Etching silicon with an already older TMAH solution gives similar results. First smooth crystal planes were visible. But, as the solution was used more often (after etching approximately 3 wafers for 100um in a 0.7 liter solution), droplet shaped hillocks formed on the structures. Because the first wafers did not show these droplet forming and the effect worsened the older the solution got, it is assumed this was due to contamination issues. This result is shown in Figure 2.24f. Due to the differences in developed etch planes by KOH + IPA and TMAH this method is not very feasible for subsequent steps. Possible smoothing by a TMAH + Triton solutions (yielding the same etch planes) would be a possible solution if the lateral etch rates would not be so much lower. This will cause less effective removal of the large hillocks.

2.8. Determined etch planes

Wet etching pyramid structures with a depth of 100 um in a KOH solution gives rise to several difficulties. The lateral undercut (⟨110⟩) for a KOH solution is too large to create a dense microelectrode array. Due to this high etch rate of the ⟨110⟩ plane, the compensating structures needed to achieve such a depth are too large. A KOH concentration too low gives rougher surfaces, but concentrations higher than 8M give rise to another set of problems: different etching planes.

A paper already published in 2000 by I. Zubel et al. showed that structures etched in a high KOH concentration show additional crystal planes. With a KOH concentration of 7.5M, only ⟨hh1⟩ planes (⟨221⟩, ⟨331⟩, ⟨441⟩) appear after etching. After etching continues, the planes favor the ⟨441⟩ direction [80], which was also experimentally found in this research. With a concentration increase, additional crystal planes start showing of the order ⟨h11⟩, next to the crystal planes already formed due to low KOH concentrations.
This means for smoother surfaces, a higher KOH concentration is wished for (which can also be seen from Appendix D Figure D.1), but this also gives additional crystal planes as shown in Figure 2.25. Decreasing the concentration will remove the additional crystal planes when etching, but increases the surface roughness. Additionally, higher temperatures exhibit the same characteristics as with the KOH concentration. Increasing the temperature, will give rise to crystal orientations ⟨hh1⟩ and ⟨h11⟩. The results in Figure 2.26 corresponds to the results from Zubel et al [80].
As already mentioned, adding IPA to the solution is known to improve the roughness of certain crystal planes. Thus, adding IPA to the KOH mixture improves the roughness and also dramatically decreases the lateral undercut, enabling for more dense small microelectrode arrays. However, IPA smooths not all crystal planes of silicon. Crystal planes in the ⟨h11⟩ direction exhibit more triangular hillocks on its plane that appear to follow the ⟨111⟩ direction [47] [51] [81]. Hence, IPA is a very practical addition to smooth certain crystal planes like the ⟨110⟩ and ⟨100⟩ but it increases the roughness in the ⟨211⟩ and ⟨311⟩ directions.

Fortunately, another advantage of IPA is that it exactly removes these ⟨h11⟩ etch planes [81] [84], as was also confirmed in this thesis results (See Figure 2.27). This figure shows that when etching in a pure KOH solution both ⟨221⟩ and ⟨211⟩ planes appear, including IPA only results in ⟨221⟩ planes.
Appendix D Figure D.2 indicates that most crystal planes become smoother when IPA is added, except for the ⟨h11⟩ planes. It is also seen that a KOH concentration too high, again gives an increase in surface roughness for the ⟨110⟩ and ⟨100⟩ planes, which is possibly caused by the fact that only a little IPA can be dissolved in the high concentrated solution. To summarize and give the reader a clear overview of the effects of KOH concentration, temperature and addition of IPA, Table 2.8 is added.

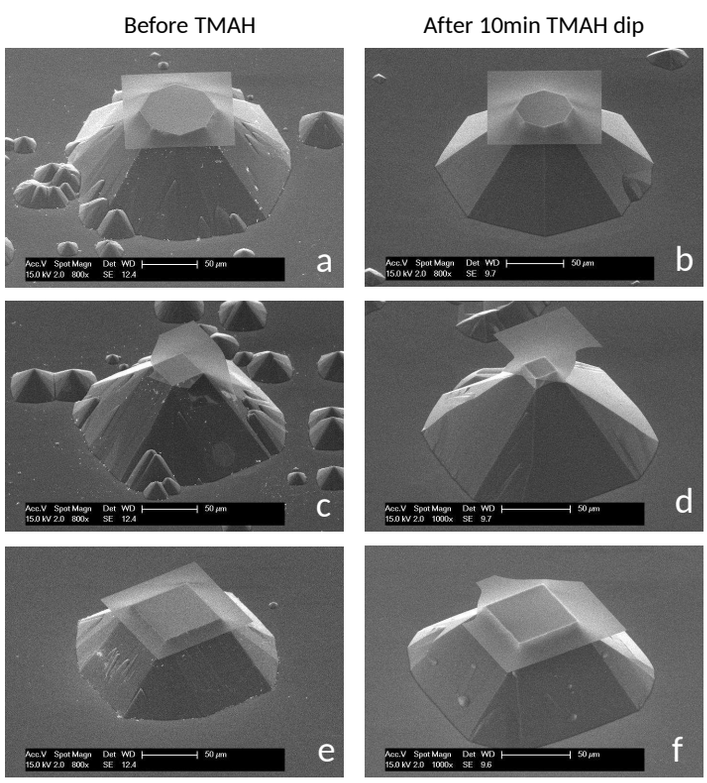


Figure 2.24: Using the high lateral etch rate of TMAH to smooth crystal planes. Change in (steeper) etch planes due to TMAH is visible.

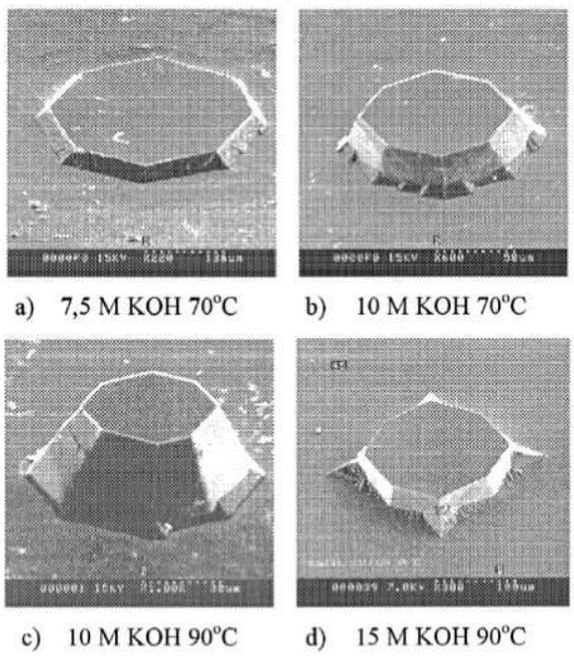


Figure 2.25: Different crystal planes with different KOH concentrations. Image reproduced from Zubel et al. (2000) page 4 [80].

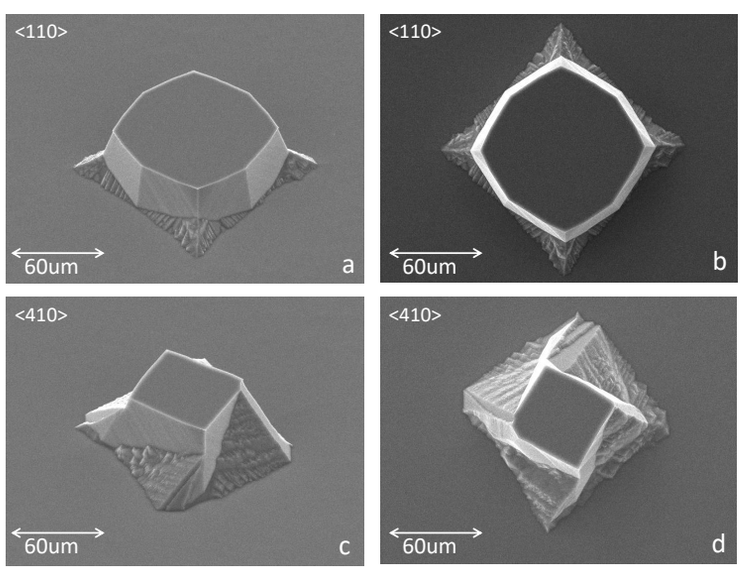


Figure 2.26: Etch result for KOH 8.5M, ⟨h11⟩ and ⟨hh1⟩ etch planes visible.

Table 2.4: Characteristics of different alkaline etching concentrations and surfactants [80].

Solution composition	**Surface roughness**	**Developed cyrstal planes**	**Lateral undercut**
KOH <7.5M (70°C)	Rough	⟨221⟩, ⟨331⟩, ⟨441⟩	High
KOH <7.M (90°C)	Rough	⟨211⟩, ⟨331⟩, ⟨441⟩, with possibly ⟨221⟩, ⟨331⟩, ⟨441⟩	High
KOH 7.5M-15M (70-90°C)	Smooth	⟨211⟩, ⟨311⟩, ⟨411⟩, ⟨221⟩, ⟨331⟩, ⟨441⟩	High
3-10M KOH + IPA	Smoother	⟨221⟩, ⟨331⟩, ⟨441⟩	Low
TMAH 25% (80°C)	Smooth	⟨211⟩, ⟨311⟩, ⟨411⟩	Very High
TMAH 25% + 0.25%v/v Triton	Smoother	⟨221⟩, ⟨331⟩, ⟨441⟩	Low

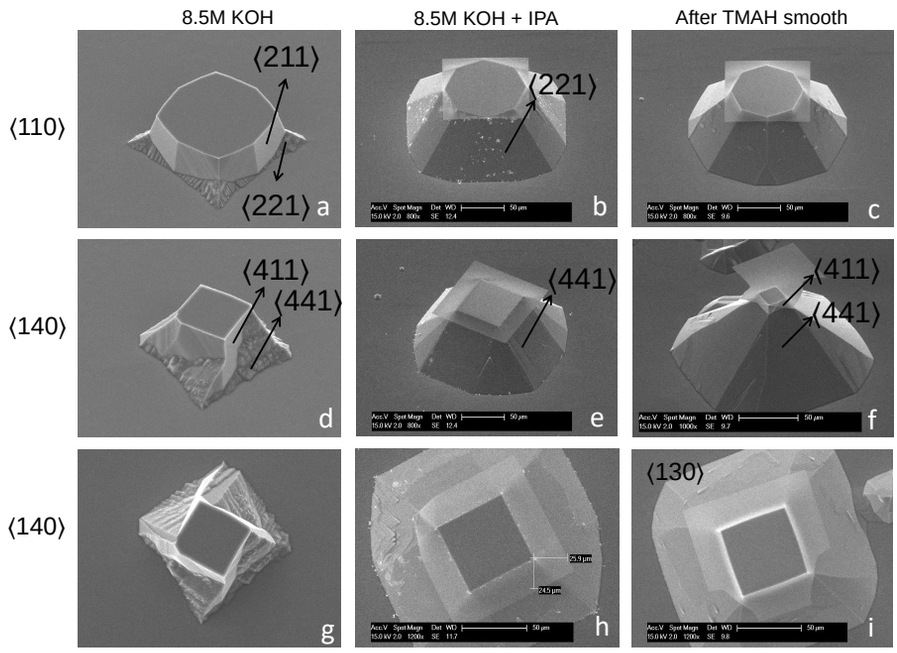


Figure 2.27: Visible etch planes for KOH and KOH + IPA etching.

2.9. Determined etch rates

Due to different activation energies of crystal planes, etch rates differ from plane to plane. Specific crystal plane etch rates can be used to estimate the sizes of the corner compensation structures for a specific depth. Figure 2.28 shows for several crystal planes their respective etch ratios. The figure shows that higher order etch planes experience faster etching than the traditional ⟨110⟩ plane. Adding IPA dramatically reduces etching of all lateral ⟨h10⟩ etch planes. Due to the very slow etch rate of the ⟨110⟩ plane, accurate results became difficult to achieve. Figure 2.28 shows that best ⟨100⟩/⟨h10⟩ are achieved with KOH + IPA etching, but due to the lower surface roughness, TMAH is still favored.
All KOH + IPA measurements were performed with IPA saturation to ensure the concentration remained the same during etching and the etch rates could be reliably determined. Saturating the TMAH solution with Triton gave, similar to TMAH only, high lateral etch rates of the ⟨h10⟩ planes. Several wafers were etched with a TMAH + saturated Triton solution and after an etch depth of 54um, the 120um mask size structures were almost completely removed due to lateral undercut. Etching with new TMAH + ≈ 0.25%v/v Triton gave the same structures top base with a depth of 118um, indicating the lateral undercut is drastically lower. Therefore, precise control of the Triton surfactant is important due to the its large influence. All TMAH experiments were performed at a temperature of 80°.

Etch rate versus temperature

It is well known that the temperature greatly influences the etch rate (and surface quality). To verify this property, as suggested by literature, several wafers were etched at different temperatures. Three samples were used for each temperature and the average is shown in Figure 2.29. The results show an Arrhenius-type kinetic relation between etch rate and increasing temperature, as expected with current literature [4] [10]. Because the electrode structures do not have a stopping layer for KOH etching, a relative slower etch rate could be more suitable due to more suitable depth control.

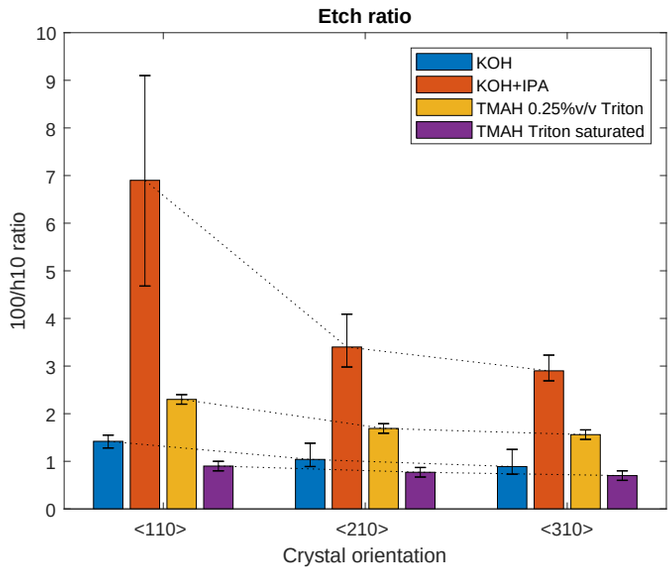


Figure 2.28: Etch ratio for different etching solutions at 80°C.

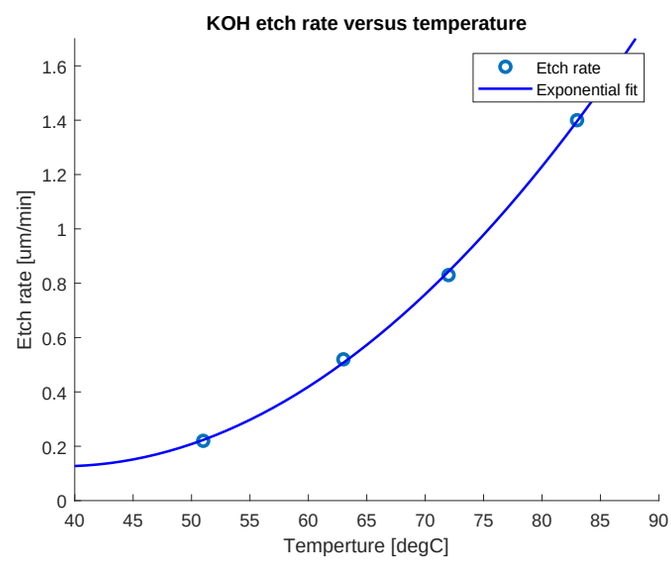


Figure 2.29: Relation between etch rate ⟨100⟩ direction and temperature.

2.10. Summary of findings

Multiple etchants, concentrations, temperatures and surfactants were used to determine the most suitable process flow for fabricating truncated pyramids with a height of 80-100um. Surfactants need to be added to the KOH and TMAH solutions to suppress the high lateral etch rates. Therefore, it is not very feasible to manufacture a dense array of microelectrodes using alkaline etchants without any surfactant. The disadvantage of the addition of IPA and Triton is the change in developing etch planes in etching. When using only KOH etching, the ⟨111⟩ planes are the well-known resulting slopes with an angle of 54.7°. As shown, it is possible to create perfect truncated pyramid with a height of 100um with double rectangular corner compensation methods in a KOH solution. But, unfortunately this technique relies on very large compensating structures and the top base cannot be decreased to the needed 10um.

Crystal rotated structures do not require large corner compensation structures. Implementing these structures with a KOH solution gives the disadvantage of either a very rough surface (low concentration) or different etch planes at the mask and base side of the structure (high concentration). Adding IPA removes both disadvantages but cause for the lower angled slopes (⟨hh1⟩, ≈ 46°) to be dominant. Hence, there seems to be a tradeoff (with KOH and IPA) between:

- Lateral undercut
- Surface roughness
- Different developed crystal planes at the top and base part of the truncated pyramids
- Slope angle

Because a small top base truncated pyramids with smooth sidewalls (as motivated and detailed in the next chapter) and in a small pitched array was wished for, it was chosen that when etching with KOH, a KOH + IPA liquid was the most feasible solution. This enabled for smoother surfaces and a less specific control over the KOH concentration. The double square corner compensation method was proven to work and result in dense arrays of pyramids but it remained difficult to determine the precisely needed compensation sizes to result in a top base of ≈10um. Because the crystal rotation structures give more freedom due to the fact that only a single rotated square mask cover is needed to construct truncated pyramids, this method is favored.

TMAH favors different etch planes and yields in the steepest <h11> crystal planes (≈76°). Due to the large undercut, it is not practically possible to create dense arrays of structures with TMAH using standard corner compensation methods. Therefore, it was chosen to continue with the crystal rotated structures. Due to the low surface tension of the liquid, the sidewalls are smoother after etching than the KOH solutions, but the slopes are possibly too steep for patterning in subsequent steps. Therefore, final structures were all designed to work with the TMAH + Triton solution. This gives the smoothest etch planes, most simple etching because the solutions are already pre-mixed to a 25% concentration, and pyramid slopes of ≈46°. A given advantage of this solution is that when changing the temperature, the ⟨110⟩/⟨100⟩ etch rate can be slightly changed. At the highest temperature of 80°C the lateral etch rate is suppressed the most [68]. Decreasing the temperature increases the lateral etch rate, giving an extra dimension for creating truncated periods with correct dimensions.
For example if the etch depth is already reached but the top base of the pyramid is still too wide, decreasing the temperature increases the lateral etch rate and reduces the top base faster (with respect to ⟨100⟩ plane). To summarize, a general overview of all etchants properties is shown in Table 2.10.

After considering all properties and trade-offs found during initial experiments, it was found that TMAH + Triton at 80° C with crystal rotated structures is the most promising setup to create dense arrays of truncated pyramids with patterned electrodes on the slopes and top.

Table 2.5: Results and properties of different etchants for rotated pyramid structures.

Etchant	**Surface texture**	**Slope angles**	**Undercut**	**Processing difficulty (1 easy, 5 hardest)**
<45% KOH	Rough	Shallow slopes	Large	5
>45% KOH	Rough	Top steep slopes, bottom shallow slopes	Large	4
KOH + IPA	Smooth (certain planes)	Shallow slopes	Small	3
TMAH	Smooth	Steep slopes	Large	1
TMAH + Triton	Smoothest	Shallow slopes	Small	2

3

Fabrication of micropyramids

Biologists from the Medical University Leiden (LUMC) gave dimension, shape and array pitch guidelines for manufacturing 3D neuron electrodes. Therefore, several parameters were determined for the electrode array, in close collaboration between the TU Delft en LUMC.

- The structures should not (all) have a sharp tip, but rather a flat top with a size of ± 5um (roughly the size of the nucleus). For first prove of concept designs, the top base can be larger.
- The structure should not contain sharp edges. A truncated pyramid structure or octagonal shape is preferred.
- The height of the structures should be at least 75um.
- Three distinct and vertically stacked microelectrodes should be patterned on the facets.
- The 3D microarrays should be able to conform to MEA readout standards. A 60 electrode read-out circuit would imply 20 structures in a 4 by 5 matrix.
- The distance between the structures can be around 200um.
- No strict sizes for sampling points were given for first designs, 10-20um was aimed for.

To investigate the different silicon properties and etch selectivity as mentioned in Section 2.3, high resolution chrome masks were ordered (see Appendix A). Different structures were tested with each a different set of corner compensation shapes, sizes and crystal orientations. The most prominent structures are shown in Figure 3.1. Additional test structures were placed on the wafer to determine crystal specific etch rates and properties. This information helped determine the mask sizes from Figure 3.1, which are shown in Table 3.1. Their respective etch behaviors are discussed and depicted in the upcoming section. Additionally, crystal orientation structures were placed on the mask to determine the misalignment in the wafer flat and crystal orientation. The zero layer (alignment markers for subsequent steps) was placed on the wafer by the ASML 50/800 Wafer stepper to have the highest possible rotation accuracy. Subsequent lithography steps were performed using the EVG 420 manual contact aligner.

Etching was performed in the fume hoods of the EKL cleanroom class 10000 (Figure 3.1). A 2.5 liter borosilicate glass beaker filled with a 2 liter etch solution was placed on a hotplate, connected to a thermocouple placed in the solution to ensure a constant temperature. A Magnetic stirrer was placed in the solution to have a constant flow in the etch solution. The wafers were fixated to individual holders and placed in the solution in a near vertical position (down facing surface structures). After the first results, it was determined to only etch up to two wafers at the same time in a 2 liter solution. This had to do with improved flow of the solution and increased longevity of the etch solution.

Table 3.1: Mask sizes corresponding to structures from Figure 3.1.

	Double square	**Single square**	**Rotation ⟨110⟩**	**Rotation ⟨210⟩**	**Rotation ⟨310⟩**	**Star**
a [um]	184	10, 30, 50	n/a	n/a	n/a	160
b [um]	195	5, 8, 10, 15, 20	110, 124	120, 136	133, 148	170

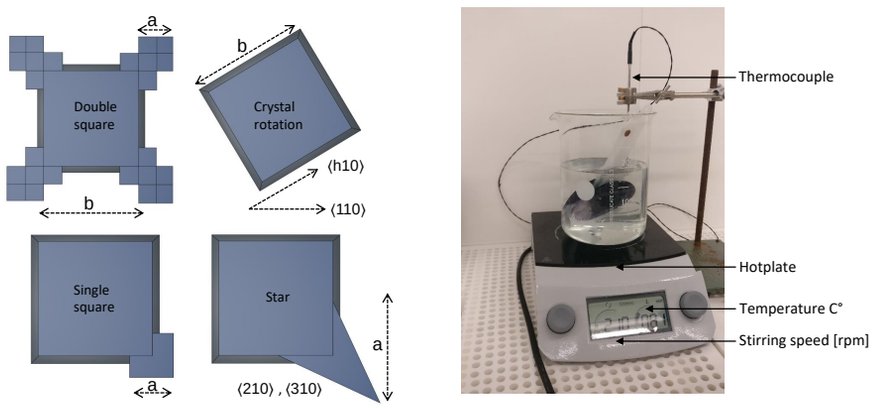


Figure 3.1: Mask structures for creating truncated pyramids and etch setup.

3.1. Corner compensation test structures

Test structures revealed that very fine mask structure connections (e.g. the connection between the corner compensation and the square itself) were not able to protect the underlying silicon, resulting in the inability to conserve the convex corners. The first results are shown in Figure 3.2. It clearly shows the middle square with four large compensating structures placed exactly at its convex corners. But instead of protecting the corners, it seems the connection was lost and the structures were etched separately from each other, leaving a hole in the middle. The electrode with more overlapping compensating structures shows correct etching and protection of the convex corners.

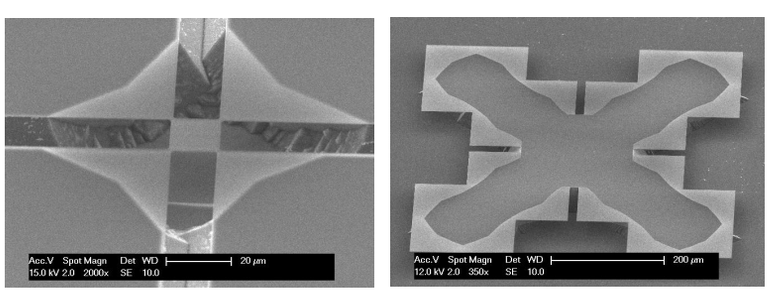


Figure 3.2: Two different corner compensation methods: small and large overlap.

It appeared that the fine connections on the mask were correctly patterning the silicon nitride (SiN) layer on the wafer, but this thin SiN layer was unable to protect the silicon at these connections. The overlap was often less than 1um, and giving the possibility of a crystal defect and very small crystal misalignment, it is possible the etchant finds a small fast etching plane and start etching until both structures are free from each other. This theory was tested by etching short times and repeatedly checking the results under the microscope (SEM). It was indeed found that after a short etch time, the structures with small overlapping corner compensating structures were separated from each other and etched away (as shown in Figure 3.3). The suspicion is that some defects and crystal misalignment can cause the etch separation and removal of the complete structures. With these tests it was also found that other compensating structures behaved as expected and protected the convex corners. These results are shown in Figure 3.4.

Multiple electrodes were protected by corner compensating structures that are too small for etching to a depth of 100 um. But, as Figure 3.6 shows, the principle is correct. It shows perfect pyramid shapes but only with a depth of less than 20 um. This shows the compensating structures are too small for etching the full 100 um. This knowledge about the horizontal etch rate of these compensating structures can give insight to what the actual sizes have to be when a depth of 100 um is etched. Therefore, a wafer was etched until 90 um to see whether the structures were able to protect the final pyramid shape. The results are shown in Figure 3.5ab, which clearly indicates that the convex corner is protected and with the final 10 um, the compensating structure is perfectly etched away (Figure 3.5cd).

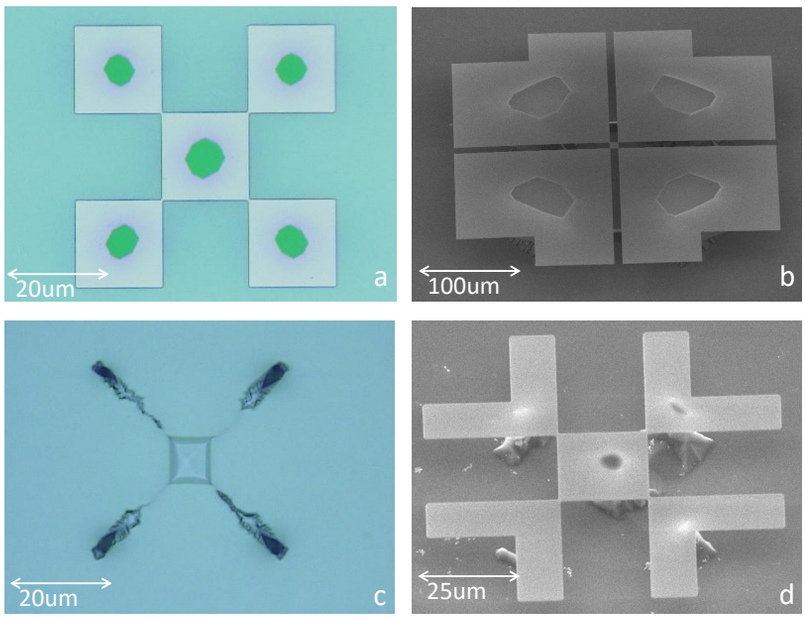


Figure 3.3: Small overlapping corner protection is not able to protect the structures.

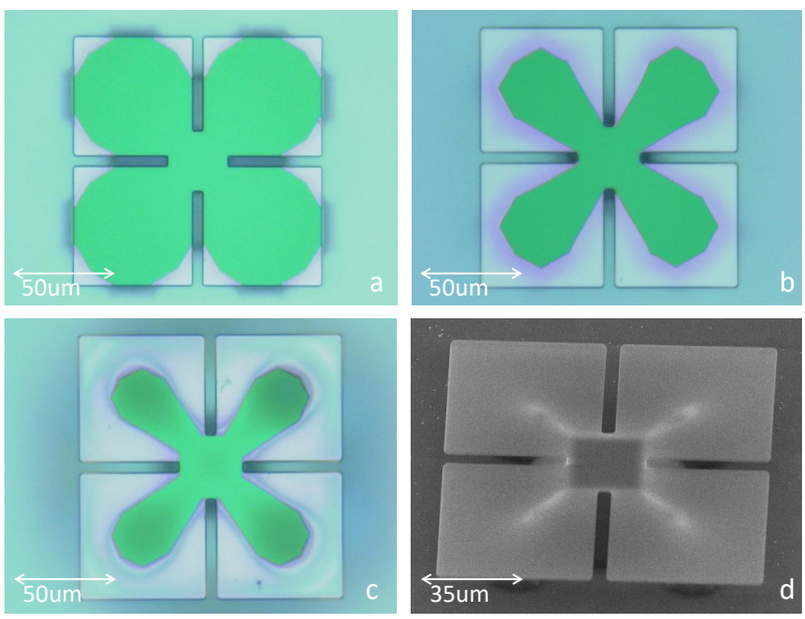


Figure 3.4: Effect of convex corner protection at different etch depths.

As Figure 3.5 shows, the large compensating structures protect the convex corners for the complete 100 um etch depth. Due to the fact that the etching ratio between the ⟨100⟩ and ⟨111⟩ planes is roughly 400:1, the undercutting in the ⟨110⟩ direction is not visible [18]. However, the size of the compensating structure is determined by the relation between the ⟨100⟩ and ⟨410⟩ etching lines, which was mathematically approximated by W. Fan et al. in 2006 [18]. The equation used to determine the size is given in Equation 3.1, where H is the etch depth, a the compensating structure size, and Uc a normalized parameter which was determined to be 1.46.

$$H = \left(\frac{11}{4\sqrt{34}Uc} + \frac{5\sqrt{2}}{32}\right)a \tag{3.1}$$

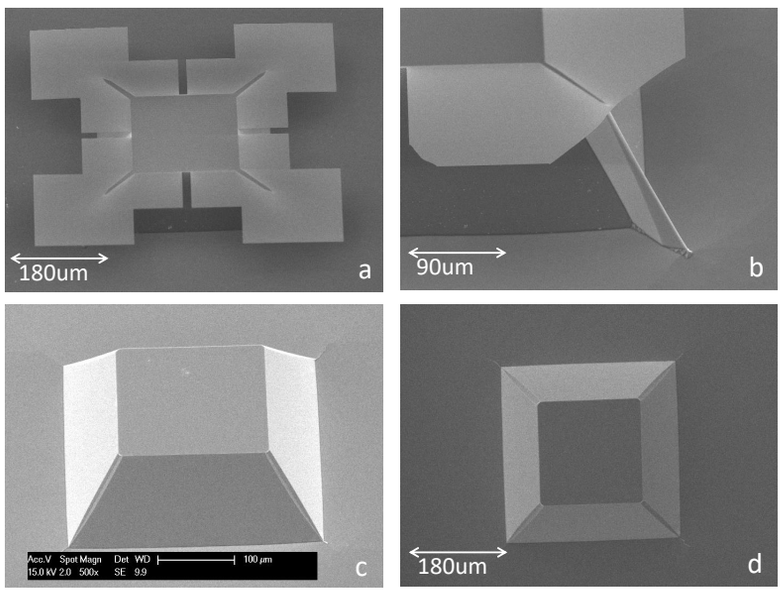


Figure 3.5: Pyramid etched with double square corner compensation to 90um (ab) and 100 um (cd).

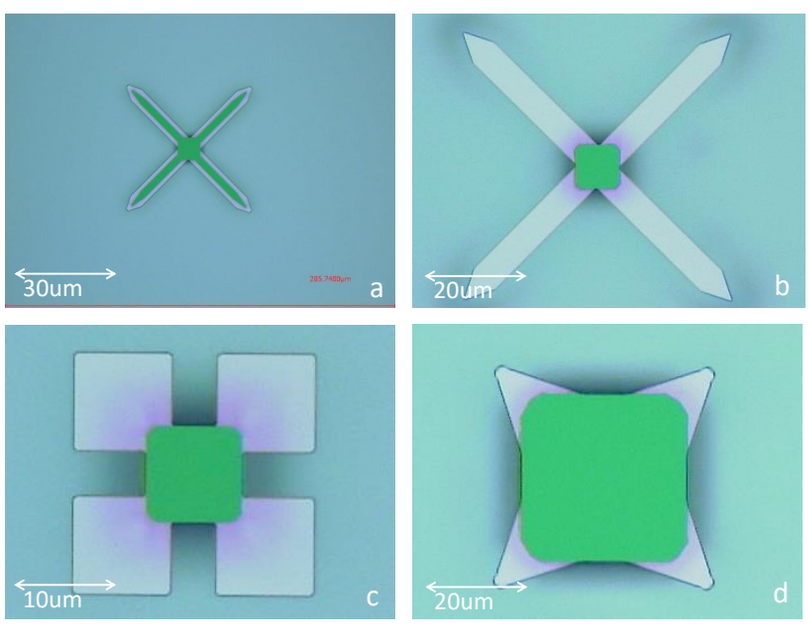


Figure 3.6: Corner compensation methods that result in pyramid structures.

The resulting size of the compensating structures was found to be 184 um. Half of this length is embedded in the original feature. This means that the original feature needs to have a minimum feature size of 184 um (both sides, see Figure 3.7). Therefore, to create a pyramid structure (in a KOH solution) with a depth of 100 um, the total area size needed for fabrication is at least 560 um (a separation distance between the structures is needed to ensure correct etching of the planes). This is graphically shown in Figure 3.7. It can be seen that a final array of electrodes can be fabricated with a size of 195 um, with a minimum pitch of 370 um (distance between electrodes). Using IPA would enable for smaller compensating structures (as literature suggests), giving a more dense electrode array. However, due to the difference in developed etch planes when using IPA this structure is not a feasible solution for this.

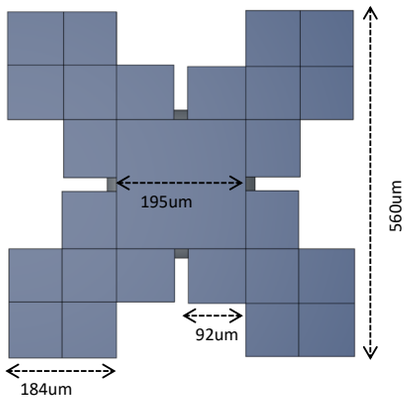


Figure 3.7: Electrode with double corner compensating structure.

KOH + IPA

Figure 3.8 shows star-like corner compensating structures that result in near perfect pyramid formation. However, this technique is also not feasible for KOH etching due to the minimum dimensions needed for the triangular corner compensation structures. With more experiments it could be possible to implement this shape with KOH + IPA etching. However, due to the difference in developing etch planes with the IPA addition, it could be possible that this technique does not result in proper pyramid shapes.

Figure 3.9 depicts small double square compensating structure sizes. Using these results and the lateral undercut ratios, estimations can be made to determine the size of the corner compensation structures for KOH + IPA etching to a depth of 100 um. The large double square KOH compensation structures were 184um wide and the once showed in Figure 3.9 are only 10um wide. This clearly shows that etching with the addition of IPA, enables for far smaller compensating structures. Therefore, by looking at the graph presented in Chapter 2 Figure 2.28, the crystal rotated structures should have a beginning mask size of around 80um (indicated by the letter *b* in right part of Figure 3.1) to end with a 5-10um top base truncated pyramid. The double square mask design cannot be estimated closely due to current lack of samples. But, first estimations indicate that the compensating squares should be between 10-12um (indicated by the letter *a* in the left part of Figure 3.1), and base part (*b*) around 50um. Decreasing the mask base causes significant undercut and therefore loss of the structures. Compensating with larger double square structures would be possible but without any further data, size estimations are difficult.

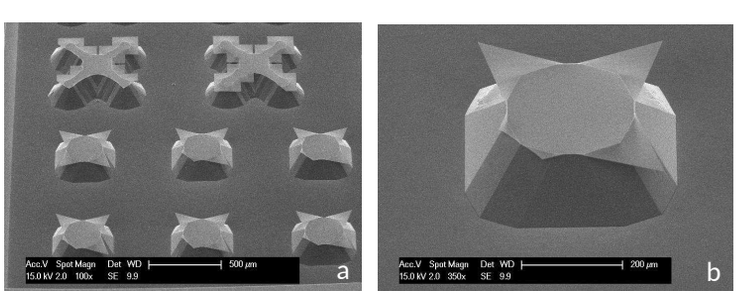


Figure 3.8: Large star-like corner compensation structure for KOH etching.

TMAH + Triton

The lowest lateral etch rate was achieved with a KOH + IPA solution. This would, in theory, yield for the most dense array of micro-electrodes. However, as the electrodes were allowed to have a space up to 250um apart, the smoothness of the structures and ease of fabrication were given priority. Looking at the graph presented in Chapter 2 Figure 2.28, depending on the crystal rotation, each crystal rotation structure should have a different size. A depth of 70um showed that the top bases of the structures were roughly the correct size, indicating the masks sizes should be larger than that. Looking at past experiments, the mask size shown in Table 3.2 are chosen for the final designs.

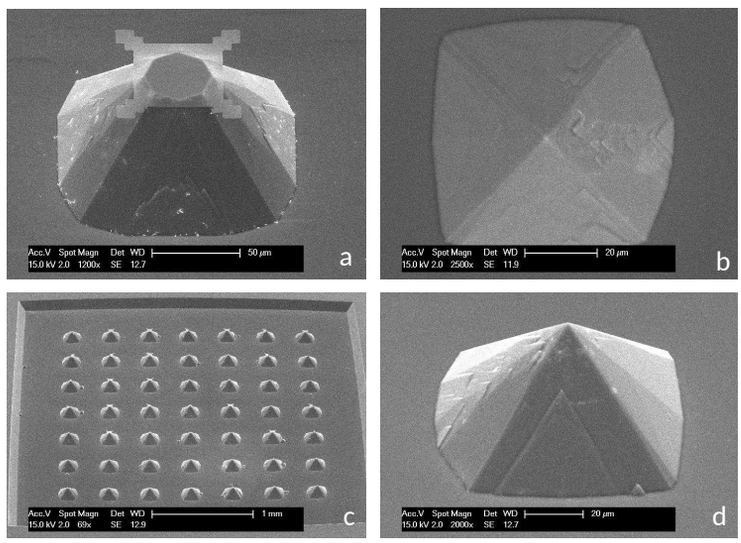


Figure 3.9: Smaller double square corner compensation structures for KOH + IPA etching.

Table 3.2: TMAH + Triton mask sizes.

Crystal rotation	**⟨110⟩**	**⟨210⟩**	**⟨310⟩**
Mask size [um]	110	120	133
Mask size [um]	124	136	148

3.2. Crystal orientation

Alignment forks are used to precisely determine the crystal orientation. If in the future a wafer stepper is used, which aligns the wafers almost perfectly to the flats orientation, these structures can be used to align the wafers even better to the ⟨110⟩ plane. The first wafer of a batch (all from the same ingot) will be used to determine the crystal orientation. All other wafers will be aligned and exposed with a wafer that is pre-rotated with the found misalignment.
The alignment fork is roughly 350 um long and the inner part has an angle of 1.5 degrees, whereas the outer parts have an angle of 5 degrees. These relative small angles should, according to literature [70], give better visible results of the difference in underetching. The zero-layer is placed by the wafer stepper and the KOH mask is manually aligned with the EVG420 contact aligner. After etching roughly 30-40 um deep, the structure was inspected with the Keyence microscope and high detailed stitched images were taken to determine the precise crystal orientation.

Figure 3.10 shows part of the crystal alignment structures. When the structures are not aligned to the ⟨110⟩ plane, underetching is clearly visible and indicating in-proper alignment (Figure 3.10 left inset). The sides of the small beams converging to the the left show different etch profiles when rotated along the ⟨110⟩ plane. When etching is symmetrically, the structure is aligned to the plane (Figure 3.10 right inset). With this technique, the misalignment of the ⟨110⟩ plane was found to be 0.15 degrees.

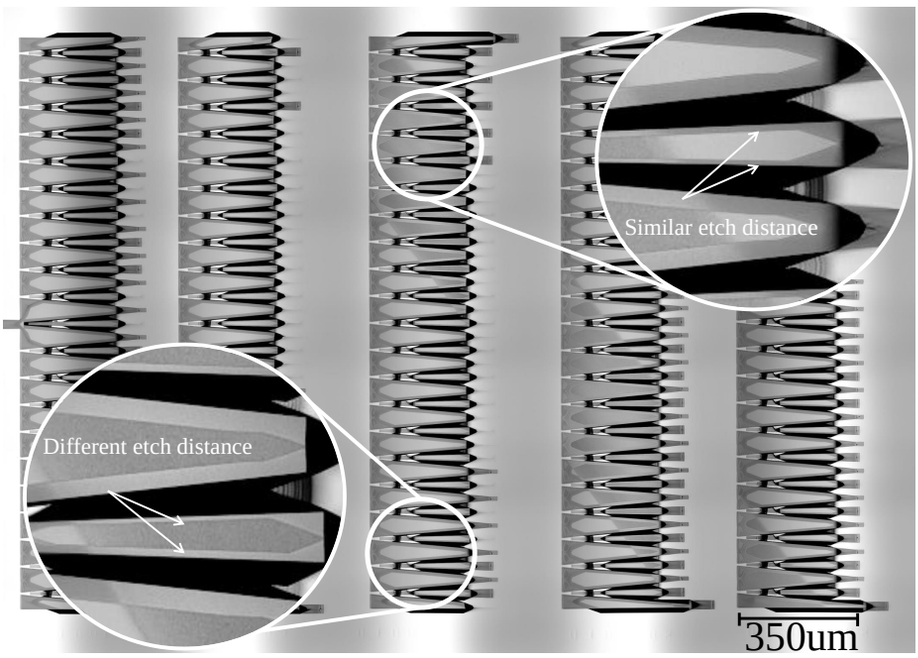


Figure 3.10: Crystal alignment structure.

3.3. Summary of findings

Fine mask connections should be avoided to minimize the effect of structure and corner-compensation separation. It was found that square masks with sizes between 110 and 148um, rotated along different crystal planes, gave the best results. To ensure proper etching, crystal alignment structures can be added on the wafer to give the possibility of rotation corrections. Adding surfactants causes the appearing facets of the structures to form from a lower slope angle, but the advantages outweigh this disadvantage: the decrease in lateral undercut and surface roughness of the etched planes. The results for etching with KOH + IPA and TMAH + Triton are shown on the page Figures 3.11 and 3.12. Differences in etch planes due to the addition of surfactants are made visible in Figure 3.13.

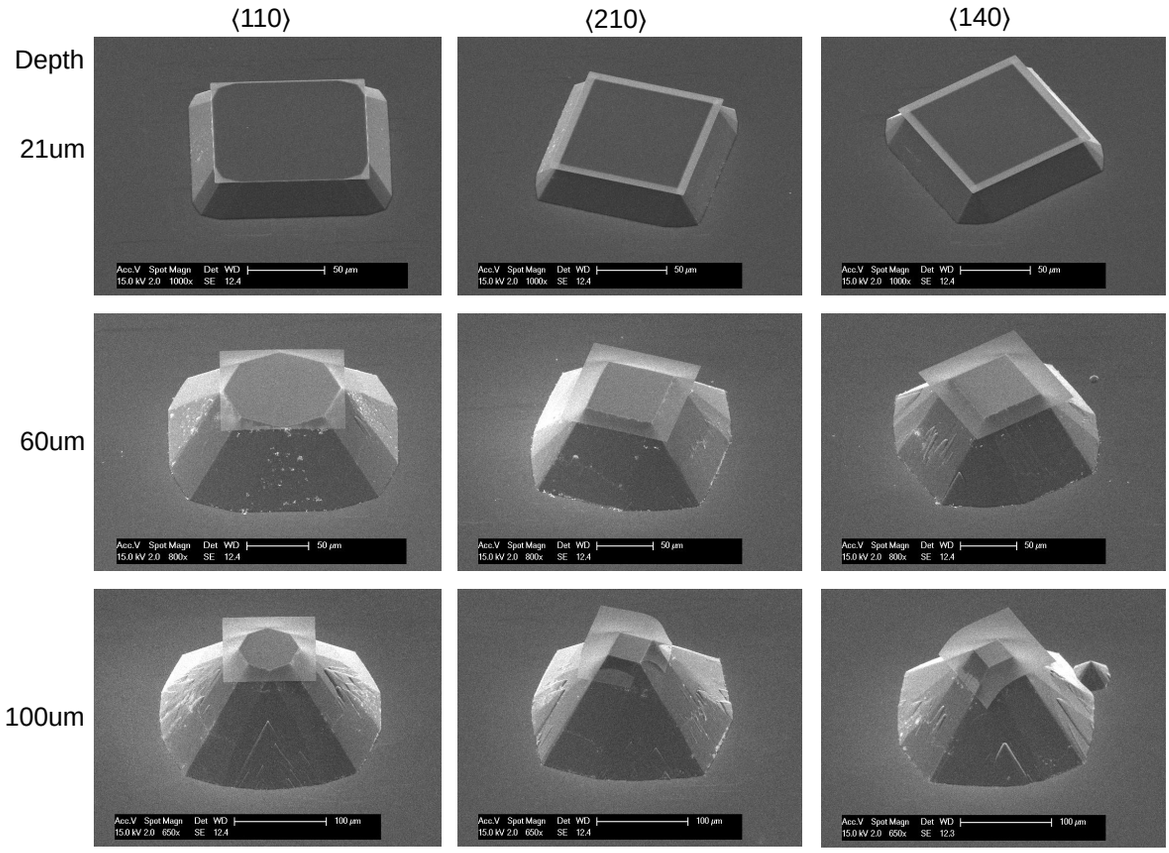


Figure 3.11: Crystal rotation structures etched in 8.5M KOH + IPA solution.

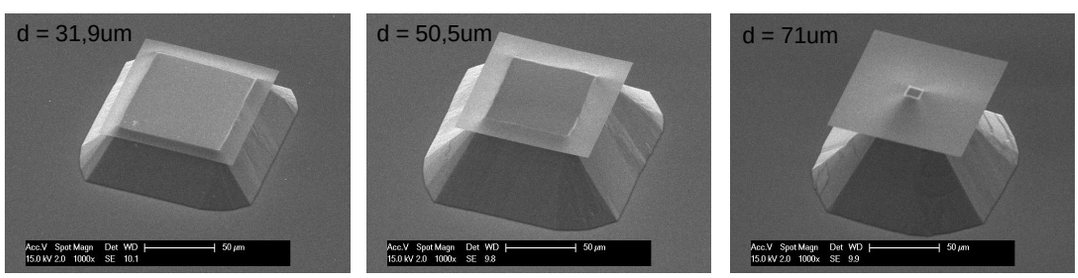


Figure 3.12: Crystal rotation structures etched in 25% TMAH + Triton solution.

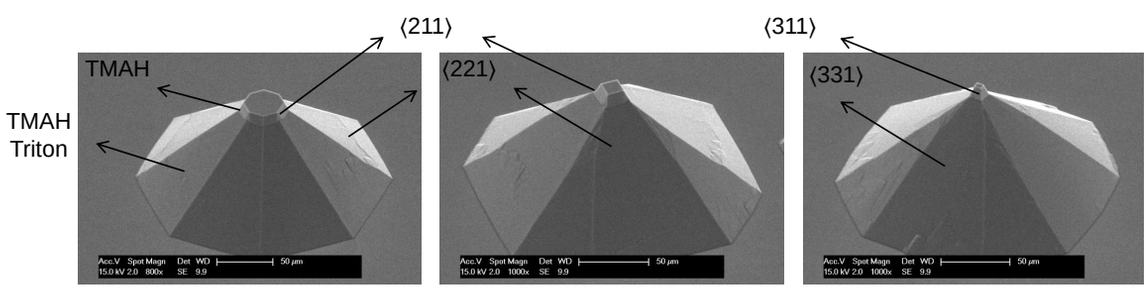


Figure 3.13: Different etching planes with TMAH and TMAH + Triton etching.

4

Microelectrode patterning by sidewall lithography

After manufacturing the 3D electrodes and growing a SiO_2 passivation layer, the metal interconnect has to be placed on the structures. It is chosen to sputter a 40 nm/200 nm-thick Ti/TiN layer with the Trikon Sigma 204 Dealer. The thin Ti layer is added for adhesion purposes. To pattern the facets of the structures, positive diluted AZ9260 photoresist is spray-coated on the wafer, acting as a mask for dry etching with the Trikon Omega 201 to reveal the metal patterns. To ensure proper bonding to the PCB, 600nm aluminum pads are placed on the edges of each chip. A detailed overview of the mask set used for fabricating the 3D microelectrodes and their interconnect can be found in Appendix A.

It is well known that patterning structures on wafers is highly suitable for 2D lithography but becomes increasingly difficult when implementing high aspect ratio 3D structures. Patterning, for example metal wire interconnect over long titled sidewalls, cannot be accomplished by regular lithography steps using spin-coating and standard exposure. Spray-coating and Multi-Step Imaging (MSI) are methods specially designed to pattern high topography wafers. As indicated by Chapter 3, TMAH + Triton etching the microstructures gave the most promising results. Therefore, it was chosen to (and due to time constraints) perform all silicon etching with a TMAH + Triton solution. An overview of the microelectrode array, after etching up to a depth of approximately 85um, is shown below in Figure 4.1. Results show 20 octagonal structures with no visible defects on the structures facets or the bottom plane.

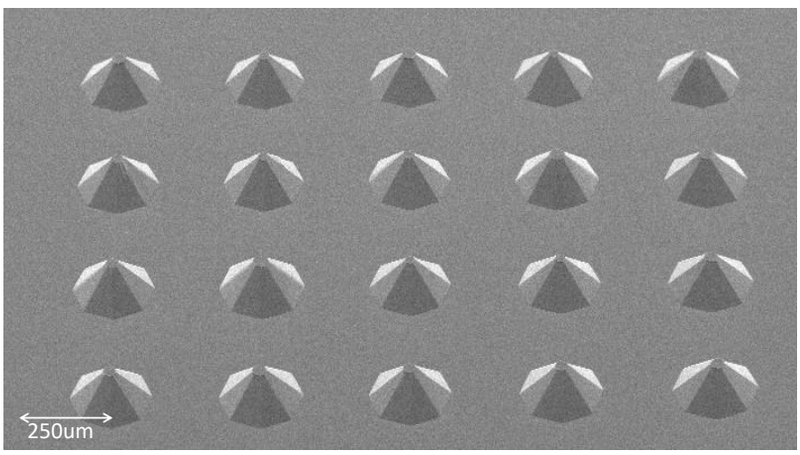


Figure 4.1: TMAH + Triton etched microelectrode array.

4.1. Multi-Step Imaging

The pattern resolution, numerical aperture of the lens and the depth of field are related to each other by equations shown in Equation 4.1 and 4.2. Current systems often have a fine resolution which is ideal for planar surfaces but limits the fabrication for 3D topography. The finer the resolution, the smaller the depth of field, meaning the smaller the height region that can effectively and accurately be patterned (as shown by the Equations 4.1 and 4.2 [78]. In these equations, R is the resolution, λ the wavelength, NA numerical aperture, and DOF the depth of field.

$$R = \frac{\lambda}{2NA} \tag{4.1}$$

$$DOF = \frac{\lambda}{NA^2} \tag{4.2}$$

Due to this effect, it is highly challenging to manufacture high aspect ratio structures with one lithography step. Multi-Step Imaging (MSI) implements the fact that only a certain height region of a photo-polymer is developed due to the focal plane of the projection tool. By changing the focal distance of the, for example, ASML wafer stepper, different regions of the sidewalls can be exposed and patterned [16].

This method was proposed and tested with high aspect ratio structures (up to 200um height) in the PhD thesis project of Z. Kolahdouz Esfahani at the TU Delft [16]. The focus range for the ASML 5500 wafer stepper was found to be around 18 um, and therefore the height of the pillars were divided in 35 um sections, resulting in eight different focal regions. An additional precaution was taken to ensure wire connectivity throughout the whole sidewall by overlapping the regions with 1 um.

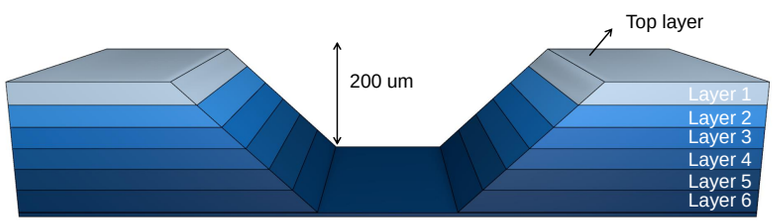


Figure 4.2: Schematic showing the different focal planes.

Figure 4.2 shows a representation of a split masks for exposing high topography structures. Each mask (with its own focal plane) is indicated by its own color. The cavity was created by wet etching of silicon. Results with only exposing the even numbered focal layers (thus not enough) are shown in the right part of Figure 4.3. It shows that not all height regions were exposed properly and the wire connections are not yet completely isolated from each other. This method shows the feasibility of multi-step imaging and patterning steep angled sidewalls, which could be an extremely useful method for fabricating the multiple isolated conductive rings/pads on the high topography electrodes.

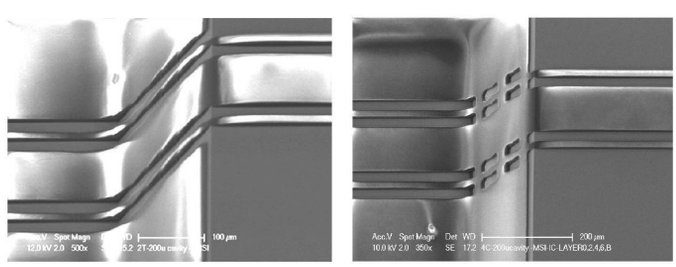


Figure 4.3: MSI results when implementing only even and all numbered focal planes.
Image reproduced from PhD Thesis Z. Koladouz Esfahani (2017) [16].

When the design lacks small features, the need for several focal regions is not strictly necessary. It was shown in previous studies that pitches (distance between features) larger than 20 um and line thicknesses over 10 um would still be successfully patterned on the entire sidewall in a single exposure (using negative NLOF photoresist on height differences up to 200um) [16]. The result is depicted in Figure 4.4, where it can be seen that a pitch too small results in overlapping structures.

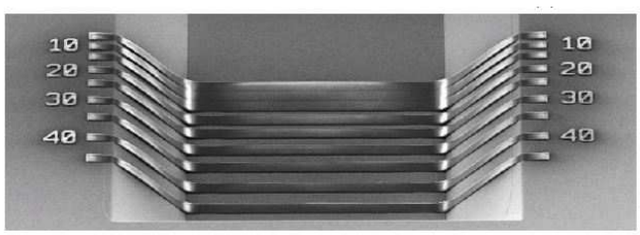


Figure 4.4: Sidewall patterning using a single mask and focal plane.
Image reproduced from PhD Thesis Z. Koladouz Esfahani (2017) [16].

4.2. Spraycoating

To achieve homogeneous resist layers, (multi-layer) spray-coating is used to deposit the resist on high aspect ratio structures. The resist is aerosolised by an ultrasonic atomizer and sprayed over the high topography wafer with a spray nozzle. The wafer rotates slowly and ideally all small droplets of resist remain on the place where they initially made contact with the wafer. Due to the rotation of the wafer and the precise pressure of the nozzle, the resist thickness should be as homogenous as possible [17]. This method yields far greater homogeneities (with high topography wafers) as with its alternative spin coating where the resist builds up next to the large surface topologies. However, several key aspects have to be fine-tuned to create a working recipe:

- The viscosity of the liquid. If the viscosity is too low, the drops can move from its initial landing point. The current mixture for this project is 30gr resist :50gr PGMEA : 240 MEK. If the density is too high, it cannot be atomized and sprayed.
- The pressure of the sprayed solution and the wafer-nozzle distance. A study showed that the nonuniform resist deposition could be caused by the horizontal air flow in the wafers vicinity [31]. The proposed method to minimize this effect was implementing a spray shield with a narrow aperture.
- The amount of sprayed diluted photoresist per second (ul/sec).
- The thickness of the final layer: Too thin a layer causes no resist coverage on the convex corners. Too thick a layer causes deep resist puddles in the bottom concave corners.
- The adhesion of the photoresist to the wafer surface. Adhesion agents can be used to promote better adhesion to silicon or metallic surfaces.

The EVG101 spraycoater is used for coating the TMAH-etched wafers. Beforehand, the wafers are baked on 115°C for 10 minutes to ensure all moisture is removed from the wafer. This step is immediately followed by an HMDS treatment, before coating the first layer. If multiple coating steps are needed, 2 minute soft bakes are performed at 115°C, followed by a final 5 minute 115°C bake out step if the coating has finished. Due to the high topography of the wafer, the diluted photoresist will 'puddle' in the lower concave corners and form thick layers (compared to the top resist layers) and cause large thickness differences throughout the wafers topography. The transition between the top surface and the etched slope (convex corner) also shows thinner layer deposition (see Figure 4.5 for spraycoated resist thickness layers).

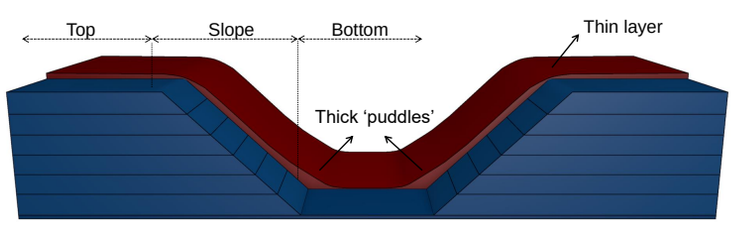


Figure 4.5: Spray-coated positive photoresist layer thickness for high topography structures.

4.2.1. Layer thickness

Thicker layers of photoresist cause the 'puddling' effect to worsen and make exposing the photoresist more difficult. After multiple experiments, increasing the amount of sprayed resist from roughly 3ul/sec to 10ul/sec caused the complete structures to be covered with resist. The top resist layers were around 3um, with a thin <1um layer on the convex corners and roughly 10um thick 'puddles' on trench bottom sides. The thickness differences are depicted in Figure 4.6.

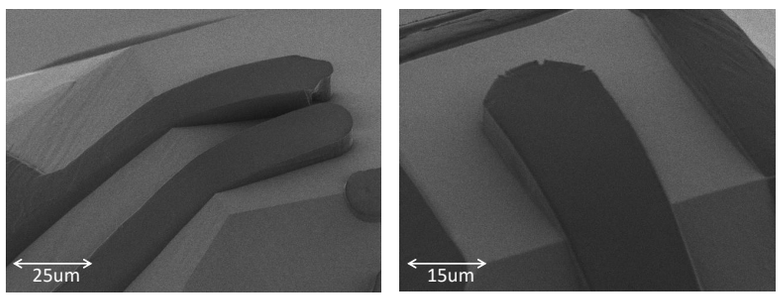


Figure 4.6: High topography spraycoating, showing large thickness differences.

4.2.2. Exposure dose

Exposing is done with the EVG420 contact aligner (wavelength h-line 405 nm). Due to the fact that the thick puddles at the bottom of the trenches (100um lower than the set focus point) need a higher dose than the thinner top resist layers, multiple experiments were performed to find a proper exposing dose (between 300 and 1100 mw/cm^2). When exposing on reflective surfaces (like aluminum), it is advised to expose with 80% of the original dose due to the additional reflections. It was found that a minimum dose of 950 mw/cm^2 was needed to completely expose the 'puddles'. The results of different exposure doses are shown in Figure 4.7. Increasing the dose from 300 to over 950mw/cm^2 yielded the results of uninterrupted lines over TMAH etched trenches, but minimum width/gap sizes remained relatively constant. The longer exposing did not result in noticeably thinner resist lines.

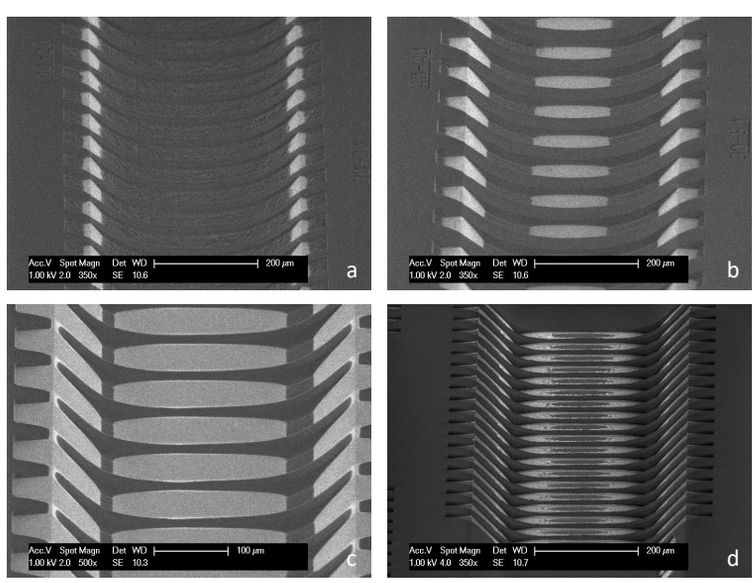


Figure 4.7: Sidewall lithography with different exposure doses. (a)-(c) increasing exposure dose but 'puddles' remain undeveloped. (d) fully correct exposed/developed test lines. Damage to 600nm aluminum layer is visible after 40 lithography cycles during test phase.

4.2.3. Developing

The photoresist was developed with AZ400K. Originally, the development was performed in undiluted AZ400K for 10-40 seconds. It was noticed that at short development times the actual removed photoresist kept on growing but after a while the resist remained unchanged. Line width and gaps remained relatively constant with increasing developing times. Increasing the exposure dose helped with exposing also thick layers of resist but did not visibly change the minimum line width/gap of the resist. It was noticed than when developing with the undiluted AZ400K, the original line widths decreased up to 50%. This effect is shown in Figure 4.8. It was thought that undiluted AZ400K developer could be less selective and therefore also removes some photoresist laterally. Diluting the solution gave the advantage of longer development times (which gave more control) and possibly higher selectivity. The resist was diluted to a 1:2 ratio (100ml developer, 200ml diwater) which gave develop times of 3-4 minutes. Results showed that the lateral removal of resist with diluted developer was slightly smaller (≈ 30%).

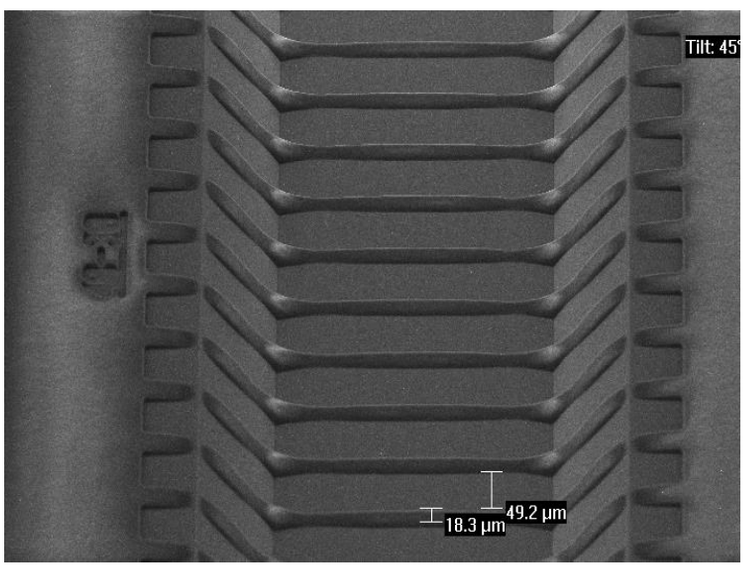


Figure 4.8: Effect of developing with undiluted AZ400K on TMAH etched sidewalls. Mask width/gap 40/30, actual width/gap ≈18um/50um.

4.2.4. Minimum line-width and gap

Due to large height differences, the developed line thicknesses varied greatly moving away from the focus point. Minimal line width and gaps were experimentally determined and categorized in three sections: top, slope, bottom. The top part of the pyramid will be in focus and the smallest resolution is possible here.

The slope of the etched structures (see Figure 4.5) steadily moves away from the focus point and the resolution will degrade and larger widths and gaps are necessary to ensure proper connections. Finally, the bottom part will be at a depth of 100um and the mask sizes will become thinnest here. Therefore, the minimum width/gap sizes are summarized in Table 4.1. Because specifications allowed it, larger widths and gaps were chosen to ensure proper connection. Some results of different line thickness on the three regions are shown in Figure 4.9. The figure clearly shows the effect when a line width of <25um is chosen. The bottom resist lines are too thin and will be completely removed. It is worth mentioning that in Figure 4.9 the wafer had seen already more than 40 lithography cycles (cleaning, coating, exposing, developing, SEM). Therefore, the original aluminum surface on the wafer had degraded already and was partly removed. The lines were completely free and the darker areas between the lines partly show the silicon layer underneath. Figure 4.11 shows this more clearly.

Because three independent electrodes had to be placed on the pyramids, it was also possible to have each electrode on the same facet, but the connection to the base of the chip on different slopes, as shown in Figure 4.10. The advantage of this method is to minimize the risk of unwanted connections at the concave bottom corners.

Table 4.1: Experimentally determined minimum line width/gap sizes.

	Width [um]	**Gap [um]**
Top	10	>2
Slope	15	>2
Base	25	>7

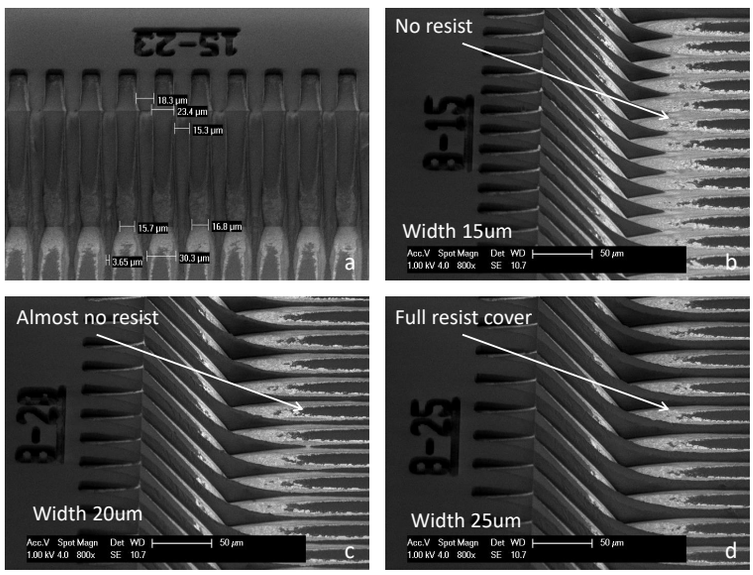


Figure 4.9: Different line widths in the three regions: top, slope and base. (a) Clear visible width differences at bottom of trench. (b)-(d) gap of 8um, width between 15 and 25, showing a minimum bottom width of 25 is necessary.

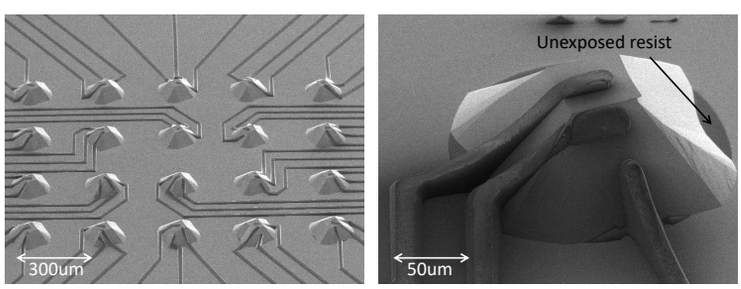


Figure 4.10: Measure points on same slope, interconnect on different facets to minimize the risk for unwanted connections by unexposed resist due to thick resist 'puddles'.

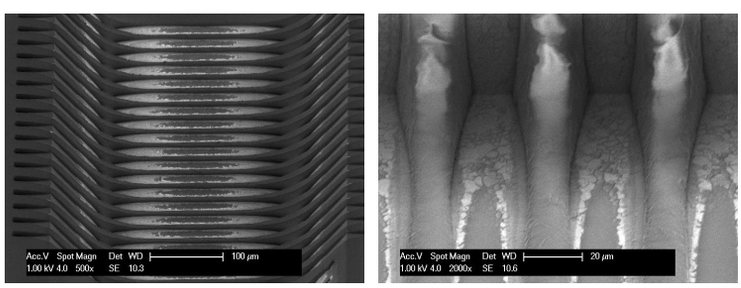


Figure 4.11: Degraded thin aluminum layer after many lithography test cycles.

4.3. Main process for microelectrode fabrication

The final 3D microarrays were manufactured on silicon dies of 2 by 2cm and assembled onto PCBs conforming to MEA readout standards. Each chip features 20 truncated pyramids with a height of ≈85um, including three distinct vertically stacked measuring points. The structures were aligned in the center of the chip in an area of $\approx 2.5mm^2$. 40/200nm Ti/TiN measuring pads and interconnect was deposited, where all sample points can be individually wire-bonded to the 60 PCB pads. A plastic/Teflon ring can be placed on the center of the chip to allow for in-vitro measurements. The final process for fabricating the microelectrodes and patterning the metal interconnect is summarized below:

- Deposit 300nm silicon nitride hard mask
- Etch wafers in 25% TMAH + ≈0.25v/v% Triton at 80°C with etch rate ≈0.4um/min
- PECVD Deposition of 200nm Silicon oxide as a passivation layer (no mask needed)
- 600nm aluminum sputtering for the bond pads in the Trikon Sigma
- Pattern with 8 layers of spray-coated diluted AZ9260 photoresist (5ML total, ≈ 10ul/sec)
- Lithography EVG420 with a dose of 950mwatt/cm^2 and 4min AZ400 development (ratio 1:2 DI-water)
- 40/200nm Ti/TiN deposition for interconnect and measure-pads
- Pattern with 8 layers of spray-coated diluted AZ9260 photoresist (5ML total, ≈ 10ul/sec)
- Lithography EVG420 with a dose of 950mwatt/cm^2 and 4min AZ400 development (ratio 1:2 DI-water)
- PECVD Deposition of 300nm Silicon oxide as a passivation layer of interconnect. Only bond pads and measure-points are open

Due to high aspect ratio lithography, over-etching, and over-developing, final interconnect widths are thinner than their original mask sizes. The smallest metal tracks patterned on the slanted facets were 12 um-wide with minimal inter-track gap of 5 um. Because only single mask lithography steps were used, smaller feature sizes were difficult to achieve. Due to the large focus offsets, the line widths had to be increased at the bottom of the structures to ensure proper connection over the entire structures. This caused for the possibility to have small measuring points on the facets, and wider interconnect lines leading away from the electrodes to the PCB connections. Due to spray-coating homogeneity difficulties, best results yielded in the outer regions of the 4" wafer. Due to thicker resist puddles in the middle of the wafer (see Figure 4.12), some unexposed resist puddles remained on the wafer, damaging further steps. Figure 4.13 shows the first produced microarray with 20 structures and their individual sampling points. A close-up SEM figure of the individual sampling points in shown in Figure 4.14, and more results are shown in Appendix E.

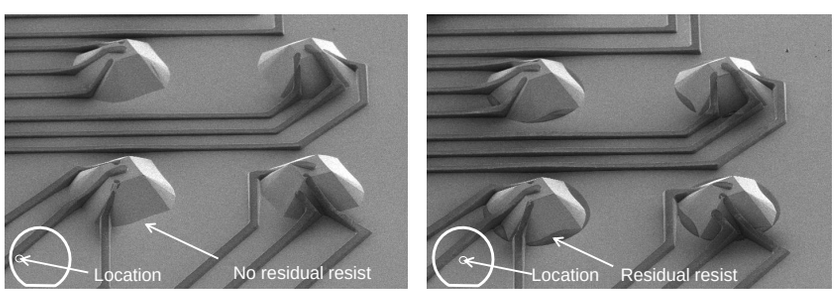


Figure 4.12: Spray-coat homogeneity differences on the wafer.

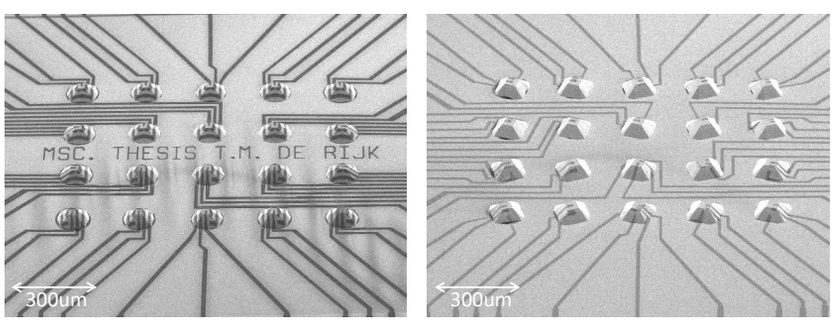


Figure 4.13: First results of the 3D array of of 20 microelectrodes.

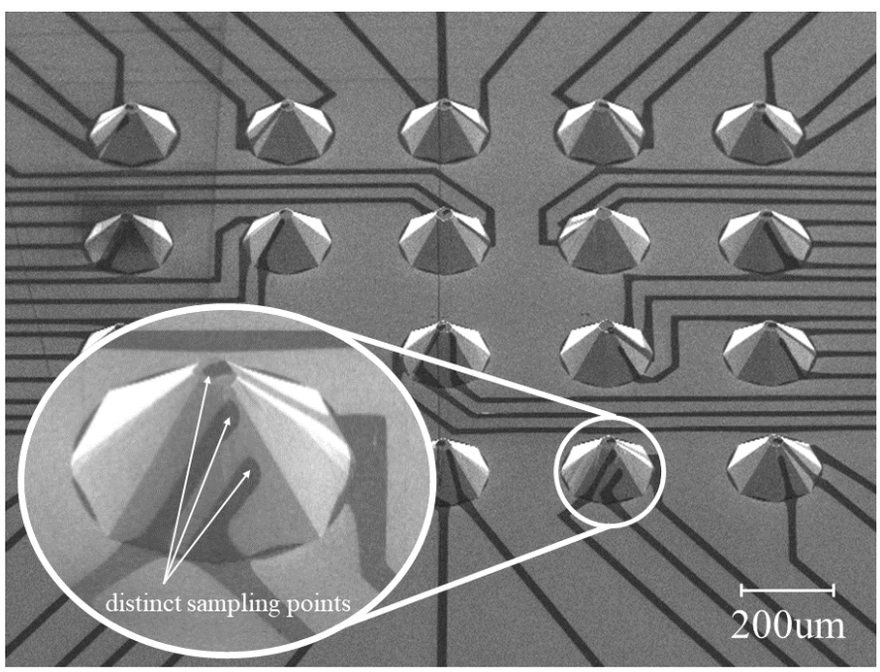


Figure 4.14: SEM micrograph of a 3D array of 20 microelectrodes. Each micro-pyramid in the array is 85 um-high and features three distinct and vertically stacked microelectrodes (see inset).

5

Assembly and measurements

This project aims to fabricate a measurement platform where it will be possible to measure neuron responses on different height levels, which differ from current planar/single electrode measurement arrays of multi-channel systems. The MEA platform which was used as a reference and is shown in the left part of Figure 5.1. To utilize the wafers surface more efficiently, the chip size is reduced to roughly 2x2cm. The small chip will be wire-bonded onto a larger PCB to meet the same dimensions as the MEA devices (right part of Figure 5.1). Due to the unforeseen circumstances caused by the Covid-19 crisis, the final assembly of the chips on the PCB was not possible in the time-span of this research.

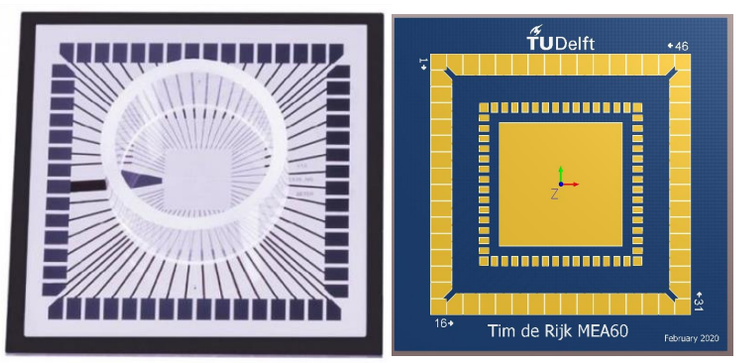


Figure 5.1: Microelectrode array. Left: Current Multichannels MEA array. Right: PCB design to correspond to MEA dimensions with wirebonded chip in center.

Instead of performing the 'in vitro' tests at the Leiden Medical University, several impedance measurements were performed to investigate whether a connection can be detected between the outer bond pads (at the border of the chip, used for wire-bonding) and the electrodes on the structures. The wafer was placed on the Probe-station Cascade Microtech 33 for electrical characterization of the 3D electrodes. One needle is placed on the outer pads, the other on top of the electrode. A voltage was swept over de electrodes and the current was measured and plotted in Figure 5.3. The top figure shows a low Ohmic response (as expected) when performing a test measurement on the same large bond pad. However, measuring between the pad and electrode, the currents are small (bottom figure). An interaction was still clearly visible as can be seen from the figure, but the impedance is large. It was already noticed with the SEM that some metal connections between the top base of the structure and the slope (see Figure 5.2) were not completely perfect. Scraping with the probe on the small and thin structures could have damaged the interconnect even more. And because the probe-needle had roughly the same size as the top base of the structures, visibility while placing the needles was slim. Additionally, multiple electrodes were positioned on the slopes of the structures. This made positioning highly difficult due to the fact that under the microscope, tilted structures are not visible and appear black on the screen and microscope.

A silicon-oxide layer was deposited on the wafer as a passivation layer. The electrodes and bond pads were etched free with the Trytek Triode 384T. A test wafer was added to measure the oxide removal rate of the Drytek to ensure that the Ti/TiN interconnect was not damaged. Visible inspection clearly showed that the oxide layer was successfully removed on the electrodes and bond-pads because the typical titanium gold color appeared again (see right side of Figure 5.2). However, it was noticed that not all oxide was removed evenly on the structures. The gold color was not everywhere perfectly visible, some darker spots remained. Therefore, it is thought that when measuring the impedance on such places, the residual oxide can act as a blocking layer.

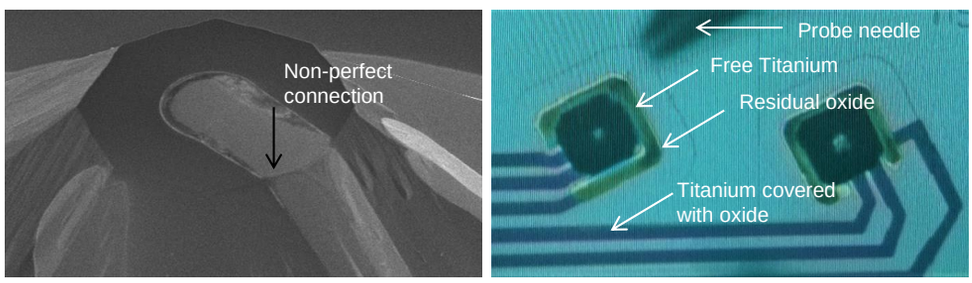


Figure 5.2: Possible in-proper connection between top base and slope. Slopes of structures are not visible under the microscope.

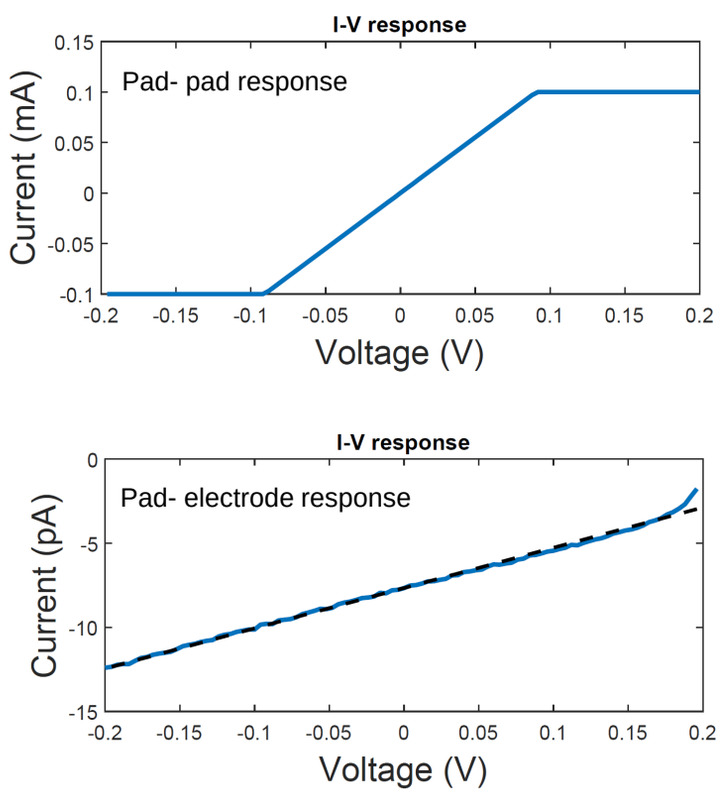


Figure 5.3: Connectivity measurements. Top figure shows the expected low impedance when measuring on the same bond pads. Bottom figure shows high an ohmic connection between outer bond pad and top electrode.

6

Conclusion

The research goal of this master thesis was to develop a 3D micro-electrode array suitable for measuring the electrical responses of clustered neurons at three different height levels, compatible with standard MEA platforms.

This thesis focused on fabrication truncated micropyramids and patterning the facets of the structures with sidewall lithography techniques. Several etch solutions were investigated, both with and without surfactants to possibly improve etch results. Surfactants (IPA and Triton) improved the surface roughness but changed the etch planes from ⟨h11⟩ to ⟨hh1⟩, resulting in less steep slopes. Rotating the structures away from the ⟨110⟩ crystal plane removed the critical need for implementing large corner compensation structures at mask corners to protect the convex corners. Increasing the rotations to ⟨310⟩ plane decreased the removal of convex corners and yielded in smoother etch planes. Regular corner compensation structures like the 'double-square' technique also resulted in truncated micropyramids, but due to difficulty in controlling the lateral etch rates in solutions with surfactants, this option was more difficult. More testing with multiple mask sizes could enable future versions to also implement this technique. However, this technique will always be very dependent on the sizes of the corner compensation structures, and therefore has only a small etch depth window. Structures rotated along the ⟨h10⟩ are far less depth limited. Etching deeper will result in gradual loss of the convex corners, but for higher crystal rotations these effects become even slower.

Diluted AZ9260 photoresist was spraycoated on the 3D structures with an HMDS pre-treatment to promote adhesion (especially to the convex corners where resist was thinnest). The resist was exposed with a dose of 950mwatt/cm^2 to fully expose all resist regions. Lower dosage showed an inability to expose thick resist puddles, resulting in unwanted connections between interconnect lines.
The resolution changes on the electrode surfaces due to the large height difference. The focus offset causes (with single mask exposure) feature sizes that are properly in-focus on top to be gone at the bottom. Therefore, it was chosen to widen the interconnect lines running down the facets to the bottom surface of the chip to ensure a proper connection (or even run all interconnect lines on different facets). Slope widths had to be >15um to provide connections over the complete height interval. Due to 'puddling' effects at the concave bottom corner, thicker interconnect lines started several um away from the base of the structures. Experiments showed a minimally needed interconnect width on the bottom of 25um.

Final results showed a microelectrode array with height differentiated independent measurement points. Twenty 85um tall truncated pyramids or octagonal structures were placed in a $\approx 2.5mm^2$ with 200um inter-structure distance. Smallest interconnect lines prove to be 12um (due to over-exposing and over-developing, smaller than original 15um mask width) with an inter-track gap of 5um. The chips will be cut in 2x2cm dies and assembled onto PCBs compatible with current MEA readout circuits. It is expected that these innovative 3D MEAs are able to measure responses of 3D neuronal networks from hiPSC-derived cortical neurons.

7

Future work and recommendations

This report was written as part of the thesis work for the master Electrical Engineering at the TU Delft. Due to the large impact of the Covid-19 crisis, fabrication of the 3D microelectrodes was delayed. Immediately after the 'version 2' masks were delivered, the first effects were already noticeable. Long cleanroom days just before the crisis yielded in first results showing that the concept is valid and fabrication of height differentiated measurement pads on single microstructures is possible. However, more testing and PCB assembly was not possible anymore due time constraints. Several remarks and propositions for future work are addressed below which hopefully will result in measuring responses from clustered neurons at different heights.

Surfactance influence. Adding Triton to the TMAH solution caused the lateral etch rate to decrease drastically. However, it was noticed that when adding Triton to the point of saturation, the lateral etch rate increased again. Older TMAH also showed signs of increased lateral etch rates, which made the precise determination of beginning mask sizes for the microstructures difficult. Fine-tuning the etch rates was possible by changing the bath temperature (higher temperature decreased lateral etch rates) but more experiments with exact Triton concentrations could help to determine exact etch rates for all implemented crystal rotations (⟨h10⟩, h>1).

AZ9260 Photoresist. This type of photoresist is currently not manufactured/sold anymore due to health concerns. This would mean that in the near future new resist types should be used for spray-coating on the high topography wafer structures. New tests should be performed to find a process that allows for good step coverage. Negative photoresist could prove to be an advantage due to the reported lessened 'puddling' effects at the bottom concave corners. Because the spraycoater EVG120 was equipped with positive diluted AZ9260 photoresist, it was chosen for this project. This choice was additionally based on an intensive literature study showing the feasibility for patterning high topography structures with this resist type.

Crystal alignment. The alignment for the crystal rotation structures is crucial to yield proper etch planes. Implementing measurement structures to determine the crystal miss-alignment between the wafers flat and the silicon crystal showed to be possible by adding several simple structures on the wafers surface. Utilizing the wafer-stepper to align all masks and possibly implementing a pre-rotation to compensate for the miss-alignment could result in better spatial control and resolution. Additionally, resolution could be improved by implementing multiple focus region masks instead of a single wafer covering the complete height interval.

PCB assembly and neuron measurements. Future work should include placing the chip on a PCB and wirebonding the chip pads to the PCB. As discussed with the team from the Leiden Medical University, a protective ring will be placed on the chip allowing for a liquid to be placed on the chips. Measurements should hopefully prove the feasibility of measuring distinct and vertically stacked neuronal responses. After the first 'in vitro' results it should be possible to further specify several parameters like interconnect dimensions, metal thickness and electrode impedance. First measurements results show the interaction between the outer pads and the electrodes. But, extra care has to be taken to completely remove the oxide passivation layer.

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A

Quartz 4" reticle design

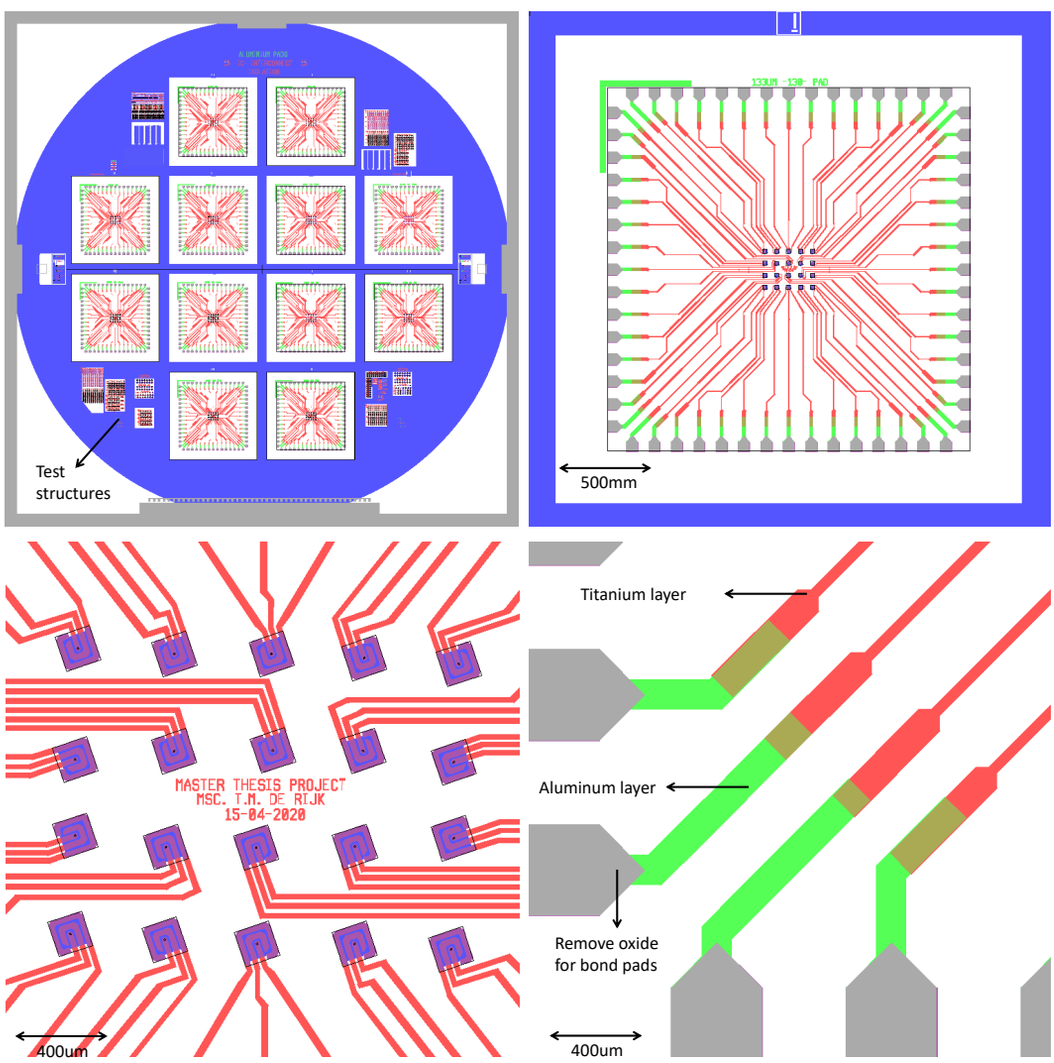

Figure A.1: Wafer mask set: overview and detailed structures.

B

KOH and TMAH etch rates

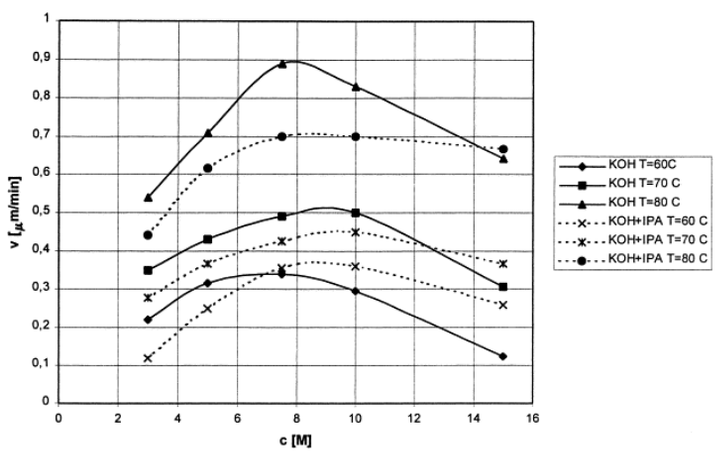

Figure B.1: KOH etch rate versus KOH concentration [82].

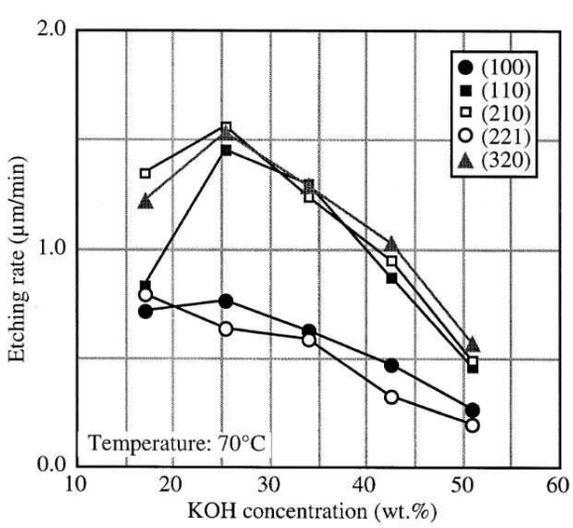

Figure B.2: KOH etch rates for different crystal planes [58].

B

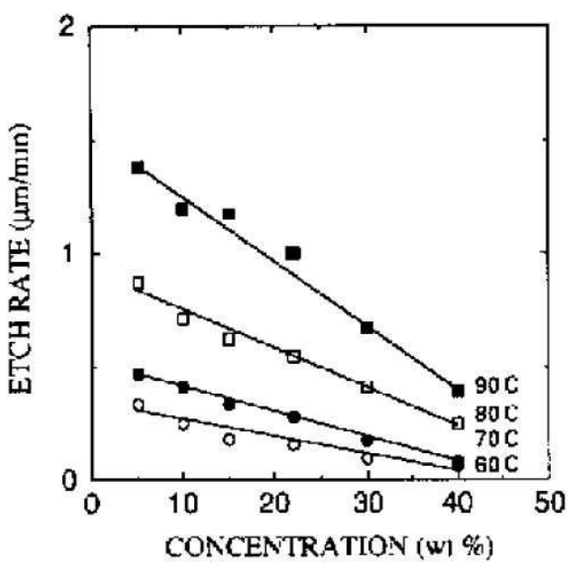

Figure B.3: TMAH etch rate versus concentration [66].

C

Cleanroom machines and equipment

To fabricate the proposed 3D electrode structures, additional cleanroom training in the EKL cleanroom is required. This is an extensive one-week training which results in that one can enter the cleanroom and partake in the 'standard processes'. During this training the safety precautions are shown and a standard BICMOS process is followed where all the tools are demonstrated and explained. For more exotic equipment and materials, additional training is needed. Some additional training sessions, which can take up a few days, are SEM training, KOH wet etching, manual contact aligner, and manual spin/spray coating. A complete list of equipment I was trained for and used this project is given below.

Tanner L-Edit IC Layout:	Reticle design software
EVG120 Coater-Developer:	Automatic coater and developer station
ASML PAS 5500/80:	Automatic wafer alignment and exposure tool
EVG420 Contact Aligner:	Manual alignment and exposure tool
Drytek Triode 384T:	Dry etching oxide/nitride layers
EVG101 Spray-coater:	Spray-coating for high topography wafers
Rinse & Dryer Si Cleaning line:	Used for cleaning wafers
Single Wafer Dryen SPIN 150:	Used for drying single wafers
Tepla Plasma 300:	Microwave Plasma System used for stripping resist after development
Leitz MPV-SP Microscope:	Automatic film thickness measuring system
SEM Philips XL50:	Scanning Electron Microscope used for inspecting the 3D structures
Trikon Sigma 204 Dealer:	PVD metal deposition tool
Trikon Sigma 201:	Dry plasma etching tool
LPCVD Furnaces:	Used for deposition (e.g. Silicon Nitride)
Keyence VK-X250:	Optical microscope used for determining etch depth and surface roughness
Dektak 8:	3D Profilometer
Novellus Concept 1:	PECVD machine for Silicon oxide deposition
Acetone bath:	For cleaning resist of wafers
Manual HMDS coating:	Manual coating HMDS adhesion layer before spray-coating
0.55% HF bath:	Remove native oxide from the SI Surface
157°C Hot phosphoric acid	Wet etch silicon nitride hard mask
Manual development:	Manual development with AZ400K
Probe-station Cascade Microtech 33:	For electrical characterization of the 3D electrodes

The etch solutions were all differently prepared and although all solutions are toxic (for inhalation and in contact), handling with TMAH asked for even more cautiousness.

KOH solution The KOH solution was made by slowly adding KOH tablets in demi-water until the determined concentration was reached. The exothermic reaction between KOH and water caused the solution to heat up quickly. Adding the tablets slowly and contentious stirring yielded in a transparent KOH solution at the predetermined temperature. The magnetic stirrer was used to ensure homogenic etching and the solution was slowly heated (and kept) to the desired temperature with a hotplate connected to a thermocouple.

KOH + IPA solution The same procedure was performed as the KOH solution. If the specified temperature and concentration was reached, IPA was added to the liquid (maximum temperature of the solution due to the IPA is now 75°C) until a thin layer IPA formed on the solution. It was checked that this layer was present at all times during etching to ensure the IPA concentration was always at the same level.

TMAH etching The TMAH solution is directly delivered in the cleanroom in liquid 25% TMAH in water form. Additional care was taken with handling and during etching due to the increased health risks.

TMAH + Triton The same 25% solution was taken for these experiments and after the correct temperature was reached, several drops of Triton were added to the solution. As only a small amount of Triton is needed in the solution (it saturates at roughly 0.25%v/v), it was chosen to perform two different experiments: A Triton saturated solution (indicated by small un-disolved 'soap' spheres in the liquid) and a low Triton concentration liquid.

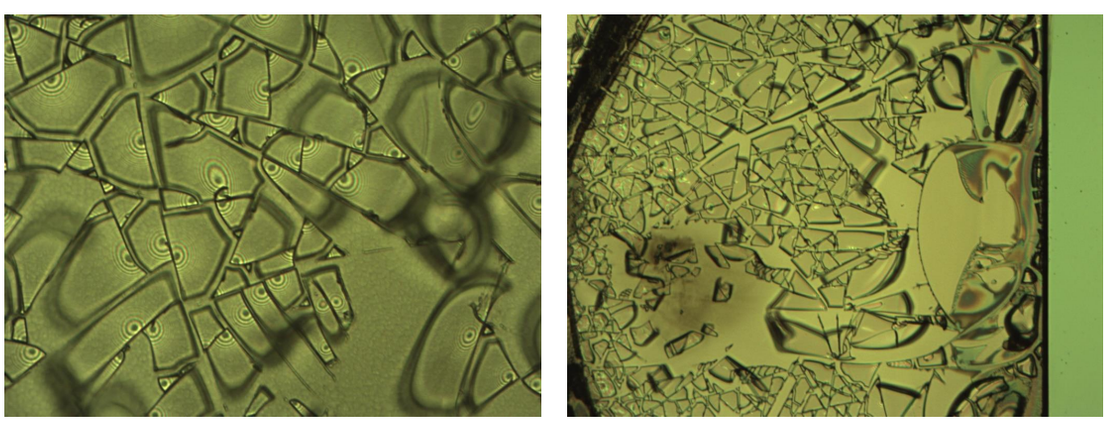

Figure C.1: Silicate layer forming after partially submerged wafer etching..

D

Developed crystal plane surfaces after etching

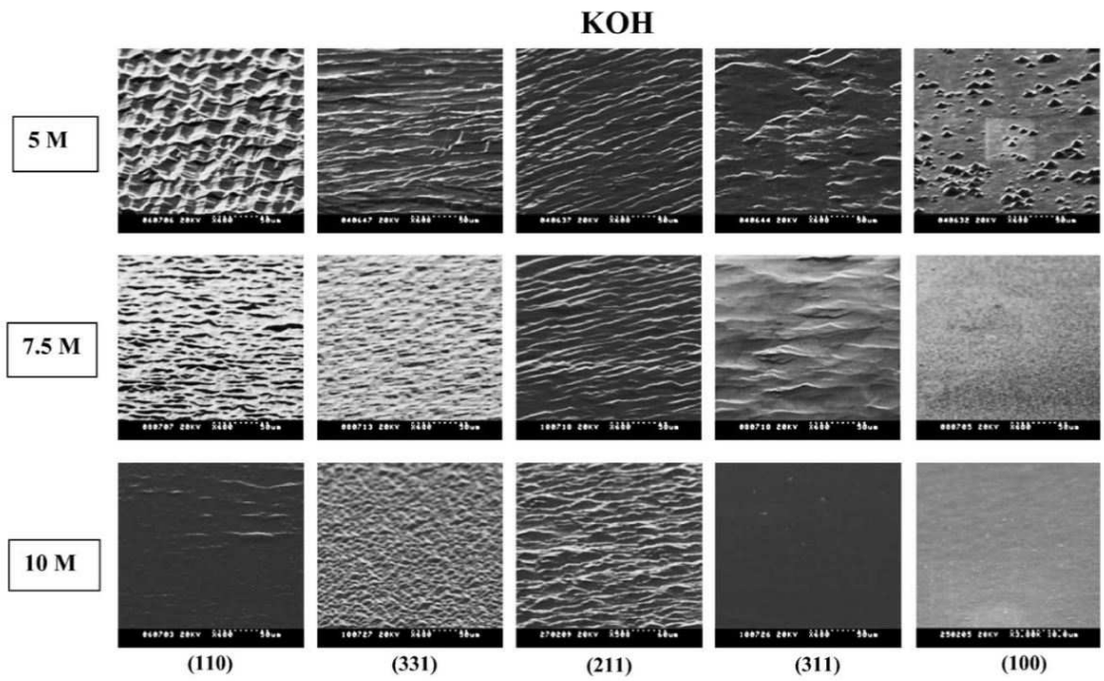

Figure D.1: Different crystal plane surfaces after KOH etching. Image reproduced from Zubel et al. (2004) page 3 [81].

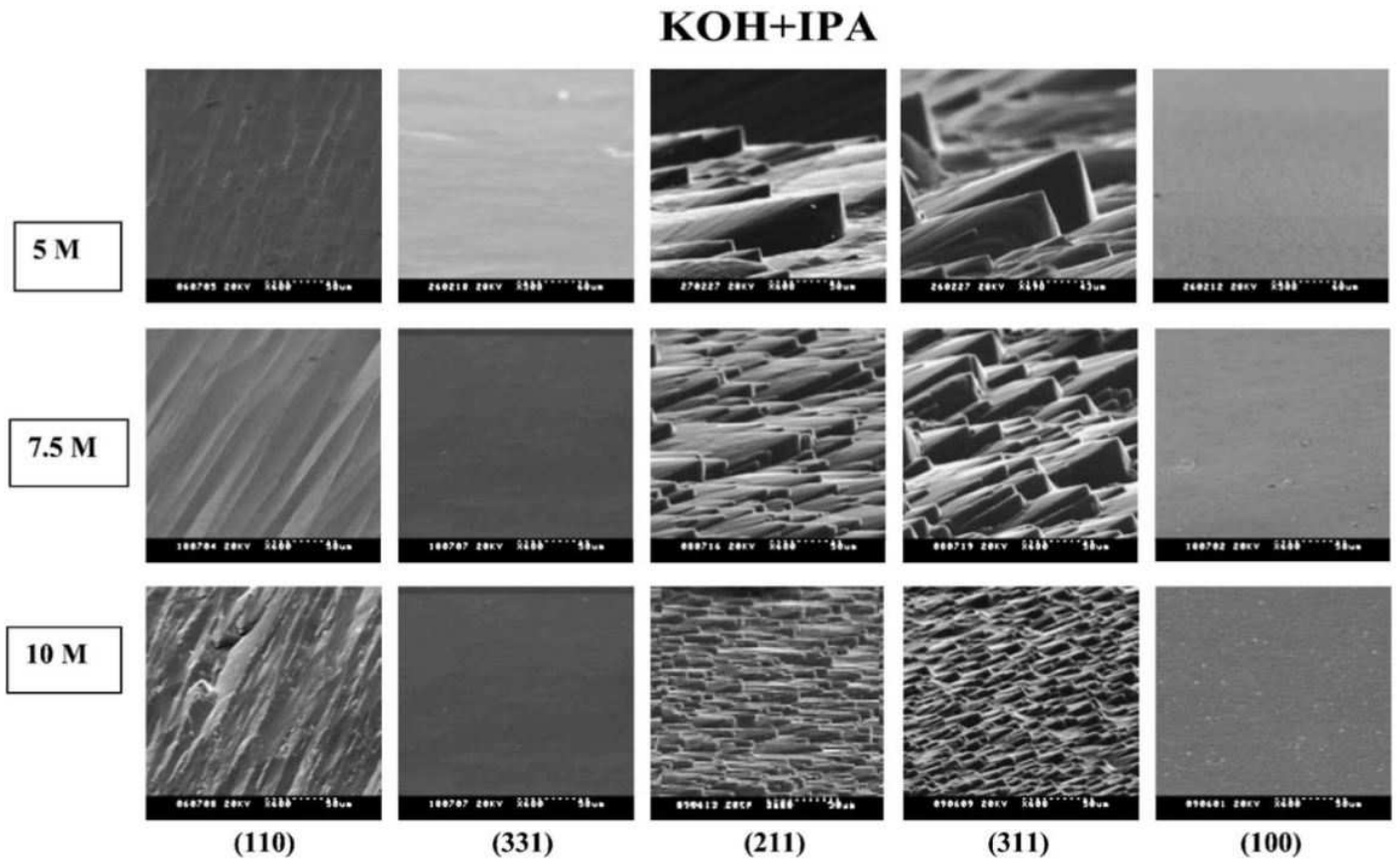

Figure D.2: Different crystal plane surfaces after KOH + IPA etching. Image reproduced from Zubel et al. (2004) page 3 [81].

E

3D electrode patterning results

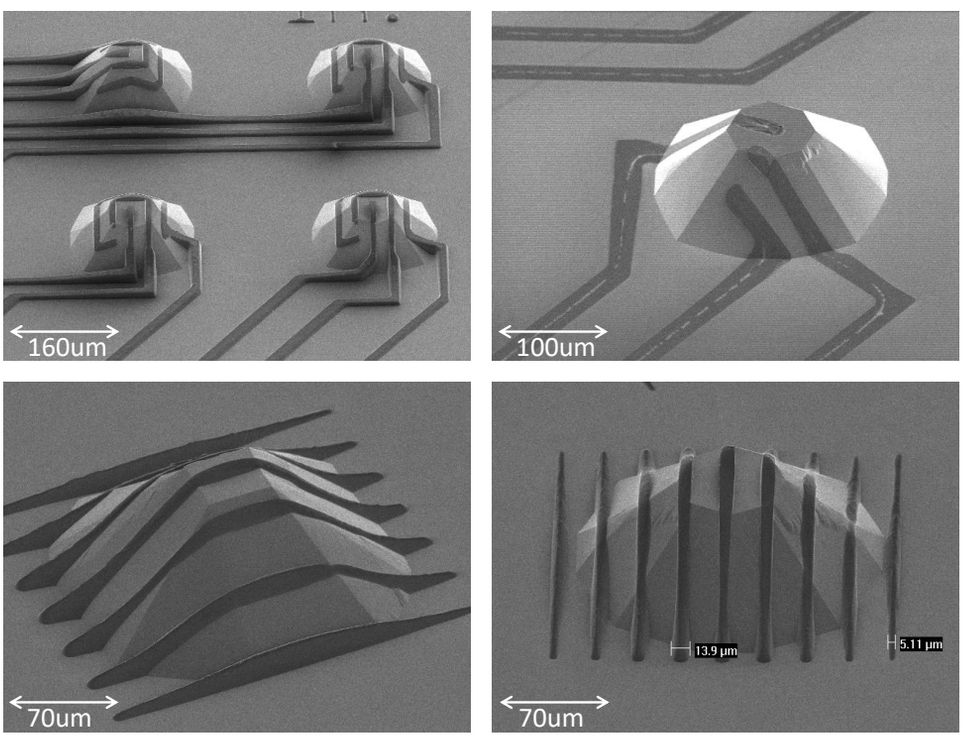

Figure E.1: Sidewall lithography results. Depth = 85um.

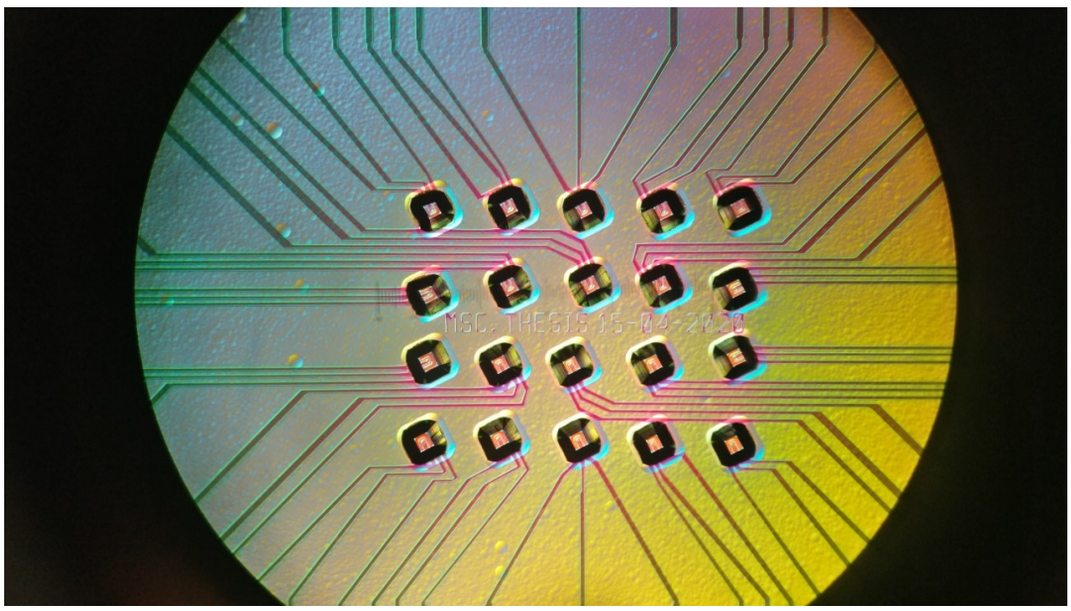

Figure E.2: Microelectrode array viewed from a microscope.

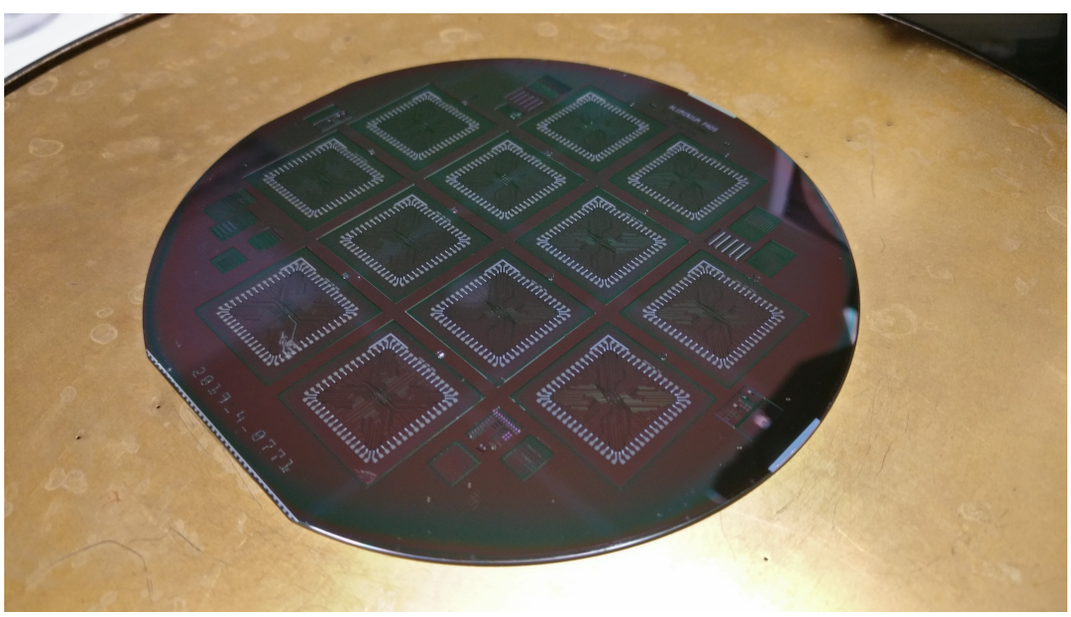

Figure E.3: Final wafer result.

F

EUROoC2020 conference abstract paper

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A 3D microelectrode array to record neural activity at different tissue depths

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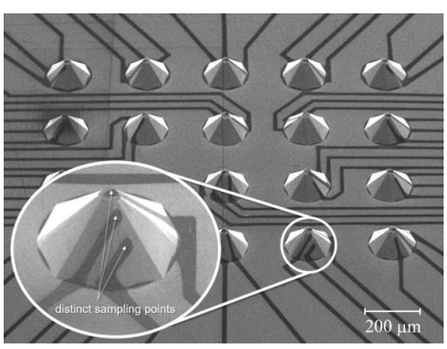
Introduction

In vitro study of high-level neurobiological systems requires three-dimensional (3D) neuronal cultures [1]. Measuring responses along all three spatial dimensions is critical to record electric activity inside 3D neuronal models, such as organoids and other 3D brain tissue constructs. However, this goes beyond the capacity of established 2D microelectrode arrays (MEAs) [2]. We present planar arrays of 3D micro-pyramids, whereby each micro-pyramid supports multiple, electrically distinct and vertically stacked microelectrodes. The 3D microarrays were manufactured by wafer-scale micromachining and assembled onto PCBs conforming to MEA readout standards.

Theory and Experimental procedure

Microelectrode arrays (Fig. 1) were fabricated on 4" Si wafers. The truncated micro-pyramids were obtained by timed anisotropic wet etching (25% TMAH + Triton solution) of the Si substrate using lithographically defined hard masks that allowed precise selection of crystallographic directions. After thermal growth of a 270 nm-thick SiO_2 passivation layer, a 40 nm/200 nm-thick Ti/TiN layer was sputtered and lithographically patterned to define the electrically independent electrodes. On each pyramid, vertically stacked and distinct sampling points were defined at the tip of each electrode by lithographic patterning of a thin polyimide layer. The wafer was saw diced into 2 by 2 cm^2 chips that were finally glued and wire-bonded to square PCBs with 60 peripheral contact pads [2].



Results and Discussion

Wet anisotropic etch of the Si substrate yielded ~100 µm-high truncated pyramids with octagonal base and ~46° slope facet as by design (Fig. 1). The etching left a smooth surface on the facets of the micro-pyramids. The smallest metal tracks patterned on the slanted facets were 15 µm-wide with minimal inter-track gap of 5 µm. Multiple geometries and configurations of the microelectrodes were defined, as will be shown in the full presentation.

Figure 1: *SEM micrograph of a 3D array of 60 microelectrodes. Each micro-pyramid in the array is ~85 µm-high and features three distinct and vertically stacked microelectrodes (see inset).*

Conclusion

We fabricated 3D microelectrode arrays able to record electric tissue activity at multiple and vertically resolved points. Metal interconnects with features down to 15 µm across the slanted and smooth facets of micro-pyramids where defined by single lithographic steps. The Si chips were assembled onto PCBs compatible with standard MEA measurement setups. By virtue of these innovative 3D MEAs we expect to be able to measure responses of 3D neuronal networks from hiPSC-derived cortical neurons cultured within biogel matrices or as brain organoids.

Acknowledgements

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G

Flowchart

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3D Microelectrode array

Zero Layer

1. COATING • **Nov 2008**

Use the coater station of the EVG120 system to coat the wafers with photoresist. The process consists of:
- a treatment with HMDS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas
- spin coating of Shipley SPR3012 positive resist, dispensed by a pump
- a soft bake at 95 °C for 90 seconds
- an automatic edge bead removal with a solvent

Always check the relative humidity (48 ± 2 %) in the room before coating, and follow the instructions for this equipment.

Use program "**Co - 3012 - zero layer**". There will be a larger edge bead removal.

2. ALIGNMENT AND EXPOSURE • **May 2011**

Processing will be performed on the ASML PAS5500/80 automatic wafer stepper.
Follow the operating instructions from the manual when using this machine.

Expose masks **COMURK** and **FWAM**, with job "**ZEFWAM**" and the correct exposure energy (check the energy list).
This results in alignment markers for the stepper and contact aligner for wafers which will not get an EPI layer.

3. DEVELOPING • **Apr 2008**

Use the developer station of the EVG120 system to develop the wafers. The process consists of:
- a post-exposure bake at 115 °C for 90 seconds
- developing with Shipley MF322 with a single puddle process
- a hard bake at 100 °C for 90 seconds

Always follow the instructions for this equipment.

Use program "**Dev - SP**".

4. INSPECTION: Linewidth and overlay • **Feb 1996**

Visually inspect the wafers through a microscope, and check the line width and overlay. No resist residues are allowed.

5. PLASMA ETCHING: Alignment markers (URK's) in Silicon • **Feb 1999**

Use the Trikon Ωmega 201 plasma etcher.
Follow the operating instructions from the manual when using this machine.
It is **not** allowed to change the process conditions and times from the etch recipe!

Use sequence **URK_NPD** (with a platen temperature of **20 °C**) to etch 120 nm deep ASM URK's into the Si.

Process conditions from chamber recipe URK_ETCH:						
Step	Gasses & flows	Pressure	Platen RF	ICP RF	Platen temp.	Etch time
1. breakthrough	CF_4/O_2 = 40/20 sccm	5 mTorr	60 W	500 W	20 °C	0'10"
2. bulk etch	Cl_2/HBr = 80/40 sccm	60 mTorr	20 W	500 W	20 °C	0'40"

6. LAYER STRIPPING: Photoresist • **Feb 1999**

Strip resist — Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma.
Follow the instructions specified for the Tepla stripper, and use the quartz carrier.
Use **program 1**: 1000 watts power and automatic endpoint detection + 2 min. overetching.

7. CLEANING: HNO_3 99% and 69.5% **• Nov 2007**

Clean — 10 minutes in fuming nitric acid at ambient temperature. This will dissolve organic materials.
Use wet bench "HNO_3 99% (Si)" and the carrier with the red dot.

Rinse — Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.

Clean — 10 minutes in concentrated nitric acid at 110 °C. This will dissolve metal particles.
Use wet bench "HNO_3 69,5% 110C (Si)" and the carrier with the red dot.

Rinse — Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.

Dry — Use the Semitool "rinser/dryer" with the standard program, and the white carrier with a red dot.

8. LPCVD DEPOSITION: 400 nm low-stress Silicon nitride **• Jan 1995**

Furnace tube: E2 Program name: 4INCHST (waits for operator)

Follow the instructions for the LPCVD furnace when using this equipment.

Process conditions from recipe 4INCHST:			
Gasses & flows	Pressure	Temperature	Time
SiH_2Cl_2 / NH_3 = 169.5 / 30.5 sccm	150 mTorr	850 °C	**variable command**

Note:
- The layer thickness depends on the deposition time, which can be calculated from the average deposition rate during recent furnace usage.
- An extra test wafer can be deposited for measurements and etch tests.

9. MEASUREMENT: Silicon nitride thickness **• Apr 2002**

Use the Leitz MPV-SP measurement system for layer thickness measurements.
Follow the operating instructions from the manual when using this equipment.

⇨ Program: LPCVDSIN on SI (400 nm)
Nitride thickness: 400 ± 10 nm ⇨ on a bare silicon wafer

10. COATING **• Apr 2008**

Use the coater station of the EVG120 system to coat the wafers with photoresist. The process consists of:
- a treatment with HMDS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas
- spin coating of Shipley SPR3012 positive resist, dispensed by a pump
- a soft bake at 95 °C for 90 seconds

Always check the relative humidity (48 ± 2 %) in the room before coating, and follow the instructions for this equipment.

Use program "1_**Co - 3012 - 1,4µm - no EBR**". There will be no edge bead removal.

11. ALIGNMENT AND EXPOSURE **• Sep 2001**

Processing will be performed on the Electronic Visions EV420 manual contact aligner.
Follow the operating instructions from the manual when using this machine.
Always check if the mask is clean before usage; perform mask cleaning if necessary.

Expose **mask pyramid** , with an exposure time of ■■ seconds.
Use top side alignment **program 1** with the "**soft contact**" option switched on.

12. DEVELOPING • **Apr 2008**

Use the developer station of the EVG120 system to develop the wafers. The process consists of:
- a post-exposure bake at 115 °C for 90 seconds
- developing with Shipley MF322 with a single puddle process
- a hard bake at 100 °C for 90 seconds

Always follow the instructions for this equipment.

Use program "**Dev - SP**".

13. INSPECTION: Linewidth and overlay • **Feb 1996**

Visually inspect the wafers through a microscope, and check the line width and overlay. No resist residues are allowed.

14. PLASMA ETCHING: 400 nm Silicon Nitride • **Jan 1995**

Use the Drytek Triode 384T plasma etcher.
Follow the operating instructions from the manual when using this machine.
It is **not** allowed to change the process conditions from the etch recipe, except for the etch time!

Use recipe **STDSIN** to etch the SiN layer. Set the etch time to 1'30".

Process conditions from recipe STDSIN:					
Step	Gasses & flows	Pressure	RF power	He pressure	Etch time
1. bulk etch (RIE)	C_2F_6 = 65 sccm	130 mTorr	250 W	8 Torr	1'30"

INSPECTION: No residues are allowed.

15. LAYER STRIPPING: Photoresist • **Feb 1999**

Strip resist — Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma.
Follow the instructions specified for the Tepla stripper, and use the quartz carrier.
Use **program 1**: 1000 watts power and automatic endpoint detection + 2 min. overetching.

16. CLEANING: HNO_3 99% and 69.5% • **Nov 2007**

Clean — 10 minutes in fuming nitric acid at ambient temperature. This will dissolve organic materials.
Use wet bench "HNO_3 99% (Si)" and the carrier with the red dot.

Rinse — Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.

Clean — 10 minutes in concentrated nitric acid at 110 °C. This will dissolve metal particles.
Use wet bench "HNO_3 69,5% 110C (Si)" and the carrier with the red dot.

Rinse — Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.

Dry — Use the Semitool "rinser/dryer" with the standard program, and the white carrier with a red dot.

17. LAYER STRIPPING: Remove native oxide from the Si surface • **Jan 1995**

Etch — Use wet bench "0.55% HF" at ambient temperature, and the carrier with the black dot.

Time — 4 minutes.

Rinse — Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.

Dry — Use the Semitool "rinser/dryer" with the standard program, and the orange carrier with a red dot.

Note: **Metallization must be performed immediately after drying.**

18. WET ETCHING: TMAH + Triton in Cleanroom Class 10000 wet benches • **Feb 1999**

Etch — Use TMAH 25% + 0.25%v/v Triton at 80°C

Time — Etch until the desired depth is reached.
The required etch time depends on the etch rate of the solution, which is dependant on the temperature and condition of the bath. Etching in several steps for better depth control is advised.

Rinse — Rinse the wafers and carrier very well in a container filled with deionized water. (At least 4 times)

19. CLEANING: HNO_3 99% and 69.5% • **Nov 2007**

Clean — 10 minutes in fuming nitric acid at ambient temperature. This will dissolve organic materials.
Use wet bench "HNO_3 99% (Si)" and the carrier with the red dot.

Rinse — Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.

Clean — 10 minutes in concentrated nitric acid at 110 °C. This will dissolve metal particles.
Use wet bench "HNO_3 69,5% 110C (Si)" and the carrier with the red dot.

Rinse — Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.

Dry — Use the Semitool "rinser/dryer" with the standard program, and the white carrier with a red dot.

20. PLASMA ETCHING: 500 nm Silicon Nitride • **Jan 1995**

Use the Drytek Triode 384T plasma etcher.
Follow the operating instructions from the manual when using this machine.
It is **not** allowed to change the process conditions from the etch recipe, except for the etch time!

Use recipe **STDSIN** to etch the SiN layer. Set the etch time to 1'30".

Process conditions from recipe STDSIN:					
Step	Gasses & flows	Pressure	RF power	He pressure	Etch time
1. bulk etch (RIE)	C_2F_6 = 65 sccm	130 mTorr	250 W	8 Torr	1'30"

INSPECTION: No residues are allowed.

Passivate metal lines from Si

21. CLEANING: HNO_3 99% and 69.5% • **Nov 2007**

Clean — 10 minutes in fuming nitric acid at ambient temperature. This will dissolve organic materials.
Use wet bench "HNO_3 99% (Si)" and the carrier with the red dot.

Rinse — Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.

Clean — 10 minutes in concentrated nitric acid at 110 °C. This will dissolve metal particles.
Use wet bench "HNO_3 69,5% 110C (Si)" and the carrier with the red dot.

Rinse — Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.

Dry — Use the Semitool "rinser/dryer" with the standard program, and the white carrier with a red dot.

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22. LAYER STRIPPING: Remove native oxide from the Si surface **• Jan 1995**

Etch	Use wet bench "0.55% HF" at ambient temperature, and the carrier with the black dot.
Time	4 minutes.
Rinse	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Dry	Use the Semitool "rinser/dryer" with the standard program, and the orange carrier with a red dot.
Note:	**Metallization must be performed immediately after drying.**

23. PECVD DEPOSITION: 200 **nm Silicon oxide (on both sides)** **• Jan 1995**

Use the Novellus Concept One PECVD reactor.
Follow the operating instructions from the manual when using this machine.
It is **not** allowed to change the process conditions and time from the deposition recipe!

Use macro **.xxxSiOStd** to deposit a **200** nm thick SiO_2 layer. Set the station deposition time to ■■ sec/station.

Process conditions from recipe .xxxSiOStd:					
Gasses & flows	Pressure	HF power	LF power	Temperature	Time
$N_2/SiH_4/N_2O$ = 3150/205/6000 sccm	2.2 Torr	1000 W	0 W	400 °C	**variable**

Note: The deposition time is subject to minor changes, in order to obtain the correct film thickness.
Add a testwafer for layer thickness measurements.

Aluminum Pads

24. ALUMINIUM SPUTTERING: METALLIZATION FOR PADS

Use the TRIKON SIGMA sputter coater for the deposition of an aluminium metal layer on the wafers.
The target must exist of 99% Al and 1% Si, and deposition must be done at 25 °C. Follow the operating instructions from the manual when using this machine.

Use recipe "**AlSi_675nm_350"** to sputter a **600 nm** thick layer. Use recipe with RF sputtering to remove native oxide.

Note: Check the wafers after aluminum deposition. Metal residuals should be not present on the edge neither on the frontside nor the backside of the wafer.

25. COATING **• Apr 2008**

Use the EVG101 spraycoater system to coat the wafers with photoresist. The process consists of:
- AZ9260 diluted positive photoresist

Always check the relative humidity (48 ± 2 %) in the room before coating, and follow the instructions for this equipment.

Use program "**HP 1000mbar 5 ml 8 layers**". 5min bake-out step

26. ALIGNMENT AND EXPOSURE **• Sep 2001**

Processing will be performed on the Electronic Visions EV420 manual contact aligner.
Follow the operating instructions from the manual when using this machine.
Always check if the mask is clean before usage; perform mask cleaning if necessary.

Expose **mask AL pads**, with an exposure dose of 950.
Use top side alignment **program 1** with the "**soft contact**" option switched on.

27. DEVELOPING MANUAL **• Apr 2008**

Use the developer fume hood in the polymer lab.

Developing with the **AZ400K** developer for **roughly 3 minutes**.
Do not use to much developer and rinsing fluid (mostly water) during the developing.

Note: Dispose the developer into the right container if it is not water based.

NOTE: When finished always turn of the DI-water.

28. INSPECTION: Linewidth and overlay **• Feb 1996**

Visually inspect the wafers through a microscope, and check the line width and overlay. No resist residues are allowed.

29. PLASMA ETCHING OF ALUMINUM

For aluminum etching use the Trikon Ωmega 210 plasma etcher. Follow the operating instructions from the manual when using this machine.

Use sequence **AL06_350** (with a platen temperature of **25 °C**) to etch the aluminium layer.

Process conditions from chamber recipe AL06_350: (use for 0.6 - 1.0 µm Al sputtered at 350 °C)						
Step	Gasses & flows	Pressure	Platen RF	ICP RF	Platen temp.	Etch time
1. breakthrough	HBr/Cl_2 = 40/30 sccm	5 mTorr	50 W	500 W	25 °C	endpoint
2. bulk etch	HBr/Cl_2 = 40/30 sccm	5 mTorr	40 W	500 W	25 °C	endpoint
3. overetch	HBr/Cl_2 = 30/15 sccm	5 mTorr	40 W	500 W	25 °C	60% of bulk

INSPECTION: No aluminium residues or undercut are allowed.

30. LAYER STRIPPING: Photoresist **• Feb 1999**

Strip resist Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma.
Follow the instructions specified for the Tepla stripper, and use the quartz carrier.
Use **program 1**: 1000 watts power and automatic endpoint detection + 2 min. overetching.

Metalization

31. CLEANING: HNO_3 99% and 69.5% + HF 0.55% **• Nov 2007**

Clean	10 minutes in fuming nitric acid at ambient temperature. This will dissolve organic materials. Use wet bench "HNO_3 99% (Si)" and the carrier with the red dot.
Rinse	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Clean	10 minutes in concentrated nitric acid at 110 °C. This will dissolve metal particles. Use wet bench " HNO_3 69,5% 110C " and the carrier with the red dot.
Rinse	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Remove native oxide	4 minutes in 0.55% HF at ambient temperature. The wafer must be **hydrophobic**. Use wet bench "0.55% HF" and the carrier with the yellow & black dots.
Rinse	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Dry	Use the Semitool "rinser/dryer" with the standard program, and the white carrier with a red dot.
Note	**The next step must be performed immediately after drying.**

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32. TITANIUM SPUTTERING: 200**nm Ti N@ 350°C (with Ti target)** • **Jan 2004**

Use the TRIKON SIGMA 204 sputter coater for the deposition of a Titanium on the wafers.
The target must exist Ti and deposition must be done at 350 °C with an Ar flow of ??? sccm.
Follow the operating instructions from the manual when using this machine.

Use recipe ■■■ to obtain a **200** nm thick Ti layer.

33. COATING • **Apr 2008**

Use the EVG101 spraycoater system to coat the wafers with photoresist. The process consists of:
- AZ9260 diluted positive photoresist

Always check the relative humidity (48 ± 2 %) in the room before coating, and follow the instructions for this equipment.

Use program "**HP 1000mbar 5 ml 8 layers**".

34. ALIGNMENT AND EXPOSURE • **Sep 2001**

Processing will be performed on the Electronic Visions EV420 manual contact aligner.
Follow the operating instructions from the manual when using this machine.
Always check if the mask is clean before usage; perform mask cleaning if necessary.

Expose **mask TiN IC**, with an exposure dose of 950.
Use top side alignment **program 1** with the "**soft contact**" option switched on.

35. DEVELOPING MANUAL • **Apr 2008**

Use the developer fume hood in the polymer lab.

Developing with the **AZ400K** developer for ■■ seconds.
Do not use to much developer and rinsing fluid (mostly water) during the developing.

Note: Dispose the developer into the right container if it is not water based.

NOTE: When finished always turn of the DI-water.

36. INSPECTION: Linewidth and overlay • **Feb 1996**

Visually inspect the wafers through a microscope, and check the line width and overlay. No resist residues are allowed.

37. PLASMA ETCHING: ■■■ nm Titanium Nitride (sputtered at 350 °C) • **Aug 2002**

Use the Trikon Ωmega 201 plasma etcher.
Follow the operating instructions from the manual when using this machine.
It is **not** allowed to change the process conditions and times from the etch recipe!

Use sequence ■■■ (with a platen temperature of **25 °C**) to etch the titanium layer.

Process conditions from chamber recipe ■■■: (use for 0.6 - 1.0 µm Al sputtered at 350 °C)						
Step	Gasses & flows	Pressure	Platen RF	ICP RF	Platen temp.	Etch time
1. breakthrough	HBr/Cl_2 = 40/30 sccm	5 mTorr	50 W	500 W	25 °C	■■■
2. bulk etch	HBr/Cl_2 = 40/30 sccm	5 mTorr	40 W	500 W	25 °C	■■■
3. overetch	HBr/Cl_2 = 30/15 sccm	5 mTorr	40 W	500 W	25 °C	■■■

INSPECTION: No titanium residues or undercut are allowed.

38. LAYER STRIPPING: Photoresist • **Feb 1999**

Strip resist Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma.
Follow the instructions specified for the Tepla stripper, and use the quartz carrier.
Use **program 1**: 1000 watts power and automatic endpoint detection + 2 min. overetching.

Passivation

39. CLEANING: HNO_3 99% metal • **Nov 2007**

Clean — 10 minutes in fuming nitric acid at ambient temperature. This will dissolve organic materials.
Use wet bench "HNO_3 99% (**metal)**" and the carrier with a red and yellow dot.

Rinse — Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.

Dry — Use the Semitool "rinser/dryer" with the standard program, and the white carrier with a black dot.

Note — **Do not perform a "HNO_3 69,5% 110C (Si)" cleaning step!**

40. PECVD DEPOSITION: 300 **nm Silicon oxide** • **Jan 1995**

Use the Novellus Concept One PECVD reactor.
Follow the operating instructions from the manual when using this machine.
It is **not** allowed to change the process conditions and time from the deposition recipe!

Use macro **.xxxSiOStd** to deposit a **300** nm thick SiO_2 layer. Set the station deposition time to ■■ sec/station.

Process conditions from recipe .xxxSiOStd:					
Gasses & flows	Pressure	HF power	LF power	Temperature	Time
$N_2/SiH_4/N_2O$ = 3150/205/6000 sccm	2.2 Torr	1000 W	0 W	400 °C	**variable**

Note: The deposition time is subject to minor changes, in order to obtain the correct film thickness.
Add a testwafer for layer thickness measurements.

41. MEASUREMENT: Layer thickness

Use the Leitz MPV-SP measurement system for layer thickness measurements.
Follow the operating instructions from the manual when using this equipment.

⇨ Program: ■■■
Layer thickness: ■■■ nm

42. COATING • **Apr 2008**

Use the EVG101 spraycoater system to coat the wafers with photoresist. The process consists of:
- AZ9260 diluted positive photoresist

Always check the relative humidity (48 ± 2 %) in the room before coating, and follow the instructions for this equipment.

Use program "**HP 1000mbar 5 ml 8 layers**".

43. ALIGNMENT AND EXPOSURE • **Sep 2001**

Processing will be performed on the Electronic Visions EV420 manual contact aligner.
Follow the operating instructions from the manual when using this machine.
Always check if the mask is clean before usage; perform mask cleaning if necessary.

Expose **mask VIAS**, with an exposure dose of 950.
Use top side alignment **program 1** with the "**soft contact**" option switched on.

3D Microelectrode array

44. DEVELOPING MANUAL • **Apr 2008**

Use the developer fume hood in the polymer lab.

Developing with the ■■■ developer for ■■ seconds.
Do not use to much developer and rinsing fluid (mostly water) during the developing.

Note: Dispose the developer into the right container if it is not water based.

NOTE: When finished always turn of the DI-water.

45. INSPECTION: Linewidth and overlay • **Feb 1996**

Visually inspect the wafers through a microscope, and check the line width and overlay. No resist residues are allowed.

46. PLASMA ETCHING: ■■■ nm oxide (to land on TiN) • **Jun 1995**

Use the Drytek Triode 384T plasma etcher.
Follow the operating instructions from the manual when using this machine.
It is **not** allowed to change the process conditions from the etch recipe, except for the etch times!

Use recipe **OXSFTLND** to etch the oxide layer with a soft landing on the layer underneath.
Set the etch times to ■'■■" for step 1 (note: min. time = 3 sec for plasma ignition) and to ■'■■" for step 2.

Note:
- Etching on a sloped sidewall takes more time to open windows.
- Fluorine chemistry will also etch titanium, so do not excessively overetch.

Process conditions from recipe OXSFTLND:					
Step	Gasses & flows	Pressure	RF power	He pressure	Etch time
1. bulk etch (RIE)	C_2F_6/CHF_3 = 36/144 sccm	180 mTorr	300 W	12 Torr	variable
2. soft land (RIE)	C_2F_6/CHF_3 = 36/144 sccm	180 mTorr	100 W	12 Torr	variable

INSPECTION: No residues are allowed.

47. LAYER STRIPPING: Photoresist • **Feb 1999**

Strip resist — Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma.
Follow the instructions specified for the Tepla stripper, and use the quartz carrier.
Use **program 1**: 1000 watts power and automatic endpoint detection + 2 min. overetching.

48. CLEANING: HNO_3 99% metal • **Nov 2007**

Clean — 10 minutes in fuming nitric acid at ambient temperature. This will dissolve organic materials.
Use wet bench "HNO_3 99% (**metal)**" and the carrier with a red and yellow dot.

Rinse — Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.

Dry — Use the Semitool "rinser/dryer" with the standard program, and the white carrier with a black dot.

Note — **Do not perform a "HNO_3 69,5% 110C (Si)" cleaning step!**

49. Wafer Dicing for packaging

50. Wire bonding to pcb