An Ultra High-Frequency 8-Channel Neurostimulator Circuit with 68% Peak Power Efficiency

Urso, Alessandro; Giagka, Vasiliki; van Dongen, Marijn; Serdijn, Wouter A.

DOI
10.1109/TBCAS.2019.2920294

Publication date
2019

Document Version
Final published version

Published in
IEEE Transactions on Biomedical Circuits and Systems

An Ultra High-Frequency 8-Channel Neurostimulator Circuit With 68% Peak Power Efficiency

Alessandro Urso, *Student Member, IEEE*, Vasiliki Giagka, *Member, IEEE*, Marijn van Dongen, *Member, IEEE*, and Wouter A. Serdijn, *Fellow, IEEE*

***Abstract*—In order to recruit neurons in excitable tissue, constant current neural stimulators are commonly used. Recently, ultra high-frequency (UHF) stimulation has been proposed and proven to have the same efficacy as constant-current stimulation. UHF stimulation uses a fundamentally different way of activating the tissue: each stimulation phase is made of a burst of current pulses with adjustable amplitude injected into the tissue at a high (e.g., 1 MHz) frequency. This paper presents the design, integrated circuit (IC) implementation, and measurement results of a power efficient multichannel UHF neural stimulator. The core of the neurostimulator is based on our previously proposed architecture of an inductor-based buck–boost dc–dc converter without the external output capacitor. The ultimate goal of this work is to increase the power efficiency of the UHF stimulator for multiple-channel operation, while keeping the number of external components minimal. To this end, a number of novel approaches were employed in the integrated circuit design domain. More specifically, a novel zero-current detection scheme is proposed. It allows to remove the freewheel diode typically used in dc–dc converters to prevent current to flow back from the load to the inductor. Furthermore, a gate-driver circuit is implemented which allows the use of thin gate-oxide transistors as high-voltage switches. By doing so, and exploiting the fundamental working principle of the proposed current-controlled UHF stimulator, the need for a high-voltage supply is eliminated and the stimulator is powered up from a 3.5 V input voltage. Both the current detection technique and the gate driving circuit of the current implementation allow to boost the power efficiency up to 300% when compared to previous UHF stimulator works. A peak power efficiency of 68% is achieved, while 8 independent channels with 16 fully configurable electrodes are used. The circuit is implemented in a 0.18 μm HV process, and the total chip area is 3.65 mm^2.**

***Index Terms*—Buck-boost DC–DC converter, high power efficiency, low power, multichannel, neural stimulation, ultra high frequency stimulation.**

Manuscript received March 1, 2019; revised April 19, 2019 and May 22, 2019; accepted May 25, 2019. Date of publication May 31, 2019; date of current version November 4, 2019. This paper was recommended by Associate Editor S.-Y. Lee. *(Corresponding author: Alessandro Urso.)*

A. Urso and W. A. Serdijn are with the Department of Microelectronics, Delft University of Technology, 2628 Delft, The Netherlands (e-mail: a.urso@tudelft.nl; w.a.serdijn@tudelft.nl).

V. Giagka is with the Department of Microelectronics, Delft University of Technology, 2628 Delft, The Netherlands, and also with the Fraunhofer Institute for Reliability and Microintegration IZM, 13355 Berlin, Germany (e-mail: v.giagka@tudelft.nl).

M. van Dongen is with the NXP Semiconductors, 6534 Nijmegen, The Netherlands (e-mail: dongen@fastmail.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TBCAS.2019.2920294

I. Introduction

OVER the past few decades, many implantable neurostimulators have been developed in order to treat various neural and brain disorders. Typical applications of such stimulators are retinal implants [3], deep brain stimulation (DBS) and spinal cord stimulation (SCS) [4]–[6]. The biggest challenge that such devices have in common is their limited battery life. Most batteries for neurostimulators last three to five years, and in case of extensive use the battery has to be replaced or recharged yearly [7]. In order to cope with this problem, the battery size is increased at the expense of post-surgery trauma and risk of infection. If the stimulator, together with the battery, is small enough, it can be implanted by means of a percutaneous injection. These devices are known as *Injectable Neurostimulators* [8]. In this scenario, a surgical operation is avoided, together with its complications. Furthermore, in the emerging field of Bioelectronic Medicine, neural implants need to be made so small to directly interface with tiny nerves, that a battery-less solution might be necessary, where all available power would have to be harvested or transferred from outside the body [9]. Hence, the need for increased power efficiency is more relevant than ever. At the same time, current trends indicate the need for an increasing number of independent stimulating channels to accommodate a large number of stimulating sites, especially for applications like cochlear implants or retinal implants. These two requirements, namely power efficiency and multichannel operation, are not trivial to accomplish simultaneously.

Conventional constant-current stimulators exploit a voltage drop across the current driver to keep the stimulation current constant. This leads to an inherently inefficient system. A popular way to reduce the energy wasted, and therefore increase the power efficiency, is to adapt the voltage supply of the neurostimulator to the voltage across the electrodes [3], [10], [11]. For instance, in [3] four different voltage supplies, both positive and negative, are generated from the main power supply. During each of the biphasic pulses, the stimulator voltage supply tracks the ramping electrode voltage such that the supply voltage is kept relatively close to the voltage required at the stimulator output. Despite that this seems a neat solution, the power efficiency improvement is not so significant due to the additional inefficiencies introduced by generating all the voltage supplies and due to the large amount of additional switches deployed. In a similar concept [12] and [13], a compliance monitor is used to continuously adjust the stimulation supply voltage. For all

the adaptive supply stimulators, however, during multichannel operation, the supply voltage has to accommodate the channel with the highest required output voltage. Hence, the voltage of the compliance monitor is still over-designed for the rest of the stimulating channels. This problem is even more significant in retinal implants where electrode arrays with hundreds of electrodes, hence larger number of independent channels, are used.

Switched Capacitor neural Stimulators (SCNS) have been introduced thanks to the fact that no external components are needed. In [14], a reconfigurable switched capacitor DC-DC converter with an adaptive supply is used to provide four different stimulation voltages, starting from an external input voltage of 6 V. The power efficiency is limited both by the parasitic capacitance of the capacitors involved in the conversion and by the large amount of high-voltage switches needed to generate all the different voltages for the neurostimulator. In [14], similarly to adaptive-supply stimulators, the stimulator voltage needs to accommodate the channel with the highest stimulation voltage, thereby affecting the power efficiency of the channels with a lower voltage compliance.

We have previously presented a neurostimulator architecture that uses a different way of stimulating the neural tissue compared to constant current stimulators [2]. Each stimulation phase is made of a sequence of current pulses injected in the tissue at a high frequency (e.g., 1 MHz). This concept of UHF stimulation will be further elaborated on in Section II. This fundamentally different stimulation type, together with the core of the architecture presented in [2], have great potential for achieving highly energy efficient multichannel stimulation.

In this work, we propose a new energy efficient, multichannel, UHF neural stimulator architecture. The key novel contributions of this paper are that the power efficiency is dramatically improved, especially when 8 channels are used simultaneously, and the external high voltage (HV) power supply, commonly used in neural stimulators, is avoided.

HV supplies, either external or on-chip, are usually necessary in neural stimulator, to ensure delivery of the required charge to large load variation. The proposed neurostimulator is powered up from a 3.5 V input voltage and can deliver the required charge without further limitations on the range of $100\,\Omega < R_{tissue} < 1\,\mathrm{k}\,\Omega$.

These results are achieved both by implementing a novel zero-current detection scheme and by using a gate-driver circuit that allows to use thin-gate oxide transistors as high-voltage switches. This drastically reduces the parasitic capacitance at the most critical node of the circuit.

The rest of the paper is organized as follows. In Section II, the concept of UHF stimulation is presented, together with a discussion on a previous implementation of a switched-capacitor high frequency neural stimulator. Section III describes the overall architecture of the stimulator and elaborates on the circuit details. Section IV reports the measurement results of a prototype IC realization. In Section V, a Figure Of Merit (FOM), originally introduced in [15], is used to compare the proposed system with other stimulator circuits present in literature. Finally, in Section VI, conclusions are drawn.

II. Related Work

The two widely used stimulation schemes are the so called *Current-Mode Stimulation* (*CMS*) and *Voltage-Mode Stimulation* (*VMS*) schemes. In CMS, the stimulator generates a well-defined current that flows into the tissue via the electrode-tissue interface (ETI). The total charge delivered to the tissue depends on the stimulation duration and the amplitude of the current, i.e., the charge is independent of the tissue and ETI impedance. In VMS, a constant and well-defined voltage is applied across the electrodes and thus the tissue and ETI. As a consequence, the charge transferred to the tissue depends on the electrode impedance itself. CMS is usually preferred over VMS for its precise charge control resulting in less circuitry to keep the residual charge within safety limits.

In this section, we first outline the concept of UHF neural stimulation. Then, we extensively discuss a recent implementation of a UHF neural stimulator that employs a switched-capacitor DC-DC converter to generate the pulses.

A. Principle of UHF Stimulation

The concept of UHF dynamic stimulation was introduced for the first time in [1]. It uses a different way of stimulating the neural tissue compared to constant-current stimulators. Each stimulation phase, i.e. the anodic and the cathodic phase, is made of a sequence of current pulses injected into the tissue at a high rate. In Fig. 1(a), an example of such a biphasic pulse is shown.

The amplitude of the pulses, indicated as A in Fig. 1(a), can be regulated and sets the stimulation intensity. In [1], by means of a stimulator circuit made of discrete components, it is shown that UHF stimulation depolarizes the cell membrane in a similar way as constant current stimulation does. In *vitro* experiments using Purkinje cells proved that this new way of stimulating the tissue also induces neural recruitment in the targeted area.

In Fig. 1(b), a high-level architecture of the UHF neural stimulator is shown. It consists of an inductor-based buck-boost DC-DC converter. The current pulses are not directly drawn from the main power supply. In fact, the inductor is first charged from the power supply, and then it is discharged into the tissue. The discharging process of the inductor into the tissue generates the current pulses. Hence, this implementation of a UHF neural stimulator provides a *CMS*. A duty-cycled signal is used to regulate the amount of energy transferred from the power supply to the load, i.e., the intensity of the stimulation (A in Fig. 1). In case more channels are operated concurrently, the pulses generated by the inductor are sent to all the activated channels in an interleaved fashion (Fig. 1(c)). Each channel can be stimulated with different intensity (A_1 and A_2 of Fig. 1(c)). This concept will be further elaborated on in Section III.

B. Switched-Capacitor Implementation of UHF Stimulator

Based on the first implementation of an UHF neural stimulator presented in [2], a switched-capacitor high-frequency neural stimulator is proposed in [16]. The stimulation voltage is derived from the main supply by using an $1:1$ switched capacitor

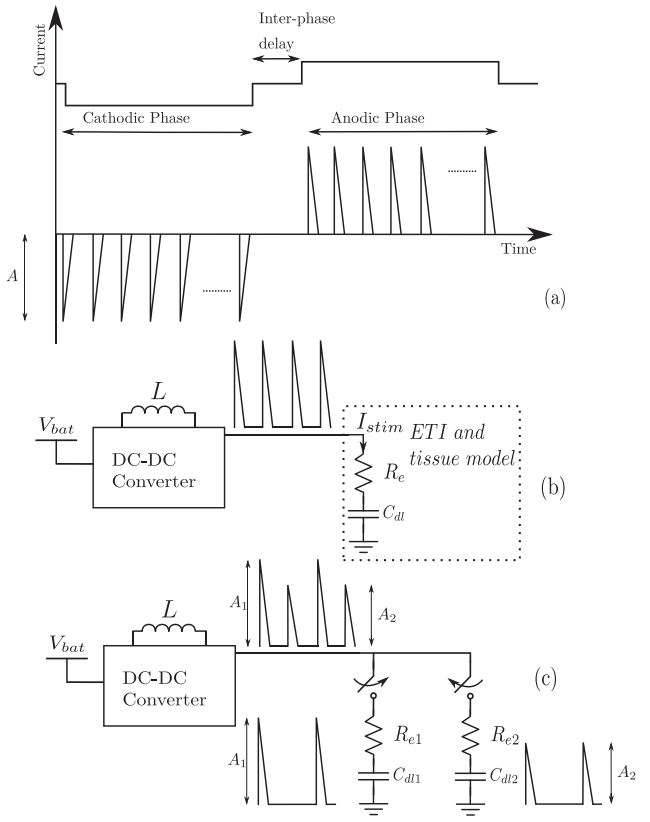

Fig. 1. Sketch of a biphasic pulse, produced by (a) constant current stimulation (top) and by UHF stimulation (bottom); (b) high level architecture of an UHF neural stimulator with a sketch of the current profile for single channel; and (c) multi-channel operation [2].

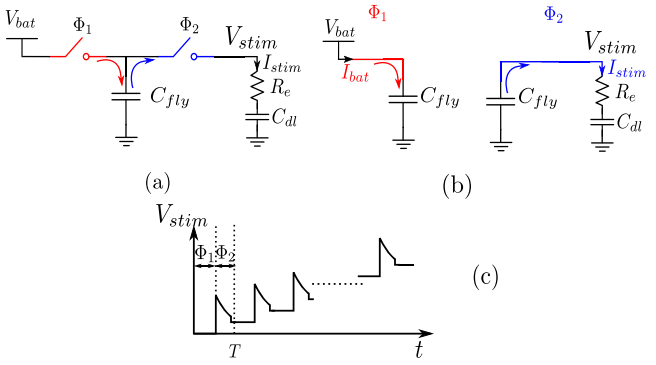

Fig. 2. Circuit representation of the DC-DC converter used in [16] to generate (a) the cathodic phase; (b) its working principle; and (c) resulting stimulation waveform.

DC-DC converter. This topology is shown in Fig. 2(a) and it is used during the cathodic stimulation phase. The circuit is made of two switches driven by two non-overlapping phases, Φ_1 and Φ_2 and a capacitance C_{fly} called flying capacitance. As shown in Fig. 2(b), during Φ_1, C_{fly} is connected between V_{bat} and ground, and therefore it is charged. During Φ_2 the capacitor is connected between the electrode and ground. Consequently, the charge stored in the capacitor is now transferred to the tissue. Fig. 2(c) shows the resulting stimulation voltage. In steady state, the power efficiency can be written as:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{stim} I_{stim}}{V_{bat} I_{bat}} = \frac{V_{stim}}{V_{bat}} \tag{1}$$

where P_{out} is the power delivered to the tissue, P_{in} is the power taken from the battery and $V_{stim} < V_{bat}$. I_{bat} and I_{stim} are the average current drawn from the battery and the average current delivered to the tissue, respectively. The last equality in Eq. (1) comes from the fact that, in steady state, the charge transferred into the capacitor during phase Φ_1 is the same as the charge that flows out of the capacitor in phase Φ_2, i.e. $I_{stim} = I_{bat}$ [17]. Eq. (1) shows that the power efficiency of the circuit in Fig. 2(a) is limited by the ratio V_{stim}/V_{bat}. The ideal voltage conversion ratio VCR of the circuit topology topology shown in Fig. 2(a) is $iVCR = \frac{V_{stim}}{V_{bat}} = 1$, which gives a theoretical efficiency of 100% [17]. As a consequence, the stimulation voltage can only be regulated at the expense of the power efficiency. However, as can be seen in Fig. 2(c), the voltage across the electrodes needs to be built up. Hence, V_{stim} is always lower than V_{bat}, the $iVCR$ is never met and the power efficiency is always lower than 100%. In the first clock period, T, capacitor C_{dl} is completely discharged. This means that, 50% of the energy is already lost when the energy is transferred from C_{fly} to C_{dl}. As the stimulation voltage builds up, the intrinsic energy loss is gradually reduced and the power efficiency converges to the value that corresponds to that particular $\frac{V_{stim}}{V_{bat}}$ ratio. This architecture is only capable of single-channel stimulation. If a multi-channel stimulation is needed, then many switched-capacitor convertors need to be deployed.

The stimulation mechanism behind the circuit in Fig. 2(a) lays in the transfer of a well-defined charge from the battery to the tissue and the ETI. In literature, it is named switched-capacitor stimulation (SCS). The amount of charge transferred at each cycle is still electrode-dependent. For this reason, in [16], additional circuitry is still needed to keep the residual charge within safety limits. In conclusion, the switched-capacitor based high frequency stimulator presented in [16] is not suitable for a power-efficient solution, especially when more channels need to be operated at the same time.

III. System Design

The circuit diagram of the proposed UHF neural stimulator is shown in Fig. 3. It is made of the following subsystems:

- *Core Circuit*, which is a power-efficient buck-boost DC-DC converter without the external capacitor. Hence, a train of current pulses is generated from the main power supply at a frequency equal to the switching frequency of the DC-DC converter. The most important requirement of this block is the power efficiency.
- *H-Bridge*, which is a particular configuration of switches that allows for the selection of the desired channel and, by reversing the direction of the current flowing into the tissue, implements the biphasic stimulation. Since the H-bridge is directly connected to the output of the Core Circuit, the parasitic capacitance introduced by those switches has to be kept minimal. By doing so, the power efficiency can be further increased.

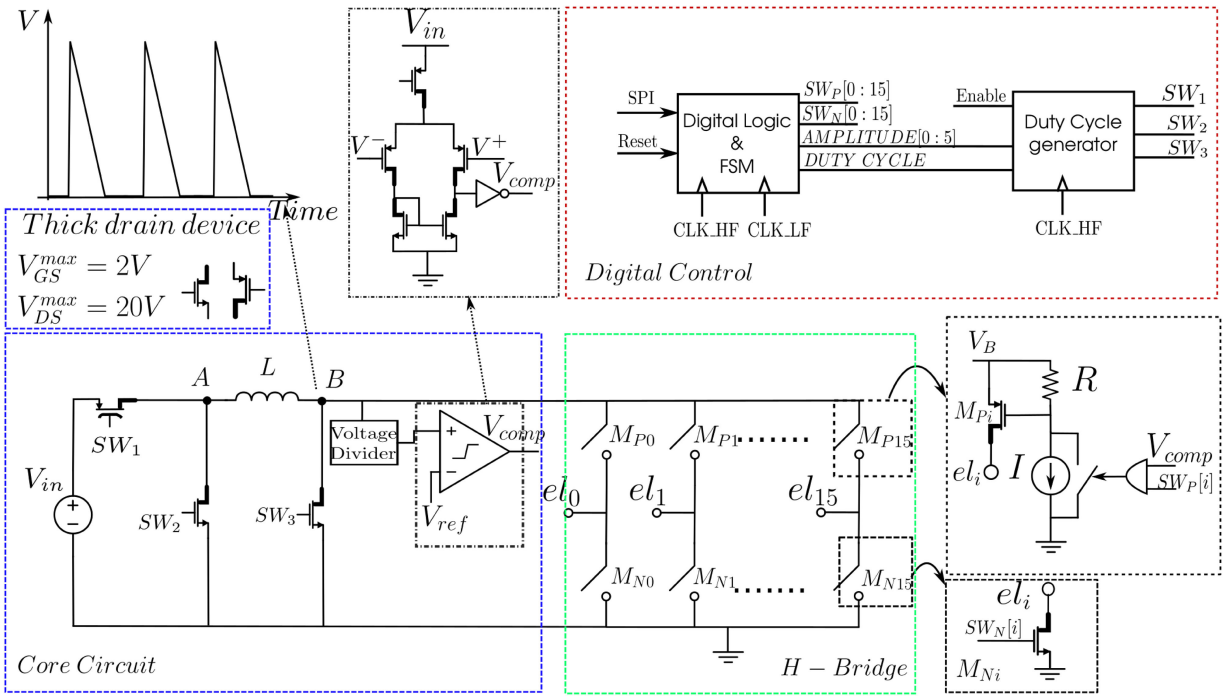

Fig. 3. System architecture showing the three subsystems of the implemented neural stimulator. The *core circuit* which generates the high-frequency pulses, the *H-bridge*, which by means of thin-oxide switches is capable of implementing a biphasic pulse and the digital control which generates all the signals needed by the *core circuit* and the *H-bridge*.

- *Digital Control Module*, which is able to generate and to store the stimulation patterns based on a serial bit stream loaded via a Serial Peripheral Interface (SPI).

The detailed operation and the structure of the subsystems are discussed in the following subsections.

A. Core Circuit With Novel Zero-Current Detection Scheme

In Fig. 4, a detailed representation of the core circuit is given along with a sketch of its most relevant waveforms. It is a forward buck-boost DC-DC converter without the external filtering capacitor. The forward topology allows to have the output voltage to be of the same polarity as the input voltage.

During Phase Φ_1, only Switches S_1 and S_3 are closed, hence the input source (V_{in}) is in parallel with the inductor and provides energy to it. The voltage across the inductor, $v_L(t)$, can be written as

$$v_L(t) = V_{in} = L\frac{di_L(t)}{dt} \tag{2}$$

V_{in} is constant, hence, during Φ_1, $i_L(t)$ has a positive constant slope as depicted in Fig. 4(b). At time $t = T_{ON}$, the inductor current reaches its peak value, which can be written as $I_{peak} = \frac{V_{in}}{L}T_{ON}$.

During Phase Φ_2, only Switch S_2 is closed. Hence, through the H-bridge, the inductor supplies its current to the load. The amount of energy transferred from the battery to the inductor during Φ_1 is proportional to *duty-cycle* $\delta = \frac{T_{ON}}{T}$. The converter works in discontinuous conduction mode, which means that, during Phase Φ_2, the inductor current reaches zero before the next phase starts. In order to prevent the current flowing from the load back to the inductor, i.e. $I_L < 0$, a freewheel diode is usually

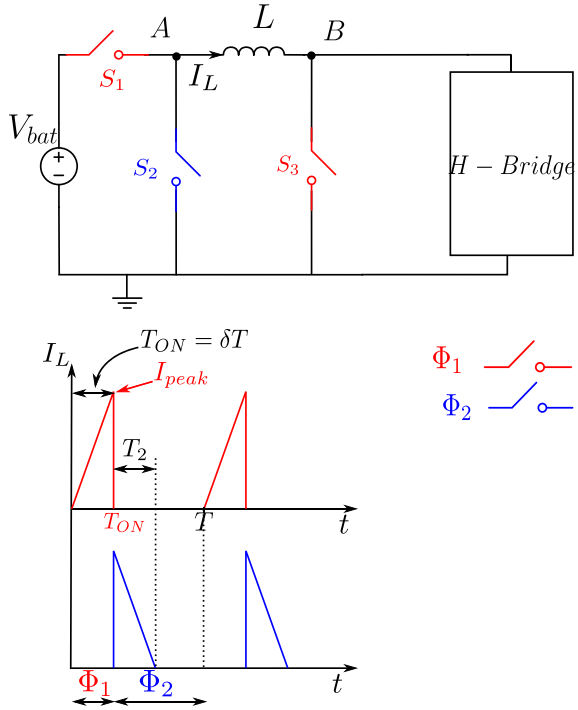

Fig. 4. (a) Operating principle of the buck-boost converter. (b) Sketch of the current waveform during Φ_1 and Φ_2.

placed between Node B of Fig. 3 and the H-bridge. The voltage drop across the diode has a big impact on the power efficiency, especially for low-intensity stimulation. In this work, the diode is avoided and a zero-current detection scheme is implemented

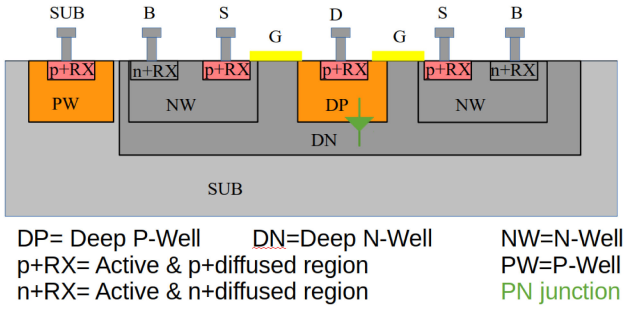

Fig. 5. Cross section view of a thick-drain PMOS transistor operated as high-voltage switch.

by means of a comparator. With respect to the Core Circuit depicted in Fig. 3, during Phase Φ_2, as soon as the inductor current becomes 0 and stays 0, the voltage across the inductor becomes 0. Since the voltage at Node A during Phase Φ_2 is 0 as well, we only need to detect when the voltage at Node B becomes 0. As the inductor and the parasitic capacitance of Switch S_3 introduce a resonance, the voltage at Node B rings around zero. Therefore, a reference voltage, V_{ref} that is slightly greater than 0 V is used [18]. Voltage V_{ref} is generated on chip and its value is much smaller than the voltage at the ETI, therefore it does not affect the accuracy of the zero-current detection technique. The output voltage is not filtered, hence the voltage at Node B, depending on the duty-cycle value, can be as high as 20 V. Exceeding this voltage would mean that some transistors would work out of their safe operating region. A comparator made of thin-oxide transistors is needed to reduce the parasitic capacitance at Node B.In order not to violate the maximum voltage compliance of the thin-oxide device, the voltage is first scaled down by means of a capacitive voltage divider and then compared to V_{ref}.

Fig. 5 shows the cross section view of the PMOS thick-drain transistor used in this design. Its rating voltages are $V_{SGMAX} = 2$ V, $V_{SDMAX} = 20$ V. The parasitic diode highlighted in green is of relevant interest for the designer. The diode always needs to be reversed biased. Since the source terminal is usually connected to the bulk terminal, the source-to-drain voltage always needs to be positive. This makes the device shown in Fig. 5 non symmetrical with respect to its source and drain terminals. The cross section view of an NMOS transistor is similar to the structure presented in Fig. 5.

The size of each capacitor used in the capacitor divider is 350 fF. The total parasitic capacitance at Node B of Fig. 3 is dominated by the gate-to-source capacitance of the 16 M_P switches. From circuit simulations, the gate-to-source capacitance of each M_P transistor is 2.5 pF which leads to a total parasitic capacitance at Node B of $16 * 2.5$ pF $= 40$ pF. As a consequence, the additional capacitance introduced by the voltage divider is negligible when compared to the total capacitance at Node B and therefore does not affect the power efficiency.

During Phase Φ_1 the total charge taken from the battery can be written as:

$$Q_{BAT} = I_{L_{\Phi_1}} T_{ON} = \frac{V_{in} T_{ON}}{2L} T_{ON} \tag{3}$$

where $I_{L_{\Phi_1}}$ is the average inductor current during Phase Φ_1. From Eq. (3), we can see that, by means of the duty cycle, the energy transferred from the battery to the inductor, and hence from the inductor to the load, can be controlled. Since the inductor directly powers the load, the stimulation is current steered. Therefore, by controlling the current flowing into the tissue, the charge transferred to the tissue can be easily controlled irrespective of the value of the load. This allows the stimulator to work with many different electrode types, and across a wide range of load impedances.

B. H-bridge

The H-bridge has a double purpose. It allows for the selection of the desired active electrodes (one electrode acts as anode while another acts as cathode), but it also allows for the implementation of biphasic stimulation pulses. A principle diagram of the H-bridge suitable for multichannel operation is depicted in Fig. 3. Assuming that N is the number of channels that can be stimulated simultaneously, in this work, as well as in [2], the H-bridge has $2 * N$ electrodes and $4 * N$ switches. A conventional current-source stimulator that has the same flexibility as this H-bridge (each channel can be connected to any pair of electrodes), would require N times more switches, therefore scaling up the total amount of switches to $4 * N * N$. This essentially means that conventional implementations of H-bridges become impractical if a large number of electrodes, that share the same inductor, needs to be independently controlled.

With respect to the H-bridge representation of Fig. 3, since the output voltages can exceed the supply voltage by a large amount, the switches on the bottom side can be implemented using NMOS transistors with thick drains and thin gate-oxides. Their source terminals are always connected to ground, hence it is relatively easy to turn the switch on and off. For the switches on the top side of the H-bridge, a similar configuration would require that the gates of the PMOS transistors are driven with a voltage directly, which would need to be as high as V_B, in this case up to 20 V. Hence, transistors with thick-gate oxide are to be used [2]. In the IC technology used, the minimum channel length of thick-oxide devices is 600 nm which leads to a significant higher gate-to-source parasitic capacitance. Since all the switches on the top side of the H-bridge have their source terminals connected together, the parasitic capacitance at Node B would be large. This has a big impact on the power efficiency because the parasitic capacitance at Node B is charged and discharged at every stimulation pulse (i.e., 1 MHz).

To reduce the parasitic capacitance at Node B, we have implemented a different approach in this work. For the switches on the top side of the H-bridge, PMOS transistors with thin gates and thick drains (M_P in Fig. 3) are used with resistors placed between their source and gate terminals. The current source provides a constant current, I, flowing through R such that the source-to-gate voltage of Transistor M_P can be controlled. Therefore, Switch M_P can be turned on and off by turning on and off the current source, respectively. Current source I is controlled by the comparator such that Transistor M_P is turned off as soon as the current flowing through the inductor

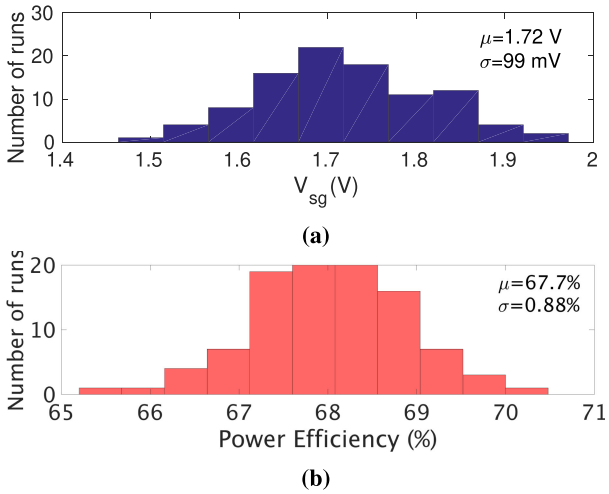

Fig. 6. Monte Carlo simulations showing (a) the gate-to-source voltage of the PMOS switches on the top side of the H-bridge and (b) the power efficiency for $R_{load} = 500\,\Omega$, $C_{load} = 1\,\mu$F and $duty\ cycle = 24\%$.

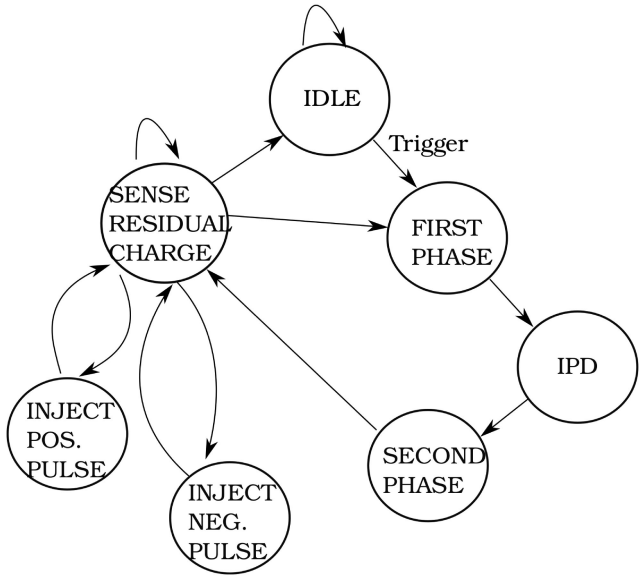

Fig. 7. Finite state machine (FSM) representation of a biphasic pulse and charge balancing procedure. The FSM moves through the phases of a classical biphasic pulse. Based on the sign of the residual charge, the stimulator sense and injects additional pulses until the residual charge changes sign.

reaches zero, as described in the zero-current detection scheme presented in the previous subsection. Using this approach makes it possible to use thin-gate-oxide devices for the PMOS transistors as well. By doing so, the external HV supply usually used in neural stimulators is also avoided. The value of I equals 1 mA. This implies that, with a resistance $R = 1.75$ kΩ, a constant source-to-gate voltage V_{SG} of 1.75 V is ensured. If a smaller value of current is used, then the value of the resistance needs to increase proportionally. Hence, the time constant associated with the charging and discharging of the parasitic gate-to-source capacitance of Transistor M_P also increases proportionally. This makes Switch M_P slower to be turned on and off, which directly impacts the efficiency.

The voltage drop across R leads to a power dissipation $P_R = V_{SG}I$, which is negligible compared to the power delivered to the load. Current I flows through the resistor only during T_2. Under the assumption that the load is purely resistive, $T_2 = T_{ON}$. Hence, the charge dissipated in the resistor is $Q_{res} = IT_2$. The ratio of the charge taken from the battery and the charge dissipated in the resistor can be written as:

$$\frac{Q_{BAT}}{Q_{res}} = \frac{V_{in}T_{ON}^2}{2LIT_{ON}} = \frac{V_{in}T_{ON}}{2LI} \tag{4}$$

For $L = 22\,\mu$H, $I = 1$ mA, $V_{in} = 3.5$ V, and $T_{ON} = 250$ ns (25% of the period), the charge dissipated by the resistor is 20 times smaller than the charge delivered to the tissue. Eq. (4) shows that the higher the duty cycle value, the lower is the impact of the gate-driving technique on the power efficiency of the whole system. This concept will be further discussed in Section V.

The overdrive voltage of the PMOS switches (M_P) on the top side of the H-bridge may vary due to process variations. This directly affects its on-resistance and therefore the power efficiency of the whole neural stimulator. To further investigate this, a Monte Carlo simulation with 100 data points has been performed. Fig. 6(a), shows that the average source-to-gate voltage of Switch M_P is 1.72 V with a standard deviation σ of only 99 mV. Fig. 6(b), shows how the total power efficiency is affected by process variations and mismatch. With the ETI modelled as $R_{load} = 500\,\Omega$ with a series $C_{load} = 1$ nF, the average efficiency is 67.7% with a standard deviation $\sigma = 0.9\%$.

C. Digital Control Module

The Digital Control Module has a similar architecture as the one presented in [2]. It generates all the required control signals to make the neurostimulator work. This block is powered from a 1.8 V supply, and from circuit simulations, its power consumption is approximately 100 μW. For each stimulation cycle, the pair of electrodes to be used, the amplitude and the pulse width can be set independently via an SPI. The stimulation pattern of each channel is stored in memory and it can be edited whenever needed. The commands used as input, and loaded into the control module via the SPI are: 1) edit a channel, 2) start the stimulation of a single channel, 3) stop the stimulation of a single channel, 4) start the stimulation of all the channels loaded in the memory (maximum of 8), 5) stop all the active channels. The digital control module runs with two different clocks: a low frequency clock CLK_LF, at $f_{clk_{LF}} = 1$ kHz and a high frequency clock, CLK_HF at $f_{clk_{HF}} = 1$ MHz. The signal CLK_LF is used to trigger the commands sent by the user. Therefore it is always active. The signal CLK_HF controls the Core Circuit and it is used to generate the DUTY_CYCLE signal used to control switches S_1, S_2 and S_3 of the Core Circuit. The value of the duty cycle for each channel is stored in the memory and it is set in accordance with the bits loaded via the SPI interface.

The basic functionality of the digital control module for biphasic stimulation is illustrated in Fig. 7. The finite state machine (FSM) starts from the IDLE state. As soon as the Trigger command is received, the first phase starts. Depending on the setup stored in the memory for that channel, the first phase can

either be an anodic or a cathodic stimulation phase. The duration of this phase is set by counting the number of CLK_HF periods and it ends when it equals the value stored in the memory for that particular channel. Also the number of pulses in between the two phases, *INTERPHASE DELAY (IPD)* in Fig. 7, is counted and compared to its reference value stored in the memory. To depolarize the cell membrane, the second phase starts. Just as for the first phase, its duration is determined by counting the number of CLK_HF periods and comparing its value to the one stored in the memory. At the end of a biphasic pulse, active charge balancing is implemented. To do so, the residual charge at the tissue-electrode interface is sensed [19]. Based on the sign of the residual charge, a pulse with the opposite sign of the residual charge and the same amplitude is injected into the tissue. Then the residual charge is sensed again and if its sign is the same as before another pulse of the same sign is injected. This sense-inject procedure is repeated until the residual charge changes sign. As a result the residual charge after charge balancing is always lower than the charge transferred by each single high-frequency pulse.

The number of biphasic pulses for each channel is also stored in the memory (*frequency* in Fig. 3). Therefore, after charge balancing, the *Digital Control Module* can decide whether another biphasic pulse is due.

When more channels are used at the same time, the core circuit keeps running at the frequency of 1 MHz, while the digital logic drives the switches of the H-bridge in such a way that all pulses generated by the core circuit are sequentially injected in the activated channels in accordance to the stimulation patterns stored in the memory for each channel. Therefore, when the system operates in multichannel mode each channel receives its own pulse at a frequency $\frac{1\,\text{MHz}}{n}$, where n is the number of channels simultaneously active. This does not affect the efficacy of the stimulation, as shown in [1].

If one would want to keep the frequency at which the pulses are injected into the tissue constant with respect the number of channels being operated, then an additional control (e.g. frequency modulation) has to be used. In such a case, the switching frequency of the DC-DC converter has to increase linearly with the number of channels operated simultaneously. A higher f_{SW} introduces higher switching losses. As a result, the power efficiency would degrade when more channels are used simultaneously.

IV. Experimental Results

This section presents the measurements results of the UHF neural stimulator previously discussed. The circuit was implemented in a standard 0.18 μm high-voltage CMOS process. The chip micrograph is shown in Fig. 8. The total silicon area occupied is 3.65 mm^2.

The system works with two voltage domains: 1.8 V and 3.5 V. The 1.8 V voltage domain is used in the digital control module and in the H-bridge. Switches S_2, S_3 and M_N of Fig. 3 are operated from the 1.8 V voltage domain. The core circuit operates from a voltage domain of 3.5 V.

The voltage waveforms are acquired by means of an oscilloscope (Tektronics TDS2014C), and plotted with MATLAB

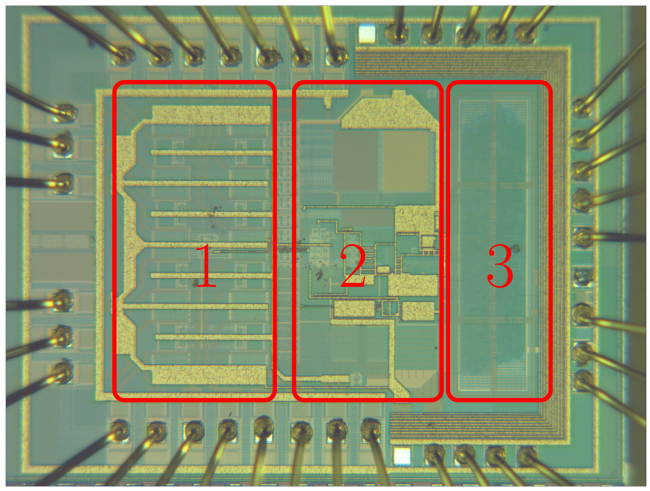

Fig. 8. Photomicrograph of the UHF neural stimulator: (1) H-Bridge. (2) Core Circuit. (3) Digital Control Logic.

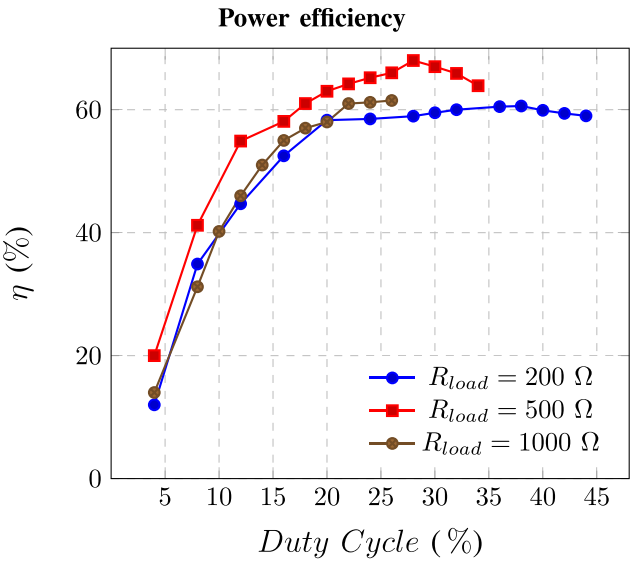

Fig. 9. Measurement results of the power efficiency for different load and duty cycle values.

software. The average currents needed to compute the power efficiency are measured with a Keithley 6430 sourcemeter.

A. Power Efficiency

The only external component of the system is the inductor of 22 μH used in the core circuit.

In Fig. 9, the measurement results of the power efficiency for different values of the duty cycle and different values of the load are shown. The values of R_{load} and the duty cycle determine the amplitude of the output voltage. In Fig. 9, the measurements were stopped when the peak voltage across the load was 18 V. Exceeding this voltage would mean that some transistors would work out of their safe operating region.

The lowest value of the duty cycle (i.e. 4%) corresponds to the lowest ETI voltage ($\approx$2 V). With such a low output voltage, the losses are dominated by the on-resistance of the high-voltage

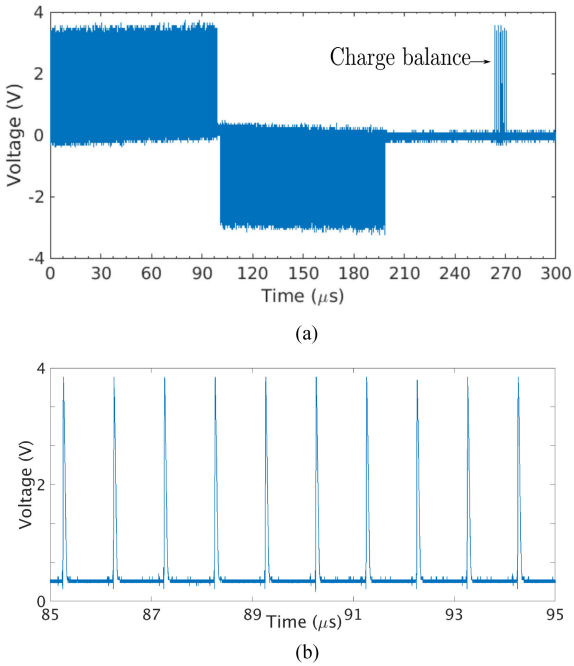

Fig. 10. (a) Single-channel biphasic pulse with $t_{cathod} = 100\,\mu$s, $R_{load} = 200\,\Omega$, $C_{load} = 500$ nF and $duty\ cycle = 15\%$. (b) Zoom showing the high-frequency pulses injected into the RC model electrode.

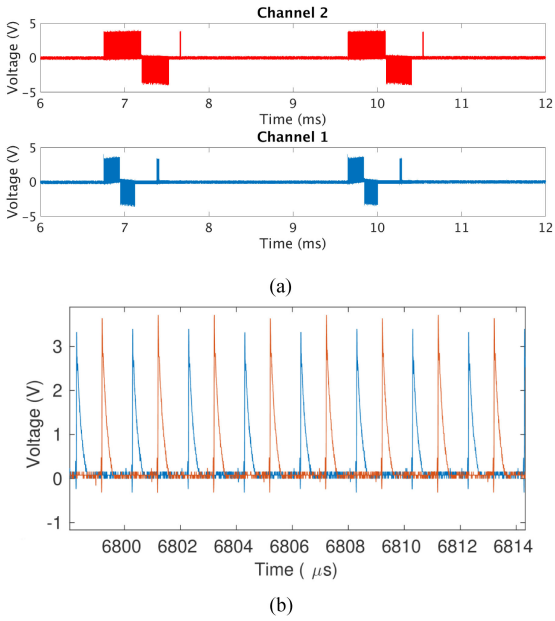

Fig. 11. (a) Multichannel operation when two independent channels are stimulated. For Channel 1: $R_{load} = 500\,\Omega$, $C_{load} = 100$ nF, $duty\ cycle = 8\%$ and for Channel 2: $R_{load} = 200\,\Omega$, $C_{load} = 500$ nF, $duty\ cycle = 15\%$. (b) Zoom of two independent channels operated simultaneously.

switches involved in the conversion, i.e. conduction losses. As the duty-cycle increases, the voltage across the ETI increases and the impact of the conduction losses on the power efficiency becomes less important. Hence, the power efficiency increases. Thanks to the gate driving technique presented in the previous section, the power wasted due to the operation of the switches, i.e. switching losses, stays relatively constant with respect to the duty-cycle. As the duty-cycle increases and approaches its highest values, the switching losses become dominant, as they are proportional to the output voltage. As a consequence, when the duty-cycle increases further, the power efficiency starts degrading.

B. Biphasic Pulse and Multichannel Operation

The authors have not noticed any significant reduction in power efficiency when more channels are used at the same time. Therefore, the power-efficiency measurements shown in Fig. 9 are valid even when 8 channels are operated simultaneously. However, if more channels were to be added to the H-bridge, the parasitic capacitance at node B of Fig. 3 would increase even further. Consequently, the energy wasted due to this parasitic capacitance would increase and the power efficiency would decrease. In Fig. 10, a single-channel biphasic stimulation is shown. The number of pulses injected into the ETI equals 100. Since it is the only channel being stimulated, the duration of the cathodic phase is $t_{cathodic} = 100\,\mu$s.

In Fig. 11 by operating two channels simultaneously, the multichannel operation is illustrated. The 1 MHz pulses generated by the inductor are delivered to the two activated channels in an interleaved fashion, as sketched in Fig. 1 c). Hence, as discussed in Section III C, each channel receives its own pulses every 2 μs. In particular, the anodic phase of Channel 2 is performed while Channel 1 is being stimulated. This means that each channel receives its own pulses every 2 μs.

Part of the cathodic phase of Channel 2 is performed while Channel 1 is not operated. During this time, Channel 2 is the only channel being stimulated, hence it receives its own pulses at a rate of 1 MHz. As a consequence, for Channel 2, the duration of the anodic and the cathodic phases are different.

C. Measurements in Saline Solution

The proposed stimulator has been tested using real electrodes immersed in a phosphate buffered saline (PBS) solution bath. The 8-contact electrodes are commercially used for spinal cord stimulation. For a complete characterization of the electrodes in the PBS solution, electrochemical impedance spectroscopy (EIS) experiments were carried out. Between two electrodes, a 50 mV RMS sinusoidal signal was applied and the impedance was measured using a frequency response analyzer (FRA). The impedance measured between the two electrodes over a 1 Hz–100 kHz frequency range is shown in Fig. 12. The electrode-tissue interface is characterized by two main contributions: a resistive and a capacitive. At a sufficiently high frequency (e.g. $f > 10^3$ Hz) the resistive part of the electrode-tissue interface dominates. Hence, from Fig. 12, we can conclude that $R_{tissue} = 154\,\Omega$. At low frequencies (e.g. $f < 10$ Hz), the impedance of the electrode-tissue interface is dominated by the capacitive contribution. By using a curve fitting technique, the FRA found the capacitive contribution to be $C_{tissue} = 13\,\mu$F.

Fig. 13(a) shows a biphasic stimulation pulse when the electrodes are immersed in a PBS solution. For this stimulation, the settings are $T_{cathode} = 200\,\mu$s and $duty\ cycle = 44\%$, leading

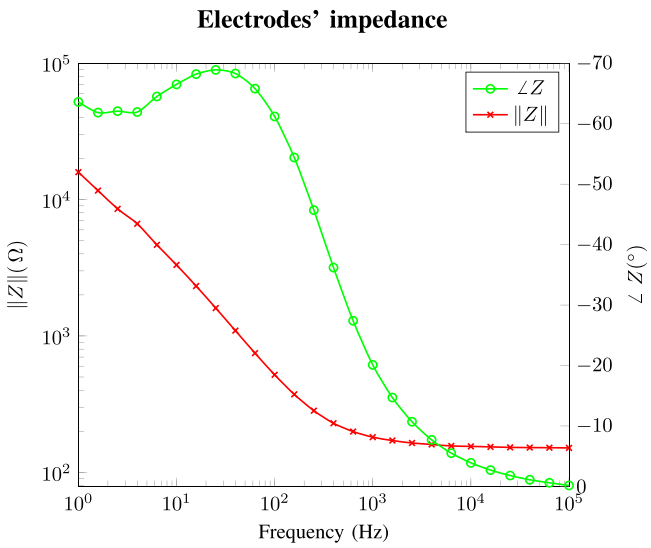

Fig. 12. Module and phase of the electrodes' impedance immersed in the PBS solution bath.

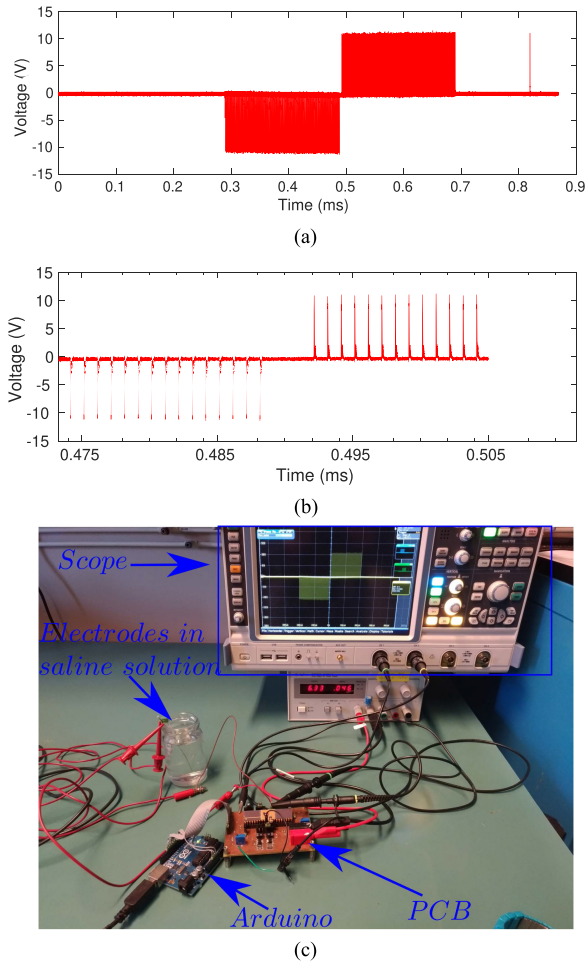

Fig. 13. (a) Measured biphasic stimulation pulse with spinal-cord stimulation electrodes immersed in a PBS solution bath. $t_{cathod} = 200\,\mu s$ and $duty\ cycle = 44\%$. (b) Zoom of the biphasic pulse showing the inter-pulse delay. (c) Detailed measurement setup. An Arduino Uno is used to program the stimulator via an SPI interface, the 8-contact electrode immersed in a PBS solution bath and a Rohde & Schwarz oscilloscope used to capture the waveform.

to a peak stimulating voltage of approximately 11 V. Fig. 13(b), shows the measurement setup in detail.

V. Comparison and Discussion

Many different implementations of neural stimulators can be found in literature. The specifications and constraints of the stimulator heavily depend on its application. One can think of retinal implants and deep brain stimulators. The former tend to have a larger number of electrodes (up to thousands). The latter, however, often deliver more power to the excitable tissue. As a result, evaluating circuits with different specifications and constraints can lead to a meaningless comparison.

In order to have a quantitative evaluation of the performances of various stimulator circuits, a Figure of Merit (FOM) was introduced in [15]. Given a stimulator system with N channels, its FOM is defined as:

$$FOM = \frac{I_{dc}P_{system}}{2N\Delta V_{supply}(I_{cath}T_{cath}f_{stim})^2} \tag{5}$$

where I_{dc} is the residual DC current after charge balancing, P_{system} is the total power consumption, ΔV_{supply} is the maximal compliance of the stimulator, I_{cath} is the average current during the cathodic phase, T_{cath} is the duration of the cathodic phase and f_{stim} is the stimulation rate. The FOM is dimensionless. An ideal neural stimulator has a FOM $= 0$. The FOM of the most recent neural stimulators along with their performance are reported in Table I. The FOM, as defined in [15] is only applicable to CMS and VMS. Hence, Eq. (5) does not hold for [16] and [20], as they present a switched-capacitor based stimulator.

This work, [2], and [21] propose an implementation of a UHF stimulator and tend to have a lower FOM. This is mainly due to the fact that, for UHF stimulators, the maximum stimulation voltage, named ΔV_{supply} in Eq. (5), tends to be higher for any given charge transferred to the tissue (I_{cath} T_{cath}). The stimulator presented in [20] has the highest peak power efficiency (80.4%). However, it requires 2 external storage elements per channel, bringing the total number of external capacitors to 8. Moreover, the 4 channels can be operated neither simultaneously nor independently. Hence, the system presented in [20] does not scale well in applications in which hundreds of channels need to be operated. Likewise in switched-capacitor stimulators, the system in [20] also suffers from power efficiency degradation when the charge delivered to the tissue needs to be regulated.

The proposed design offers a peak power efficiency of 68% with 8 independent channels and only one external component, the inductor, shared among all the channels. Moreover, the need for an external high-voltage power supply is avoided.

In Fig. 14, the power efficiency of the proposed UHF stimulator is compared with our previous implementation [2]. For low duty-cycle values, conduction losses dominate. The output peak voltage is in the order of a few volts and the voltage drop across the diode, which typically is around $V_{DROP} = 0.6$ V, is comparable to the output voltage. Hence, by avoiding the use of the diode, the power efficiency can be boosted up to three times. For low duty cycle values, the power efficiency is now limited by the energy dissipated by the resistor placed between the gate

TABLE I
COMPARISON OF PERFORMANCE

	This work	[3]	[2]	[22]	[14]	[16]	[21]	[23]	[20]
Application	**Gen. Purpose**	Retinal	Gen. Purpose	Gen. Purpose	Nerve Stimulation	Gen. Purpose	Neuroprostheses	DBS	DBS
Process	**0.18 μm**	1.5 μm	0.18 μm	0.35 μm	0.18 μm	0.18 μm	0.6 μm	0.18 μm (low-voltage)	0.35 μm
Operating voltage	**3.5 V**	$\pm$1.75 V	3.5 V	3.3 V	1.8 V	5 V	5 V	3.3 V	$\pm$2.1 V
Channels	**8**	1	8	1	8	1	1	1	4
Electrodes	**16 (fully arbitrary)**	15 (monopolar)	16 (fully arbitrary)	2	16 (Non-reconfigurable)	2	2	2	8
HV Generation	**Not needed**	Inductive link	External 20 V	N.A.	Integrated Charge pump	On-Chip	External 12 V	Integrated Charge pump	-
Stimulator peak Efficiency	**68 %**	39%	57%	35 – 50%	82% (DC-DC converter only)	49%	–	56%	80.4%
Stimulation type	**CMS**	CMS	CMS	CMS	CMS	SCS	CMS	CMS	SCS
FOM ($*10^3$)	**0.0075**	0.4	0.009	–	71.2	*N.A.*	1.15	0.67	*N.A.*
Stimulation Current	**$<$ 10 mA**	0.4 mA	$<$ 10 mA	$<$ 450 μA	2 μA – 504 μA	-	<= 1 mA	0.2 mA – 3 mA	<= 4 mA
Load Impedance	**100 Ω – 1 $k\Omega$**	1.15 $k\Omega$	100 Ω – 1 $k\Omega$	500 Ω – 2 $k\Omega$	-	1.79k Ω – 4.8 $k\Omega$	-	4 kΩ	0.5 kΩ
Multichannel Efficiency	**Yes**	No	Yes	No	Yes	No	Yes	No	No
# of external components	**1**	N.A.	1	3	0	0	0	0	8

when implemented on SOI technology.

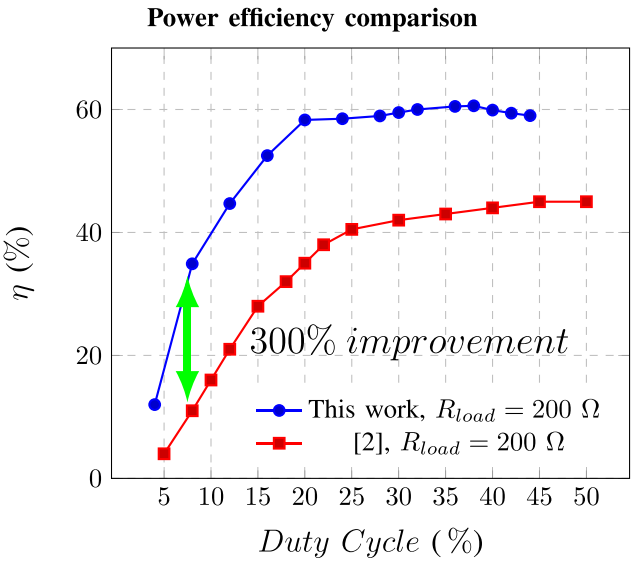

Fig. 14. Power efficiency comparison when the ETI is modeled as $R_{load} = 200\,\Omega$, $C_{load} = 500$ nF.

and source terminal of transistor M_P of Fig. 3. Implementing an even more efficient gate-driving technique would allow, for low duty-cycle values, to boost the power efficiency even further.

The main limitation to increase the number of electrodes even further is the gate-to-source parasitic capacitance of all the M_P switches connected at Node B (Fig. 3). This limitation can be easily overcome in applications, in which the stimulating current is in the order of μA. This allows to reduce the size, and therefore the parasitic gate-to-source capacitance, of the M_P switches. If we reduce the current delivered to the tissue by 10 times, the size of each M_P transistor can be reduced by the same amount. This would allow, given the same parasitic capacitance at Node B, to have 10 times more electrodes, bringing the total number of electrodes to 160. Another approach to increase the number of electrodes without increasing the capacitance at Node B would be to arrange the H-bridge in several blocks. Each block is made of a fixed number of electrodes (e.g. 16) and one additional switch that connects the block to Node B. Every time a pulse is generated by the core circuit, the digital control module decides which block is used and within the block which pair of electrodes receives the pulse. A combination of the two mentioned approaches could scale the number of electrodes up to several hundreds.

VI. CONCLUSION

This paper presents the design and the measurements results of an 8-channel current-mode neural stimulator. A novel zero current detection scheme has been discussed which allows to remove the freewheel diode usually used in DC-DC converters. A gate-driver circuit allows the use of thin-oxide transistors as high-voltage switches, eliminating the need to control the switches from an external high-voltage supply. A prototype IC was fabricated in a standard CMOS process. Measurements results show a peak power efficiency of 68% and prove multichannel operation. The implementation presented in this work achieves the lowest FOM with respect to the state of the art.

ACKNOWLEDGMENT

The authors would like to thank Kambiz Nanbakhsh for his help during the characterization of the electrodes and Ali Kaichouhi for his technical support during tape out.

REFERENCES

[1] M. N. van Dongen, F. E. Hoebeek, S. K. E. Koekkoek, C. I. De Zeeuw, and W. A. Serdijn, "High frequency switched-mode stimulation can evoke post synaptic responses in cerebellar principal neurons," *Frontiers Neuroeng.*, vol. 8, p. 2, 2015.

[2] M. N. van Dongen and W. A. Serdijn, "A power-efficient multichannel neural stimulator using high-frequency pulsed excitation from an unfiltered dynamic supply," *IEEE Trans. Biomed. Circuits Syst.*, vol. 10, no. 1, pp. 61–71, Feb. 2016.

[3] S. K. Kelly and J. L. Wyatt, "A power-efficient neural tissue stimulator with energy recovery," *IEEE Trans. Biomed. Circuits Syst.*, vol. 5, no. 1, pp. 20–29, Feb. 2011.
[4] E. K. Lee, E. Matei, V. Gang, J. Shi, and A. Zadeh, "A multiple-output fixed current stimulation ASIC for peripherally-implantable neurostimulation system," in *Proc. IEEE Custom Integr. Circuits Conf.*, 2014, pp. 1–4.
[5] Y. Tao and A. Hierlemann, "A 15-channel 30-V neural stimulator for spinal cord repair," *IEEE Trans. Very Large Scale Integration (VLSI) Syst.*, vol. 26, no. 10, pp. 2185–2189, Oct. 2018.
[6] M. Shrivastav and S. Musley, "Spinal cord stimulation for complex regional pain syndrome," in *Proc. 31st Annu. Int. Conf. IEEE Eng. Medicine Biol. Soc.: Eng. Future Biomedicine*, 2009, pp. 2033–2036.
[7] T. M. Wascher, "Rechargeable spinal cord stimulators for chronic pain (Research Article)," pp. 1/2, 2005. [Online]. Available: https://www.spinehealth.com/treatment/pain-management/rechargeable-spinal-cord-stimulators-chronic-pain-research-article
[8] X. Li, W. A. Serdijn, W. Zheng, Y. Tian, and B. Zhang, "The injectable neurostimulator: An emerging therapeutic device," *Trends Biotechnol.*, vol. 33, no. 7, pp. 388–394, 2015. [Online]. Available: http://dx.doi.org/10.1016/j.tibtech.2015.04.001
[9] V. Giagka and W. A. Serdijn, "Realizing flexible bioelectronic medicines for accessing the peripheral nerves technology considerations," *Bioelectronic Medicine*, vol. 4, p. 8, 2018. [Online]. Available: https://bioelecmed.biomedcentral.com/articles/10.1186/s42234-018-0010-y
[10] H. Xu, E. Noorsal, K. Sooksood, J. Becker, and M. Ortmanns, "A multichannel neurostimulator with transcutaneous closed-loop power control and self-adaptive supply," *Eur. Solid-State Circuits Conf.*, pp. 309–312, 2012.
[11] K. Sooksood, E. Noorsal, J. Becker, and M. Ortmanns, "A neural stimulator front-end with arbitrary pulse shape, HV compliance and adaptive supply requiring 0.05 mm^2 in 0.35 μ m HVCMOS," *Digest Tech. Papers—IEEE Int. Solid-State Circuits Conf.*, vol. 4, no. 3, pp. 306–307, Feb. 2011.
[12] E. Noorsal, K. Sooksood, H. Xu, R. Hornig, J. Becker, and M. Ortmanns, "A neural stimulator frontend with high-voltage compliance and programmable pulse shape for epiretinal implants," *IEEE J. Solid-State Circuits*, vol. 47, no. 1, pp. 244–256, Jan. 2012.
[13] C. Y. Lin, W. L. Chen, and M. D. Ker, "Implantable stimulator for epileptic seizure suppression with loading impedance adaptability," *IEEE Trans. Biomed. Circuits Syst.*, vol. 7, no. 2, pp. 196–203, Apr. 2013.
[14] I. Williams and T. G. Constandinou, "An energy efficient dynamic voltage scaling neural stimulator for a proprioceptive prosthesis," *IEEE Trans. Biomed. Circuits Syst.*, vol. 7, no. 2, pp. 129–139, Apr. 2013.
[15] F. Kolbl and A. Demosthenous, "A figure of merit for neural electrical stimulation circuits," in *Proc. Annu. Int. Conf. IEEE Eng. Med. Biol. Soc.*, vol. 2015, 2015, pp. 2075–2078.
[16] W. Y. Hsu and A. Schmid, "Compact, energy-efficient high-frequency switched capacitor neural stimulator with active charge balancing," *IEEE Trans. Biomed. Circuits Syst.*, vol. 11, no. 4, pp. 878–888, Aug. 2017.
[17] T. V. Breussegem and M. Steyaert, *CMOS Integrated Capacitive DC-DC Converters*. New York, NY, USA: Springer, 2013.
[18] S. K. Manohar and P. T. Balsara, "94.6% peak efficiency DCM buck converter with fast adaptive dead-time control," in *Proc. Eur. Solid-State Circuits Conf.*, 2013, pp. 153–156.
[19] K. Sooksood, T. Stieglitz, and M. Ortmanns, "An active approach for charge balancing in functional electrical stimulation," *IEEE Trans. Biomed. Circuits Syst.*, vol. 4, no. 3, pp. 162–170, Jun. 2010.
[20] H. M. Lee, K. Y. Kwon, W. Li, and M. Ghovanloo, "A power-efficient switched-capacitor stimulating system for electrical/optical deep brain stimulation," *IEEE J. Solid-State Circuits*, vol. 50, no. 1, pp. 360–374, Jan. 2015.
[21] D. Jiang and A. Demosthenous, "A multichannel high-frequency power-isolated neural stimulator with crosstalk reduction," *IEEE Trans. Biomed. Circuits Syst.*, vol. 12, no. 4, pp. 940–953, Aug. 2018.
[22] S. K. Arfin and R. Sarpeshkar, "An energy-efficient, adiabatic electrode stimulator with inductive energy recycling and feedback current regulation," *IEEE Trans. Biomed. Circuits Syst.*, vol. 6, no. 1, pp. 1–14, Feb. 2012.
[23] Z. Luo and M. D. Ker, "A high-voltage-tolerant and power-efficient stimulator with adaptive power supply realized in low-voltage CMOS process for implantable biomedical applications," *IEEE J. Emerging Sel. Topics Circuits Syst.*, vol. 8, no. 2, pp. 178–186, Jun. 2018.

Alessandro Urso (S'16) was born in the province of Lecce, Italy, in 1991. He received the bachelor's degree and the M.Sc. degree (*cum laude*) in electronic and telecommunications engineering from the University of Ferrara, Italy, in 2013 and 2015, respectively. He is currently a Ph.D. candidate at the Section Bioelectronics of Delft University of Technology, Delft, The Netherlands. His research interests include the design of power efficient neural stimulators as well as the design of switched-capacitor dc–dc converters for energy-harvesting applications.

Vasiliki Giagka (S'10–M'15) was born in Athens, Greece, in 1984. She received the M.Eng. degree in electronic and computer engineering from the Aristotle University of Thessaloniki, Thessaloniki, Greece, in 2009. She then moved to London to join the Analogue and Biomedical Electronics Group, University College London, U.K. from where she received the Ph.D. degree in 2014. In 2015, she joined the Implanted Devices Group, University College London, as a Research Associate. Since September 2015, she has been an Assistant Professor with the Bioelectronics Group, Delft University of Technology, Delft, The Netherlands, and since September 2018 she has also been leading the group technologies for Bioelectronics, Fraunhofer Institute for Reliability and Microintegration IZM, Berlin, Germany. Between her two affiliations, she is carrying out research on the design and fabrication of active neural interfaces. In particular she is investigating new approaches for neural stimulation and wireless power transfer, as well as implant miniaturization, microsystem integration, packaging and encapsulation to meet the challenges of bioelectronic medicines.

Marijn van Dongen (S'11–M'14) was born in Pijnacker, The Netherlands, in 1984. He received the M.Sc. and Ph.D. degrees in electrical engineering from the Delft University of Technology, Delft, The Netherlands, in 2010 and 2015, respectively. Currently he is working for NXP Semiconductors, Nijmegen, The Netherlands, where he is involved in the design of ICs for automotive applications. His research interests include the design of neural stimulator output circuits as well as the modeling of the electrophysiological and electrochemical processes during electrical stimulation. Dr. van Dongen served as the Financial Chair of the IEEE BioCAS2013 Conference.

Wouter A. Serdijn (M'98–SM'08–F'11) was born in Zoetermeer (Sweet Lake City), The Netherlands, in 1966. He received the M.Sc. (*cum laude*) and Ph.D. degrees from the Delft University of Technology, Delft, The Netherlands, in 1989 and 1994, respectively. Currently, he is a Full Professor of Bioelectronics with the Delft University of Technology, where he heads the Section Bioelectronics. He teaches circuit theory, analog integrated circuit design, analog CMOS filter design, active implantable biomedical microsystems, and bioelectronics.

He is the coeditor and coauthor of 10 books, 8 book chapters, 3 patents, and more than 300 scientific publications and presentations. His research interests include integrated biomedical circuits and systems for biosignal conditioning and detection, neuroprosthetics, transcutaneous wireless communication, power management and energy harvesting as applied in, e.g., hearing instruments, cardiac pacemakers, cochlear implants, neurostimulators, portable, wearable, implantable and injectable medical devices, and electroceuticals.

Prof. Serdijn is an IEEE Distinguished Lecturer and a mentor of the IEEE. He was the recipient of the Electrical Engineering Best Teacher Award in 2001, 2004, and 2015, and IEEE Circuits and Systems Society Meritorious Service Award in 2016. He has served, a.o., as a General Co-Chair for IEEE ISCAS 2015 and for IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS (BioCAS) 2013, Technical Program Chair for IEEE BioCAS 2010, and for IEEE ISCAS 2010, 2012, and 2014, as a member of the Board of Governors of the IEEE Circuits and Systems Society (2006–2011), as a Chair of the Analog Signal Processing Technical Committee of the IEEE Circuits and Systems Society, and as Editor-in-Chief for IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS-I: REGULAR PAPERS (2010–2011). He is currently the Chair of the Steering Committee and an Associate Editor of the IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS.