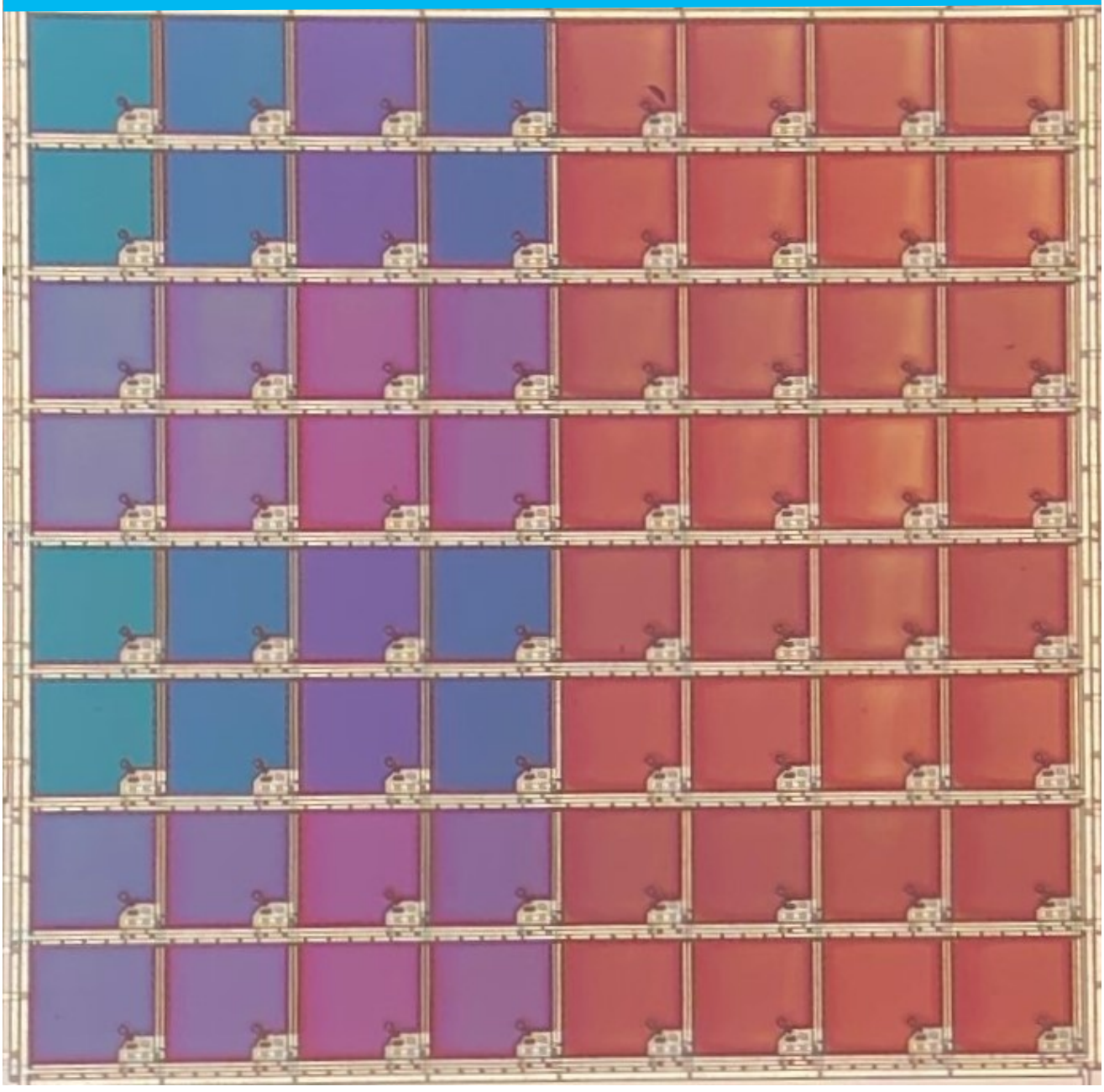
Design and Realization of a Lensless CMOS Image Sensor for Light Source Tracking

S. Şanseven



TU Delft Delft University of Technology

Design and Realization of A Lensless CMOS Image Sensor for Light Source Tracking

by

Seçil Sanseven

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TU Delft

Abstract

Localization of a light source in the space requires capturing its light intensity and angle information. However, conventional CMOS image sensors can only capture the light intensity and wavelength. These sensors need to be augmented with an optical extension such as an aperture or a lens in order to capture the angle information. The use of optical apertures presents various drawbacks regarding the need for calibration, difficulty of miniaturization and CMOS integration. This work presents a lensless CMOS image sensor architecture for light source tracking applications, thereby eliminating the need for an optical aperture for angle sensitivity. The proposed design of angle-sensitive pixels (ASPs) with 1 μm, 1.5 μm, and 2 μm grating pitches is implemented on a 5.6x5.6 mm^2 photodiode array. The fabricated ASP device with 2 μm grating pitch can resolve angles up to 0.37°accuracy with post-process characterization. Furthermore, a metal shading structure is incorporated to the pixel array for coarse angle detection which determines the incident angle's location on the periodic ASP response.

Acknowledgements

There were many people who contributed to the success of this work with their help. First of all, I would like to thank my supervisor Sten for his guidance and invaluable insights all throughout my thesis. His enthusiasm, commitment and knowledge has continued to inspire me at each meeting. Secondly, I thank my daily supervisor Joost who was involved at every step of this work with his guidance and help. I learnt a lot from him during the past twelve months. He gave me technical insights but more often he helped me find my own ways and approaches within the project. I thank the people of ECTM; PhD students for their help in and out of the cleanroom, secretaries for helping me arrange all the shipments for implantation and Filip for his help with dicing and packaging of my fabricated devices. I also thank the people of EKL who never stopped to surprise me with their knowledge of the cleanroom and their generosity to share it. I am also grateful for their warmth and kindness which made me feel like a part of the cleanroom, or rather made the cleanroom a part of me. The optical setup was built thanks to the contributions of dr. ir. Ger de Graaf who opened the doors of this optical lab to me and Tianyi Jin who helped me with the light sources. I would like to thank both of them. Furthermore, I thank Shriya and my fellow MSc students at ECTM, who became my dear friends along the way for their joyful company and support. I also thank my friends at home; Zeynepcan, Elifsu and Özüm for always believing in me more than I believe in myself. Finally, I thank my family; my mum, my dad and my brother for their endless support in everything I do.

Preface

This thesis is a part of the Master graduation program that is conducted in partial fulfillment for the degree Master of Science in Electrical Engineering. The thesis project was performed for twelve months and during the project, lensless angle-sensitive pixels were successfully designed, fabricated and characterized. In doing so, lensless CMOS image sensors for angle detection and light source localization were successfully presented.

The first stage of the project consisted of a literature review that focused on the lensless CMOS image sensors to identify the state-of-the-art angle detection techniques and to assess their manufacturability in EKL. I also went through the cleanroom process integration training during this stage, which gave me a lot of insight on the available fabrication processes.

During the next phase, COMSOL Multiphysics simulations were performed in order to create a complete overview of proposed pixel architectures. Based on the characterization of these pixel, design parameters were determined. Following the design of the pixel geometry, layout design of the pixel array as well as the read-out electronics was implemented. Joost has shared his sun position sensor layout with me, which became my guidebook of layout design and formed the starting point of my own design. ASP gratings layers were implemented both on Joost's existing design and my new pixel design.

In the following stage, designed sensor architectures were fabricated in EKL. Fabrication was started in mid-May and the first full wafer was completed by the end of August. Unfortunately, I couldn't complete the fabrication of my own device design during my processing time in EKL. The ion implanter broke down right after the N-well definition and the rest of the implantation steps had to be completed by an external company eventually. During this time, Joost trusted his implanted wafers with me that made the successful completion of this work possible.

The final stage was the optical measurements and characterization of the fabricated device. For this purpose, an optical setup was built that allowed accurate angular rotation of the angle-sensitive chip and its coherent illumination with red light. 2 μm pitch amplitude grating based ASPs were measured and angle detection was successfully demonstrated within ±26°range.

The thesis committee consists of prof. dr. Guoqi Zhang, my supervisor dr. Sten Vollebregt, my daily supervisor Joost Romijn and dr. Olindo Isabella from PVMD group.

Seçil Sanseven
Delft, November 2021

Contents

1 Introduction **1**

1.1 Problem Formation . . . 2

1.2 Research Objectives and Outline . . . 2

2 Background Theory **5**

2.1 Diffraction gratings . . . 5

2.1.1 Amplitude Gratings . . . 6

2.1.2 Phase Gratings . . . 8

2.2 Odd-symmetry Spiral Phase Gratings . . . 9

2.3 Metal Shading Pixel . . . 10

2.4 Hybrid Methods . . . 11

2.4.1 Track-and-tune Architecture . . . 11

2.4.2 Polarization-based Pixels . . . 11

2.5 Conclusion . . . 12

3 Simulations **15**

3.1 Angle sensitive pixels and Talbot effect . . . 15

3.2 Characterization and design of angle sensitive pixels . . . 16

3.2.1 Grating metal . . . 17

3.2.2 Grating pitch . . . 17

3.2.3 Duty cycle . . . 18

3.2.4 Intergrating distance . . . 18

3.2.5 Grating thickness . . . 19

3.2.6 Grating depth . . . 20

3.2.7 Overetch . . . 20

3.2.8 Summary & Final ASP Design . . . 20

3.3 Characterization and design of metal shading structure . . . 21

3.3.1 Metal shading method and angle detection . . . 21

3.4 Conclusion . . . 24

4 Read-out Electronics and Layout Design 25

4.1 Background on 3T active pixel read-out . . . 25

4.2 Read-out Electronics . . . 26

4.3 Layout Design . . . 27

4.3.1 Angle-Sensitive Pixel (ASP) Layout Design . . . 27

4.3.2 Active Pixel Read-out Layout . . . 29

4.3.3 Metal Shading Pixel Layout . . . 30

4.4 Photomasks . . . 30

5 Fabrication 33

5.1 BiCMOS Process . . . 33

5.2 Fabrication of the grating stack . . . 36

5.3 Optimization of Linewidths . . . 40

5.3.1 Lithography . . . 40

5.3.2 Development . . . 43

5.3.3 Etching . . . 43

5.4 Fabrication-related Challenges . . . 43

5.5 Fabrication Results and Conclusion . . . 44

5.5.1 Fabrication verification . . . 47

6 Measurements & Device Characterization 49

6.1 Optical Measurement Setup . . . 49

6.2 Device Characterization . . . 51

6.2.1 Measurement Results . . . 52

6.3 Conclusion . . . 55

7 Conclusions and Future Work 57

7.1 Summary of Research Conclusions . . . 57

7.2 Future Work and Recommendations . . . 58

A List of Acronyms 59

B List of Symbols 61

C Simulations **63**

D Layout **65**

E Fabrication **69**

F Process Flow **75**

1

Introduction

Attitude control system is an indispensable part of an aerospace vehicle that identifies and controls the position of an aircraft. The system is made up of two essential parts: a sensor to measure the orientation of the vehicle and a control system to steer the vehicle in the desired direction. The sensing part, also referred to as attitude determination, can be realized either with respect to the initial frame of reference of the craft or with respect to a celestial body in space. Many satellites and spacecraft around the orbit of the Earth make use of the latter method, using the sun as the point of reference to position themselves. These sun sensors, also called sun position sensors, determine the relative position of the spacecraft to the sun using the sun beams reaching the surface of the sensor architecture. Sun sensors can vary in their principle of working, however the research on this field mainly takes these four types into its focus: collimating sensor, sun-pointing sensor, tilted mount photo sensor and hybrid sensor [1]. Although used extensively in attitude control of satellites thanks to their low-cost and simple structures, sun position sensors commonly make use of optical extensions on top of the photo-sensitive bulk of the sensor. Collimating sensors are usually accompanied with an optical mask with apertures or a set of lenses in order to collimate the incident light. These lenses can be very thick and wide in order to successfully collimate the light. Up to 20 mm lens thickness and 100 mm lens diameter are reported in the literature [1]. The use of lenses limit the miniaturization of the sun sensors substantially. Furthermore, these architectures require calibration since small offsets in the alignment of optical apertures to the light-sensitive pixel area can distort the angle response of the sensor. One such example of a collimating sun sensor that uses a mask and an aperture-array is given in Figure 1.1. Incident sun light is collimated through the aperture-array and illuminates a certain coordinate on the image sensor below depending on its incident angle.

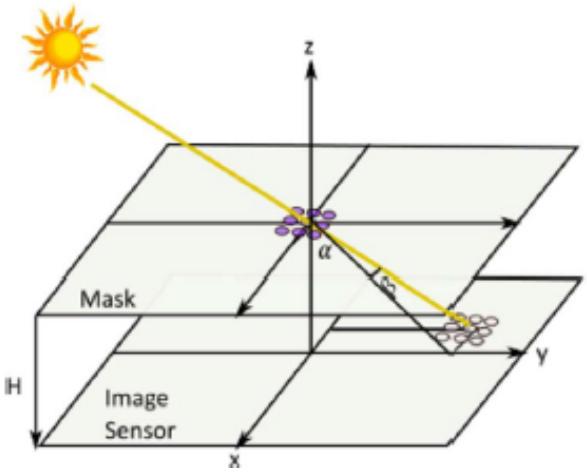


Figure 1.1: Collimating sun sensor [2]

Nowadays, the space industry faces an increasing trend of satellite miniaturization. New small satellites are becoming an important tool for Earth and planetary observation. This is made possible mainly due to their low-cost manufacturing and launching which opens the space to commercial and academic explorers. Additionally, constellation of small satellites enable more comprehensive observation of the celestial bodies in shorter timescales. Compared to traditional large satellites that weight more than thousand kilograms, small satellites' weight can range between half ton and one kilogram. These group of micro- and nanosatellites come with their own special challenges one of which being the attitude control. These new set of challenges mainly stem from the requirement for a light-weight, scalable, low-power and low-cost attitude determination system. Eliminating the need for the optical augmentation and post-process calibration are also desired properties on the way for the mass production of new generation sensors. Other requirements can be brought upon by the harsh environment of space, such as temperature range and durability [3].

Considering the needs of emerging small satellite market, CMOS image sensors come forward as an appealing options for light-source tracking applications. Thanks to the trend predicted by Moore in the 60's [4], microelectronics technology has witnessed constant shrinking of feature sizes from which modern CMOS sensors benefited greatly. These advancements in integrated circuit technology enables CMOS image sensors to offer great sensing performance with the advantages of pixel scaling and electronic integration [5].

1.1. Problem Formation

In order to identify the location of a light source in the space, capturing its light intensity and angle information are two crucial prerequisites. However, conventional CMOS image sensors can only capture the light intensity and wavelength. In order to capture the angle information, these sensors are augmented with an extra optical part such as aperture or lens. In the example of collimating sensors as shown in Figure 1.1, light is collimated through a pin hole and directed on a specific quadrant of the pixel array which represents the angle information. Accuracy of this kind of sensors depends greatly on the optimization and costly calibration of the optical apertures. Field of view (FOV) is another concern, since active photosensitive area must increase with the larger incident angles. These augmentations also tend to make the sensor vulnerable to fabrication errors and limit the miniaturization of the sensor. They also tend to be bulky structures due to the large dimensions of the optical extensions. These drawbacks of current sun sensors make their integration with miniaturized solar technologies difficult. Eliminating the need for an optical augmentation and realizing a lensless architecture help greatly with the improvement of the above-listed drawbacks of traditional sun sensor architectures.

The main motivation for this project is realization of scalable lensless angle-sensitive CMOS image sensor for light source tracking that eliminates the need for calibration. These points can be summarized in the following research question:

Can a lensless image sensor architecture be realized in standard CMOS technology for light source tracking applications?

1.2. Research Objectives and Outline

Following research objectives are defined in order to successfully answer the formulated research question and realize the proposed solution to this research's main problem. Each objective constitutes an important research stage during the time span of this thesis work, and are implemented with the given order. Research goals are documented in separate chapters as listed here:

1. Study of lensless CMOS image sensor architectures
   This aims to provide the required background information on the state-of-art architectures in the literature and identify the most suitable structures to realize the proposed solution. The findings of the literature review are presented in Chapter 2.

2. Characterization and design of the proposed angle-sensitive architectures
   This part of the research aims to study the proposed angle-sensitive structure more extensively to characterize its principle of operation as well as the design parameters. Following the characterization, a design is proposed based on the findings of the simulation and mathematical models. The results of this part are given in Chapter 3.

3. Realization of the optimized architecture for light source tracking This stage of the research is based on the previous work of Romijn, et al. on the scalable sun sensor architecture using the principle of collimation [6]. Design of the read-out electronics and layout as well as CMOS fabrication flow are developed with taking this work as the base point. Realization of the proposed pixel design comprises of two sub-research stages:

   (a) Design of the read-out electronics and IC layout of the chip In this part, layout of active-pixel read-out circuitry and pixel array is design according to the proposed design. On-chip electronics and IC layout are presented in Chapter 4.

   (b) Fabrication of the proposed architecture Fabrication flow is designed and fabrication of the designed layout is done in Else Kooi Laboratory (EKL) using BiCMOS processing. The details of the fabrication are explained in Chapter 5 with the reasonings for the fabrication choices.

4. Characterization of the fabricated structures Final part of this research is the post-fabrication characterization of the manufactured chips with electrical and optical measurements. The measurement setup and results are discussed in Chapter 6.

Lastly Chapter 7 concludes this thesis and provides recommendations on the future work. At the end of this document, Appendix is included with a list of acronyms and symbols, additional figures and process flowchart.

2

Background Theory

This chapter presents an introduction to the image and angle sensors in the literature. All structures included to this chapter are fabricated in standard CMOS technology and they are not augmented with any optical aperture or lens. Although many of the techniques that will be discussed are developed for imaging applications and reconstruction of the 3D images from the pixel information, they form a basis for this background theory as angle detection is an important part of the 3D image capturing.

2.1. Diffraction gratings

One of the earliest also the most prominent lensless 3D imaging architectures in the literature is based on Talbot effect. According to this optical phenomenon, first observed by English scientist Talbot in 1836, diffraction grating illuminated by a monochromatic light source creates strong intensity patterns at certain depths in the substrate [7]. These intensity patterns, referred to as 'self-images', form at the integer multiples of Talbot depth given in Equation 2.1 where d symbolizes the grating pitch and λ_n the wavelength of the incident light in the dielectric. Important observation from this equation is the absence of angle information θ. This signifies that Talbot depth is independent from the incident angle.

$$z_T = 2\frac{d^2}{\lambda_n} \tag{2.1}$$

Periodic diffraction gratings display another optical effect called off-axis Talbot effect. This refers to the lateral shift of self-images on the same Talbot depth with the changing incident angle [8]. Both Talbot and off-axis Talbot effects are visualized in Figure 2.1. Figure 2.1.b shows the self-images occurring at half-Talbot depths meanwhile Figure 2.1.c illustrates the effect of incident angle on the created pattern via off-axis Talbot effect. The peaks of the light intensity shift towards left as the incident angle is increased from 0 degrees to 5 degrees. Measuring this shift of self-images can help detect the angle information [8].

There are two approaches to identifying the shift in the intensity pattern and thus extracting the incident angle [9]. The first and the most straightforward one is to place a photodiode array underneath the diffraction gratings. However, this method requires photodiodes to have smaller feature sizes than the pitch of the gratings since the intensity pattern has the same periodicity as the gratings.These small interleaved photodiodes lead to lowered resolution of the captured information, additionally presenting serious manufacturing challenges [8]. Carrier effects between these narrow diodes should also be considered for a successful design. The second approach is using a second grating layer, at the Talbot depth, which filters the light field created by the primary diffraction grating layer. This second layer, called analyser grating and having the same characteristics as the first one, allows the light to pass

through to the silicon substrate when peaks of the intensity pattern are aligned with the gaps of the grating and it blocks the light when peaks are aligned with the lines of the grating [9]. This additional optical modulation of the light allows the use of single large photodiode to sample the complete angle information.

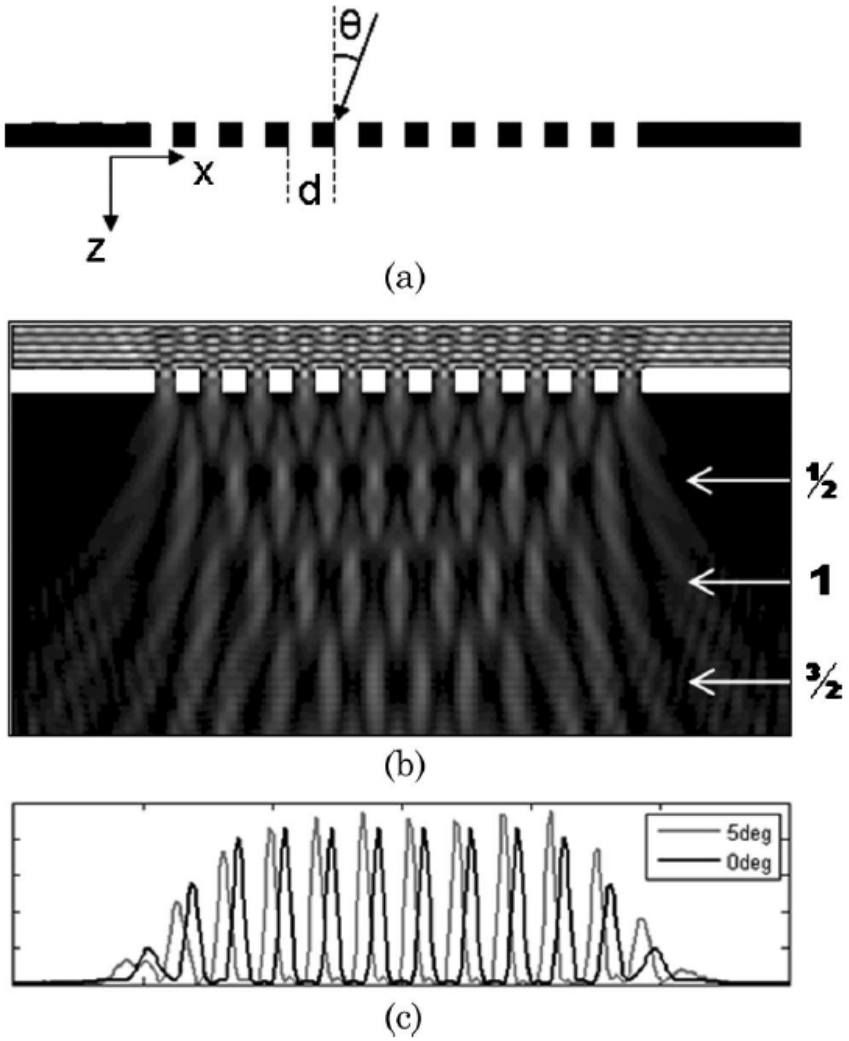


Figure 2.1: Talbot effect.(a) Diffraction grating with period d (b) Talbot self-images observed at various depths (c) Intensity pattern of the self-images showing off-axis Talbot effect [8]

Depending on the nature of its angle modulation, diffraction gratings can be divided into two different grating types, *amplitude and phase gratings*. Amplitude gratings modulate the amplitude information of the signal and leaves the phase information unchanged. Phase gratings, on the other hand, modulate the phase of the signal and leave the amplitude information unchanged. Following subsections will discuss the characteristics of each of these diffraction gratings with an analyser layer implemented underneath for angle detection.

2.1.1. Amplitude Gratings

Amplitude grating-based pixels, referred as ASPs (angle sensitive pixel) in the literature, consist of two identical opaque layers of periodic gratings that are separated by a certain multiple of Talbot depth. Cross-sectional image of an ASP is given in Figure 2.2. In the figure, diffraction gratings are highlighted in blue whereas the analyser gratings are given in green. Grating stack is placed over a large single photodiode area. Transfer function of ASPs is empirically derived by Gill et al. and it is shown in Equa-

tion 2.2, where $F(\theta)$ represents the non-idealities and noise, V the photodiode response, I_0 intensity coefficient, m modulation depth, β angular sensitivity, θ angle of the incident light and α phase offset between two grating layers. α, β and m are geometry-dependent parameters [10].

$$V = I_0 * (1 - mcos(\beta\theta + \alpha))F(\theta) \tag{2.2}$$

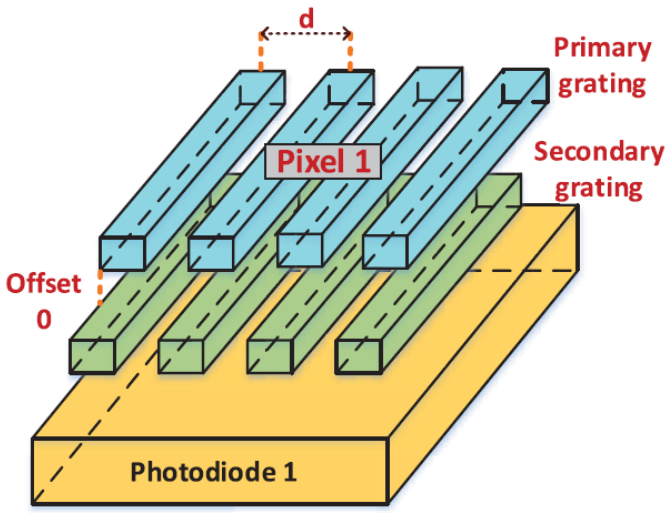


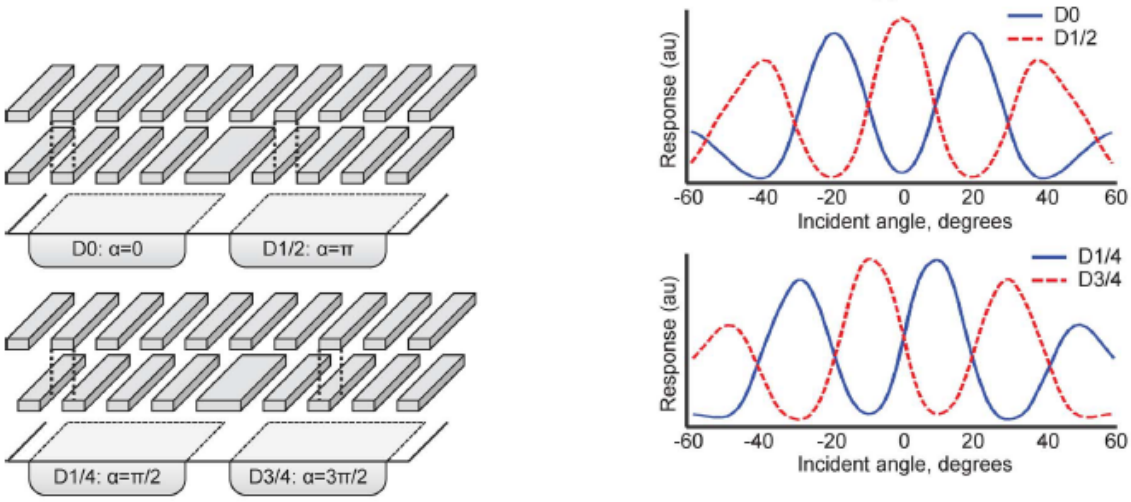
Figure 2.2: Structural cross-section of an ASP [11]

Response of the photodiode, represented in Equation 2.2, shows a sinusoidal pattern and it contains both angle and intensity information. Hence, when single pixel is employed, it is not possible to differentiate a small incident angle with high intensity and a high incident angle with low intensity from each other simply due to the number of unknowns in the equation. Thus, it becomes a necessity to either know the light intensity or implement a differential measurement architecture that eliminates the need to know the light intensity. Second method is preferable for multiple reasons, the most important of which being the noise and other non-ideality cancellation of differential measurement. This way, both $F(\theta)$ and m are removed from the equation, and only sinusoidal angle information is left.

Four different pixels, all with different phase offsets are employed in the design to be able to extract the incident angle [9]. As identified by parameter α in Equation 2.2, each $\pi/2$ phase shift between the gratings changes the photodiode response between cosine and sine waves. Phase offsets and the resulting photo responses are illustrated in Figure 2.3. As shown on the figure, bottom grating layer is shifted by a certain offset with respect to the top grating layer. Sum of each pixel pair corresponds to the intensity information, while their difference contains the angle information. Thus, the angle can be derived using the response from four pixels as shown in Equation 2.3. V_0, V_{14}, V_{12} and V_{34} represent the pixels with 0, $\pi/2$, π and $3\pi/2$ phase offsets, respectively.

$$\theta = \frac{1}{\beta} * tan^{-1}(\frac{V_{14} - V_{34}}{V_{12} - V_0}) \tag{2.3}$$

The measure of angular sensitivity, β, an important unitless parameter to characterize the angle detection properties of an ASP. It determines the number of individually resolvable angles in the angular response. Higher angular sensitivity creates larger change in the angular response compared to lower angular sensitivity pixels for the same angle variation [11]. Angular sensitivity can be calculated from the design parameters of the device using Equation 2.4, where n is the refractive index of the dielectric.



(a) Phase offsets of four ASPs

(b) Photodiode responses corresponding to each phase offset

Figure 2.3: Phase offsets in ASP [12]

$$\beta = 2\pi \frac{Z_T}{n * d} \tag{2.4}$$

Double-grating structures demonstrate how small arrays of ASPs, fabricated using standard CMOS technology, can successfully identify the variations in the incident angle of the light hence the location of the light source. However, being the earliest lensless architecture, regular ASPs also have many drawbacks. The first one is the requirement of four different phase offsets to solve the ambiguity between the angle and the intensity of the incident light. Secondly, there is a trade-off between the range of detectable angles and the angular sensitivity. This limitation can be explained by the tan^{-1} in the final angle equation whose range lies between -90°and +90°. If angular sensitivity is 1°, all 180 degrees can be identified individually. However, if design has higher angular sensitivity, such as 20, the angular response shows a repeating pattern with 9°periods. Hence, this leads to having pixels with different angle sensitivities (ranging from low to high) to capture richer information of the light source [13]. Thirdly, ASPs only response to the changes in the angle when it is orthogonal to the gratings. Hence, gratings with different orientations, such as horizontal and vertical, to capture the full angle information. These three limitations increase number of pixels required, thus increasing the total active pixel area and decreasing the spatial density. Another important drawback of ASPs is their wavelength sensitivity. The effect of wavelength is observed strongly on the Talbot depth as shown in Equation 2.1. Since double-grating architectures require the secondary grating layer to be at a certain multiple of the Talbot depth, they can only be optimized for a unique wavelength and its neighbouring wavelengths. Other limitations of ASP stem from the use of opaque metal layer as the grating choice. Due to reflections off the metal surface, angular sensitivity is reduced. It also results in reduced quantum efficiency, due to metal gratings blocking the great portion of the incident light. These last two limitations are addressed and mitigated by the following architecture.

2.1.2. Phase Gratings

Enhanced ASPs replace the top grating layer of ASPs with phase gratings to create an angle-sensitive structure with improved angular sensitivity and quantum efficiency (QE) [14]. Since phase gratings are implemented using the transparent dielectric material, the blockage of the light intensity is minimized and hence, QE is increased. Phase gratings have been shown to create intensity patterns similar to Talbot self-images at $1/4z_T$ and $3/4z_T$ for gratings with a phase step of $\pi/2$ and duty cycle of 50% [14], [15]. Hence, enhanced ASPs make use of the same optical phenomena as ASPs only without the drawback of light-blocking metal gratings. Similar to amplitude gratings, two approaches can be

used to measure the shifts in the intensity pattern. Figure 2.4.a illustrates phase gratings combined with metal analyser grating layer. This structure needs a grating pattern with various phase offsets in order to accurately extract incident angle. Second approach in Figure 2.4.b further increases quantum efficiency and pixel density by replacing metal gratings with interleaved diodes. However, interleaved diode method is not preferred in this work due to afore-explained difficulties related to its fabrication and performance.

Presented ASP structures and corresponding relative quantum efficiencies are compared in Table 2.1. Each additional metal line contributes to the decreasing quantum efficiency, resulting in the double-grating structure having the lowest quantum efficiency. Hence, it is not fit for applications in areas where the incident light can be dim.

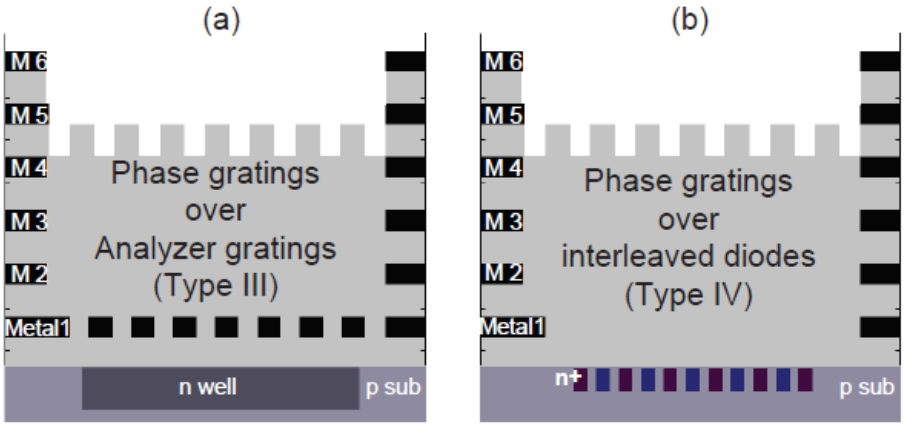


Figure 2.4: Different implementations of enhanced ASPs [14]

Table 2.1: ASP types in the literature, adapted from [14] *pn junction photodiode, ** 1: highest QE

ASP Type	Top grating	Bottom grating	Photodiode type	of pixel phases	QE ranking** (relative)
I	Amplitude	Amplitude	Single diode*	4	4
II	Amplitude	-	Interleaved diode	1	3
III	Phase	Amplitude	Single diode	4	2
IV	Phase	-	Interleaved diode	1	1

2.2. Odd-symmetry Spiral Phase Gratings

Although sharing the same name part with the *phase gratings*, odd-symmetry phase gratings don't rely on the Talbot effect as its operating principle, but rather relies on the destructive interference of light. In Figure 2.5 cross section of such a structure is shown. Parameters w_0, w_1 and w_2 show the width of phase structures on the device surface. The surface is designed anti-symmetrically around the point P in order to introduce a phase difference of π in the thicker regions compared to thinner ones. Along the plane of point P, these out-of-phase waves cancel each other thus creating a so-called 'curtain'. These repeating pattern of curtains shift laterally with the changes in the incident angle similar to the occurrence of off-axis Talbot effect [16]. Hence the variations of the incident angle can be detected by photosensitive structure underneath.

One of the most important advantages introduced by odd-symmetry gratings is that they show almost no dependence on the wavelength of the incident light. This is a very desirable property in the presence of a broadband light source. The structure is also depth-robust, dark curtain doesn't only appear at a certain depth but rather around the complete plane of X, indicated by red dashed line in Figure 2.5 [17]. However, design and fabrication complexity of this architecture presents serious drawbacks in its implementation due to the spiral structure of the final sensor and use of silicate gratings.

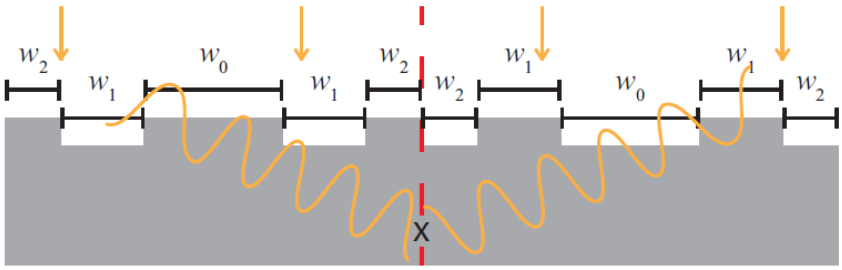


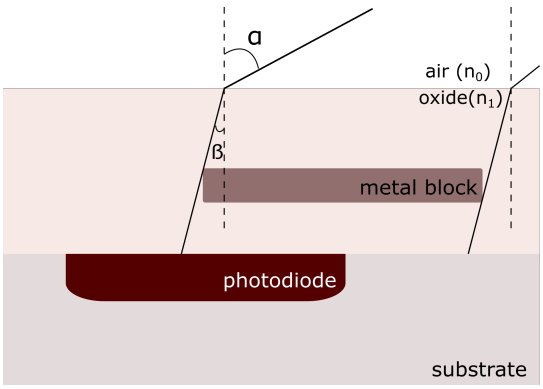
Figure 2.5: Cross-sectional image of an odd-symmetry phase grating [16]

2.3. Metal Shading Pixel

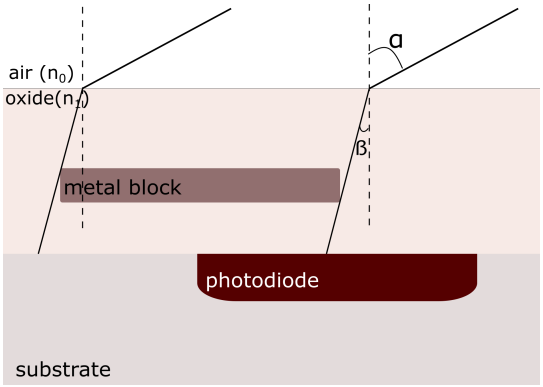
This pixel type makes use of the basic principle of metal shading, a technique also employed in sun-pointing sensors for sun position tracking applications [1]. However, different from the commonly employed sun sensors, metal shading pixels reviewed here are integrated on a single chip using standard CMOS fabrication process [18], [19]. Shown in the Figure 2.6, the structure comprises of a metal block that partially blocks the illuminations on the left and right photodiodes. As incident light angle α changes, the illuminated areas on each photodiode change correspondingly. This difference in illumination creates a difference in photodiode responses as well. Since the response is linearly dependent on the illumination strength, incident angle can be extracted using the difference between photodiode responses.

Metal shading pixel differentiates itself from other architectures with its straightforward design, linear angular response and independence from the wavelength of the incident light. However, it falls short in terms of angle resolution, hence, it is better suitable for coarse angle detection applications. Metal shading pixels are limited in their angular response due to several structural and process non-idealities. Firstly, mismatch between left- and right-photodiodes can create an error in the angle detection. This can be mitigated by the use of sufficiently large photodiodes so that the effecr of the mismatch is small enough neglect [18]. Secondly, refraction at air/dielectric border causes non-linearity in the angle response due to Snell's Law (Eqn. 2.5). Thirdly, light reflects from the metal surface inside the dielectric which causes cross-talk between the photodiodes and distorts the angle information.

$$sin\beta * n_1 = sin\alpha * n_0 \tag{2.5}$$



(a) Photodiode on the left side of the metal shading block, i.e. left photodiode



(b) Photodiode on the right side of the metal shading block, i.e. right photodiode

Figure 2.6: Cross-sectional view of left and right photodiodes in a metal shading structure

2.4. Hybrid Methods

While ASP structure focuses on combining different pixel types *(pixels with different angular response but all rely on the same angle detection method)* to increase spatial resolution [20], hybrid architectures combine two or more different angle detection methods to create a superior angular response whether it is in its angle range, angular sensitivity, spacial density or ability to localize multiple light sources.

2.4.1. Track-and-tune Architecture

Track-and-tune architecture consists of two previously mentioned angle detection principles: amplitude gratings and metal shading. It is designed based on the idea that the angle detected by linear coarse angle detection technique of metal shading can be further improved by the non-linear but fine angle detection of ASPs [11]. The proposed architecture by Varghese et al. uses Quadrature Pixel Cluster (QPD) as the metal shading structure, as shown in Figure 2.7. Although it has a different geometry than the previous designs of Koch et al., its principle of angle detection is the same, namely metal shading. Hence, it also shows similar angular properties and same equations apply to both designs. QPC has a large metal block stacked within the dielectric covers equal amount of areas over each photodiode. Including four photodiodes, highlighted as pixels A, B, C and D in Figure 2.7, allow angle detection in both vertical and horizontal orientations as opposed to simple design of left- and right diodes that can only identify angle variations in single orientation.

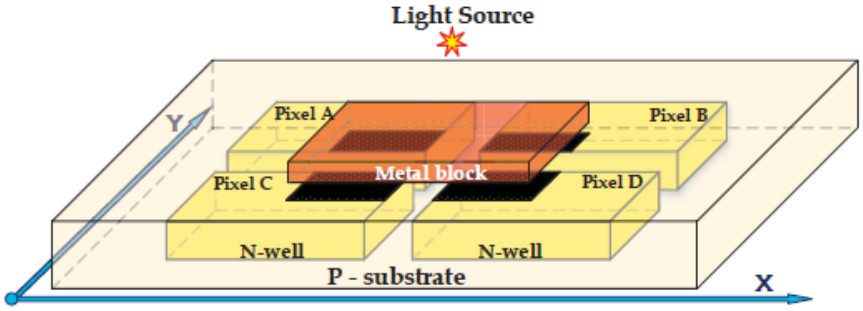


Figure 2.7: Quadrature Pixel Cluster [11]

2.4.2. Polarization-based Pixels

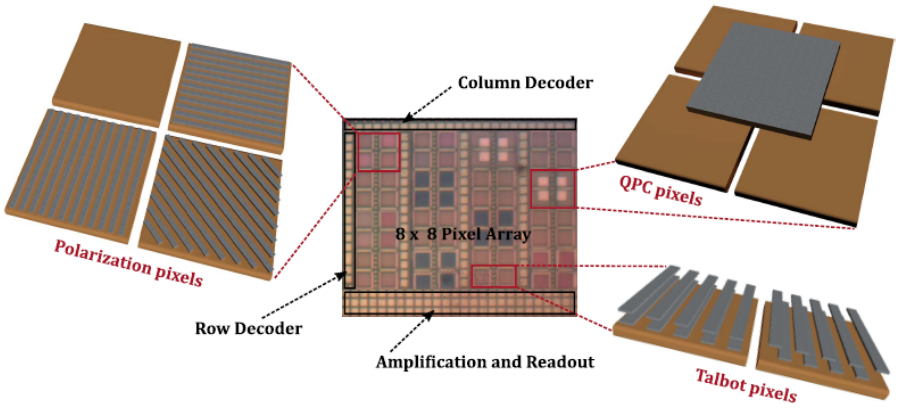


Figure 2.8: Hybrid sensor design combining amplitude grating, metal shading and polarization methods [20]

Polarization imaging can be realized by placing polarization gratings on top of a photosensitive pixel area. If a randomly polarized light hits these gratings, all components of the electric field that are in the same direction of the gratings are blocked while the other components that are orthogonal are

allowed to pass through [21]. Polarizer gratings have similar structure to diffraction gratings and are characterized by their grating pitch as well as their width. For a grid polarizer grating to show good polarization properties, its grating pitch must be smaller than the half of the wavelength of the incident light ($d < \lambda/2$) [22]. In the visible light spectrum, this limits the choice of the pitch between 200 nm and 350 nm.

Polarization pixels are very sensitive to small angle variations, hence they can act as local angle detectors alongside QPC which only detects coarse angles. However, polarization pixels cannot differentiate between positive and negative angles meaning that their response is symmetric around 0°. Example of a polarization pixel with three different grating orientations is given in Figure 2.8. For an unpolarized incident light, any of these grating orientations can detect the angle of the light. However, if the incident light is polarized in an unknown way, minimum two orthogonally-placed gratings are required to identify the polarization of the electric field of the incident wave [20].

2.5. Conclusion

Six different lensless CMOS angle-sensitive pixel architectures were introduced in this chapter that were found insightful for the research question formulated in Chapter 1. They all employ different principles and techniques to achieve angular sensitivity without depending on optical augmentation, hence each brings its own unique advantages and disadvantages to the angle detection. These six architectures are summarized in Table 2.2 together with the properties that were considered to be the most influential on their adoption as the base point in this work.

Table 2.2: Summary of the above-presented pixel architectures. *in EKL

Pixel type	Angular sensitivity	λ dependence	Complexity	Manufacturability*
ASP	Good	Yes	Medium	Yes
Enhanced ASP	Good	Yes	Medium	Yes
Odd-sym. phase grating	Very good	No	High	Yes
Metal shading	Medium	No	Low	Yes
Track-and-tune	Good	Yes/No	Medium	Yes
Polarization pixel	Good	No	Medium	No

First criteria to evaluate the presented pixels is angular sensitivity. Many of the works included here focus mainly on 3D image reconstruction and don't report any detectable angle range or angle accuracy. Hence, it makes it difficult to numerically compare the performances of pixel architectures. However, comparison can be made based on angular sensitivities. Metal shading architecture offers low angular sensitivity, meanwhile ASP and enhanced ASPs have higher angular sensitivities. Furthermore, their angular sensitivities can be adjusted according to the design requirements since it depends solely on the geometry of the pixel. Angular sensitivity of odd-symmetry gratings are reported to be improved over the ASPs, hence it is the architecture with the highest angular sensitivity.

Second evaluation criteria is the wavelength-dependence. The architectures using Talbot self-images are inherently dependent on the wavelength, since the depth these images form is directly dependent on the wavelength of the incident light. This property also makes them vulnerable to fabrication errors, since variations in the position or the thickness of the layers can alter the photodiode response. On the other hand, odd-symmetry phase gratings, metal shading pixels, and polarization pixels' responses are not dependent on the wavelength. For the track-and-tune architecture, the use of ASPs for fine angle tuning leaves it dependent on the wavelength.

Third evaluation criteria is the design complexity. Metal shading method, especially quadrature pixel cluster offers the simplest design architecture. On the other end of the complexity spectrum lies odd-symmetry phase gratings due to its elaborate surface profile and spiral shape of the imaging pixels.

Lastly, evaluation is performed based on the manufacturability of each architecture in EKL. All, except polarization pixels, can be fabricated using BiCMOS process in EKL. This is due to the small grating

pitch of polarization pixels. Since required grating pitch ranges around 200-350 nm and falls below the smallest printable feature size of the available lithography technology, it is not possible to fabricate polarization pixels that operate in the visible light range.

ASP and enhanced ASP are concluded to make great candidates as an angle-sensitive pixel for light source tracking. Although odd-symmetry phase gratings have high angular sensitivity, they are found more suitable for imaging applications and not necessary for angle detection. ASPs can be designed to perform with different angular sensitivities combined on a single chip, which significantly improves the robustness of the angle detection method. Although wavelength dependency of ASPs might initially seem as an undesirable characteristic to have in multi-wavelength applications such as solar tracking, it is open to be used as an advantage to eliminate the effect of Earth's albedo, i.e. Earth's reflection of solar radiation. Angle-sensitive pixels, despite their excellent angular sensitivities fall short in identifying the whole angle range due to their periodic angle response. In order to compensate this, metal shading structure is integrated to the pixel design to aid the ASPs with the angle detection.

3

Simulations

In the previous chapter, state-of-the-art imaging architectures in the literature were presented and evaluated based on various criteria. Based on this evaluation, three angle sensitive architectures were identified to be the best fitting structures for this work. This chapter will delve into the characterization of these identified structures. Due to the lack of a well-rounded mathematical model that describes angle sensitive pixels, simulation results and empirical results presented in Chapter 2 will be the main source of characterizing the ASPs. For this purpose, each structure is modelled and simulations are carried out using cross-platform finite element analysis software COMSOL Multiphysics. Results of these physics-based simulations are processed in MATLAB to produce the angular response of ASPs using an angle detection script written for this work.

Firstly Section 3.1 will expand on the concept of Talbot effect and angle-sensitive pixels using COMSOL simulations. This section will also explain the angle detection method used in this work. In Section 3.2 each design parameter will be identified and its effect on the angular sensitivity will be examined through simulations. Following the characterization of ASPs, metal shading structure will be studied in Section 3.3. Finally, the findings of section 3.2 and 3.3 will be summarized in the conclusion.

3.1. Angle sensitive pixels and Talbot effect

As explained in Chapter 2, Talbot effect forms the foundation of the angle sensitive pixels. Thus, understanding the self-image formation and the factors influencing this optical effect play a key role in characterizing and design of the pixels. Talbot effect can be observed in both amplitude and phase gratings. Self-image formation in phase gratings is included in appendix Figure C.2. Figure 3.1 shows the illumination of amplitude gratings and the resulting Talbot self-images at multiple depths. It can be observed from this figure that self-images occur at depths of $m/2 * Z_T$ where m is an integer number and that the strongest self-image occurs at half-Talbot length, $1/2 * Z_T$. Theoretically, analyser grating can be placed at any of these depths where self-images are formed. However, it is a common practice in the literature to place them at half-Talbot depths where the self-image is phase-shifted. In a CMOS-based processing it is required that the self-images are formed within microns of the diffraction gratings [9]. This restricts our design choices for grating pitch and light wavelength. (See Equation 2.1) In order to have the Talbot depth closest to the diffraction grating surface, we can follow these two design directions:

1. Increasing the wavelength of incident light
2. Decreasing the grating pitch

However, decreasing the grating pitch influences the angular sensitivity of ASPs as well. Hence, it cannot be decided only based on the Talbot depth requirement. This will be elaborated in Section 2.2.1. In the following sections and simulations as well as the pixel design, wavelength will be taken as 632 nm. This wavelength, corresponding to red color is chosen due to its being at the end of the visible spectrum, hence the highest wavelength in the visible spectrum, and the ease of access to red LEDs later for the test setup. The choice of 632 nm as the wavelength will be explained more in the design of ASPs in Section 3.2.8. Effect of the wavelength on Talbot depth is illustrated in appendix Figure C.1.

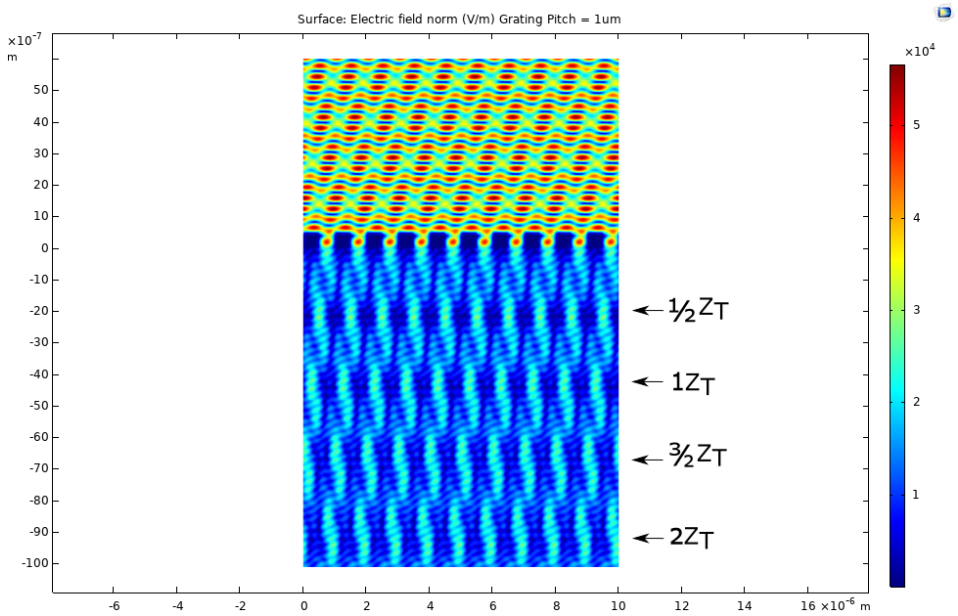


Figure 3.1: Talbot self images created by amplitude gratings. Metal gratings are shown in dark blue at y = 0. Grating pitch = 1 μm, Incident angle = 10°, λ = 625 nm

3.2. Characterization and design of angle sensitive pixels

Before modelling and simulation of the angle-sensitive pixels with COMSOL, it is important to understand the main design parameters that have an effect on the subsequent angle detection. First of all, the pixel geometry is the main determinant of angular sensitivity. Below in Figure 3.2 cross-section of each ASP with different grating offsets is shown and important physical parameters, grating pitch and Talbot depth, are highlighted. In the following subsections, each geometrical and physical design parameter will be discussed. Their effect on the resulting angle curve will be investigated mainly in four categories; angular period/angular sensitivity, angular response range, distortion and angular offset.

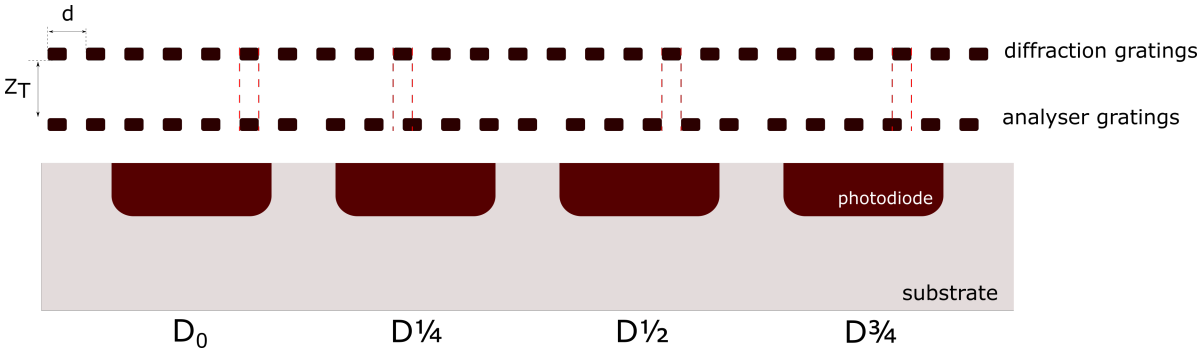


Figure 3.2: Cross-section of four pixels with different offsets. From left to right: 0, $\pi/2$, π, $3\pi/2$ offset. Offset between top and bottom gratings are illustrated with red dotted lines.

3.2.1. Grating metal

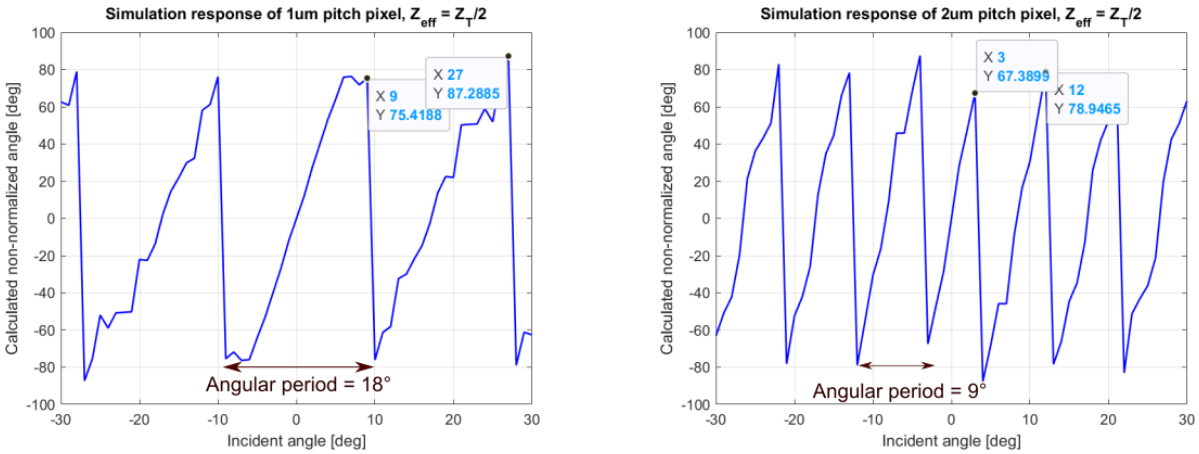
Chapter 2 discussed the implementation of grating stack in various designs in the literature. These designs are fabricated using modern CMOS processing and grating layers are built in the interconnect lines. This directly necessitates the use of same metal for both interconnect and grating layers. Considering that 130 nm or 180 nm processes were employed for the fabrication and the primary interconnect metal used at these technology nodes is copper, copper can be the metal choice for these designs. However, there are two main issues related to copper that constrains its use in this work. Firstly, its reflectivity increases sharply with the light wavelength after 550 nm. Reflected beams interfere with the diffraction pattern causing a noisy pixel output. Hence, it is suitable for applications with green light (as in the literature), but not for this design that is optimized for the use of red light. Second problem is that copper is considered a contaminating metal in EKL.

As it can be inferred from the above stated issues with copper, metal type influences the angle response mainly through metals' reflective properties. Low reflectivity metals are preferred to high reflectivity metals (such as aluminium, gold and silver) since they produce smoother pixel responses which in turn leads to higher angle accuracy. TiN, with its below 10% reflectivity at 632 nm and its common use at EKL, is most fitted as the grating metal.

3.2.2. Grating pitch

Effect of the grating pitch on the depth and periodicity of the Talbot self-images were presented in Chapter 2. This section will investigate the effects of grating pitch on the combined angular response of four ASPs shown in Figure 3.2. Grating pitch, also referred to as grating period, corresponds to the distance between mid-points of two metal gratings and can be expressed as the sum of metal width and gap width.

In Figure 3.3 angular response of two pixels with different grating pitches are given. In both pixels, analyser gratings are placed at the first order Talbot depth, $Z_{eff} = 1/2 * Z_T$ and all other design parameters are kept constant and equal. This comparison shows that grating pitch and angular periodicity are inversely related to each other. Higher angular period, as in Figure 3.3.a helps identifying more angles in one period, however the price is the diminished angular sensitivity. For each one degree increase in the angle, output of 2 μm pitch pixel changes twice as much the 1 μm one. Thus, it can be concluded that higher grating pitch results in a higher angular frequency (shorter angular period) and higher angular sensitivity.

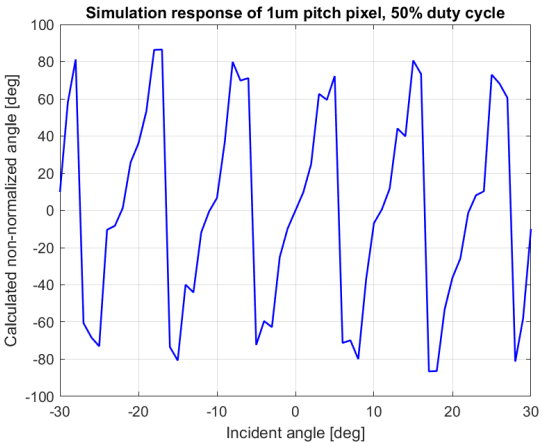


(a) Angular response of 1 μm pitch gratings with period of 18°

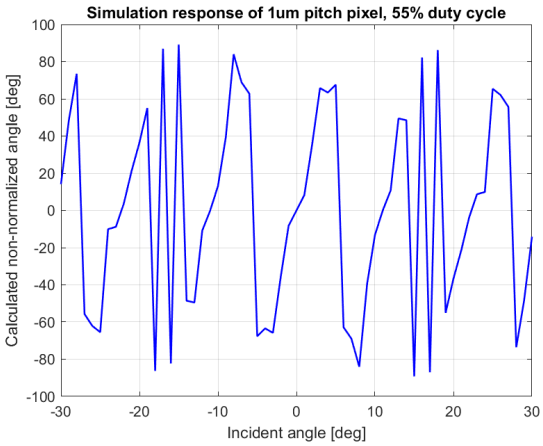
(b) Angular response of 2 μm pitch gratings with period of 9°

Figure 3.3: Comparison of angular periodicity generated by different grating pitches

3.2.3. Duty cycle



(a) Angular response of 1 μm pitch gratings with 50% duty cycle



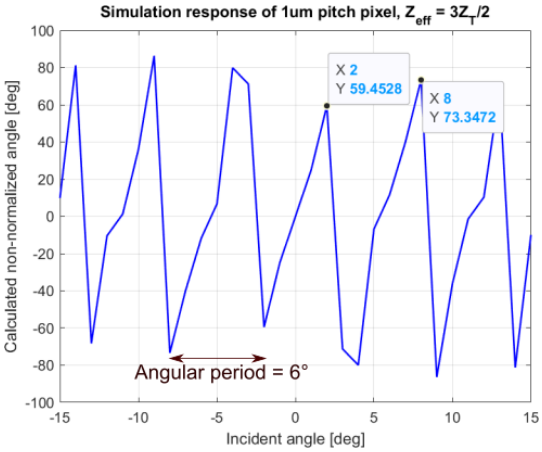
(b) Angular response of 1 μm pitch gratings with 55% duty cycle

Figure 3.4: Figure showing the change in the angular response with duty cycle deviation

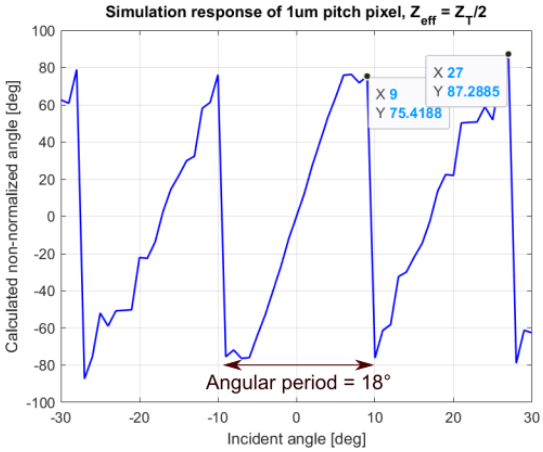
Duty cycle of the gratings is defined as the ratio of the grating width to the grating pitch. Deviations from 50% duty cycle can distort the angular response and make some angles almost impossible to differentiate. Figure 3.4 illustrates these distortions by comparing the response of 55% duty cycle ASPs with the ideal 50% duty cycle. The main goal here is to examine the robustness of the angular response to the duty cycle variation and eventually to determine the maximum deviation that can be tolerated without disrupting angle detection. The simulation results show that in order to differentiate the angles within -30°to +30°range, duty cycle deviation must be kept within 5% for 1 μm pitch gratings. This tolerance tends to be higher for 2 μm pitch gratings.

3.2.4. Intergrating distance

The effect of intergrating distance on the angular response manifests itself in two ways. The first one depends on which Talbot depth the analyser gratings are located at. This depth, called Z_{eff}, directly influences the periodicity of the resulting angle plot. Responses of two different ASPs with analyser gratings located at 3/2 Talbot depth and 1/2 Talbot depth are shown in Figure 3.5. Period of the angular response triples as the effective Talbot depth is reduced by three times. Another way that intergrating spacing effects the angular response is through the fluctuations from the exact Talbot depth. These small deviations in the location of analyser gratings with respect to the diffraction gratings introduces non-linearity on the angle lines at each angular period. Range of the response(range between the maximum and minimum non-normalized angle response) starts to shrink for many periods. It also affects the period of the response in a similar way the Talbot depth choice does. However, for small deviations this effect of the angular period is not very pronounced.



(a) Angular response of 1 μm pitch gratings with analyser gratings at 3/2 Talbot depth



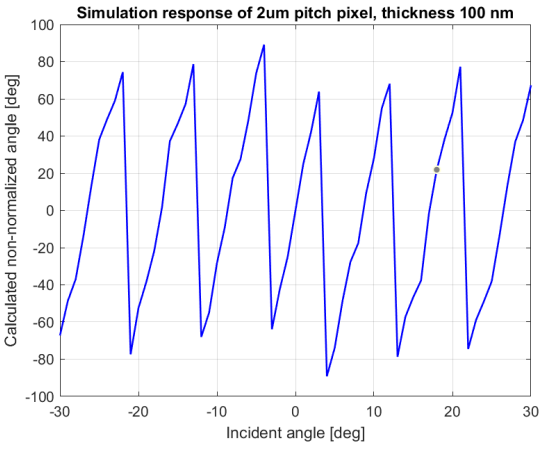
(b) Angular response of 1 μm pitch gratings with analyser gratings at 1/2 Talbot depth

Figure 3.5: Figure showing the change in the period with different Talbot depths

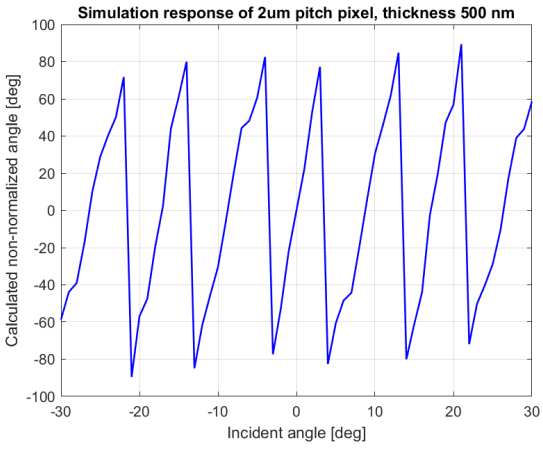
3.2.5. Grating thickness

Grating thickness is one of the most vaguely defined design parameters in the literature. This can be partly due to their use of unmodified CMOS processes where the grating stack is built as a part of interconnect layers. Hence, the grating thicknesses are pre-determined by the thickness of the interconnect layer used. However, with BiCMOS fabrication process in EKL there is more freedom to choose a grating thickness independent from the rest of the layers.

Simulations are carried out to find the relation between the grating thickness and angular response. Figure 3.6 shows the response of 2 μm pitch gratings implemented with 100 nm and 500 nm thick metal lines. Responses don't differ in their angular period whatsoever. Two important changes that follow the thinning of the gratings are the decrease in linearity of each angle period and non-uniformity in the range of the angular responses. These effects, especially non-linearity of the angle curves reduces the accuracy of the angle detection.



(a) Angular response of 2 μm pitch gratings with 10 nm thickness



(b) Angular response of 2 μm pitch gratings with 500 nm thickness

Figure 3.6: Comparison of angular responses for ASPs with different grating thicknesses

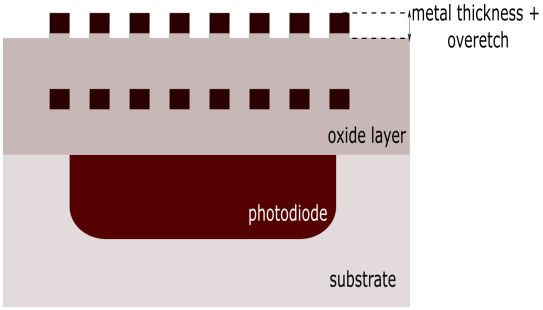
3.2.6. Grating depth

Grating depth, also referred as phase step, is a parameter that defines the step height of the phase gratings. Phase gratings with phase step of $\pi/2$ and duty cycle of 50% have been previously studied in the literature and are known to generate Talbot-like intensity patterns at $1/4Z_T$ and $3/4Z_T$ [23]. Simulation data shows that similar optical effect can also be observed for all odd multiples of $\pi/2$. The difference occurs when the phase shift is $3\pi/2$ instead of $\pi/2$. This causes pixel behaviours to get swapped between the pixels with 0 and 180°offset, and the pixels with 90 and 270°offset. However this change isn't reflected to the angular response due to the division in the final calculation. Optical path difference required to create $\pi/2$ phase shift (ϕ) can be calculated using Equation 3.1 for each wavelength.

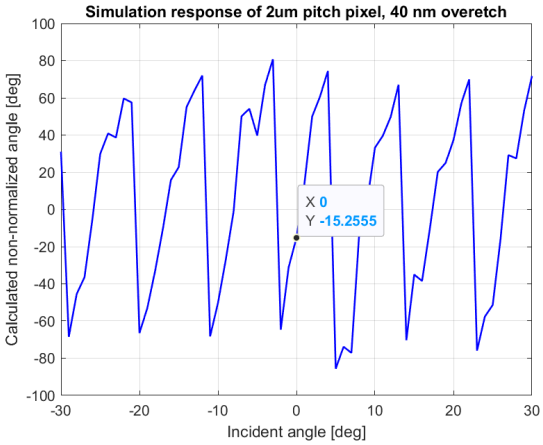
$$\phi = 2\pi \frac{OPD}{\lambda} \tag{3.1}$$

3.2.7. Overetch

Overetch happens during the fabrication process as a result of plasma etching where the excited ions hit the surface to remove the unmasked regions off the wafer. These collisions also remove a part of the underlying layer depending on the etching time. Although overetch is not a design parameter its effect on the ASP response will be discussed here as a precursor to the fabrication process. Overetch has a different impact on amplitude and phase gratings. Figure 3.7.a shows a cross-sectional view of an amplitude grating stack with 40 nm of overetched oxide layer. This overetched thickness translates to a shift in the angle response as well as distortions on the signal. This is also shown in Figure 3.7.b where the curve shifts 1°to the right. Effect of overetch on the phase gratings, on the other hand, creates an increase in the grating depth. This deviation than the design value has similar influence on the angular response as duty cycle variations. It distorts the angular response and makes the angle detection almost impossible for the effected periods.



(a) Overetched amplitude grating sideview



(b) Simulation response of amplitude gratings with 40 nm overetch

Figure 3.7: Simulations showing the functioning of metal shading block for two different incident angles

3.2.8. Summary & Final ASP Design

The sections until this point have studied how design and fabrication parameters influence the angular response of ASPs. Based on this analysis, each design parameter will be determined in this section.

The choice of grating pitch is defined by two factors; wavelength and Talbot depth. Its lower end is limited by the CD of the lithography system, which is 0.5 μm for the ASML PAS5500/80B stepper in

EKL.Hence, the minimum linewidth is 0.5 μm and the minimum pitch that can be printed is 1 μm. Its higher end, on the other hand, is limited by the thickness of intergrating dielectric. Although this is not a technical limit and thick dielectric layers can be well achieved by deposition, it is chosen to be restricted within 10 μm due to increasing non-uniformity in the thick layers. To allow the fabrication of higher grating pitches with less than 10 μm intergrating distance, wavelength is chosen to be the highest visible wavelength, that is red light. Thus, grating pitch of the designed ASPs should lie within 1-2 μm range. Gratings also have duty cycle of 50%, i.e. with equal lines and gaps.

The highest intergrating dielectric thickness is limited to 10 μm by design choice as mentioned. This allows only the first half-Talbot depth to be used as the effective depth for grating pitches greater than 1.1 μm. With 1 and 1.1 μm gratings, third half-Talbot depth also falls within the 10 μm limitation, hence can be chosen as the effective Talbot depth. This increases the angular sensitivity(β) of the pixel response (see Equation 2.4) and pixel variations in the designed pixel array.

In the previous sections, the effect of the grating thickness on the angular response was observed to be minimal. This leaves freedom for the choice of this parameter that would be the most ideal for the fabrication process. In order to minimize the steps height created by the bottom gratings, thickness of this layer is reduced to 100 nm, yet not below 100 nm due to transparency of the thin metal layers. Whereas the top grating layer is chosen as 500 nm, much thicker than the bottom layer, for better step height coverage. For similar reason, grating depth is set to be 750 nm. Although $\pi/2$ phase step (107 nm) produces a more accurate angular response, phase step accuracy, thus angular accuracy, cannot be achieved during the fabrication process without a planarization step, i.e smoothing out the surface topography.

Final pixel types and corresponding design parameters are presented in Table 3.1. Different angular sensitivities can be implemented on one design to increase the range of the individually detectable angles and increase the performance of the pixel array in the presence of multiple light sources. Chapter 3 will discuss the layout design of each pixel as well as their distribution on the 8x8 pixel array.

Table 3.1: Design parameters of ASPs

Pixel type	Grating pitch	Intergrating distance	Angular period	Angular sensitivity
Amplitude	2 μm	$1/2 * Z_T$ (9.5 μm)	9°	20
	1.5 μm	$1/2 * Z_T$ (5.34 μm)	12°	15
	1 μm	$1/2 * Z_T$ (2.37 μm)	18°	10
	1 μm	$3/2 * Z_T$ (7.1 μm)	6°	30
Phase	2 μm	$1/4 * Z_T$ (4.75 μm)	18°	10

3.3. Characterization and design of metal shading structure

As proposed in Chapter 2, metal shading structure is integrated to the design to assist the periodic ASP response with wide-range angle detection. This section will elaborate on the concept of metal shading using a mathematical approach. Once the working principle and angle detection method are explained, final design and its dimensions will be presented.

3.3.1. Metal shading method and angle detection

Cross-sectional geometry of a simple metal shading structure is given in Figure 3.8. An opaque metal block is placed inside a transparent dielectic material and covers half of each photodiode width. Separation between the substrate and metal block is represented with parameter T_{OX}, metal thickness with T_M, photodiode width with W_D and separation between two photodiodes with T_{sep}. Also optical path of incident light with angle of α is illustrated on the same figure. Separation of photodiodes is a good design practice to minimize the cross-talk between the photodiodes via reflecting beams. Depending on the incident angle, certain photodiode areas are illuminated and some are left in darkness as a result

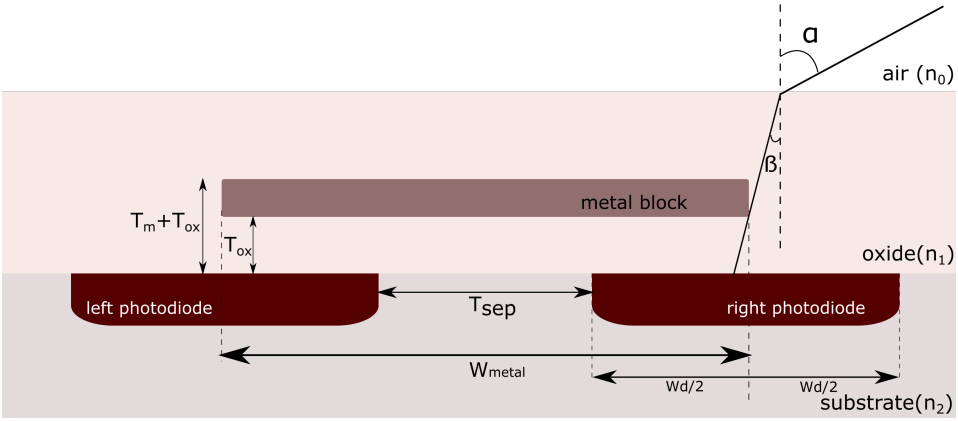
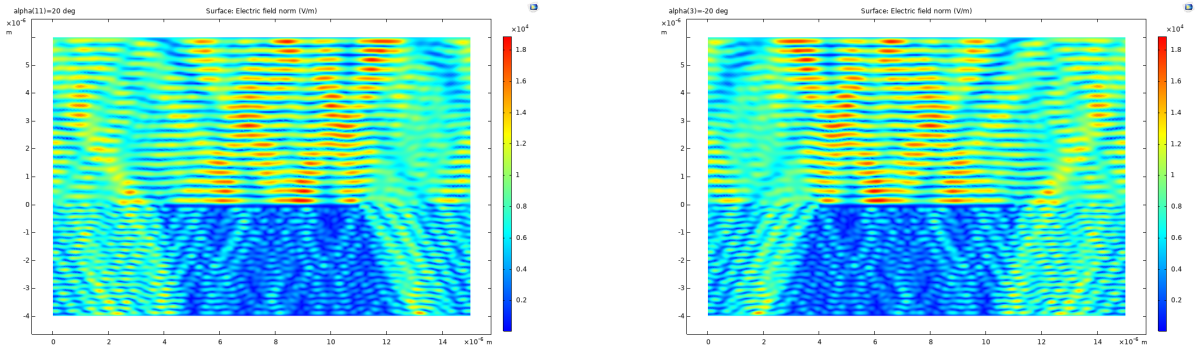


Figure 3.8: Cross-section showing metal shading block with left and right photodiodes. Adapted from [19]

of metal blocking the light. This principle of metal shading is visualized in Figure 3.9 using COMSOL Multiphysics. The illuminated and shaded parts can be observed for 20°and -20°.



(a) Metal shading illuminated by 20°angle

(b) Metal shading illuminated by -20°angle

Figure 3.9: Simulations showing the functioning of metal shading block for two different incident angles

Each photodiode generates a photocurrent whose value is proportional to the irradiance on the diode surface. When the incident angle is positive (as shown in Figure 3.8), larger surface area of right photodiode is illuminated, hence, producing larger current. Likewise when the incident angle is negative, larger surface area of left photodiode is illuminated. Currents generated by the each photodiode can be expressed by a multiplication of illuminated diode area by a current coefficient, shown in Equation 3.2, where I_L and I_R stand for the left and right photodiode current, respectively.

$$\begin{aligned} I_L &= I_0 * [W_{d/2} - tan\beta * (T_M + T_{OX})] \\ I_R &= I_0 * [W_{d/2} + tan\beta * T_{OX}] \end{aligned} \tag{3.2}$$

The difference of the currents result in a value that is proportional with the tangent of the reflected angle β. For coarse angle detection $tan\beta$ can be approximated to β, resulting in the following relation:

$$\begin{aligned} I &= I_R - I_L \\ &= I_0 * [tan\beta * (2T_{OX} + T_M)] \\ &= K * \beta, \quad \text{where} K = I_0 * (2T_{OX} + T_M) \end{aligned} \tag{3.3}$$

The incident angle of the light can be calculated using Snell's Law (Equation 3.4):

$$sin\beta * n_1 = sin\alpha * n_0$$
$$\alpha = arcsin(sin\beta * \frac{n_1}{n_0}) \tag{3.4}$$

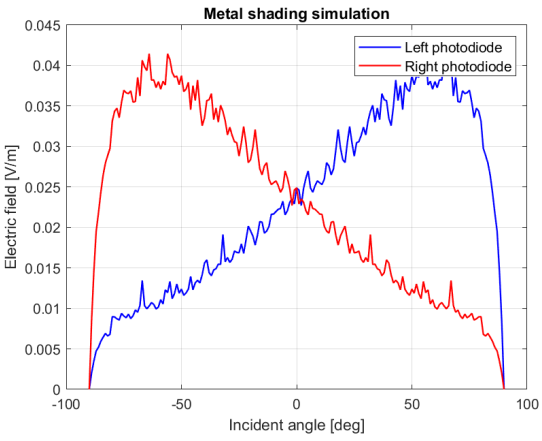
Design considerations for the metal shading structure includes metal thickness, oxide thickness, metal width, photodiode width, and separation distance between photodiodes. The first two, $T_M/quad\text{and}/quadT_{OX}$ can be chosen freely *(unless there's a minimum current requirement)*. Separation of the diodes is determined by the horizontal path followed by the beam with β_{max} to make sure the beam reflected off the metal surface doesn't fall on the other photodiode. Parameters photodiode and metal width are calculated using the optical path of the β_{max} beam while taking the fill factor into consideration.

Table 3.2: Dimensions of the final metal shading structure

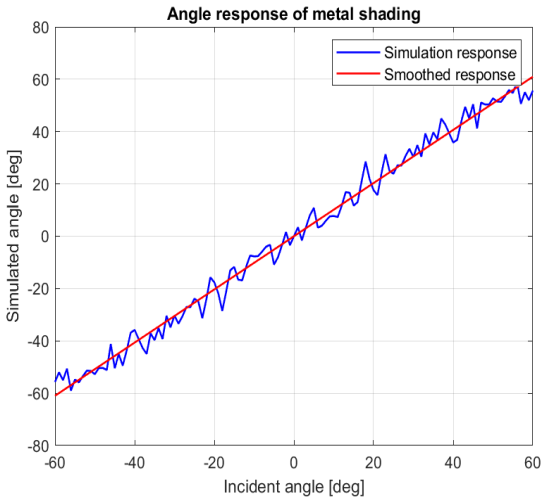
Design parameter	Value
Metal width	7 μm
Photodiode width	8 μm
Separation	6 μm
Metal thickness	0.1 μm*
Oxide thickness	3 μm

**Metal thickness is set by the bottom ASP layer. Metal shading and bottom ASP layers are merged in one optical mask during the mask generation step. Layers in the layout and optical masks are discussed in Chapter 4.*

The designed structure is verified with COMSOL simulations. The electric field on each photodiode due the changing incident angle is shown in Figure 3.10.a for the range of ±90°. Generated photodiode currents are proportional to the electric field values. The response starts to deteriorate around 60°, hence only ±60°range is taken into account for the angle calculation. Resulting angular response is presented in Figure 3.10.b, where red curve corresponds to the ideal smoothed linear curve with slope of 1. Actual response of the structure, blue curve, is noisier than the ideal response, thus limiting the angle accuracy. Average calculated angle error is 3.1°which corresponds to 20.7%.



(a) Electric field on left and right photodiodes with changing incident angle



(b) Calculated angle curve

Figure 3.10: Plots showing angle detection using metal shading

3.4. Conclusion

This chapter focused on the characterization of the proposed angle-sensitive pixel architecture as well as the accompanying metal-shading method. Each design parameters of ASP was analysed in Section 3.2 using simulation model and final design was presented. Similarly Section 3.3 discussed the metal-shading method using an analytical model. Following the analysis and design, metal shading block was verified at the end using a simulation model. Additionally, its performance is evaluated in terms of angle accuracy. Layout design of each designed pixel will be carried out in Chapter 4.

4

Read-out Electronics and Layout Design

4.1. Background on 3T active pixel read-out

Active pixel sensors are commonly used in the read-out circuit of CMOS image sensors to sense light intensity and convert it to voltage. In this work, active pixel sensors with three transistors, called 3T pixel read-out, are utilized to read signals from the pixel array. Circuit schematic of a 3T pixel read-out is shown in Figure 4.1. It is composed of three NMOS transistors, these are reset transistor M_{RST}, source follower M_{SF} and selection transistor M_{SEL}. Each read-out cell in the pixel array is resetted through RST signal before read-out cycle begins. This action turns M_{RST} transistor on and sets the voltage at node A to V_{DD}. After a while RST signal is returned back to zero and M_{RST} becomes disconnected from the rest of the circuit. In the meantime, photodiode is shown light and it starts to generate current. This generated current discharges node A and voltage starts to drop. Through M_{SF}, source follower, this voltage change at node A is also appears at node B. The last step of the read-out occurs with the row selection signal. If row signal is high, column output is read from the source of M_{SEL}; if it is low, no signal is read. Active read-out behaves as an inverting cell. This means when light intensity is high, higher photodiode current is generated and the resulting voltage drop on the photodiode is higher. This leads to lower node voltage at A, hence lower column output.

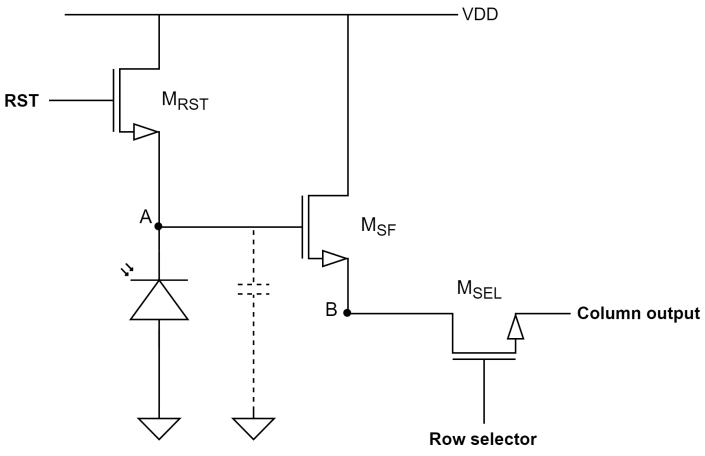


Figure 4.1: 3T active pixel read-out, adapted from [24]

4.2. Read-out Electronics

Sun position sensor design by Romijn et al. [6] constitutes the starting point of the electronics design in this work. Final measurements in Chapter 7 are also carried out using the chips with this electronics design on them. Therefore, first part is allocated to look into the work of Romijn et al. and to give an overview of its read-out circuitry.

Central block in the signal flow, as shown in Figure 4.2 is the active pixel read-out. Each pixel output is read through a different 3-transistor cell, hence this block comprises of 64 read-out cell in total for the 8x8 pixel array. Each of these read-out cells are connected to row selection signal, generated by the address generator and decoded by the row decoder, and to column output lines. Each column output on a single row goes through the analog processors simultaneously, however only the output corresponding to the currently measured pixel is passed to the output via column decoder block.

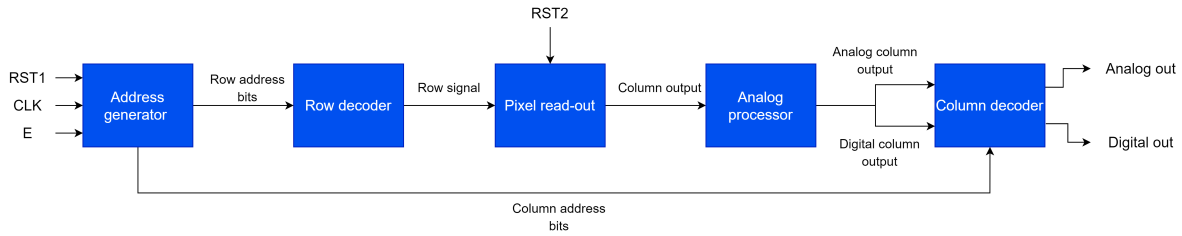


Figure 4.2: Design overview of the sun position sensor, adapted from [6]. RST1 is the counter reset, while RST2 is the pixel reset. E is the enable signal that connects or separates two reset signals.

The proposed electronics design adopts the same pixel read-out method, namely the 3T active pixel read-out. However, the electronics design is simplified through various modifications. Final block diagram of the on-chip electronics is shown in Figure 4.3. Firstly, address generator block is removed. Row address information is externally provided to the chip through 3-bit row input and each column is read from a separate output pin. This allows individual read-out of the pixels. This modification greatly simplifies the electronics design since it eliminates the need for clock signal, counter reset and enable signal that allows us to switch between counter reset and pixel reset. Analog processor is kept and each column output can be read-out either in analog or digital format. However, this design also gives direct access to the output of the active pixel read-out cells through output pins.

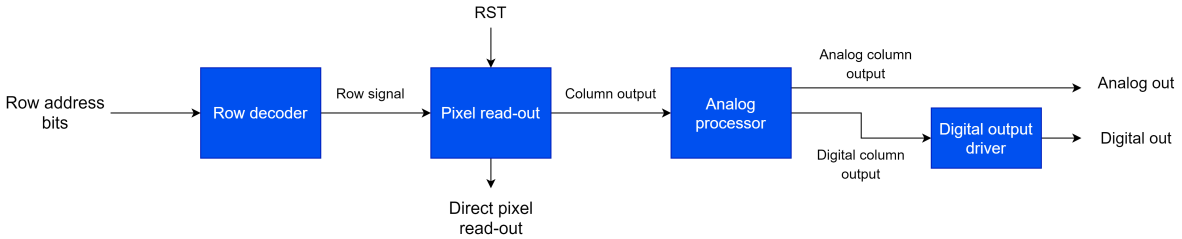


Figure 4.3: Design overview of the angle-sensitive sensor

4.3. Layout Design

As explained in the electronic design part, angle-sensitive pixel array constitutes the central part of the chip. Hence, the first step of layout is the design of individual pixel block and following pixel array. Layout design of the active pixel read-out follows the pixels array. Row decoder and signal processing unit are then integrated into the layout design. Finally, test structures are designed and placed on the chip layout.

4.3.1. Angle-Sensitive Pixel (ASP) Layout Design

8x8 pixel array consists of 64 identical pn-junction photodiodes. Dimensions of each photodiode is based on the determined current requirement for measurements. In order to estimate the photocurrent hence to design the dimensions, three parameters must be known. These are current generation per active photodiode area, quantum efficiency of the designed ASP, and responsivity of photodiode to red light.

Current generation of the photodiodes fabricated by BiCMOS process are not reported or documented, therefore the work of Romijn, et al. [6] is taken as the base point. Photodiode test structures on their fabricated chips are measured using Cascade33 Microtech measurement tool. Anode and cathode currents are noted down in Table 4.1 for dark and light measurements of two different photodiode areas. Cathode current of the illuminated photodiodes is the most important value that will be simply referred to as the photodiode current, meanwhile dark current refers to the leakage current of the pixel. As the measurements show, photodiode current is 36 $pA/\mu m^2$ for broadband light and it is linearly dependent on the active area.

Table 4.1: Photocurrent Measurements

Active area		I_A	I_C
48x48 μm^2	dark	34 pA	1.8 nA
	light	6.5 nA	85 nA
58x58 μm^2	dark	42 pA	4.7 nA
	light	1.2 nA	122 nA

Double-grating structure of ASP leads to substantial loss of light intensity before light beams hit the surface of photodiode. These losses stem mainly from the light blocking of metal gratings and the use of thick oxide layers as inter-grating dielectric. Although exact quantum efficiency of designed ASPs are not known, it is reported by Sivaramakrishnan et al. as 10% [14]. This way we can approximate that 10% of incident light energy is lost through the grating stack hence decreasing the generated current by the same amount.

Responsivity of BiCMOS photodiodes around 600 nm wavelength is reported as 0.2 A/W [25]. Total photocurrent generation of a photodiode can be calculated by the multiplication of responsivity, irradiance(W/m^2) and photodiode area.

Considering the above explained factors of photocurrent, pixel is designed as 700x700 μm^2 photodiode with 678x678 μm^2 of active area. This results in approximately 0.1 μA current generation when illuminated with red LED source with 21.9 $\mu W/mm^2$ irradiance. *(Light source utilized for the optical measurements have irradiance of 21.9 $\mu W/mm^2$.)* Layout design of a single pixel with metal gratings is given in Figure 4.4.b alongside a metalized image of a pixel of Romijn et al. shown in Figure 4.4.a. Despite being shown the same size, new pixel design is 2.6 times larger in active area to compensate for the intensity loss introduced by the grating stack. Larger pixels can help create the illusion of infinite grating by increasing the number of gratings and prevent the edge effects of finite diffraction gratings [12].

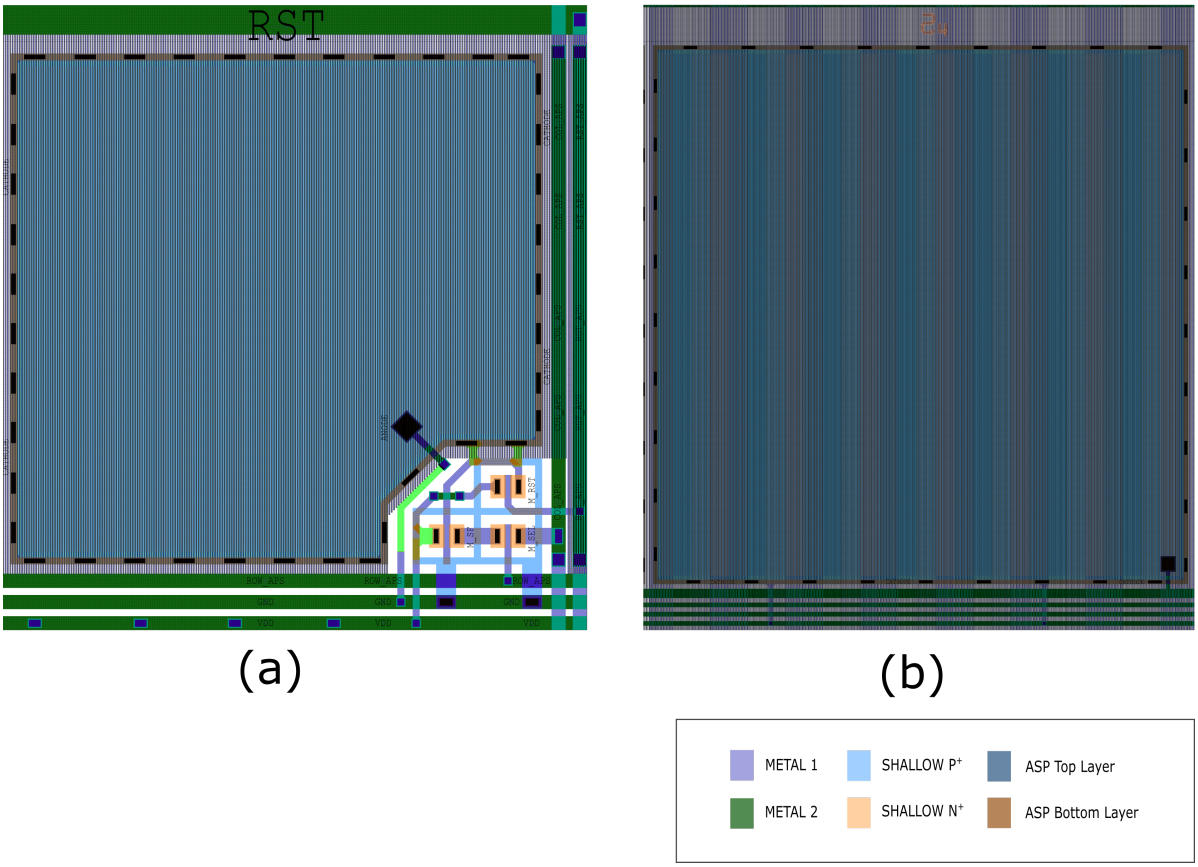


Figure 4.4: Metalized pixel designs. (a) Pixel design of Romijn et al. (b) Proposed pixel design

Another difference between the two pixels is the location of 3T read-out circuitry in the layout. This part, shown as the three transistors on the bottom right corner of Figure 4.4.a, is separated from the pixel array in the new layout design to improve the uniformity between vertical and horizontal ASP pixels. In this way, metal lines can also be extended further from the pixel active area. Extended lines block the light entering the dielectric around the edges of the pixel without being modulated by the gratings, especially for higher incident angles. However, this is not a must since its effect will be canceled out by the differential measurement of the pixels. Extension of metals is only partially possible with read-out circuitry in the pixel array since metal gratings can form stress on the transistors and influence their I-V characteristics.

Following the design of pixel array, each ASP type is distributed among the 64 pixels. Two pixel orientations, vertical and horizontal, are chosen to be able to identify both azimuth and elevation angles of the incident light. It is also known from Chapter 2 and 3 that each orientation should have four different phase offsets hence four pixels. This makes up to 8 pixels in total for each ASP type. Pixel distribution is accomplished fairly differently on pixel array of Romijn et al. and new proposed pixel array. Layouts of both designs are included in the appendix Figure D.1 and Figure D.2 with each pixel type highlighted.

Initial idea was to implement all pixel types on the same chip. However, there needs to be a separation between different pixel types. If they are too close to each other, field of view of thinner pixels *(pixels with thinner layer of inter-grating dielectric)* can be blocked by those that are thicker. It also requires multiple masks for the fabrication of single layer. This is due to the otherwise created large step height between the pixels that would result in lithography issues in terms of exposure focus. Need for multiple masks arises so that each pixel gratings can be patterned independently from individual layer thicknesses. Hence, each pixel type on the array will be implemented on a different process wafer in the following chapter regarding fabrication.

4.3.2. Active Pixel Read-out Layout

The reasons for separating the pixel read-out from pixel array were presented in the previous subsection. In this section, the layout choices for the complete read-out will be given and explained. Figure 4.5 shows the fundamental read-out block in the layout design. Comprising of eight 3T configurations for each column on a single row, the block is connected to the cathode of each pixel with Metal 1 lines shown on the right side of the figure. Depending on the row input to the block, these signal inputs are either transferred to the output of the read-out for further signal processing or they are blocked by the open selection transistor (M_{SEL}).

However, the downside of this configuration and separate placement of read-out from the pixels is extended signal route that connects the output of each diode to the read-out. This route is especially longer for the last column than the first column which can create slight changes in the measured currents.

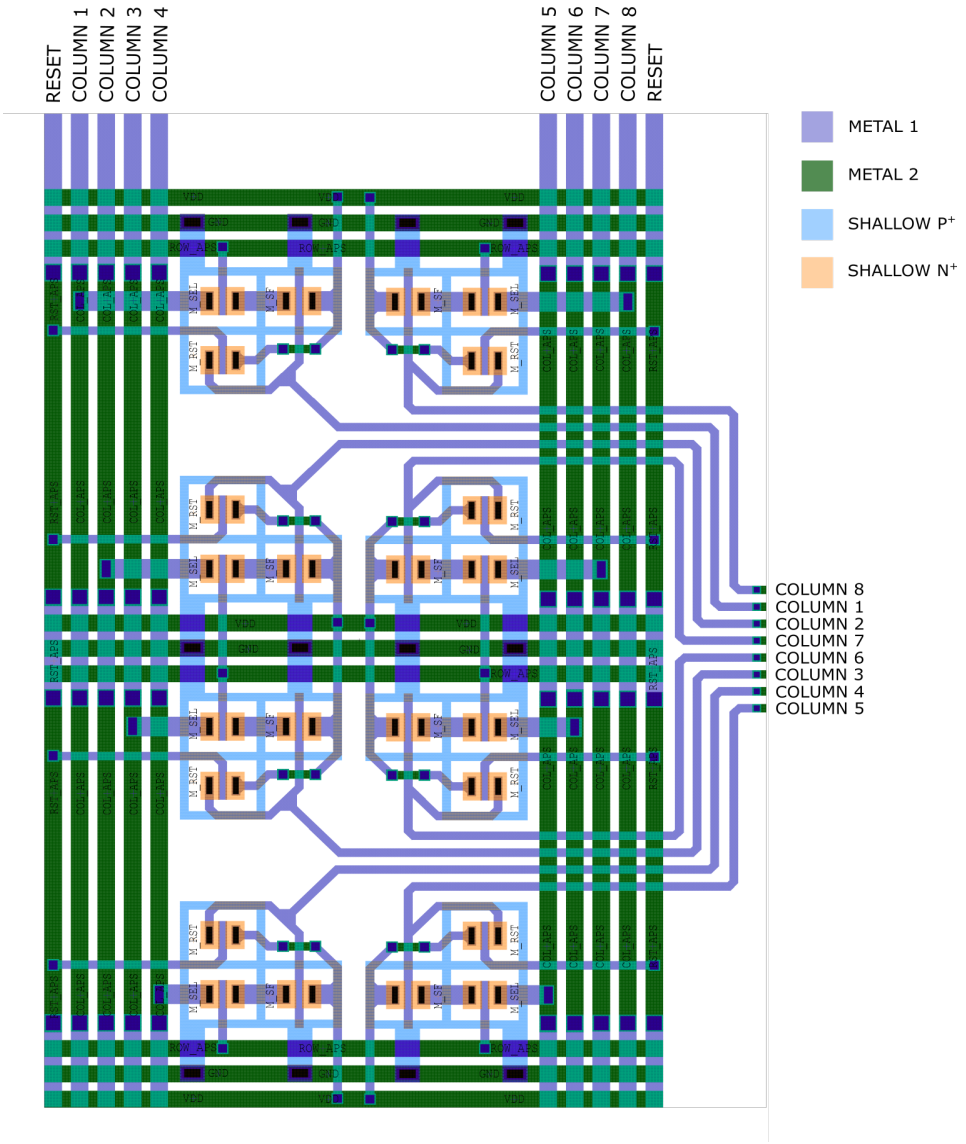


Figure 4.5: Active pixel read-out of single row

4.3.3. Metal Shading Pixel Layout

Complementary to the ASPs, layout design also includes metal shading structure. In the proposed design metal shading is implemented using the method of left-and right photodiode shading with the design parameters derived in Chapter 3 rather than the single metal block technique called QPC (quadrature pixel cluster). As metal shading pixels are to assist ASPs in angle detection, they have the same geometrical orientations as ASPs, namely vertical and horizontal. Figure 4.6 shows all four types of metal shading pixels in the design. Top two images show the implementation of vertical pixel orientation with photodiodes placed either on the right or left side of the metal line, whereas bottom two images show the implementation of horizontal pixel orientation with photodiodes placed either on the upper or down side of the metal line. All photodiodes share the same N-well area, meaning that the cathode current of the pixel corresponds to the sum of all photodiodes' cathode current. This technique both saves chip area and simplifies the read-out of photodiodes. However, its fill factor is still lower than QPC since active pixel area is decreased by the interleaved placement of anode regions.

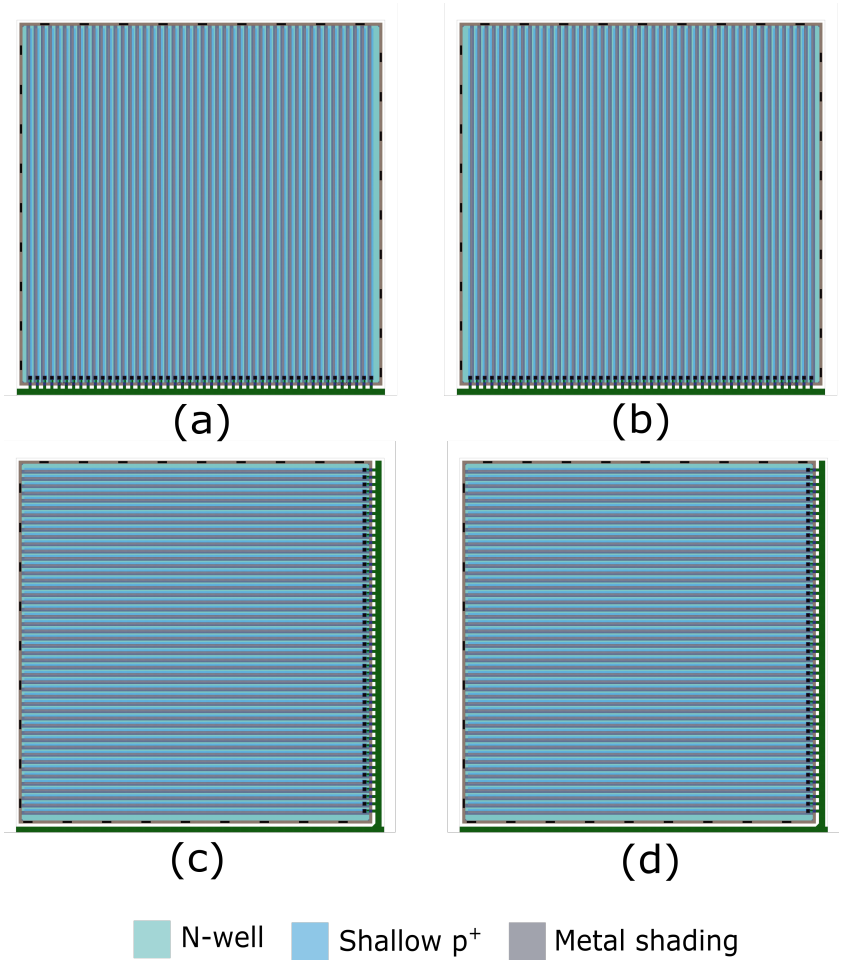


Figure 4.6: Metal shading layout.
(a) Right photodiode (b) Left photodiode (c) Up photodiode (d) Down photodiode

4.4. Photomasks

Following the completion of layout design, photomasks are generated for each layout layer. The design containing the particular pattern of each layer is transferred on a quartz photomask with chrome on it to identify the patterned areas. Photomasks are categorized into two depending on this transfer, light field and dark field masks. With a light field mask, the patterned areas remain after the etching process whereas with a dark field mask patterned areas are etched away. In this design, the layers of ion

implantation and openings are generated as dark field masks, while metal lines are defined using light field masks.

BiCMOS7 process requires use of 7 masks to realize fully-metalized CMOS design. On top of this, proposed design requires two additional layers. The first one consists of ASP bottom gratings combined with metal shading lines and the second one ASP top gratings. Grating design on top of the sun sensor design of Romijn et al. similarly needs two masks to define. Hence, in total 11 photomasks are needed to complete the fabrication of the proposed designs. They are fitted on 3 quartz masks shown in Figure 4.7 where design 1 refers to the sun position sensor while design 2 refers to this work.

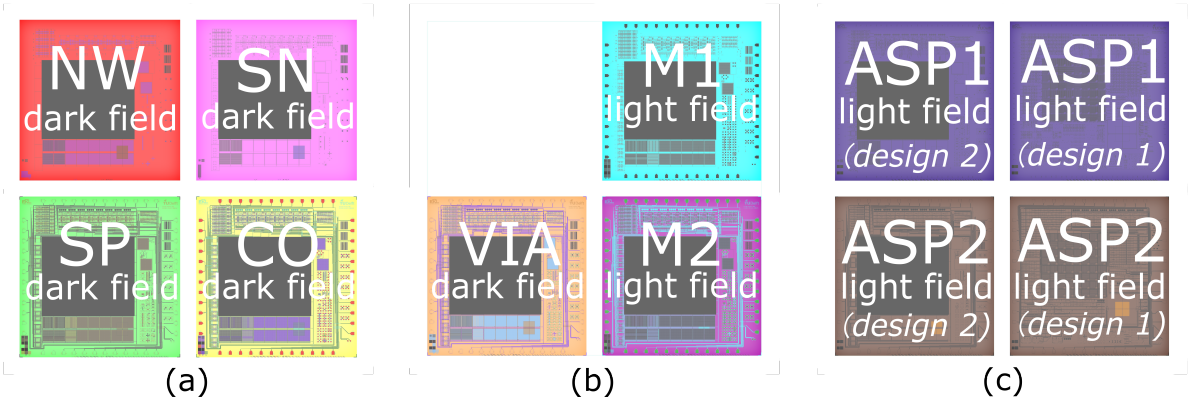


Figure 4.7: Complete mask set.
(a) MASK 1 (b) MASK 2 (c) MASK 3 as identified on the quartz masks

5

Fabrication

The proposed angle-sensitive sensor architecture was described in the previous chapter. This chapter delves into the fabrication process of the design and the results of the fabrication. Firstly, the main IC fabrication steps will be explained to familiarize the reader with IC processing and specifically processing at Else Kooi Laboratory (EKL). Fabrication of the grating stack will follow right after the BiCMOS where design-specific fabrication steps will be illustrated. Section 3 will discuss the influence of various fabrication processes on the resulting grating structure and explain how optimization for the linewidths was performed. Fabrication-related challenges will be mentioned shortly in section 4. Subsequently, fabrication results will be given and commented on in the final section.

The fabrication batch includes four wafers. Each wafer with its implemented pixel type is shown below in Table 5.1. Design of the 1.5 μm pitch amplitude gratings weren't included in the fabrication flow due to the limited availability of implanted wafers and project time. The full fabrication flow of the designs can be found in Appendix F.

Table 5.1: Fabrication wafer batch

Wafer	Implemented pixel type
Wafer 1	2 μm pitch amplitude grating
Wafer 2	1 μm pitch amplitude grating (higher angular selectivity)
Wafer 3	1 μm pitch amplitude grating (lower angular selectivity)
Wafer 4	2 μm pitch phase grating

5.1. BiCMOS Process

Fabrication of planar IC technology requires multiple layers to be superimposed on each other. These layers are defined by specific photomasks at each step. With the ever-increasing complexity of today's modern electronics, the number of layers, hence the number of photomasks needed, increases as well. BiCMOS5 process was developed at TU Delft that would allow low-cost and low-complexity processing for educational and research purposes [26]. As its name suggests, the process is suitable for combining bipolar and MOS transistors on one integrated circuit [27]. (However, this work uses only CMOS process in the electronics and layout design.) A simple CMOS inverter can be fabricated with 5 mask steps which are NW (N-well), SN (Shallow N), SP (Shallow P), CO (Contact openings), IC (Interconnect). These steps are illustrated in Figure 5.1.

Starting material used for the fabrication flow is 4 inch, 525 µm, p-type wafer. Wafer is first deposited an epitaxial layer of single-crystal silicon at high temperature. This step creates a highly uniform and doped layer of silicon on top of the wafer surface. The low-defect epi-layer serves as the bulk region

for n-type transistors.

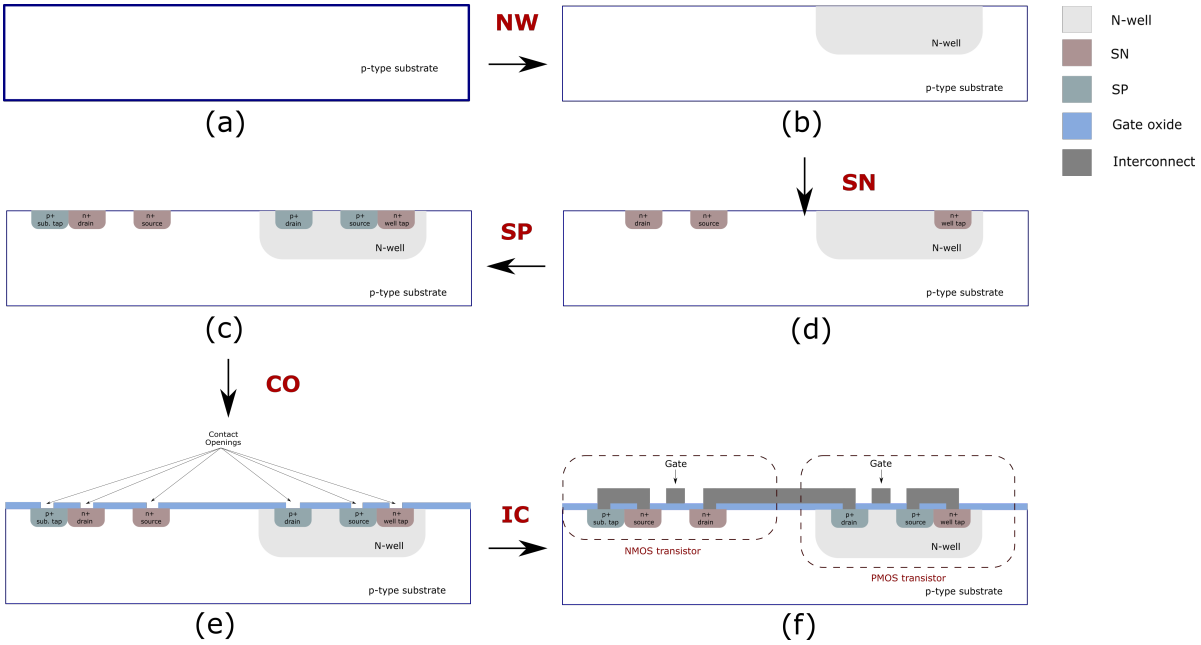


Figure 5.1: BiCMOS5 process flow including the 5 mask steps

Well and channel formation (N-well process)

First step of the N-well process is N-well definition. Phosphorus ions are bombarded into the wafer to form n-type doped regions inside the silicon lattice. N-well regions extend deeper into the wafer than shallow N and P regions, hence ion implantation energy used for N-well formation must be much higher than the energy used for shallow regions. This high energy implantation requires using thicker photoresist layer to stop the ions hitting regions that are not to be implanted. After the implantation, wafer is subjected to annealing (also called 'N-well drive-in') at 1150°C in order to drive the implanted phosphorus ions deep into the silicon lattice to form a deep implanted area. This annealing step also repairs the lattice structure damaged by the high energy ions hitting the crystal and electrically actives the implanted ions. The next two steps are SN (shallow N) and SP (shallow P) layers that define drain and source regions of the NMOS and PMOS transistors respectively. Here arsenic ions are used to create highly doped n-type regions and boron ions for highly doped p-type regions.

Fourth step, threshold voltage (V_T) adjustment, is performed in order to achieve similar threshold voltage values in magnitude for NMOS and PMOS transistors. Implanted boron ions increase the acceptor ion concentration (N_A) in p-type doped regions and decrease the donor ion concentration (N_D) in n-type doped regions, thus shifting the threshold voltage value. Commonly different doping concentrations are implanted on each wafer quarter to find the optimum implantation dose that leads to desired threshold voltages. However, for this flowchart the value $9.0 * 10^{11} ions/cm^2$ was known to gives the closest threshold voltages from Joost Romijn's previous work [28]. Hence, the complete wafer area was implanted using this value.

A thin (20 nm) oxide layer is grown on the wafer before each implantation step. This layer acts as a dirt barrier that scatters the accelerated ions before they hit the wafer surface therefore minimizes the channelling effect. Channelling effect is the disturbance of the desired Gaussian dopant distribution of the implanted ions inside the silicon lattice and it is caused by the implanted ions that travel further into the lattice through the channels created by the orientation of silicon atoms. Another way of minimizing this undesired effect is using implantation rotation of 22° clockwise and tilt of 7°. This makes sure that the implanted ions see the silicon as amorphous as possible [29].

Gate oxidation

After the ion implantation steps that create doped transistor regions, 100 nm gate oxide is grown on the wafer surface with wet oxidation method. Silicon atoms react with H_2O molecules at an elevated temperature resulting in silicon dioxide formation. Dynamics of this reaction and oxide growth rate are described by Deal - Grove model [30]. Oxidation time for 100 nm can be calculated using this model.

$$Si + 2H_2O \rightarrow SiO_2 + H^2 \tag{5.1}$$

Oxide growth rate is influenced by the existence of dopant atoms in the silicon. Higher dopant concentration closer to the silicon surface introduces more crystal defects and creates larger surface area where the oxidation can take place faster [31]. This difference in oxide growth rate results in different oxide thickness on each implantation region. Figure 5.2 shows a microscope image of SN and SP regions of a process wafer with different colors. An approximate oxide thickness can be obtained from oxide color chart. *(Oxide color chart shows the color of the oxide film depending on its thickness.)*

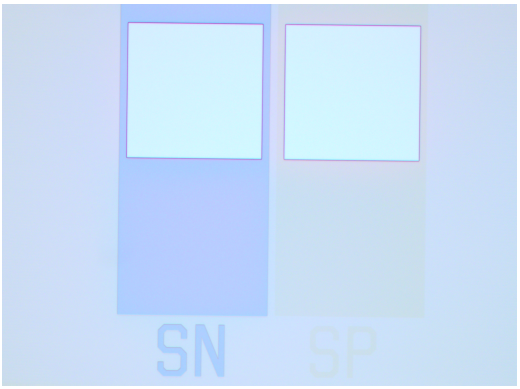


Figure 5.2: Color of SN and SP regions after gate oxidation

Contact openings & Metallization

Contacts to the silicon surface are opened through the gate oxide layer by plasma etching. Afterwards first interconnect layer(M1) is deposited on the whole wafer. Aluminium has been the main metal choice for the interconnect layer historically due to its good conductivity and adhesion to dielectric layers.

Aluminium alloys such as Aluminium 99% Silicon 1% (will be referred to as AlSi) or Aluminium 98% Copper 2% have also been used instead of Aluminium for their better electromigration performance and durability. In this work AlSi is used as the metal for both interconnect layers due to its ease of deposition in EKL, and to prevent the spiking between the interconnect and silicon.

There are three methods of oxide deposition available at EKL. The first one, mentioned in the gate oxidation section, is thermal oxidation. Thermal oxidation, depending on the oxidating gas can be divided to wet and dry oxidation. Both these occur at elevated temperatures (1000°C) and produce high conformity oxide layer. Second one is LPCVD (low pressure chemical vapour deposition) that take place in low pressure furnaces. Using lower pressures for the deposition allows the process to happen at lower temperatures. However, this reduction in the temperature isn't enough to allow processing with metals. This leaves the third type, PECVD (plasma-enhanced chemical vapour deposition) as the main choice of deposition method after metallization where deposition happens at relatively low temperatures of 350°C - 400°C. Deposition also takes shorter time thanks to the high deposition rate of reactive gas molecules in the plasma. The downside of PECVD is that the step coverage and conformity of the oxide layer is much poorer than thermal oxidation and LPCVD. However, greater batch uniformity can be accomplished using PECVD compared to other two methods, where the wafers placed closer to the gas flow tend to have a thicker oxide deposited due to higher gas concentrations.

BiCMOS7 process

Layout design in this work employs two metal layers for the interconnect. The first one, also referred as M1, is the local interconnect that runs between short distances and connects circuit entities that are close to each other. The second metal layer, called M2 or global interconnect, on the other hand stretches along the whole chip area and usually carries signals that must travel along the chip such as V_{DD} and GND, as well as inputs and outputs. This fabrication flow is named BiCMOS7 after the addition of the second interconnect.

Firstly 600 nm PECVD TEOS oxide is deposited on the first metal layer. It acts as an insulator layer between two interconnects and allows us to place the VIAs that connect M1 and M2. After the etching of VIAs, another layer of AlSi is deposited on the wafer and M2 layer is defined using the corresponding photomask.

BiCMOS7 process allows fabrication of complete electronics part of the design. The remaining processing steps are the implementation of the designed grating stack that will allow us to modulate the incoming light beam before it hits the photodiodes on the chip surface. Fabrication steps for the grating stack will be explained in the following section

5.2. Fabrication of the grating stack

Fabrication steps for the grating stack can be seen as an extension of the metallization part in BiCMOS process flow. Their main difference is that interconnect lines have electrical contacts to the wafer surface whereas grating lines don't have any connections to other layers, thus are separate entities. In this section, the fabrication of the grating stack is explained from bottom up in two main steps; 1 - Fabrication steps of the analyser grating *(bottom ASP layer)*, 2 - Fabrication steps of the diffraction gratings *(amplitude phase gratings)*

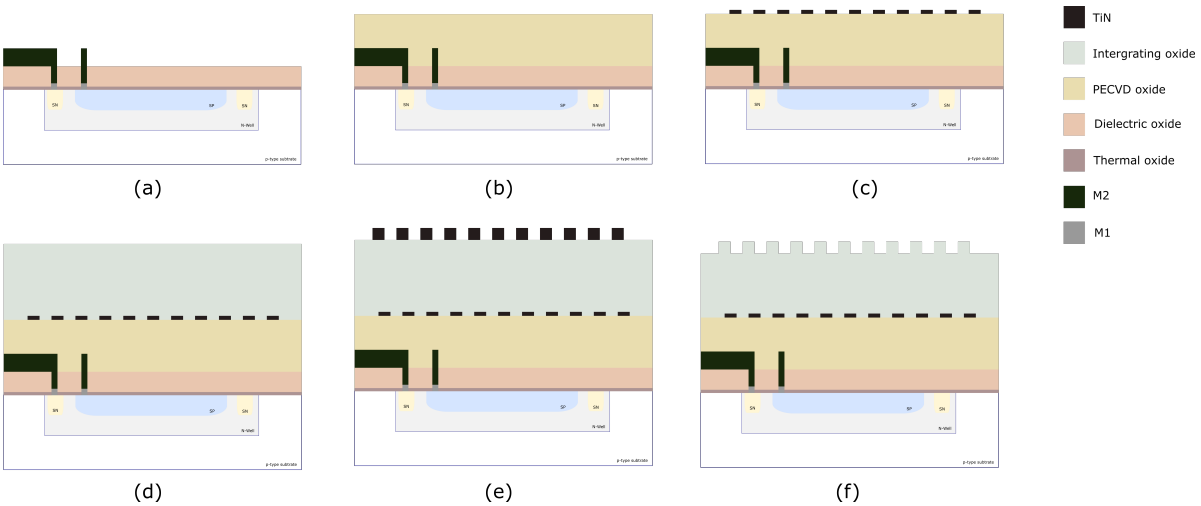


Figure 5.3: Diffraction gratings process flow. (a) Wafer surface after BiCMOS7 process (b) First oxide layer (2275 nm) (c) Bottom grating layer (d) Deposition of intergrating oxide (e) Top grating layer (Amplitude grating) (f) Top grating layer (Phase grating)

1. Fabrication steps of the analyser grating

Step 1: PECVD Oxide Deposition

The first step is the deposition of PECVD oxide to create the 3 µm thick oxide layer as the bottom material for the first grating layer. Figure5.3.b shows the sideview of the wafer after the PECVD deposition. At the bottom of the oxide stack we see 125 nm thermally-grown gate oxide on p-type

doped active region of the photodiode and on top of that 600 nm dielectric material that make up 725 nm oxide on the active area of the photodiodes (SP region). The remaining 2275 nm oxide is deposited at this step and is shown in yellow in Figure 5.3.b.

Table 5.2: Thickness of each layer in oxide stack

Layer thickness	Layer
125 nm	Gate oxide
600 nm	Dielectric oxide
2275 nm	Deposited oxide
3000 nm	Total oxide thickness

At EKL, PECVD depositions are done with Novellus Concept 1 tool that allows two different processes for the deposition of SiO2. These methods, PECVD TEOS and silane based PECVD, use TEOS (tetraethoxysilane), and silane (SiH_4) with N_2O as the source molecule respectively. TEOS oxide is known for its superior step coverage and conformity. These qualities, specifically high conformity makes it a preferrable material for optical applications. However, Novellus TEOS oxide's downside is its worse batch uniformity compared to the silane-based oxide. *(This is due to the specific performance of deposition tool used, not a general fact.)* From the oxide thickness accuracy point of view, silane-based oxide also performed better than TEOS oxide.

After the consideration of the points mentioned above, silane-based oxide is chosen as the deposition material for the grating stack. Firstly, the performance improvement by using TEOS oxide instead of silane-based oxide is not substantially high for the designed grating stack. This is due to the fact that the first layer of PECVD oxide is deposited on a flat oxide on top of the photodiode area, hence there's no topography to cover. Second layer of PECVD oxide is deposited on the thin (100 nm) TiN gratings, hence step height is very short. Second reason for choosing silane-based oxide is higher batch uniformity and deposition accuracy. During the test measurements of oxide thickness, it was observed that silane-based oxide performs much better in these aspects than TEOS oxide. This is not a predictable result; however, it can be tied to the performance of the specific deposition tool employed, namely Novellus Concept 1. Since accuracy of the deposited layer thickness is one of the critical parameters of the grating structure, silane-based oxide was opted for. Ease of silane-based deposition in EKL is another factor. This process is commonly used by the lab users. Hence, deposition rates are up-to-date and well documented. This shortens the processing time since we have an approximate value of deposition rates for various thicknesses before the deposition.

Step 2: ASP Bottom Layer Definition

First step is sputtering of 100 nm TiN film on the oxide stack. *(The reasoning behind the use of TiN instead of AlSi was explained previously in Chapter 2.)* ASP bottom layer is transferred onto the wafer using the designed mask. This process comprises of three steps: coating, exposure, and development. The wafer is first coated with positive photoresist. Thickness of the photoresist layer is dependent on the requirements of the exposed layer as well as the conditions of the existing layers. While wafer topography with deep steps and trenches requires thicker photoresist to cover the whole area, thinner photoresist is used to pattern small structures. In this process, 1.4 µm photoresist was needed to pattern 0.5 µm lines. This meant that the step height introduced by interconnects M1 and M2 would not be covered well with photoresist. However, these interconnect wires don't cross the active pixel areas, where the grating pattern is exposed on, hence making it possible to use 1.4 µm photoresist. In order to increase the resist uniformity along the wafer 'Co-Topo-3012-1.4µm – no EBR' coating recipe is used. This recipe is optimized to produce better step coverage of the wafer topography by spraying the photoresist liquid along the wafer instead of only at the centre. Resist non-uniformity has serious effects on the patterning of the gratings. This will be explained in detail in the fabrication results section.

ASP bottom layer pattern is then transferred on the photoresist using ASML PAS5500/80 wafer stepper. The following step is revealing the transferred ASP pattern via plasma etching of the TiN layer using plasma etcher Trikon Omega 201. Etch rate of TiN is 310 nm/min, thus requiring

19 seconds to etch 100 nm TiN. Initially, the wafer was subjected to 19 seconds of etch plus 7 seconds of overetch (approx. 30%-40% of the etch time). SEM image of the etched lines can be seen in Figure 5.4. SEM inspection shows us that the residues and the lines have similar surface structure, thus the residues are indeed unetched TiN, not dirt particles that might have been stuck on the wafer inside the etching chamber. We can conclude from the metal residues on the wafer that it is not completely etched. However, these residues don't necessarily hinder the performance of the gratings since thin metal films with a thickness of some tens of nanometres can behave as transparent [32]. However, in order to fully conclude that the grating functionality would not be influenced by these residues, the thickness of the thin films must be known.

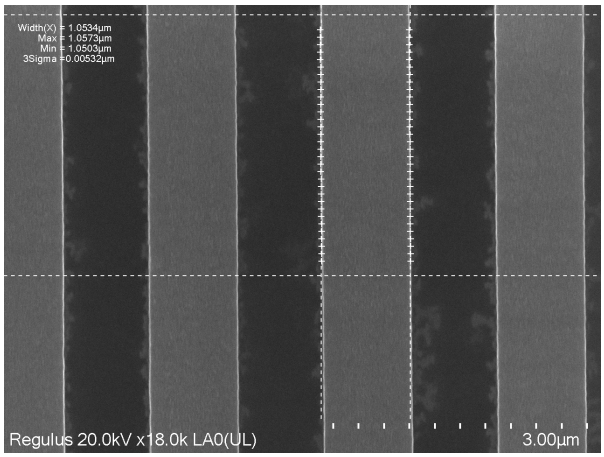


Figure 5.4: SEM image of 2 μm pitch gratings with etch residues

Three test wafers, each with different overetch times are used to test the effect of the overetch time on the residues, line width and overetched oxide thickness. For the overetch time of 11 seconds and above the residues disappear. The main difference observed between these three wafers is the amount of the overetched oxide. This is due to the low selectivity of the dry etching process where etching happens as combination of both chemical and physical effects. Measured step heights and corresponding overetch thicknesses are given in Table 5.3.

Table 5.3: Etch times for bottom ASP layer and corresponding overetched thicknesses of three test wafers

Wafer	Etch time	Overetch time	Step height measurement	Overetched thickness
Ti 1	19 sec	11 sec	115 nm	15 nm
Ti 2	19 sec	15 sec	125 nm	25 nm
Ti 3	19 sec	19 sec	135 nm	35 nm

Wet etching is another method available in semiconductor fabrication to etch metals. Compared the above-mentioned method of dry etching, it offers much higher selectivity hence minimizing the overetch. However, its isotropic etch characteristics, i.e. same etch rate in all directions, makes it vulnerable to underetch and eventually undercuts. Hence, it is not a suitable process for structures under 1.5 μm [33].

2. Fabrication steps of the diffraction gratings

Step 3: PECVD Oxide Deposition

This is one of the most critical steps in the fabrication flow since thickness accuracy of ±100 nm is aimed for the functioning of the grating stack. The most controlled way of depositing oxide was found out to be in multiple layers of smaller thicknesses. At each deposition step oxide deposition rate is measured using a dummy wafer and deposition time is updated accordingly to give the desired thickness. Table 5.4 shows the final oxide thickness for each fabrication.

An important point to note here is that Wafer 4 has thicker oxide than its intergrating spacing. This is a combination of 4.75 μm oxide that will perform as the intergrating spacing and 0.75 μm

oxide that will form the phase gratings after patterning.

Table 5.4: Process wafers and the corresponding oxide thicknesses

Wafer	Deposited oxide thickness
Wafer 1	9.5 μm
Wafer 2	2.37 μm
Wafer 3	7.1 μm
Wafer 4	5.5 μm

Step 4: Definition of amplitude gratings (Wafers 1,2 and 3)

Wafers 1, 2 and 3 are deposited 500 nm TiN which will form the top grating layer. Deposition is done at elevated temperature of 350°C to improve the step coverage of the deposited layer. The wafers are then coated with 1.4 μm photoresist and exposed with the top grating pattern. Metal dry etch is applied once again to reveal the top ASP pattern. Resulting sideview of the amplitude gratings are illustrated in Figure 5.3.e.

Table 5.5 shows the three test wafers (named Ti 1, Ti 2, and Ti 3) etched with different overetched times. Same etch time 95 seconds is used for all three wafers. Ti 1 is overetched 55 seconds, calculated from the overetch time of the bottom ASP layer. Step height measurement shows that this causes 125 nm of oxide layer to be etched. Since this is higher than the tolerable overetch, Ti 2 and Ti 3 test wafers are employed to find the overetch time that would minimize the overetch and not leave any residues meantime. Based on this, 95 seconds etch and 15 seconds overetch is found as the optimum and these values are used for the process wafers.

Table 5.5: Etch times for top ASP layer and corresponding overetched thicknesses of three test wafers

Wafer	Etch time	Overetch time	Step height measurement	Overetched thickness
Ti 1	95 sec	55 sec	740 nm	125 nm
Ti 2	95 sec	35 sec	690 nm	75 nm
Ti 3	95 sec	15 sec	640 nm	25 nm

Step 5: Definition of phase gratings (Wafer 4 only)

Wafer 4 is coated with 1.4 μm photoresist and exposed with top grating layer mask. Following the lithography steps, 750 nm oxide is etched using plasma etching for one minute. Grating depth is determined by the etch time. After the etching, step height is verified using Dek-tak Profilometer. However, the gaps in the gratings are too small for the measurement needle to go in and perform correct measurements. Hence, the measurements are carried out on a test structure on the left bottom corner of the layout Final cross section view is shown in Figure 5.3.f.

Phase gratings are defined in the literature by a post-processing of the amplitude gratings. Thick oxide layer is deposited on the wafer to protect the existing bondpad openings from etching process. Contrary to this way of processing, in this fabrication flow bondpads are etched after the phase gratings are defined. To protect the gratings during long etch process, thicker photoresist is used.

5.3. Optimization of Linewidths

Chapter 3 investigated each design parameters' effect on the functioning of the angle sensitive pixels. One of the parameters that came forward was the duty cycle of the grating pitch. Deviations from 50% duty cycle distorts the periodicity of the final angle signal,hence resulting in an imprecise angle detection. Therefore, it is an important to keep the duty cycle withing the range of 45% - 55%. This requires additional effort especially for 1 μm pitch gratings, since required line widths (500 nm) are pushing the limit of the available stepper lithography technology.

In this section, fabrication steps that influence the printed linewidths are discussed. These steps are **1 - lithography** that transfers the mask design on the photosensitive resist layer **2 - development** that dissolves the exposed photoresist *(in the case of positive photoresist)* **3 - etching** that removes the undesired material parts to reveal the printed design. Out of these three lithography plays the central role and will be given the most attention.

5.3.1. Lithography

Optical lithography is a technique used mainly in semiconductor fabrication to pattern the substrate. Image is projected on the photosensitive resist layer through an optical mask using UV or EUV radiation. Lithography tool used in this work, ASML5500/80B stepper, an i-line stepper which uses light with a wavelength of 365 nm. It is designed for production at 0.5 µm and above. Critical dimension of a lithography system, the smallest dimension that can be printed, can be calculated with Rayleigh criterion shown in Equation5.2 where k_1 is a coefficient, λ is the wavelength and NA stands for the numerical aperture.

$$CD = k_1 * \frac{k_1}{NA} \tag{5.2}$$

Energy Focus Matrix

Understanding the effects of exposure focus and energy on the transferred pattern is one of the most important aspects of lithography. Since the way focus' influence on the exposed linewidth is dependent on the energy (see Bossung plots in the appendix Figure E.1), it is a good approach to use a matrix of focus and energy to see how the line widths are changed in each die as we move along the wafer. Figure 5.5 here shows the die locations on the wafer. Centre die is marked with the black ring. Energy is varied on the horizontal axis, while focus is varied on the vertical axis.

SEM inspection after lithography can reveal the effects of focus and energy. Figure 5.6 shows the effect of the focus on the TiN gratings for the exposure energy of 190 mJ/cm^2. Between focus -0.5 and 0.5 (for a focus change of 1 μm), linewidth changes almost 10%. This proves that even a small focus adjustment can lead to a substantial change in the patterned layer. Meanwhile the effect of the exposure energy is more straightforward than focus. Figure 5.7 compares the linewidths for the energy of 180 mJ/cm^2 and 210 mJ/cm^2 for the same focus of 0. The lines thin down as the exposure energy is increased.

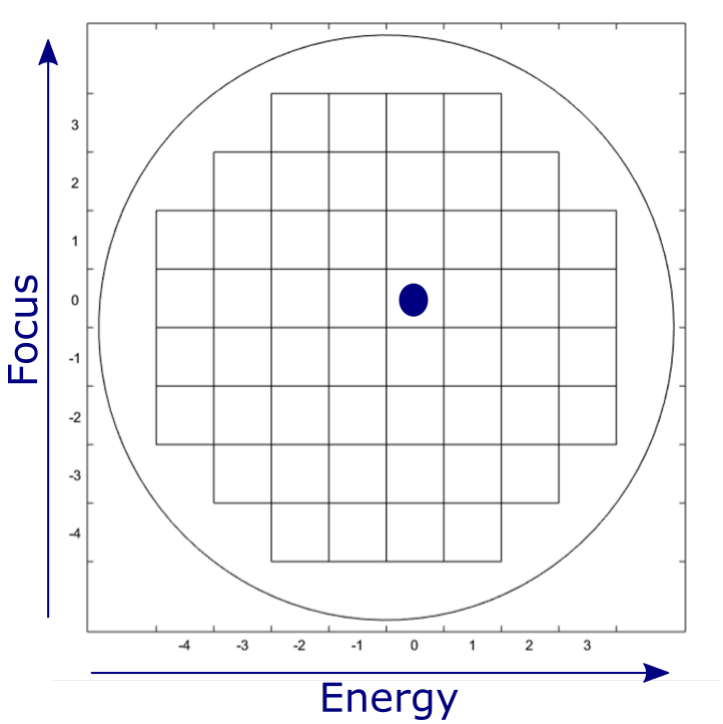
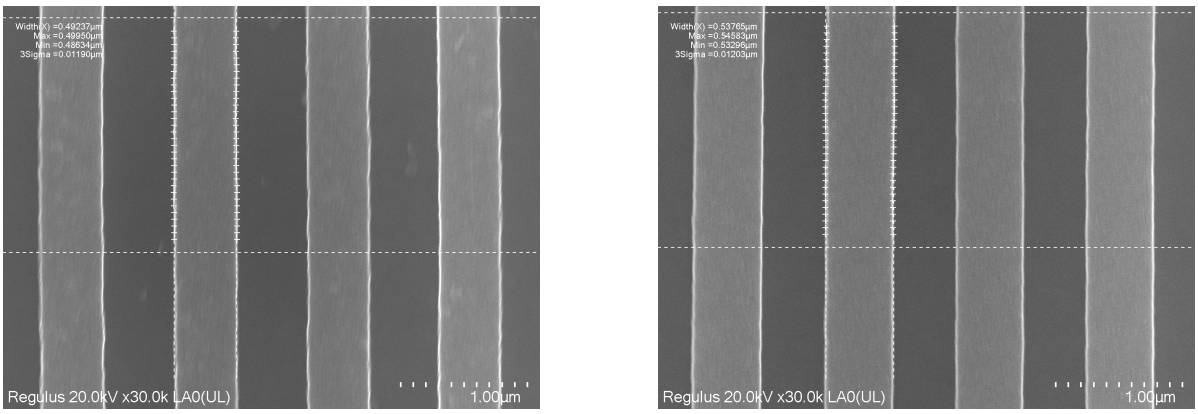
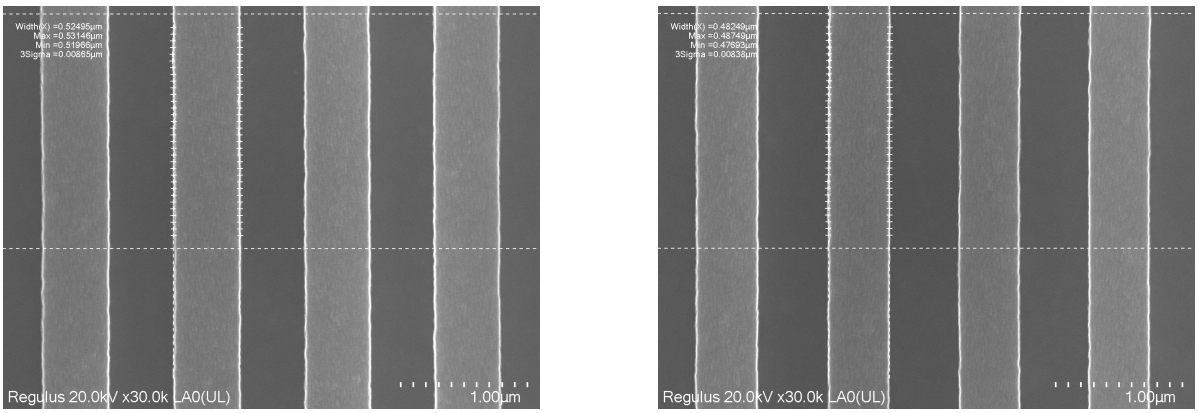


Figure 5.5: Die map showing focus and energy increase directions



(a) E190F0.5 (b) E190F-0.5

Figure 5.6: Linewidths for different exposure focus [dark lines = oxide, bright lines = TiN]



(a) E180F0 (b) E210F0

Figure 5.7: Linewidths for different exposure enery [dark lines = oxide, bright lines = TiN]

Effect of the substrate material

A metal substrate's primary effect on the exposed linewidths occurs through reflections. Figure 5.8 shows the incident exposure beams that reflect from the substrate surface back to the photoresist layer. This reflected beams, when they hit the photoresist, contribute to the exposure; hence resulting in a higher total exposure energy. As a result, linewidths get thinner.

Figure 5.9 compares the linewidths patterned on two different metal films using the same exposure parameters. In Figure 5.9(a) we see TiN gratings with 751 nm width. On its right are the AlSi gratings with 566 nm width. This large change in the linewidths is related to the different reflectivity of the metals. Around 365 nanometer, aluminum reflects more than 90% of the incident light, meanwhile this rate is lower than 10% for titanium nitrate. Due to its low reflectivity TiN is commonly used as anti-reflection coating in lithography processes.

Consequentially, the same amount of increase in the exposure energy creates less change in the width of TiN gratings than AlSi gratings, since the change in the energy is virtually amplified by the reflections of aluminum. This property makes the low-reflectivity materials desirable for applications that require precise linewidth control.

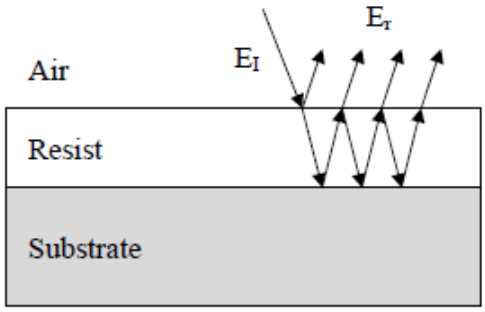
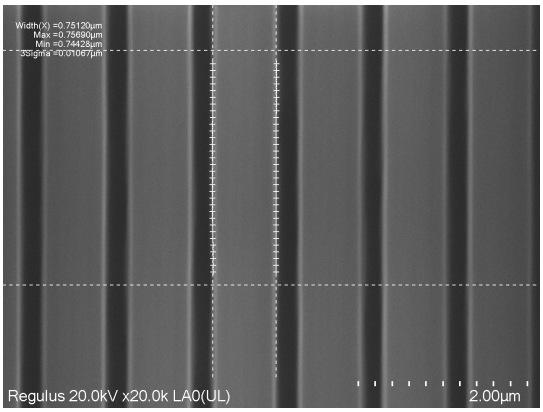
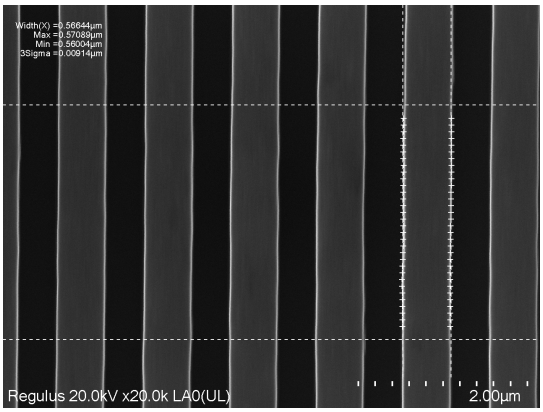


Figure 5.8: Reflections from the substrate and photoresist [34]



(a) TiN gratings with E130F0



(b) AlSi gratings with E130F0

Figure 5.9: Linewidths for TiN and AlSi lines with same exposure parameters [dark lines = oxide, bright lines = TiN/AlSi]

5.3.2. Development

Developing chemical is applied on the photoresist which dissolves the resist parts weakened by the exposed radiation and reveals the transferred pattern on the resist. Parameters such as development time and amount of development liquid affect the resulting linewidths. Figure 5.10 shows grating pattern developed with DEV-DP2 recipe instead of standart DEV-SP recipe. Linewidth shrinks to 882 nm from 1 μm as a result of using longer development time and double-puddle developing. *(Developing liquid is sprayed twice on the wafer in the double-puddle development. This increases the solubility of the resist, hence the development rate. Additionally, the development time of the DEV-DP2 recipe is twice as the development time of the DEV-SP.)*

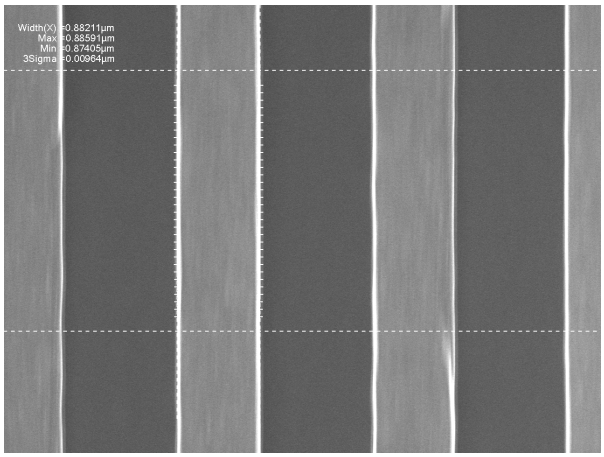


Figure 5.10: Result of DEV-DP2 development after exposure (E130F0) [dark lines = oxide, bright lines = AlSi]

5.3.3. Etching

Etching is the last step of the patterning process. *(Etching here refers to the plasma etching of metals.)* Out of the mentioned three factors it has the least effect on linewidths. Plasma etching is anisotropic, it etches only in the direction of the bombarded ions. This prevents the underetching of the patterned lines.

5.4. Fabrication-related Challenges

This sections aims to identify the challenges related to the fabrication of the diffraction gratings. Some cleanroom-related challenges are also included to inform the reader who would like to continue or replicate this process.

- Optical imaging
  There are two main issues concerning the optical imaging of the diffraction gratings. First is the insufficient magnification of the optical microscopes. A regular optical microscope's magnification can go up to 1500x. This is substantially lower than the required magnification. *(As a reference, 15kx magnification is used to measure the line thicknesses with SEM)* Another issue is observed with Keyence microscope where the diffracted rays from the grating acts as a noise and makes the image very difficult to distinguish. As a consequence, in this work only SEM imaging was used.
- SEM imaging
  SEM imaging was employed to inspect the gratings mainly to measure the linewidths and check the etching quality. However, SEM imaging has its own drawbacks on measuring the linewidth. First limitation is the change in the auto-measured linewidth with beam voltage since the line borders get more indistinguishable in higher beam voltages. Second one is the change in the

auto-measured linewidth with the location of the measured entity on the screen. Since these changes are within the 2% of the linewidth, close to the measurement accuracy of SEM, they were neglected. However, they still do limit the correct identification of the linewidths and hence their optimization.

- Photoresist
  Photoresist thickness has an important effect on the CD. This has two important consequences on the fabrication process. Firstly, thin photoresist layer must be used to be able to pattern small structures. For example, smallest feature size that can be patterned on 1.2 μm AZ ECI 3012 photoresist is 0.35 μm [35]. If smaller lines are required, photoresist thickness should be decreased as well. Second is the linewidth variations along the wafer due to resist non-uniformity. This causes the devices on the same wafer to be slightly different from each other and eventually decrease the yield.

- Connection error in the layout and correction
  During the test runs it was realized that MASK2-IMAGE4 has a layout error which causes disconnection through the local interconnect lines in 3T-pixel read-out. This gap in the layout, shown in Figure 5.11.a, is measured to be 0.5 μm and the lines themselves are 12 μm. This error can be corrected during the patterning of the mask design on the wafer surface using a combination of low exposure energy and off-focus techniques. Resultant wafer after etching is shown on the right side of the same figure.

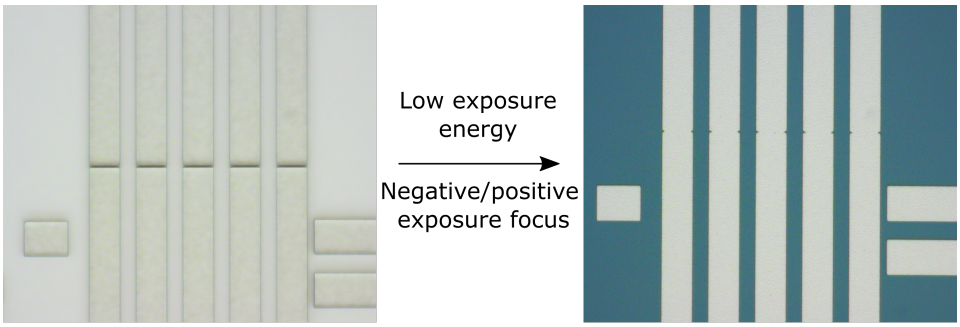


Figure 5.11: Layout error and its correction with lithography

5.5. Fabrication Results and Conclusion

In this section fabrication results will be presented in two parts. We will first focus on the angle sensitive pixels and assess the results of their fabrication through optical and SEM imaging. Afterwards electrical properties of the chips will be investigated to verify fabrication parameters.

Linewidths and duty cycles of each pixel type are given in Table 5.6 along with their corresponding exposure parameters. Same development and etching recipes are used for all 3 pixel types. Duty cycle deviation of both 2 μm and 1 μm grating pixels fall within the intended 5% range. This demonstrates that the chosen lithography method and exposure values were well fitted for the aimed design.

Table 5.6: Final exposure values and resulting linewidths of process wafers

Pixel type	Exposed material	Exposure values	Linewidth	Duty cycle
2 μm amplitude grating	TiN	E = 210 mJ/cm^2 F = 0	1046 nm	52%
1 μm amplitude grating	TiN	E = 190 mJ/cm^2 F = 0	509 nm	51%

Wafer 1 is shown in Figure 5.12 after complete fabrication process. The beams reflected from each diffraction grating creates a colorful wafer surface. These coloring changes with the orientation of the wafer due to the existence of both vertical and horizontal gratings. Grating pitch also has an effect on the wavelength of the reflections, thus determining the color pattern on the wafer. This characteristic property of the diffraction gratings can be utilized to assess the linewidth uniformity along the wafer. Microscope images that compares different linewidths on different die locations are given in the appendix Figure E.3 and Figure E.4.

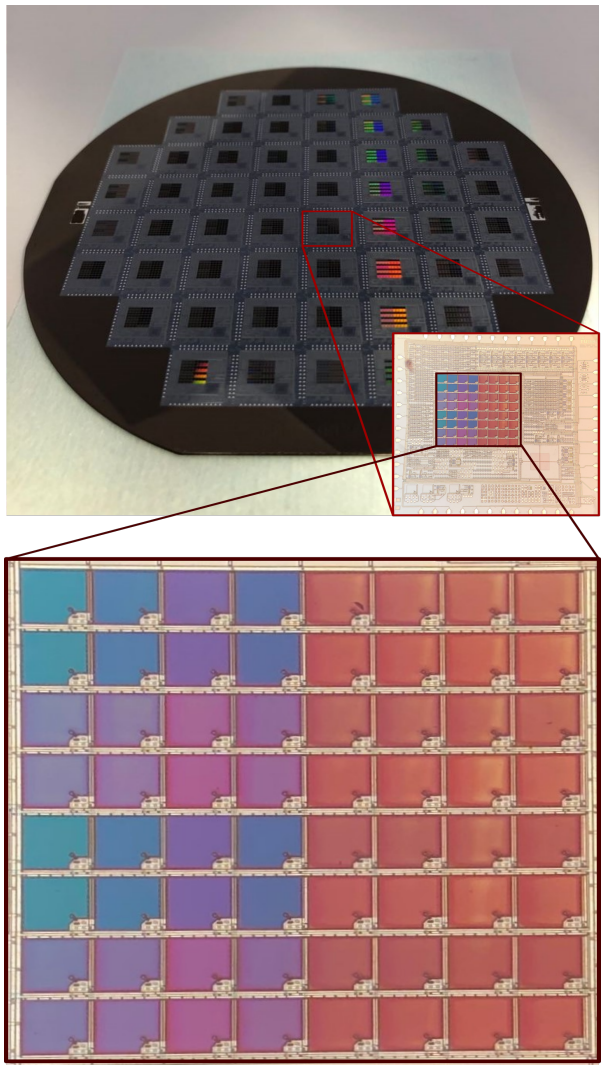


Figure 5.12: Fabricated wafer focusing on a single die and pixel array

SEM imaging is carried out on one of the fabricated chip in order to inspect the cross-section of the gratings. Complete grating stack together with the underlying oxide and silicon substrate are shown in Figure 5.13. Thin bottom grating layer is buried 9.5 μm deep in the dielectric layer under the top grating layer with an offset of 0°. Cross-sectional SEM images of complete pixel set with four different offsets are included in the appendix Figure E.5. Top gratings are brought to closer inspection in Figure 5.14. Small steps heights introduced by the bottom ASP layer are well covered with the top layer. Due to the sloping and rough edges of metal lines, the measurement accuracy of the linewidths is not very high.

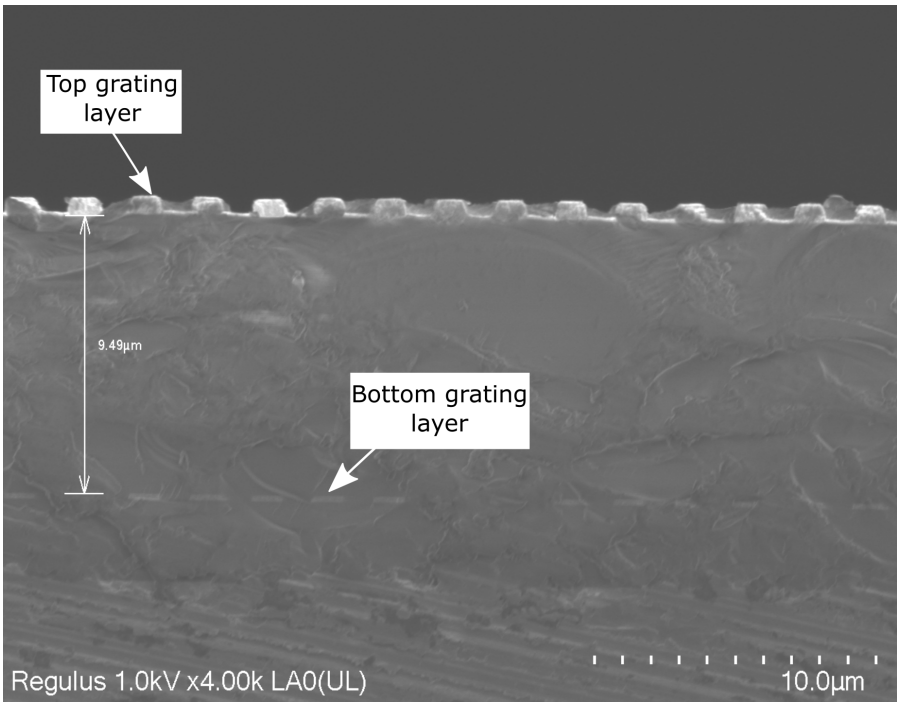


Figure 5.13: Cross-sectional view of Wafer 1.
Grating stack (from bottom up): 100 nm thick bottom grating layer, 9.5 μm intergrating spacing (PECVD oxide), 500 nm thick top grating layer

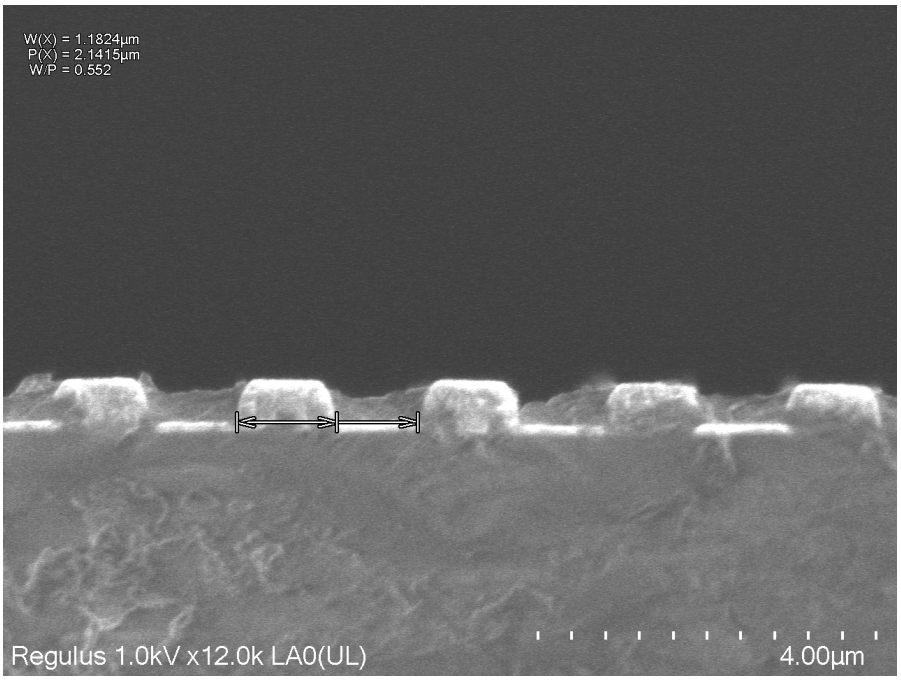


Figure 5.14: Linewidth measurement of 2 μm pitch gratings.
Width = 1182 nm, Pitch = 2141 nm

5.5.1. Fabrication verification

Initial verification of the design and fabrication is carried out by electrical measurements using Cascade33 Microtech probe station.

1. Electrical resistivity measurements
   Sheet resistance of the doped regions are measured right after the fabrication of first interconnect layer (M1) to check the contact of M1 to the substrate as well as verify the doping doses of each layer. The measurements are done using van der Pauw method which allows accurate four-probe measurements of substrate resistances. Current is forced from one probe and taken off at the opposite contact. Voltage is sampled via other two probes and the sheet resistance of the substrate is found using the equation5.3.

$$R_{\square} = \frac{\pi}{ln2} * \frac{V_{measured}}{I_{forced}} \tag{5.3}$$

   Doping concentration of each region can be verified using the sheet resistance measurements. This is due to the doping ion concentration's influence on the mobility and hence conductivity of the material. For this process, approximated values of expected resistance for each region are, for NW 10^3 Ω, for SN 60 Ω , for SP 120 Ω.

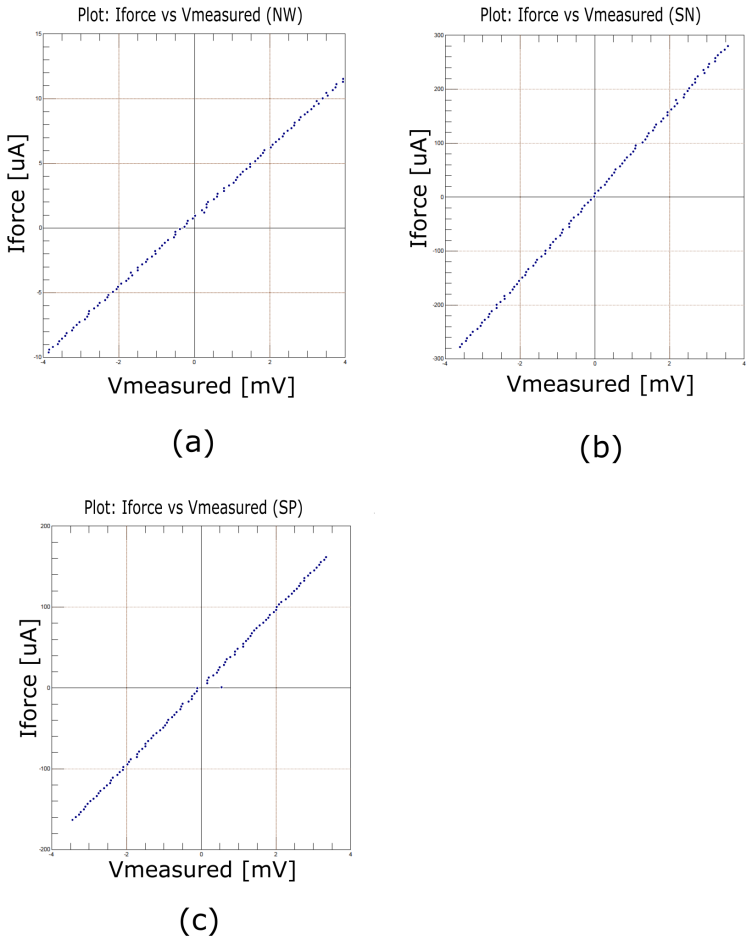
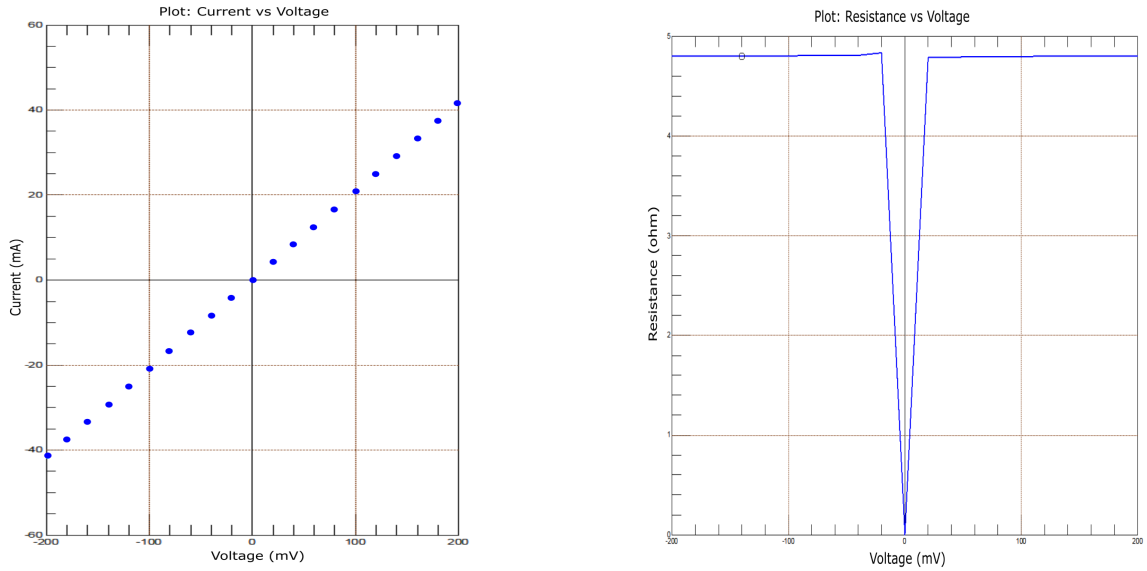


Figure 5.15: van der Pauw 4-probe resistance measurements of NW, SN & SP regions. Measured sheet resistances for each region are: for NW: 1.5 kΩ for SN: 53 Ω for SP: 87 Ω

2. Resistance measurements after complete fabrication

Die-level electrical measurements are carried out to confirm the connections of V_{DD} and GND interconnects as well as bondpad openings. Three different resistance measurements are done: V_{DD} to V_{DD}, GND to GND and V_{DD} to GND. In the first two, interconnect lines are short-circuited, hence resistance value is expected to be 0 Ω or very close to it. In the latter however, two contacts ideally shouldn't be connected to each other, hence resistance value is expected to be infinity or rather a very high number in reality. The Iv and resistance curves of the V_{DD} to V_{DD} measurement is shown in Figure 5.16. Small line resistance (4.8 Ω) indeed verifies that line is short-circuited.



(a) Current vs Voltage

(b) Resistance vs Voltage

Figure 5.16: Electrical measurements after complete fabrication

6

Measurements & Device Characterization

The chapters up to this point covered the design and fabrication of the proposed lensless CMOS angle sensitive pixel. In this chapter, optical measurements will be carried out to characterize the fabricated chip. Firstly, an overview of the measurement setup will be presented. Following this, measurement procedure will be explained and measurement results will be presented. Interpretation of the results and conclusions will be given in the last section of the chapter.

Following the fabrication of four different pixel designs on different wafers, Wafer 1 is diced, packaged, and wire-bonded in order to make electrical connections to the chip. The measurements presented in this chapter are carried out on the wire-bonded chips of Wafer 1 with 2 μm grating pitch.

6.1. Optical Measurement Setup

Optical measurement setup is built from scratch inside an enclosure as shown in Figure 6.1. The enclosure is patched from the sides properly to prevent any entry of ambient light. Inside the enclosure, optical setup is mounted on an optical table and it includes a rotation table to vary the angle, a PCB to mount the angle sensitive chip as well as to make electrical connections to the chip, a red LED and collimator to supply the collimated rays, and a breadboard to bridge between the PCB and other electrical components of the setup. The use of the collimated beams is based on the far-field light source application. Since the light source is at far-field, beams radiated from the source can be assumed to be parallel as they hit the small chip surface. However, LEDs are incoherent light sources and radiate uncollimated light unless they are inherently collimated by design or augmented with an external collimation adaptor. In this setup, ThorLabs M625L3 625 nm wavelength (red) mounted LED and COP1-A collimator are used for the generation and collimation of the required parallel beams. *(625 nm LED is the closest available LED wavelength to the design wavelength of 632 nm. Its effect on the device performance is discussed in the next section.)* After the installation of the setup, it is prerequisite to the measurements that collimation of the light source must be well adjusted. A well-collimated beam should not diverge or converge at any point and this can be observed from the image created by the light source. The image must be circular and homogeneous which indicates the well-collimation of the beams. If beams are not well-collimated, discrepancies occur between the angles each pixel sees and disrupts the angle detection step.

A PCB with mounted chip is placed right across the light source, with adjusted distance for best collimation as shown in Figure 6.2. It stands clipped on a rotation table used for vertical and horizontal angle adjustments. PCB is placed with 0°with respect to the horizontal plane of the rotation table. However, this initial angle placement of the PCB is not error-free and can create a certain amount of angle offset in the measurements. This can be easily corrected later on during the process of off-chip angle detection.

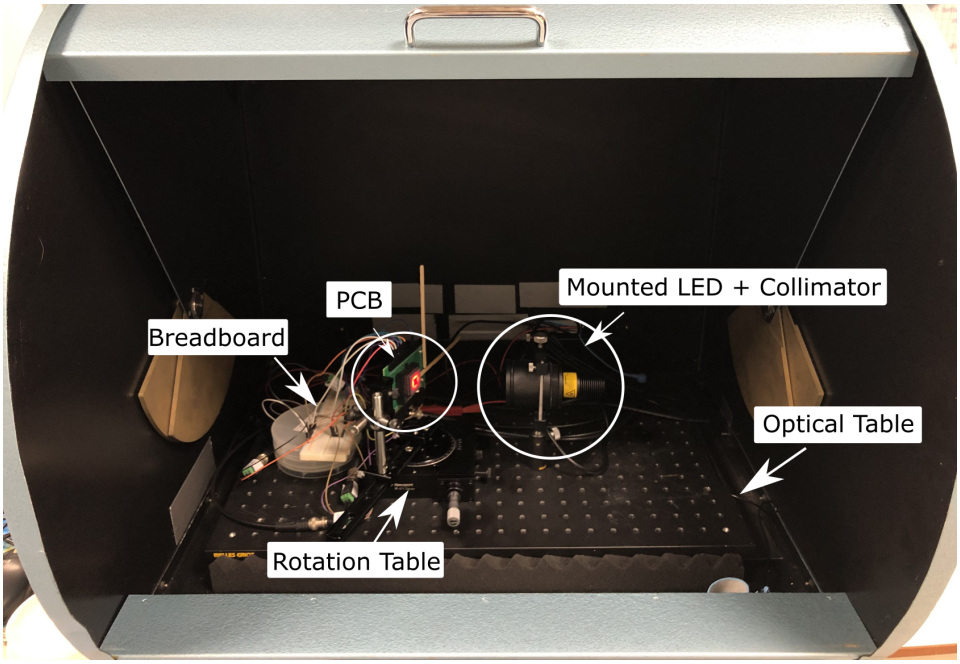


Figure 6.1: Enclosure containing the optical measurement setup

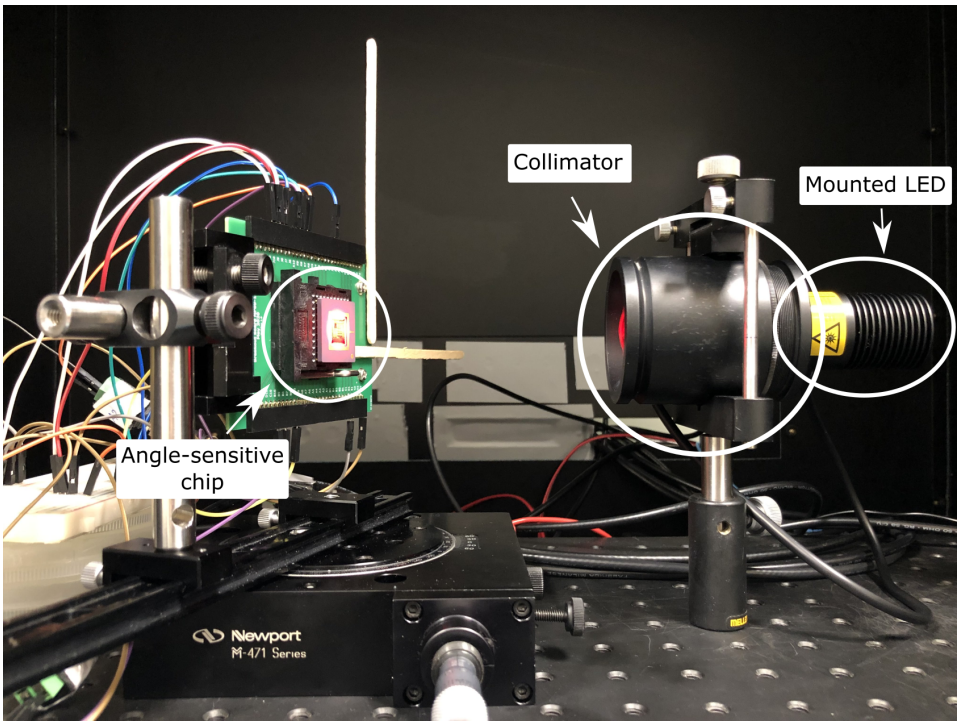
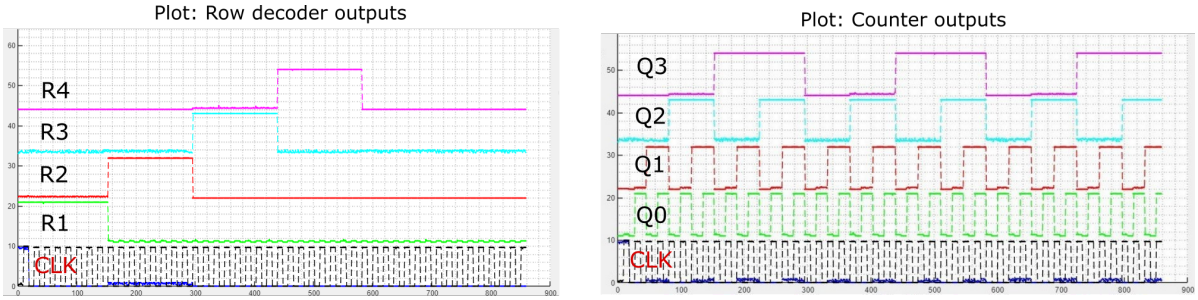


Figure 6.2: Main components of the measurement setup

6.2. Device Characterization

Correct operation of the chip is verified by checking the row and counter outputs before the optical measurements. Counter outputs are generated by the address generator block. This 6-bit code that signifies row and column information of the pixel array increases with each clock cycle until the complete array is covered, then the cycle starts again. It is important for the counter to work correctly in order to measure each pixel at distinct time intervals and not to have overlapping pixel outputs. Least significant 4 bits of the address information is shown in Figure 6.3.b as Q3, Q2, Q1, and Q0. As it can be seen on this figure, counter is counting correctly with the clock signal. Most significant 3 bits of the address information are decoded by the row decoder to generate the row information shown in Figure 6.3.a. Each row signal is 8 clock cycles wide corresponding to the 8 columns at each row. Furthermore, correct pixel operation is controlled with dark and light measurements of each pixel output. Based on this verification of pixel outputs, 5^{th} row's first 4 columns (2 μm grating pitch, vertical ASP pixels with 4 different phase offsets) are chosen as the pixels to be measured.



(a) (b)

Figure 6.3: Initial circuit operation verification through a) row decoder outputs, b) counter outputs

Separate reset signals are used for the counter and pixels, RST1 and RST2 respectively to ensure consistency between pixel measurements. The first reset for the counter is only high at the beginning of a counting cycle. The second reset, on the other hand, is activated only for the measured pixels at the beginning of their measurement cycle. The use of the pixel reset is illustrated in Figure 6.4. Reset is high for a short time at the beginning of the measurement of each of the four target pixels. As soon as it goes back to zero, the pixel read-out starts to decrease due to the photocurrent generation. Slope of the each voltage output is proportional to the slope of the pixel current since signal path of each pixel output is assumed to be equal, hence pixels see the same equivalent resistance. This forms the base of the measurement method. During each measurement cycle, pixel voltages are sampled. During the off-chip signal processing, sampled signal is smoothened to improve the robustness of the measurements. Afterwards, smoothened curve's slope is derived using first order linear approximation. Finally, angle is calculated using Equation 2.3.

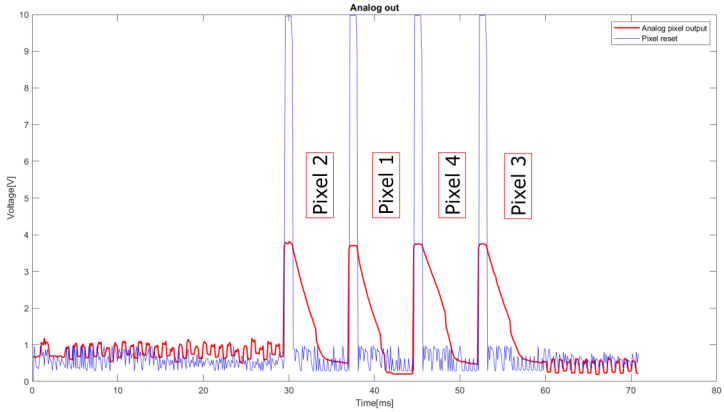


Figure 6.4: Resetting and read-out of 4 different pixels

6.2.1. Measurement Results

Optical measurements are performed using the measurement method explained in the previous section. The angle range is determined as $\pm 26^{\circ}$ with 1°increments as the coherence of the illuminated pixel area is distorted for higher angles. This is due to the increased distance between corner pixels and the light source since these pixels get further away from the well-collimated range. Non-normalized measurement results are presented in Figure 6.5. Horizontal axis signifies the angle of the vertical placement of the angle-sensitive chip on the rotation table, and vertical axis represents the calculated angles using measurement data.

The angle plot is periodic as it is an expected characteristic of an ASP architecture. The period of the curve may not be easy to read from the plot directly. The best method to calculate it is using the angular sensitivity. Angular sensitivity corresponds to the slope of each period since vertical axis is in fact equal to angular sensitivity times angle $(\beta\theta)$ as stated in Equation 2.3. Angular sensitivity of the periods are calculated to change between 22 and 23, resulting in a period of approximately 8°. This can also be observed on the Figure 6.5 where each angle period contains 8 distinct angle points. Exception to this happens at the second and third periods from the left due to the misplacement of -12°. The error at this data point can be explained in two ways. Firstly, it can be a characteristic of the fabricated structure. As it was investigated in Chapter 3, changes in the device geometry can cause perturbation in the angular response. In this case, if the device is well-characterized, the shift of the data point can be corrected during the angle detection phase. The second way that can cause this shift is the measurement inaccuracy. This is very likely since the maxima of the third period(-5°) is also not at the expected location, namely around 90°. Both of these errors call in the possibility that all data points on the third period together with -12°are shifted approximately +1°during the measurements.

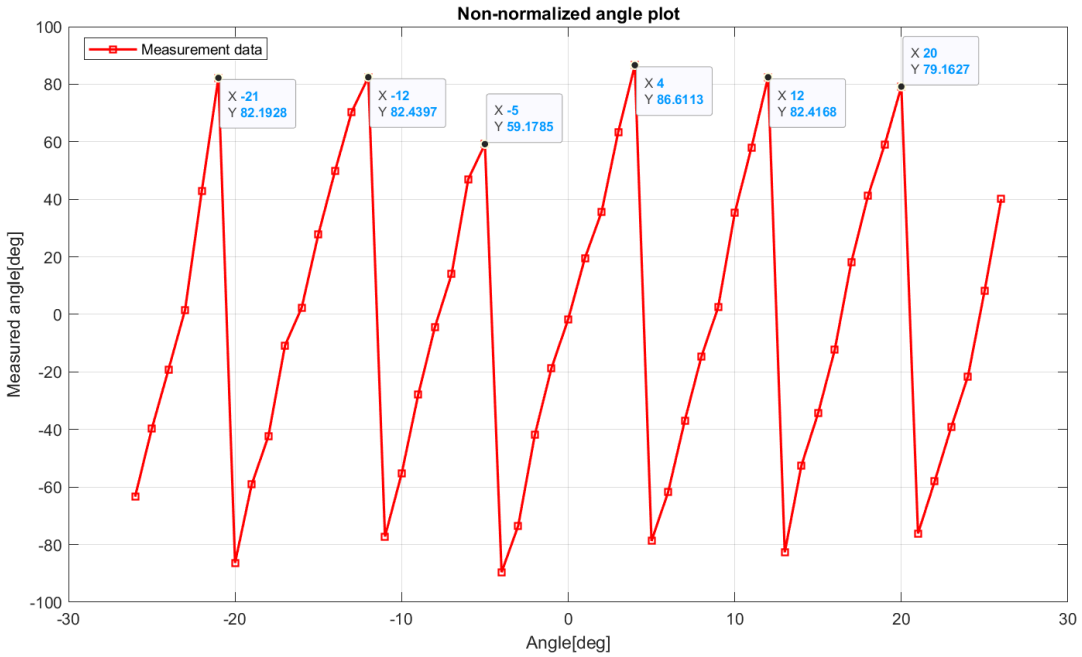


Figure 6.5: Measured non-normalized angle points for angle range of ś26°

Final measurement results, normalized with angular sensitivity are presented in Figure 6.6 as the red data points. Angular sensitivity values used for normalization are given in Table 6.1. The curve follows the general trend of cyan coloured ideal line with an exception at -12°as expected. The use of the characterized angular sensitivities increases the accuracy of the measurements. However, theoretical value of 20 can also be used with a certain degree of accuracy loss. Mean absolute error is calculated for both cases as listed in Table 6.2. This shows that angle accuracy can be improved significantly with device characterization and off-chip angle corrections.

Table 6.1: Angle sensitivities of each period

Angle range	Angular sensitivity	Corresponding angular period
−26°-−21°	28.5	6.3°
−20°-−12°	22.2	8.1°
−11°-−5°	23.4	7.7°
−4°-4°	21.8	8.3°
5°-12°	23.3	7.7°
13°-20°	23.2	7.7°
21°-26°	22.8	7.9°
Theoretical value	20	9°

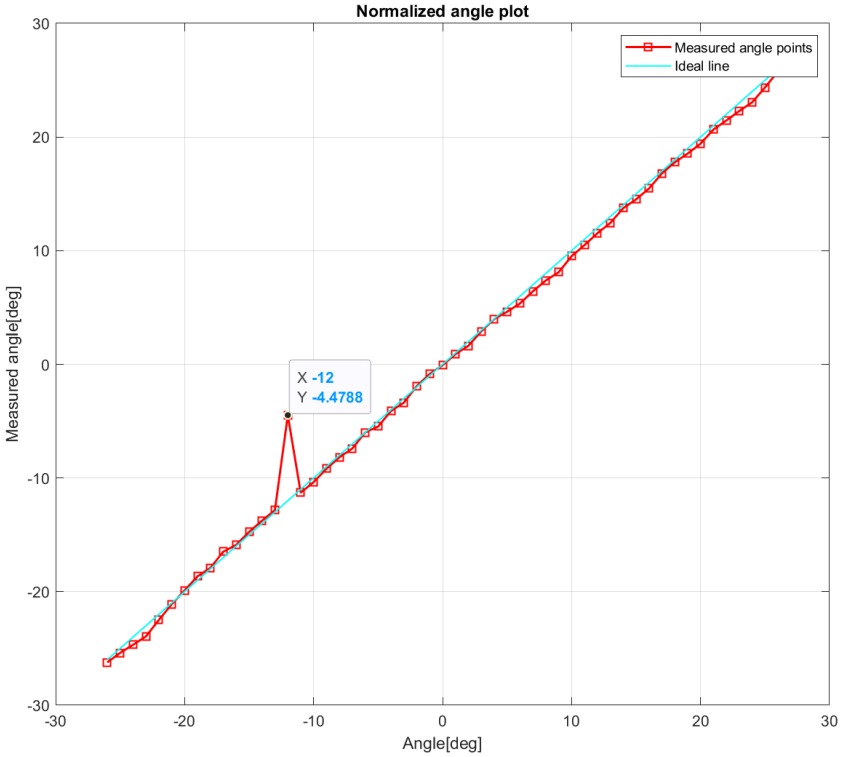


Figure 6.6: Normalized measurement results (using the values in Table6.1)

Table 6.2: Mean absolute error of angle measurements

Angle calculation method	Mean absolute error [deg]
Normalized with $\beta = 20$	0.63
Normalized with $\beta = 20$ & corrected for-12°	0.48
Normalized with values in Table 6.1	0.50
Normalized with values in Table 6.1 & corrected for-12°	0.37

Measured angle results are shown comparatively with the simulation results in Figure 6.7. The first and the most clear observation is the difference between the angular periods of two curves. Simulation results, shown by blue curve, show periodicity between 8.6°- 8.9°. This suggests that the fabricated device has higher angular sensitivity than the simulated model. There can be couple of reasons that explain this change. The first one is the use of 625 nm wavelength LED instead of the design wavelength of 632 nm. This decrease in the light wavelength increases effective Talbot depth, hence increasing the angular sensitivity (shown in Equation 2.4). The second one is the printed pitch of the gratings being higher than the designed 2 μm. The effect of this is similar to the wavelength, it contributes to the increase of the effective Talbot depth and thus the angular sensitivity. However, the combined effect

of both of the mentioned factors brings the period down to 8.6°. The third one can be the effect of non-planarized grating surfaces. Due to the step height created by the bottom grating layer, top grating surface is not as ideal. However, how non-planarized surfaces influence the angular sensitivity was not investigated by this work.

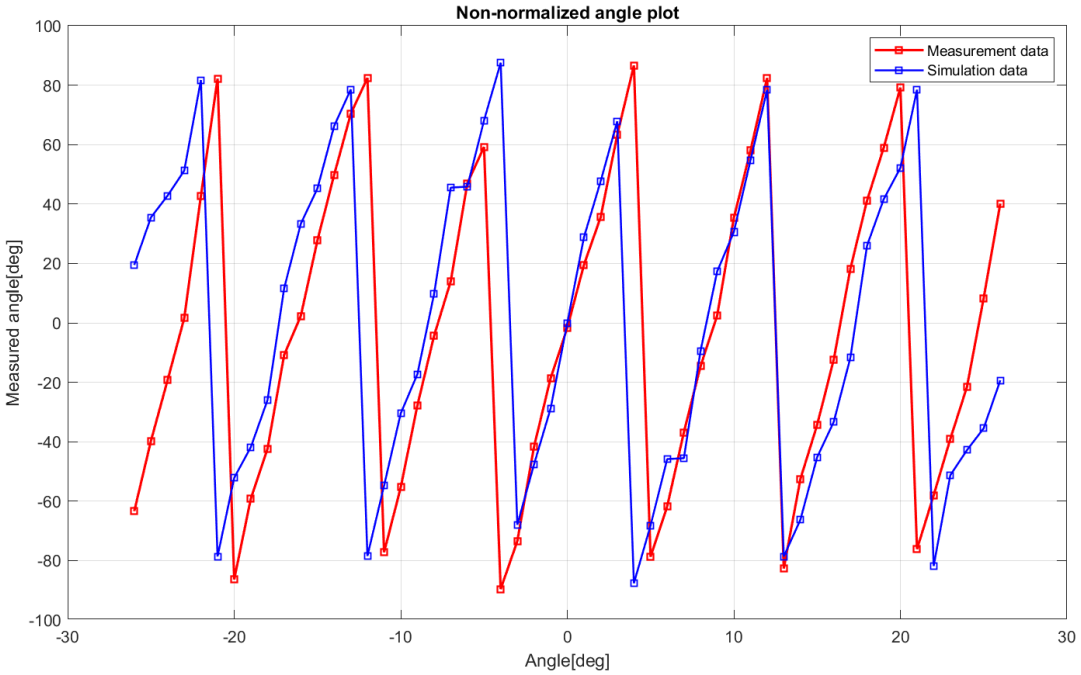


Figure 6.7: Comparison of angular responses of measurement and simulation data

The differences in angular sensitivity between the simulation and measurement results are also reflected on the angle detection. On average, there is 0.8°difference between the final angles calculated using these two data sets. These angles are shown in Figure 6.8 compared with a linear ideal angle curve.

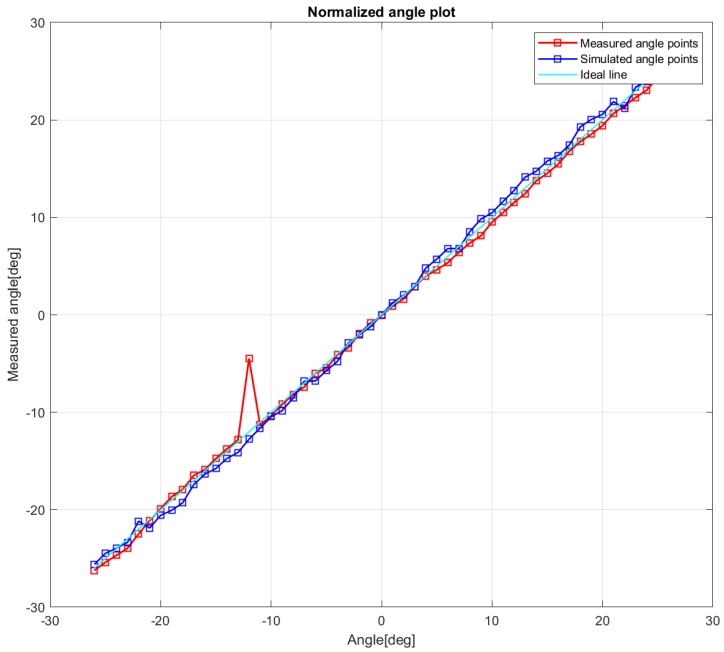


Figure 6.8: Measured and simulated normalized angle points compared with an ideal angle line

6.3. Conclusion

Angle-sensitive chip with 2 μm grating pitch ASP structures was measured under a well-collimated 625 nm red light illumination and its angular response was recorded within $\pm 26^{\circ}$ angle range in vertical direction. Measured angular response shows a periodic characteristic with a period of approximately 8°. The difference of angular periods between the simulation model and measurement results can be attributed to the variations in the fabrication process as well as the wavelength of the light source. Properties of the materials used in the fabrication (such as reflectivity of the metal) may not match with the parameters in the simulation model. Furthermore, the change in the inter-grating dielectric thickness and the effect of non-planarized grating surfaces contribute to this discrepancy.

Measurement results are compared to ideal angles as well as simulation results using mean absolute angle error (MAE). Direct processing of the measurement data without prior pixel characterization results in 0.63°MAE compared to the ideal angle curve. Corrections for the angular period and varying angular sensitivity of each period can reduce this error down to 0.37°. Considering that the simulation model results in 0.58°MAE using the same angle detection method, response of the fabricated device is considered very good.

Another important factor that affects the angle accuracy of the measurements is the accuracy of the measurement setup itself. The angle is controlled manually using the knobs of rotation table with 0.1°resolution. Hence, this should also be considered while calculating the angle accuracy of the fabricated ASP.

7

Conclusions and Future Work

This chapter will present an overview of the design steps and the research objectives reached in the previous chapters. Following, the research questions will be revisited and answered by the research conclusions. Recommendations on the future work will conclude the chapter.

7.1. Summary of Research Conclusions

Literature review was conducted to identify state-of-the-art lensless image sensor architectures, the angle detection techniques and assess their angular responses. Evaluation of pixel structures with respect to their angular sensitivity, complexity, and manufacturability resulted in a conclusion to select amplitude and phase grating based ASPs as the main pixel type for the proposed device. ASPs offer high angular sensitivity and they are easy-to-implement in BiCMOS process. However, their high angular sensitivity comes with a drawback of smaller number of resolvable angles. In order to compensate for this drawback and aid ASP with identifying angle periods, metal shading structure is integrated to the proposed device design.

Simulation-based pixel characterization was carried out to determine the design parameters of ASPs. Angular response of an ASP was identified to depend mainly on its geometry, the choice of materials, and the incident light's properties. 632 nm red light was selected as the design wavelength to keep the intergrating dielectric thickness within the determined range while keeping the pixel variations possible. Using this particular design wavelength and the limitations of the available lithography technology pinned down the grating pitch of the pixels between 1 μm and 2 μm. Hence, four different pixel types were designed in order to achieve four different angular responses with grating pitches within this range. This richness in the angular information was intended to help increase the accuracy of angle detection.

During the fabrication step, linewidths of each grating type was controlled with lithography steps. Exposure parameters were optimized to achieve 50% grating duty cycle. Exposed material was also found out to be as important as the exposure parameters on the patterned linewidths. At the end, 52% and 51% duty cycles were achieved for 2 μm and 1 μm grating pitch pixels, respectively. The gratings were implemented on top the photodetector array without using surface-polishing. In order to decrease the effect of step heights on the angular response of the pixels, bottom grating thickness was reduced to 100 nm, while top grating layer was 500 nm to successfully cover the steps. Similarly, for the phase gratings a thick phase step was decided to be implemented as the top grating layer.

Angular measurements were carried out using an optical angle measurement setup. Due to its availability, 625 nm red LED was employed rather than the design wavelength of 632 nm. This had a small effect on the effective depth of the Talbot self-images, however it wasn't enough to explain the deviation in the angular period on its own. Variations in the deposited oxide thicknesses, and mismatches between the values of simulation parameters and fabrication parameters were presented as other pos-

sible influences on the angular period. Although period was shifted to 8°from 9°, it was observed not to seriously alter the accuracy of angle detection since linearity of the angle curves in each period was preserved. Angle detection was only affected severely at the transition angles between the periods and these points showed approximately 7°angle error. However, since the calculated angle falls outside of the range of the corresponding angular period (8°), this error can be easily pointed out and corrected with the help of metal shading structure. Accuracy of the proposed design can be improved significantly if device is characterized once for the employed fabrication process flow. It is very likely that the shifts in the angular periodicity and specific angle locations are a result of the specific fabrication processes. Once these are identified, accuracy of the device can be increased up to 0.37°.

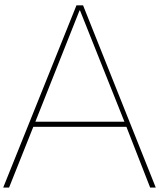
Above-stated research conclusions gave an overview of the design, fabrication and characterization stages of the proposed pixel architecture. The measurement results show higher than 1°angle accuracy achieved through the use of an ASP image sensor architecture for angle detection application. Thus, this work successfully demonstrates lensless image sensor architecture realization for light source tracking applications with integration in BiCMOS process.

7.2. Future Work and Recommendations

The method of angle detection using ASPs was demonstrated in this work for high visible wavelengths. This design can be optimized for different wavelengths, such as UV that would allow its successful application as a sun position sensor. Moreover, the use of smaller wavelengths would require smaller grating pitches, hence it can help further scale down the pixel sizes. Scaling of the pixels is desired from many aspects for miniaturized space applications as explained in Chapter 1. However, this would require patterning of thinner lines that is not currently possible in EKL. Miniaturization of the pixels is also beneficial from the measurement point of view. As mentioned in Chapter 6, limited collimation range of the light source had restricted the measured angle range to ±26°. This can be mitigated to a certain point with smaller pixels. Additionally, four pixels of each ASP type can be placed in a quarter-shaped structure rather than lining them next to each other. This would improve the angle detection by minimizing the incident angle variations between the pixels.

Fabrication steps can be improved to improve angular response as well as to minimize the discrepancies between the measurement and simulation results. TiN etching recipe can be further optimized to result in a lower overetch rate. Current recipe has the same parameters for etch and overetch, and this leaves the wafer surface more vulnerable to the ion bombardments during the overetch time. Wafer surfaces can be planarized through surface polishing to improve the angular response of especially phase gratings whose response is directly linked to the step height. Implementation of every designed pixel type on a single wafer can be carried out in order to disambiguate multiple light sources.

Further post-fabrication characterization of the ASPs was planned, however wasn't able to be completed due to limited project time. The first work is to characterize the pixels under the coexistence of ambient light and a coherent light source to mimic the solar radiation in space. Secondly, the characterization of the response under neighbor wavelengths, such as deep red can be completed which would eventually lead to the characterization of the response under multi-wavelength light, i.e. sun light. Furthermore, laser diodes can be employed in the measurement setup to increase measurement accuracy through their smaller bandwidth and very coherent light. Improving the collimation of the incident light is important to be able to correctly identify the accuracy of the angle detection, hence to characterize the device. It would also allow optical measurements in higher angular range which helps determine the FoV of the device.



List of Acronyms

Acronym	Meaning
AlSi	Aluminum with 1% silicon
ASP	Angle-sensitive pixel
APS	Active pixel sensor
BHF	Buffered HF
BiCMOS	Bipolar Complementary Metal-Oxide-Semiconductor
CD	Critical dimention
DRIE	Deep reactive-ion etching
EKL	Else Kooi Laboratory
FOV	Field of view
LED	Light emitting diode
LPCVD	Low-pressure chemical vapour deposition
MAE	Mean Absolute Error
NW	N-well
OPD	Optical path difference
PECVD	Plasma-enhanced chemical vapour deposition
QE	Quantum efficiency
QPD	Quadrature Pixel Cluster
SEM	Scanning Electron Microscope
SN	Shallow n-typed doped region
SP	Shallow p-typed doped region
TiN	Titanium nitrade

B

List of Symbols

Symbol	Meaning
Z_T	Talbot depth
d	Grating pitch
w	Grating width
th	Grating thickness
β	Angular selectivity
α	Phase offset
λ	Wavelength
λ_n	Wavelength in the dielectric material
ϕ	Phase shift due to OPD
V_0	Pixel response, 0°phase offset
V_{14}	Pixel response, $\pi/2$ phase offset
V_{12}	Pixel response, π phase offset
V_{34}	Pixel response, $3\pi/2$ phase offset
3T	3 transistor

C

Simulations

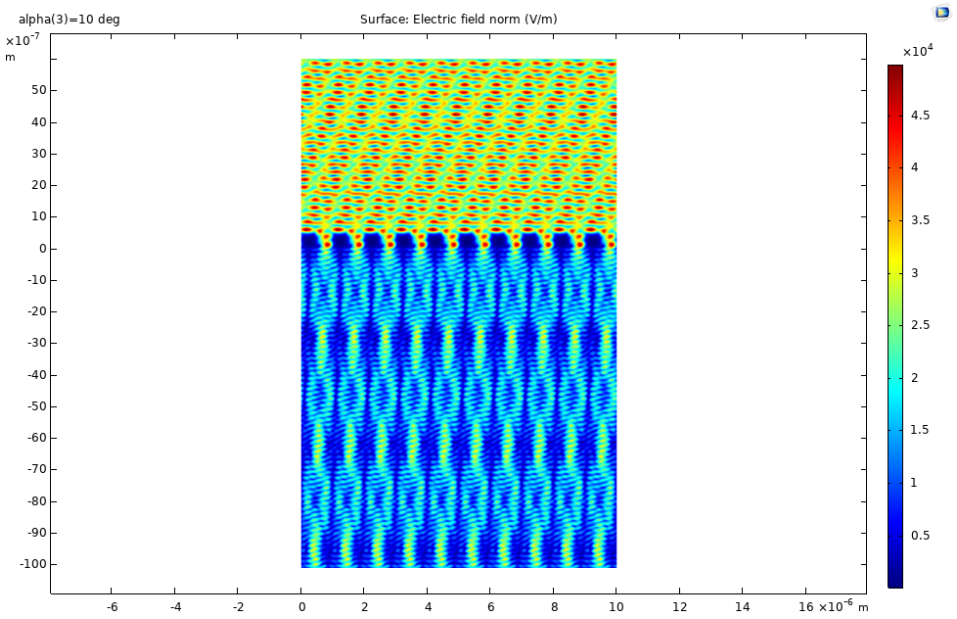


Figure C.1: Talbot self images created by amplitude gratings. Incident angle = 10°, λ = 450 nm. This figure illustrates the vertical shift of the Talbot self-images when illuminated with blue light. Talbot depth moves to 13.3 μm for the same grating structure. This requires the analyser grating to be placed deeper in the oxide material.

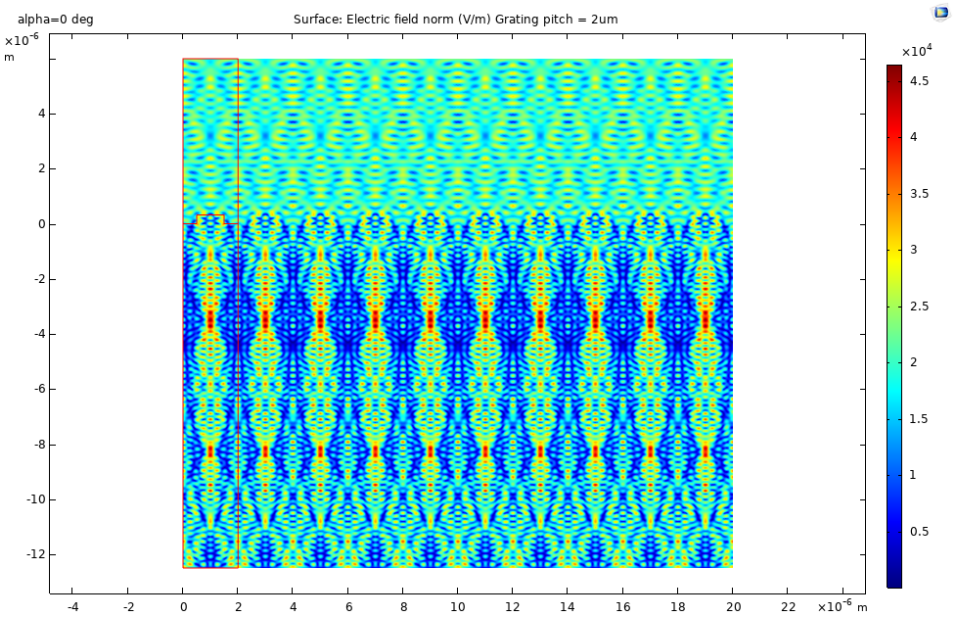
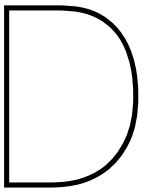


Figure C.2: Talbot self images created by phase gratings.
Strong intensity patterns with the same periodicity as the gratings can also be produced using phase gratings. This figure shows these patterns occurring at $1/4Z_T$ for 2 μm pitch phase gratings with phase step of 107 nm.



Layout

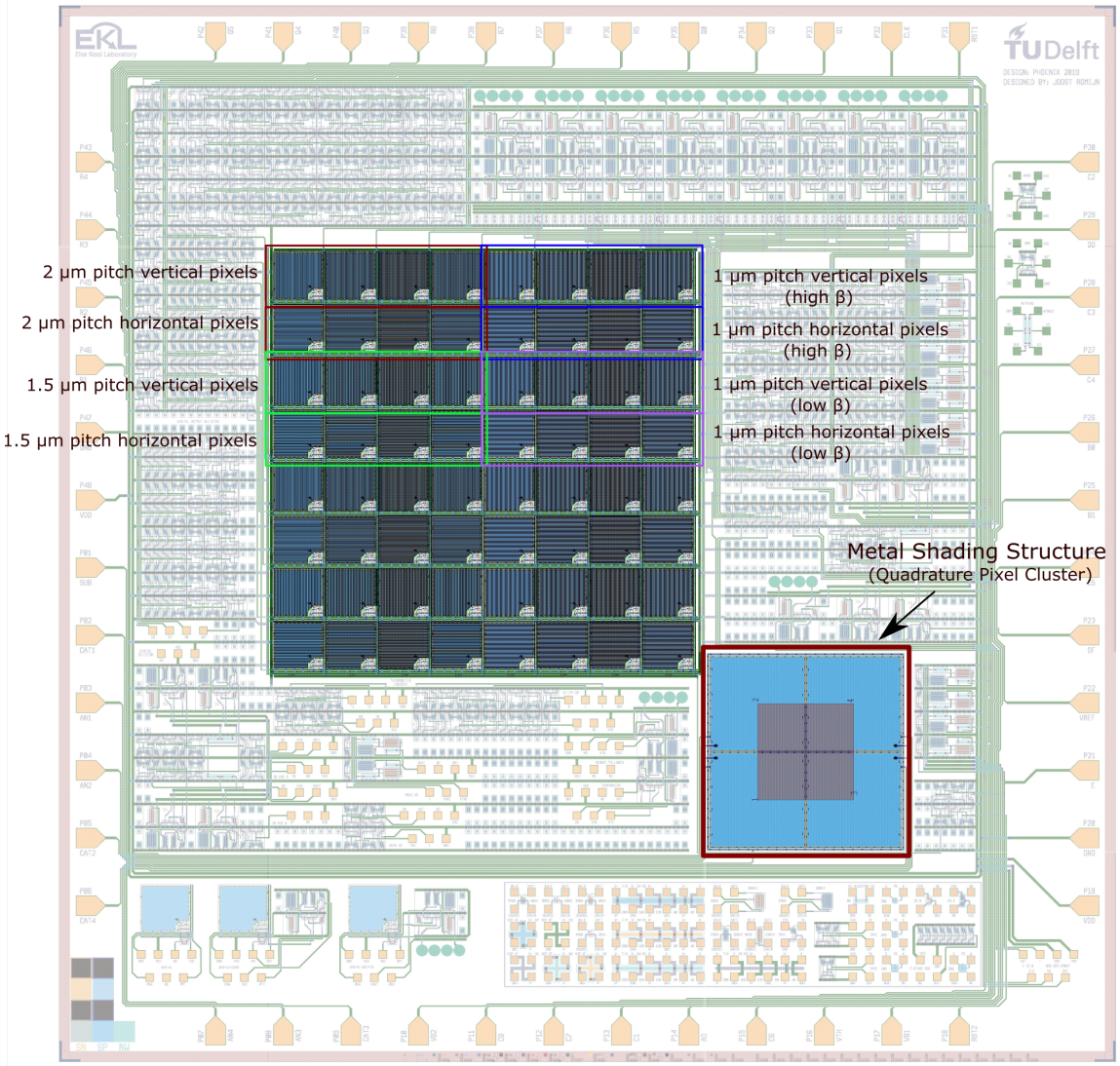


Figure D.1: Complete layout design of Romijn et al. with designed angle-sensitive pixel allocation. Adapted from [6]. ASP pixels are distributed on the existing pixel array design of Romijn et al. 4 different pixel types are employed in the design in order to increase the variations in angle sensitivity. Pixel design on the top half of the array is also copied to the bottom half of the array. Metal shading structure is implemented on the sensor quadrant on the bottom right of the die.

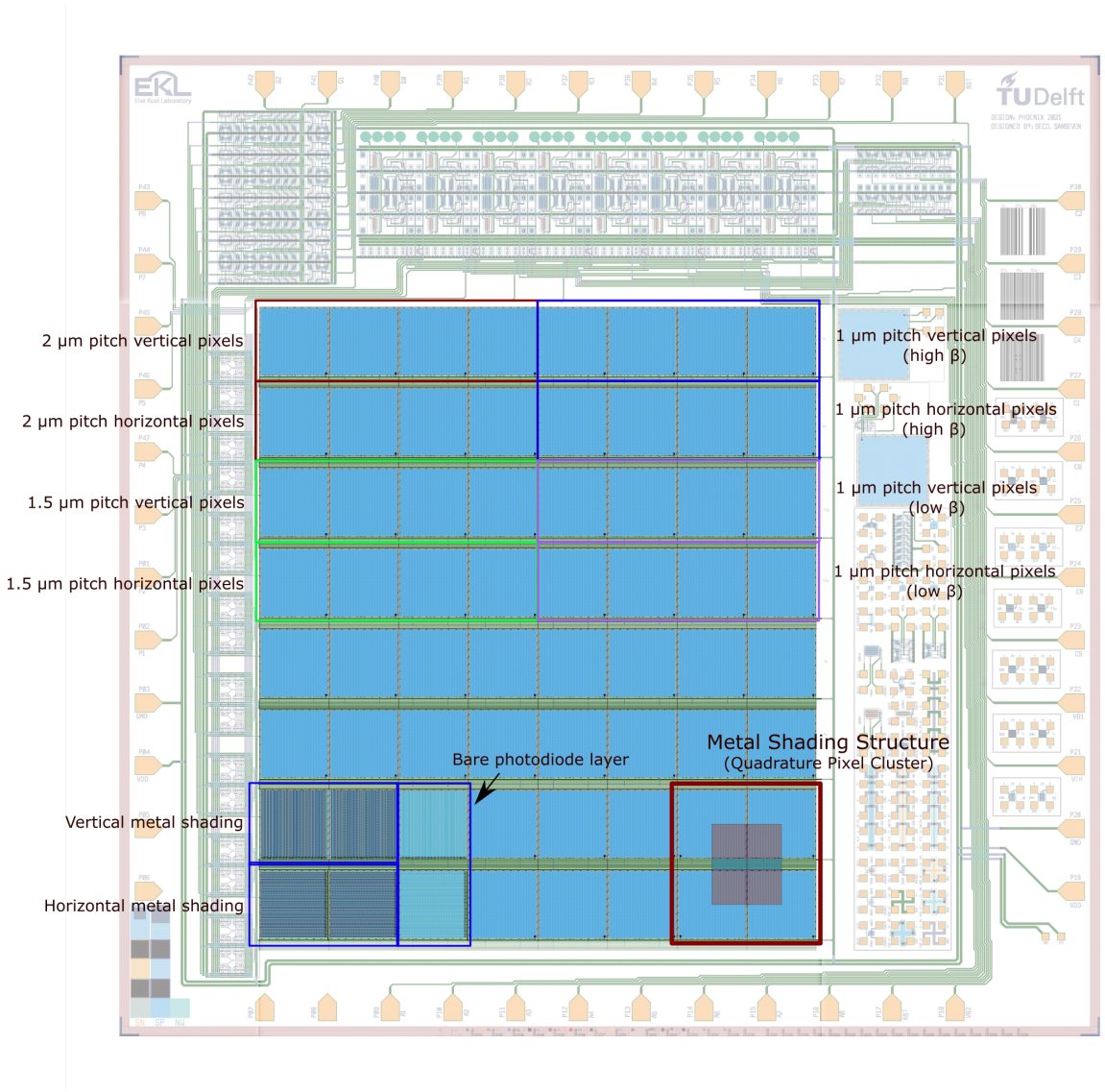


Figure D.2: Complete layout design with designed angle-sensitive pixel allocation. (ASP lines are not shown on the picture due to limited rendering of layout software.)

E

Fabrication

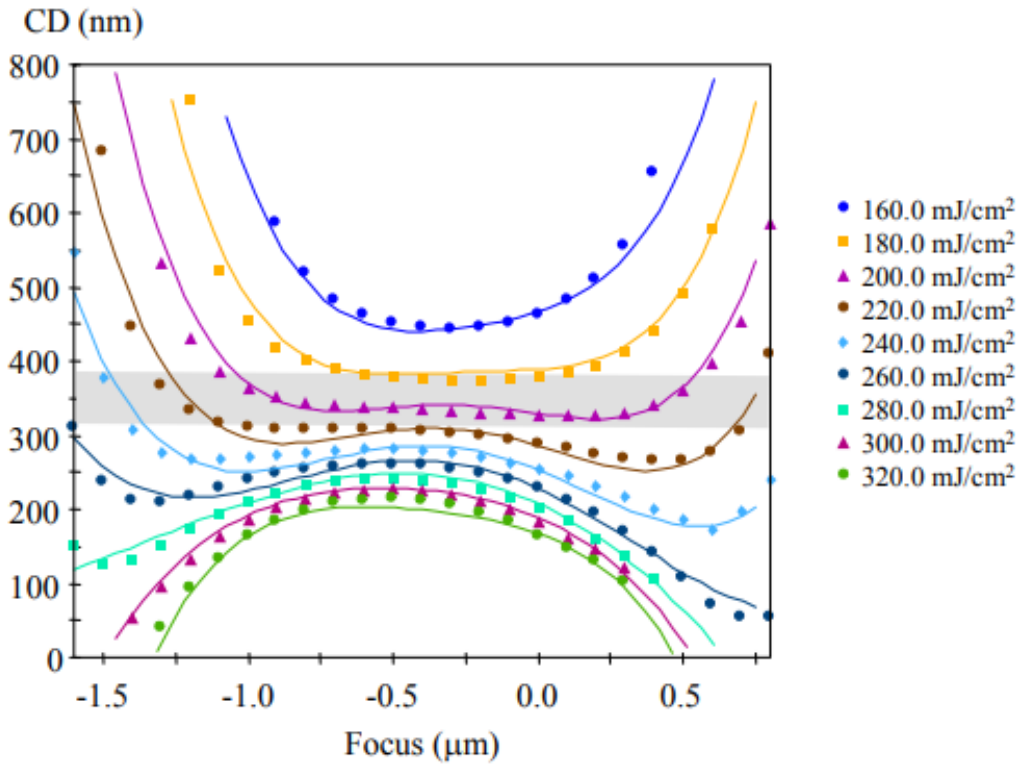


Figure E.1: Bossung plot[34] Bossung plots illustrate the results of energy-focus matrix on the critical linewidths. They are an important tool to understand the effect of exposure energy and focus since there is not a direct and linear relationship between these two parameters and the critical dimensions. We can see from the Bossung plot that increasing exposure energy results in thinner dimensions, however this relationship is not linear but rather logarithmic. Understanding the results of changing focus is more complex, since its effect on CD is closely tied to the exposure energy.

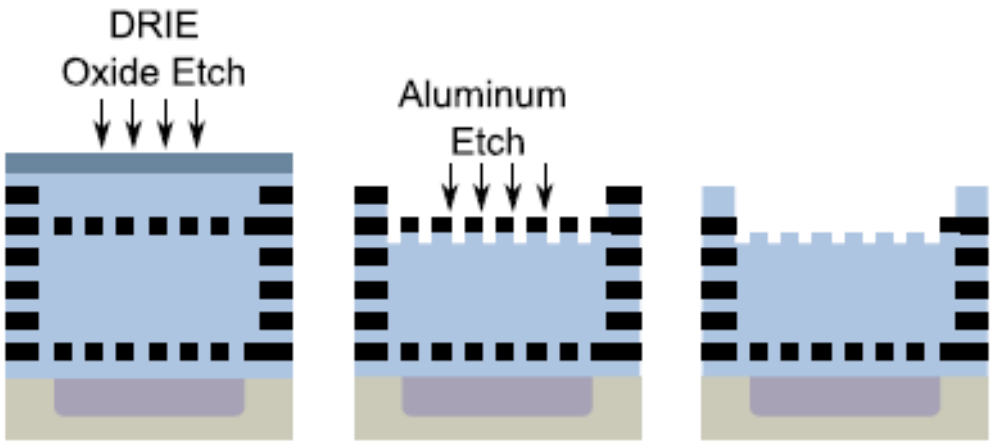
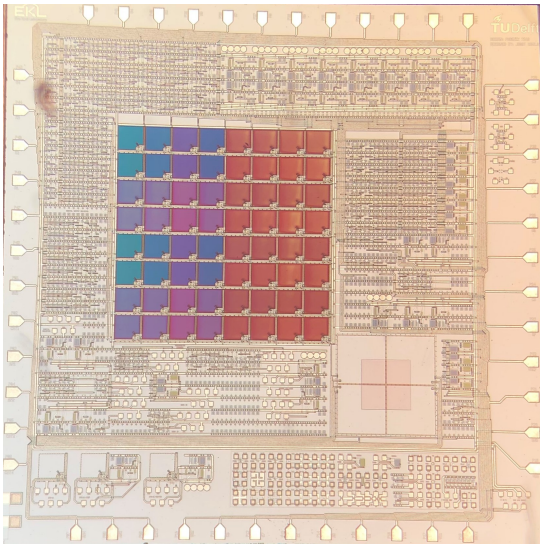
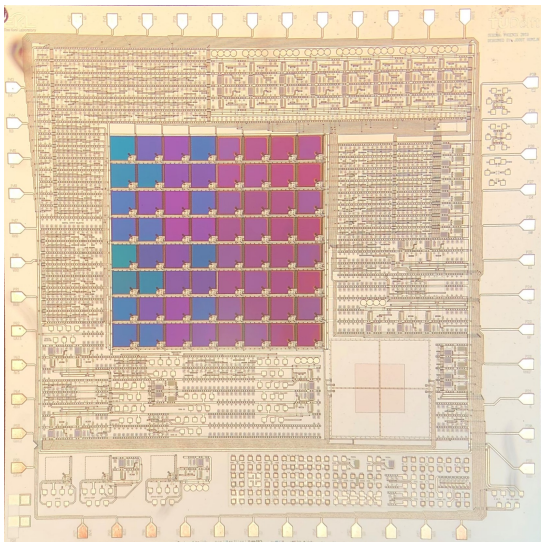


Figure E.2: Post-processing steps to define phase gratings in the work of Sivaramakrishnan et al. [15] After the fabrication of amplitude gratings are completed, post-processing flow is followed to create the phase gratings. 1^{st} step: Wafer surface is covered with a thick layer oxide oxide to protect the bondpad openings and electronic components during the etch process. 2^{nd} step: Deposited oxide is etched with DRIE oxide etching where the top metal gratings act as a mask that define the phase gratings. DRIE process is an anisotropic etch, this helps create the sharp steps that are needed for the phase structure. 3^{rd} step: Metal gratings are removed with etching. [15]

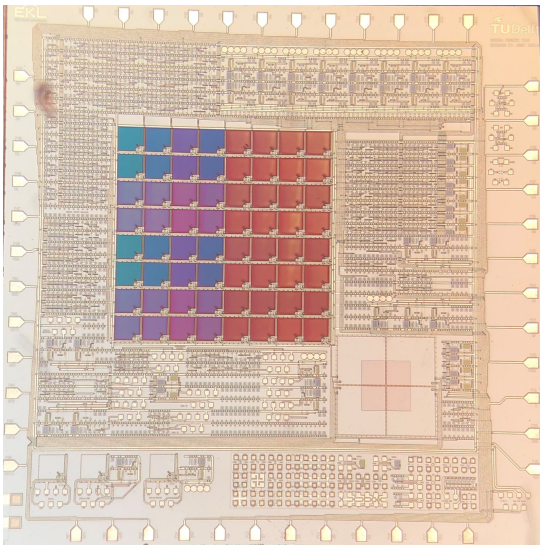


(a) 2 μm pitch wafer centre die

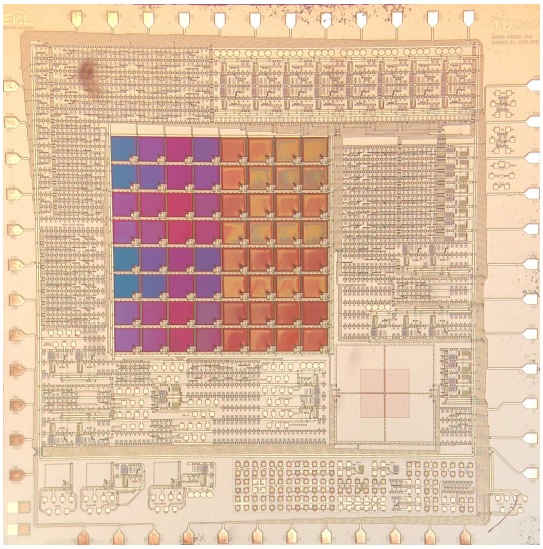


(b) 1 μm pitch wafer centre die

Figure E.3: Comparison of two process wafers (a) Wafer 1 with 2 μm pitch gratings (b) Wafer 3 with 1 μm pitch gratings



(a) 2 μm pitch wafer centre die



(b) 2 μm pitch wafer top rightmost die

Figure E.4: Comparison of two dices on Wafer 1. Effects of photoresist non-uniformity are depicted in this comparison between two pixel arrays on different die locations. It can be observed that linewidth uniformity is seriously damaged for the edge dices, especially in 1 μm pitch gratings where the color varies inside a single pixel. These lines are close to the CD and more inclined to get influenced by the small changes in the resist thickness.

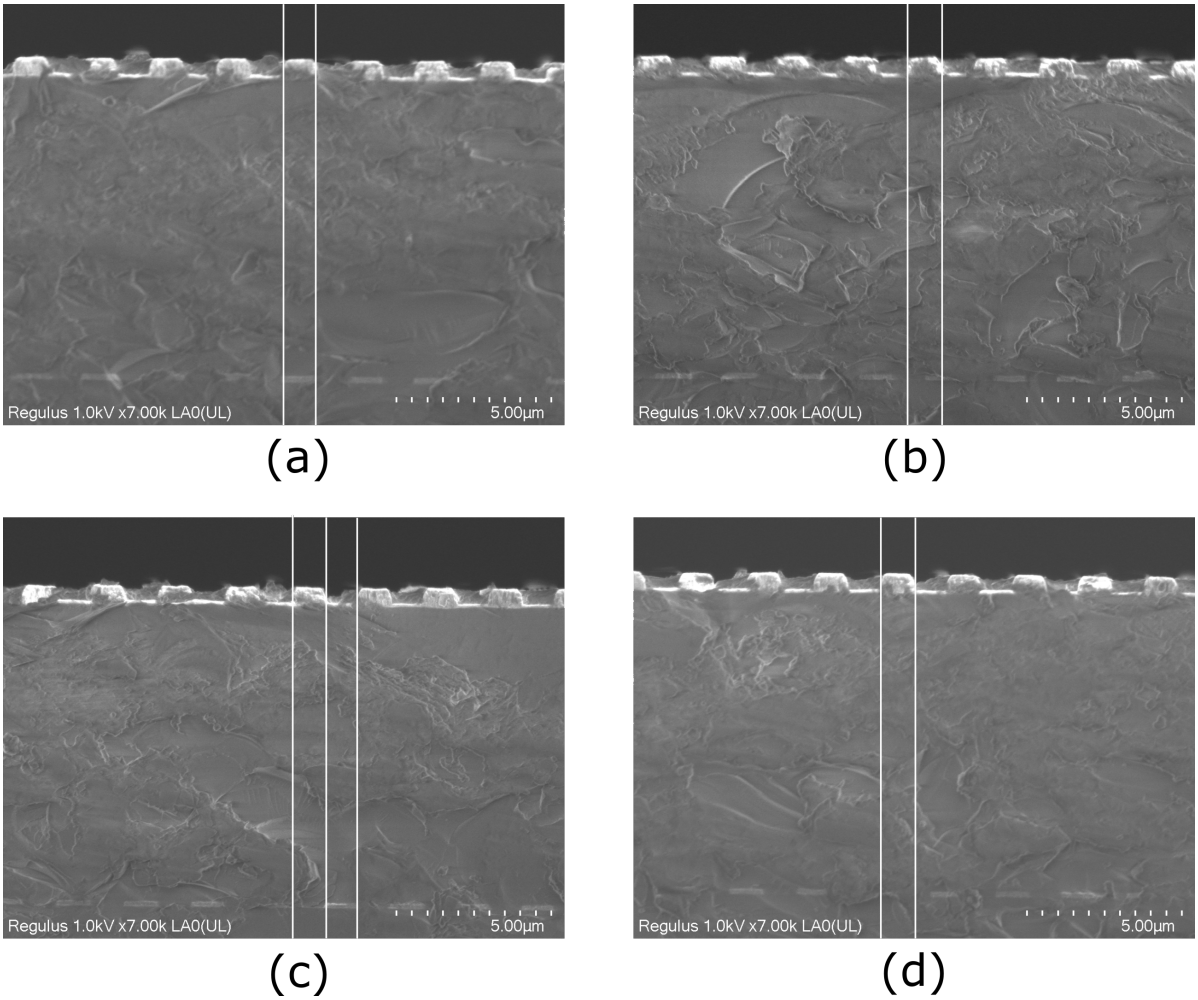


Figure E.5: SEM cross-section images of 4 different pixel offsets. Offsets are accentuated using white vertical lines. (a) 0 offset (b) $\pi/2$ offset (c) π offset (d) $3\pi/2$ offset

F

Process Flow

ZERO LAYER

1. Cleaning. 4 minutes Marangoni cleaning in 0.55% HF.
2. Epitaxial Growth. 2 μm, 1050°C, 60 Torr and the p-type substrate doping; $1x10^{16}\ ions/cm^3$
3. Coating. EVG120, CO-3012-1.4 μm – no EBR.
4. Exposure. COMURK0.0, energy 120, focus 0.
5. Post Exposure Bake.
6. Exposure. FWAMTOZE, energy 120, focus 0.
7. Development. EVG120, DEV-SP.
8. Inspection.
9. Numbering of the wafers
10. Dry etching. Trikon Omega 201, URK_NPD at 20°C.
11. Photoresist strip. Tepla Stripper, program 01.
12. Cleaning. Si cleaning line.

N-WELL DEFINITION

13. Oxidation. Furnace A1, DIBARVAR.
14. Measurement: Oxide thickness, target 20 nm.
15. Coating. EVG120, CO-3027-3.1 μm – no EBR.
16. Exposure. Mask 1, IMAGE 1, energy 420, focus −1.
17. Development. EVG120, DEV-SP.
18. Inspection. Inspect overlay and if correctly developed.
19. Implantation. Ion P^+, energy 150 keV, dose $6x10^{12}\ ions/cm^2$.
20. Resist strip. Tepla Stripper, program 01.
21. Cleaning. Si cleaning line.
22. N-Well Drive-in. Furnace A1, OA002.
23. Measurement: Oxide thickness, target 230 nm.
24. Oxide strip. BHF bath, 3 minutes.
25. Cleaning. Si cleaning line.

SN DEFINITION

26. Oxidation. Furnace A1, DIBARVAR.
27. Measurement: Oxide thickness, target 20 nm.
28. Coating. EVG120, CO-3012-1.4um – no EBR.
29. Exposure. Mask 1, IMAGE 2, energy 120, focus 0.
30. Development. EVG120, DEV-SP.
31. Inspection. Inspect overlay and if correctly developed.
32. Implantation. Ion As^+, energy 40 keV, dose $5x10^{15}\ ions/cm^2$.
33. Resist strip. Tepla Stripper, program 01.
34. Cleaning. Si cleaning line.

SP DEFINITION
35. Coating. EVG120, CO-3012-1.4um – no EBR.
36. Exposure. Mask 1, IMAGE 3, energy 120, focus 0.
37. Development. EVG120, DEV-SP.
38. Inspection. Inspect overlay and if correctly developed.
39. Implantation. Ion B^+, energy 15 keV, dose $5x10^{15}\ ions/cm^2$.
40. Resist strip. Tepla Stripper, program 01.
41. Cleaning. Si cleaning line.

Vt-ADJUST
42. Implantation. Ion B^+ energy 25 keV, dose $9x10^{11}\ ions/cm^2$.
43. Resist strip. Tepla Stripper, program 01.
44. Cleaning. Si cleaning line.
45. Oxide strip. BHF bath.
46. Cleaning. Si cleaning line.

GATE OXIDE GROWTH & CONTACT OPENINGS
47. Thermal oxidation. Furnace C1. ICTOXA.
48. Measurement: Oxide thickness.
49. Coating. EVG120, CO-3027-2.1um – no EBR.
50. Exposure. MASK2, IMAGE 3, energy 315, focus 0.
51. Development. EVG120, DEV-SP.
52. Inspection.
53. Plasma etch. Dry-tek plasma etcher, STDOXIDE, 30 sec.
54. Inspection.
55. Resist strip. Tepla Stripper, program 01.
56. Cleaning. Si cleaning line. Only HNO_3 (99%) bath, no boiling HNO_3.

M1 DEFINITION
56. Marangoni cleaning, 4 mins in 0.55% HF.
57. Metal deposition. Trikon Sigma, AlSi_20nm_350.
58. Coating. EVG120, CO-3027-2.1um – no EBR.
59. Exposure. MASK2 IMAGE 4, energy 340, focus -1.
60. Development. EVG120, DEV-SP.
61. Inspection.
62. Plasma etch. Trikon Omega, Al02_350.
Resist strip. Tepla Stripper, program 01.
63. Cleaning. Metal cleaning line.
64. Electrical measurements. Cascade31.
65. Cleaning. Metal cleaning line.

DIELECTRIC DEFINITION VIAs
66. Oxide deposition. Novellus, xxxxnm_teos, 600 nm TEOS oxide.
67. Measurement: oxide thickness.
68. Coating. EVG120, CO-3027-2.1um – no EBR.
69. Exposure. MASK2 IMAGE 1, energy 315, focus 0.
70. Development. EVG120, DEV-SP.
71. Inspection.
72. Plasma etch. Dry-tek plasma etcher, STDOXIDE, 75 seconds.
Resist strip. Tepla Stripper, program 01.
73. Cleaning. Metal cleaning line.

M2 DEFINITION
74. Metal deposition. Trikon Sigma, AlSi_2075nm_350.
75. Coating. EVG120, CO-3027-2.1um – no EBR.
76. Exposure. MASK2 IMAGE 4, energy 340, focus -1.
77. Development. EVG120, DEV-SP.

78. Inspection.
79. Plasma etch. Trikon Omega, Al20_350.
80. Resist strip. Tepla Stripper, program 01.
81. Aluminum fence removal.
82. Cleaning. Metal cleaning line.

ASP BOTTOM LAYER METAL SHADING DEFINITION
83. Oxide deposition. Novellus, xxxxnm_sio2, 2270 nm oxide.
84. Measurement: oxide thickness.
85. Metal deposition. Trikon Sigma, TiN_100nm_350.
86. Coating. EVG120, Co-Topo-3012-1.4um – no EBR.
87. Exposure. MASK3 IMAGE 2, energy 210, focus 0 for 2 μm pitch.
88. Exposure. MASK3 IMAGE 2, energy 190, focus 0 for 1 μm pitch.
89. Development. EVG120, DEV-SP.
90. Inspection.
91. Plasma etch. Trikon Omega, TiN_NSL, 19 seconds etch, 11 seconds overetch.
92. Resist strip. Tepla Stripper, program 01.
93. Cleaning. Metal cleaning line.

ASP TOP LAYER DEFINITION (Amplitude Gratings)
94. Oxide deposition. Novellus, xxxxnm_sio2, different oxide thicknesses in Table 5.4.
95. Measurement: oxide thickness.
96. Metal deposition. Trikon Sigma, TiN_500nm_350.
97. Coating. EVG120, Co-Topo-3012-1.4um – no EBR.
98. Exposure. MASK3 IMAGE 4, energy 210, focus 0 for 2 μm pitch.
99. Exposure. MASK3 IMAGE 4, energy 190, focus 0 for 1 μm pitch.
100. Development. EVG120, DEV-SP.
101. Inspection.
102. Plasma etch. Trikon Omega, TiN_NSL, 95 seconds etch, 15 seconds overetch.
103. Resist strip. Tepla Stripper, program 01.
104. Cleaning. Metal cleaning line.

ASP TOP LAYER DEFINITION (Phase Gratings)
105. Oxide deposition. Novellus, xxxxnm_sio2, 750 nm oxide
106. Measurement: oxide thickness
107. Coating. EVG120, Co-Topo-3012-1.4um – no EBR.
108. Exposure. MASK3 IMAGE 4, energy 210, focus 0 for 2 μm pitch
109. Development. EVG120, DEV-SP.
110. Inspection.
111. Plasma etch. Dry-tek, STDOXIDE, 60 seconds.
112. Resist strip. Tepla Stripper, program 01.
113. Cleaning. Metal cleaning line.

BONDPAD OPENINGS
114. Coating. EVG120, several PR thicknesses.

Table F.1: Photoresist thicknesses & exposure times for each fabrication wafer. for light intensity of 14.4 mW/cm²

Wafer number	PR thickness	Exposure time*
Wafer 1	6.2 μm	58 sec
Wafer 2	4.6 μm	36.8 sec
Wafer 3	2.3 μm	18.4 sec
Wafer 4	4.6 μm	36.8 sec

115. Exposure. Mask aligner, CA mask8, exposure times given in Table F.1.
116. Development. EVG120, DEV-SP.
117. Inspection.
118. Plasma etch. Dry-tek, OXDSFTLND.
119. Inspection.
120. Cleaning.
121. Metal cleaning line.
122. Electrical measurements. Cascade31-33.

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