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FACULTY OF ELECTRICAL ENGINEERING,  
MATHEMATICS AND COMPUTER SCIENCE

MICROELECTRONICS

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# An Error Feedback Noise-Shaping SAR ADC

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# Abstract

Analog-to-digital converters are important blocks in any electronic system which act as a bridge between analog signals and digital processors. The conventional SAR ADC employs a binary search algorithm and has emerged as the most suitable solution for low-power applications, due to its excellent power efficiency.

The proposed ADC architecture incorporates a new design approach which combines the high resolution capabilities of oversampled ADCs with a 5-bit configuration asynchronous SAR ADC. In this thesis, the theory, analysis and design of a 2<sup>nd</sup> order error feedback noise shaping SAR are addressed. The underlying concept of the error feedback topology is to optimize the location of complex zeros in the noise transfer function and improve the SQNR for a lower sampling frequency.

The stringent power and area budget imposes challenges in designing active blocks with a low transistor count. The impact of a new switching scheme for the capacitive DAC is examined analytically while considering the trade-off between linearity and power savings. The design uses a small assisting SAR and reaches 96% improvement in power consumption due to switching when comparing to a conventional scheme.

The converter operates at 1 MHz and consumes 11  $\mu$ W, from a 1.8 V supply. In a bandwidth of 20 kHz and an OSR of 25, it achieves an SNDR of 71 dB, an ENOB of 11.5 bits and a Walden FOM of 98 fJ/conversion-step.



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# Contents

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<b>1</b>	<b>Introduction</b>	<b>10</b>
1.1	SAR vs. Sigma Delta Converters . . . . .	10
1.2	ADC Survey - Energy efficiency vs. Resolution . . . . .	15
1.3	Motivation . . . . .	18
1.4	Thesis Organization . . . . .	19
<b>2</b>	<b>High-Resolution Hybrid ADCs</b>	<b>20</b>
2.1	Subranging ADCs . . . . .	20
2.2	Nonlinearity Effects in a Two-step ADC . . . . .	22
2.3	System Requirements . . . . .	24
<b>3</b>	<b>Noise Shaping SAR Techniques</b>	<b>28</b>
3.1	Noise Shaping SAR ADCs . . . . .	28
3.2	Feedforward Topology . . . . .	30
3.3	First Order Error Feedback Noise Shaping SAR . . . . .	35
3.4	Second Order Error Feedback Noise Shaping SAR . . . . .	38
<b>4</b>	<b>Design of an Error Feedback Noise Shaping SAR</b>	<b>41</b>
4.1	Sampling Technique Considerations . . . . .	41
4.2	Error Feedback Basic Operation . . . . .	43
4.3	Implementation of a First Order Error Feedback Architecture . . . . .	44
4.4	Implementation of a Second Order Error Feedback Architecture . . . . .	51
4.5	OTA Static and Dynamic errors . . . . .	53
4.6	Noise Limitations . . . . .	61
<b>5</b>	<b>Design of an Energy Efficient 2<sup>nd</sup> order Error Feedback Noise Shaping SAR</b>	<b>65</b>
5.1	Energy Consumption for CDACs . . . . .	65
5.2	Aligned Switching . . . . .	66



5.3	Detect and Skip Switching . . . . .	67
5.4	Decoding Algorithm for MSB decisions . . . . .	70
<b>6</b>	<b>Simulation Results</b>	<b>73</b>
6.1	Power Savings . . . . .	73
6.2	CDAC Linearity . . . . .	74
6.3	2 <sup>nd</sup> Order NSSAR Dynamic Performance . . . . .	80
<b>7</b>	<b>Conclusions</b>	<b>81</b>
7.1	Benchmarking . . . . .	81
7.2	Original Contributions . . . . .	84
7.3	Future Work . . . . .	86

## List of Figures

---

1.1	Resolution vs. sampling frequency . . . . .	11
1.2	SAR ADC architecture . . . . .	12
1.3	$\Sigma\Delta$ modulator linear model . . . . .	13
1.4	ADC techniques: Nyquist vs. Oversampling vs. Noise Shaping . . . . .	14
1.5	Performance overview of ADC architectures . . . . .	16
2.1	Single Step ADC vs two step subranging ADC . . . . .	20
2.2	Two step subranging ADC . . . . .	21
2.3	Hybrid subranging ADC with fine stage nonlinearity . . . . .	23
2.4	SNDR vs. input signal amplitude sweep for a nonlinear fine ADC . . . . .	25
2.5	Hybrid Subranging ADC with filtered frontend - Spectrum of Coarse ADC output (top), Residue (middle), Hybrid ADC (bottom) . . . . .	27
3.1	Timing diagram for 5 bit SAR ADC . . . . .	28
3.2	Noise Shaping SAR SNDR vs. $f_{nyq}$ vs. Area . . . . .	29
3.3	Feedforward architecture . . . . .	30
3.4	Feedforward NSSAR loopfilter implementations . . . . .	31
3.5	Feedforward NSSAR NTF and Pole-zero map . . . . .	32
3.6	First order error feedback NSSAR diagram . . . . .	35
3.7	Non-idealities of error feedback NSSAR . . . . .	36
3.8	Finite gain effects for first order EF NSSAR . . . . .	37
3.9	Second order error feedback NSSAR diagram . . . . .	39
3.10	Finite gain effects for second order EF NSSAR . . . . .	40
4.1	SAR ADC top and bottom plate sampling . . . . .	41
4.2	Bottom plate sampling based residue subtraction . . . . .	43

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4.3	First order error feedback NSSAR operating modes and timing	45
4.4	Error Feedback NSSAR OTA configurations	46
4.5	1st order Error Feedback NSSAR Gain error effects	48
4.6	Interleaved residue capacitors	50
4.7	2 <sup>nd</sup> order Error Feedback NSSAR Operating modes and timing	52
4.8	OTA parasitic capacitance	53
4.9	OTA finite gain and finite transconductance	54
4.10	OTA Bode diagram and settling operation	55
4.11	Current reuse OTA schematic	56
4.12	Constant gm biasing	57
4.13	OTA Cadence corner simulations	59
4.14	Switched capacitor common mode feedback	60
4.15	Sampling mode noise	61
4.16	Noise limitation due to the residue capacitor	62
4.17	Comparison of 1 <sup>st</sup> order and 2 <sup>nd</sup> order NSSAR - thermal noise SNR vs. quantization noise SQNR	63
5.1	Capacitive switching energy consumption	65
5.2	Aligned switching basic principle	67
5.3	Energy efficient SAR implementation	68
5.4	Aligned switching based on small SAR	69
5.5	Decoding algorithm	71
5.6	Timing diagram of decoding scheme	72
5.7	Domino Logic and Bit Slice Unit	72
6.1	SAR energy consumption for different switching schemes	73
6.2	Energy efficiency comparison for different configurations of SAR capacitive arrays	74
6.3	Static linearity effects	75
6.4	Monte Carlo simulation for unit capacitor	76
6.5	Transfer function linearity	76
6.6	Conventional Scheme INL and DNL - 10 bit (left) and 5 bit (right)	77
6.7	Implemented Scheme INL and DNL - 10 bit (left) and 5 bit (right)	78

6.8	Comparison of schemes - dynamic linearity . . . . .	79
6.9	Histogram and FFT for Cadence Monte Carlo simulation . . . . .	79
6.10	Design limits of OTA . . . . .	80
7.1	Power budgeting comparison pie chart Fs 1MHz . . . . .	81
7.2	Figures of merit vs. sampling frequency . . . . .	83
7.3	Figures of Merit [1] . . . . .	85

## List of Tables

---

2.1	ADC requirements . . . . .	26
3.1	Comparison of state-of-the-art NSSARs . . . . .	29
4.1	OTA Performance across corners . . . . .	58
7.1	Comparison with state of the art . . . . .	82



## Chapter 1 Introduction

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Analog to Digital Converters (ADCs) are essential building blocks for a vast range of IC applications as they are used in almost any electronic equipment. Man's ultimate dream of enabling a smart environment is possible due to the advancements in Internet of Things technology. Current research investigates compact circuit designs suitable for sensors that are powered by batteries with limited storage capability while enduring long time operation under stressful conditions such as low/high temperature or external interference. This trade-off between area minimization, energy efficiency and robustness requires a careful investigation of suitable ADC architectures that can deal with signals in noisy environments and can convert signals with different bandwidths. Therefore, performance indicators such as speed and resolution must meet requirements of modern applications.

### 1.1 SAR vs. Sigma Delta Converters

ADCs will always benefit from process scaling in deep submicron CMOS, resulting in increased interest in finding architectures with the potential to achieve power efficiency and high resolution. The Successive Approximation Register (SAR) ADC is suitable for high power efficiency and medium speed, whereas the Sigma Delta modulator achieves high dynamic range and high resolution at the expense of speed. The main operation of these two architectures will be briefly introduced in this section. The general domains of operation of these ADCs are illustrated in Figure 1.1.

Although a Nyquist rate SAR ADC could achieve high resolution similar to a Sigma Delta ADC, there is a penalty in power and area in order to mitigate some of the inherent limitations of the architecture such as thermal noise and mismatch [2][3].

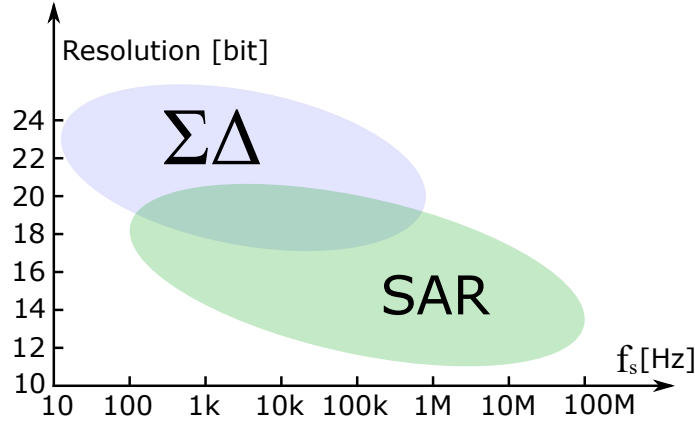


Figure 1.1: Resolution vs. sampling frequency

The main operation of a SAR ADC is based on a binary search algorithm, where  $N$  bits are computed in  $N$  cycles. As shown in Figure 1.2, a binary weighted capacitive array samples the input and converts the signal into the digital domain by gradually switching the capacitors to the references. The register holds the digital value of each comparison between the two input terminals of the comparator. Due to the successive operation required for approximating the input, the inherent advantage of using a single comparator results in a trade-off for latency. After a revival of the SAR topology due to the advance of the CMOS technology, several techniques such as bottom plate sampling, bootstrapping and asynchronous logic have been implemented in order to enhance the linearity and the speed of the design [2][3][4][5].

Figure 1.3 illustrates the linearized model of a single-loop Sigma Delta ADC [3][6]. The output of the  $L^{\text{th}}$  order modulator (where  $L$  is the order of the loop filter),  $Y(z)$ , can be described as:

$$Y(z) = X(z) \cdot \frac{H(z)}{1 + H(z)} + E(z) \cdot \frac{1}{1 + H(z)} \quad (1.1)$$

$$Y(z) = X(z) \cdot z^{-k} + E(z) \cdot (1 - z^{-1})^L \quad (1.2)$$

where  $X(z)$  is the input,  $H(z)$  is the loopfilter transfer function and  $E(z)$  is the quantization error.

The noise transfer function (NTF) and signal transfer function (STF)



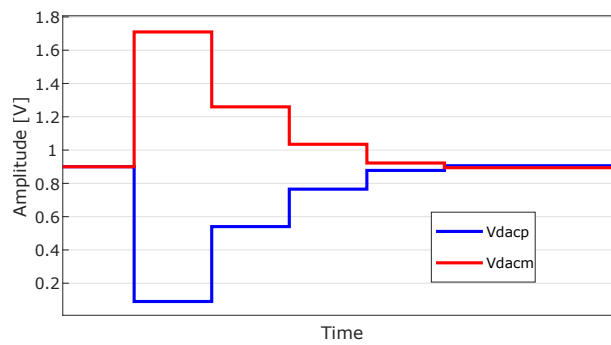
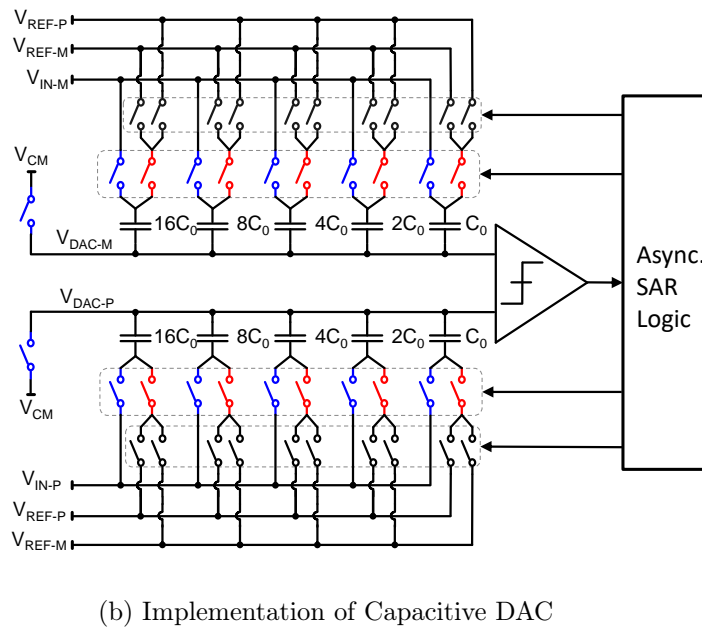
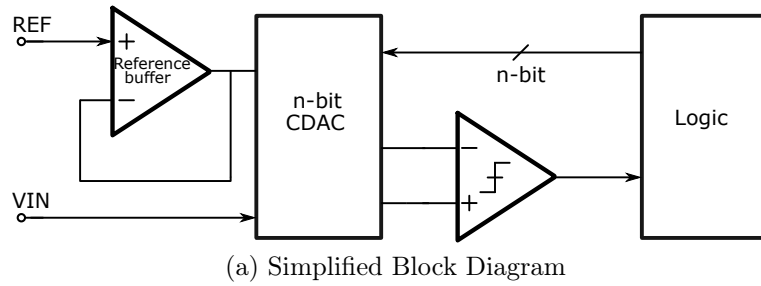
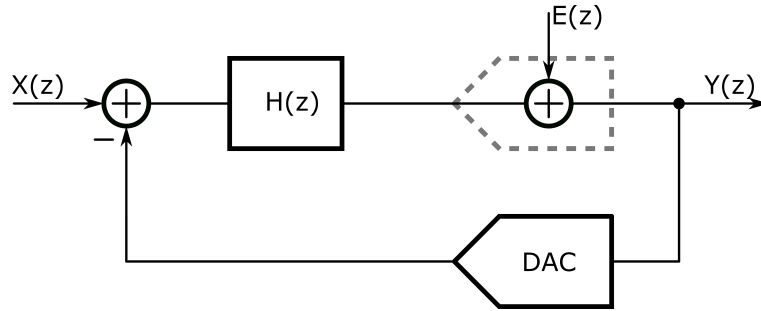


Figure 1.2: SAR ADC architecture

Figure 1.3:  $\Sigma\Delta$  modulator linear model

describe, respectively, the spectral shaping of the quantization error and the transfer function of the input signal:

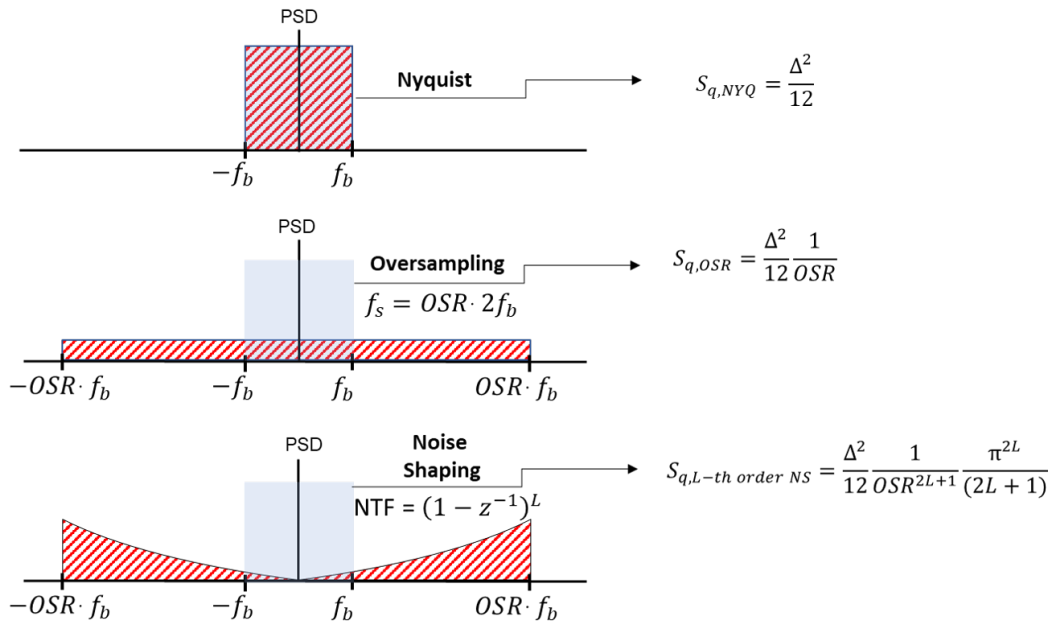
$$NTF(z) = \frac{1}{1 + H(z)} = (1 - z^{-1})^L \quad (1.3)$$

$$STF(z) = \frac{H(z)}{1 + H(z)} = z^{-k} \quad (1.4)$$

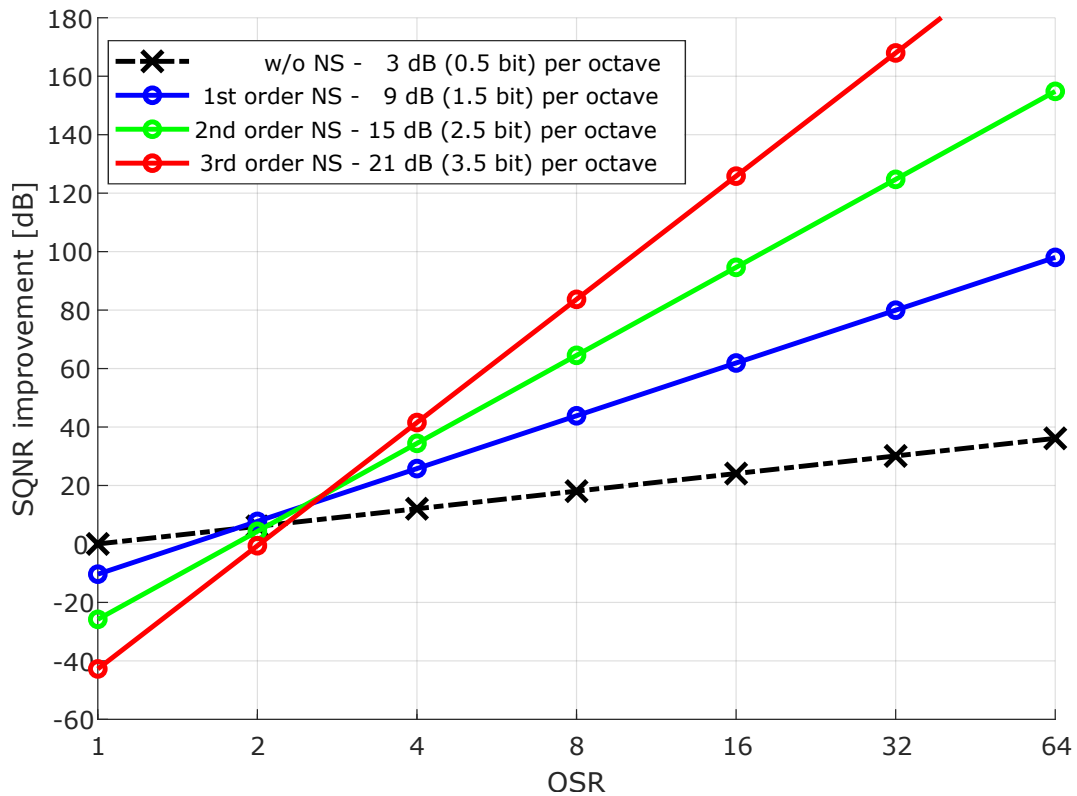
By pushing the quantization noise power outside of the band of interest (Figure 1.4 (a)), especially when a higher order loop filter is used for noise shaping, a much higher SQNR (Signal to Quantization Noise Ratio) can be obtained as opposed to simple oversampling (Figure 1.4 (b)). However, for the case of a higher order NTF, the out-of-band gain increases rapidly, leading to an overload of the quantizer and resulting in instability [3]. This effect can be reduced by using a multi-bit quantizer instead of a single-bit; nevertheless, a multi-bit quantizer comes in pair with a multi-bit feedback DAC which limits the accuracy of the overall modulator.

The interesting fact to keep in mind is the inherent capacitive DAC found in most SAR architectures. By merging the input sample and hold with the feedback DAC of a classic closed loop ADC, the SAR ADC seems to be a good candidate for minimizing the required area and satisfying the noise/matching requirements. A significant improvement can be achieved by implementing a hybrid architecture which combines the power efficiency of the SAR and the benefits of noise shaping and oversampling while trying to minimize the number of opamps and multi-bit DACs that increase power consumption and area [5].

## 1.1. SAR vs. Sigma Delta Converters



(a) Inband quantization noise Power Spectral Density [3]



(b) SQNR improvement vs. OSR

Figure 1.4: ADC techniques: Nyquist vs. Oversampling vs. Noise Shaping

## 1.2 ADC Survey - Energy efficiency vs. Resolution

In order to have a better overview of the different architectures, Figure 1.5 illustrates Nyquist and Oversampled Data Converters, while taking into account only state of the art publications with an area lower than  $0.25\text{mm}^2$  [1]. The size of the bubbles are proportional to the area of the ADCs.

The SNDR (Signal to Noise and Distortion Ratio) of an ADC is defined as:

$$SNDR = \frac{\text{Signal Power}}{\text{Noise and Distortion Power}} \quad (1.5)$$

Using the SNDR calculations, the ENOB (effective number of bits) can be calculated as:

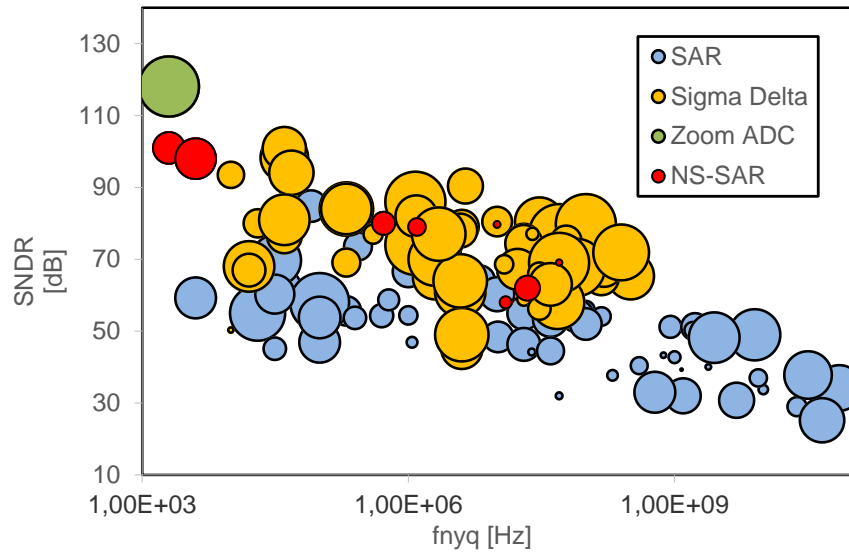
$$ENOB = \frac{SNDR(dB) - 1.76dB}{6.02dB} \quad (1.6)$$

Figure 1.5(a) shows the  $SNDR$  as a function of  $f_{nyq}$  (Nyquist frequency). Due to the inherent linearity of a Sigma Delta Modulator with a 1-bit quantizer or due to the use of DEM (dynamic element matching) for the feedback DAC associated with a multi-bit quantizer, Sigma Delta ADCs are still dominant in terms of resolution and linearity in comparison to SAR ADCs. However, the downside of Sigma Delta architectures is the bandwidth limitation and the power efficiency as illustrated in Figure 1.5. The main limitation comes from limited UGBW of amplifiers and finite time constants of latches.

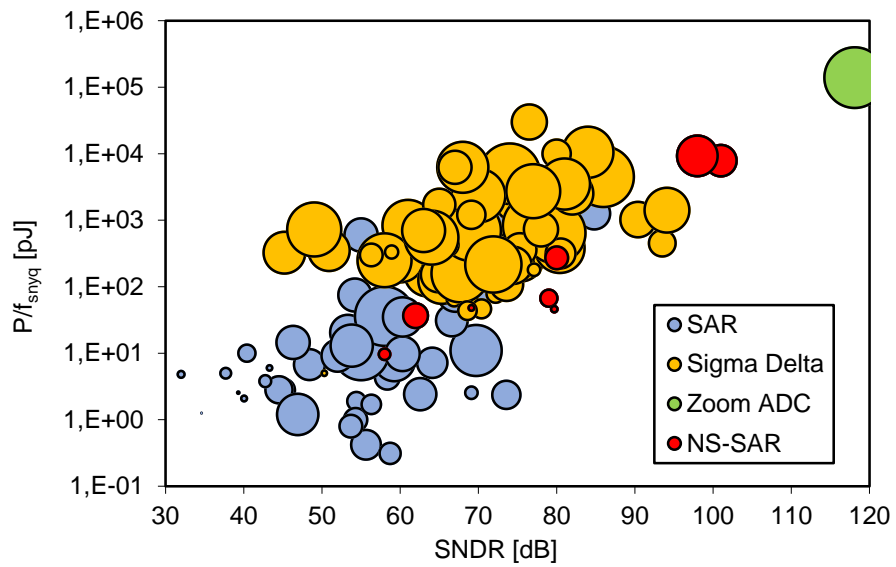
On the other hand, SAR ADCs challenge flash ADCs in terms of speed by using techniques such as asynchronous operation and time interleaving [4] [5]. Furthermore, technology scaling enables low power digital calibration, relaxing matching requirements. This results in a scaling down of the CDAC to the  $kT/C$  limit and a higher bandwidth due to less stringent settling requirements.

In terms of energy efficiency (Figure 1.5(b)), the SAR ADC is a viable

## 1.2. ADC Survey - Energy efficiency vs. Resolution



(a) Resolution vs Nyquist frequency



(b) Energy efficiency vs. SNDR

Figure 1.5: Performance overview of ADC architectures

solution because it consumes only dynamic power and there is no need for an operational amplifier. The comparator is still a significant limitation for this architecture since the noise and metastability of this circuit during LSB decisions can result in a degraded performance of the ADC. Several measures have been proposed to mitigate these issues: duplication of the LSB decision, using a low power comparator for MSB decisions and a low noise comparator for LSB decisions or determining the result based on a repetition of the comparison (0 or 1 are identified by majority voting) [5].

## 1.3 Motivation

The Noise Shaping SAR (NSSAR) is currently an interesting topic in data converter research since it combines the merits of both SAR and Sigma Delta ADCs. Therefore, by using oversampling and noise shaping techniques, NSSARs enable a reduction in power and area required for achieving similar SQNR as a conventional Nyquist SAR ADC. For example, an NSSAR does not require a low noise comparator in order to take the fine decisions, therefore improving power efficiency.

Moreover, by applying the noise shaping technique, the capacitive DAC does not require the same configuration of binary elements as a conventional SAR and enables a scaling down of the capacitor array by simply eliminating the MSB elements. The red bubbles in Figure 1.5 illustrate that NSSARs can be very efficient in both ways: energy efficiency and resolution.

In Figure 1.5, the green bubble corresponds to a hybrid architecture such as the Zoom ADC [7] which can achieve more than 110 dB SNDR with good power efficiency and low area. The Zoom ADC uses a sub-ranging technique that combines a 5-bit asynchronous SAR based coarse stage with a high-resolution Sigma Delta based fine quantizer.

The motivation for this thesis is to investigate a low area and power efficient Noise Shaping SAR ADC which can replace the conventional SAR ADC as a coarse quantizer and therefore alleviate the linearity requirements of the fine stage. Noise shaping in the front end can act as a sort of dithering by randomizing the residue applied to a non-ideal fine quantizer and therefore reducing the effect of inaccuracies such as incomplete settling, opamp finite gain or a nonlinear transfer function due to mismatch. This work aims to provide a stand-alone circuit design for a NSSAR which can, therefore, be used in enhancing the overall linearity of a sub-ranging architecture such as the Zoom ADC.

## 1.4 Thesis Organization

The thesis is structured as follows:

**Chapter 2** presents the operating principles of two-step subranging ADCs such as the Zoom ADC and analyzes the system's linearity requirements. It is shown that a 5-bit 2<sup>nd</sup> order Noise Shaping SAR is the most suitable option for boosting the performance and reducing the overhead of the fine quantizer.

**Chapter 3** deals with the literature review of previous published Noise Shaping SAR implementations. Matlab simulations are used to verify the trade-offs of two main approaches for NSSAR design: feedforward and error feedback. Lastly, a system-level analysis of the proposed 1<sup>st</sup> order and 2<sup>nd</sup> order Error Feedback architecture is presented.

**Chapter 4** aims to gradually present the circuit design of the Error Feedback NSSAR. The 1<sup>st</sup> order and 2<sup>nd</sup> order NSSAR circuit implementation details are discussed while motivating the design choices for the amplifier and the biasing.

**Chapter 5** investigates a new switching scheme in order to reduce the power consumption of the NSSAR. This chapter shows the schematic and the implementation details of the 2<sup>nd</sup> order Noise Shaping SAR with detect and skip switching.

**Chapter 6** provides the simulation results for the implemented design with emphasize on the switching scheme's energy efficiency and linearity. Design trade-offs are presented for different configurations of capacitive DACs and biasing conditions for the amplifier.

**Chapter 7** illustrates the conclusions and shows the performance of this design compared with state of the art ADCs.



## Chapter 2 High-Resolution Hybrid ADCs

### 2.1 Subranging ADCs

Subranging was initially implemented as a countermeasure for the exponentially increasing number of comparators required for a high-resolution flash ADC[2]. The main idea is to divide the conversion into 2 steps: coarse and fine. This results in a division of the input range into multiple subranges as shown in Figure 2.1. The Coarse ADC decision is used by the coarse DAC (Figure 2.2 (a)) in order to shift the signal into the input range of the fine ADC.

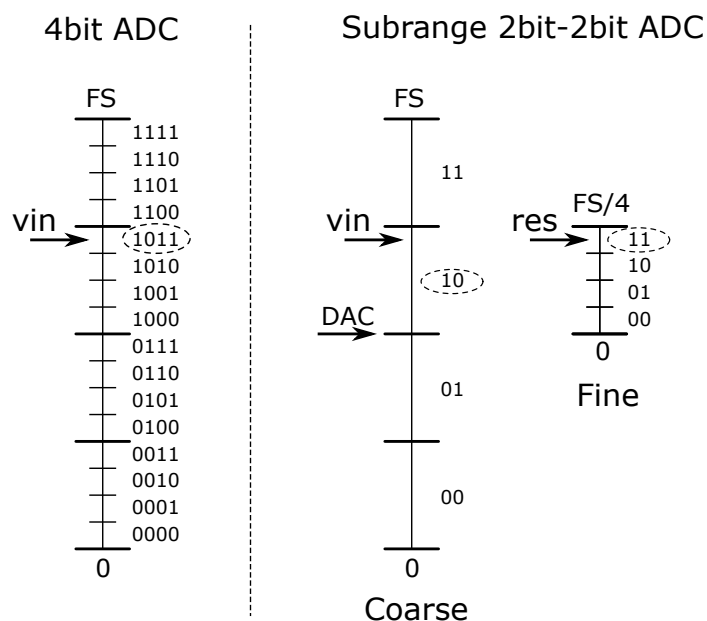


Figure 2.1: Single Step ADC vs two step subranging ADC

Figure 2.2 (b) shows that a Two-Step Subranging architecture enables a specialization of the front-end and back-end stages for different purposes

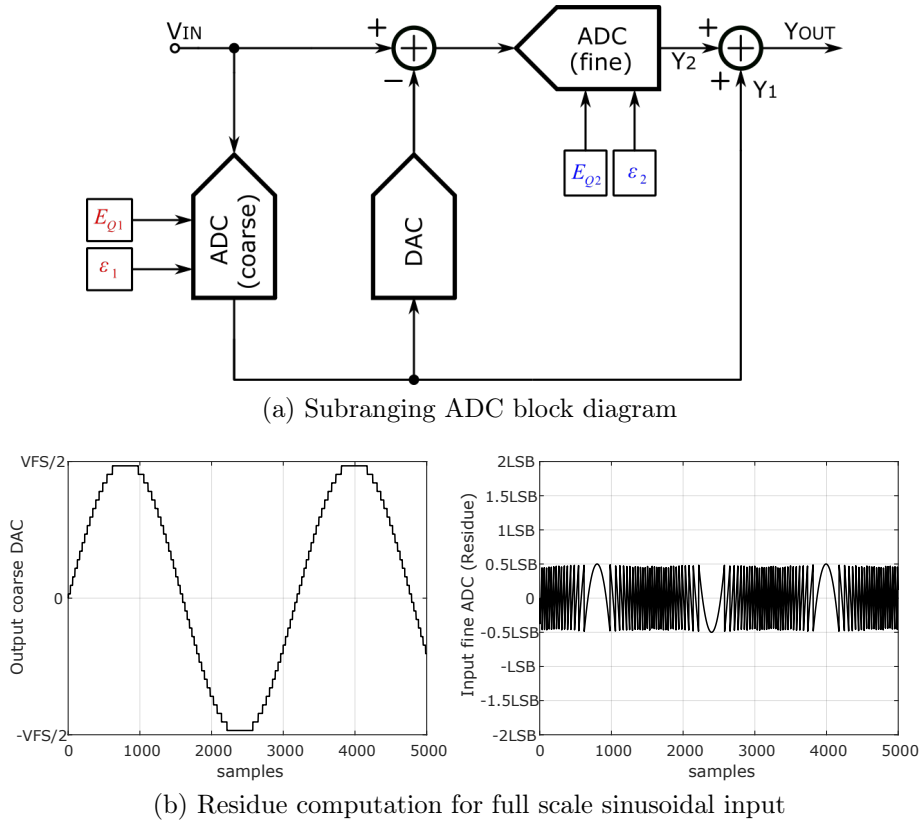


Figure 2.2: Two step subranging ADC

and signal handling capabilities [2]. The two stages can decouple large signal requirements (e.g. slew rate) from small signal requirements (e.g. thermal noise) by using a low-resolution coarse quantizer (with high input range - covering the full-scale range) and a high-resolution fine quantizer (with lower input range - covering the swing of the quantization error of the coarse stage between  $-0.5$  LSB and  $0.5$  LSB). This shows that a trade-off between the resolution of the coarse and fine stages must be assessed in order to achieve optimum performance: a lower number of bits for the coarse quantizer implies a larger amplitude residue and therefore limitations due to the fine quantizer linearity, whereas a higher number of bits in the coarse stage can result in a relaxation of the fine quantizer requirements, but with a compromise in area and power for the coarse stage.

Assuming that  $\varepsilon_1$  and  $\varepsilon_2$  from Figure 2.2 (a) are non-idealities introduced

by the coarse and fine stage, while  $E_{Q1}$  and  $E_{Q2}$  are the quantization errors, it can be shown that for a given noise transfer function of the coarse stage ( $NTF_1$ ) and the fine stage ( $NTF_2$ ), the output can be calculated as following:

$$Y_1 = V_{IN} + E_{Q1} \cdot NTF_1 + \varepsilon_1 \quad (2.1)$$

$$Y_2 = -(E_{Q1} \cdot NTF_1 + \varepsilon_1) + E_{Q2} \cdot NTF_2 + \varepsilon_2 \quad (2.2)$$

$$Y_{OUT} = V_{IN} + E_{Q2} \cdot NTF_2 + \varepsilon_2 \quad (2.3)$$

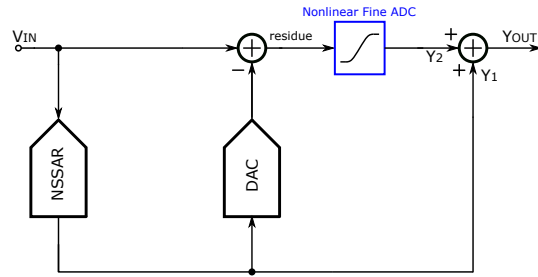
The previous calculation assumed that an ideal DAC is used, which is not the case. However, in order to deal with the DAC mismatch, techniques such as dynamic element matching can be applied to take advantage of the technology scaling and the benefit of reduced power consumption necessary for digital computations.

## 2.2 Nonlinearity Effects in a Two-step ADC

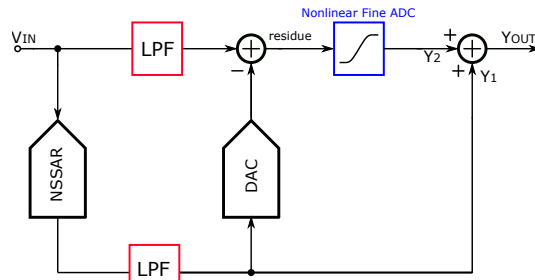
As long as the coarse ADC nonlinearity does not cause significant deviations so that the residue is outside the input range of the fine ADC (which can be solved by over-ranging as in the case of the Zoom ADC [7]), the sub-ranging architecture will shift the design limitations to the resolution and linearity of the fine quantizer.

Figure 2.3(a) illustrates the block diagram of a two-step ADC which has an NSSAR based coarse stage. In order to analyze the impact of the addition of a noise shaped coarse quantizer on the overall hybrid system, Matlab simulations are carried out using an ideal fine quantizer combined with a hyperbolic tangent nonlinearity which will directly distort the residue. It has been proven in [8] that for the case of an oversampled two-stage ADC with noise shaping in the front-end it is necessary to add a low pass filter (LPF in Figure 2.3(b)) on both the digital path and analog path. The purpose of this LPF is to reduce the differentiated out-of-band quantization noise and counteract any overloading of the fine quantizer due to this increase in rms quantization power.

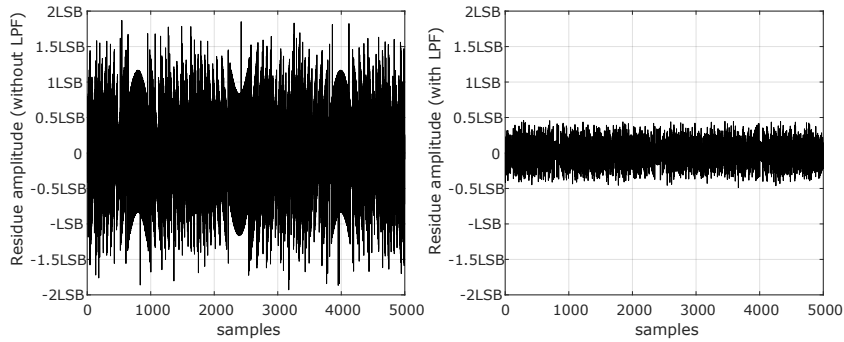
## 2.2. Nonlinearity Effects in a Two-step ADC



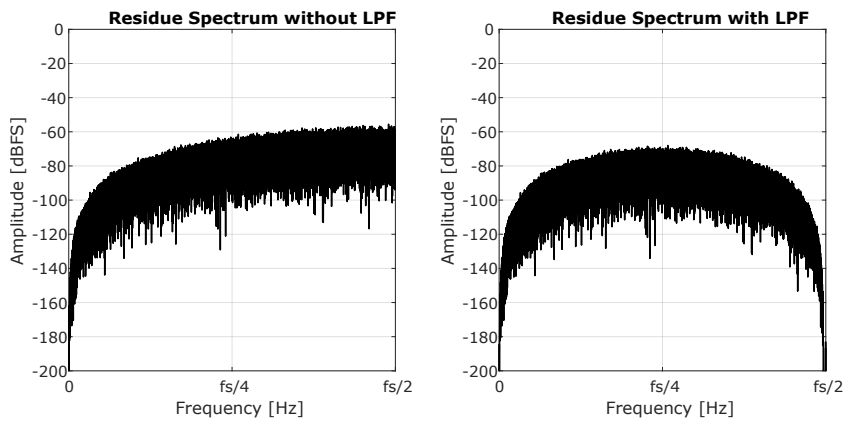
(a) Without out of band filtering



(b) With out of band filtering



(c) Residue in time domain



(d) Spectrum of Residue

Figure 2.3: Hybrid subranging ADC with fine stage nonlinearity

Assuming that the coarse stage has a noise shaping order of value  $L$ , the differentiation operation is expressed by the  $NTF = (1 - z^{-1})^L$ . This implies that the NTF has a number of  $L$  zeros at DC, which causes the increase of out-of-band quantization noise power. Therefore, a LPF with  $L$  zeros should be placed at  $fs/2$  in order to filter out the excess noise power introduced by the differentiation operation. The transfer function of the FIR (Finite Impulse Response) filter required for the LPF can be expressed as [8]:

$$H_{LPF}(z) = \frac{(1 + z^{-1})^L}{2^L} \quad (2.4)$$

Figures 2.3 (c) and (d) show a comparison between two systems that use a 2nd order NSSAR coarse stage: one without an LPF and one which includes an LPF. Due to filtering, the residue will have the same signal excursion as the quantization noise of a conventional Nyquist ADC (Figure 2.2 (b)) and therefore it relaxes the input range requirements for the fine stage with a nonlinear transfer function.

## 2.3 System Requirements

Figure 2.4 illustrates the hybrid ADC performance for a Matlab sweep of the input amplitude when the fine quantizer is modeled as a hyperbolic tangent nonlinearity. It can be concluded that a significant improvement in performance can be achieved by implementing a 2<sup>nd</sup> order Noise Shaping coarse quantizer, with the condition that a lowpass FIR filter is used on the analog and digital path.

It can be seen that for a 5-bit configuration of the capacitor array of the DAC, the case with noise shaping and low pass filtering achieves similar performance as a for the case when a 6-bit configuration is used. Moreover, just for the 5-bit configuration, using a 2<sup>nd</sup> order noise shaping quantizer instead of the conventional coarse quantizer implies at least 20dB of improvement

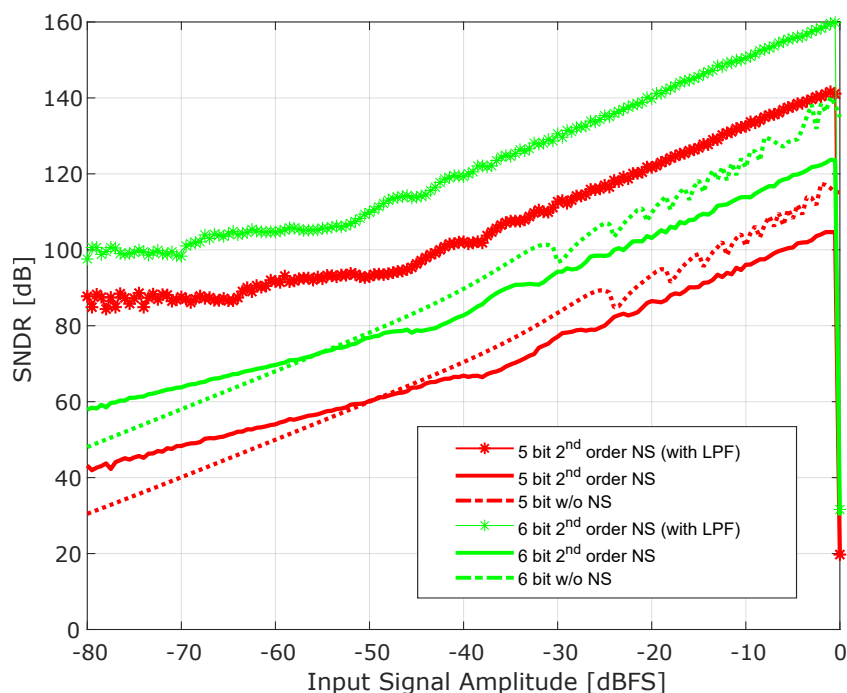


Figure 2.4: SNDR vs. input signal amplitude sweep for a nonlinear fine ADC

in linearity over the entire input signal range. The clear advantage of this implementation is the reduced overhead for the fine quantizer, besides the savings in power and area (for both quantizer and DAC in frontend) when compared to a 6-bit capacitive array. Additionally, the flattening out of the SNDR at amplitudes below -60 dBFS are resulting from the fact that the fine ADC is an ideal quantizer (no quantization error, thermal noise etc. is introduced) combined with a hyperbolic tangent transfer function which at very small signal amplitudes is very linear and introduces no gain error (but only for the case when a LPF is introduced and the residue swing is limited). Furthermore, for the case when Noise Shaping is used in the coarse stage, the residue resembles a white noise and therefore less harmonics of the input signal are generated.

When comparing the spectrum of the hybrid ADC's outputs in Figure 2.5, the highest linearity is achieved for the 2<sup>nd</sup> order noise shaping case. This shows that the best suppression of the in-band tones due to analog imperfections in the fine quantizer is enabled only by a higher order noise

shaping. In comparison to the conventional and 1<sup>st</sup> order implementations, only the 2<sup>nd</sup> order coarse quantizer can be used to obtain a residue which is independent of the input signal, creating an effect similar to dithering [3]. The combination of a 5 bit configuration NSSAR and a LPF can result in a 20 dB improvement in the SNDR of a subranging ADC.

As a conclusion, this work will focus on the investigation of a SAR ADC with a 5 bit CDAC and 2<sup>nd</sup> order noise shaping which can be integrated into a two-step subranging hybrid ADC. Therefore, the specifications of the ADC (Table 2.1) should be optimized such that it can replace the conventional asynchronous SAR from the previously published Zoom ADC [7].

CDAC size	Area [ $mm^2$ ]	BW [kHz]	ENOB	Power [ $\mu$ W]
5 bits	<0.015	20	>10 bits	<20

Table 2.1: ADC requirements

### 2.3. System Requirements

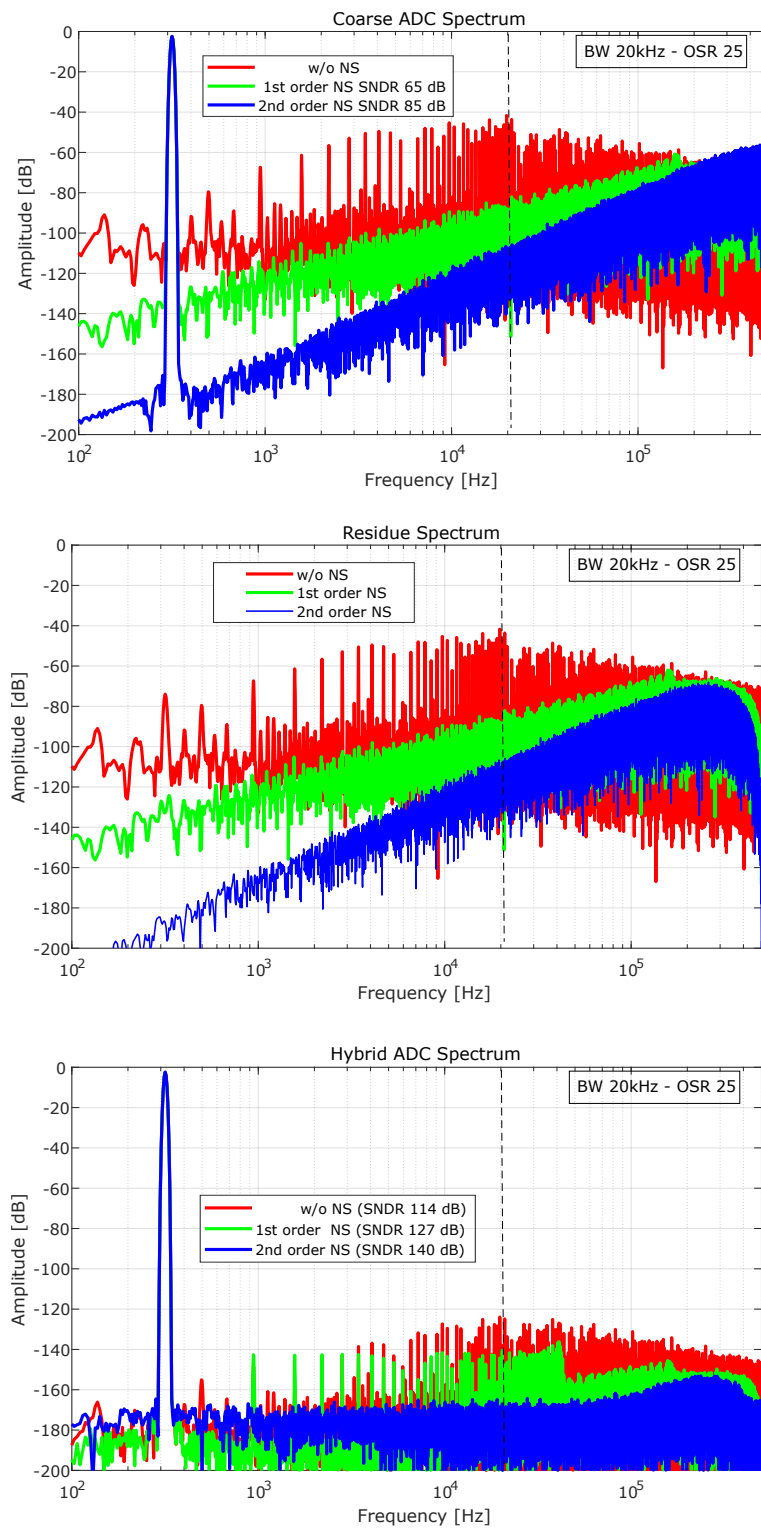


Figure 2.5: Hybrid Subranging ADC with filtered frontend - Spectrum of Coarse ADC output (top), Residue (middle), Hybrid ADC (bottom)



## Chapter 3 Noise Shaping SAR Techniques

### 3.1 Noise Shaping SAR ADCs

In a conventional SAR, the residue voltage produced on the DAC after the final N-th step is not equivalent to the difference between the digital output (scaled to the analog domain) and the sampled input. This happens because it usually requires only to find the LSB value, therefore not needing an additional switching of the last capacitor. However, as shown in Figure 3.1, the residue (which really reflects the quantization error) is obtained only by proceeding with this final switching operation. However, in conventional SAR ADCs, the residue is lost when entering into sampling mode.

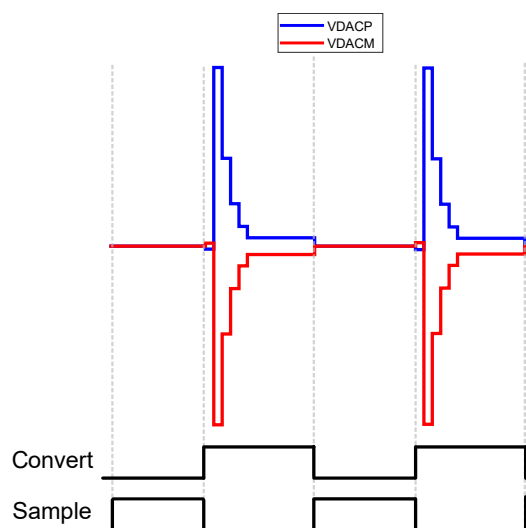


Figure 3.1: Timing diagram for 5 bit SAR ADC

The basic idea of noise shaping SAR ADCs is to find a way to use this residue information in order to reduce the inband quantization noise and the thermal noise of the comparator. This results in a drastic reduction in power

consumption and improvement in resolution. Figure 3.2 depicts state of the art SAR ADC designs that implement noise shaping (NS) (the bubbles have different sizes that are proportional to the area of the ADCs).

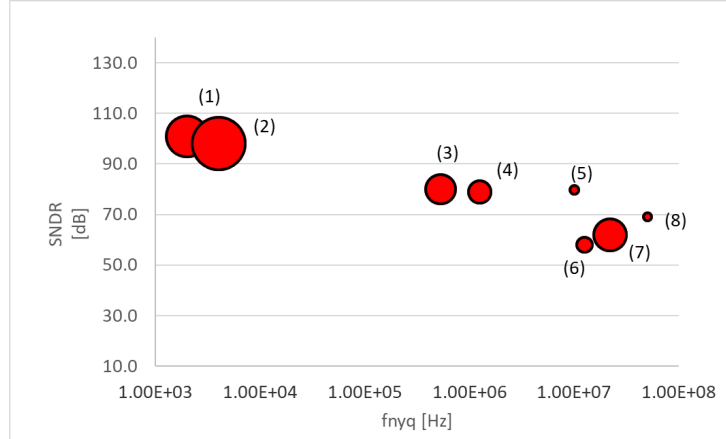


Figure 3.2: Noise Shaping SAR SNDR vs. Fnyq vs. Area

Fig. ID	1	2	3	4	5	6	7	8
Fsnyq [Hz]	2e3	4e3	5.26e5	1.25e6	10e6	12.5e6	22e6	50e6
OSR	500	25	16	8	13.2	4	4	6
Tech.[nm]	55	28	40	40	30	65	65	14
Area [ $mm^2$ ]	0.072	0.116	0.04	0.024	0.0049	0.0123	0.0462	0.0043
SNDR [dB]	101	98	80	79	80	58	62	69
FOMw [fJ]	86	143	33	9	6	15	36	21
Reference	[9]	[10]	[11]	[12]	[13]	[14]	[15]	[16]

Table 3.1: Comparison of state-of-the-art NSSARs

It can be seen that the design with ID (1) (Figure 3.2 and Table 3.1) can achieve 101 dB SNDR for a Nyquist frequency of 2kHz. However, the design uses mismatch error shaping, which is not the case for the targeted design since it should be implemented in a Zoom ADC where the coarse stage non-linearity is eliminated.

### 3.2 Feedforward Topology

A commonly used architecture in a NSSAR design is illustrated in Figure 3.3. The obvious hallmark of this scheme (firstly introduced in [15]) is the direct feedforward path to the quantizer input and the single feedback path from the output. The residue information will capture not only the quantization error, but also the noise from the final comparison and therefore it becomes:

$$V_{RES}(z) = D_{OUT}(z) - V_{IN}(z) \quad (3.1)$$

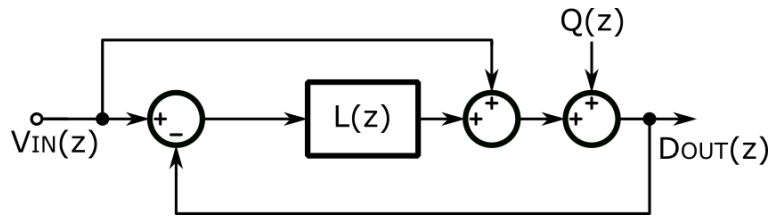


Figure 3.3: Feedforward architecture

Assuming that the loop filter  $L(z)$  comprises at least one integrator, this topology will benefit from the fact that the input signal to the loop filter contains only the shaped quantization noise. This relaxes the dynamics of the integrator and does not require any scaling of the coefficients, which leads to smaller values for the feedback capacitors.

Since the feedforward NSSAR was until recently the most popular approach of designing such a system, there were numerous implementations of this topology, each with its own advantages and disadvantages [9]-[11] [13]-[16].

It is useful to briefly discuss some of them since this can provide useful insights that can serve for the basis of a new design. Hence, the principle of operation of a feedforward NSSAR will be discussed next based on three different loop filters ( $L_1(z)$ ,  $L_2(z)$  and  $L_3(z)$ ) in Figure 3.4). The pole-zero mappings and the magnitudes of the noise transfer functions are illustrated in Figure 3.5.

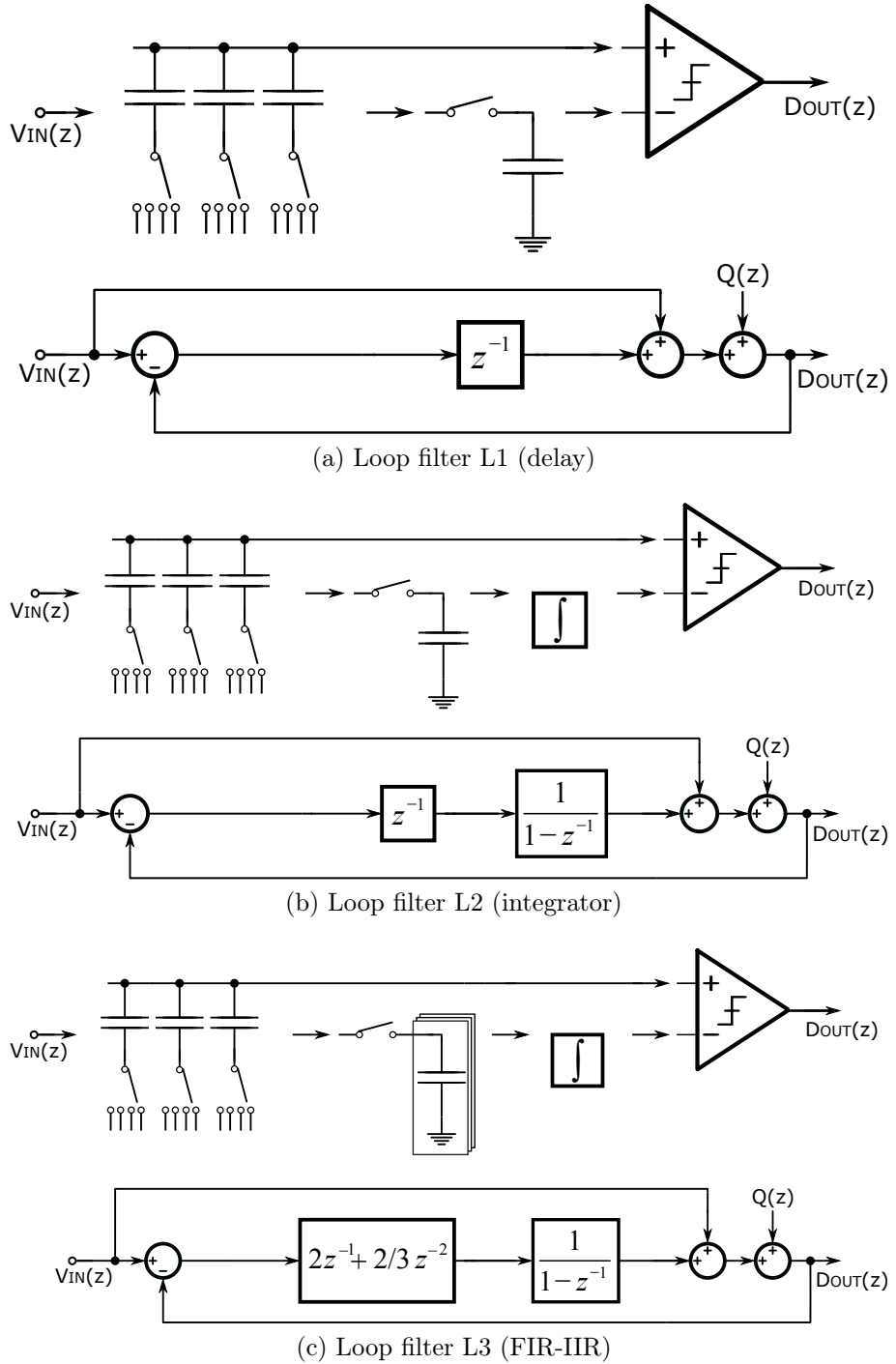
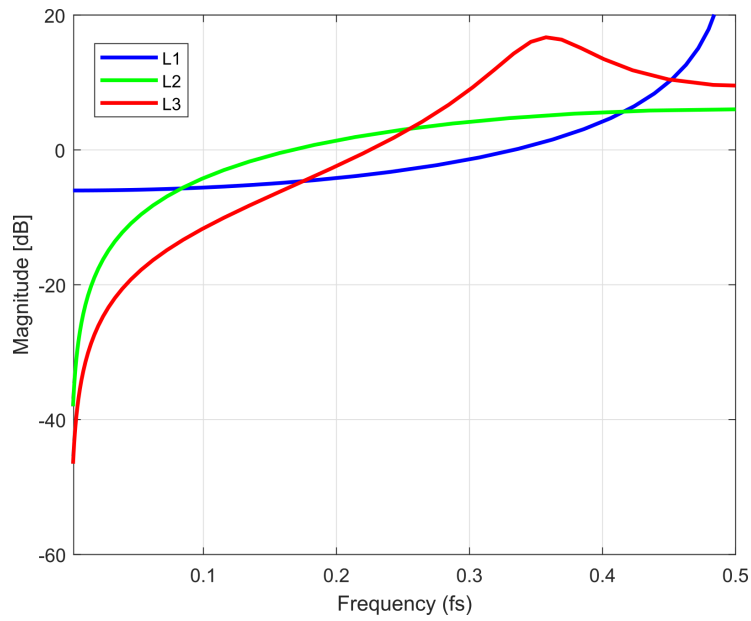
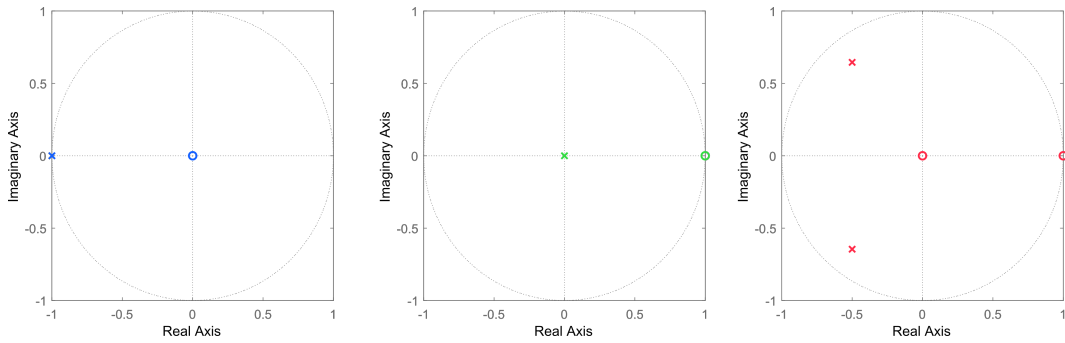


Figure 3.4: Feedforward NSSAR loopfilter implementations



(a) Noise Transfer Function



(b) Pole Zero Map

Figure 3.5: Feedforward NSSAR NTF and Pole-zero map

The simplest loop filter that can be implemented is shown in Figure 3.4(a), where  $L_1(z)$  is just a delay of the residue from the previous operation to the current cycle:

$$L_1(z) = z^{-1} \quad (3.2)$$

The residue voltage stored on a small residue capacitor charge-shared with the much larger CDAC contains both the quantization noise  $Q(z)$  and the thermal noise of the comparator  $V_{n,comp}(z)$ . The summation of the current cycle input (feedforward path) and the residue stored on the capacitor (output of the loop filter) can be realized by applying them to opposite polarity inputs of the comparator. The output  $D_{OUT}(z)$  can be expressed as:

$$D_{OUT}(z) = V_{IN}(z) + Q(z) + V_{n,comp}(z) - V_{RES}(z - 1) \quad (3.3)$$

Substituting 3.1 into 3.3 results in the following system transfer function:

$$D_{OUT}(z) = V_{IN}(z) + \frac{1}{1 + z^{-1}} \cdot (Q(z) + V_{n,comp}(z)) \quad (3.4)$$

This results in a high pass noise transfer function expressed as:

$$NTF_1(z) = \frac{1}{1 + z^{-1}} \quad (3.5)$$

Although there is some mild reduction of the inband quantization noise power, this loopfilter results in a very high out of band gain due to a pole at  $z = -1$ , which can be clearly seen in Figure 3.5.

In order to achieve a more effective noise shaping, the topology in Figure 3.4(b) implements an additional integrator after the sampling capacitor. This design requires a high-gain amplifier and a careful sizing of the residue capacitor in accordance with the kT/C limit. The loopfilter corresponding to this implementation is:

$$L_2(z) = \frac{z^{-1}}{1 + z^{-1}} \quad (3.6)$$

The system transfer function can be calculated as:

$$D_{OUT}(z) = V_{IN}(z) + (1 - z^{-1}) \cdot Q(z) \quad (3.7)$$

Consequently, the noise transfer function is equivalent to a first order differentiation:

$$NTF_2(z) = 1 - z^{-1} \quad (3.8)$$

In order to further improve the inband noise shaping, a combination of a FIR (time interleaved residue capacitors) and IIR filter (integrating the FIR output) is implemented, as shown in Figure 3.4(c). The following transfer function can be implemented for loop filter  $L_3(z)$ :

$$L_3(z) = 2 \frac{z^{-1} + 1/3z^{-2}}{1 - z^{-1}} \quad (3.9)$$

The corresponding noise transfer function with complex conjugate poles (Figure 3.5) can be expressed by:

$$NTF_3(z) = \frac{1 - z^{-1}}{1 + z^{-1} + 2/3z^{-2}} \quad (3.10)$$

All previously presented feedforward architectures will have a very effective suppression at very low frequencies, but most of the in-band noise contribution will be coming from the band edge where the noise power increases rapidly. Therefore, designing for a more aggressive noise shaping requires a straightforward optimization step of moving the location of the poles of the loopfilter, which are the zeros of the NTF.

Consequently, a good design direction is to find an architecture which combines the power efficiency of the SAR ADC and the possibility of achieving aggressive noise shaping for a very high SQNR by implementing this technique of zero placement optimisation.

### 3.3 First Order Error Feedback Noise Shaping SAR

The error feedback topology has recently shown a lot of potential for the case of the hybrid SAR ADC [17][18]. Figure 3.6 illustrates the basic flow diagram of such a structure where the quantization noise is obtained in the analog form and fed back through a filter, which in this particular case is a simple delay. The output of the system is given by:

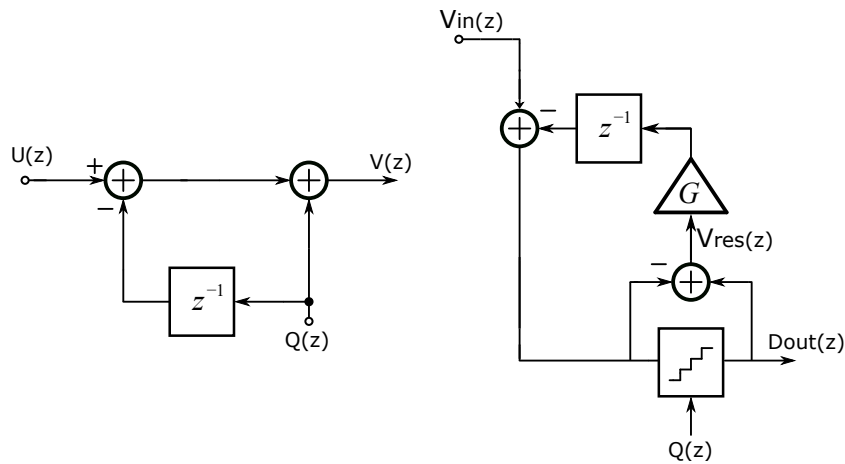


Figure 3.6: First order error feedback NSSAR diagram

$$V(z) = U(z) + Q(z) - Q(z - 1) \quad (3.11)$$

In a conventional Error Feedback Sigma Delta, the quantization error  $Q(z)$  is obtained by subtracting the digital output of the ADC  $Dout(z)$  with the input of the quantizer. Hence, the ADC requires an additional DAC in order to convert the digital output to the voltage domain, enabling the subtraction and obtaining  $Vres(z)$ .

The reason for which this structure was mainly used in the digital domain is the fact that any mismatch between the quantizer threshold levels and the DAC limits the resolution significantly.

However, this issue is readily solved by the inherent property that the



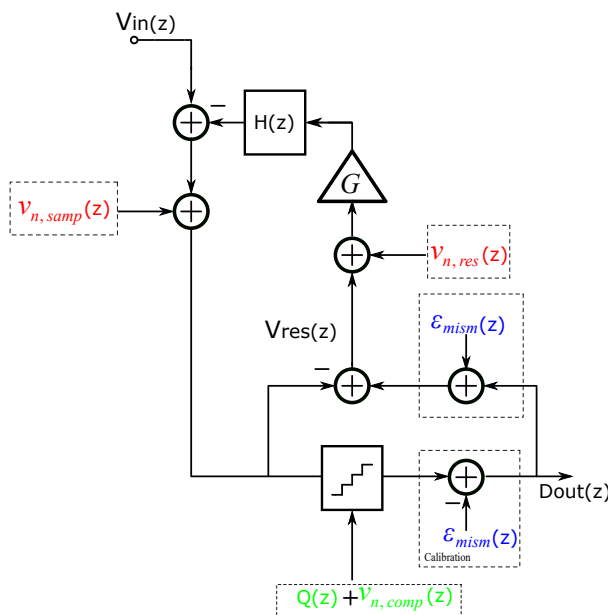


Figure 3.7: Non-idealities of error feedback NSSAR

quantization and the subtraction are executed by the same DAC. Consequently, no charge is lost after redistribution, which shifts the design issue from the mismatch between the quantizer and the DAC as for a conventional Sigma-Delta modulator to the linearity of a single structure (CDAC).

Moreover, in order to overcome the mismatch error injected at the output of the ADC, it has been shown in [12] that a simple calibration can suppress its effects similarly as for an open loop Nyquist ADC (Figure 3.7). Furthermore, thermal noise  $v_{n,samp}$  and  $v_{n,res}$  will not be noise shaped by the loop as for the case of the quantization noise and the thermal noise of the comparator, which can limit the SNR.

Although most of the energy efficient topologies deal with means of buffering the residue with a Dynamic-Amplifier [13] or passively sampling the residue [11][14][16] for minimizing power consumption and as a result benefit from process scaling, these implementations still require calibration due to PVT variations and other effects.

Therefore, since the supply for this project was not limiting the headroom (1.8 V supply), the design will use an OTA for minimizing the errors in the loopfilter of the error feedback architecture, benefiting from the simple fact

### 3.3. First Order Error Feedback Noise Shaping SAR

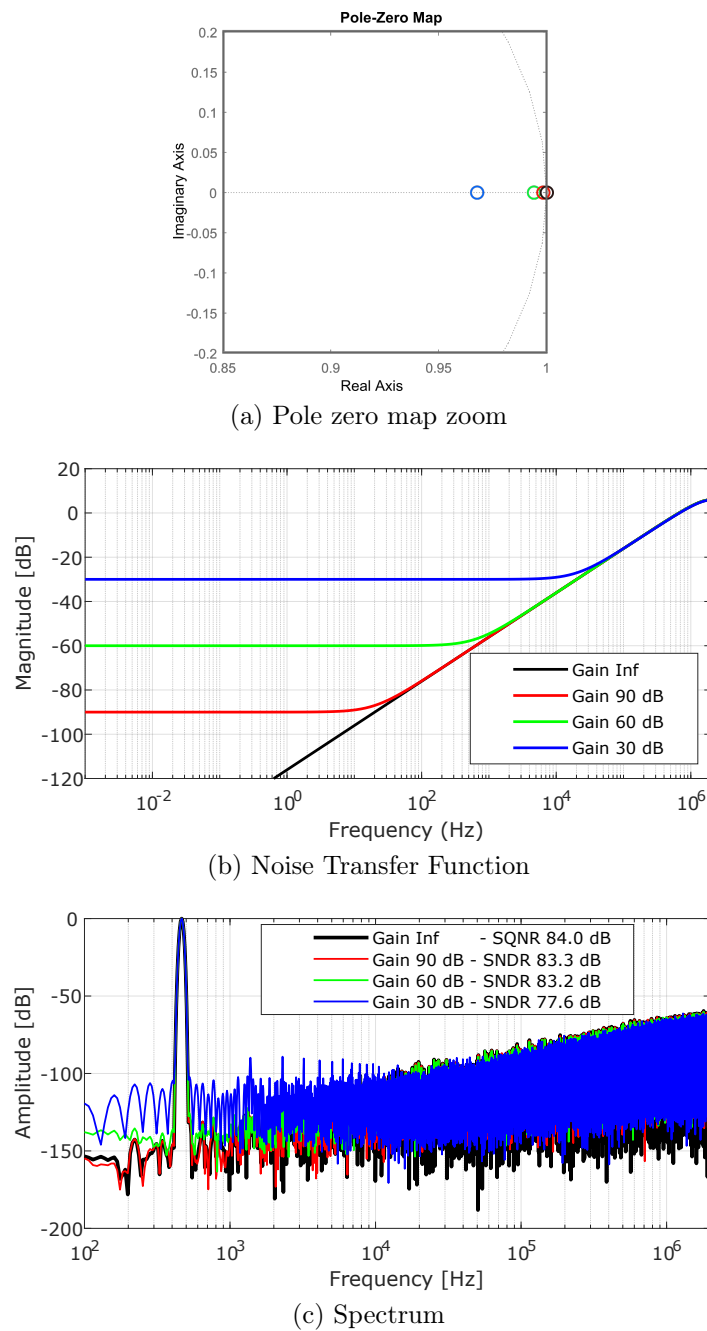


Figure 3.8: Finite gain effects for first order EF NSSAR

that the final residue has a very small swing (approximately 100mV for a 5 bit SAR). Moreover, a single stage amplifier with cascode transistors can be designed without any significant consequences on the power budgeting of the

ADC. Additional details about the circuit implementations are given in the next chapters.

After linearizing the first order system with a finite gain error  $G$ ,  $NTF_1$  reduces to:

$$NTF_1 = 1 - Gz^{-1} \quad (3.12)$$

Assuming that the open loop gain of an OTA  $A_v$  is constant and that  $G$  is an approximation of the static error due to incomplete charge transfer, the zero of  $NTF_1$  is:

$$z_{NTF_1} = G \quad (3.13)$$

$$z_{NTF_1} = 1 - \frac{1}{A_v} \quad (3.14)$$

Therefore, the effect of finite gain translates into an inward shift of the zero of the NTF (Figure 3.8). Consequently, the inband noise power will increase due to NTF attenuation.

### 3.4 Second Order Error Feedback Noise Shaping SAR

A higher order Noise Shaping SAR can also be implemented easily by changing the loopfilter  $H(z)$  with a higher order polynomial. Figure 3.9 illustrates the implementation of a second order topology. It has been shown in [12] that a two tap FIR filter will result in an inband notch, which will cause a significant improvement in the value of the SQNR.

The output of the linear system is given by:

$$V(z) = U(z) + (1 - 2z^{-1} + z^{-2}) Q(z) \quad (3.15)$$

For  $G = 1$  the zeros of the NTF are at DC and provide good suppression at low frequencies. But if the gain error  $G$  is included, the output can be

### 3.4. Second Order Error Feedback Noise Shaping SAR

expressed as:

$$D_{OUT}(z) = V_{IN}(z) + (1 - 2Gz^{-1} + Gz^{-2}) Q(z) \quad (3.16)$$

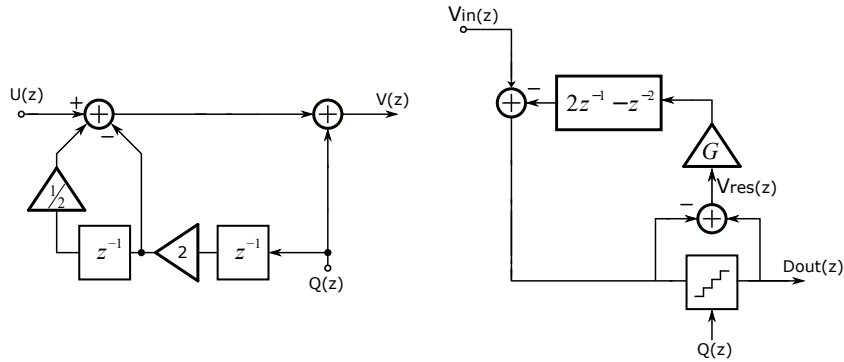


Figure 3.9: Second order error feedback NSSAR diagram

Consequently, the zeros will move from DC to complex positions given by:

$$z_{NTF2} = G \pm j\sqrt{G - G^2} \quad (3.17)$$

Finally, the effect of the zero optimization for a second order Error Feedback NSSAR can be seen in Figure Figure 3.10. The topology can reach an SQNR of 120 dB even with an OTA finite gain of 90 dB.

### 3.4. Second Order Error Feedback Noise Shaping SAR

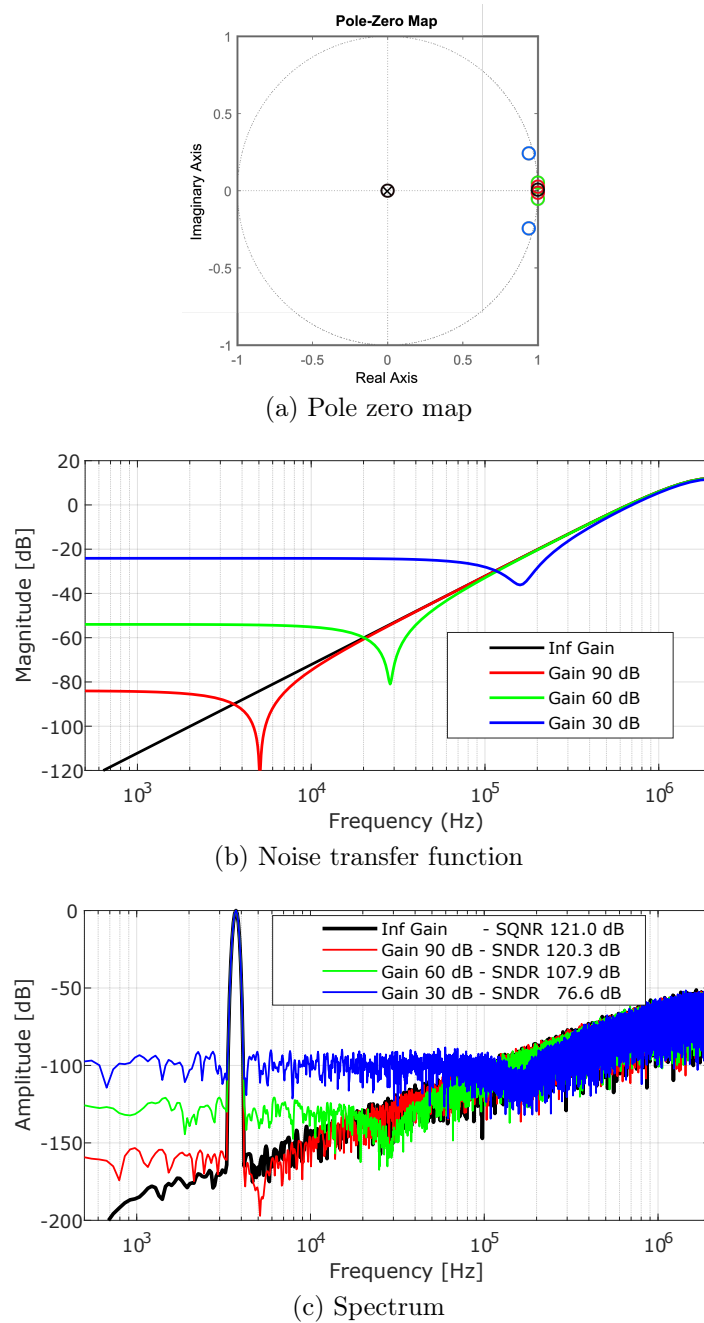


Figure 3.10: Finite gain effects for second order EF NSSAR



## Chapter 4 Design of an Error Feedback Noise Shaping SAR

### 4.1 Sampling Technique Considerations

With an advance in technology scaling, SAR ADCs are benefiting mostly due to their inherent characteristic of being switching intensive, which fits well with the increase in the speed of the transistors. Since the architecture of a SAR ADC is relatively simple, most design challenges are shifted towards improving the power and area efficiency while aiming for high resolution and speed. For the case of an NSSAR, blocks such as the digital controller or comparator are not as critical as the CDAC. Therefore, the choice of a proper switching scheme will enable a good design with high linearity and power efficiency. The implementation of a switching scheme determines not only the energy efficiency, but it also defines the size of the capacitive DAC since it is directly linked with performance metrics such as noise and matching.

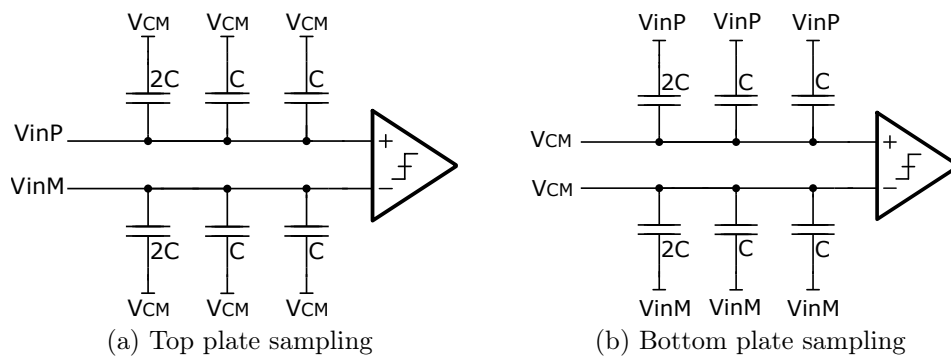


Figure 4.1: SAR ADC top and bottom plate sampling

For the case of charge redistribution capacitive DACs, the top plate of the capacitors is always associated with the plate applied to the input of the

comparator. Therefore, there are two choices that must be considered, and that is on which side of the capacitors should the input signal be applied (Figure 4.1). Top plate sampling applies the input signals to the input of the comparator, while bottom plate sampling keeps the input of the comparators at a well-defined voltage such as the common mode [3].

For the case of the top plate sampling (which is most commonly used), the advantage is that the decision of the MSB can be taken without any switching since the differential input signal is applied directly at the input of the comparator, which means that half the total amount of capacitors is required. On the other hand, a conventional bottom plate sampling procedure first samples the input, followed by switching to one of the references in order to redistribute the charge and compute the MSB.

However, there are a few issues related to top plate sampling: since there will undoubtedly be some parasitic capacitance on the top plate, this will result in an attenuation of the reference voltage due to this capacitive division, which results in a decrease of the allowable input signal range [3]. Moreover, there is an additional critical effect due to this gain error: the parasitics are usually non-linear, and any nonlinearity will degrade the SNDR. Lastly, the top plate sampling scheme is sensitive to non-linear clock feedthrough effects which means that using such a scheme is not suitable for the case of SAR ADCs with high-resolution [19].

Hence, for the case of bottom plate sampling, the reference, and the signal share the same path, and therefore there will be no issue in covering the range. Furthermore, using the bottom plate sampling approach will minimize the charge injection from the switches at the end of the sampling step, which results in a higher linearity design.



## 4.2 Error Feedback Basic Operation

For the case of the bottom plate sampling procedure, having the input of the comparator connected to a common mode voltage during the sampling step requires the use of an additional power hungry voltage generator which can limit the performance of the ADC if it isn't designed accurately [20].

There are mainly two ways of generating any reference voltage: using an off-chip reference with a very low impedance (usually needs a big decoupling capacitor in order to give sufficient cycle to cycle charge to the ADC, having bond wire inductance as a downside for settling) or a low impedance on-chip buffer which supplies sufficient current to the reference node (but needs to be very fast, while not consuming too much power).

Although most papers don't declare the power budgeting of the references, there is still considerable interest in optimizing the use of such blocks. For this reason, the design of this project is focused on the merge of the conventional voltage reference for the common mode with a block that changes the common mode voltage at the input of the comparator during sampling mode with a different voltage, from cycle to cycle, dependent on the residue from the previous cycle.

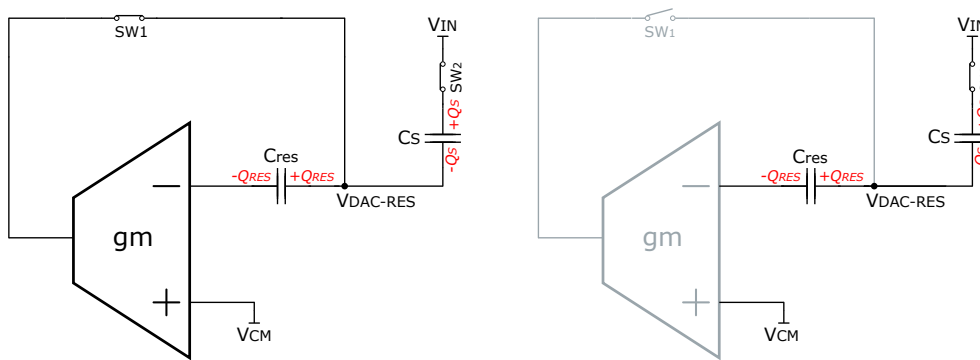


Figure 4.2: Bottom plate sampling based residue subtraction

For most switching schemes, the use of a binary capacitive array also implies having 2 LSB capacitors, where one is used for computing the LSB after its switching to a reference while the other is used as a dummy in order to counteract a gain error. As shown in Figure 4.2, error (residue) feedback

implies the use of this dummy capacitor for storing the charge from the end of the conversion and applying it in combination with an unity gain OTA. Considering that one end of the residue capacitor was previously connected to the common mode during the conversion step, applying it to the input of the OTA will not lead to any loss of charge since the virtual ground is an infinite impedance point (assuming an ideal case where parasitics are not taken into account).

Furthermore, charge conservation implies the fact that the voltage across the capacitor will not change while the input is applied to the bottom plate of the capacitors in the capacitive array. As a result, the charge sampled on the  $C_S$  capacitor is proportional to the difference between the input signal and the residue of the previous cycle, which clearly illustrates the principle of an error feedback architecture.

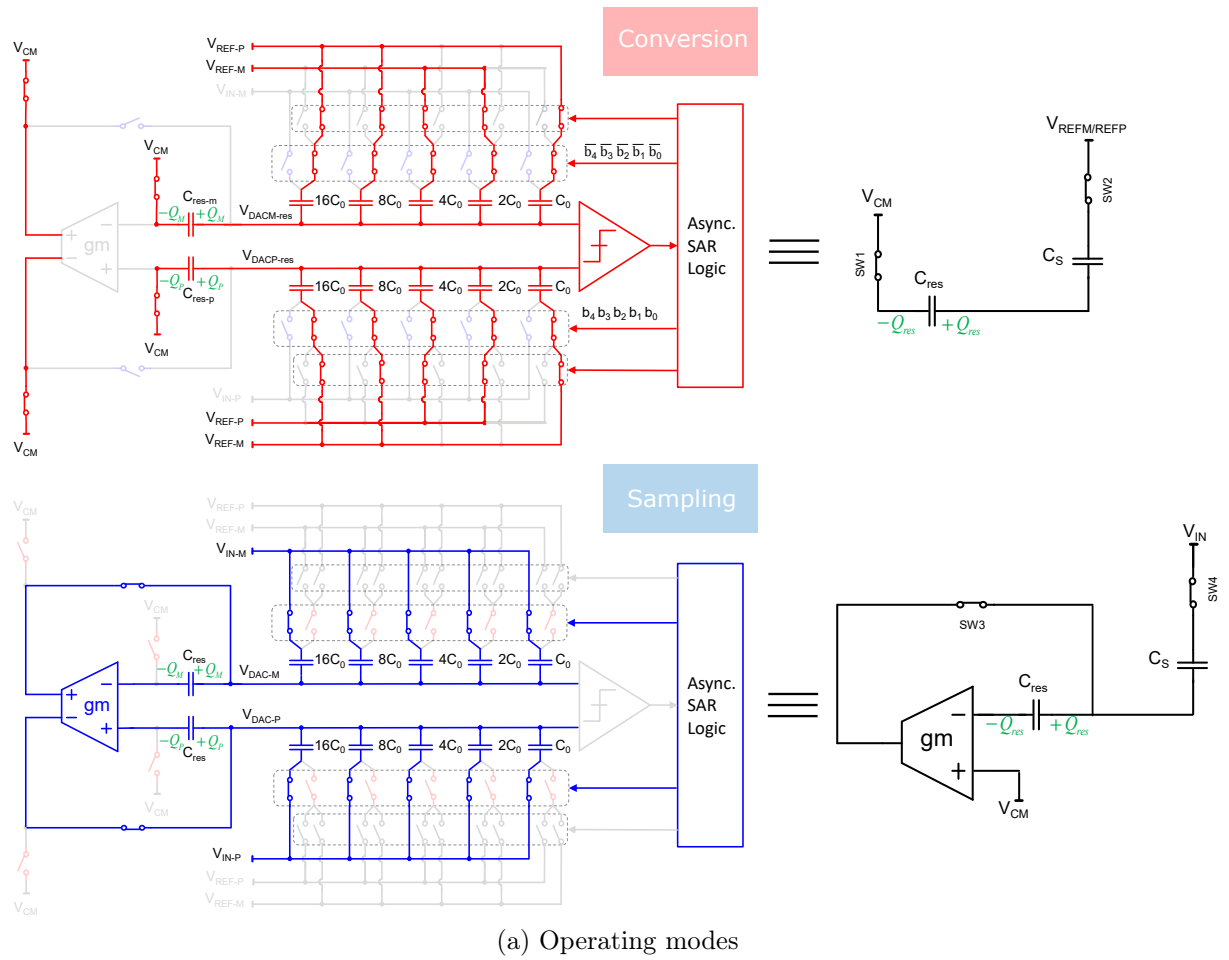
### 4.3 Implementation of a First Order Error Feedback Architecture

The basic operation of an error (residue) feedback from the previous cycle using the dummy capacitor is illustrated in Figure 4.3. Although a previous design of this type of architecture was implemented in [17], a few design changes were implemented. Firstly, it uses a simple asynchronous timing based on a manually designed digital domino logic in order to maximize power efficiency and minimize the latency of the conversion step.

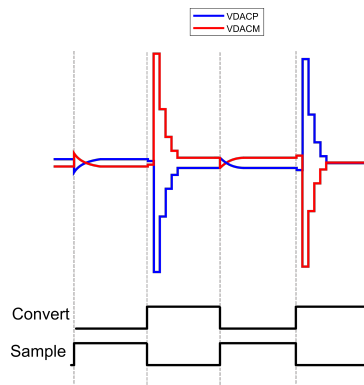
The use of a single clock for defining the two modes (*Sampling* and *Conversion*) gives the possibility of changing the oversampling rate easily since it uses only a non-overlapping clock generator for generating the timing signals. Secondly, due to area requirements, the unity capacitor chosen for the capacitive array has a value of 6fF, which results in a total allocation of  $2 \times 192$  fF for the 5 bit capacitive DAC used for this design.

Since the CDAC occupies most of the area, the target of this design is to have an area lower than  $0.01mm^2$ , and to keep the design space limited. Moreover, using a small CDAC is helpful for bandwidth limitations, but

### 4.3. Implementation of a First Order Error Feedback Architecture



(a) Operating modes

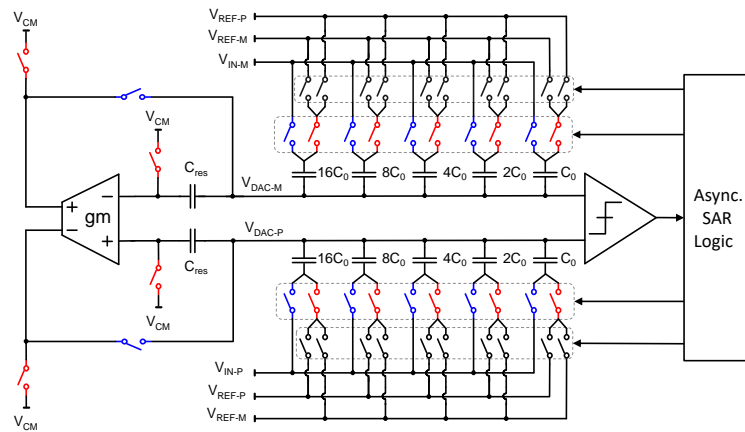


(b) Timing

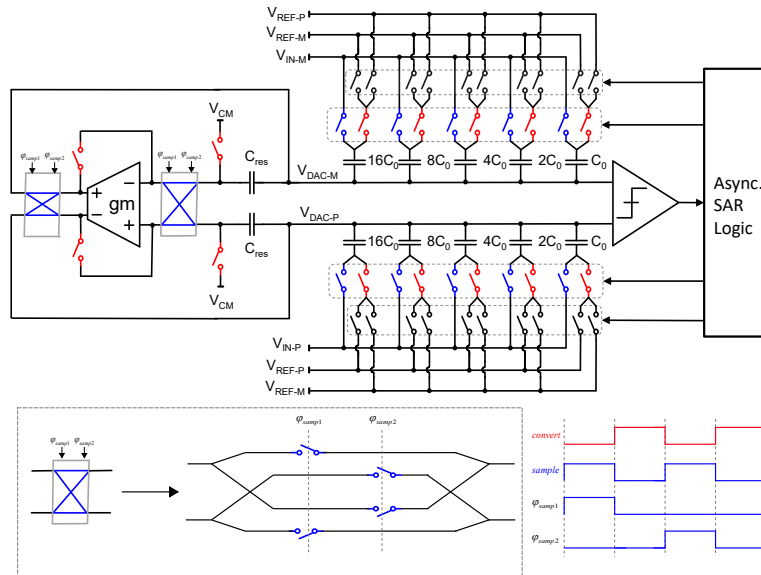
Figure 4.3: First order error feedback NSSAR operating modes and timing

### 4.3. Implementation of a First Order Error Feedback Architecture

can also increase the sensitivity to charge injection. Having a constraint on power efficiency and area at the same time should clearly prove the advantages of implementing a noise shaping SAR architecture that benefits from both worlds: the power efficiency and small area of a SAR and the high resolution of a Sigma Delta Modulator.



(a) Disable OTA in conversion mode



(b) Enable OTA in conversion mode

Figure 4.4: Error Feedback NSSAR OTA configurations

Also, a design option for saving power is to disable the OTA during the

conversion period. Note that having an active open loop OTA with inputs shorted to common mode during the conversion phase can saturate the output and can burn a lot of power. If the sampling rate is too high, it is better to keep the OTA in unity gain configuration since a power down and power up requires charging the parasitics (Figure 4.4(a)).

OTA offset adds up to the offset of the ADC, which can only affect the maximum input signal that can be applied. A limiting factor can be the 1/f thermal noise of the OTA, which can be easily removed by implementing butterfly switches for the feedback of the OTA which up-modulate the offset and 1/f noise of the OTA to higher frequencies (Figure 4.4(b)). This technique exploits the fact that the switches were already necessary in order to enable/disable the feedback around the residue capacitors. Additional details on the principles of chopping can be found in [3].

One key issue of the circuit is shown in Figure 4.5(a). At the transition from sampling mode (charge  $Q_S$ ) to conversion mode (charge  $Q_C$ ), the plate previously connected to the virtual ground of the OTA is connected to  $V_{CM}$ , while the bottom plate of the DAC capacitance  $C_S$  is switched from  $V_{IN}$  to  $V_{REF}$ , which gives the following change in charge:

$$Q_C = Q_S + (V_{REF} - V_{IN}) \cdot \frac{C_S \cdot C_{res}}{C_S + C_{res}} \quad (4.1)$$

This means that the new voltage on the top plate of the DAC  $V_{DAC-conv}[n]$  can be expressed as:

$$V_{DAC-conv}[n] = V_{DAC-res}[n-1] + (V_{REF} - V_{IN}[n]) \cdot \frac{C_S}{C_S + C_{res}} \quad (4.2)$$

This is equivalent to the influence of any parasitic capacitance on the top plate of the DAC. Furthermore, the inputs of the comparator  $V_{DAC-resP}[n]$

### 4.3. Implementation of a First Order Error Feedback Architecture

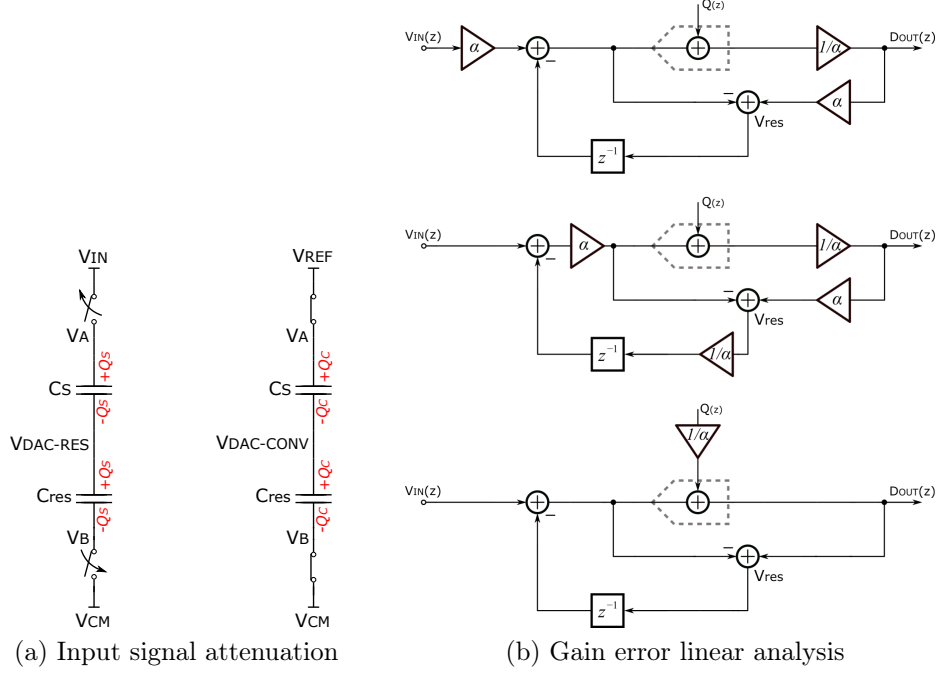


Figure 4.5: 1st order Error Feedback NSSAR Gain error effects

and  $V_{DAC\_resM}[n]$  at the end of the conversion process can be expressed as:

$$\begin{aligned}
 V_{DAC\_resP}[n] = & V_{DAC\_resP}[n-1] + \\
 & + (V_{REF\_M} - V_{INP}[n]) \cdot \frac{2^N - 1}{2^N} + \\
 & + (V_{REF\_P} - V_{REF\_M}) \cdot \sum_{k=0}^{N-1} \left( \frac{b_k \cdot 2^k}{2^N} \right)
 \end{aligned} \tag{4.3}$$

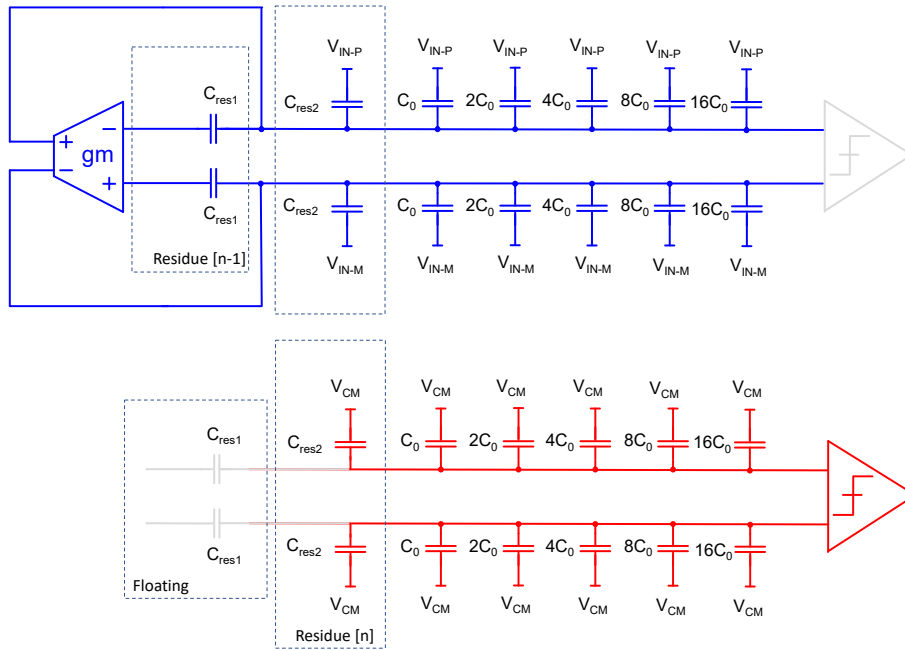
$$\begin{aligned}
 V_{DAC\_resM}[n] = & V_{DAC\_resM}[n-1] + \\
 & + (V_{REF\_P} - V_{INM}[n]) \cdot \frac{2^N - 1}{2^N} - \\
 & - (V_{REF\_P} - V_{REF\_M}) \cdot \sum_{k=0}^{N-1} \left( \frac{b_k \cdot 2^k}{2^N} \right)
 \end{aligned} \tag{4.4}$$

Equations 4.3 and 4.4 show that the input is multiplied by an attenuation factor  $\alpha$ :

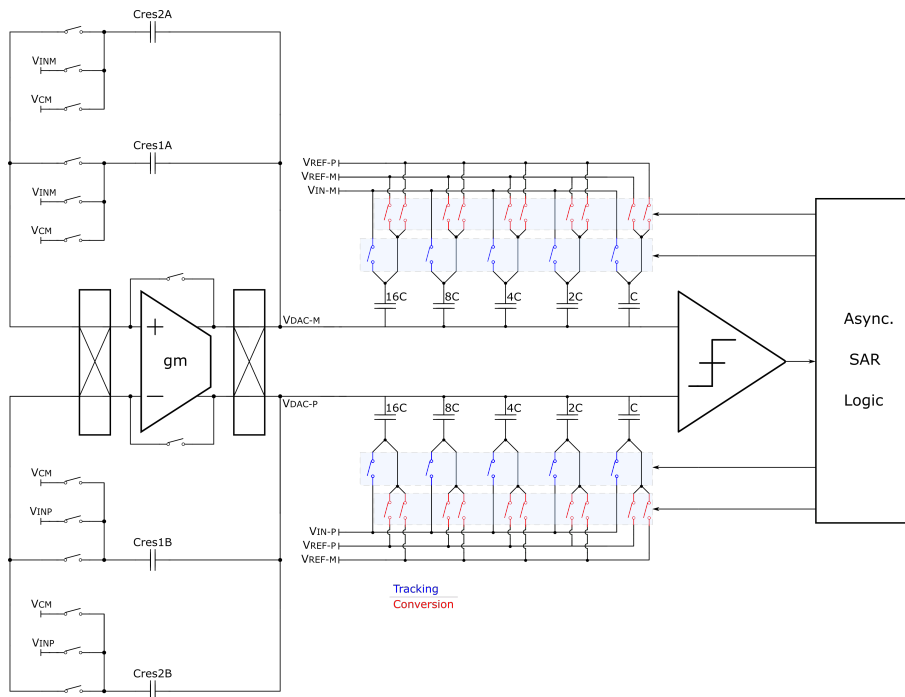
$$\alpha = \frac{2^N - 1}{2^N} \quad (4.5)$$

Since any gain error should be corrected in the digital domain, the linear analysis in Figure 4.5(b) shows that any input attenuation can be seen as an increase of the quantization error. In order to correct for this systematic error, Figure 4.6 shows the solution of using an additional pair of residue capacitors. Assuming the pair  $C_{res1}$  holds the residue from the previous cycle, the pair  $C_{res2}$  samples the input. Consequently, in the conversion step, capacitors  $C_{res1}$  are left floating. As a result of this solution, the gain error is removed since no more capacitors are connected to VCM.

### 4.3. Implementation of a First Order Error Feedback Architecture



(a) Interleaved floating of residue capacitors



(b) Implementation of 1<sup>st</sup> order NSSAR

Figure 4.6: Interleaved residue capacitors



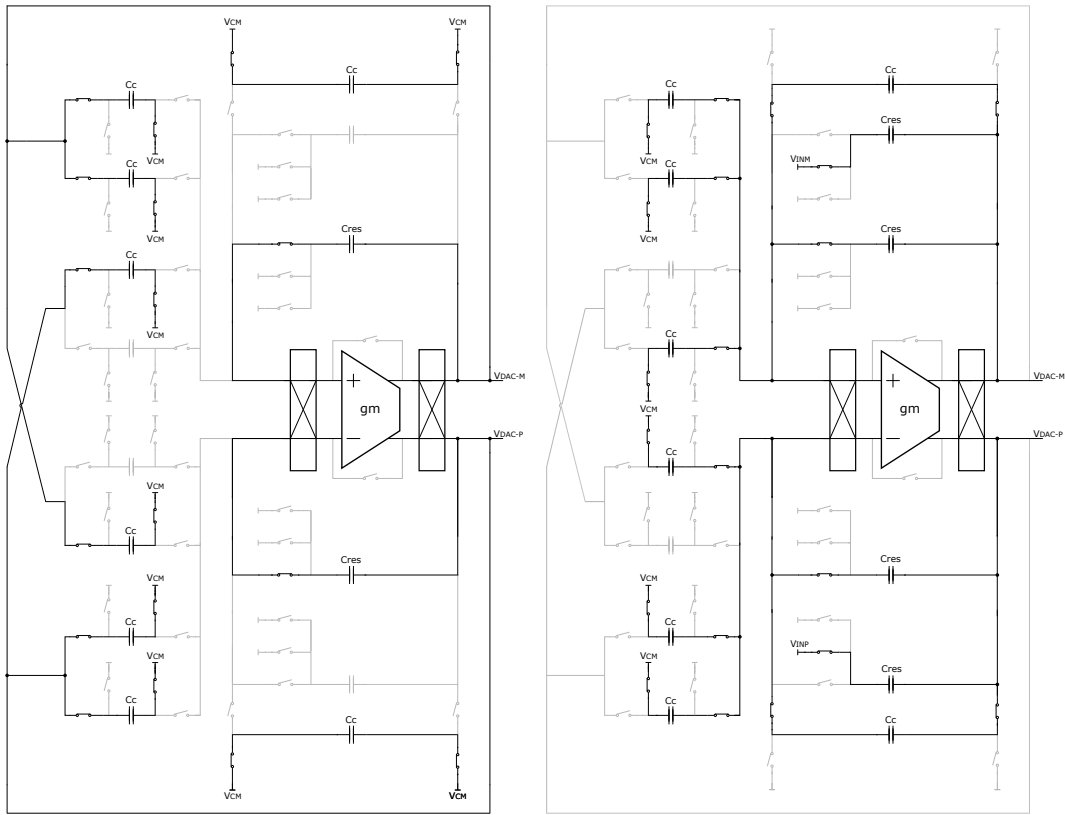
## 4.4 Implementation of a Second Order Error Feedback Architecture

Based on the analysis from the previous chapter, a second order NSSAR architecture would have a much more aggressive NTF. The advantage of this error feedback architecture is given by the fact that in between the end of conversion time (around 15 ns after the rising edge of the clock) and the falling edge of the clock when the SAR starts sampling again, there is sufficient time for an additional operation of the OTA. Therefore, an additional control signal (*Copy*) can be seen in Figure 4.7. In order to implement the FIR transfer function, the OTA is used to copy the value of the current residue on multiple capacitors  $C_C$ .

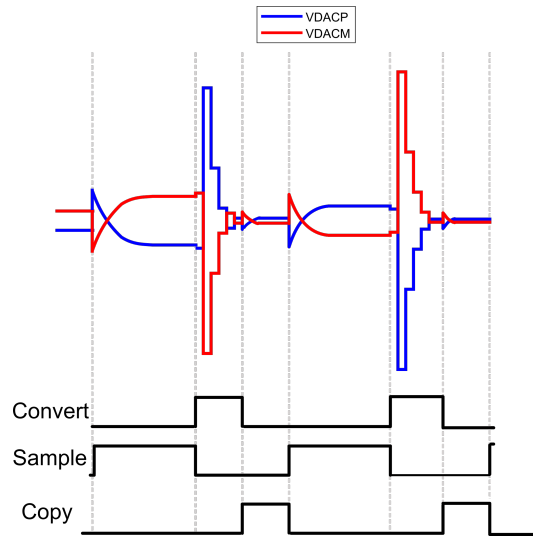
As a further observation, there are 2 types of capacitors used for the  $(2z^{-1} - z^{-2})$  FIR filter: the ones that implement the coefficient related to the one cycle delay ( $z^{-1}$ ), which are used for the immediate sampling step following the current copy process, and the ones corresponding to 2 cycles delay ( $z^{-2}$ ) where one pair samples the current residue for the cycle following the current one. Again, the timing is relatively simple since it only requires a D flip flop for generating an interleaving signal for the pair of capacitors. Finally, the summation of the charge is carried out at the beginning of the sampling mode, by connecting the  $C_C$  capacitors to the virtual ground of the OTA. Consequently, since there is an additional  $C_C$  which is reset during each conversion, the FIR filter will have no other memory effects besides the 2 coefficients given by the  $C_C$  capacitors. Furthermore, the transfer function can be easily changed by using different values for the feedback capacitor, which will result in a zero optimization and therefore increase the performance of the NSSAR. This means that a digital calibration procedure can also be applied in order to find the optimum value of the coefficients.

Since the OTA is assumed to have a finite gain, it has been shown in the previous chapter that a finite gain of 90 dB will give the same SQNR as for the case when an infinite gain OTA is used. This is an important design detail since not many circuits can achieve similar performance with the ideal case without making a lot of design efforts.

#### 4.4. Implementation of a Second Order Error Feedback Architecture



(a) Residue copy (left) and sampling (right)



(b) Timing of the second order NSSAR

Figure 4.7: 2<sup>nd</sup> order Error Feedback NSSAR Operating modes and timing

## 4.5 OTA Static and Dynamic errors

The parasitic capacitance at the input of the OTA is a sensitive design point since the unit residue capacitor has a value of 6 fF. Therefore, not only finite gain, but also the parasitic capacitance (Figure 4.8) can have a contribution to the final static error which can be expressed as:

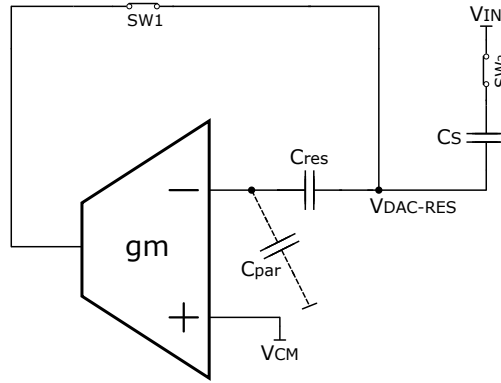


Figure 4.8: OTA parasitic capacitance

$$V_{DACRES} \simeq V_{in} \left[ 1 - \frac{1}{A_{open-loopDC}} \left( 1 + \frac{C_{par}}{C_{res}} \right) \right] \quad (4.6)$$

$$\varepsilon_{static} = \frac{1}{A_{open-loopDC}} \left( 1 + \frac{C_{par}}{C_{res}} \right) \quad (4.7)$$

A sweep of the transconductance and gain for an ideal OTA model implemented in the 1<sup>st</sup> order Noise Shaping SAR for a sampling frequency of 4MHz is illustrated in Figure 4.9. It can be clearly seen that depending on the OSR value of the application, the design could be limited not only by static error but from dynamic error also. The OTA is used for both sampling and copying the residue and therefore, depending on the specifications it can be designed to be either power efficient with low dynamic performance or the opposite, power hungry and with high dynamic performance.

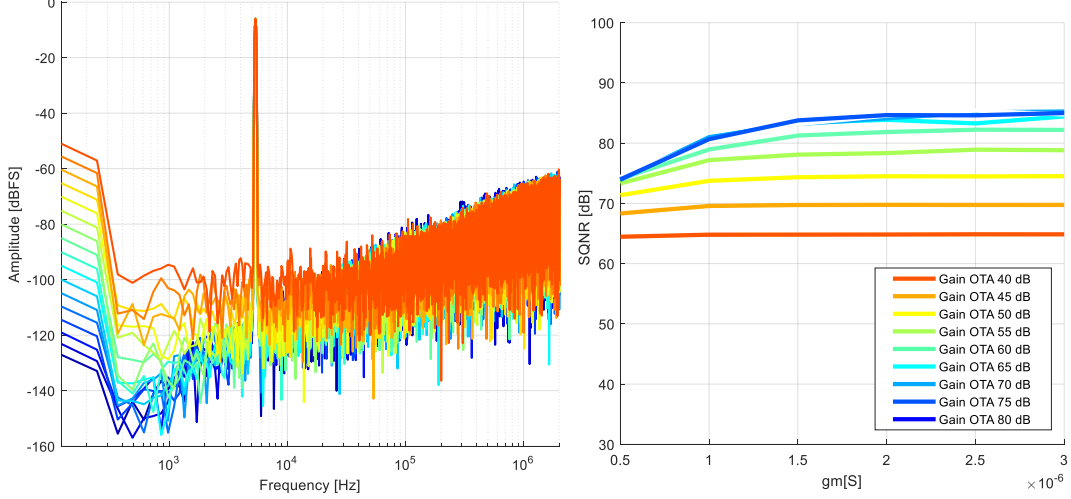


Figure 4.9: OTA finite gain and finite transconductance

The Bode diagrams of the open loop and closed loop transfer functions of an amplifier are shown in Figure 4.10.

The dynamic performance of the amplifier is dependent on the dominant pole of the closed loop transfer function:

$$\omega_{closed-loop} = \beta_F \frac{g_m}{C_{Load,total}} \quad (4.8)$$

Where  $\beta_F$  is the feedback factor,  $g_m$  is the total transconductance of the amplifier and  $C_{Load,total} = C_S + (1 - \beta_F)C_{res}$  is the equivalent output capacitance of the OTA. The dynamic error can be calculated as:

$$\varepsilon_{dynamic} = e^{-\frac{T_{settling}}{\tau}} \quad (4.9)$$

Where  $T_{settling}$  is the time allocated for the OTA operation and  $\tau = \frac{1}{\omega_{closed-loop}}$  is the time constant of the amplifier.

Therefore, the dynamic error of the OTA can also be expressed as:

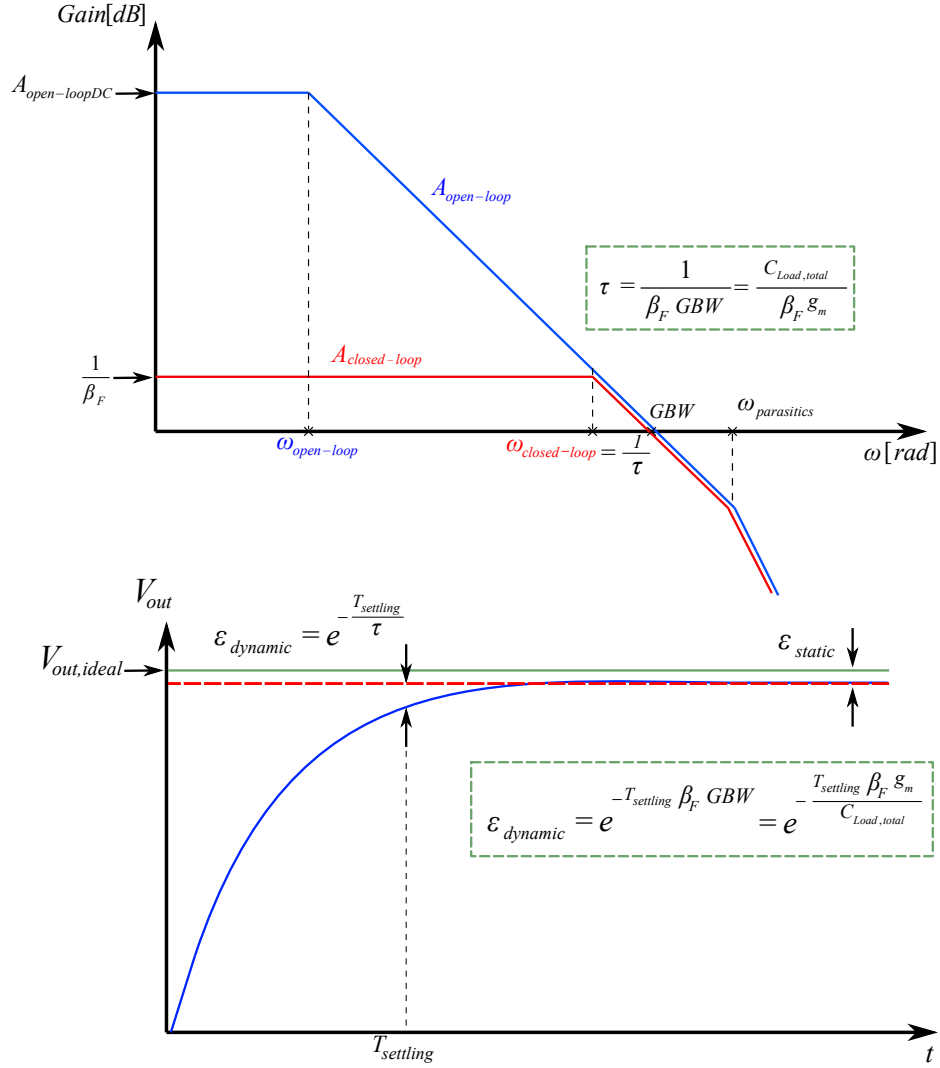


Figure 4.10: OTA Bode diagram and settling operation

$$\epsilon_{dynamic} = e^{-\frac{T_{settling} \beta_F g_m}{C_{Load,total}}} \quad (4.10)$$

This shows that in order to reduce the dynamic error for a fixed settling time, capacitive load  $C_{Load,total}$  and  $\beta_F$  (which are system level constraints), it is necessary to invest current and increase the transconductance of the amplifier.

The schematic of the current reuse OTA used in the design is illustrated in Figure 4.11. It benefits from this architecture since the residue of a 5 bit SAR is smaller than 100mV and it allows a small swing at the output of the OTA.

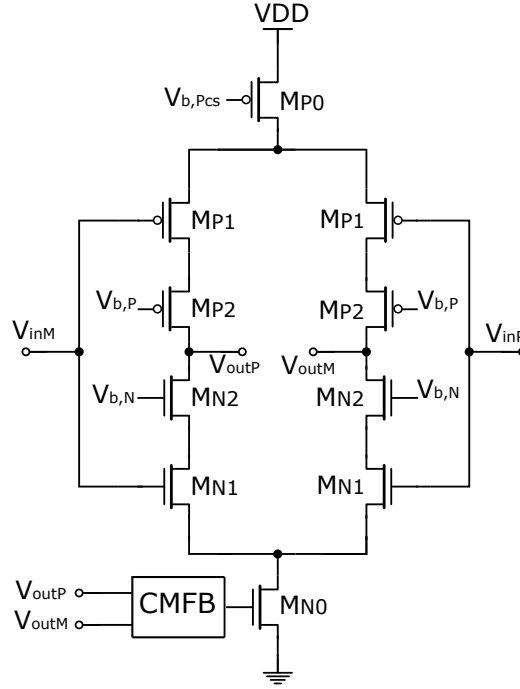


Figure 4.11: Current reuse OTA schematic

The static current of the OTA was chosen to be 2  $\mu\text{A}$  since it is a single pole amplifier (pole is defined by the capacitive load of the total 192 fF on each output) and doesn't require additional current or any compensation. It is biased with current mirrors generated from a constant  $g_m$  biasing (Figure 4.12) in order to guarantee a stable gain over PVT variations. The transconductance of transistor  $M_A$  in Figure 4.12 can be calculated as:

$$g_{mA} = 2 \frac{\left(1 - \sqrt{\frac{(W/L)_A}{(W/L)_B}}\right)}{R_B} \quad (4.11)$$

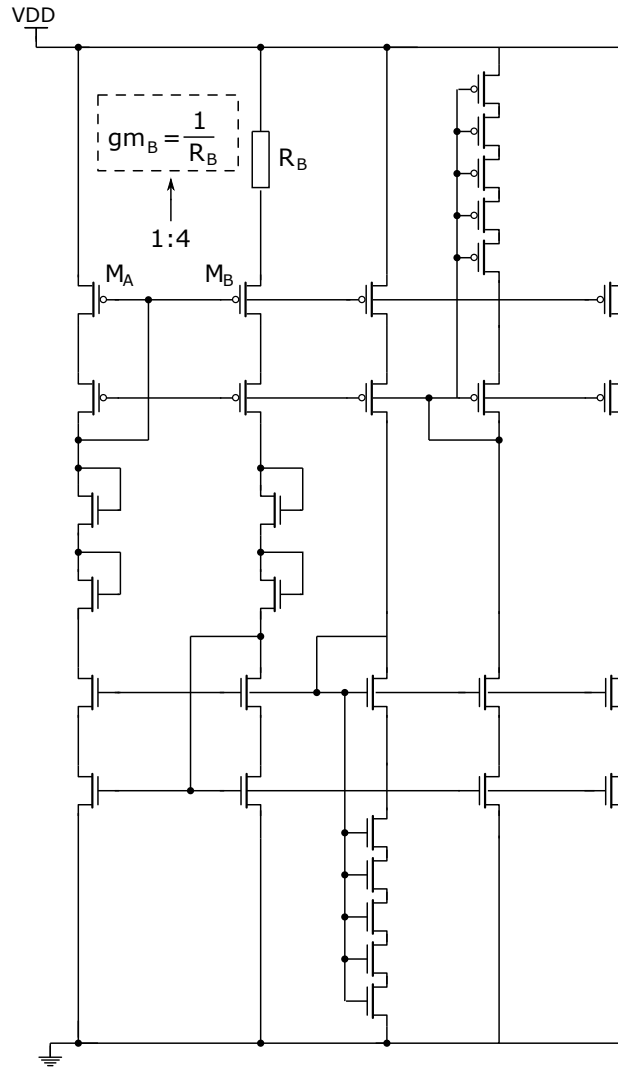


Figure 4.12: Constant gm biasing

For the case when  $(W/L)_B/(W/L)_A = 4$ , the transconductance is given by:

$$g_{mA} = \frac{1}{R_B} \quad (4.12)$$

The biasing is designed with a 1uA static current consumption and is dependent only on the spread of the resistor. Table 4.1 shows the OTA performance across all corners. The design achieves a minimum/maximum GBW of 6.6/11.7 MHz in the slow/fast corner.

Corner	Temperature [ °C]	Gain [dB]	GBW [MHz]
slow	-40	70.94	6.61
slow	25	70.90	7.08
slow	85	69.18	7.02
sensp	-40	71.41	7.13
sensp	25	71.32	8.03
sensp	85	68.96	8.16
snfp	-40	72.84	8.90
snfp	25	71.88	8.79
snfp	85	68.97	8.65
Nominal	-40	71.89	9.21
Nominal	25	70.63	8.96
Nominal	85	66.64	8.81
fensp	-40	70.09	9.38
fensp	25	67.89	9.12
fensp	85	59.29	8.96
fnfp	-40	70.19	9.52
fnfp	25	68.00	9.31
fnfp	85	59.54	9.18
fast	-40	71.21	11.77
fast	25	67.88	11.51
fast	85	56.05	11.31

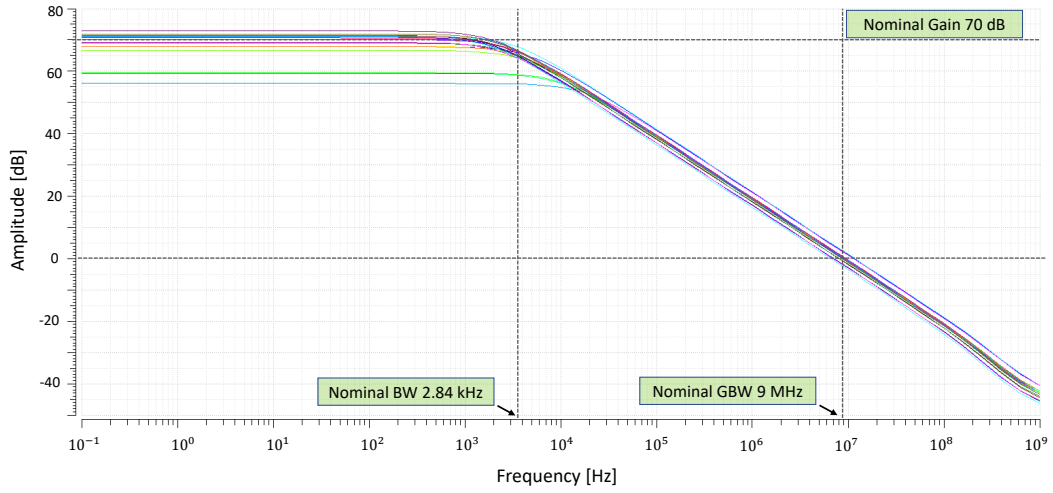
Table 4.1: OTA Performance across corners

The Cadence AC analysis in Figure 4.13(a) shows that the OTA nominal gain is 70 dB and the nominal GBW has a value of 9 MHz.

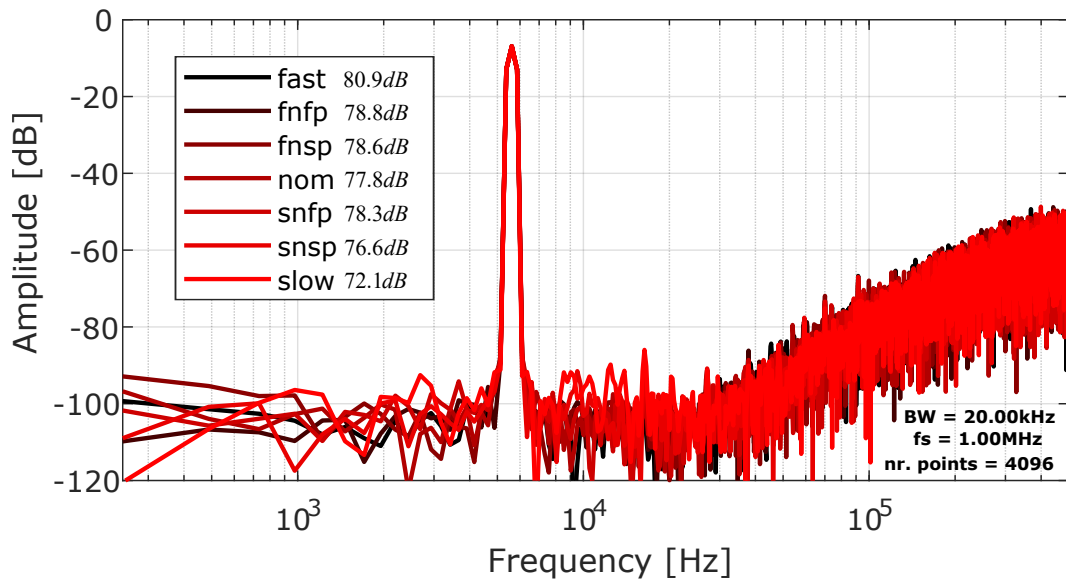
Finally, since the fully differential OTA requires a common mode feedback, the implementation of the low power switched capacitor CMFB is illustrated in Figure 4.14(a). The step response in Figure 4.14(b) shows that the common mode is stable over all corners and over the temperature range.



#### 4.5. OTA Static and Dynamic errors



(a) Switched capacitor common mode feedback implementation



(b) FFT for Second order NSSAR - SNDR without noise

Figure 4.13: OTA Cadence corner simulations

#### 4.5. OTA Static and Dynamic errors

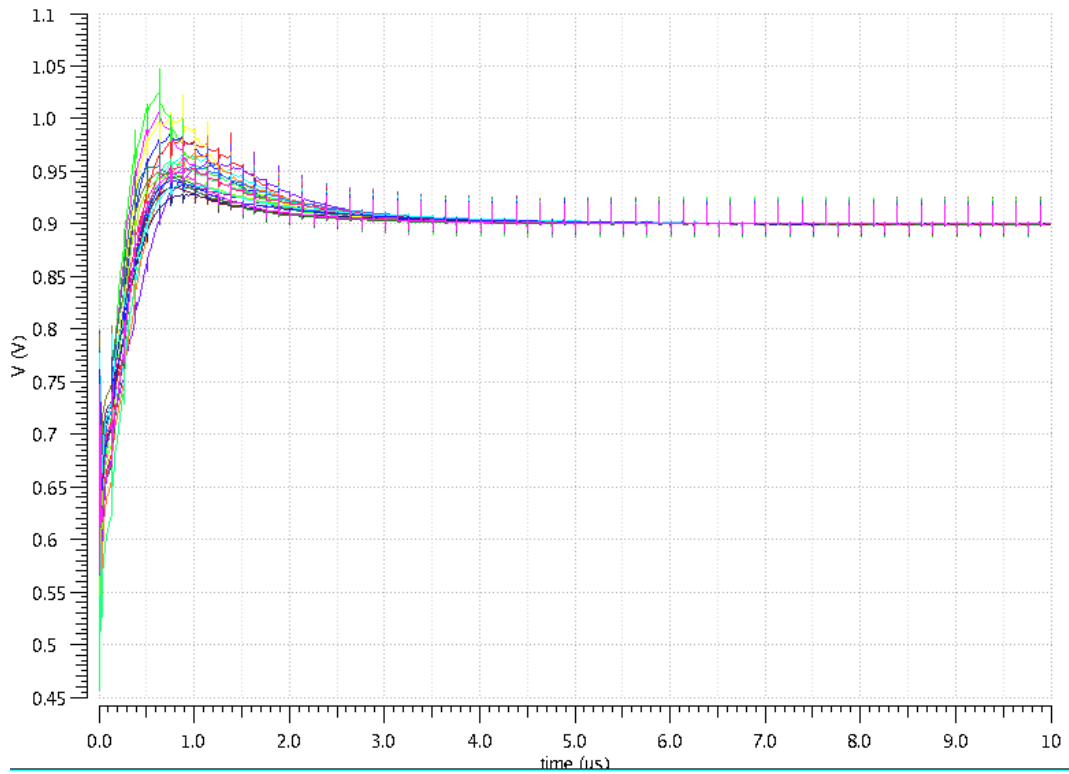
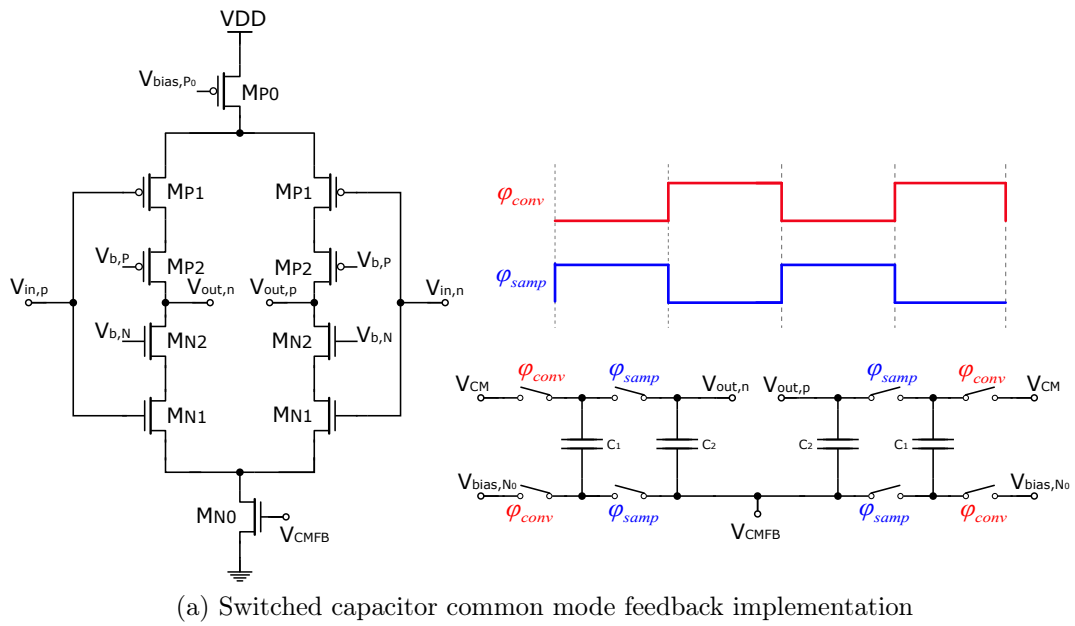


Figure 4.14: Switched capacitor common mode feedback

## 4.6 Noise Limitations

During the sampling operation, the OTA should contribute most of the thermal noise since the switches should be designed for speed. Therefore it requires a very low impedance, at least 10x smaller than  $1/g_m$ , in order not to limit the dynamic performance of the circuit either. However, it is easy to refer the noise contribution of the switches to the input of the OTA and summing their power, since their equivalent noise voltage sources are in series, as can be seen in Figure 4.15.

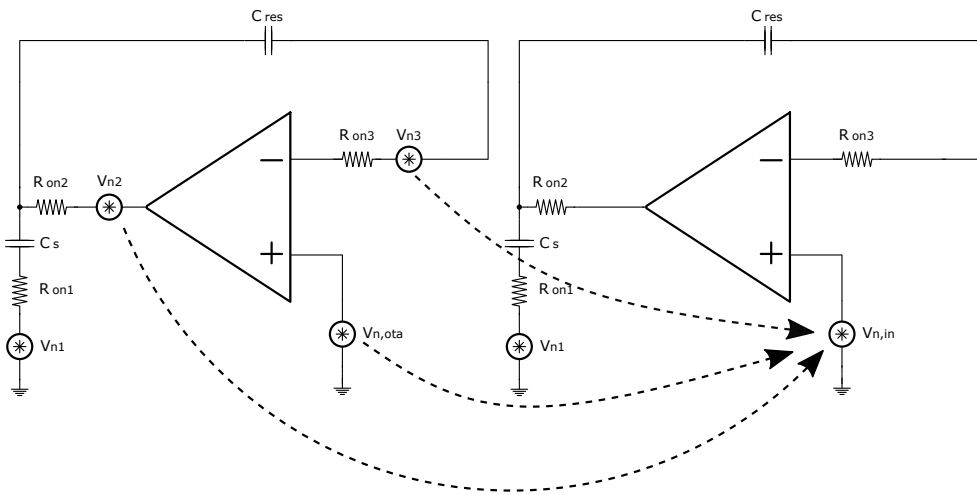


Figure 4.15: Sampling mode noise

Considering that the OTA input referred noise is dominant, contribution of  $V_{n,in}$  to the output can be found to be:

$$\overline{V_{n,out,samp}^2} = \frac{N_{EF}kT}{\beta_F C_{Load,total}} \quad (4.13)$$

where  $k$  is the Boltzmann constant,  $T$  is the temperature and  $N_{EF}$  is the noise excess factor that varies between 1 and 2 depending on the choice of the OTA design. Since a current-reuse design has an inverter type of input, the  $N_{EF}$  will be much closer to 1 since the tail transistor or cascode transistors will have limited contribution. Furthermore, this topology uses both NMOS and PMOS devices as input differential pairs, resulting in a doubling of the

total transconductance.

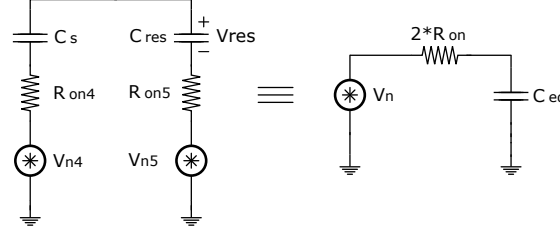


Figure 4.16: Noise limitation due to the residue capacitor

For the case of the residue sampling noise (Figure 4.15), the power spectral density (PSD) of the noise voltage across  $C_{eq}$  is given by:

$$S_{C_{eq}}(f) = \frac{8kTR_{on}}{1 + [2\pi f (2R_{on}C_{eq})]^2} \quad (4.14)$$

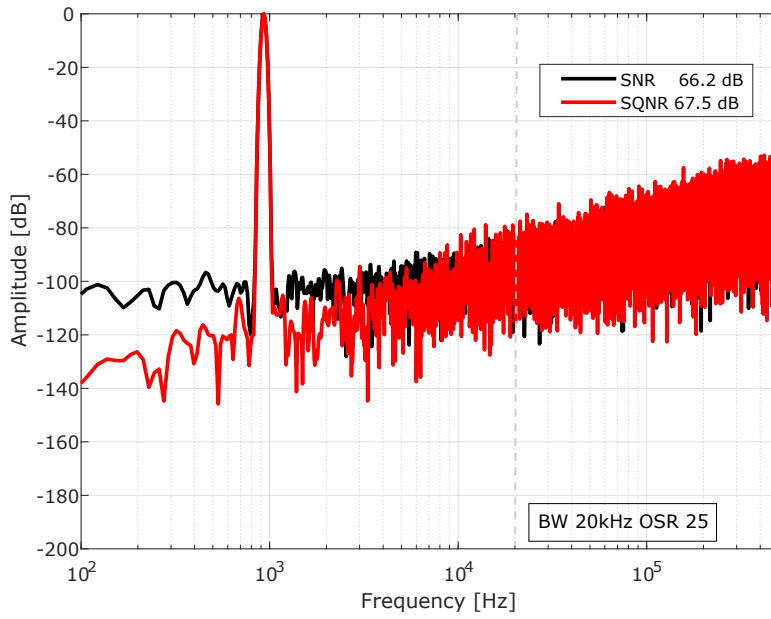
Since the PSD is integrated and shaped by the transfer function of the equivalent low pass filter, the change of state from conversion to sampling mode will cause for the noise charge to be trapped on  $C_{eq}$ , which will cause a folding of the noise spectrum with a noise power given by:

$$\overline{V_{C_{eq}}^2} = \frac{8kTR_{on}}{4(2R_{on}C_{eq})} = \frac{kT}{C_{eq}} \quad (4.15)$$

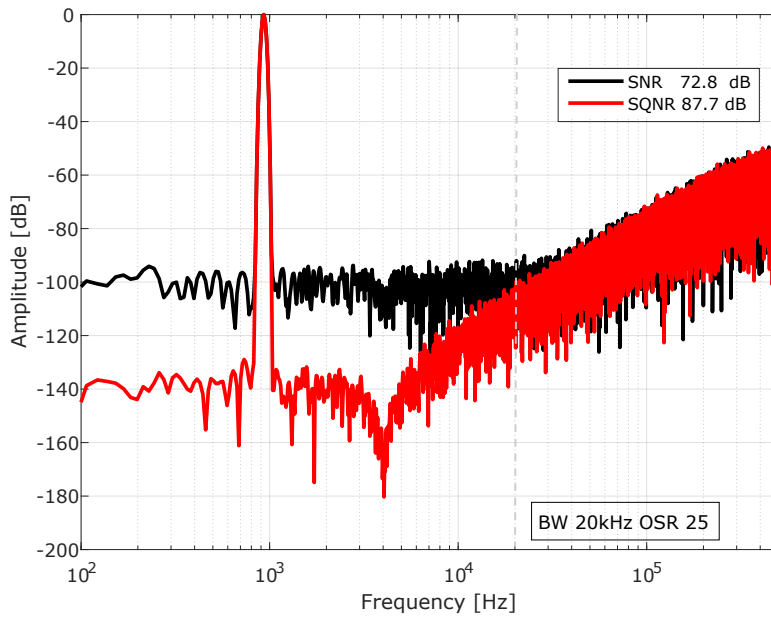
The noise charge stored on  $C_{eq}$  is  $q_{eq}(t) = C_{eq}V_{C_{eq}}(t)$ , so the mean square of the noise charge is  $C_{eq}^2 \frac{kT}{C_{eq}} = kTC_{eq}$ . This noise charge is transferred to the residue capacitor, which gives the output referred noise power of:

$$\overline{V_{n,out,res}^2} = \frac{kTC_{eq}}{C_{res}^2} \simeq \frac{kT}{C_{res}} \quad (4.16)$$

This shows that the design is limited for a very low value for the residue capacitor and the only solution is to either increase the unit cap size or to increase the OSR.



(a) Spectrum of 1<sup>st</sup> order NSSAR



(b) Spectrum of 2<sup>nd</sup> order NSSAR

Figure 4.17: Comparison of 1<sup>st</sup> order and 2<sup>nd</sup> order NSSAR - thermal noise SNR vs. quantization noise SQNR

Finally, after seeing all the limitations of the ADC, a comparison between the 1<sup>st</sup> order and 2<sup>nd</sup> order NSSAR illustrated in Figure 4.17 shows the benefit of implementing a higher order. For an OSR of 25, in the case of the 1<sup>st</sup> order, the design is limited by both thermal noise and quantization noise, while the 2<sup>nd</sup> order is only limited by thermal noise in a 20 kHz BW.

## Chapter 5 Design of an Energy Efficient 2<sup>nd</sup> order Error Feedback Noise Shaping SAR

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### 5.1 Energy Consumption for CDACs

For the purpose of illustrating the charge loss due to switching and to understand the energy requirements for a SAR ADC, 3 capacitors are used ( $C_o$ ,  $C_m$  and  $C_p$ ).  $C_m / C_p$  are the sum of the static capacitances connected to ground/ $V_{ref}$  which are not switched during the n-th cycle. Figure 5.1 illustrates the simple case when the bottom plate of the capacitor  $C_o$  is switched from ground to  $V_{ref}$ . The change in the voltage  $V_x$  for the n-th cycle can be calculated using the principles of charge conservation as:

$$V_x[n] = V_x[n - 1] + V_{ref} \frac{C_o}{C_o + C_m + C_p} \quad (5.1)$$

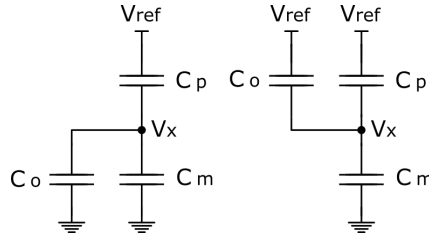


Figure 5.1: Capacitive switching energy consumption

Furthermore, the energy required to charge each individual capacitor connected to the reference of interest can be calculated as:

$$E_{ref}[n] = -V_{ref} [(Q_{C_o}[n] - Q_{C_o}[n - 1]) + (Q_{C_p}[n] - Q_{C_p}[n - 1])] \quad (5.2)$$

$$E_{ref}[n] = -V_{ref} [C_o (V_x[n] - V_{ref}) - C_o (V_x[n-1] - 0)] - \\ -V_{ref} [C_p (V_x[n] - V_{ref}) - C_p (V_x[n-1] - V_{ref})] \quad (5.3)$$

After substituting 5.1 into 5.3, the energy  $E_{ref}[n]$  consumed while switching the capacitance is given by:

$$E_{ref}[n] = \frac{C_m C_o}{C_o + C_m + C_p} V_{ref}^2 \quad (5.4)$$

## 5.2 Aligned Switching

The focus in recent years for SAR ADCs has been the implementation of efficient switching schemes. The amount of energy consumed in a conventional scheme can easily increase with the increase of the sampling frequency, which means that any design should take into consideration a suitable implementation. One very efficient technique is named aligned switching. As can be seen in Figure 5.2(a), the conventional successive switching approach gives the following energy calculations for the first transition  $E_1$  and for the second transition  $E_2$ , based on the previously derived equation 5.4:

$$E_1 = \frac{2C \cdot (C + C)}{4C} V_{ref}^2 = CV_{ref}^2 \quad (5.5)$$

$$E_2 = \frac{C \cdot C}{4C} V_{ref}^2 = 0.25V_{ref}^2 \quad (5.6)$$

$$E_{successive} = E_1 + E_2 = 1.25CV_{ref}^2 \quad (5.7)$$

Assuming that the transition is made directly to the final position as shown in 5.2(b), the total energy can be derived as:

$$E_{aligned} = \frac{(2C + C) \cdot C}{4C} V_{ref}^2 = 0.75CV_{ref}^2 \quad (5.8)$$

By comparing  $E_{aligned} = 0.75CV_{ref}^2$  with  $E_{successive} = 1.25CV_{ref}^2$ , it can be



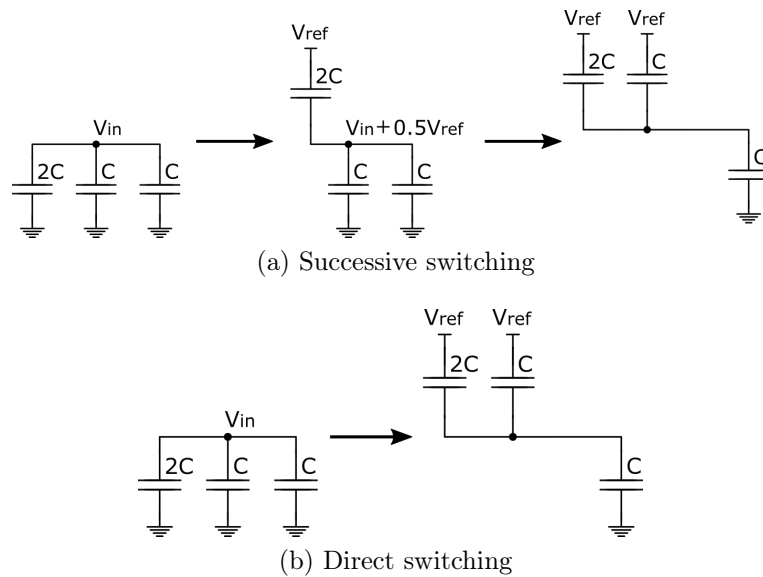


Figure 5.2: Aligned switching basic principle

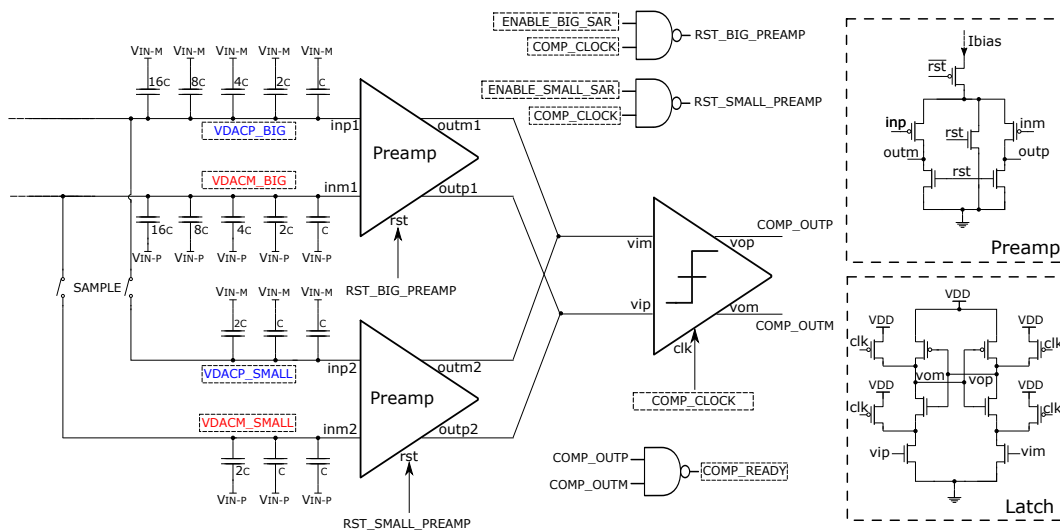
clearly concluded that aligned switching can save significant power if the technique is applied for the case of the MSB capacitors of a SAR ADC.

### 5.3 Detect and Skip Switching

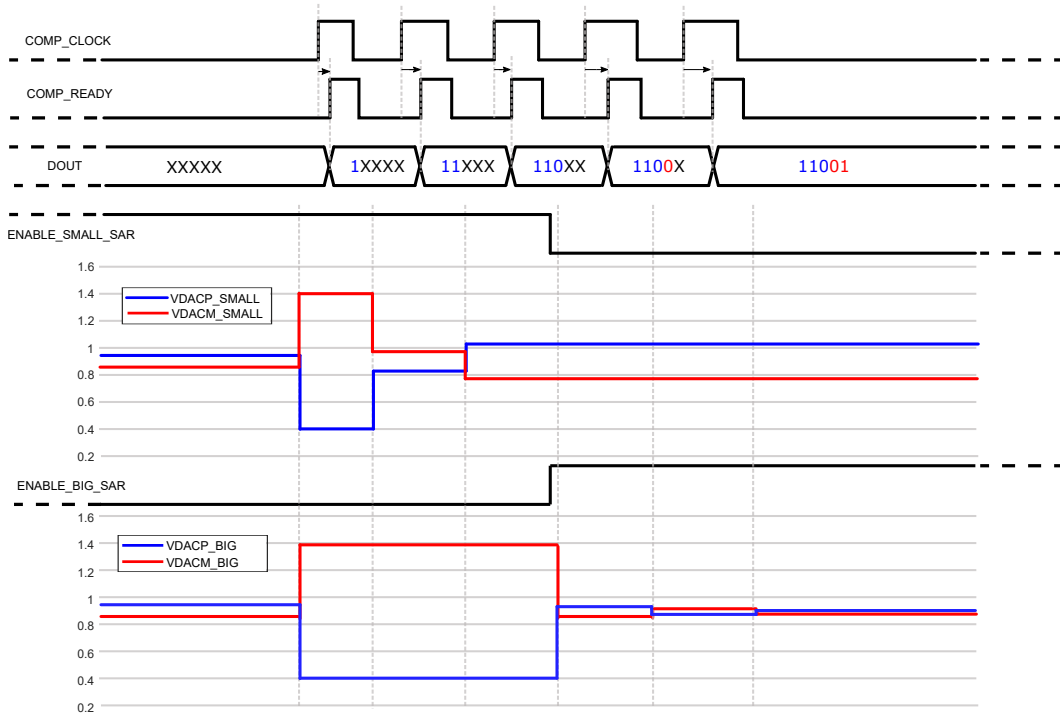
Another technique called Detect and Skip [21] has been adapted for this architecture. The main difference is that this application uses bottom plate sampling, whereas the previous designs exploited a top sampling scheme. The idea is to use one small CDAC for computing the MSB decisions which are decoded in order to implement the aligned switching and detect and skip algorithms.

Consequently, it is possible to decode the results of the smaller SAR Figure 5.4 and directly compute the switching of the large capacitors of the big SAR, saving power and reducing the settling time in comparison with a conventional scheme where the designer has to guarantee that sufficient time is allocated for settling before enabling another comparison. Furthermore, the comparator is a simple implementation of a Strong Arm comparator which is preceded by 2 preamplifiers, each connected to the top plates of the small/big

### 5.3. Detect and Skip Switching



(a) Circuit implementation



(b) Timing Diagram

Figure 5.3: Energy efficient SAR implementation

CDACs. The simple operation of disabling the preamplifiers when no conversion is needed results in the possibility of sharing the same Strong Arm

latch as can be seen in Figure 5.3(a). Besides this optimization of sharing the logic, having 2 preamplifiers is useful for mitigating any strong kickback from the latch.

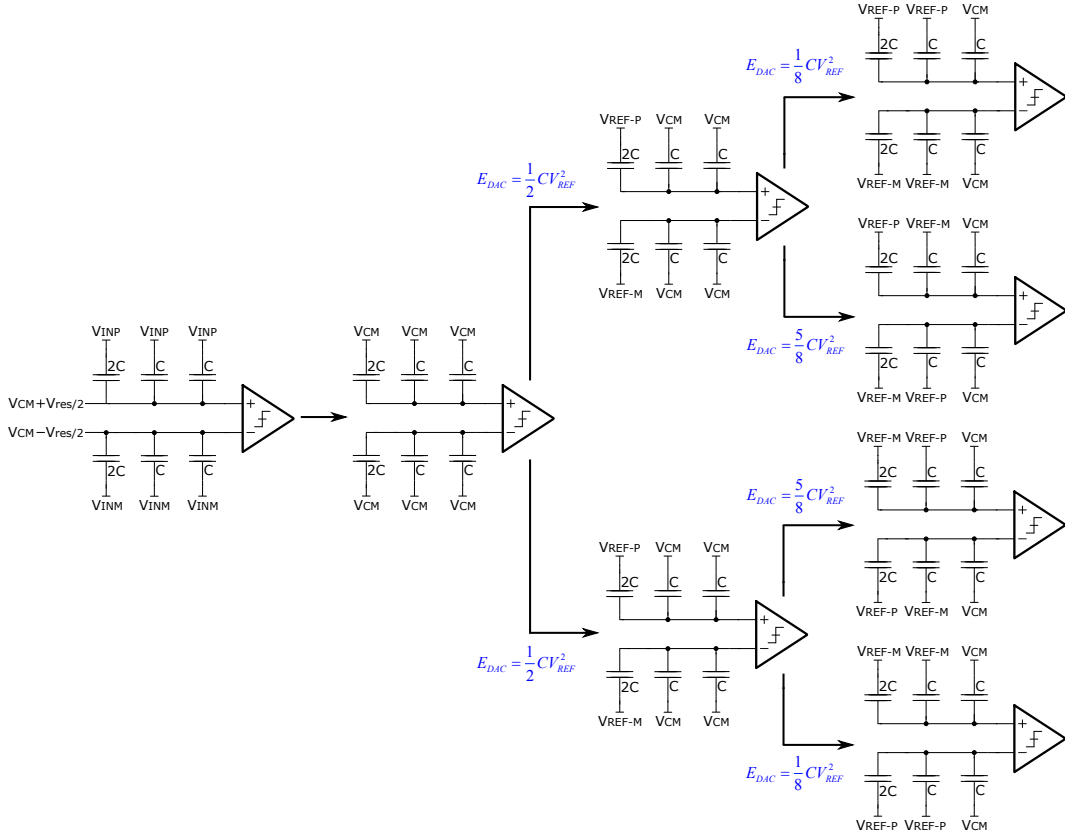


Figure 5.4: Aligned switching based on small SAR

Additionally, the small SAR switching exploits another well-known switching scheme called merged capacitor switching (MCS), which was also initially designed for top plate sampling based ADCs. The idea is to use the common mode voltage as a third reference and to be able to compute the MSB by switching all the capacitors to the VCM voltage. While this won't require any energy consumption (assuming parasitics are low enough), it has the inherent advantage of computing the MSB directly [22].

Moreover, in comparison with other switching schemes, this one takes full advantage of a fully differential CDAC array where the same weight oppo-

site polarity capacitors are connected either both to VCM or each one to the opposed reference as a function of what was the result of the previous comparison[23]. Consequently, this means that there is no need to use an additional high power voltage reference during conversion since the charge is provided directly from the charge redistribution of the symmetrical array.

## 5.4 Decoding Algorithm for MSB decisions

Lastly, Figure 5.5(a) shows exactly the mapping of the Small SAR decisions and how to switch the MSB capacitors in the larger SAR after finding the 3 values corresponding to MSB, MSB-1, and MSB-2.

The decoding scheme algorithm is also shown in Figure 5.5(b), where it can be seen that the small SAR bits are circular shifted to the left by one position.

This operation is required in order to redistribute the charge of the large SAR and to continue the successive approximation algorithm. Depending on the value of the small SAR computed MSB, if it is 0 then all small SAR VREFP connections are mapped with VCM connections in the big SAR or if the MSB is 1 all small SAR VREFM connections are mapped with VCM connections. Furthermore, for more details about the skipping algorithm, the reader is encouraged to check [21].

The basic idea of the algorithm is to compare the MSB with all the following bits and decide if that bit should be switched or should be skipped. For example, if MSB MSB-1 are 01 or 10, the switching of MSB-1 is skipped, but if MSB MSB-1 are 00 or 11, the switching is carried out. In the end, the final residue will be found on the same interleaved pair of dummy capacitors, which shows that there is no disadvantage in using a bottom plate sampling based Noise Shaping SAR in combination with an energy efficient scheme.

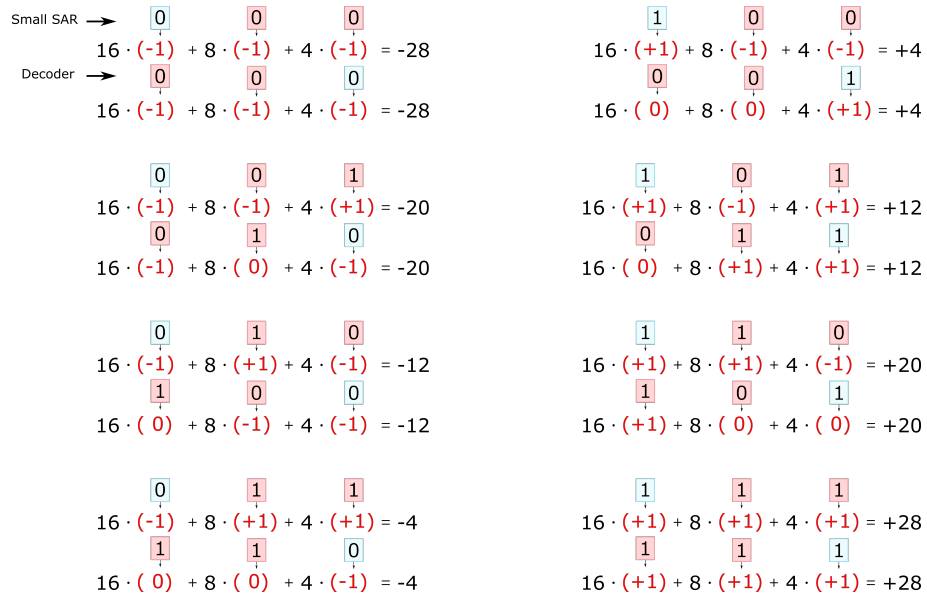
The timing diagram of the decoding is shown in Figure 5.6.

Finally, in order to further reduce the area and power consumption, the digital logic is custom made and is not synthesized with a hardware descrip-

## 5.4. Decoding Algorithm for MSB decisions

MSB (small) decision	MSB-1 (small) decision	MSB-2 (small) decision	MSB (big) connect to	MSB-1 (big) connect to	MSB-2 (big) connect to
0	0	0	VREFM	VREFM	VREFM
0	0	1	VREFM	VCM	VREFM
0	1	0	VCM	VREFM	VREFM
0	1	1	VCM	VCM	VREFM
1	0	0	VCM	VCM	VREFP
1	0	1	VCM	VREFP	VREFP
1	1	0	VREFP	VCM	VREFP
1	1	1	VREFP	VREFP	VREFP

(a) Mapping of Small SAR decisions



(b) Illustration of decoding process

Figure 5.5: Decoding algorithm

tion language. A domino logic (Figure 5.7) carries out the asynchronous sequencing of the switching based on the *COMPREADY* signal from the comparator (Figure 5.3) and generates the digital bits and control signals necessary for decoding and switching the capacitors in the main CDAC.

## 5.4. Decoding Algorithm for MSB decisions

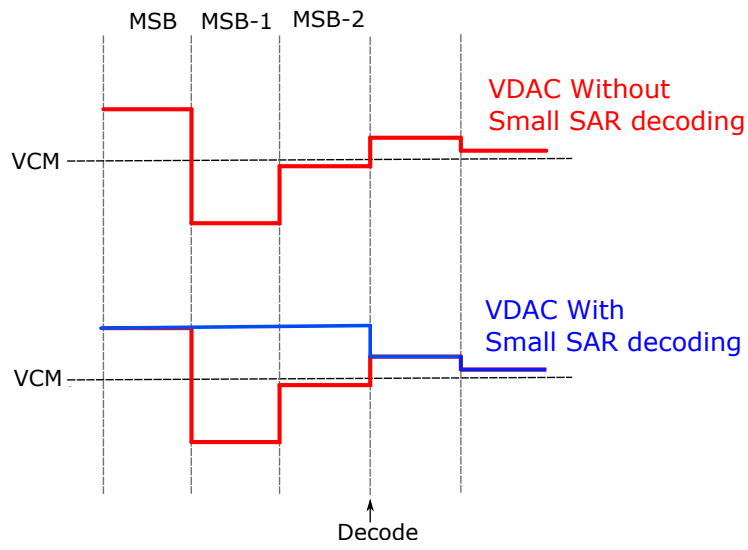


Figure 5.6: Timing diagram of decoding scheme

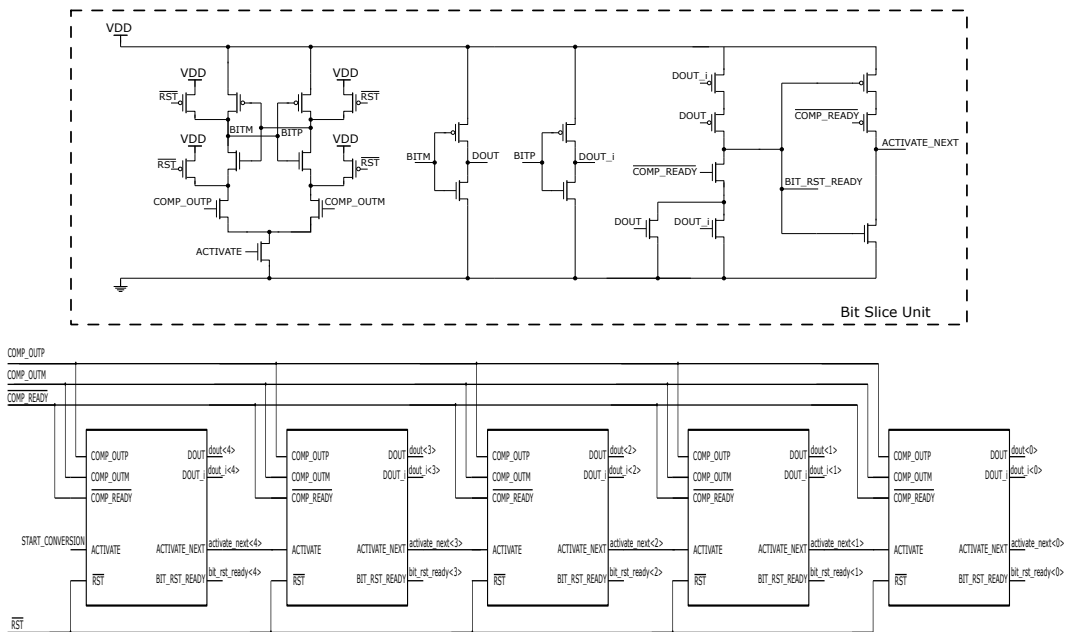
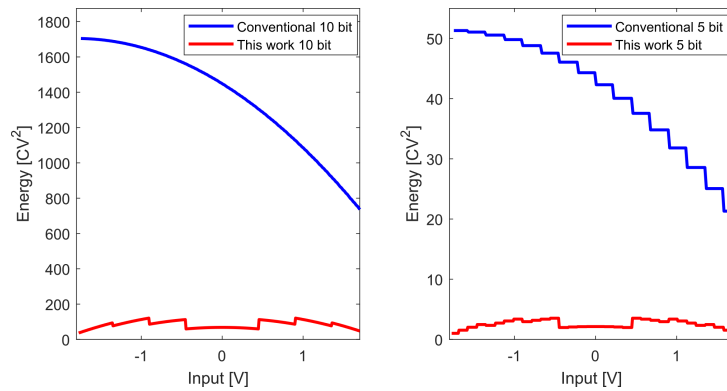


Figure 5.7: Domino Logic and Bit Slice Unit

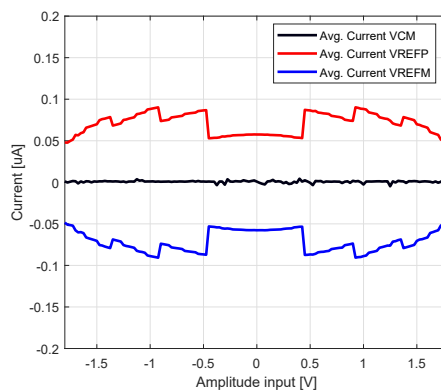
## Chapter 6 Simulation Results

### 6.1 Power Savings

As can be seen in Figures 6.1 (a) and (b), the Matlab simulations are in a good agreement with the average current extracted from Cadence simulations. The implemented switching scheme achieves a 96% improvement in energy efficiency in comparison with a conventional switching scheme.



(a) Matlab Simulation



(b) Cadence simulation

Figure 6.1: SAR energy consumption for different switching schemes

Finally, Matlab based estimations on the power efficiency of different configurations of bits for the small SAR and the big SAR are shown in 6.2. There is a significant rise in energy consumption when the number of small SAR bits increases and therefore confirming the benefits of using techniques such as Aligned Switching or Detect and Skip Switching [24].

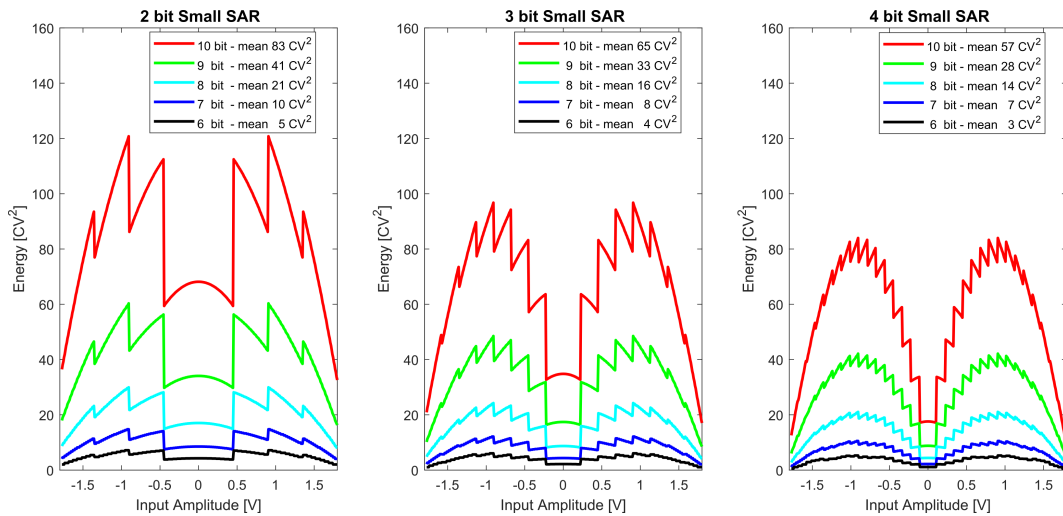


Figure 6.2: Energy efficiency comparison for different configurations of SAR capacitive arrays

## 6.2 CDAC Linearity

The performance of the ADC is defined by both static (DC) and dynamic (AC) specifications. Although a final 5-bit configuration is implemented, it is still necessary to understand how a new switching scheme can affect the linearity of the ADC, in order to set a path for possible projects where the architecture might benefit due to technology scaling and if a larger number of bits can be chosen. In order to express the linearity of a transfer function, the integral nonlinearity (INL) and differential nonlinearity (DNL) are two important parameters which give a statistical viewpoint of the static characteristics and are defined as:

$$DNL = \frac{A(i+1) - A(i)}{A_{LSB}} - 1, \forall i = 0..(2^N - 2) \quad (6.1)$$



$$INL(i) = \frac{A(i) - i \cdot A_{LSB}}{A_{LSB}}, \forall i = 0..(2^N - 1) \quad (6.2)$$

, where  $A(i)$  in an analog to digital converter stands for the the ideal transition point spaced by 1 LSB.  $DNL(i)$  offers a measure of the deviation of each code from the ideal  $A_{LSB}$  value (Figure 6.3(a)), while  $INL(i)$  gives an insight over the deviation of the transition code from its ideal location (Figure 6.3(b))

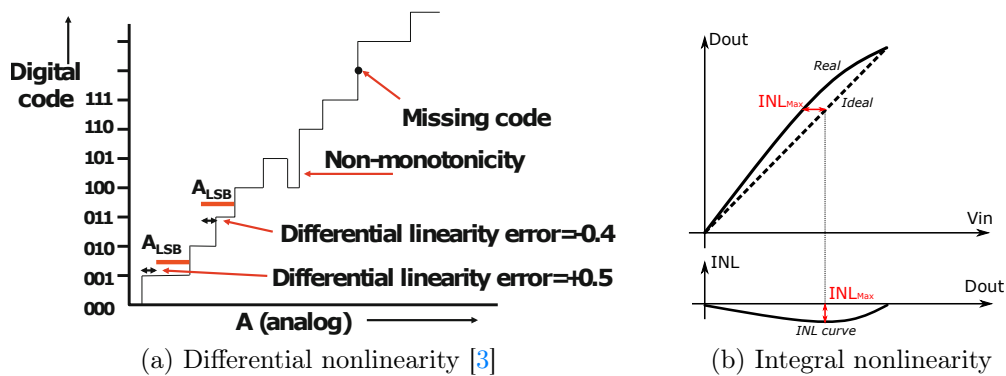


Figure 6.3: Static linearity effects

One critical aspect which needs to be verified for any ADCs used in control feedback loops or instrumentation applications is the monotonicity: the output increases when the input increases but never changes sign. (Figure 6.3(a)). If  $|DNL| < 1LSB$  then the ADC is guaranteed to be monotonic, but it can still have missing codes.

In order to demonstrate the linearity of the switching scheme, the real standard deviation (200aF) of the unit capacitor of 6fF is extracted from a Cadence Monte Carlo simulation as seen in Figure 6.4.

The transfer function for a 5 bit SAR using the implemented switching scheme is shown in Figure 6.5. The mismatch is exaggerated, but it is only to illustrate that the sensitive points of the transfer function. The middle code point will always have the minimum INL since it corresponds to the conversion starting point where all capacitors are kept to the VCM and any transition to the left or to the right corresponds to switching of capacitors with smaller error contributions.

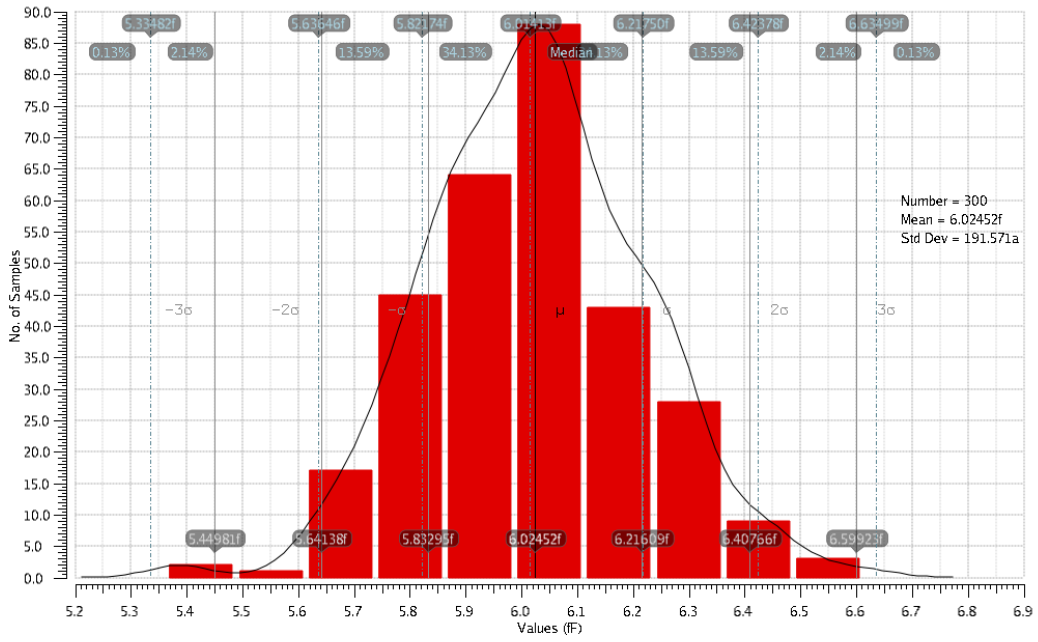


Figure 6.4: Monte Carlo simulation for unit capacitor

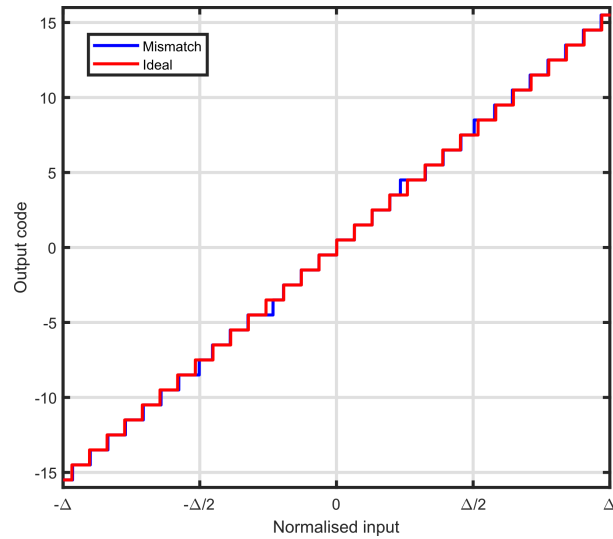


Figure 6.5: Transfer function linearity

In order to make a comparison, an end-point worst case code density testing of 5 bit/10 bit configurations for conventional (Figure 6.6) and implemented (Figure 6.7) switching schemes are shown. By using an end-point approximation instead of the best fit line, gain error and offset are removed, but illustrate worse values for INL and DNL. From a first view, it can be seen that a 10-bit implementation can actually have worse INL and DNL than for the case of a conventional switching scheme. Moreover, the codes for the worst statistical DNL can be identified on the exaggerated mismatch transfer curve shown in Figure 6.5.

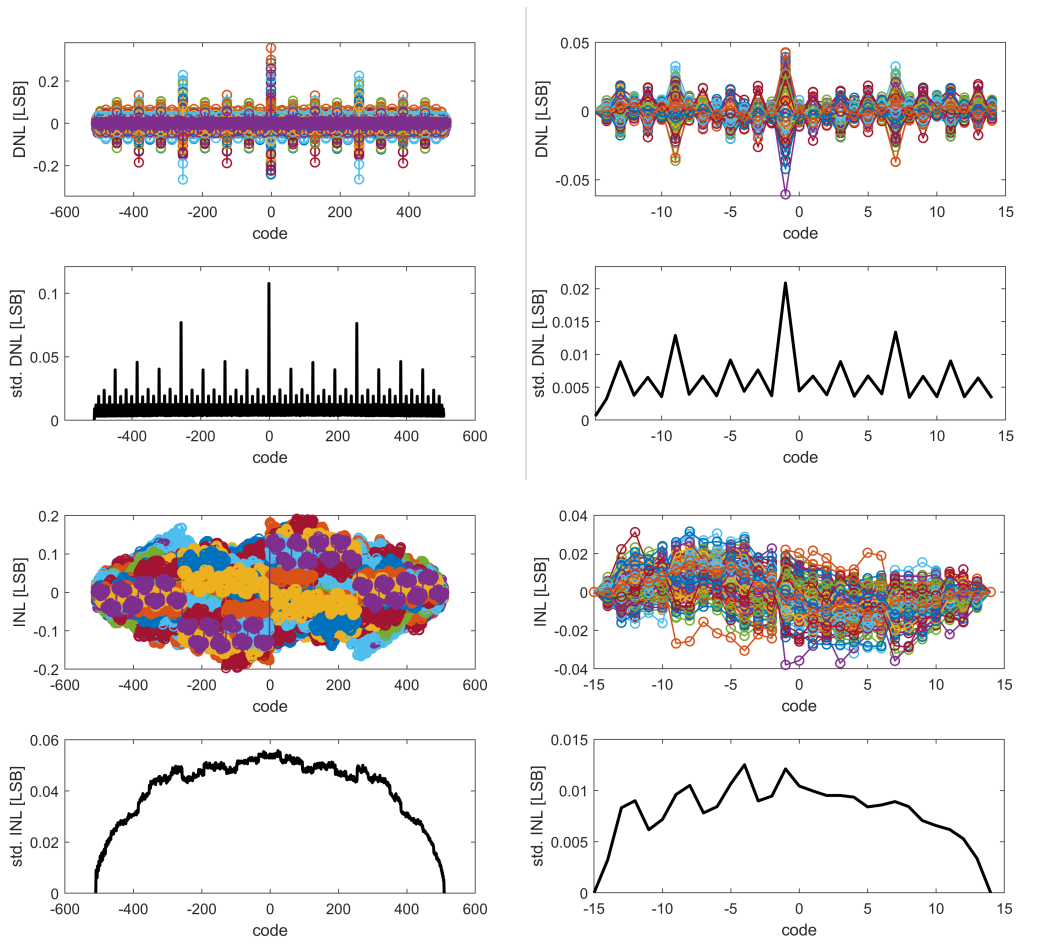


Figure 6.6: Conventional Scheme INL and DNL - 10 bit (left) and 5 bit (right)

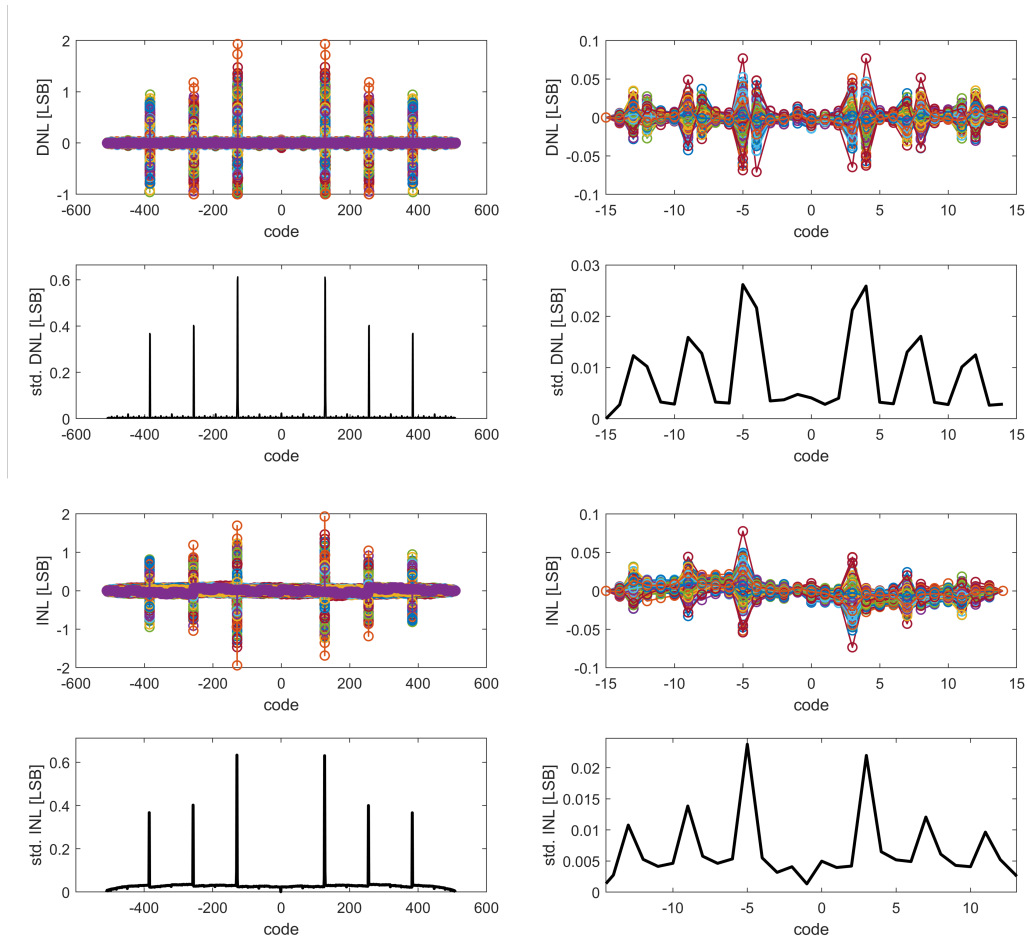


Figure 6.7: Implemented Scheme INL and DNL - 10 bit (left) and 5 bit (right)

Since any design has some weak points, it can be seen that a 10-bit implementation of the switching scheme will have a  $DNL > 1$  LSB, which means that monotonicity can't be guaranteed for a 10-bit implementation with the current sizing. However, this clearly illustrates the benefit of implementing a noise shaping SAR: using smaller CDAC can reduce the calibration complexity. Note also the sinusoidal pattern of the INL, which shows that a third harmonic distortion term appears if a sinusoidal input is applied to the transfer curve which can be verified by looking at the spectrum.

However, the static characterization is suitable mostly for data converters

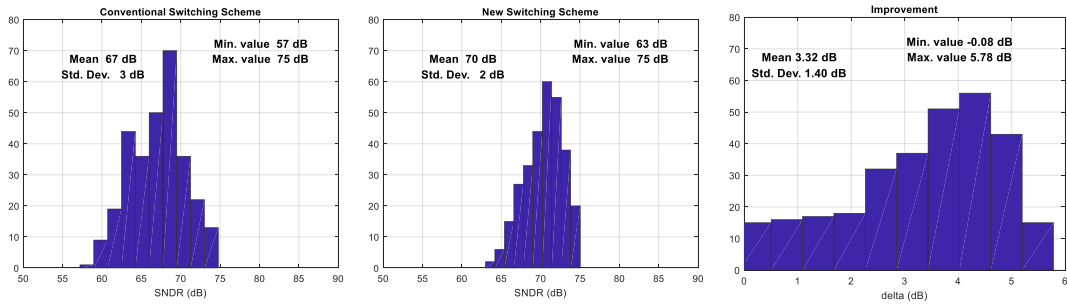


Figure 6.8: Comparison of schemes - dynamic linearity

that have DC input signals, which is not the case for the application of this design. Therefore, after running simulations in the time domain, it can be seen in Figure 6.8 that the ADC can actually improve the dynamic linearity performance of the ADC by about 6dB, for the case of a 5 bit Noise Shaping SAR implementation.

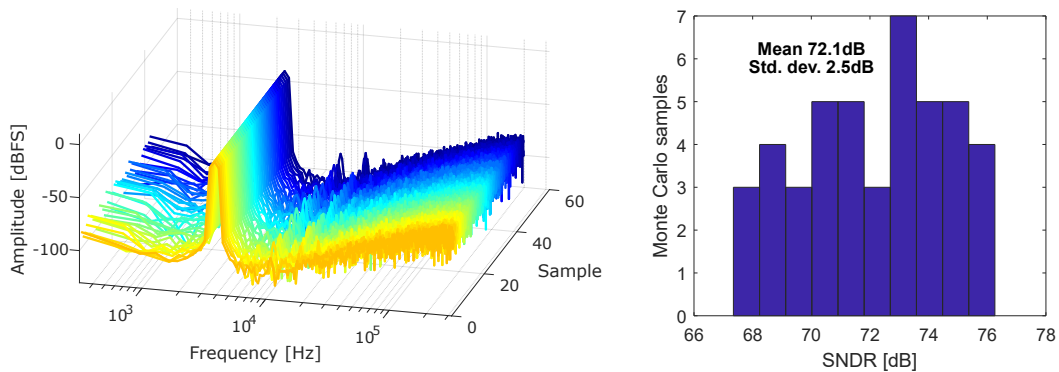


Figure 6.9: Histogram and FFT for Cadence Monte Carlo simulation

Furthermore, Matlab simulations of the switching scheme linearity are verified with Cadence Matlab simulations as shown in Figure 6.9, where the histogram depicts a 72.1dB mean (for Matlab it is 70dB) and a 2.5 dB standard deviation (for Matlab it is dB). As a conclusion, both Matlab and Cadence approximate similar effects of the capacitor mismatch over the linearity of the ADC.

### 6.3 2<sup>nd</sup> Order NSSAR Dynamic Performance

In order to show the limitations given by the OTA for a 2<sup>nd</sup> order NSSAR, Figure 6.10 illustrates a sweep of the current of the OTA and a sweep of the OSR ( $f_s = 0.5\text{MHz}$ ). It can be seen that for the case of the 2X OSR ( $f_s = 1\text{MHz}$ ), the dynamic error is dominant for low bias currents and that the quantization noise limit is much higher. However, for the 1x OSR, the design is limited by both quantization error and noise. Not to mention the 0.5 X OSR which is completely limited by the quantization noise. As a consequence,  $f_s = 1\text{MHz}$  corresponding to 2X OSR seems to be an optimum point. However, this comparison didn't include energy consumption. By extracting the energy consumption of the ADC for different frequencies, the final Walden Figure of Merit ( Figure 6.10) starts to increase due to the fact that more power is consumed, while the design is still limited by thermal noise (only 3dB increase for 2x increase in OSR).

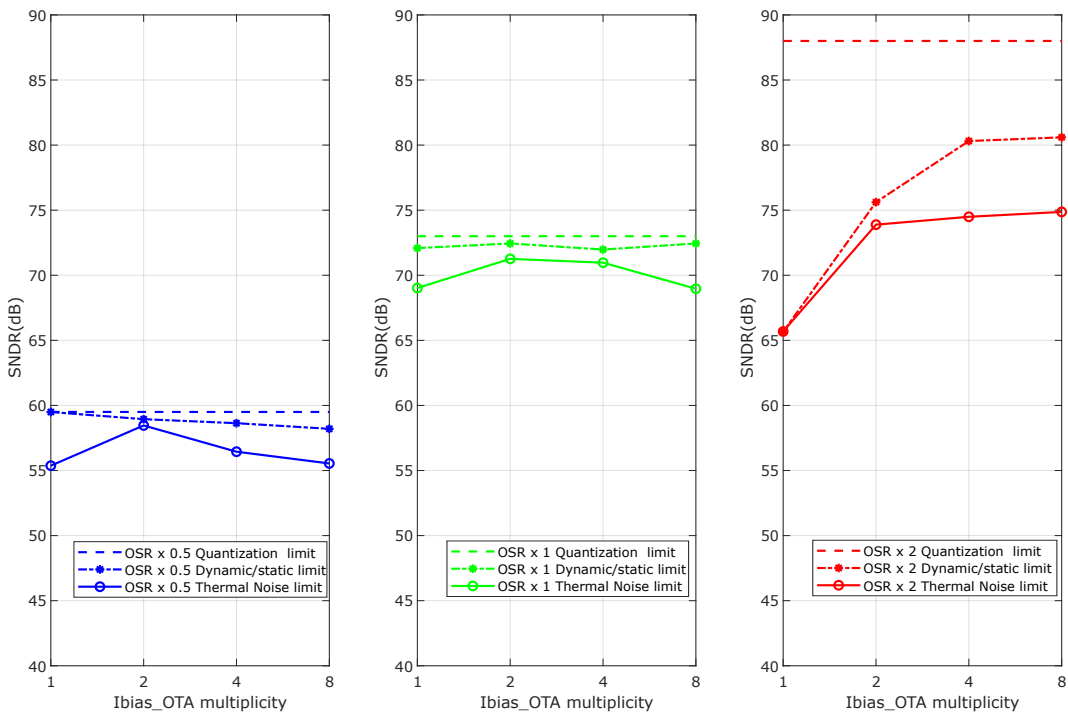


Figure 6.10: Design limits of OTA

## Chapter 7 Conclusions

### 7.1 Benchmarking

The energy efficiency of the NSSAR is improved by implementing techniques such as aligned switching, detect and skip switching and merged capacitor switching. The comparison between the implemented scheme (total power consumption of  $11 \mu\text{W}$ ) and the conventional one (total power consumption of  $25 \mu\text{W}$ ) is shown in Figure 7.1. The switching scheme improves the power consumption of the ADC by 2x for a sampling frequency of 1MHz.

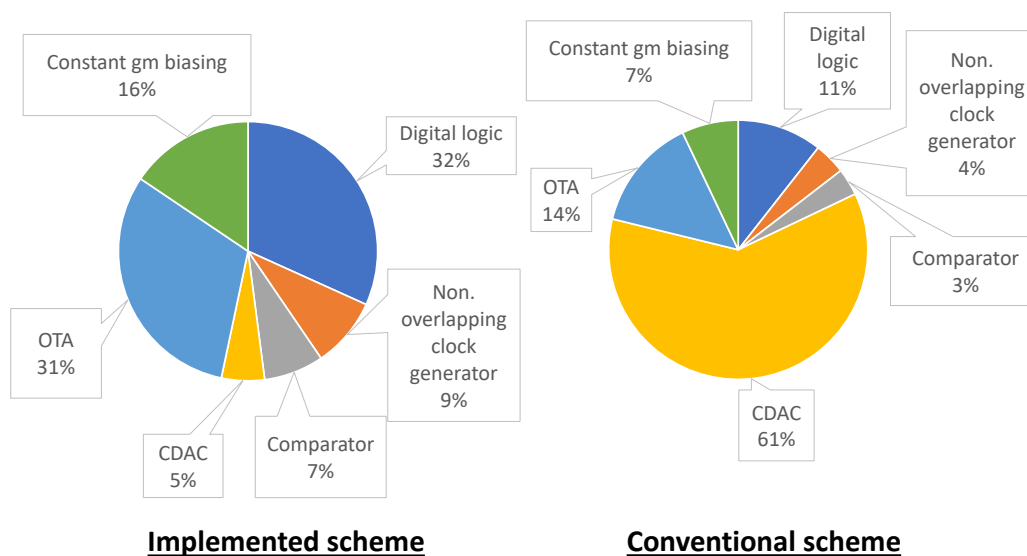


Figure 7.1: Power budgeting comparison pie chart  $F_s$  1MHz

The implementation of the energy efficient 2nd order Noise Shaping SAR has been simulated in Cadence. During the final step of the design, it has been discovered that a kickback from the dynamic amplifier can affect the constant gm biasing, therefore, it is necessary to properly isolate any kick-

back from the active circuits to the biasing. Figure 7.2 shows the performance of the design for different sampling frequencies. Although the best Walden FOM is obtained for Fs around 0.5 MHz, this means that the design is limited by quantization error and not by thermal noise. As a consequence, the sampling frequency of 1MHz is the optimum design point.

The following table illustrates a performance survey on some of the relevant Noise Shaping SAR architectures. It can be seen that the use of a 2<sup>nd</sup> order noise shaping SAR with zero optimization for the NTF can give significant improvement for a Figure of merit which includes the Area, the technological process and FOM of Walden (resolution and energy efficiency). However,

Specifications	Obata[10]	Shu[9]	Guo[11]	Li[12]	This work
Process [nm]	28	55	40	40	140
Supply [V]	1.8/1.1	1.2	1.1	1.1	1.8
NS order	3	1	2	2	2
Area [ $mm^2$ ]	0.116	0.072	0.04	0.024	0.01
BW [kHz]	2	1	262	625	20
Fs [MS/S]	1	1	8.4	10	1
OSR	25	500	16	8	25
SNDR [dB]	98	101	80	79	71
Power [uW]	493	15.7	143	84	11
FoMs [dB]	170	179	173	178	164
FoMw [fJ/step]	143	85	33	9	98
FoMw $\cdot \frac{\text{Area}}{\text{Process}}$	0.592	0.111	0.033	0.0054	0.007
NTF zero optimization	No	No	No	Yes	Yes

Table 7.1: Comparison with state of the art

Figures 7.3 (a) and (b) show the Energy efficiency and the FOM Walden of the NSSAR design with respect to other ADCs [1].



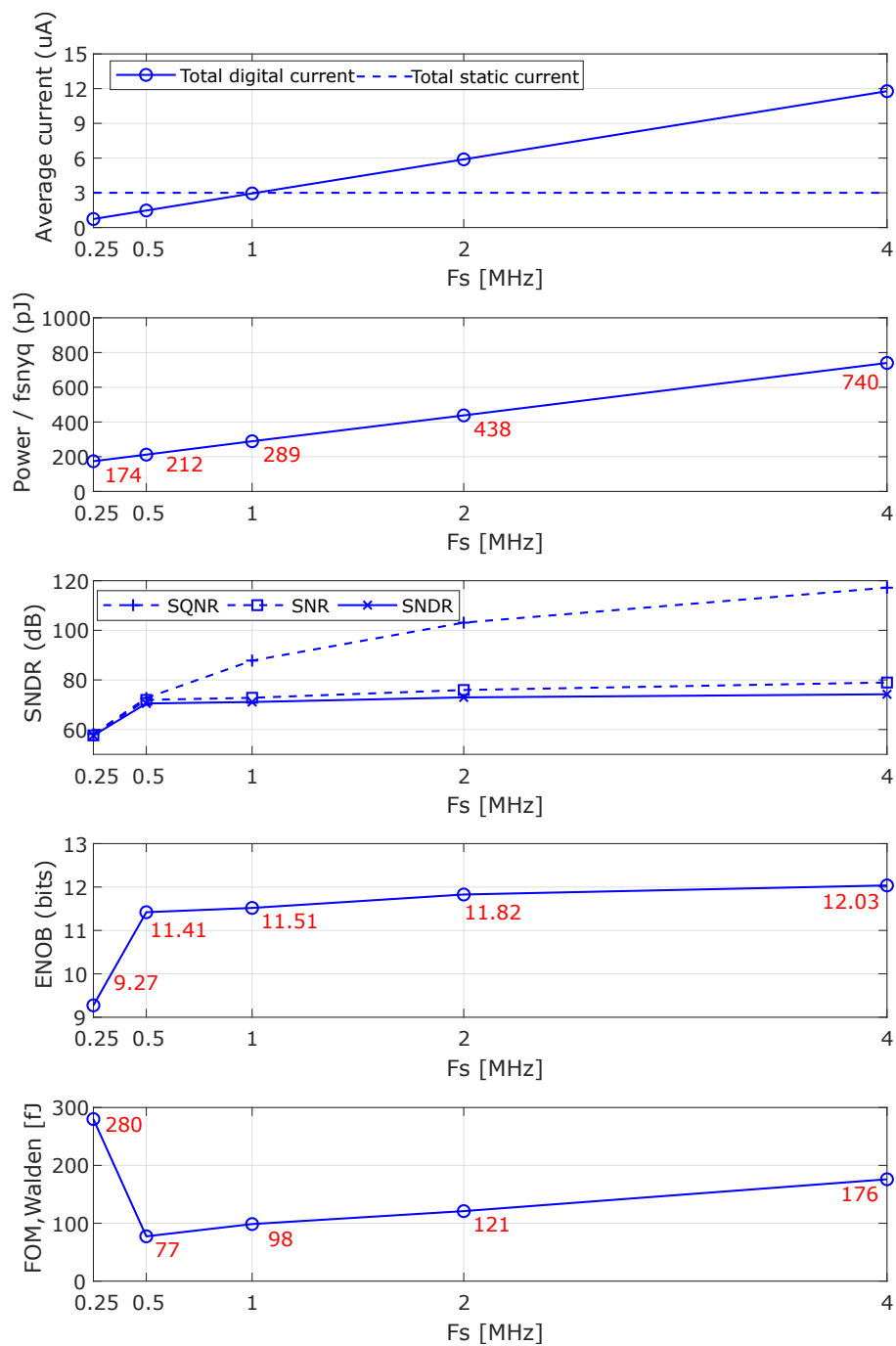


Figure 7.2: Figures of merit vs. sampling frequency

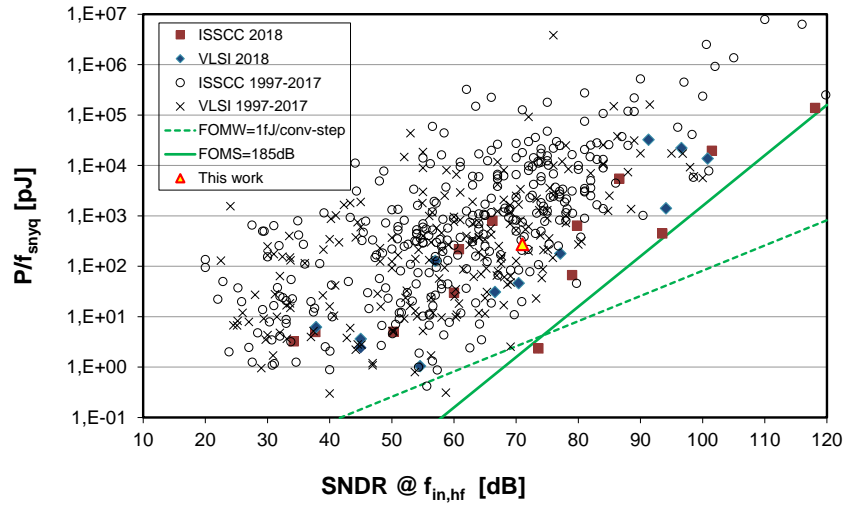
The main difference between this design and the state of the art NSSARs is that it is designed to be integrated in a system such as a Zoom ADC, where a high resolution and energy efficient coarse stage can improve the performance of the overall hybrid subranging ADC. Although for a sampling frequency of 0.5MHz, the NSSAR achieves a Walden FOM of 77 fJ/conv-step , a higher sampling frequency is necessary such that the ADC is thermal noise limited and not quantization noise limited. Usually, for the case of audio applications, the quantization noise level should be at least 20 dB under the thermal noise level.

The main design challenge has been to find an architecture which requires a lower OSR (25) in comparison with other published Noise Shaping SAR architectures. This design manages to achieve the targeted ENOB of 11.5 bits while consuming 11  $\mu$ W for a sampling frequency of 1MHz and a BW of 20kHz.

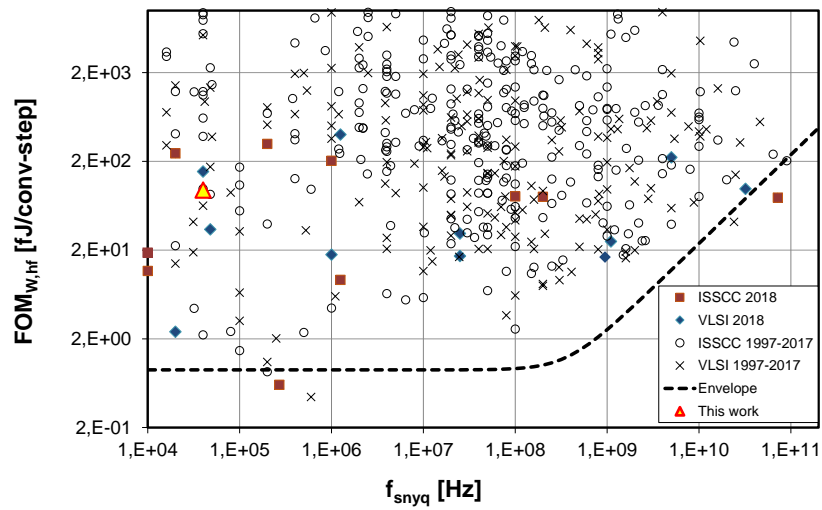
## 7.2 Original Contributions

This thesis has shown that a second order Error Feedback Noise Shaping SAR is a suitable architecture which can significantly increase the performance of a two step ADC when a nonlinear fine quantizer is used. Matlab simulations were carried out and it has been shown that by introducing a 5 bit Noise Shaping SAR in the coarse stage of a Zoom ADC, the resulting residue will be less tonal and therefore it results in an effect similar to dithering (residue is similar to white noise). The final output of a Zoom ADC was proven to have a significant improvement of Spurious Free Dynamic Range (SFDR) when the order of noise shaping is increased from first order to second order.

Furthermore, a new architecture of second order NSSAR has been implemented by adapting the error feedback topology (usually implemented only in the digital domain) and optimizing it for maximum performance. More-



(a) Energy efficiency



(b) FOM Walden

Figure 7.3: Figures of Merit [1]

over, the error feedback implementation of an FIR filter in combination with a power efficient current reuse OTA enables an optimum placement of the notch filter in order to suppress in-band quantization noise.

Moreover, techniques such as detect and skip or aligned switching have been analyzed and adapted to the current architecture which uses a bottom plate sampling technique although most power efficient switching schemes use top plate sampling. The design achieves 96% savings in switching related energy consumption due to the procedure of decoding a small assisting SAR.

Finally, the circuit implementation was optimized considering circuit non-idealities such as capacitor mismatch, OTA dynamic and static errors, and thermal noise.

### 7.3 Future Work

The current design should be optimized in terms of energy efficiency by reducing the static power consumption. This can be achieved by implementing a dynamic amplifier without static current biasing such as ring amplifiers or comparator based amplifiers. Furthermore, solutions such as mismatch error shaping can be implemented for a higher configuration SAR in order to further improve the resolution of the ADC. Another solution would be to use a lower supply for the digital logic and therefore improve the energy efficiency of the ADC.

Finally, the 2<sup>nd</sup> order Noise Shaping SAR is a suitable candidate to be integrated in a hybrid ADC which can achieve both high resolution and power efficiency.

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