Noise and loss in superconducting resonators

By

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Abstract

Sub-mm astronomy in space calls for an array of photon noise limited detectors, both for imaging and broadband spectroscopy. Microwave Kinetic Inductance Detectors (MKIDs), superconducting resonance circuits, are a suitable candidate for this purpose due to its multiplexing potential, but in literature excess noise in phase readout is encountered and attributed to so-called two-level systems (TLSs). Reduction in TLS induced noise and loss will provide greater flexibility in design and a route towards background limited detector performance.

In this thesis, TLSs from surface and bulk sources are modelled, so that their behaviour can be predicted through numerical computations of the field distributions inside the resonators. These calculations not only provide a guide for sensible chip designs, but allow for interpretation of experimental data and determination of dominant TLS sources.

It is found that for Al CPW resonators on Si or SiN, the noise is surface dominated but with a non-negligible bulk contribution, while for microstrips on a SiN membrane, the noise is bulk dominated. As the loss in microstrips for narrow microstrips is dominated by the substrate-air interface, the dominant TLS loss and noise sources do not necessarily coincide and should be treated independently. This makes it impossible to determine the dominant CPW surface noise contribution. Additionally, microstrips and CPWs on the same dielectric perform similarly, while Si is better than SiN, both in terms of loss and noise, due to a combination of SiN interface and bulk effects. Finally, material dependent loss and noise parameters have been determined and the importance of thorough Si surface cleaning has been established, yielding the best Al CPW noise ever encountered.

For sub-mm astronomy in space, the logical path to improvement would be the use of thorough cleaned Si as a dielectric, overetching and the use of LEKIDS and hybrid resonators, where microstrips are still viable for use. Importantly, having located the important TLS locations for various cases, tackling these problems areas further could provide the step towards background limited performance in space.

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1 Introduction

1.1 Why sub-mm astronomy ?

To gain insight in the time evolution of the universe in terms of distribution of matter and large scale structure, one can trace back the light of galaxies from the present (redshift $z = 0$) to the end of the dark ages ($z \approx 7$), when matter reionized hundreds of millions of years after the Big Bang. However, as light from older galaxies originates from further away, this will also be fainter, more likely to be absorbed or scattered by dust and the interstellar medium and hence more difficult to observe in the visible and infrared bands. For this reason, surveys in these frequencies tend to favour nearby objects.

However, with increasing redshift the intensity peak of the galaxy spectrum also shifts towards longer wavelengths. If one then observes at low frequencies, such as the sub-mm band, the faintness of more distant objects is counterbalanced by the increase in brightness as the spectral peak enters the observing window. This ‘negative k-correction’ makes sub-mm astronomy particularly useful for surveys across a wide range of redshifts [1] and hence to create a 3-D map of the universe using z as a distant measure. Additionally, sub-mm astronomy also has the potential for studying star and planet formation [2].

The determination of z is most accurately done by detecting the frequency shifts of known spectral lines. These will typically be molecular rotational lines like CO, which is a very good probe for molecular gas [3]. In total, the International Astronomical Union identified 38 important spectral lines in the $100\,\mathrm{GHz} - 810\,\mathrm{GHz}$ range [4]. The downside of this method is that a high spectral resolution is necessary. As explained in [5], for this frequency range the ground-based Atacama Large Milliimeter Array is well suited, while in space another heterodyne instrument, HIFI (on Herschel), has operated in the lower half of this frequency range, but both have limited instantaneous frequency bandwidth. This means that a broad-band spectrometer capable of having a large bandwidth while containing many pixels and frequency bins is a solution to efficiently cover the sub-mm frequency range to find the desired spectral line.

Additionally, there is the necessity for detectors that are easily multiplexed into imaging arrays with large fields of view. These can swiftly locate the sub-mm sources whose redshift should be determined. Examples of these imaging arrays are NIKA (356 pixels, operational), NIKA-2 (5000 pixels, expected to start in 2015) [6] and A-MKID (up to 25000 pixels).

The problem for directly detecting for sub-mm photons is that they carry little energy and their sources are still typically faint. Bolometers, detecting absorbed light through an increase in temperature, are sensitive enough but are very difficult to multiplex. This is not the case for semi-conducting devices but they not sensitive enough to be *photon noise limited*, i.e. a performance limited by the random flucutations from astronomical background sources. This motivate the use of Microwave Kinetic Inductance Detectors (MKIDS), which combine sensitivity with multiplexing capabilities by emplying superconductivity.

1.2 Use of superconductivity

After the first observation of superconductivity in metals by Kamerlingh Onnes in 1913, any theory on superconductivity attempted to phenomenologically describe the basic superconductive properties, such as zero resistance and the Meissner effect, until BCS theory in 1957 [7]. Under the assumption of a net attractive force between electrons, a sort 'bond' between electrons with pairing energy 2Δ could exist, creating 'Cooper pairs' [8]. These form the ground state in a superconductor. Intuitively, this attractive force can be envisioned as an electron passing through a lattice, which slightly attracts surrounding positive lattice ions. Another electron at a large distance, will then see a small, net attractive potential from the first electron as the negative electron charge is screened by the lattice [9]. However, this weak effect which causes superconductivity will only exist below a critical temperature T_c ($T_c < 0.6\Delta/k$ according to BCS theory [7]), in metals below a few Kelvin. This also means that a Cooper pair (the ground state) is easily broken into two quasiparticle excitations, which for some purposes may been seen as analogous to electrons, for example by an incoming photon with energy $hf > 2\Delta$, as illustrated in Figure 1.

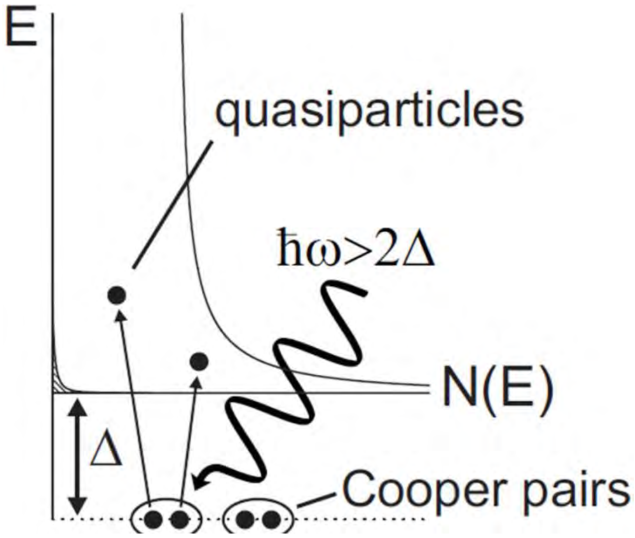

Figure 1 Illustration of pair breaking, figure from [10]. On the horizontal axis is the density of states, on the vertical is the energy. All Cooper pairs are situated at the ground state and at energies below Δ, no quasiparticles can exist. Above Δ, a small thermally induced number of quasiparticle excitations exist which can be accompanied by quasiparticles created by photons with energy greater than 2Δ breaking a Cooper pair.

With Al having a critical temperature as low as $1.17\ \mathrm{K}$ [11], photons require a frequency of $\gtrsim 80\ \mathrm{GHz}$ for pair-breaking, exactly at the low frequency end of the sub-mm range, which is what makes the use of superconductivity in sub-mm astronomy ideal. As will be explained in the next subsection, MKIDs are superconducting pair-breaking detectors, which operate at $T \ll T_c$ for minimum thermal noise in the number of Cooper pairs and quasiparticles. They employ an easily multiplexed method of operation which converts this pair-breaking to a measurable quantity.

1.3 MKIDS

1.3.1 Working principle

A MKID is a planar superconducting circuit structure composed of two planes on either side of a dielectric (microstrip) or three superconducting planes placed on top of a dielectric (CPW). This structures meanders to conserve space, see the top view on Figure 3 (left), while a cross-sectional view is presented in Figure 2. These circuits have a *geometrical* inductance, as well as a capacitance which is boosted by the dielectric.

Moreover, the inertia of the Cooper pairs gives rise to an inductance associated with their inertia, called the *kinetic* inductance L_{kin}. The kinetic inductance then depends on the number of Cooper pairs. In the two-fluid model, charge carries are divided into two categories, quasiparticles excitations and Cooper pairs. At $T \ll T_c$, Cooper pairs form by far the largest fraction of the total number of charge carriers, while quasiparticles form a minority. Cooper pairs can be broken by photons with $f > 2\Delta/h$. The result is an increase in inductance, as well as an increase in resistance originating from the increase in quasiparticles number. A MKID converts these consequences of pair-breaking into easily measureable quantities by having the superconductor in a resonance circuit, as shown in Figure 3 (right).

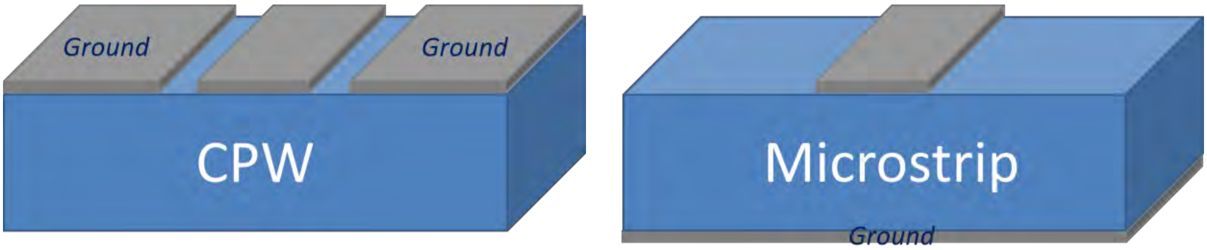

Figure 2 Schematic cross section of a CPW (left) and microstrip (right). The grey areas represent the superconductor, the blue area the dielectric.

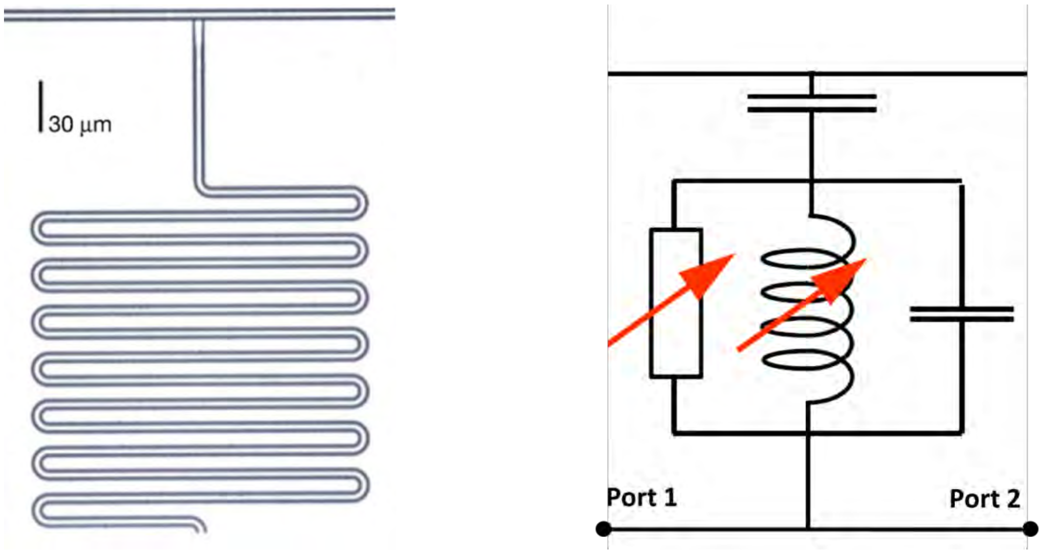

Figure 3 Left: Meandered CPW, connected to a signal line (straight line on the left), figure from [12]. In gray is the sapphire dielectric, in white is the aluminium superconductor.
Right: MKID electrical circuit equivalent, figure from [13].

The inductance and capacitance form a resonant circuit with resonant frequency f_{res}, which may be tuned by adjusting the length of the resonator. When incoming light changes L_{kin} , it changes f_{res} which is detected by probing the resonator with a readout signal. At f_{res}, analogously to a tuning fork, a standing wave exists which decreases the transmission heavily, creating a dip in the transmission from port 1 to port 2 as a function of frequency. Due to small losses, this dip is not a perfect delta peak, but has a Lorentzian profile with a sharpness represented by Q around f_{res}, which moves when light reaches the resonator, as seen in Figure 4 (left). The real and imaginary part of the transmission describe a circle in the complex plane and can then be converted to amplitude and phase, as described in [14] and seen in Figure 4 (right), which are the quantities that are actually measured.

Importantly, because the transmission dips at resonance are so narrow, it is easy to couple multiple resonators with slightly different lengths and hence slightly different f_{res} on the same readout line, while maintaining the ability to identify each dip to its corresponding resonator. This makes MKIDS ideal for Frequency Domain Multiplexing (FDM), an example of which can be seen in Figure 5.

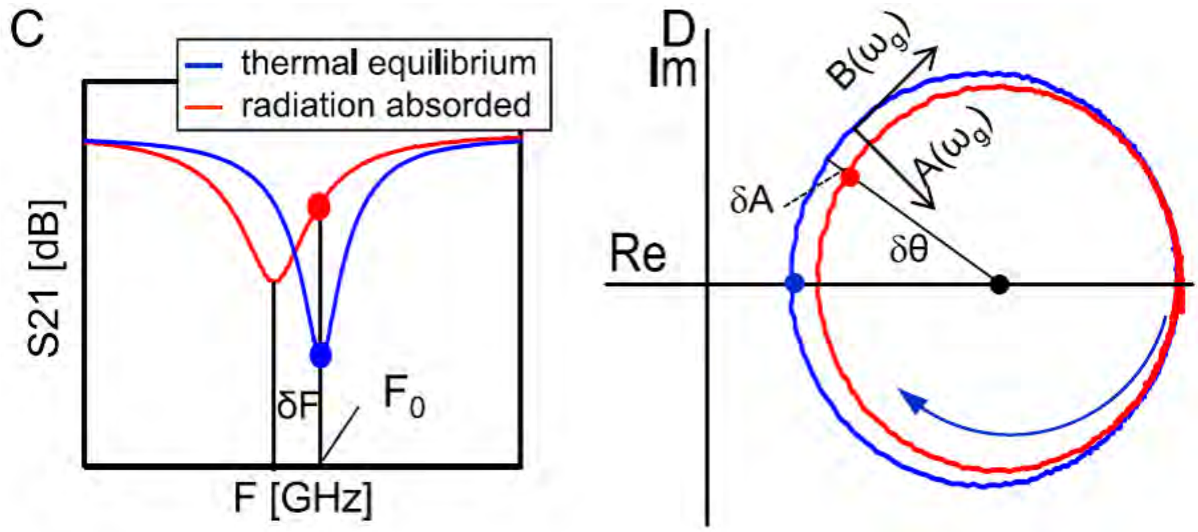

Figure 4 Figure from [13] showing the equivalence between frequency shift and phase and between transmission dip depth and amplitude in the complex plane respectively.

It is this multiplexing potential (up to 10000 detectors per signal line), together with the ease of fabrication of large arrays, that make MKIDs ideally suited for sub-mm astronomy, compared to other detectors like TES-bolometers (see [15] for a more extensive treatment on TES). There are also more benefits, such as relative ease of fabrication and not very stringent magnetic and temperature requirements while maintaining good sensitivity. An example of a full MKID array for imaging is shown in Figure 6, while the next subsection shows an example of how MKIDs are used to determine redshifts of galaxies to form a 3-D map of the universe as explained in section 1.1.

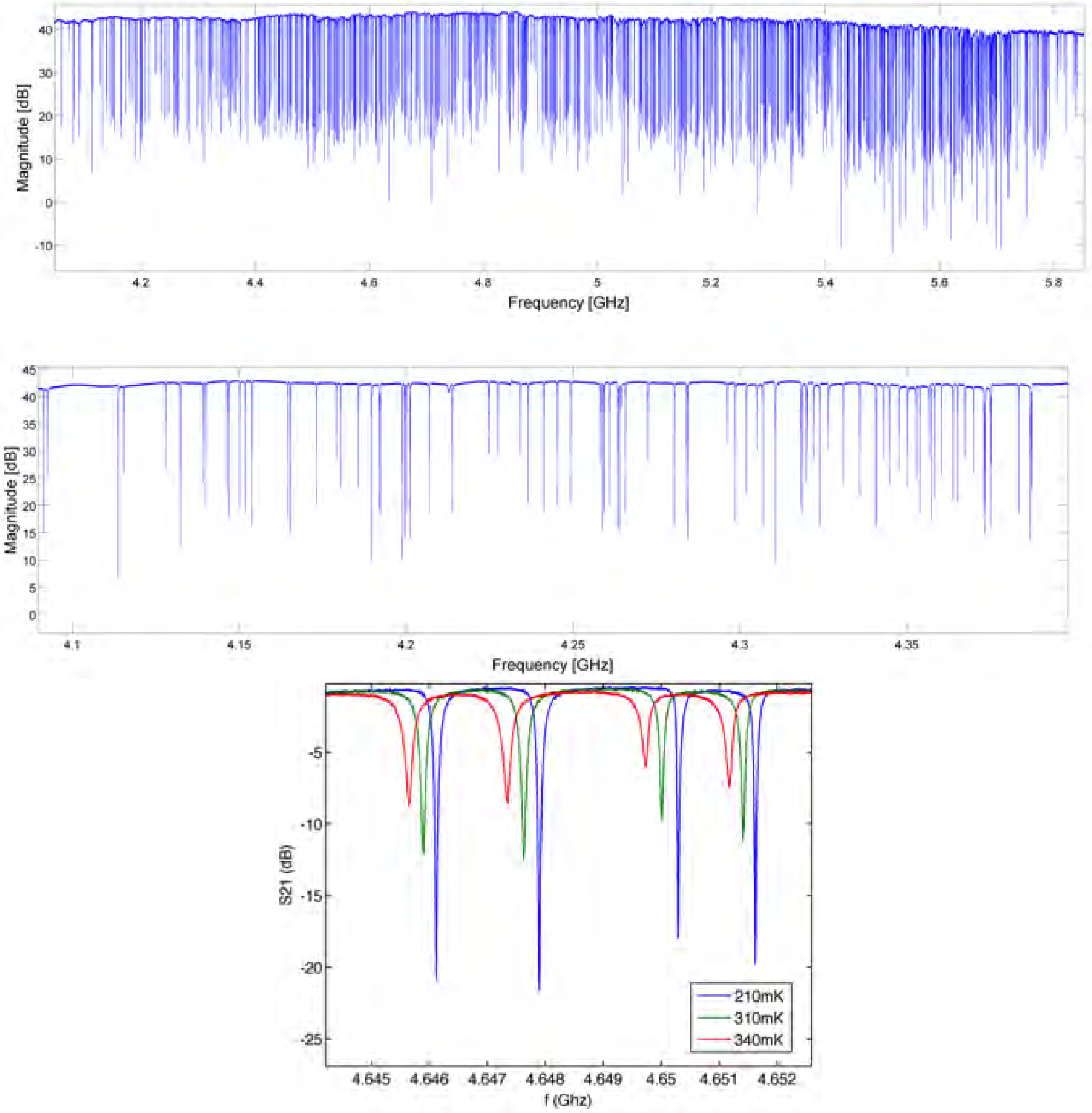

Figure 5 Example of frequency domain multiplexing (FDM) for MKIDS, figures from [16]. Top: Transmission as a function of frequency. Each dip corresponds to a resonator with a different resonance frequency. Bottom: Transmission versus frequency zoomed in around 4.65 GHz. As the dips are very narrow, spacing of the resonators can be on the order of MHz. Also visible are both the shift in f_{res} as well as the smoothing of the dip at higher operating temperatures.

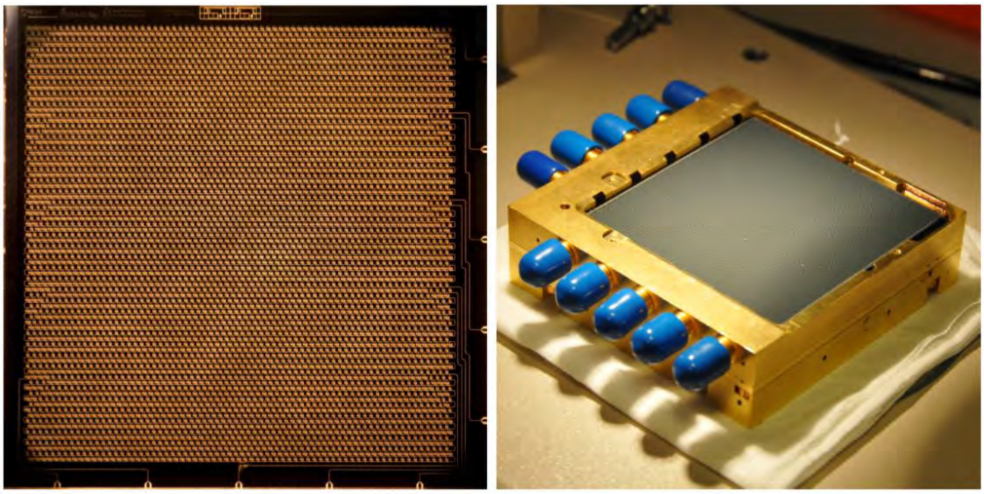

Figure 6 Imaging array example in A-MKID, where 5 transmission lines connect a total of 5400 detectors, figure from [11].

1.3.2 DESHIMA

A very promising project using MKIDS is DESHIMA [5], a spectrograph with both detectors (MKIDS) and filters (also superconducting resonators) on one chip, see Figure 7.

The sub-mm signal, received by the antenna, is transported in a signal line (a CPW). Coupled to this line is a superconducting resonator, NbTiN in Figure 7, which prevents further transmission along the signal line at a particular frequency, hence acting as a filter. This resonator is relatively short to give a f_{res} of around 600 GHz. This signal is preserved in the filter by using NbTiN which has a band gap frequency of 1.2 THz, so that the signal cannot break Cooper pairs. Coupling multiple resonators with slightly different lengths and f_{res} splits the signal into various frequency components. Coupling every filter to a MKID then provides a way of detecting how much light is at every frequency selected by the filters. The superconductor used in this MKID is Ta, which has a low band gap energy so that the signal is absorbed. By assigning different lengths an f_{res} to each MKID, their corresponding transmission dips can be identified when a probe signal is passed through the read-out line to which all MKIDs are coupled. It is essential for the frequency resolution that many KIDs can be multiplexed this way for each pixel, with a goal of at least $600/\text{pixel}$.

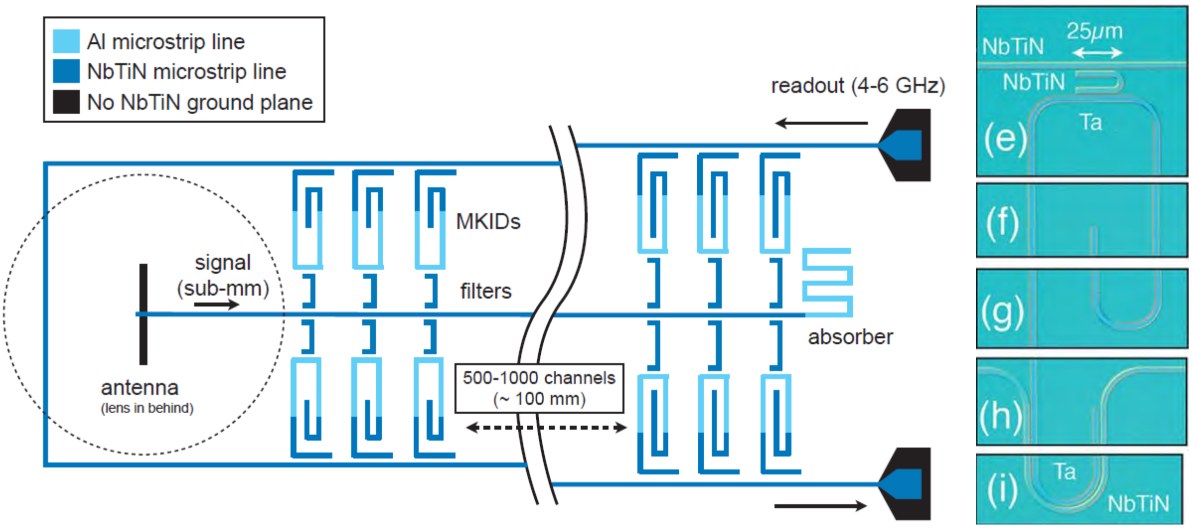

Figure 7 Left: Proposed design of DESHIMA, with the filters and MKIDS coupled to one signal and read-out line. Figure from [5]. Right: NbTiN superconducting resonator filter, coupled to a Ta (lower gap energy) MKID. Figure from [17].

1.4 Performance

Regarding the choice of geometry, microstrips would be the preferred option. The electric fields are better confined in microstrips as more of the field is concentrated in the dielectric, limiting cross-coupling between KIDs and hence allowing for a more closely packed array of resonators. This benefits both spectroscopic projects as DESHIMA, as well as imaging arrays which require as many pixels as possible. Furthermore, the smaller volumes of microstrips allow for measurements in the THz range, as there the light that passes through the lens onto the antenna gives a smaller diffraction spot, requiring smaller structures. Finally, microstrips provide better stray light rejection than for CPWs. Unfortunately, microstrips have stayed behind in performance compared to CPW in literature so far. To assess the problem, the relevant attributes of a detectors must be explained.

For the detection of resonance frequency shifts, two properties are important: the sharpness of the resonance peak (Q-factor), which determines the resolution with which the shift in resonance frequency can be determined, and the accuracy with which the location of the resonance frequency is known. High losses create shallower dips, while fluctuations in the resonance frequency reduce the signal to noise ratio. Losses and noise are hence two properties of the system which must be reduced as much as possible, to obtain sub-mm detectors with optimal sensitivity.

The sensitivity of a detector is commonly expressed as the noise equivalent power (NEP), given in $\mathrm{W}/\sqrt{\mathrm{Hz}}$, which is defined as the input power level resulting in a signal equal to the standard deviation of the signal in an integration time of 0.5 s [18]. It can be seen as the ratio between noise and responsivity, or the minimum detectable signal. For the responsivity, it is very important whether amplitude or phase is measured. As seen in Figure 8, the reponsivity in phase θ is much larger than in amplitude A, which would make phase measurement preferable.

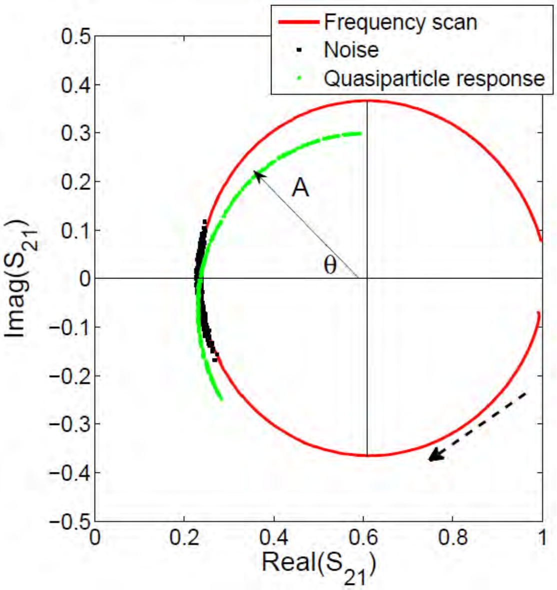

Figure 8 Resonance circle with complex transmission plotted, figure from [11]. The red circle denotes the frequency sweep, while the black points denote time domain data sampled at the resonance frequency (in this picture the left crossing between the red circle and the horizontal axis) at a rate of 50 kHz. The time domain points are not exactly on the red circle, showing the noise. The green points denote the responsivity to a sub-mm signal at the resonance frequency, which is given as a fuinction of amplitude A and phase θ.

For dark measurements (without incoming photons), the fundamental noise limit in a pair breaking detector is given by generation-recombination (g-r) noise, fluctuations from equilibrium in the quasiparticle number. Authors in [19] measure noise and reposnivity in Al CPWs and show that this limit can be reached using amplitude readout. However, the most important fundamental limit for astronomy purposes is the photon noise limit, which is the noise arising from random arrivals of photons from the source. Once a detector has intrinsic noise negligible compared to the photon noise limit, there is no point in further improving the detector. The incoming photon flux also set the limit on the quality factor Q (also the maximum frequency resolution), as due to the photons Cooper pairs are broken into quasiparticles, which create resistive losses and hence limit the Q. Photon noise is further described in the next subsection.

1.4.1 Fundamental limit: Photon noise

Photon noise originates from the random arrival time of photons that obey Bose-Einstein statistics for mode occupancy [20]. The spectrum, with accompanying NEP limit, can be approximated as [21]:

$$S_P = 2hP_{source}f_{source} \cdot \underbrace{\left(\frac{dX}{dP_{source}}\right)^2}_{responsivity} \cdot \frac{1}{1+(\nu\tau)^2} \tag{1.1}$$

$$NEP_P = \sqrt{2hP_{source}f_{source}} \tag{1.2}$$

where X is the measured quantity (amplitude A or phase θ) and τ is the quasiparticle lifetime. Important to realize is that the responsivity depends on P_{source} such that the total noise level S_P is *independent* of optical power.

Figure 9 shows the photon noise limited NEP that is required for future space based observatories. These observatories will use $4\ \mathrm{K}$ optics to eliminate thermal self-emission and can therefore reach an instrument sensitivity which is only limied by the photons from the astronomical source, instead of being limited by self-emission from the telescope optics. For spectroscopy, this limit decreases as dividing the signal into R bands reduces the optical power per band by $1/R$ and the photon noise limit scales with $\sqrt{P_{source}}$. Assuming $R = 1000$, the NEP from the Galactic cirrus will be about $10^{-20}\ \mathrm{W}/\sqrt{\mathrm{Hz}}$ at on the order of $0.1\ \mathrm{aW}$ optical power per frequency band given the specification, which is a very ambitious goal considering the current state-of-the-art detectors. For photometry, this requirement relaxes to about $4 \cdot 10^{-19}\ \mathrm{W}/\sqrt{\mathrm{Hz}}$ at $0.1\ \mathrm{fW}$ optical power.

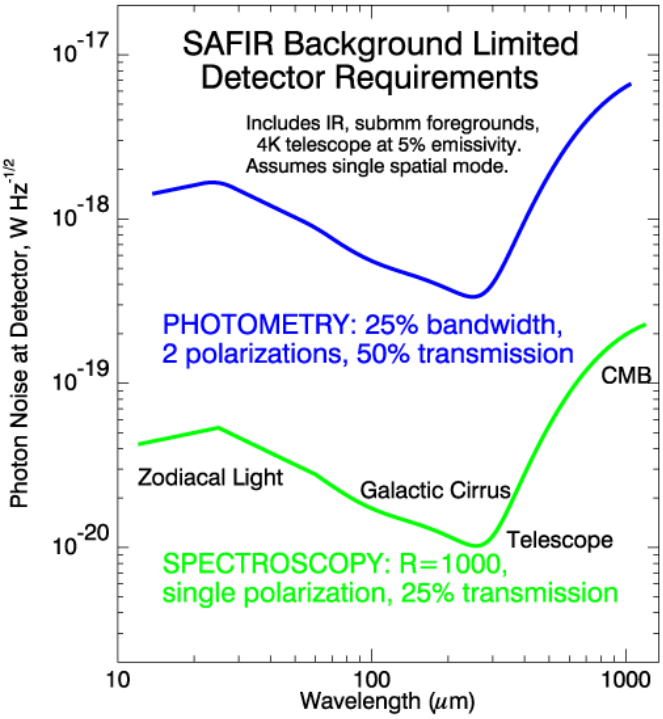

Figure 9 Figure courtesy NASA/JPL-Caltech [22]. In blue and green are the photon noise limits for SAFIR, a proposed space-based sub-mm telescope, for photometry (for imaging) and spectroscopy (for redshift determination) respectively.

For CPWs, the photon noise limit for photometry in space has been demonstrated in amplitude readout [23], where the authors measure noise and responsivity in a lens antenna coupled MKID and reach a NEP of $4 \cdot 10^{-19}$, see also Figure 10 (left). However, for phase readout a problem arises, as can be seen in Figure 10 (right). In phase, a source of excess noise is clearly present, increasing the noise level by about $20\ \mathrm{dBc/Hz}$. Unlike the photon noise spectrum from (1.1) which is flat, the excess noise spectrum has a frequency dependence. This has been difficult to attribute to a concrete physical mechanism, but modelling the excess noise as originating from two-level systems (TLSs, treated extensively for glasses in [24]) has been successfull in explaining the observed characteristics [25], where the authors are able to accurately fit noise data to their TLS model. Attempts to locate the origin of these TLSs has pointed towards surfaces as primary candidates [26, 27], where the authors in these articles compare their data with theoretical calculations and etch away CPW regions respectively.

Recent improvement in detector geometry have shown that phase readout is possible but only for hybrid CPWs, which have a CPW part optimized for sensitivity and another part optimized for noise. The difference in performance of regular and hybrid CPWs can be seen in Figure 10 (left) and Figure 11, where the hybrid CPW shows the flat spectrum with roll-off expected for photon noise from (1.1). Figure 11 shows that this continues down to $5\ \mathrm{pW}$ of power.

Microstrips suffer from the same TLS problem. Authors in [28] report a NEP of $5 \cdot 10^{-17}\ \mathrm{W}/\sqrt{\mathrm{Hz}}$ in a dark measurement of microstrips. This means that, from Figure 11, one can hope to reach the photon-noise limit only in the pW range, while as mentioned previously, even for photometry this limit should be reached until $0.1\ \mathrm{fW}$. In Figure 12 the result from [29] is reproduced, showing that microstrips have higher noise than the standard CPW from [25]. TLS noise levels of $-200\ \mathrm{dBc/Hz}$ are reached, but these microstrips require thick ($4\ \mu\mathrm{m}$) and very wide geometries ($30\ \mu\mathrm{m}$) and are operated at very high internal power ($-5\ \mathrm{dBm}$).

To summarize the difference in performance between microstrips and CPWs more quantitatively, Table 1 shows the comparison on the important criteria for the two MKID types. This leads to the research question formulated in the next subsection.

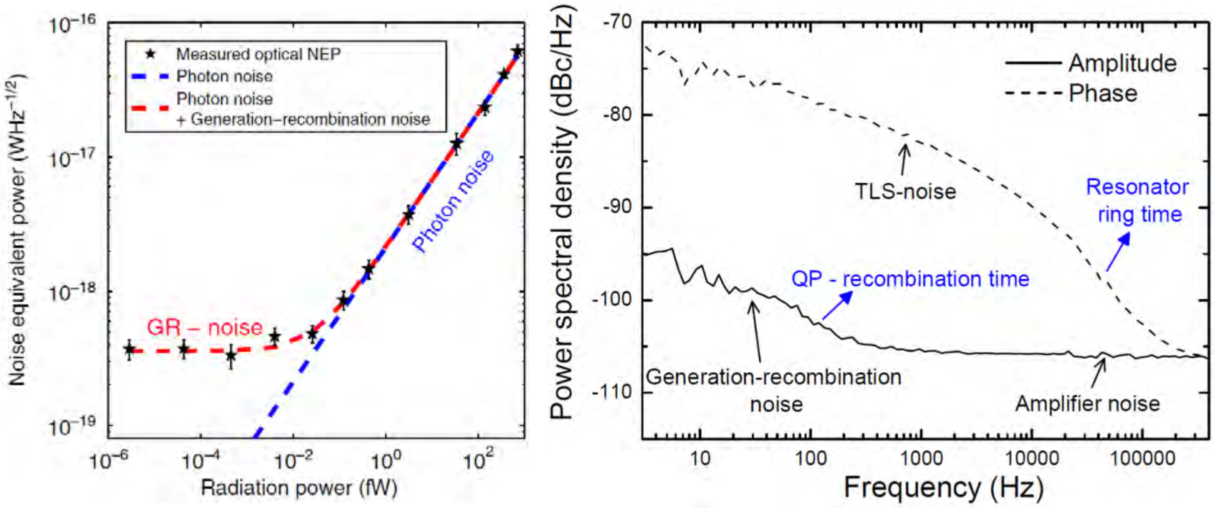

Figure 10 Left: NEP versus radiation power, figure from [23]. Above $0.05\ \mathrm{fW}$, the Al CPW resonator has photon-noise limited sensitivity.
Right: Noise spectrum for an Al CPW, figure from [11]. In amplitude read-out (solid line), only noise inherent to the system is visible, whereas in phase read-out TLS noise dominate, with the sloped spectrum with roll-off.

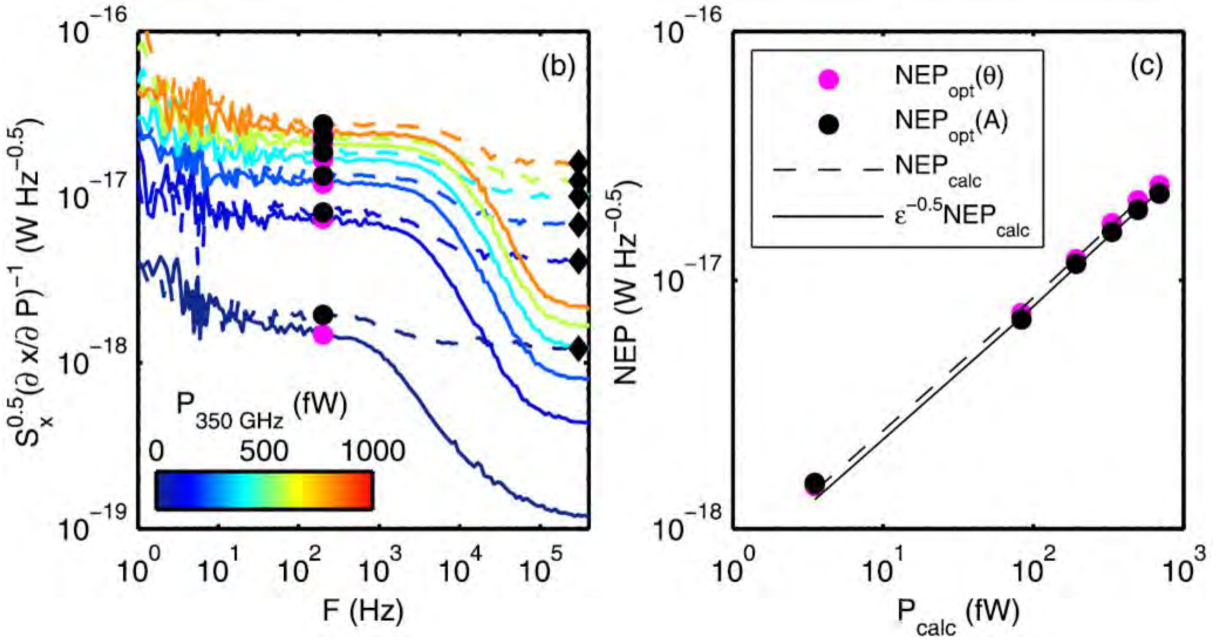

Figure 11 Left: Noise spectrum for various optical powers (color is lighter with increasing power) in a hybrid CPW, right: NEP versus optical power, both figurea from [30]. A $\sqrt{P}$ dependence for the NEP, typical for photon-noise limited sensitivity, can be seen down to 5 fW of power.

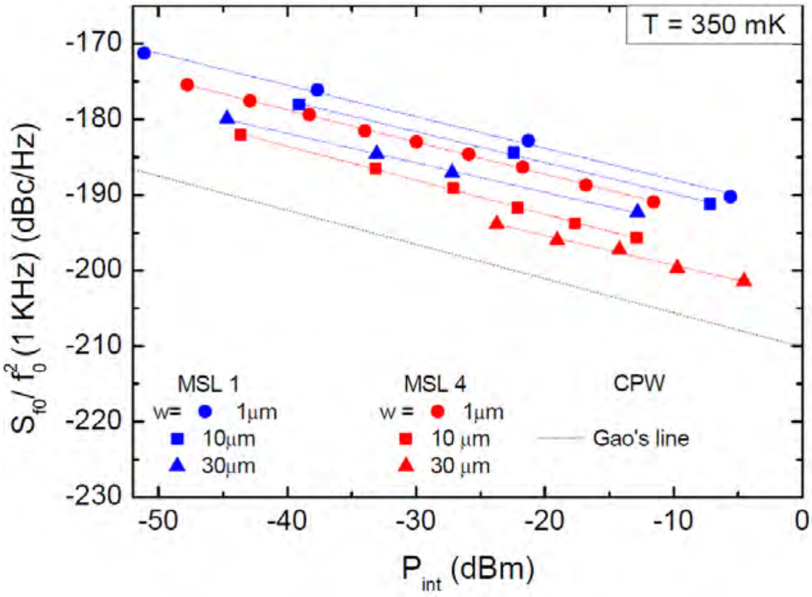

Figure 12 Noise versus internal power plot from [29] for microstrips with dielectric thicknesses 1 (MSL1) and 4 μm (MSL4), for various widths w. Also plotted is the best CPW from [25].

Table 1 Comparison of the DESHIMA specifications with the best CPW and microstrip performances on the criteria loss, noise and sensitivity. Examples from literature are measured at $P_{int} \approx -30\ dBm$.

	DESHIMA specifications	CPW	Microstrip
Loss	"Photon noise limited" as $Q = f(P)$	$5 \cdot 10^6$ [11]	$3 \cdot 10^5$ [29]
Sensitivity: Amplitude readout		Photon noise limited, $P > 0.05$ fW [23]	
Sensitivity: Phase readout	Photon noise limited, $P > 100$ fW [5]	Photon noise limited, $P > 5$ fW [30]	TLS limited, $5 \cdot 10^{-17}\mathrm{W}/\sqrt{\mathrm{Hz}}$ [28] (Dark measurement)

1.5 Goal of this project

Reducing TLS noise and obtaining high quality factors are relevant for achieving arrays of photon noise limited detectors, suitable for spectroscopy and imaging in the sub-mm range. The smaller volume associated for microstrips compared to CPW is among the best reason to use microstrip for MKIDs, but there in particular, TLS loss and noise are a problem. The benefit of increased responsivity for smaller volumes is counterbalanced by an increase in TLS noise which currently limits the sensitivity. For this purpose, this project aims to establish if microstrips can be made photon-noise limited and with losses similar or better than CPWs.

The strategy to reach this goal is to first use numerical methods to model the potential loss and noise sources in microstrips and CPWs (chapter 3). From geometrical dependencies and comparison with existing data, conclusions can be drawn on the dominant noise and loss sources. Then, the acquired knowledge is tested by measuring the loss and noise on a new set of resonators, made by the fabrication method described in chapter 4. The numerical results are used to propose a sensible chip design for resonator set. The experimental data (chapter 5) can then be compared with numerical results, to determine quantitatively the contribution of possible loss and noise sources and to obtain estimates on source specific parameters.

1.6 Link to other research fields

The research of MKIDS is also connected to research done on qubits. A good example of the cross-over is [31]. There, the qubit is a Cooper pair box on a superconducting island located on a superconducting microwave resonator will cause small resonance frequency shifts depending on its state. This allows for non-destructive measurement of the qubit. Considering the multiplexing capabilities of microwave resonators, this system could be suitable for quantum memory. Moreover, it is also essential for quantum computation to have perfect control over the creation of the quantum states. Authors in [32] show exactly that, as well as reliable read-out, for the quantized photon states inside their resonator which is coupled to a phase qubit.

The use of MKIDS has also extended to astronomical observations in the optical range, where the read-out speed of its direct detection of photons can help study gravitational waves and extrasolar planets [33]. Furthermore, MKIDS could even be used as detectors for dark matter, as proposed in [34]. This shows the relevance of this research in a broad range of fields such as cosmology, imaging, elementary particles physics and even astrobiology.

2 Two-level system theory

To limit losses and noise, a good understanding of the physical nature of the underlying processes is necessary. This requires an assessment of the important characteristics of the loss and noise that is observed. Figure 13 (left) from [10] shows the phase noise in solid lines and the ampltidue noise in dashed lines. While the ampltiude noise is on the same level as the system noise (black), in the for responsivity preferential phase readout there is clearly excess noise of about $20\ \mathrm{dBc/Hz}$ higher than the system noise. This excess noise has a $1/\sqrt{f}$ dependence with a roll-off related to the response time [14]. Furthermore, Figure 13 (right) from [25] shows that this excess noise has a $1/\sqrt{P}$ dependence. In [35], the author demonstrates that two-level systems (TLSs) regardless of their origin, fit that profile well, building on theory that had been first applied to glasses [24].

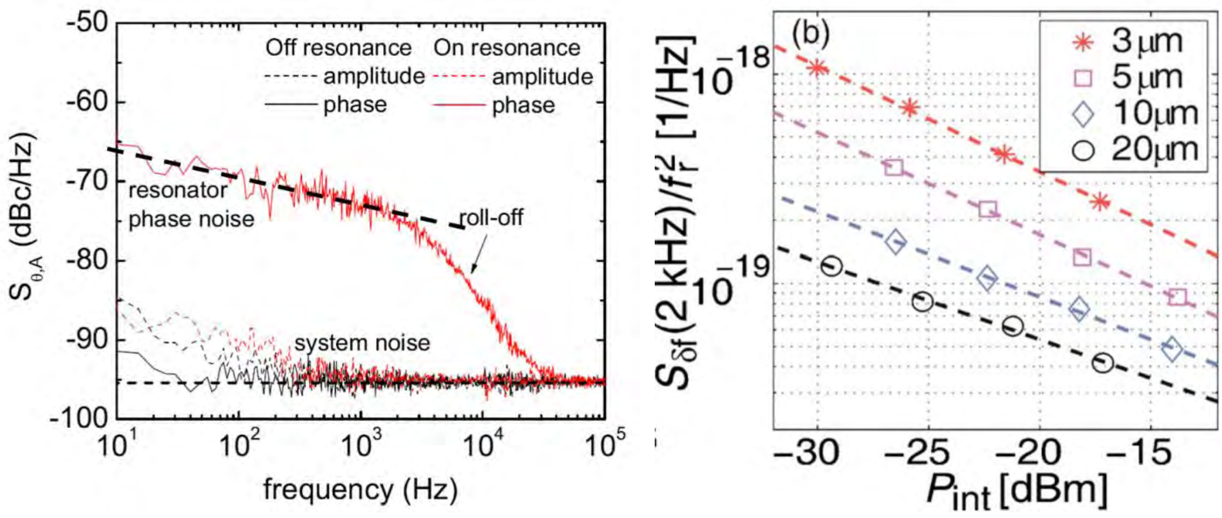

Figure 13 Left: Frequency noise spectrum from [10], for a CPW containing $300\ \mathrm{nm}$ NbTiN on Si. The phase noise is decreasing as a function of frequency with a roll-off due to the resonator response time.
Right: Frequency noise as a function of internal resonator power (corresponding to the strength of the readout signal inside the resonator), figure from [25] for a Nb CPW with various central strip widths. The dashed lines are power laws fitted to the experimental points, all of which are close to a $1/\sqrt{P}$ dependence.

The question is what can be said about the sources of dissipation, absorption and fluctuations in electromagnetic energy in the resonators. Figure 13 (right) shows a geometrical dependence on the width of the central strip in a CPW, Calculations suggest that TLSs are present at the surfaces of the resonator. Experimental evidence for that claim has been provided by e.g. [27], where part of the substrate located in the gaps of a CPW is etched away and a reduction in noise is observed. But while surfaces are likely candidates to host TLSs, the exact location has not been proven and bulk contributions may come into play if surface contributions are reduced. This calls for a extensive analysis on TLSs. For this purpose, first the concept of TLSs is explained. Then, potential locations for the loss and noise sources are discussed, with arguments from literature.

2.1 Two-level systems

The previous section has provided the evidence for TLSs as the cause of excess noise, based on its experimental characteristics. This does not tell what these energy levels physically represent. In the original theory on TLS from [24], it is associated to a slight non-periodicity of the lattice due to a non-zero temperature and inevitable impurities. This creates multiple potential minima for the atoms. At low temperatures, the relevant regime for this thesis, transfer from one state to the other will mainly occur due to tunnelling and only from the ground state to the first excited state (two levels). If other sources of energy become available due to e.g. the presence of an electric field and a particle can couple to that field through a dipole moment, that particle may absorb some of the electrical energy to move from the ground state. This is how TLSs cause losses through absorption. However, if too much energy is present, all two-level systems will be excited and cannot absorb more energy. The systems are then said to be saturated and do not contribute to the losses anymore.

Additionally, as the orientation of dipole moments is influenced through coupling with the electric field, the TLSs can cause a change in dielectric constant ε, which in turn causes a change in capacitance, subsequently influencing the resonance frequency f_{res}. Hence, fluctuations in the occupations of TLSs cause fluctuations in f_{res} otherwise known as noise. It is well possible that the TLSs responsible for losses are the same as for the noise, as suggested in [35].

A good mathematical description of TLSs can be found in [35], but here an expression for the losses, denoted by $1/Q$, is used from [36], see (2.. Two contributing factors to the losses may be distinguished: the *participation ratio*, sometimes also called filling factor [26], which specifies the fraction of the electromagnetic energy available for TLSs inside the layer, and the *loss tangent* which is surface specific and determines how much of that available energy is transformed into loss. The participation ratio is subject to saturation, determined by saturation field E_s above which losses scale roughly linearly with the field.

$$\frac{1}{Q} = 2 \underbrace{\frac{\tanh\left(\frac{hf}{2kT}\right)}{Q_{TLS,0}}}_{loss\ tangent} \underbrace{\frac{\varepsilon_{sdi} \int \frac{|E|^2}{\sqrt{1+|E|^2/E_s^2}} dV_{layer}}{W}}_{participation\ ratio} \tag{2.1}$$

Here, ε_{sdi} is the dielectric constant of the surface dielectric layer with volume V_{layer}. The electrical energy in the whole system W can be determined through a equivalent circuit-element approach as in the article of [36], but in this thesis, the following expression is evaluated, which corresponds to [37]:

$$W = \frac{\int \varepsilon |E|^2 dV_{system}}{2} \tag{2.2}$$

where ε is the dielectric constant from the material over which is integrated, e.g. air or dielectric.

The saturation of TLSs is typically studied by determining the loss as a function of Internal power. This is defined, using time constant $\tau = 2l/v_\phi$ with $v_\phi = \omega/\beta$ as the phase velocity, β as the propagation constant and l as the length of the microstrip/CPW resonator, as:

$$P_{int} = \frac{energy}{\tau} = \frac{v_\phi W}{2l} = \frac{\omega W}{2l\beta} \tag{2.3}$$

For the noise, the semi-empirical expression (2.4) from [35] is used, with $\kappa(\nu, f, T)$ as the noise spectral density coefficient whose ν (fluctuation, modulation or operating frequency) dependency is empirically derived for $f = 5\ \mathrm{GHz}$, $T = 0.120\ \mathrm{K}$, but can be extended by the fitting formula (2.5) from [38]. Unless otherwise specified, $\kappa(\nu, 5\ \mathrm{GHz}, 120\ \mathrm{mK}) = \kappa(500\ \mathrm{Hz}, 5\ \mathrm{GHz}, 120\ \mathrm{mK}) = 5 \cdot 10^{-26}\ [\mathrm{Vm}^2/\mathrm{Hz}]\varepsilon_0^2$ is assumed throughout chapter three. In chapter five, this κ is taken as a material dependent parameter to be determined by experiments.

$$\frac{S}{f_r^2} = \frac{\kappa(\nu, f, T)}{4E_s} \frac{\int \frac{|E|^4}{\sqrt{1 + |E|^2/E_s^2}} dV_{layer}}{W^2} \tag{2.4}$$

$$\kappa(\nu, f, T) = \kappa(\nu, 5\ \mathrm{GHz}, 120\ \mathrm{mK}) \left(\frac{0.120}{T}\right)^{0.14} \left(\frac{\tanh\left(\frac{hf}{2k_B T}\right)}{\tanh\left(\frac{h \cdot 5\ [GHz]}{2k_B \cdot 0.120\ [K]}\right)}\right)^2 \tag{2.5}$$

From (2., a crucial geometrical dependence can already be distinguished. For the same field distribution, the numerator only scales with the volume V and the denominator scales with V^2. This means that decreasing the volume to increase responsivity automatically means that TLS noise is increased, compromising the sensitivity.

2.2 TLS related loss and noise in real systems

For the purposes of identifying the potential TLS locations, the microstrip as given in Figure 14 is considered. A CPW has the same types of surfaces and bulk volumes, only in different quantities.

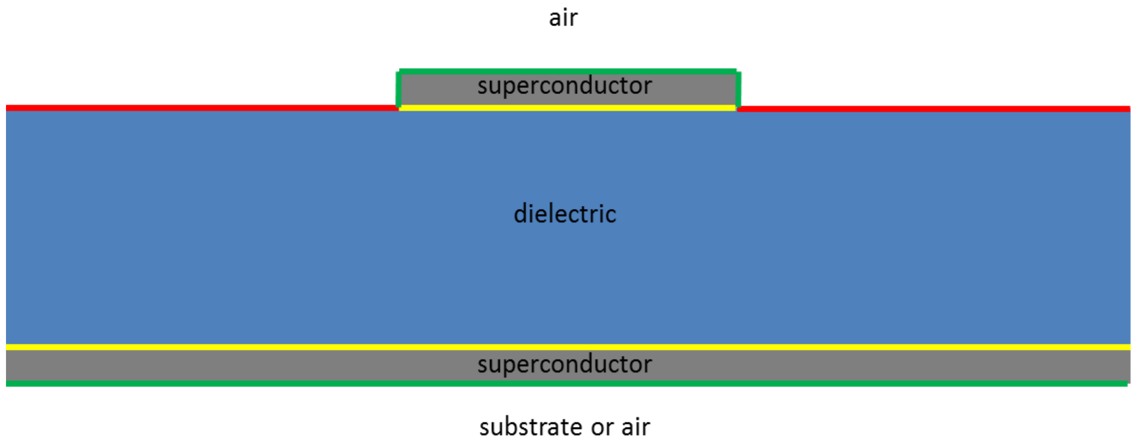

Figure 14 Cross section of a superconducting microstrip. Different colors denote different surface or volume types.

The dielectric bulk may hold TLS, as the author in [29] cannot distinguish between bulk or surface loss for microstrips. As already mentioned, more evidence points towards surfaces. More specifically, three different surface types may be distinguished: superconductor-dielectric interface (or metal-dielectric, yellow), superconductor-air interface (or metal-air, green), dielectric-air interface (red), superconducting bulk (grey):

- The superconductor-dielectric interface has been suggested by theoretical work in [37] using numerical simulations and by experimental work in [26] using niobium CPWs with various central strip widths. The TLSs may find their origin in fabrication, through damage done on the substrate if reactive ion etching is used. Authors in [39] show interface states due to impurities or dangling bonds after reactive ion etching on a Si substrate, particularly with carbon based gases. They state that for certain gases, the 'damaged layer' can span tens of nm (referring to [40], where surface layers damaged after etching using various gas compositions are examined with e.g. TEM).

- The dielectric-air interface has been shown to be a TLS location in [36], where removing the top surface of the exposed dielectric improved the quality factors in CPWs.

- The superconductor-air interface has been conjectured to hold TLS in [41]. There, using a superconductor with less surface oxides (Re versus Al) improved the quality factor.

2.3 Other loss mechanisms

2.3.1 Superconductor loss

At any non-zero temperature, a number of thermally excited quasiparticles exist, which as mentioned in [29], can cause additional losses. Authors in [42] also state that non-equilibrium quasiparticles from external sources may play a role. However, thermal quasi-particles at temperatures of the order $T/T_c < 0.1$ should hardly be present.

Alternatively, it is suggested by [43] that a 'bi-layer' could form at the bottom of the superconductor, where the authors find a Nb layer of about 20 nm thickness below their bulk Nb with different properties. This could have originated from a high temperature fabrication step, where contaminants in the film locally create a region with lower T_c. In experiments in [17], the existence of a bi-layer is hypothesized. It is suggested that a NbTiN layer with lower T_c may have formed, "either during the $300°\mathrm{C}$-deposition of $\mathrm{SiN_x}$, or at the initial stages of the deposition of the wire", but no conclusive evidence is given. That there may be imperfections in the superconductor is supported in the diffraction (where the NbTiN shows several grain orientations) and the HREM images (thin layer at the superconductor-substrate interface) made by [44] in Figure 15.

Unfortunately, if one would try to incorporate this situation in a numerical model, which is the goal of identifying potential loss sources, one would have to estimate two experimental unknowns: the thickness of the low T_c layer and the value of the lower T_c. The danger rises that with too many unknowns in the system, a fit with experimental results can always be made which not necessarily corresponds to the physical reality. For the reason, a more parsimonious approach is taken for the numerical models in this thesis, abandoning the notion of a low T_c layer.

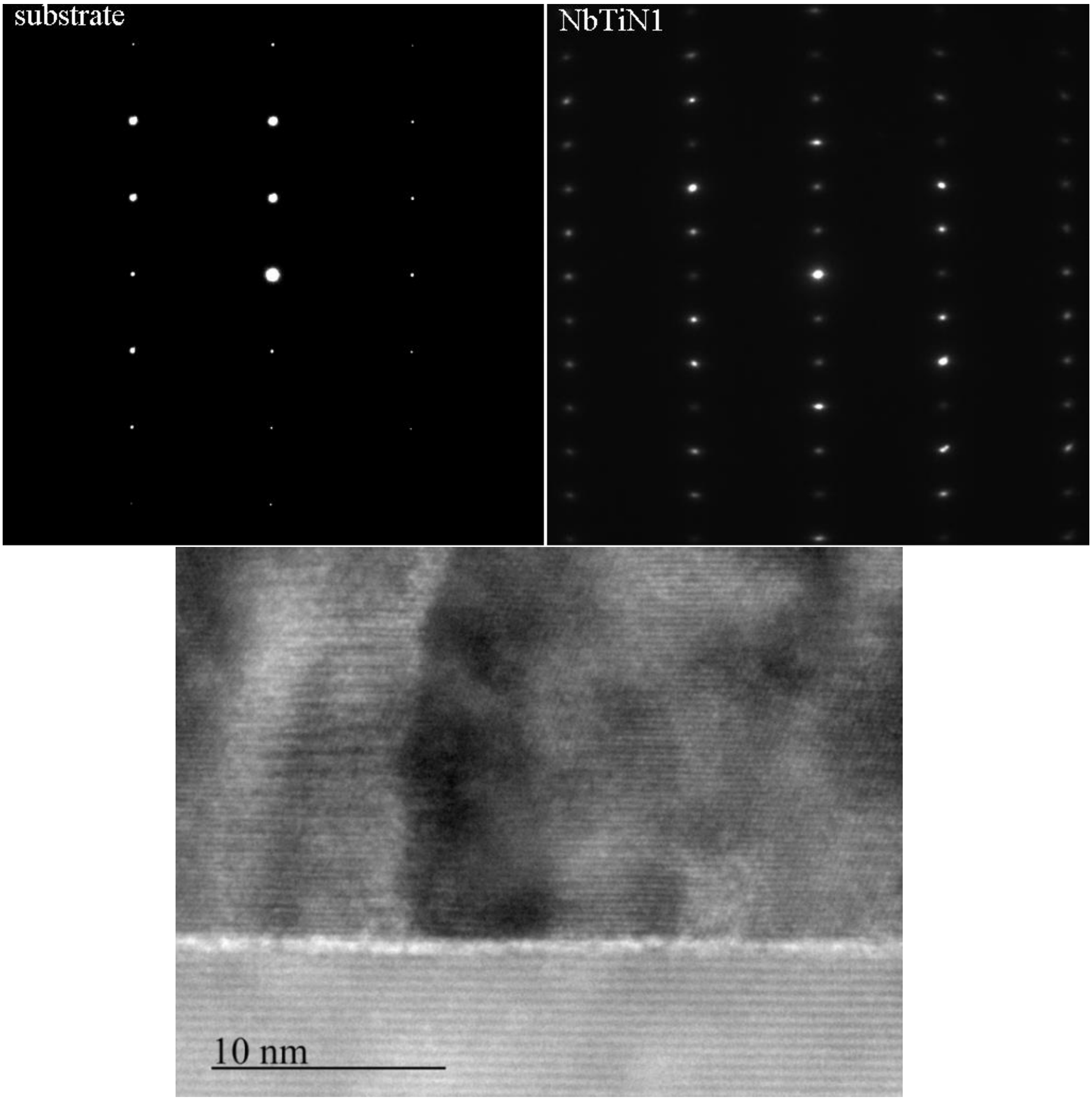

Figure 15 Top left and right: diffraction images of the substrate below the bottom superconductor and the bottom superconductor itself of a microstrip used in [17] respectively.
Bottom: HREM image of the substrate-bottom superconductor interface. Images by [44].

2.3.2 Radiation loss

While not an issue in microstrips, for wide CPWs radiative losses may start to dominate. These can be simulated numerically or calculated analytically for simple structures [45], assuming that all radiated power does not reflect back to the structure. Note that this then only provided an upper limit on the loss, as in reality, the detector is always enclosed in a box. The relevant equations from [45] are restated here for convenience (where w is the central strip width, g is the gap width, s is the dielectric thickness, ε_{di} is the dielectric constant, c as the speed of light and K is the complete elliptical integral of the first kind):

$$a = 10^{\left(0.54-0.64\log_{10}\left(\frac{w}{s}\right)+0.015\log_{10}\left(\frac{w}{s}\right)\right)^2\log_{10}\left(\frac{w}{g}\right)+0.43-0.86\log_{10}\left(\frac{w}{s}\right)+0.54\log_{10}\left(\frac{w}{s}\right)} \tag{2.6}$$

$$\varepsilon_{eff} = \left(\sqrt{\frac{\varepsilon_{di}+1}{2}} + \frac{\sqrt{\varepsilon_{di}} - \sqrt{\frac{\varepsilon_{di}+1}{2}}}{1 + a\left(\frac{4sf\sqrt{\varepsilon_{di}-1}}{c}\right)^{-1.8}}\right)^2 \tag{2.7}$$

$$\frac{1}{Q_{rad}} = 2\left(\frac{\pi}{2}\right)^5 \frac{\left(1-\frac{\varepsilon_{eff}}{\varepsilon_{di}}\right)^2}{\sqrt{\frac{\varepsilon_{eff}}{\varepsilon_{di}}}} \frac{(w+2g)^2\varepsilon_{di}^{3/2}f^3}{c^3K\left(\sqrt{1-\left(\frac{w}{w+2g}\right)^2}\right)K\left(\frac{w}{w+2g}\right)} \tag{2.8}$$

3 Numerical analysis

3.1 Motivation

In order to assess whether the underperformance of microstrips compared to CPWs can be explained and in principle be resolved, a theoretical study is done on the predicted losses and noise of microstrips and CPWs. In particular, the dependencies on geometry are investigated.

Some analytical approaches exist for calculating the electric fields necessary for determining the loss and noise in microstrips and CPWs, such as conformal mapping [46] and the method of partial images [36]. However, these methods have their limitations, as they typically assume a simplified structure, such as zero film thickness. From the theory and literature on loss and noise, it is expected that even thin surfaces filled with TLSs are actually very influencial. Also, it is necessary to distinguish between the superconductor-air interface and the superconductor-dielectric interface, so a non-zero film thickness is required. Modelling these thin layers would then lead to intractable expressions, in which case a numerical analysis is still required. Moreover, it would be of interest to explicitly model the superconductor. Hence, the added flexibility of numerical computations motivates the use of a full numerical approach based on a finite element method, as method of moments solvers do not solve inside the bulk of the superconductor either, but rather assume a surface impedance [47], which substitutes the behaviour of the bulk. This is only valid when the thickness of the superconductor is much larger than the penetration depth of the fields.

For this purpose, COMSOL (version 4.3b) will be used to simulate the electromagnetic fields of microstrips and CPWs throughout this thesis. The RF and Multiphysics modules are selected and the study type of choice is Mode Analysis. Additionally, Matlab (version R2013a) will be used to provide external functions embedded into COMSOL and to perform data reduction steps, while numerical data are fitted using ORIGIN 8. The following models will be used, which are characterized briefly below but are more extensively covered in the following subsection:

- Model 1: Simplest model using perfect metals with identical, unsaturated TLSs on all interfaces. The results can be compared to [37].
- Model 2: Most realistic model, which adds TLS saturation, distinguishes between TLSs on various interfaces and incorporates complex conductivity of the superconductor by means of Mattis-Bardeen theory instead of a perfect metal.

3.2 Model 1

It is important to know whether the results of the simulations can be relied upon. The starting points is a relative simple model, for which literature is available to which the results may be compared, to be called model 1. Goal is to reproduce the numerical results of the simplified model in [37] for losses, involving both CPWs and microstrips. Analogous to that article, the subsequent assumptions are made on what to incorporate in the model and what not. Noise is not yet investigated, as these values are not stated there. Since noise reduction is essential for microstrips and CPWs as well, it will be investigated later on in model 2.

3.2.1 Assumptions

- Only the Q (loss) is calculated, as there is no literature on noise
- The field will be symmetric on both sides of the centre of the microstrip / CPW
- Loss only in surface dielectrics with a thickness of $3\ \mathrm{nm}$ which have identical properties
- No saturation in loss ($E_s = \infty$)
- Perfect metal ($E_{\parallel,surface} = 0$)[1]
- Perfect dielectric ($\sigma = 0$) with dielectric constant $\varepsilon_{di} = 10$
- Electric field inside the surface dielectrics is thickness independent
- The presence of surface dielectrics does not alter the field distribution elsewhere
- Frequency is $600\ \mathrm{GHz}$ (not specified in [37])

The implications of these assumptions in terms of modelling are as follows:

- Only the right-half of the microstrip / CPW cross section needs to be modelled
- Loss tangent (complex part of the permittivity) is zero for the dielectric
- The metal does not require meshing as fields cannot penetrate the surface of a perfect metal
- The thin surface dielectrics do not have to be explicitly included in the model, but can assumed to be present after calculation as the field distribution would not change.

As a consequence of the first and third implication, the modelled area for a microstrip is as in Figure 17. For clarity, the same symbols are used in this thesis for the dimensions of the CPWs and microstrips as in [37], which are shown in Figure 16. A minimum overetch d of $2.5\ \mathrm{nm}$ is assumed if [37] uses $d = 0\ \mu\mathrm{m}$ to ensure that the interface of the metal-substrate-air corners are always of the same shape for fairer comparison amongst geometries. Although this should not matter much, this makes the comparison with the geometries from [37] with a non-zero overetch most useful.

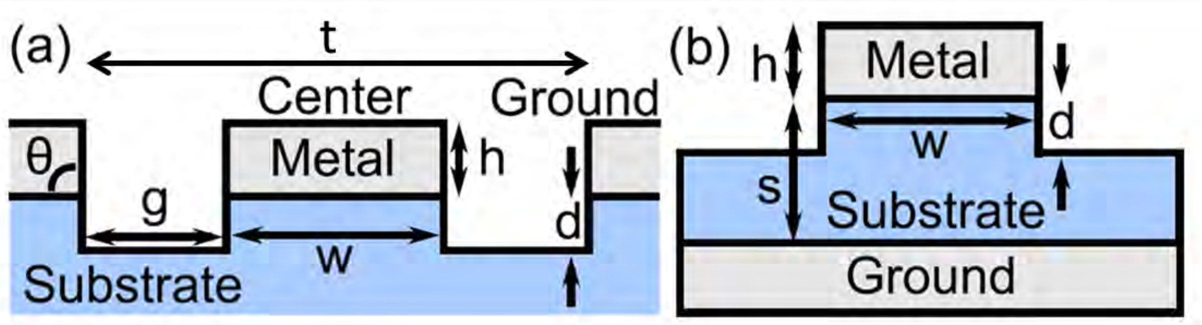

Figure 16 Figure from [37], showing the definitions of the dimensions in CPWs (left) and microstrips (right).

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[1] Perfect metal is defined as the bulk of the material. The boundaries of the perfect metal are considered perfect electric conductors (PEC).

Model 1b

A variation can be made on model 1, discriminating between the interfaces by assigning different loss tangents and by setting a realistic value for the saturation fields from literature. In that case, the third and fourth assumption are replaced by:

- Surface dielectric loss tangents from [36] which are $4.6 \cdot 10^{-3}$ and $1.7 \cdot 10^{-4}$ for surface dielectrics on Si and NbTiN respectively (they are denoted in the table in the article as $1/Q_{TLS,0}$)
- Saturation fields E_s with values of 5 and $0.05\ \mathrm{kV/m}$ [36] for surface dielectrics on Si and NbTiN respectively

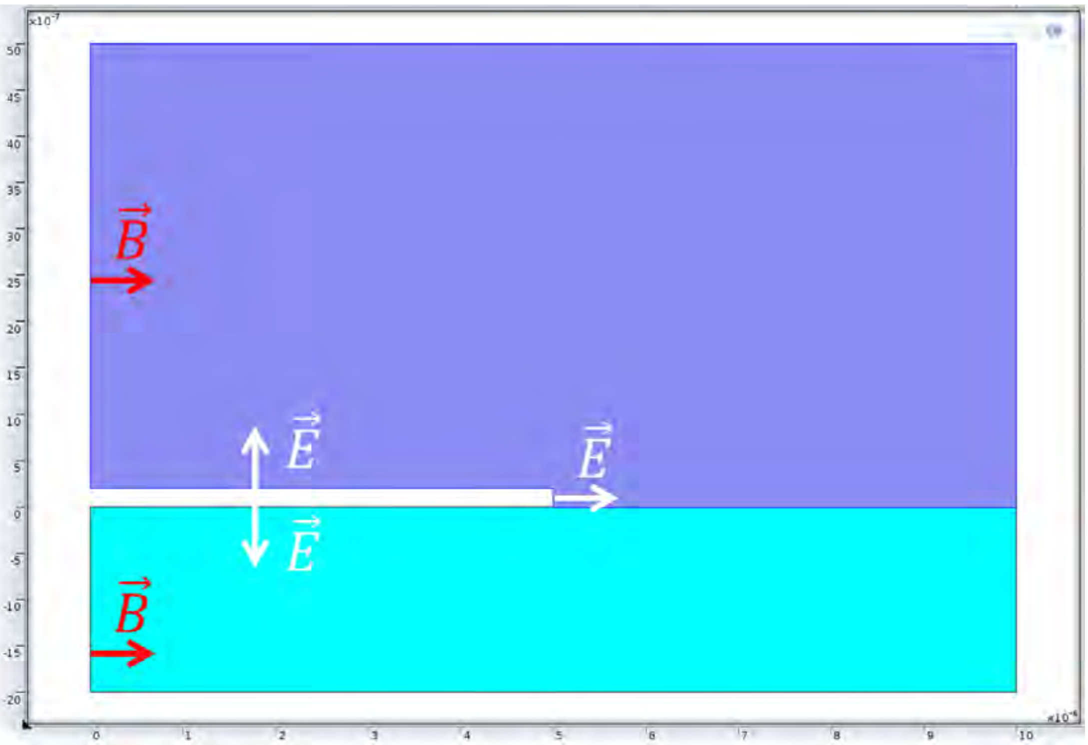

Figure 17 Overview of a microstrip, truncated along its symmetry axis (left boundary), where the magnetic field (red) only has a horizontal component. The white rectangle is the perfect metal, whose volume does not need to be modelled, to whose edges the electric field (white) is perpendicular. In light blue is the dielectric, above in dark blue is air / vacuum.

3.2.2 Boundaries

In order to get the required symmetry of the electric field on the symmetry-axis of the CPW or microstrip, so that the one half (here the left half) does not need to be modelled, current must be prevented to pass through that boundary, otherwise symmetry is broken. This is identical to saying that the magnetic field may not have a component parallel to the symmetry plane. This boundary is then a *Perfect Magnetic Conductor* (PMC), which is mathematically described by:

$$\vec{B} \times \hat{n}_{boundary} = \vec{0} \tag{3.1}$$

The behaviour of a perfect metal is that no current can flow from its surface to its interior. This means that the electric field must be perpendicular to the perfect metal boundary, so all parallel components are zero. This boundary is then a *Perfect Electric Conductor* (PEC), which is mathematically described by:

$$\vec{E} \times \hat{n}_{boundary} = \vec{0} \tag{3.2}$$

The only boundaries that remain are then the outer bounds of the system, which theoretically should be at infinity, but in numerical models must be at a finite distance. If this distance is taken large enough, it should in principle not matter that much which boundary conditions are taken here, but for simplicity these boundaries are also assigned to be PEC. Figure 18 shows a graphical overview of the boundary conditions.

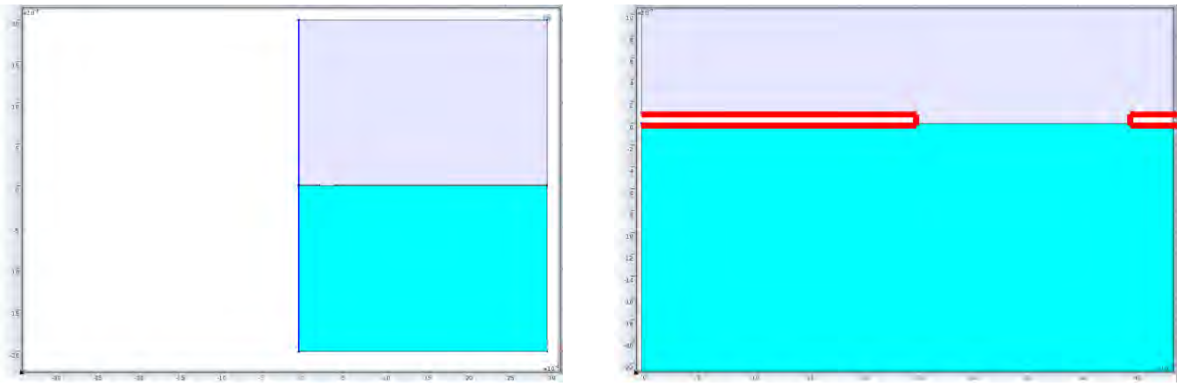

Figure 18 Left: the blue line denotes the PMC boundary. Right: the red lines indicate the PEC boundaries on the perfect metal.

As mentioned, care must be taken to ensure the system size is large enough so that the fields around the CPW or microstrip are not affected by the PEC boundaries of the box. In this model, this is done by sweeping the system size for CPW and microstrip with the largest dimensions from the article of [37]. This yields for the CPW a system size (with width defined as the length from the unmodelled left outer bound to the right outer bound and height defined from the bottom of the dielectric to the top of the air column) of $6.7(w + 2g) \times 2.2\,(w + 2g)$. For the microstrip (with height now defined as the height of the air column above the microstrip), this is $100\ \mu\text{m} \times 50\ \mu\text{m}$. Rescaling for microstrip dimensions is not necessary in this case, as even its largest system size is still relatively small.

3.2.3 Meshing

Meshing is one of the most important steps in numerical calculations and requires some insight in what regions are expected to be important (with steep fields gradients), to find the correct balance between accuracy and computation time. From the chapter on theory, it is apparent that surface dielectrics play an important role in both loss and noise. While the assumptions associated with this model do not require the explicit inclusion of these surface dielectrics, it is still crucial to determine the values of the electric field accurately at the boundaries. For this purpose, six (eight for microstrips) boundary layers are placed at all boundaries where surface dielectrics may be present, which are very thin mesh elements. Furthermore, the results in [37] suggest an important contribution from the metal-dielectric-air corner, so the corners are a further five times refined. Together with the mesh parameters found in Table 2, the mesh as in Figure 19 and Figure 20 is made. As an example for the justification of these parameters, figure shows the effective dielectric constant and the participation ratios of a microstrip as a function of minimum element size, keeping all other parameters constant. While the dielectric constant has already converged as the details of the microstrip are not important for such a global parameter and while the metal-substrate participation ratio does not suffer from large mesh elements either, the other ratios require a minimum size of $\leq 1\ \mathrm{nm}$, where it is safest to include some margin.

Table 2 Meshing parameters used for model 1 for both CPWs and microstrips.

	CPW	**Microstrip**
Maximum element size $[\mu\mathrm{m}]$	10	10
Minimum element size $[\mu\mathrm{m}]$	0.000338	0.000338
Maximum element growth rate	1.15	1.15
Resolution of curvature	0.25	0.25
Resolution of narrow regions	1	1

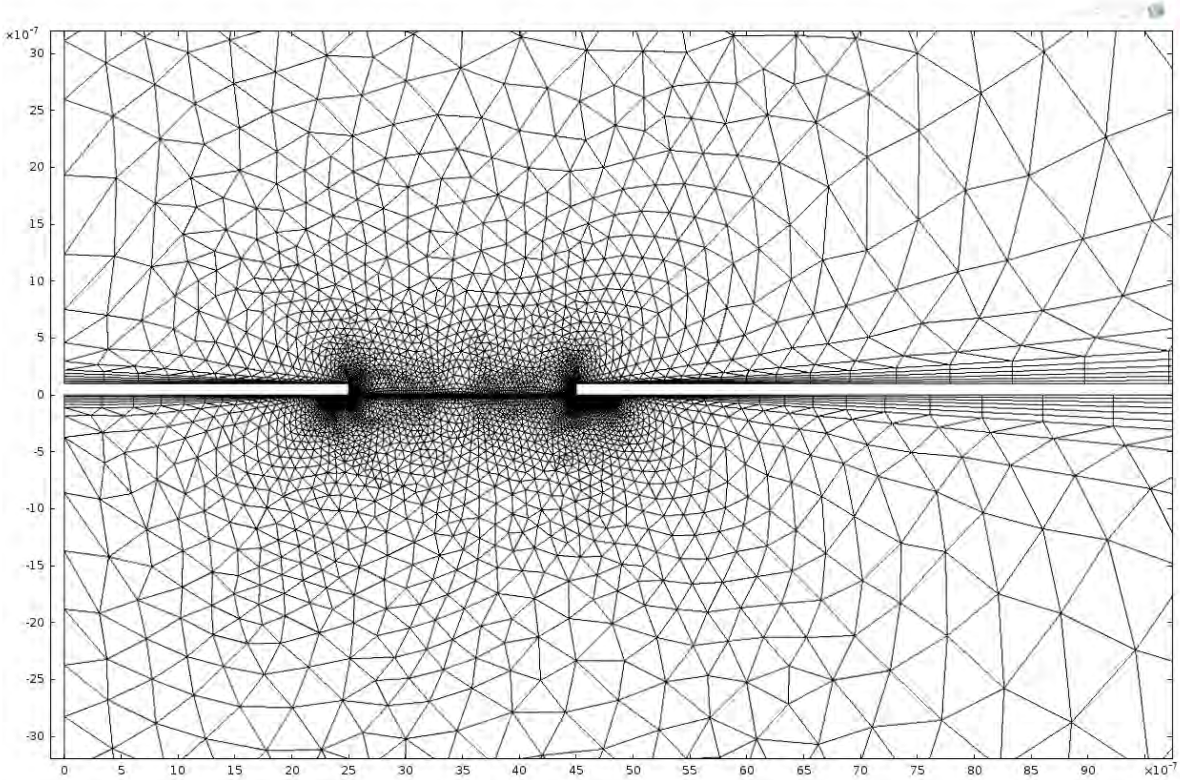

Figure 19 Meshing of a CPW. The unmeshed rectangles are the perfect metals, above and below which air and dielectric respectively is present. Denser elements are concentrated around the gap, while boundary layers are present across all interfaces (particularly visible further away from the gap).

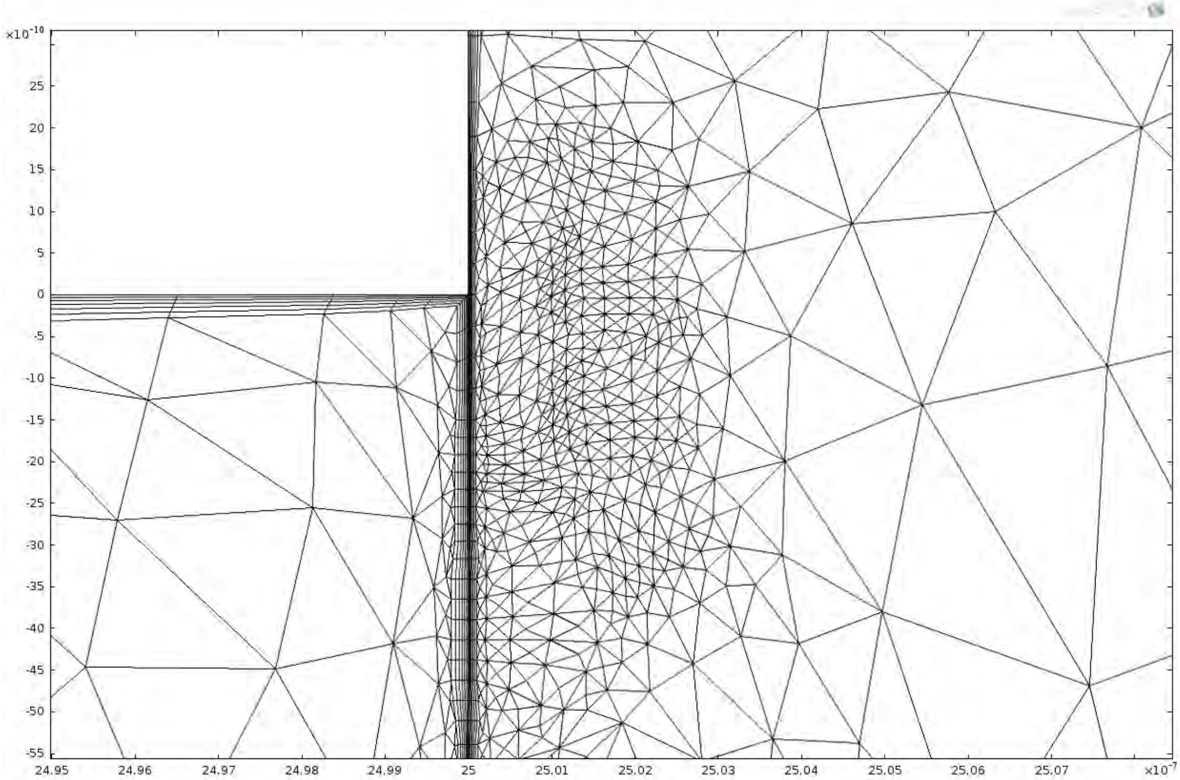

Figure 20 Mesh at the perfect metal (unmeshed, top left)-dielectric (bottom left)-air (right) corner. Visible are the boundary layers across the interfaces and the denser mesh close to the corner.

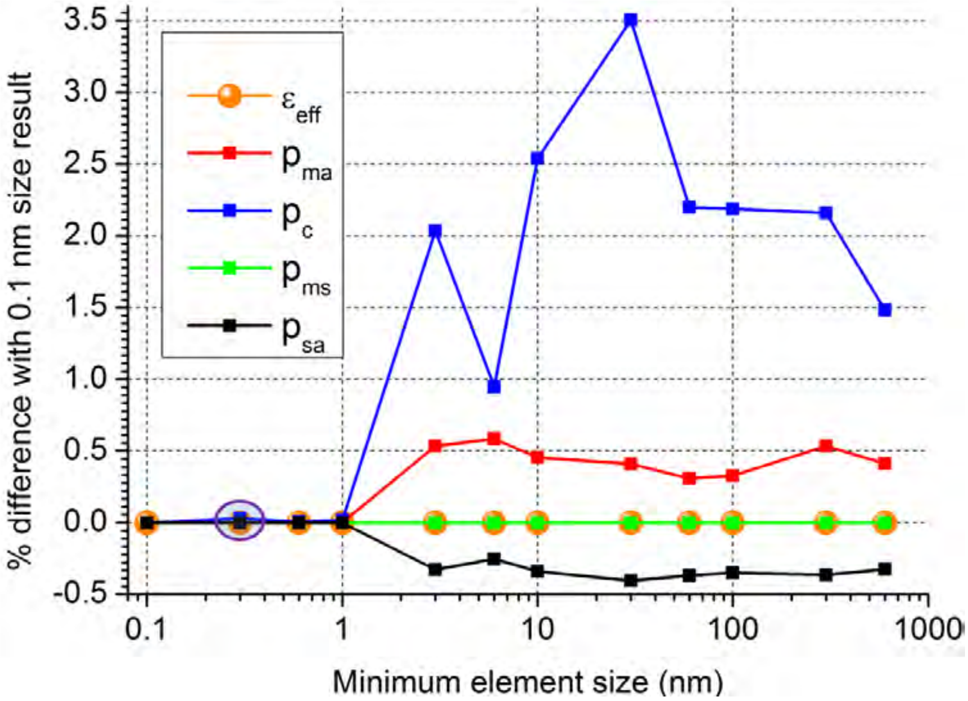

Figure 21 Effective dielectric constant (orange) and particpation ratios p for the metal-air (ma, red) surface, the metal-substrate-air corner (c, blue), the metal-substrate surface (ms, green) and substrate-air (sa, black) surface in a microstrip, as a function of minimum element size (in nm). The purple circle indicates the minimum element size ($0.338\ \mathrm{nm}$) ultimately used for subsequent calculations.

If wider geometries are considered than in [37], the choices of system size and the meshing are particularly for CPWs not straightforward. The following procedure is employed where necessary:

The system size (box that contains the geometry which is meshed) for microstrips is determined by adjusting the size such that the participation ratios no longer change as a function of system size, using the widest geometry. This system size is then used for all geometries, which turns out to be $200\ \mu\mathrm{m} \times 50\ \mu\mathrm{m}$. This does not work for CPWs. Especially for the case where the gap scales with the central strip width, unphysical jumps for large widths are present. This is due to the meshing and more specifically, due to the difficulty in meshing when aspect ratios become very large. There are nm size corners with angstrom sized meshing compared to $100\ \mu\mathrm{m}$ central strip width with hence mm box size. There is a large risk of errors during meshing, making it complicated to derive one recipe from which all geometries may be meshed. Adding a linear scaling with $(w + 2g)$ to the largest box size also does not suffice. Instead, a rather brute force method is employed, which consists of optimizing the box size for all geometries separately. 64 pairs of system widths and heights are tried for each geometry, with system widths of 1.1, 1.5, 2, 5, 10, 20, 50 and 100 times $(w + 2g)$ and system heights of 0.1[2], 0.3, 0.5, 1, 2, 5, 10 and 30 times $(w + 2g)$. The system size yielding the best results (see Appendix on how "best" is determined) for both the effective dielectric constant and the participation ratios is then taken as appropriate and those values are plotted in this chapter. Note that this is only a problem in CPWs, where box sizes necessarily vary more than in microstrips.

3.2.4 Mode analysis

CPWs and microstrips support many propagation modes, but the goal is to find the field distribution corresponding to a quasi-TEM mode, where both electric and magnetic fields are perpendicular to the direction of wave propagation. This is characterized by an effective mode index $n_{eff} = \sqrt{\varepsilon_{eff}}$ [48], where ε_{eff} is the effective dielectric constant. This input parameter must be supplied but COMSOL uses this merely as an initial guess around which modes are searched, so the exact ε_{eff} does not have to be known. For CPWs, a good estimate would be $\varepsilon_{eff} = \frac{\varepsilon_{di}+1}{2}$ [49], a quasi-static approximation averaging the dielectric constant of the substrate with that of air, as the fields can be assumed to be equally divided in the dielectric and the air. For microstrips, good approximations can be calculated using [50], which summarizes results from conformal mapping into accurate closed form expressions. Superconductivity can be included using [51], and [52], if necessary, where in both cases the authors use conformal mapping as well, taking into account the thickness of the superconductor. Adjusting the estimate becomes critical if the dielectric thickness becomes on the order of the film height.

3.2.5 Frequency choice

When using mode analysis, the frequency supplied should be on the order of 6 GHz, as that is where these resonators operate. The calculations so far have used 600 GHz. At first glance, the calculated

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[2] For the narrow CPWs with $w = 1\ \mu\mathrm{m}$ and $g = 2/3\ \mu\mathrm{m}$, 0.1 times $(w + 2g)$ for the height must be excluded, as $h_{film} = 0.3\ \mu\mathrm{m}$.

field distributions are rather similar, as seen in Figure 22 and Figure 23, taken at 600 and 6 GHz respectively.

However, the problem becomes apparent once the densely meshed region is magnified (Figure 24), where unphysical features (sharp peaks) in electric field strengths appear at the edges of the fine mesh elements, which are not present (and should never be present) at 600 GHz (Figure 25). Also worrying is the random direction of the electric field, demonstrated by the arrow plot.

For a consistency check, the calculation is repeated after rescaling the geometry by a factor of ten and decreasing the frequency by a factor of ten. The governing equations then remain the same as no other physically relevant length scale exists, and indeed this yields the same results. The problem is hence due to the ratio of geometry/mesh size versus wavelength (below about 60 GHz).

After contacting COMSOL, they state that indeed the small system size versus wavelength ratio means that the RF module is not really applicable anymore. At such long wavelength, the B and E field will have weak coupling, invalidating the wave equation used in the RF module and motivating the AC/DC module, which uses a static approach to solve for the fields, neglecting wave propagation.

However, from a frequency sweep (not included here) from 600 to 6 GHz, the results remain reliable to 60 GHz. In the decade from 600 to 60 GHz, it can be shown that participation ratios do not change significantly. This means that the 600 GHz data can be used as an adequate approximation.

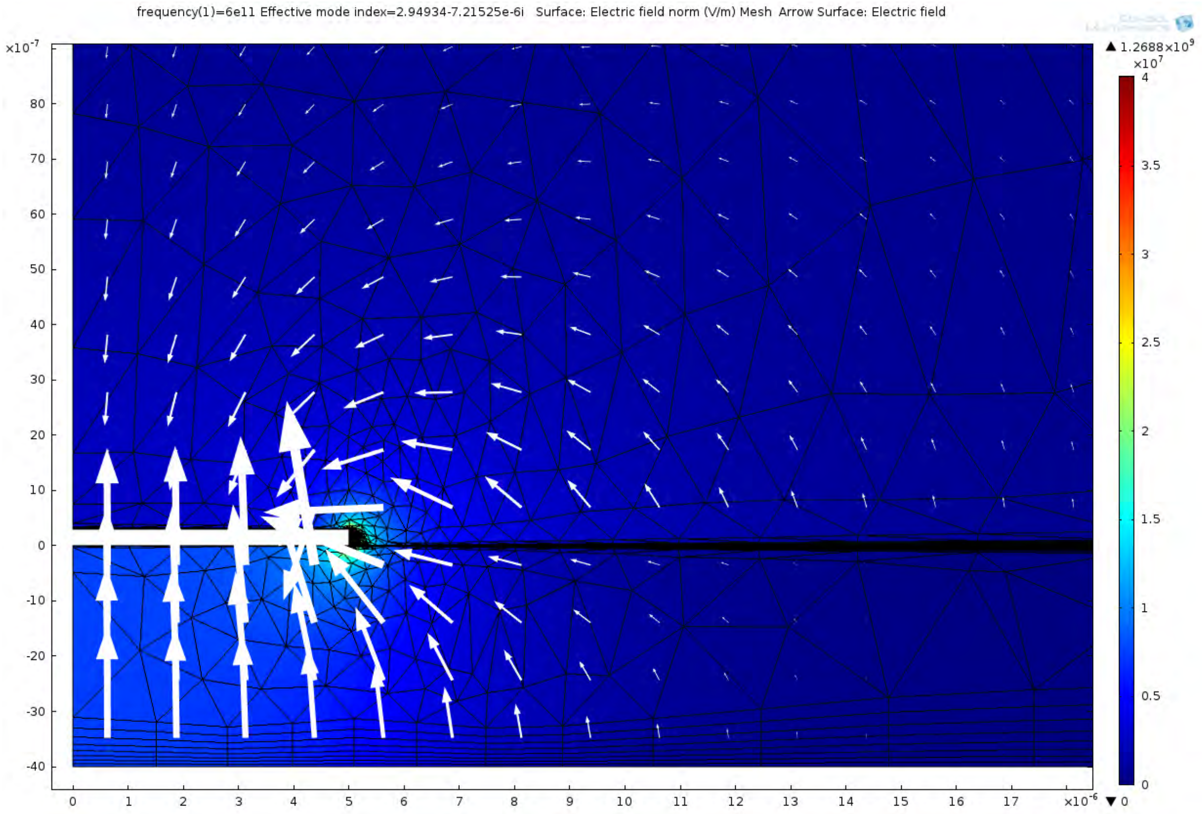


Figure 22 Surface plot of the electric field norm of a microstrip for the TEM mode at 600 GHz. The white rectangle indicates the PEC boundaries, below which the dielectric and above which vacuum is present. The black lines represent the mesh, the white arrows are an arrow plot of the electric field (in-plane components).

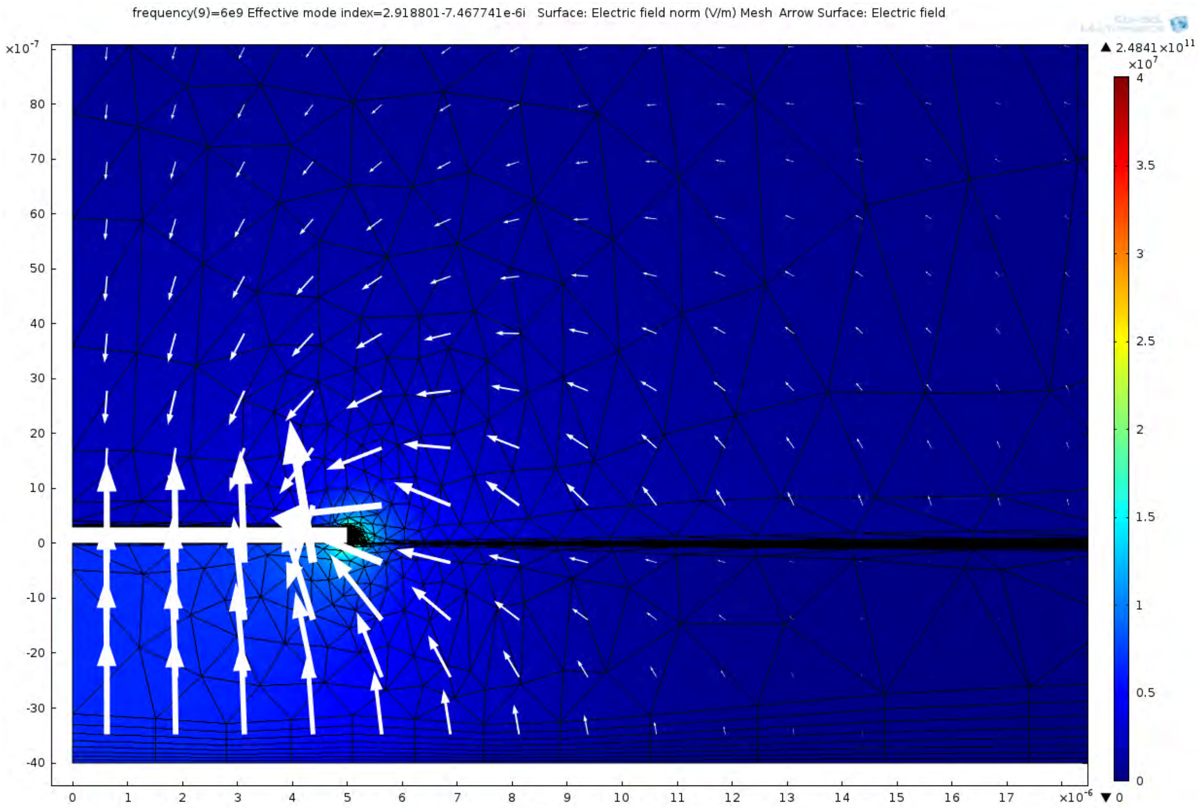


Figure 23 Surface plot of the electric field norm of a microstrip for the TEM mode at 6 GHz. The white rectangle indicates the PEC boundaries, below which the dielectric and above which vacuum is present. The black lines represent the mesh, the white arrows are an arrow plot of the electric field (in-plane components).

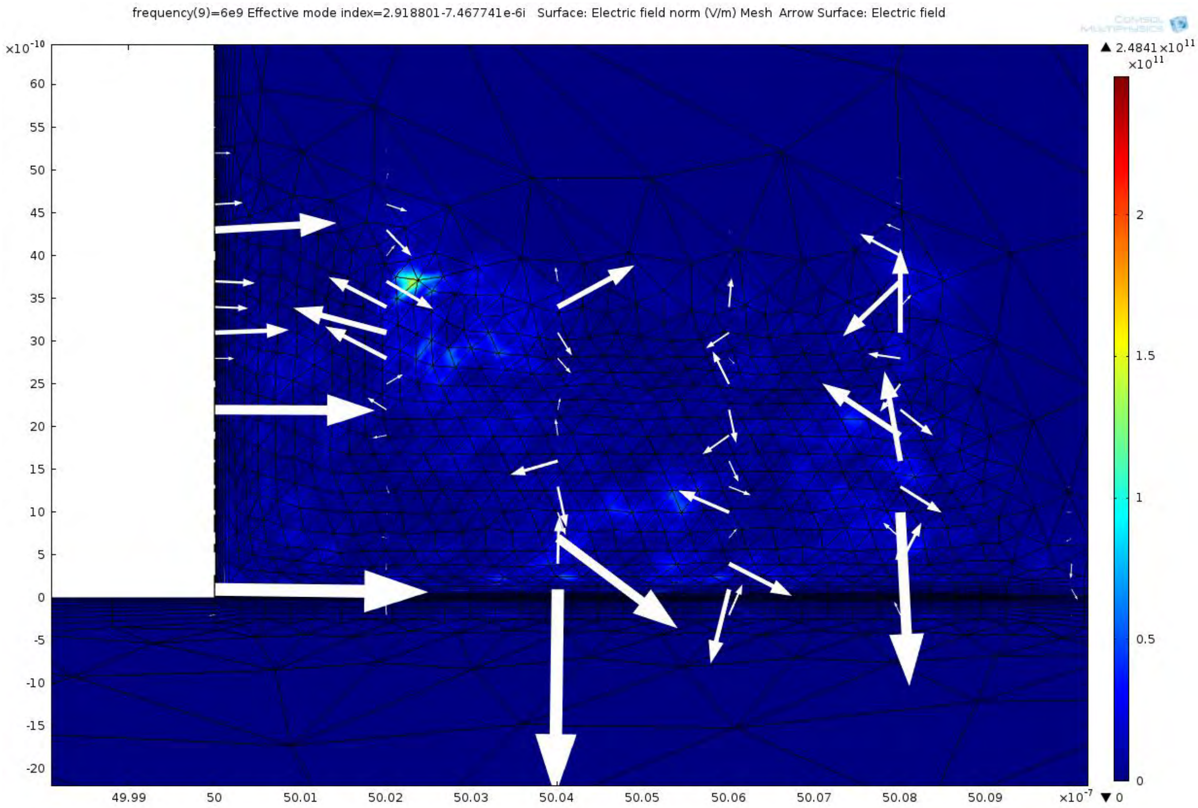


Figure 24 Surface plot of the electric field norm of a microstrip for the TEM mode at 6 GHz, while zoomed into the very densely meshed region at the bottom-right corner of the PEC rectangle. The black lines represent the mesh, the white arrows are an arrow plot of the electric field (in-plane components). Visible are anomalous electric field strength peaks and random field orientations where the mesh elements are at their smallest.

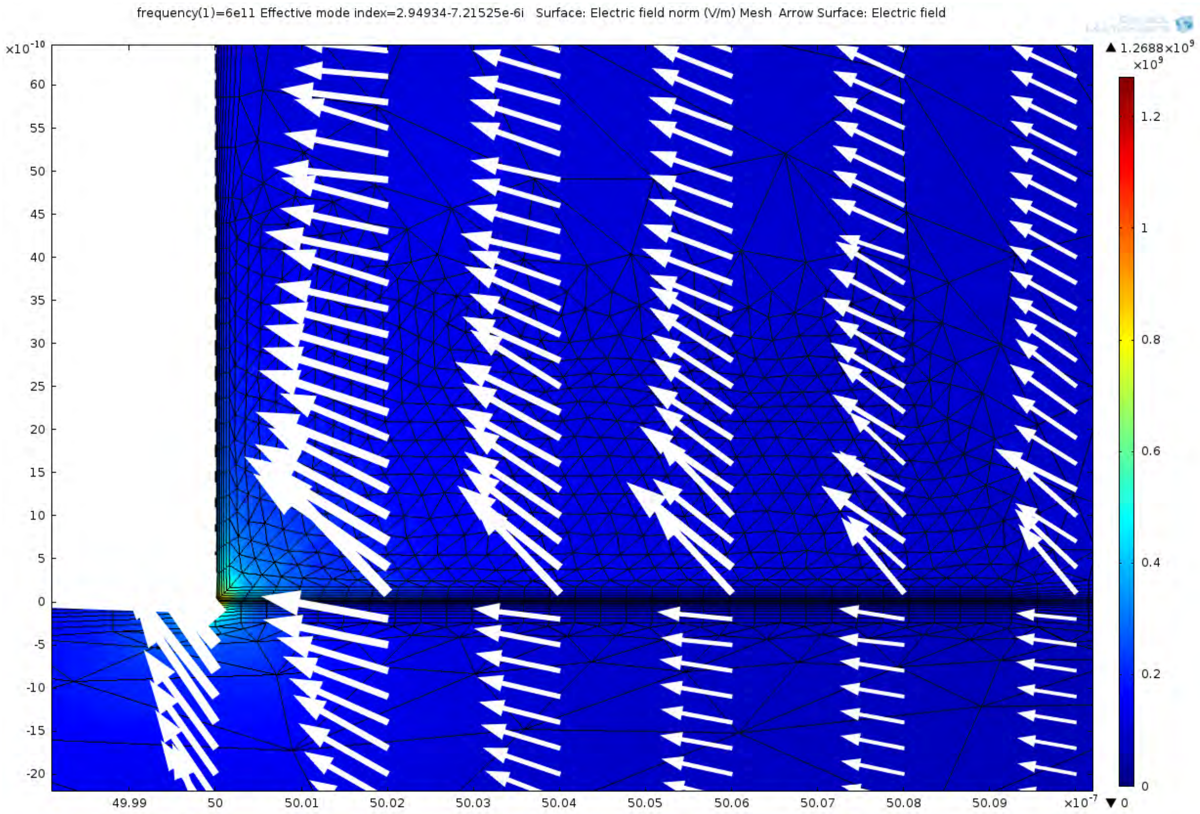


Figure 25 Surface plot of the electric field norm of a microstrip for the TEM mode at 600 GHz, while zoomed into the very densely meshed region at the bottom-right corner of the PEC rectangle. The black lines represent the mesh, the white arrows are an arrow plot of the electric field (in-plane components). No anomalous behaviour is seen, as it should be.

3.2.6 Post processing

After calculating the fields, the participation ratios and losses are calculated in COMSOL. Because of the assumption on the independence of the electric field of the thickness the surface dielectrics inside the interface, equations (2.1) and (2.3) can be simplified to (3.3) and (3.4) respectively, defining t_{sdi} as the surface dielectric layer thickness ($3\ \mathrm{nm}$) and with the line integral running across width of the surface dielectric layer with coordinate s_{sdi}:

$$\frac{1}{Q} = \underbrace{0.002}_{loss\ tangent} \underbrace{\frac{\varepsilon_{sdi} t_{sdi} \int \frac{|E|^2}{\sqrt{1+|E|^2/E_s^2}} ds_{sdi}}{W'}}_{participation\ ratio} \tag{3.3}$$

$$W' = \frac{\int \varepsilon |E|^2 dA_{system}}{2} \tag{3.4}$$

The noise has no literature available for comparison and is hence only calculated for model 1b, where (2.4) may be simplified to:

$$\frac{S}{f_r^2} = \frac{\kappa(\nu, f, T)}{4E_s l} \frac{t \int \frac{|E|^4}{\sqrt{1+|E|^2/E_s^2}} ds}{W'^2} \tag{3.5}$$

If as in model 1b, the saturation field is included, the main post-processing is done in Matlab after exporting the data on the fields from COMSOL. This requires an externally introduced discretization, as the coordinates on which the fields must be evaluated, must be supplied by the user. This is done as follows:

All interfaces are uniformly sampled with at least 10^5 points, treating the corner also as a separate interface. For CPWs only, the large aspect ratios sometimes cause troubles when evaluating the fields at the corners, so only there the number of points is limited to 10^3, which for such a small region is still more than sufficient. Fields are evaluated at $3 \cdot 10^{-3}\ \mathrm{nm}$ distance from the exact interface boundaries, to prevent sampling on the boundary itself where COMSOL averages the fields from both sides.

Concerning the determination of the “best” system size as described in the subsection on meshing earlier, this is based on participation ratios without saturation field calculated in COMSOL as an approximation, as exporting from COMSOL the field data from all calculated resonators is simply unfeasible. However, the deviations due to wrong system sizes far exceed the error made in that approximation, which justifies this procedure.

3.2.7 Results

Overall, agreement with [37] (whose results are shown in Table 3 and Figure 26 (left)) is very good, see Table 4, Table 5 and Figure 26 (right), except at the second CPW case for the metal-dielectric surface. This has been investigated and an exponential decrease with overetch is observed in COMSOL. Considering [37] shows an inconsistent overetch dependency of metal-dielectric surface loss and all other results agree, the discrepancy is attributed to a numerical error in [37] and not to the simulations of model 1.

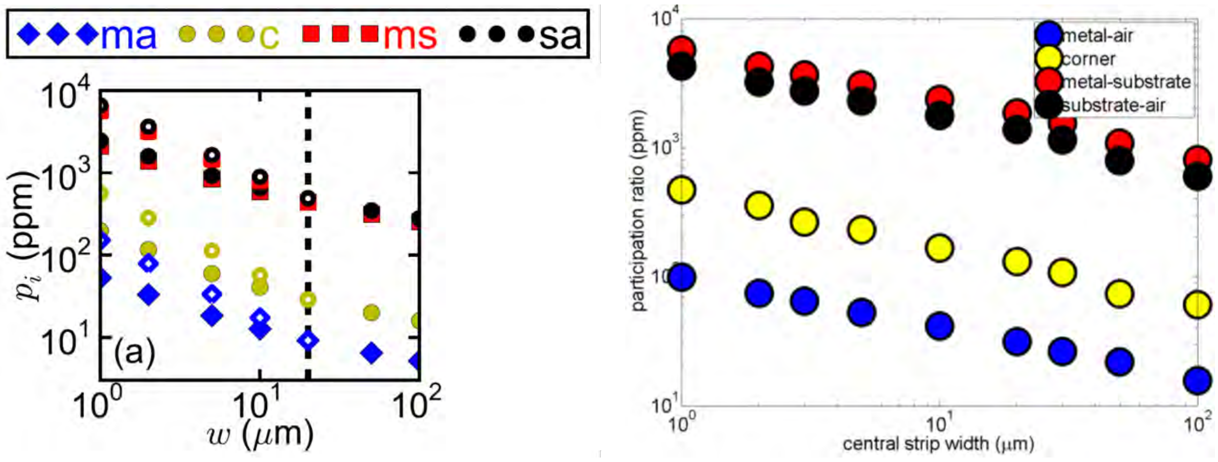
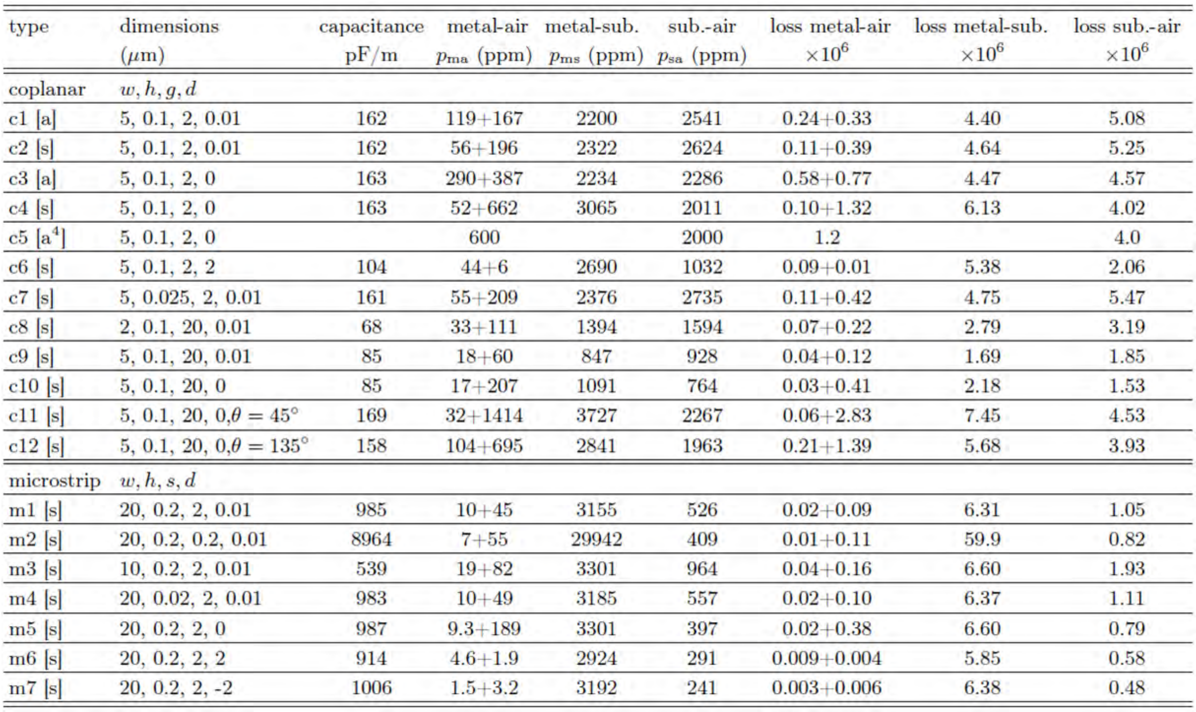


Figure 26 Participation ratios versus central strip width (in $\mu\mathrm{m}$) for CPWs with film thickness $0.3\ \mu\mathrm{m}$ and gap width $2\ \mu\mathrm{m}$. Left: results figure from [37].
Right: Model 1b at $-90\ \mathrm{dBm}$ internal power, which is the unsaturated regime as the model used in [37] also has no saturation fields.

Table 3 Participation ratios and losses for CPWs and microstrips with various geometries, table from [37].



type	dimensions (μm)	capacitance pF/m	metal-air p_{ma} (ppm)	metal-sub. p_{ms} (ppm)	sub.-air p_{sa} (ppm)	loss metal-air $\times 10^6$	loss metal-sub. $\times 10^6$	loss sub.-air $\times 10^6$
coplanar	w, h, g, d							
c1 [a]	5, 0.1, 2, 0.01	162	119+167	2200	2541	0.24+0.33	4.40	5.08
c2 [s]	5, 0.1, 2, 0.01	162	56+196	2322	2624	0.11+0.39	4.64	5.25
c3 [a]	5, 0.1, 2, 0	163	290+387	2234	2286	0.58+0.77	4.47	4.57
c4 [s]	5, 0.1, 2, 0	163	52+662	3065	2011	0.10+1.32	6.13	4.02
c5 [a^4]	5, 0.1, 2, 0		600		2000	1.2		4.0
c6 [s]	5, 0.1, 2, 2	104	44+6	2690	1032	0.09+0.01	5.38	2.06
c7 [s]	5, 0.025, 2, 0.01	161	55+209	2376	2735	0.11+0.42	4.75	5.47
c8 [s]	2, 0.1, 20, 0.01	68	33+111	1394	1594	0.07+0.22	2.79	3.19
c9 [s]	5, 0.1, 20, 0.01	85	18+60	847	928	0.04+0.12	1.69	1.85
c10 [s]	5, 0.1, 20, 0	85	17+207	1091	764	0.03+0.41	2.18	1.53
c11 [s]	5, 0.1, 20, 0,$\theta = 45°$	169	32+1414	3727	2267	0.06+2.83	7.45	4.53
c12 [s]	5, 0.1, 20, 0,$\theta = 135°$	158	104+695	2841	1963	0.21+1.39	5.68	3.93
microstrip	w, h, s, d							
m1 [s]	20, 0.2, 2, 0.01	985	10+45	3155	526	0.02+0.09	6.31	1.05
m2 [s]	20, 0.2, 0.2, 0.01	8964	7+55	29942	409	0.01+0.11	59.9	0.82
m3 [s]	10, 0.2, 2, 0.01	539	19+82	3301	964	0.04+0.16	6.60	1.93
m4 [s]	20, 0.02, 2, 0.01	983	10+49	3185	557	0.02+0.10	6.37	1.11
m5 [s]	20, 0.2, 2, 0	987	9.3+189	3301	397	0.02+0.38	6.60	0.79
m6 [s]	20, 0.2, 2, 2	914	4.6+1.9	2924	291	0.009+0.004	5.85	0.58
m7 [s]	20, 0.2, 2, -2	1006	1.5+3.2	3192	241	0.003+0.006	6.38	0.48

Table 4 Results from model 1 as calculated by COMSOL for losses in CPWs for various surfaces, differences are with respect to [37], e.g. -9 means model 1 underestimates results from [37] by 9 %.

Configuration (μm)	Metal-air loss$\times 10^6$	% diff	Dielectric-metal loss$\times 10^6$	% diff	Dielectric-air loss$\times 10^6$	% diff
$\boldsymbol{w = 5, h = 0.1, g = 2, d = 0.01}$	0.10	-9	4.38	-6	5.17	-1
$\boldsymbol{w = 5, h = 0.1, g = 2, d = 2}$	0.08	-9	1.21	-78	1.93	-6
$\boldsymbol{w = 5, h = 0.025, g = 2, d = 0.01}$	0.10	-10	4.54	-4	5.36	-2
$\boldsymbol{w = 5, h = 0.1, g = 20, d = 0.01}$	0.03	-17	1.44	-15	1.63	-12
$\boldsymbol{w = 2, h = 0.1, g = 20, d = 0.01}$	0.06	-13	2.57	-8	3.01	-6

Table 5 Results from model 1 as calculated by COMSOL for losses in microstrips for various surfaces, differences are with respect to [37], e.g. -9 means model 1 underestimates results from [37] by 9 %.

Configuration (μm)	Metal-air loss$\times 10^6$	% diff	Dielectric-metal loss$\times 10^6$	% diff	Dielectric-air loss$\times 10^6$	% diff
$\boldsymbol{w = 20, h = 0.2, s = 2}$	0.02	-8	6.31	0	1.07	1
$\boldsymbol{w = 20, h = 0.2, s = 0.2}$	0.01	-9	59.89	0	0.86	5
$\boldsymbol{w = 10, h = 0.2, s = 2}$	0.03	-8	6.60	0	1.98	3
$\boldsymbol{w = 20, h = 0.02, s = 2}$	0.02	-6	6.37	0	1.13	2

Also interesting to note is that there are no electromagnetic fields in the direction of propagation, meaning that the field distribution corresponds to a pure TEM mode, as can be expected for perfect metals with a lossless dielectric [35]. However, in practice, this will be a quasi-TEM mode with small out-of-plane field components compared to the in-plane ones. To illustrate the fields, Figure 27 shows an example of the calculated electromagnetic field in a CPW.

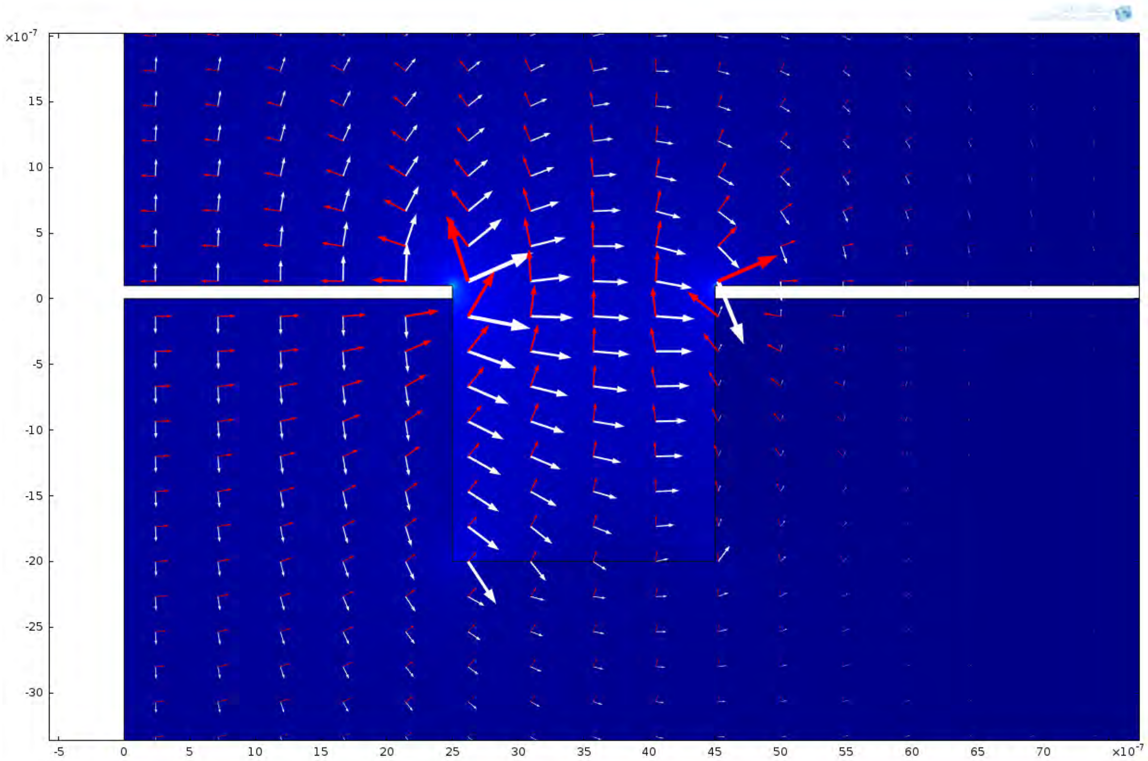


Figure 27 Example of electric (white arrows) and magnetic fields (red arrows) in a CPW calculated in COMSOL, with the electric field norm surface plotted, peaking at the perfect metal edges. Numbers on the axes denote length scales in $\mathbf{m}$.

Calculations from model 1b for the loss and the noise are given in Figure 28 to Figure 31 for CPWs and microstrips. The introduction of loss tangents only shifts the loss levels of each surface, while the saturation fields create a point after which a $\sqrt{P}$ slope is observed. These values do not affect the nature of the numerical calculations and for application in the experimental section should be determined from the data. For these reasons, the figures resulting from model 1b are stated without comparison to literature. Note that the plots are not perfectly smooth, but this is the inevitable numerical inaccuracy of not having exactly identical meshing for all widths.

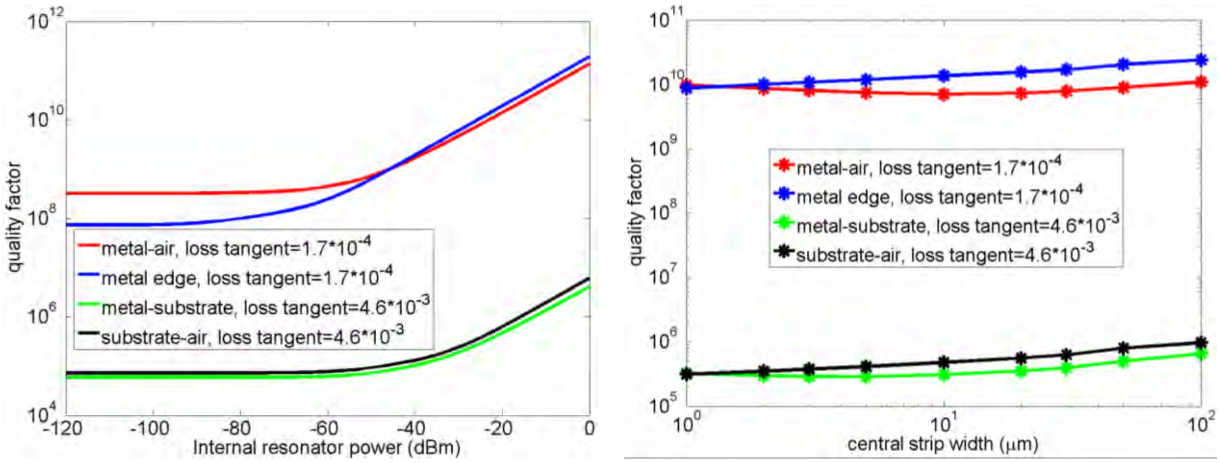


Figure 28 Left: Quality factors versus internal resonator power (in dBm) for CPWs for four interfaces: substrate-air (black), metal (top side)-air (red), substrate-metal (green) and metal edge–air (blue) with superconducting film thickness $\mathbf{0.3\ \mu m}$, film width $\mathbf{3\ \mu m}$ and gap width $\mathbf{2\ \mu m}$, for four interfaces as calculated by COMSOL model 1b. Right: Quality factors versus central strip width (in $\mathbf{\mu m}$) for CPWs at $\mathbf{-25\ dBm}$ internal power.

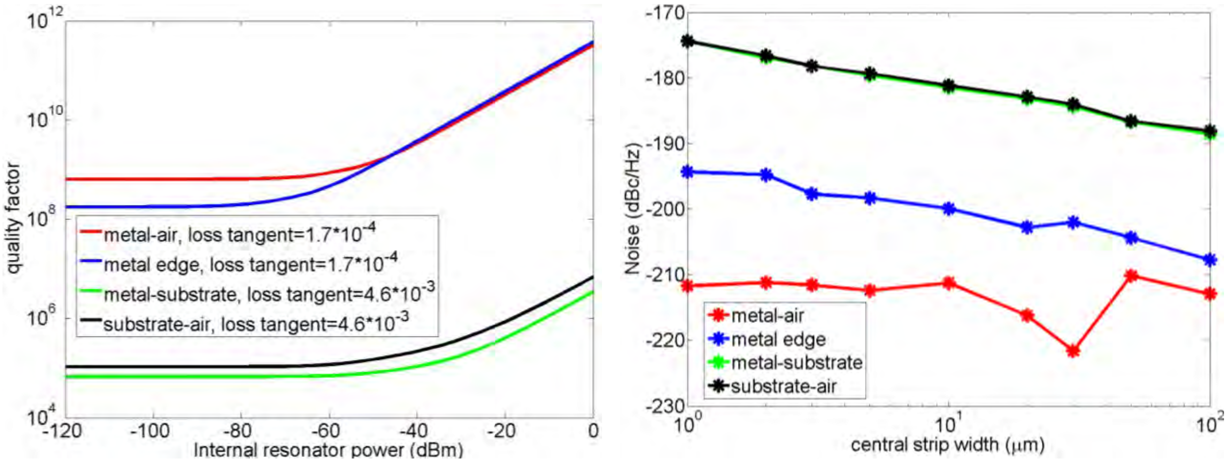


Figure 29 Left: Quality factors versus internal resonator power (in dBm) for microstrips with dielectric thickness $4\ \mu\mathrm{m}$ film thickness $0.3\ \mu\mathrm{m}$ and film width $3\ \mu\mathrm{m}$, for four interfaces: substrate-air (black), metal (top side)-air (red), substrate-metal (green) and metal edge–air (blue) as calculated by COMSOL model 1b. Right: Quality factors versus central strip width (in $\mu\mathrm{m}$) for microstrips at $-90\ \mathrm{dBm}$ internal power.

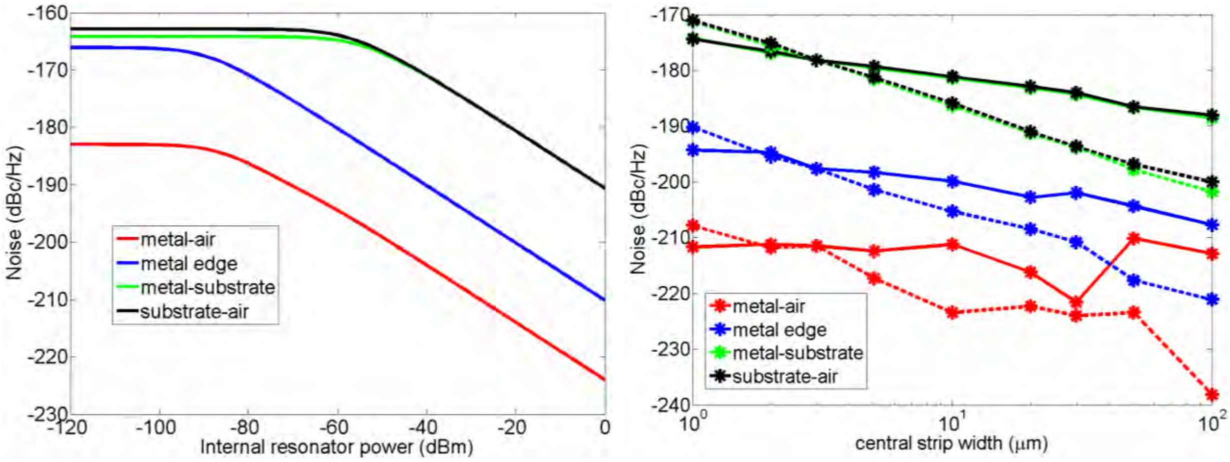


Figure 30 Left: Noise (in $\mathrm{dBc/Hz}$) versus internal resonator power (in dBm) for CPWs with film thickness $0.3\ \mu\mathrm{m}$, film width $3\ \mu\mathrm{m}$ and gap width $2\ \mu\mathrm{m}$, for four interfaces: substrate-air (black), metal (top side)-air (red), substrate-metal (green) and metal edge–air (blue) as calculated by COMSOL model 1b. Right: Noise (in $\mathrm{dBc/Hz}$) versus central strip width (in $\mu\mathrm{m}$) for CPWs with gap width $2\ \mu\mathrm{m}$ (solid) and $2w/3$ (dashed) at $-25\ \mathrm{dBm}$ internal power.

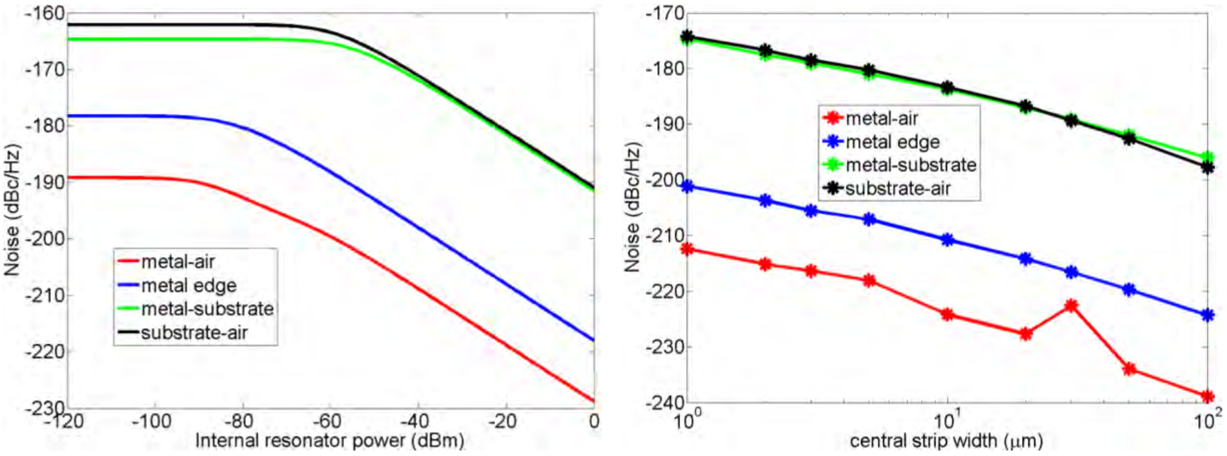


Figure 31 Left: Noise (in $\mathrm{dBc/Hz}$) versus internal resonator power (in dBm) for microstrips with dielectric thickness $4\ \mu\mathrm{m}$, film thickness $0.3\ \mu\mathrm{m}$ and film width $3\ \mu\mathrm{m}$, for substrate-air (black), metal-air (red), substrate-metal (green) and metal edge–air (blue) interfaces as calculated by COMSOL model 1b. Right: Noise (in $\mathrm{dBc/Hz}$) versus central strip width (in $\mu\mathrm{m}$) for microstrips at $-25\ \mathrm{dBm}$ internal power.

3.3 Model 2

The next and final step in complexity for the model would be to assume regions of complex conductivity given by [53] (Mattis-Bardeen conductivity σ_{MB}), instead of assuming a perfect metal, see (3.6) to (3.8). Note: in (3.7) the second term is only added if $\Delta - E_p < -\Delta$, with $E_p \equiv \hbar\omega$.

$$\sigma_{MB} = \sigma_1 - i\sigma_2 \tag{3.6}$$

$$\begin{aligned}\frac{\sigma_1}{\sigma_n} = \frac{2}{E_p}\int_{\Delta}^{\infty}\left(\frac{1}{e^{E/kT}+1} - \frac{1}{e^{(E+E_p)/kT}+1}\right)\frac{\left(E^2+\Delta^2+E_pE\right)dE}{\sqrt{E^2-\Delta^2}\sqrt{\left(E+E_p\right)^2-\Delta^2}} \\ + \frac{1}{E_p}\int_{\Delta-E_p}^{-\Delta}\left(1 - \frac{2}{e^{(E+E_p)/kT}+1}\right)\frac{\left(E^2+\Delta^2+E_pE\right)dE}{\sqrt{E^2-\Delta^2}\sqrt{\left(E+E_p\right)^2-\Delta^2}}\end{aligned} \tag{3.7}$$

$$\frac{\sigma_2}{\sigma_n} = \frac{1}{E_p}\int_{\max(\Delta-E_p,-\Delta)}^{\Delta}\left(1 - \frac{2}{e^{(E+E_p)/kT}+1}\right)\frac{\left(E^2+\Delta^2+E_pE\right)dE}{\sqrt{\Delta^2-E^2}\sqrt{\left(E+E_p\right)^2-\Delta^2}} \tag{3.8}$$

where σ_n is the normal state conductivity, which for NbTiN is $0.9 \cdot 10^6\ \mathrm{S/m}$ [54]. The band gap energy Δ is corrected for the non-zero temperature by [55], where a very accurate approximation for $T/T_c < 0.5$ is presented:

$$\Delta = \Delta_0\sqrt{\cos\left(\frac{\pi T^2}{2T_c^2}\right)} \tag{3.9}$$

where Δ_0 is the band gap energy at $T = 0\ \mathrm{K}$. For NbTiN, Δ_0 and T_c are $2.2\ \mathrm{meV}$ and $14.2\ \mathrm{K}$ respectively [17]. Formulae are incorporated in COMSOL by calling a Matlab function which numerically evaluates the expressions by the built-in function *integral*, which has tunable tolerance.

3.3.1 Assumptions

- Both loss and noise are calculated
- Si as dielectric, with bulk loss tangent of $5 \cdot 10^{-6}$ [56]
- κ_{surf} is assumed to be equal to κ_{bulk}, for which the value for SiO$_2$ of $5 \cdot 10^{-26}\ [\mathrm{Vm^2/Hz}]\varepsilon_0^2$ from [35] is taken in absence of a good value for Si.
- Surface dielectric loss tangents from [36] which are $4.6 \cdot 10^{-3}$ and $1.7 \cdot 10^{-4}$ for surface dielectrics on Si and NbTiN respectively (they are denoted in the table in the article as $1/Q_{TLS,0}$)
- Saturation fields E_s with values of 5 and $0.05\ \mathrm{kV/m}$ [36] for surface dielectrics on Si and NbTiN respectively
- Mattis-Bardeen complex conductivity [53] defining the superconductors
- Electric field inside the surface dielectrics (thickness $3\ \mathrm{nm}$) is independent of layer thickness
- The presence of surface dielectrics does not alter the field distribution elsewhere
- Frequency for mode analysis is $600\ \mathrm{GHz}$

- The temperature is $250\ \mathrm{mK}$
- A small overetch of $2.5\ \mathrm{nm}$, for reasons discussed in model 1.

Model 2b

The last assumption is replaced by:

- No overetch

The implications of these assumptions are similar to the ones for model 1, with these exceptions:

- The complex part of the permittivity in the dielectric is non-zero.
- The superconductor must be modelled and meshed.

3.3.2 Boundaries

In contrast with model 1, the PEC boundaries surrounding the perfect metal are no longer necessary. Due to the inclusion of the superconducting region, the PMC is now one continuous line. Concerning the system size, the same meshing strategy is employed as described in model 1.

3.3.3 Meshing

A meshing approach similar to model 1 is taken, with the exception that the CPWs have less corner refinement and the microstrips have eight boundary layers. The other relevant parameters are given in Table 6.

Table 6 Meshing parameters used for model 2 for both CPWs and microstrips.

	CPW	Microstrip
Maximum element size $[\mu\mathrm{m}]$	5	10
Minimum element size $[\mu\mathrm{m}]$	10^{-9}	0.00338
Maximum element growth rate	1.3	1.2
Resolution of curvature	10^{-7}	0.25
Resolution of narrow regions	1	1

3.3.4 Post processing

The addition of dielectric bulk loss requires the bulk field to be sampled as well in post-process. It is uniformly sampled with $2 \cdot 10^6$ points for the part of the dielectric that is below the central strip (and in the CPW case, also including the part below the gap), and logarithmically sampled with $2 \cdot 10^6$ points with decreasing spatial frequency further away from the central strip for the remaining dielectric.

3.3.5 Results

In terms of choosing the correct system size, the microstrips (Figure 34 and Figure 35) experience almost no problems. For all CPWs, the tedious reoptimization procedure as described in Appendix is performed, resulting in Figure 32 and Figure 33.

Assuming saturation fields of 5 and $0.05\,\mathrm{kV/m}$ for surface dielectrics on Si and NbTiN respectively, microstrips and CPW should be operated at powers higher than $-30\,\mathrm{dBm}$ to benefit from saturation in loss. Powers higher than $-55\,\mathrm{dBm}$ respectively are necessary to benefit from saturation in noise. These are all reasonable powers to operate these resonators, this may vary if different values are assumed. Unfortunately, the dominant surfaces (metal-dielectric and dielectric-air) require the highest powers to saturate independent of the saturation field. Also note that the high bulk noise probably means that the value for κ in bulk is different than from the surface, as in [35], where the TLS model is introduced, it is already mentioned that κ depends on the TLS distribution, which could be different for the bulk compared to a surface.

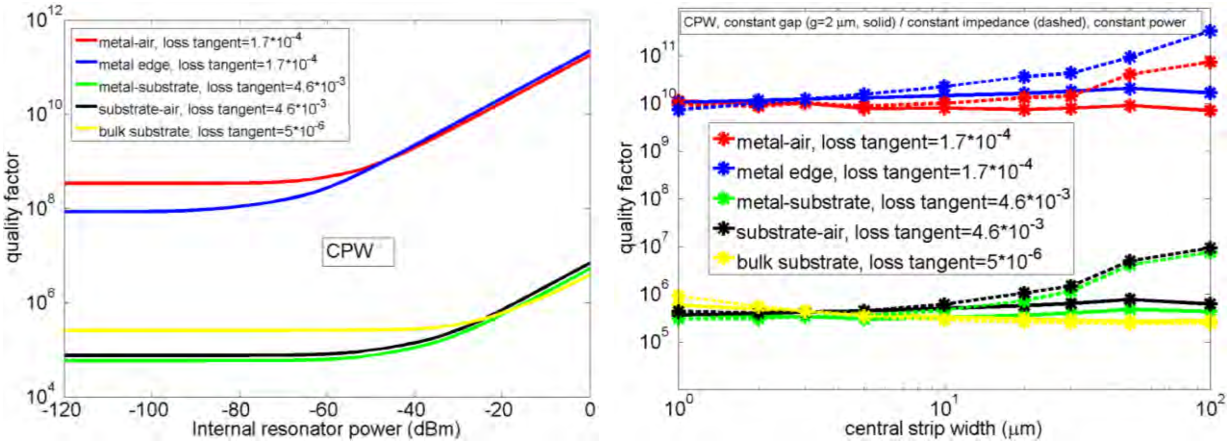


Figure 32 Left: Quality factors versus internal resonator power (in $\mathbf{dBm}$) for CPWs with superconducting film thickness $\mathbf{0.3\ \mu m}$, film width $\mathbf{3\ \mu m}$ and gap width $\mathbf{2\ \mu m}$, for four interfaces: substrate-air (black), metal (top side)-air (red), substrate-metal (green) and metal edge–air (blue) and bulk (yellow) as calculated by COMSOL.
Right: Quality factors versus central strip width (in $\mathbf{\mu m}$) for CPWs with gap width $\mathbf{2\ \mu m}$ (solid) and $\mathbf{2w/3}$ (dashed) at $\boldsymbol{P_{int} = -25\ \mathrm{dBm}}$.

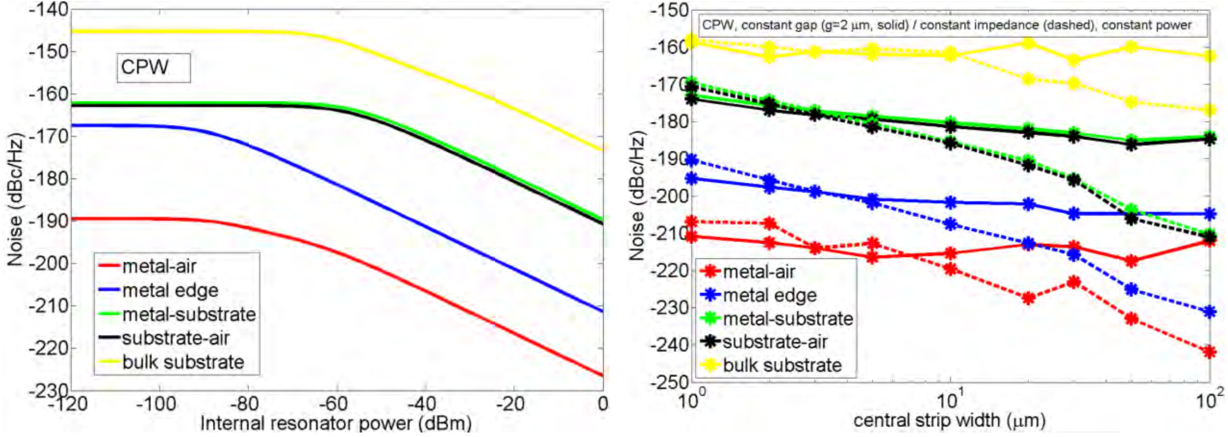


Figure 33 Left: Noise (in $\mathbf{dBc/Hz}$) versus internal resonator power (in $\mathbf{dBm}$) for CPWs with superconducting film thickness $\mathbf{0.3\ \mu m}$, film width $\mathbf{3\ \mu m}$ and gap width $\mathbf{2\ \mu m}$, for four interfaces: substrate-air (black), metal (top side)-air (red), substrate-metal (green) and metal edge–air (blue) and bulk (yellow) as calculated by COMSOL.
Right: Noise (in $\mathbf{dBc/Hz}$) versus strip width (in $\mathbf{\mu m}$) for CPWs with gap width $\mathbf{2\ \mu m}$ (solid) and $\mathbf{2w/3}$ (dashed) at $\boldsymbol{P_{int} = -25\ \mathrm{dBm}}$.

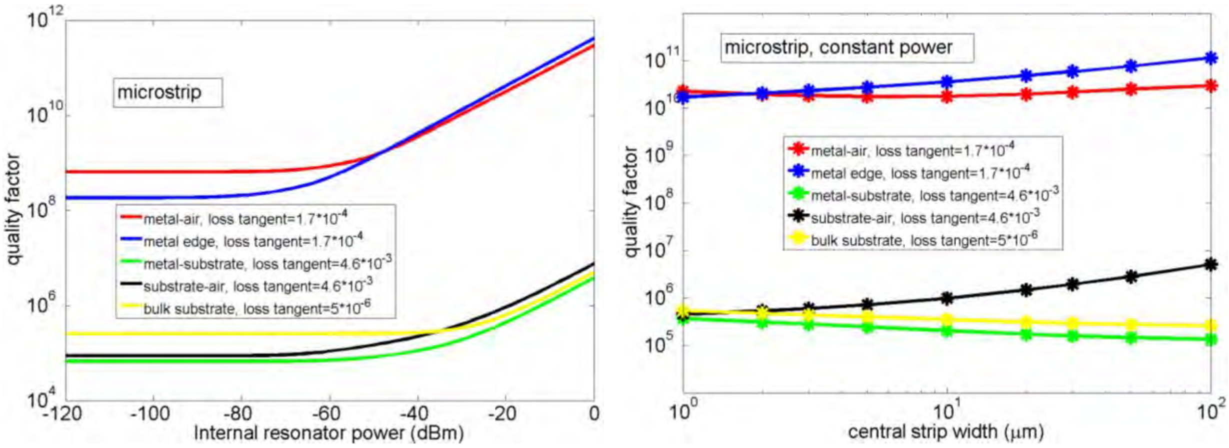


Figure 34 Left: Quality factors versus internal resonator power (in dBm) for microstrips with dielectric thickness $4\ \mu\mathrm{m}$, superconducting film thickness $0.3\ \mu\mathrm{m}$ and film width $3\ \mu\mathrm{m}$, for substrate-air (black), metal-air (red), substrate-metal (green) and metal edge–air (blue) interfaces and dielectric bulk (yellow) as calculated by COMSOL.
Right: Q-factors versus strip width (in $\mu\mathrm{m}$) for microstrips at $P_{int} = -25\ \mathrm{dBm}$.

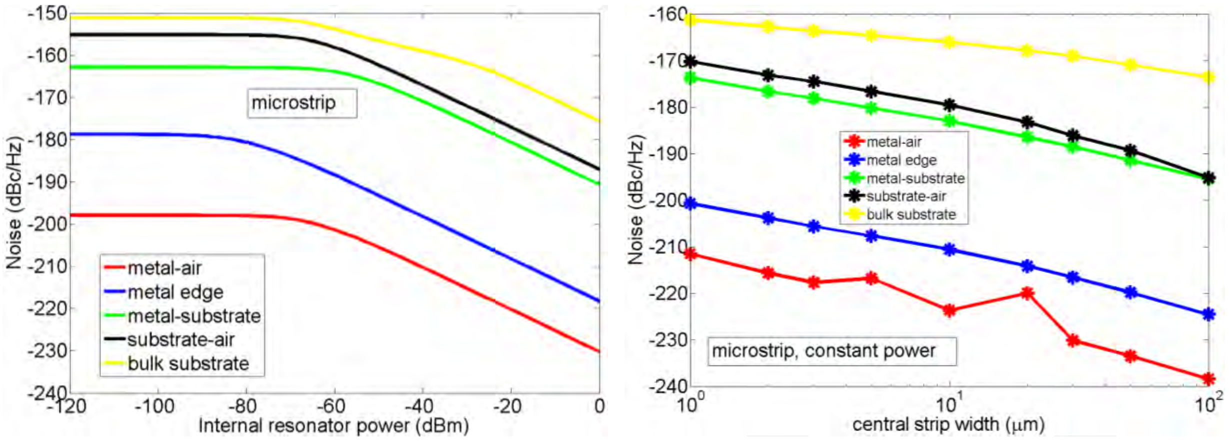


Figure 35 Left: Noise (in $\mathrm{dBc/Hz}$) versus internal resonator power (in dBm) for microstrips with dielectric thickness $4\ \mu\mathrm{m}$, superconducting film thickness $0.3\ \mu\mathrm{m}$ and film width $3\ \mu\mathrm{m}$, for substrate-air (black), metal-air (red), substrate-metal (green) and metal edge–air (blue) interfaces and dielectric bulk (yellow) as calculated by COMSOL.
Right: Noise (in $\mathrm{dBc/Hz}$) versus central strip width (in $\mu\mathrm{m}$) for microstrips at $P_{int} = -25\ \mathrm{dBm}$.

When varying geometry, constant internal power has been chosen so far to ensure comparable TLS environments. It may be worthwhile to also consider other criteria, such as constant voltage and constant current. However, for example for CPWs the noise optimization would always involve the long, wide part of a hybrid CPW, while only the current inside the other, high responsivity part would be of interest. This means that fixing the current is less relevant than fixing the voltage. The constant voltage and current plots are shown in the Appendix where voltage and current follow from the characteristic impedance (approximated by analytical formulae from [14] and from [57], whose formulae result from conformal mapping approximations) and internal power as in [29].

When comparing fixed power and fixed voltage, the argument for fixing V would be that it seems a better proxy for constant TLS environment. This is because it is likely that TLSs consist of dipole moments coupling to electric fields, hence it is the voltage that matters in physics terms. For experimental reasons, P_{int} is the sensible parameter to keep constant. For example for microstrips, the highest P_{int} that can be used could be increased by widening the geometry. However, increasing the volume would lead to a fast deterioration of the responsivity. So in practice P_{int} is not a free parameter that may be geometrically optimized, in a sense it is already fixed. For this reason, a discussion with fixed V should be interpreted as a relevant physics-based analysis on TLSs. For practical purposes, the fixed P_{int} discussion is more useful. In the figures, the difference may be summarized as follows:

- Wide microstrips resonators must be operate at larger powers P to get the same electric field (same voltage V if thickness is not varied) in the resonator. Because of the saturation in loss and noise as a function of internal power, the width dependence of microstrips at constant voltage moves more towards improving loss and noise with increasing width.
- For constant gap CPW, the impedance change is small, particularly when $w \gg g$. This means that this effect of higher P at larger widths when keeping V constant is less pronounced, bringing the constant power and constant voltage power index n closer to each other.
- For constant impedance CPW, one would expect no difference in fixing P, I or V. The origin of the apparent loss difference in particular between V and P is likely caused by the choice of fixing P at $-25\ \mathrm{dBm}$, right at the saturation point of the dielectric bulk, which is important for the total as well. The fixed V chosen corresponds to a higher P_{int}. The total width dependence is hence slightly different, as the fixed voltage data is in another saturation regime than the fixed power data. The fixed I also corresponds to a relatively high P_{int}, as it can be seen that the width dependencies of the fixed V and fixed I data are already similar. Also, the noise has much lower saturation powers, so there is no discrepancy there. All surfaces are completely saturated, so that the width dependency is power independent.

After calculating the loss and noise for the same geometries (varying central strip width and for CPWs, with constant impedance as well) as for model 1b, it is of interest to extend this to other relevant geometrical variations, namely varying gap width for CPWs with and without keeping the total width fixed, and for microstrips varying dielectric thickness, as shown in Figure 36 to Figure 38. Note that fixing the width and increasing the gap means increasing the impedance for CPWs. At fixed V, this lowers the P_{int} and due to saturation, wider CPWs have higher loss. Because of the lower P_s for the noise, this effect is less pronounced in the noise power indices.

Finally, taking into consideration the results from model 1, it is important to determine the influence of the overetch on the loss and noise. These results are presented in Figure 39 and Figure 40, where only the internal power is kept constant. Constant voltage and constant current would yield the same results, as the impedance remains constant while varying the overetch.

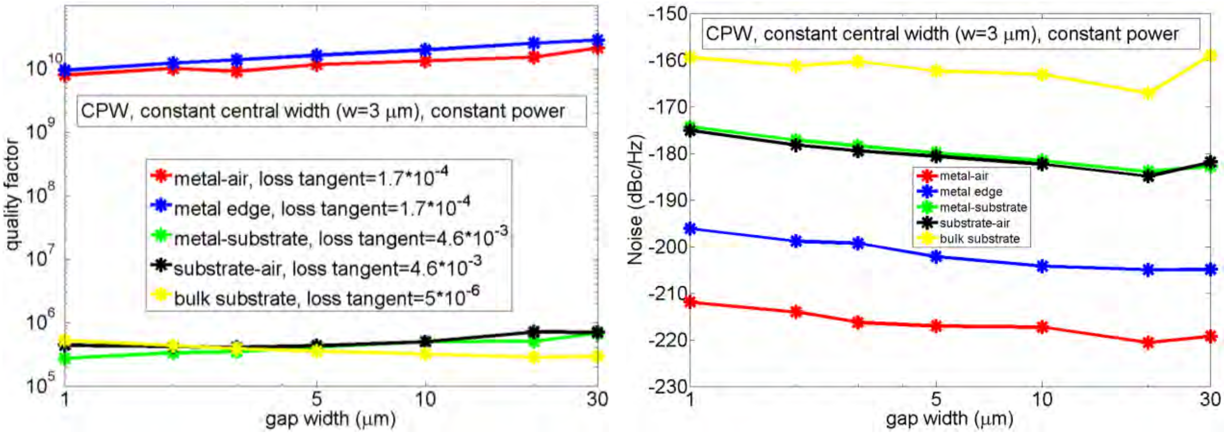


Figure 36 Left: Quality factors versus gap width (in μm) for CPWs with superconducting film thickness $0.3\ \mu m$ and film width $3\ \mu m$, for four interfaces: substrate-air (black), metal (top side)-air (red), substrate-metal (green) and metal edge–air (blue) and bulk (yellow) at $P_{int} = -25\ \mathrm{dBm}$ as calculated by COMSOL.
Right: Noise (in $\mathrm{dBc/Hz}$) versus gap width (in μm) for the same CPWs at $P_{int} = -25\ \mathrm{dBm}$.

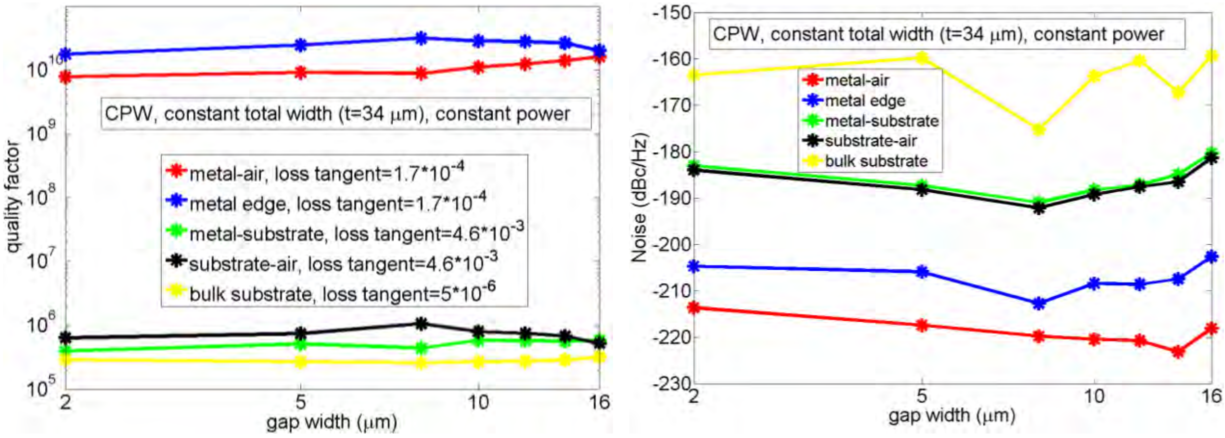


Figure 37 Left: Quality factors versus gap width (in μm) for CPWs with superconducting film thickness $0.3\ \mu\text{m}$ and total width $w + 2g = 34\ \mu\text{m}$, for four interfaces: substrate-air (black), metal (top side)-air (red), substrate-metal (green) and metal edge–air (blue) and bulk (yellow) at $P_{int} = -25\ \text{dBm}$ as calculated by COMSOL.
Right: Noise (in dBc/Hz) versus gap width (in μm) for the same CPWs at $P_{int} = -25\ \text{dBm}$.

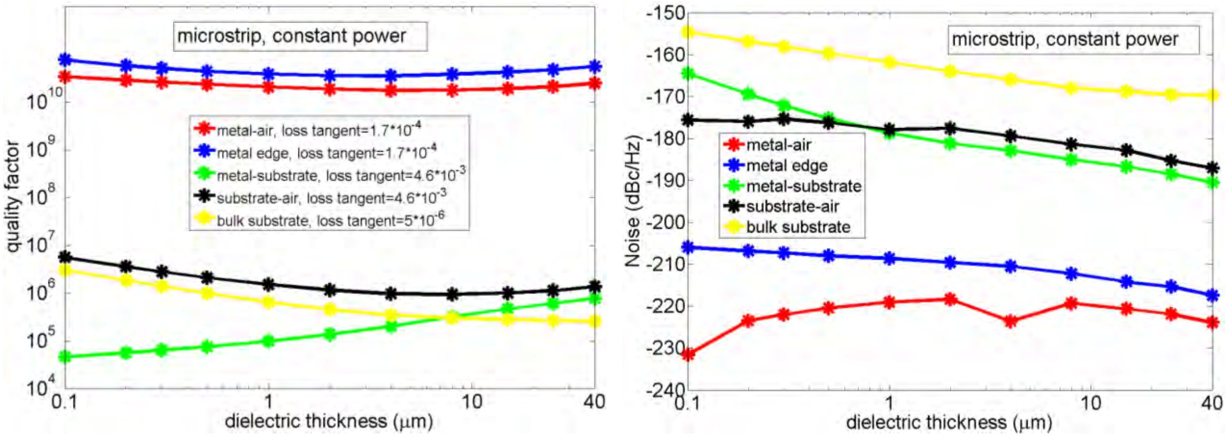


Figure 38 Left: Quality factors versus dielectric thickness (in μm) for microstrips with superconducting film thickness $0.3\ \mu\text{m}$ and central strip width $10\ \mu\text{m}$, for four interfaces: substrate-air (black), metal (top side)-air (red), substrate-metal (green) and metal edge–air (blue) and bulk (yellow) at $P_{int} = -25\ \text{dBm}$ as calculated by COMSOL.
Right: Noise (in dBc/Hz) versus dielectric thickness (in μm) for the same microstrips at $P_{int} = -25\ \text{dBm}$.

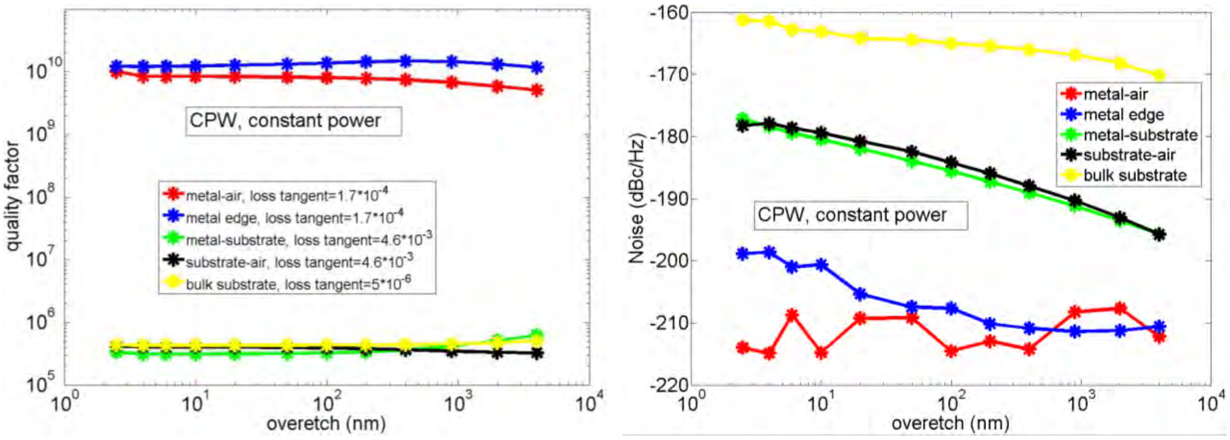


Figure 39 Left: Quality factors versus overetch (in nm) for CPWs with superconducting film thickness $0.3\ \mu\text{m}$ and film width $3\ \mu\text{m}$, for four interfaces: substrate-air (black), metal (top side)-air (red), substrate-metal (green) and metal edge–air (blue) and bulk (yellow) at $P_{int} = -25\ \text{dBm}$ as calculated by COMSOL.
Right: Noise (in dBc/Hz) versus overetch (in nm) for the same CPWs at $P_{int} = -25\ \text{dBm}$.

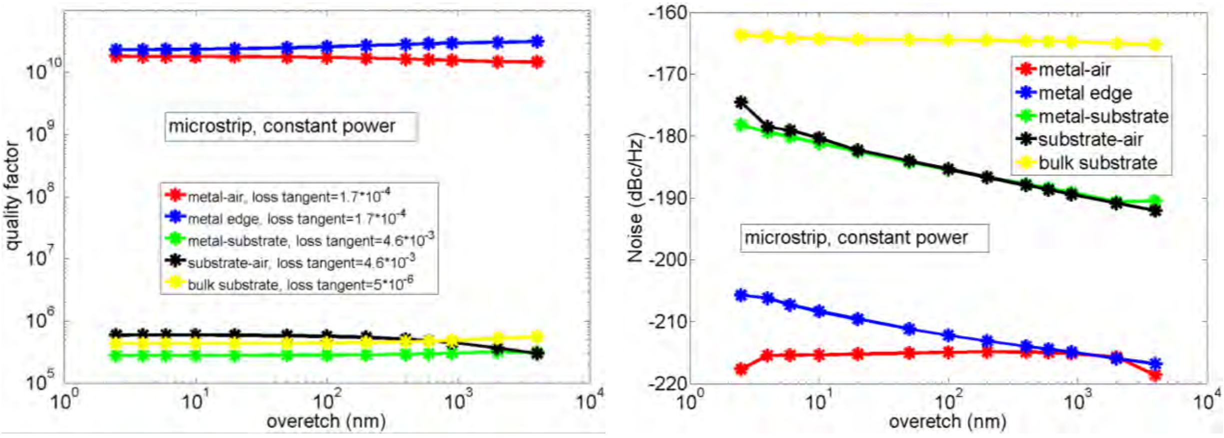


Figure 40 Left: Quality factors versus overetch (in nm) for microstrips with superconducting film thickness 0.3 $\mu\mathrm{m}$ and central strip width 3 $\mu\mathrm{m}$, for four interfaces: substrate-air (black), metal (top side)-air (red), substrate-metal (green) and metal edge–air (blue) and bulk (yellow) at $P_{int} = -25$ dBm as calculated by COMSOL.
Right: Noise (in $\mathrm{dBc/Hz}$) versus overetch (in nm) for the same microstrips at $P_{int} = -25$ dBm.

Having made all relevant gemotrical variation, it is now time to state the conclusions of the numerical efforts, which are given in the next subsection.

3.3.5.1 Conclusions: fixed power

- **Microstrip, loss:** The dielectric-metal interface is the dominant surface for wide resonators in particular. This is because the field is gets more concentrated inside the dielectric for wider microstrips, exposing the dielectric-air interface to smaller fields. The benefit from widening for the substrate-air interface is cancelled out by the metal-substrate interface and dielectric bulk, which become more lossy for wider strips. In total, there is a very small negative effect of widening due to the importance of the metal-substrate. By contrast, making the dielectric thicker is beneficial for the dominant metal-substrate. This makes sense: as the strongest field lines are mostly vertical, the field gets stretched by thickening, which is a strategy for reducing participation ratios and loss. The metal-air interface does not play a role, so varying film height is not useful. Quantitatively, the geometrical dependencies for the loss are $w^{-0.12}$ and $s^{0.21}$. Surprisingly, increasing overetch does not decrease the loss, in sharp contrast with the conclusions from model 1. However, when realizing the key difference between model 1 and 3, this effect becomes clear: overetching reduces the average field strengths in the surface layers, so the participation ratios should go down, but simultaneously, the reduction in TLS saturation keeps the ratios roughly constant. Only at $P \ll P_s$, the loss is again reduced.
- **Microstrip, noise:** The steeper power dependence of the noise on the electric field makes a clear width dependence of about $1/w$ of all surfaces including the metal-dielectric interface noticeable, in contrast to the loss plots. This makes sense as from (2., the denominator in the noise scales with volume V^2 while the numerator only scales with V. The dominant surfaces are the metal-dielectric and dielctric-air interfaces. The geometrical dependencies on the width and dielectric thickness for the noise are $w^{-1.16}$ and $s^{-0.73}$. Widening the microstrip improves the noise for all surfaces as the size of the surfaces is increased (the same $1/V$ as mentioned earlier), whereas the thicker dielectric is mostly beneficial for the metal-substrate interface, as it is the only surface which can benefit from stretched fields. All surfaces maintain the same size, so the effect of thicker dielectrics is smaller than from wider strips. When increasing the overetch, the electric field dependence for the noise is stronger than for

the Q-factor, so that the reduction in average field strength will reduce the noise regardless of the power, as was found in literature [27]. Quantitatively, the geometrical dependencies on the overetch for the noise is $d^{-0.45}$.

- **CPW, loss:** The metal-dielectric and dielectric-air interfaces dominate the losses and have the highest participation ratios. In fact, the metal-dielectric and dielectric-air behave very similarly, which may already explain the difficulty in literature to attribute the dominant loss source to either of the two interfaces. As the metal-air interface has negligible loss and noise contributions, modifications affecting only the latter surface hence do not help (varying film height). In contrast, varying film width and gap width by contrast influence the losses, as they modify the electric fields near the two dominant interfaces. Widening of these interfaces stretches the electric fields, lowering the participation ratios and hence lowering the losses. The geometrical dependencies on the loss are $w^{0.0}$ (constant gap), $t^{0.14}$ (constant impedance) and $g^{0.06}$, implying that geometrical influences on the quality factors are small. Note that this is not in contrast with the conclusions from model 1b, where the loss was evaluated in the unsaturated regime of $P_{int} = -90\ \mathrm{dBm}$.
- **CPW, noise:** The constant gap CPW have the lowest width dependence, while the constant impedance CPWs have the largest width dependence. This can be understood by noting that increasing the gap stretches the fields, reducing the noise, but increasing the width simultaneously will give the $1/V$ bonus as also seen in microstrips. Only increasing the width means not the whole geometry is wider, so there this latter effect is less pronounced. Overetching provides a good increase in performance as the electric field peaks near the metal-dielectric-air corner. In terms of surfaces, the metal-dielectric and the dielectric-air surfaces are dominant. The geometrical dependencies on the noise are $w^{-0.59}$ (constant gap), $t^{-2.01}$ (constant impedance), $g^{-0.57}$ and $d^{-0.56}$. The value of -2.01 is not far from the experimental value from [25] of -1.58. In the case of constant impedance, both geometrical parameters are increased when widening, so that the fields get stretched more in that case, explaining the larger width dependencies. Overall, the noise has a steeper dependence on the electric field than the loss, which explains the larger power indices. The constant gap and strip width dependencies are similar to those found experimentally in [10], see Figure 41.

3.3.5.2 Conclusions: fixed voltage

- **Microstrip, Q:** the loss is almost independent of width (index 0.05), entirely due to the metal-substrate surface. This is because under constant voltage, the electric field values between the plates is also constant for all widths. The most important surface, the metal-substrate interface and the dielectric bulk which is also relevant, will then experience almost no width dependence. Unfortunately, choosing fixed voltage as the TLS measure also completely negates the benefit of making the dielectric thicker and it actually becomes disadvantageous. This is because thicker dielectrics implies lower capacitance, hence higher impedance and therefore lower internal powers, so less saturation. On the other hand, thin dielectrics means higher responsivity, so this result is not completely disappointing. Quantitatively, the geometrical dependencies for the loss are $w^{0.05}$ and $s^{-0.28}$.

- **Microstrip, noise:** the geometrical dependencies for the nosie are $w^{-1.43}$ and $s^{-0.37}$. For the same reason as for the loss, the benefit of thicker dielectrics is somewhat limited.
- **CPW, loss:** the geometrical dependencies are $w^{-0.08}$ (constant gap), $t^{-0.22}$ (constant impedance) and $g^{-0.22}$.
- **CPW, noise:** the geometrical dependencies are $w^{-0.73}$ (constant gap), $t^{-1.98}$ (constant impedance), $g^{-0.43}$ and $d^{-0.53}$. Particularly for the constant impedance case the noise has a very large geometrical dependence, as both the central strip and the gap are increased. The constant gap and central strip width dependencies match again those in [10], see Figure 41.

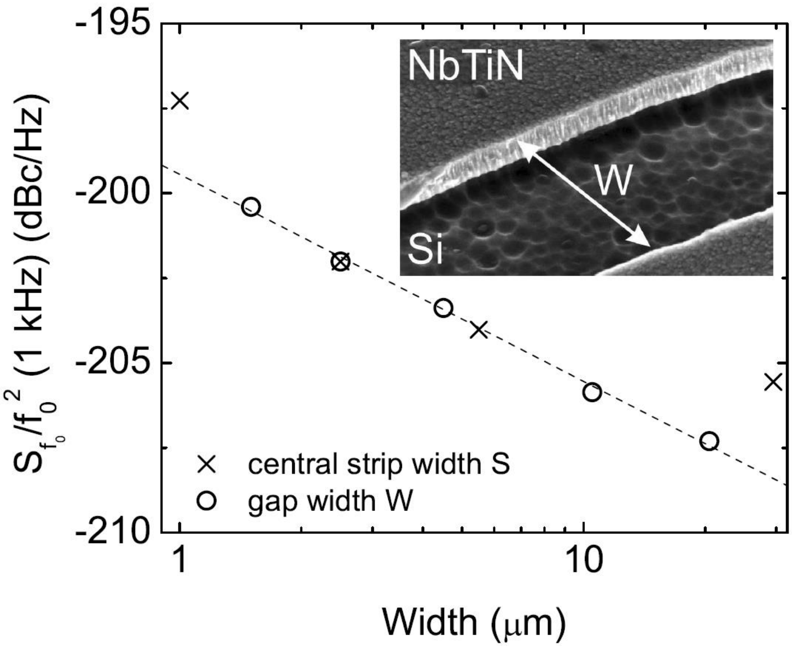


Figure 41 Figure from [10]. Plotted is the dependence of the noise in $\mathrm{dBc/Hz}$ on the either the central strip width (crosses) with constant gap width or on the gap width (circles) with constant central strip width.

3.4 Model comparison

While model 2 is on paper the most realistic model, with superconductivity added compared to model 1b, the effect of this addition is limited and mostly visible for small widths comparable to the penetration depth. Regarding microstrips, the superconductivity has a positive effect on the losses for small widths, but for large widths the results of the metal-dielectric and dielectric-air interfaces converge to the perfect metal case. The effect remains visible for the metal-air interface, but this loss was already negligible. This convergence for all surfaces is seen for the CPWs. This means that for wide resonators, model 1b would already provide a very accurate picture, without the added complexity and computational effort. For widths below roughly $10\ \mu\mathrm{m}$, the more realistic model 2 is more appropriate to model losses.

The comparison between models in terms of the noise provides another insight in the added value of model 2, as for CPWs the difference between the figures seems comparable to the scatter of the plots. Even for small widths, the perfect metal assumption seems a good approximation. The power dependence figures do not provide new conclusions either. Remarkably, for microstrips this is not the case and the total noise increases compared to the perfect metal case by about $2-3\ \mathrm{dBc/Hz}$ for all widths, for the substrate air interface alone by up to $4\ \mathrm{dBc/Hz}$. This means that for microstrips, explicitly modelling the complex conductivity is always useful. Intuitively, this makes sense: the main difference between the two models is that model 2 has penetration of the field inside the superconductor. This will for CPWs only be significant for narrow central strips, because for wide CPWs the fraction of the superconductor that is penetrated becomes insignificant. For microstrips, the field penetrates the microstrip across the whole width, regardless of the central strip width, so that influence never becomes negligible.

The benefit of model 2 is that it also has dielectric loss and noise included. For both CPWs and microstrips, this seems a very relevant addition as the bulk loss can compete with the dominant surfaces. The same cannot be concluded for the noise yet as that value depends heavily on the value taken for the noise spectral coefficient κ, which can vary from material to material.

3.4.1 Note on out-of-plane electric field dependency

So far all numerical simulations have been calculated using a 2D cross section of the microstrip-p or CPW resonator, assuming a constant electric field strength distribution along the length direction of the resonator. This is a good approximation of a LEKID, where an interdigitated capacitor is connected to a microstrip or CPW, as the latter part would experience almost constant electric field strength with respect to the direction along the resonator, while the capacitive part has almost no field. In other situations, as for example in a quarter-wave resonator, the dependency is more subtle. The electric field is maximal at the end that is coupled to the transmission line and minimal at the shortened end. More specifically, from [35], the dependency of the electric field strength on the position z in along a resonator with length l is given by:

$$E(z) \propto \cos\left(\frac{\pi z}{2l}\right) \tag{3.10}$$

Accounting for this in the volume integrals for the Q and noise ((2.1) and (2.4) respectively), this will lead to a difference of 0 and $1.76\ \mathrm{dBc/Hz}$ respectively in the unsaturated regime and $27\ \%$ and $2.30\ \mathrm{dBc/Hz}$ respectively in the saturated regime. However, the fit parameters regarding the geometrical parameters will be virtually unchanged, as within a regime the offset is constant.

3.5 Validation numerical results with existing literature

Given that from the previous section follows that the results from model 2 and model 1b are different, but not by an enormous margin, this increase the confidence in the validity of the results from model 2. Still, in absence of equivalent numerical results in literature, the best validity check is comparison with experimental data.

3.5.1 Comparison with peer-reviewed literature

Figure 42 and Figure 43 show the numerical results from COMSOL for CPWs presented in the same manner as in literature. The value of κ from [25] using a sapphire substrate is not applicable here, so it is a fit parameter, estimated from the $3\ \mu\mathrm{m}$ data from [25] which is unaffected by the noise contribution from the coupler. If the data corrected for this coupler contributions is compared to the numerical calculations, good agreement is observed. The width dependency is comparable and while in the experimental data there is some scatter in the power dependencies, they are all around the $P^{-0.5}$ dependency exhibited in the results from model 2 based on TLSs.

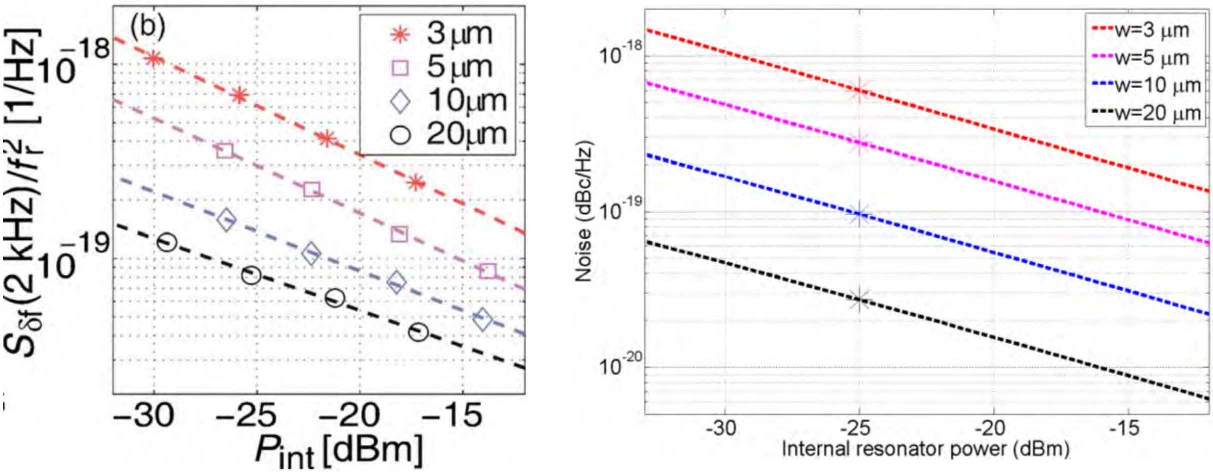


Figure 42 Noise (in $\mathrm{dBc/Hz}$) versus internal power (in dBm) for CPWs with gap width $2w/3$ and four film widths at $2\ \mathrm{kHz}$ and $55\ \mathrm{mK}$.

Left: CPW noise figure from [25], results are not corrected for the noise contribution of the coupler. The dashed lines represent fitted power laws.

Right: Total noise arising from three surfaces (substrate-air, metal-air and substrate-metal) as calculated by COMSOL model 2 are taken into account. Bulk noise is disregarded, as κ_{bulk} is not well known. Prefactor in equation (2.5) for κ at $2\ \mathrm{kHz}$ estimated is $7 \cdot 10^{-27}\ [\mathrm{Vm^2/Hz}]$.

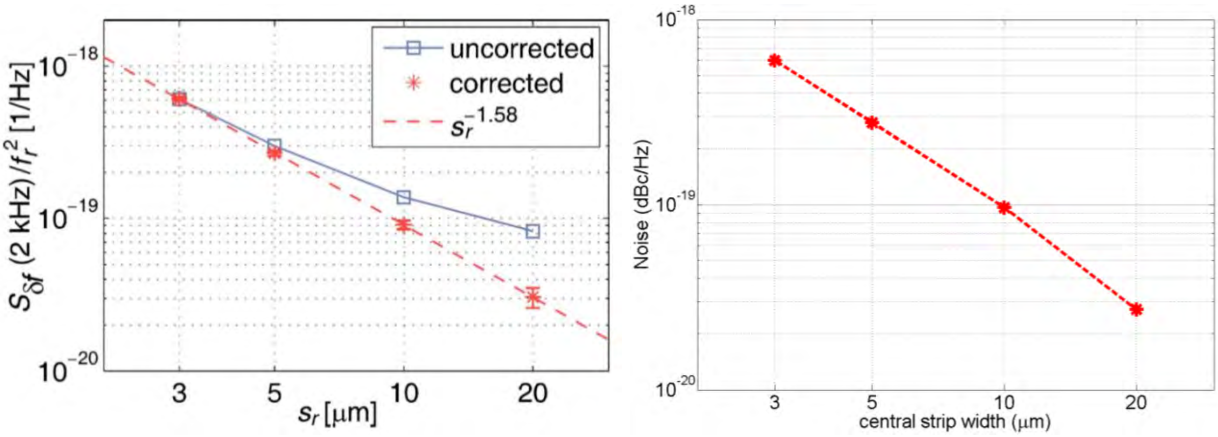


Figure 43 Noise (in $\mathrm{dBc/Hz}$) versus central strip width (in $\mu\mathrm{m}$) for CPWs with gap width $2w/3$ at $2\ \mathrm{kHz}$, $55\ \mathrm{mK}$ and $P_{int} = -25\ \mathrm{dBm}$.

Left: CPW noise figure from [25]. "Corrected" refers to the removal of the noise contribution of the coupler.

Right: Total noise arising from three surfaces (substrate-air, metal-air and substrate-metal) as calculated by COMSOL model 2 are taken into account. Bulk noise is disregarded, as κ_{bulk} is not well known. Prefactor in equation (2.5) for κ at $2\ \mathrm{kHz}$ estimated is $7 \cdot 10^{-27}\ [\mathrm{Vm^2/Hz}]$.

3.5.2 Comparison with other literature

Figure 44 and Figure 45 show the numerical results from COMSOL for microstrip loss and noise respectively, presented in the same manner as in literature. Regarding the Q-factors, agreement with data from [29] is excellent, except that no plateau arises for MSL1 at high electric fields. Note that the COMSOL model had already incorporated the better dielectric (crystalline Si instead of $\mathrm{SiN_x}$), with higher dielectric constant, and uses the saturation field of Si, which may explain why bulk TLS saturation does not limit the Q for MSL1 (what would cause a plateau) in the numerical results. For the noise, agreement is not so good as the noise is well overestimated, but improves for larger widths at high powers because the experimental data deviates slightly from the theoretical $1/\sqrt{P}$ dependence. One cause for this discrepancy is the unknown overetch in the resonators from [29]. The author commented that an overetch will be presented, while in the model only a $2.5\ \mathrm{nm}$ overetch is assumed. Results from Table 24 show that this could affect the results significantly. A more important factor is the incorrectly modelled bulk behaviour, as the materials used in [29] are NbTiN on SiN, while the value of κ is based on Nb on $\mathrm{SiO_2}$. As in [35] it is mentioned that the value of κ depends on the TLS distribution, this may very well differ among materials. Furthermore, with a bulk κ such that its noise contribution becomes significant compared to the surface contribution, the excessive width dependence can be reduced. This motivates a summary of available literature on various materials to determine material dependent influences on the noise given in Chapter 5.

With the validity of model 2 established, it is now possible to use the numerical analysis to make a sensible chip design, so that conclusions on the dominant TLS locations can be drawn. To condense the amount of information of the figures in the previous subsections on model 2, the results of varying internal power and dimensions are quantitatively summarized by fitting simple functions to them. This allows for a handle on the dependencies which is accurate enough for the chip designs, but is not intended to be the prediction on loss and noise for any geometry. These fit results can be found in Appendix: Model 2 – Fit summary and beyond

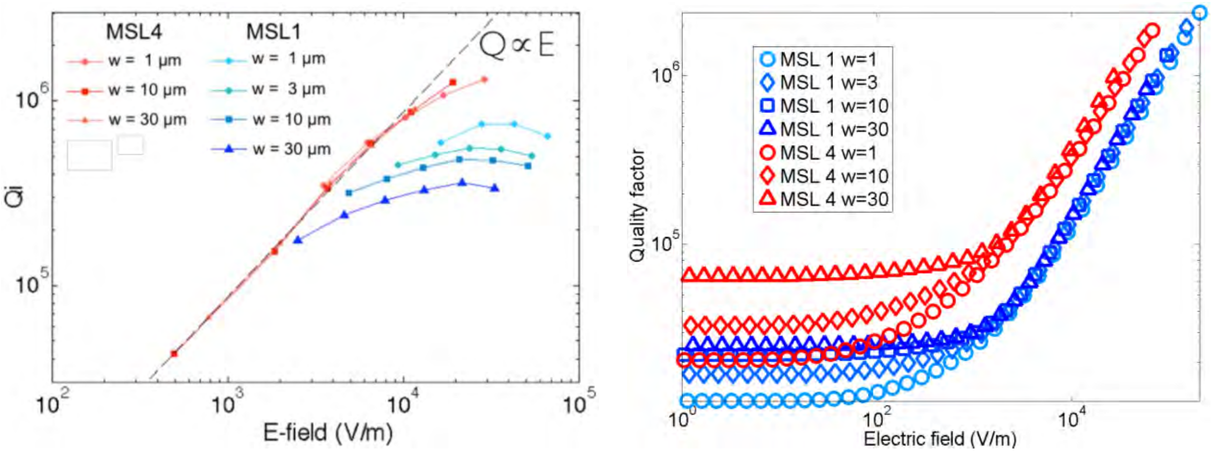


Figure 44 Quality factor versus 'electric field' (in $\mathrm{V/m}$) for microstrips with film thickness of $300\ \mathrm{nm}$, two dielectric thicknesses (MSL1 = $1\ \mu\mathrm{m}$, MSL4 = $4\ \mu\mathrm{m}$) and four film widths at $315\ \mathrm{mK}$.
Left: Microstrip data figure from [29]. Right: Total loss arising from three surfaces (substrate-air, metal-air and substrate-metal) and bulk dielectric ($\varepsilon = 11.9$) as calculated by COMSOL are taken into account. Electric field follows from characteristic impedance (approximated by formulae from [57]) and internal power as in [29].
Right: Quality factor versus 'electric field' (in $\mathrm{V/m}$) for microstrips with film thickness of $300\ \mathrm{nm}$, two dielectric thicknesses (MSL1 = $1\ \mu\mathrm{m}$, MSL4 = $4\ \mu\mathrm{m}$) and four film widths. Right: Noise versus internal power for two dielectric thicknesses and three film widths.

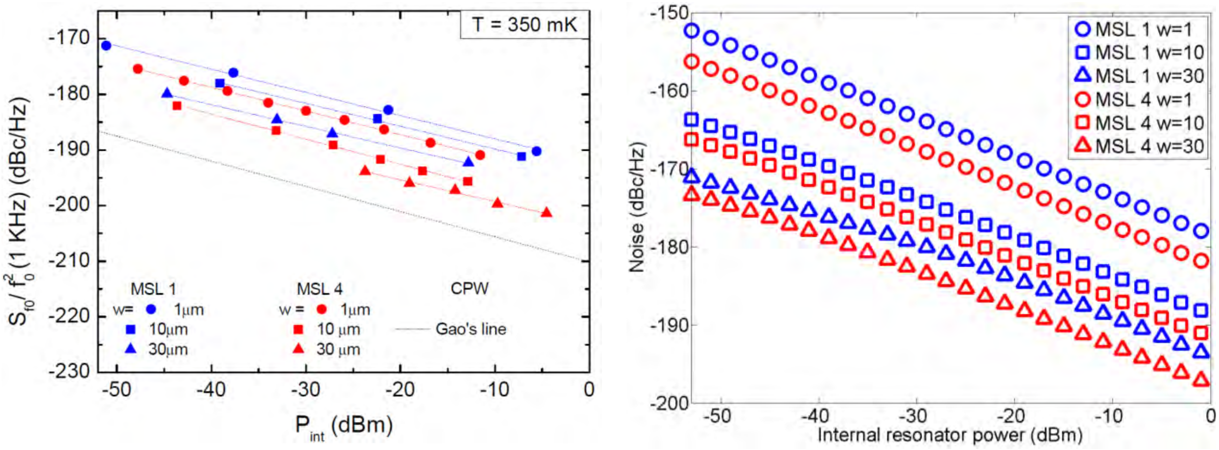


Figure 45 Noise (in $\mathrm{dBc/Hz}$) versus internal power (in dBm) for microstrips with film thickness of $300\,\mathrm{nm}$, two dielectric thicknesses (MSL1 = $1\,\mu\mathrm{m}$, MSL4 = $4\,\mu\mathrm{m}$) and three film widths at $1\,\mathrm{kHz}$ and $315\,\mathrm{mK}$.
Left: Microstrip data figure from [29].
Right: Total noise arising from the same three surfaces as calculated by COMSOL are taken into account. Bulk noise is disregarded, as κ_{bulk} is not well known. Prefactor in equation (2.5) for κ at $1\,\mathrm{kHz}$ estimated from [35] is now $4 \cdot 10^{-26}$ $[\mathrm{Vm^2/Hz}]$ instead of $5 \cdot 10^{-26}$ $[\mathrm{Vm^2/Hz}]$.

3.6 Chip design

Using the results from model 2, it is now possible to device an experiment that would definitively determine the dominant TLS source in the experimental system and to obtain material dependent parameters. The primary goal is to distinguish between bulk and surface TLSs for microstrips and CPWs, while the secondary goal is to distinguish between the surface contributions if the surface TLSs are dominant. As varying the dielectric thickness requires the fabrication of many chips, the only option for microstrips is to vary the central strip width, because in model 1 it was already shown that varying film height is not very useful. For CPWs, its reminaing degrees of freedom can be varied in three different ways: constant gap, constant impedance and constant central strip width.

Given Table 25 and Table 26 on fits for CPWs, the most prominent geometrical dependencies are visible in the noise and not in the loss. The strongest difference in width dependencies of bulk and surfaces can be seen in the constant impedance case, where bulk dominated noise would yield a $1/w$ dependence, whereas all surface contributions scale as $1/w^2$. The latter facilitates the distinction of the bulk from the surfaces, but it will not help to reach the secondary goal. Furthermore, the constant impedance case does not have many useful dependencies in terms of the loss as the metal edge is not expected to dominate. This makes it impossible to design an experiment with CPWs only that could distinguish metal-substrate from substrate-air.

Interestingly, this is not true for microstrips. If the bulk does not dominate the loss, an improvement of the loss for wider resonators would point towards the substrate-air as the dominant source, as the metal-edge contribution is negligible. Then, one could go one step further by stating that that if the distinction between the substrate surfaces can be made for microstrips, this is also strong evidence for the same conclusion in CPWs, if both are fabricated under the same conditions.

The dielectric of choice is SiN, as the fabrication procedure for this dielectric is well known. Further away from the resonators on only the SiN membrane, $400\ \mu\mathrm{m}$ thick Si is beneath the SiN, so that a CPW can be placed there as a reference. As mentioned, varying the film height is not very useful and is fixed to $100\ \mathrm{nm}$, a normal height for Al (e.g. [11]). The motivation for Al is clear from

Table 26: an overetch has a big influence on the noise, but problematically, this overetch is typically unknown. However, wet etching Al will not yield an overetch, which fixes this degree of freedom.

Due to technical restrictions, the minimal central strip width or gap width is $2\ \mu\mathrm{m}$. Starting from $w = 3, g = 2$ to $w = 30, g = 20$ provides a decade in width which should translate in between one or two decades in noise, which is easily observed. The approximately (logarithmically) equally spaced sequence of widths would be $3, 4, 6, 8, 11, 16, 22$ and $30\ \mu\mathrm{m}$.

Additionally, to better determine the influence of the thin dielectric SiN layer, a separate CPW chip is made containing the same geometries as on SiN-Si, to which the results from the CPW on only the SiN membrane may be compared. The influence of the Si can be distinguished by placing the same CPW geometries on only Si. This then yields a chip design as seen in Figure 46.

On all chips, the resonance frequency of the KID with the smallest width is designed to be at $6\ \mathrm{GHz}$, where the other KIDS on the same chip are designed to be in ascending order of both width and frequency, with a spacing of $0.1\ \mathrm{GHz}$. The exception is the reference CPW which is always the highest frequency KID at $0.2\ \mathrm{GHz}$ above the second-highest resonance frequency on the chip. Within the design, the kinetic inductance is taken into account to determine impedance and resonance frequency through [47], using a penetration depth for Al of $92\ \mathrm{nm}$ [11]. The coupling Q is $1.5 \cdot 10^5$.

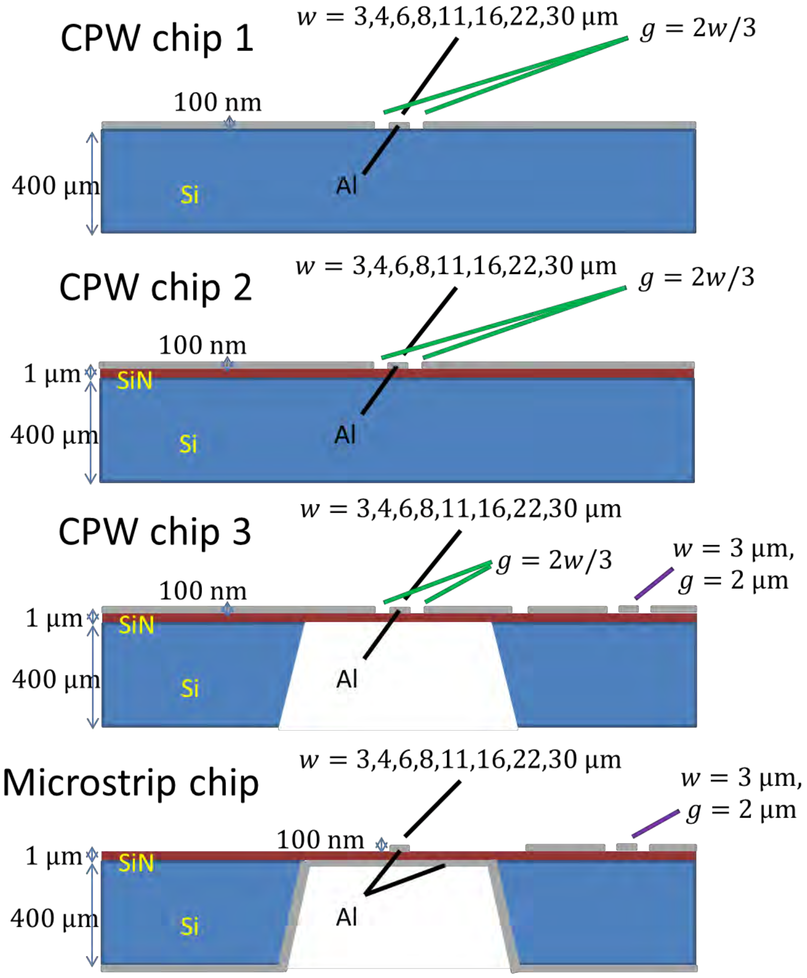


Figure 46 Cross section of the chip design for microstrips and CPWs. Al (grey, $100\ \mathrm{nm}$ thick) is placed on $1\ \mu\mathrm{m}$ SiN (brown) dielectric which is LPCVD deposited on $400\ \mu\mathrm{m}$ Si (blue), the latter having been etched away in the microstrip chip and CPW chip 3. Central strip widths are between 3 and $30\ \mu\mathrm{m}$, gap widths between 2 and $20\ \mu\mathrm{m}$.

4 Fabrication and experimental setup

4.1 Fabrication

The thorough description of all fabrication procedures, which have taken place at SRON, is given in the Appendix, but below a summary of the most important steps is presented.

4.1.1 Al-Si CPW

- $< 100 >$ Si, 3 batches, one with a resistivity of $< 10\ \mathrm{k\Omega cm}$ (to be called low resistivity) and two with $> 10\ \mathrm{k\Omega cm}$ (to be called high resistivity).

- Cleaning has been done in two ways: *thorough cleaning* (applied on one high resistivity wafer) using a Piranha mixture, a $3:1\ \mathrm{H_2SO_4:H_2O_2}$ mixture and dilute HF. The *basic cleaning*, applied on the other high resistivity wafer and the low resistivity wafer involved aceton, IPA and dilute HF.

- $100\ \mathrm{nm}$ Al deposition (LLS, pressure $5\ \mathrm{mTorr}$, power 876 W, Base pressure $< 5 \cdot 10^{-6}\mathrm{mbar}$, substrate rotation: oscillating drum).

- Wet etch patterning using a $16:1:1:2\ \ \mathrm{H_3PO_4:CH_3COOH:HNO_3:H_2O}$ mixture at $29\ ^\circ\mathrm{C}$, resist (AZ6612/AZ6632) pattern removed by acetone.

4.1.2 Al-SiN-Si CPW

This procedure is very similar to the fabrication of the Al-SiN microstrip except for the additional KOH and RIE etch to remove the SiN and Si on the back side of the wafer to yield a SiN membrane and without the Al deposition on the back side of the wafer.

4.1.3 Al-SiN CPW

This procedure is very similar to the fabrication of the Al-SiN microstrip except for the Al deposition on the back side of the wafer.

4.1.4 Al-SiN microstrip

- $< 100 >$ Si with $1\ \mathrm{\mu m}$ SiN on both sides, 2 batches (both high resistivity), acetone cleaned.

- RIE to remove SiN on the back side, KOH etching to remove the Si.

- Then, cleaning has been done in two ways: *thorough cleaning* (applied on one high resistivity wafer) using a Piranha mixture, a $3:1$ $\mathrm{H_2SO_4{:}H_2O_2}$ mixture and dilute HF. The *basic cleaning*, applied on the other high resistivity wafer involved aceton, IPA and dilute HF.

- 100 nm Al deposition (LLS, pressure 5 mTorr, power 876 W, Base pressure $< 5 \cdot 10^{-6}$mbar, substrate rotation: oscillating drum).

- Wet etch patterning using a commercial etchant mixture at 29 ℃, resist (AZ6612) pattern removed by acetone and IPA.

4.2 Experimental setup

All measurements have been performed at SRON, Utrecht, using the same experimental setup as extensively described in [11], without the blackbody, as shown in Figure 47. In the next subsections a brief overview is given on the basics of this setup.

4.2.1 Cooling

As aluminium has a critical temperature of 1.17 K [11], the sample must be cooled to well below 1 K. For this purpose, an adiabatic demagnetization refrigerator (ADR) is used. The working principle of the ADR is as follows: an external magnetic field does work on a salt with random orientations of spins, causing these spins to align with the field. If this is done adiabatically by insulating this system as much as possible, the entropy of the salt does not change (second law of thermodynamics) and only the internal energy (first law of thermodynamics) and hence the temperature increases. If this heat is then dissipated, the entropy is decreased until the salt has cooled to its original temperature. Decreasing the field will then cause the opposite process: the negative work decreases the internal energy and temperature, as desired. In this experiment, two salts are used: gadolinium gallium garnet (GGG) and ferric ammonium alum (FAA). As these salts have limited cooling capacity, a helium filled pulse tube cooler brings the temperature down to about 4 K by repetitively expanding high pressure gas. Then, the GGG performs the initial bulk of the cooling, the latter one brings the temperature of the sample to as low as 60 mK in this experiment.

The magnetic field is generated by applying a current to a superconductor, which can reach a maximum of 36 A. To ensure the cooling process is performed under adiabatic conditions, the current is slowly turned off (at most 0.025 A/s) which avoids large dissipation through eddy currents. Once the desired temperature has been reached, it is then regulated by very small adjustments to the current, which once it reaches zero, will have lost all its cooling power. As the volume of salts is limited, a trade-off exists between how cool the sample is and the amount of time this can be maintained before the salts need to be ‘recharged’.

4.2.2 Measurement

After a microwave signal to read-out the transmission of the resonators is generated, part of this signal is transported through the sample in the cryostat and fed into an IQ-mixer, where it is combined with the other part of the signal which did not travel through the sample. From the measured amplitude reduction and phase shifts, the transmission may be visualized in the complex plane, from which the loss and the noise follow. Instead of the IQ-mixer, a Vector Network Analyser (VNA) can be used, which is faster but noisier, which means that this option is mainly suited for a quick determination of the location of the resonance frequency (compared to the designed value) at which the noise must be measured, but the actual noise measurements are performed using the IQ-mixer. Calibration of both the VNA and the IQ-mixer occurs at $800\ \mathrm{mK}$ for Al, where the transmission line is already superconducting but where the resonance dips are effectively to shallow to be noticed.

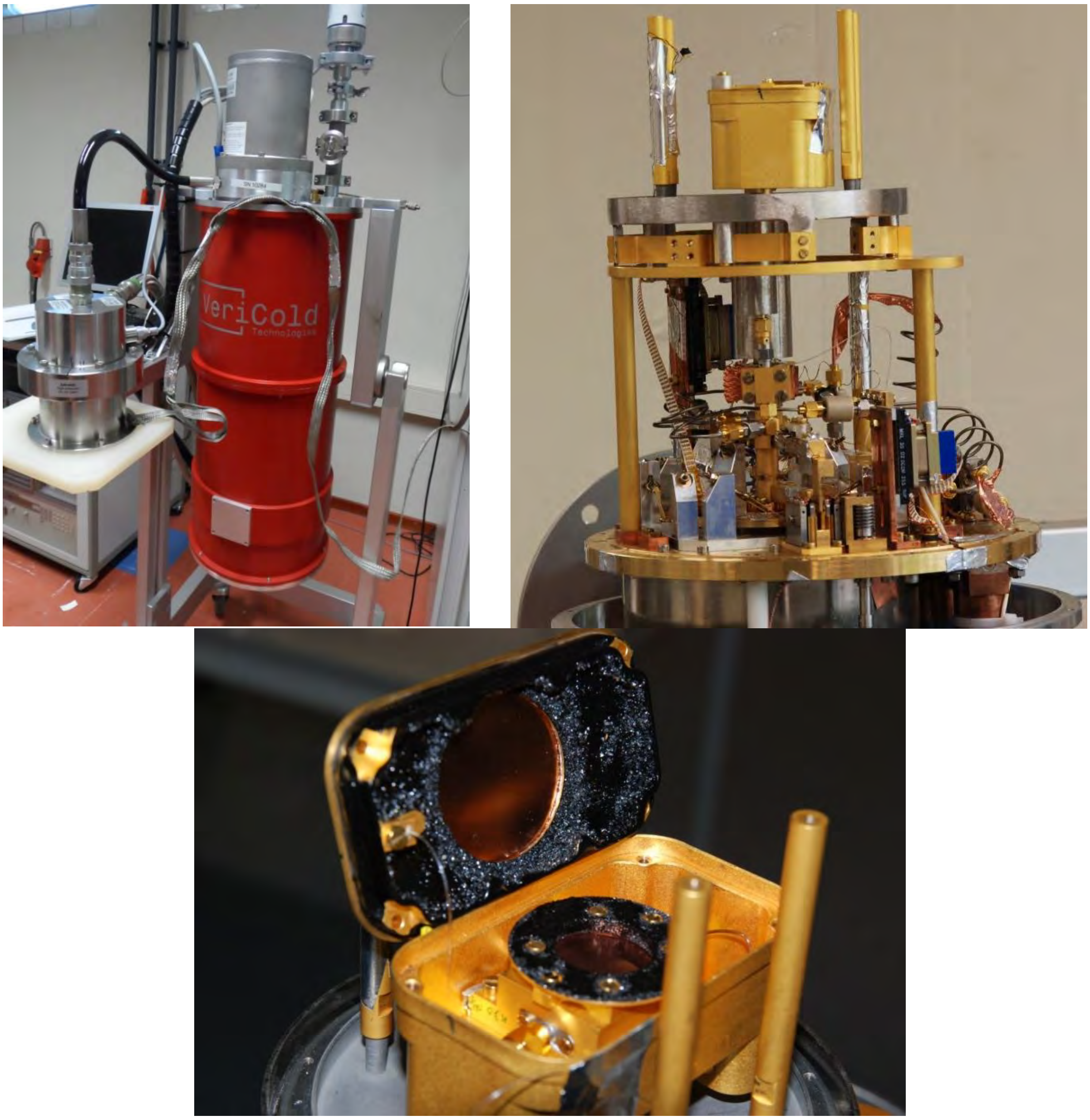


Figure 47 Top left: Overview of the cryostat. Top right: Inside view of the cryostat. At the bottom of the figure, the volume is visible which contains the two salts (FAA and GGG), above that a small gear operates a heat switch between the two salts and at the top of the image the sample holder is visible. Right: Picture of the sample holder, where the box-in-box configuration containing the Stycast coated sample holder for stray light rejection as described in [11] is visible.

5 Experimental Results

5.1 Experimental summary so far

The following figures show a relevant selection from literature of the noise of CPWs and microstrips with various materials. The noise is plotted against the internal power in Figure 48, the geometrical dependence is plotted in Figure 49.

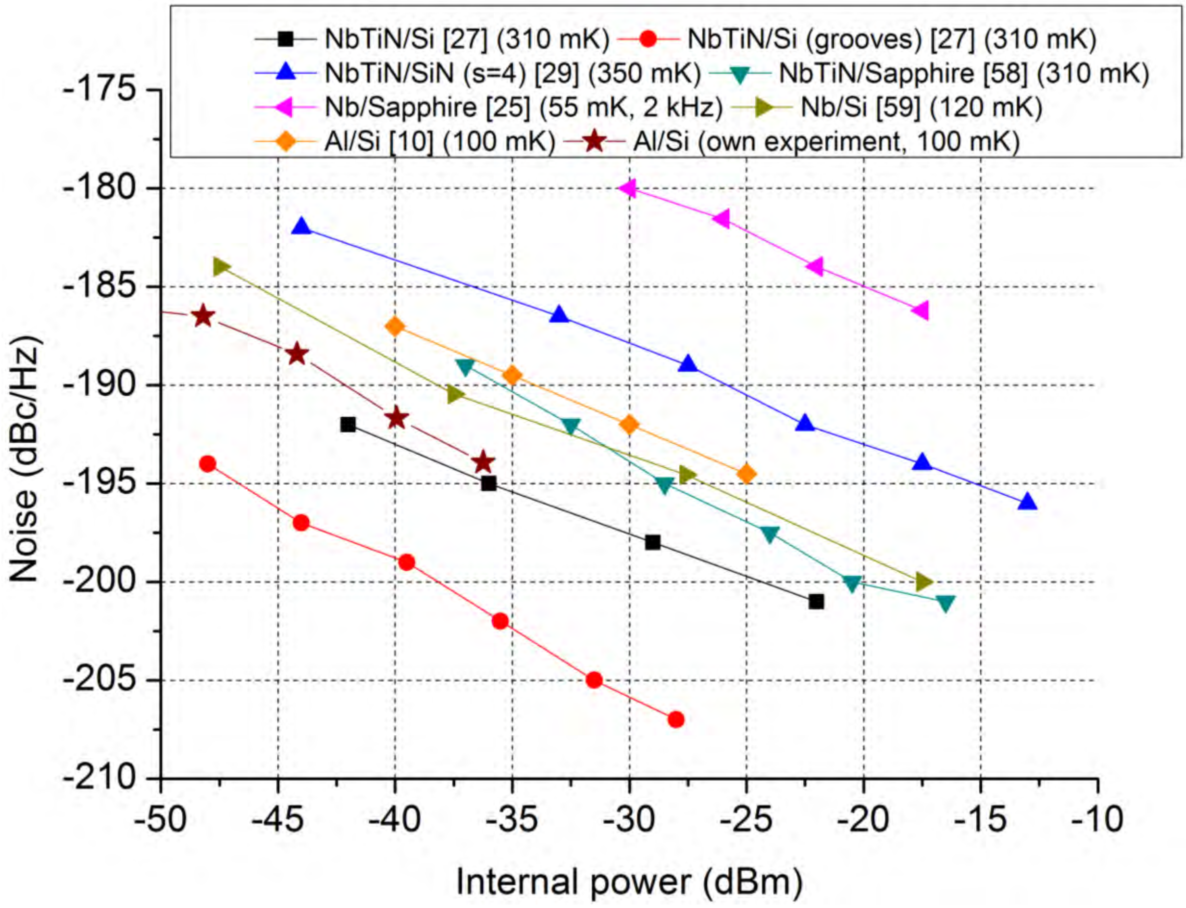


Figure 48 Noise in $\mathrm{dBc/Hz}$ versus internal power in dBm for eight different resonators, all CPWs except the NbTiN/SiN, which is a microstrip. All CPWs have central strip width w of $3\ \mu\mathrm{m}$ and gap width g of $2\ \mu\mathrm{m}$, the microstrip has $w = 10\ \mu\mathrm{m}$ and dielectric thickness of $4\ \mu\mathrm{m}$. The Nb film has a thickness of $120\ \mathrm{nm}$, the NbTiN films have a thickness of $300\ nm$ and the Al film has a thickness of $100\ \mathrm{nm}$. All resonators are measured at $1\ \mathrm{kHz}$ except Nb/Sapphire. Al/Si data from [10] are extrapolated from the value at $P_{int} = -40\ \mathrm{dBm}$ assuming a $1/\sqrt{P}$ dependency.

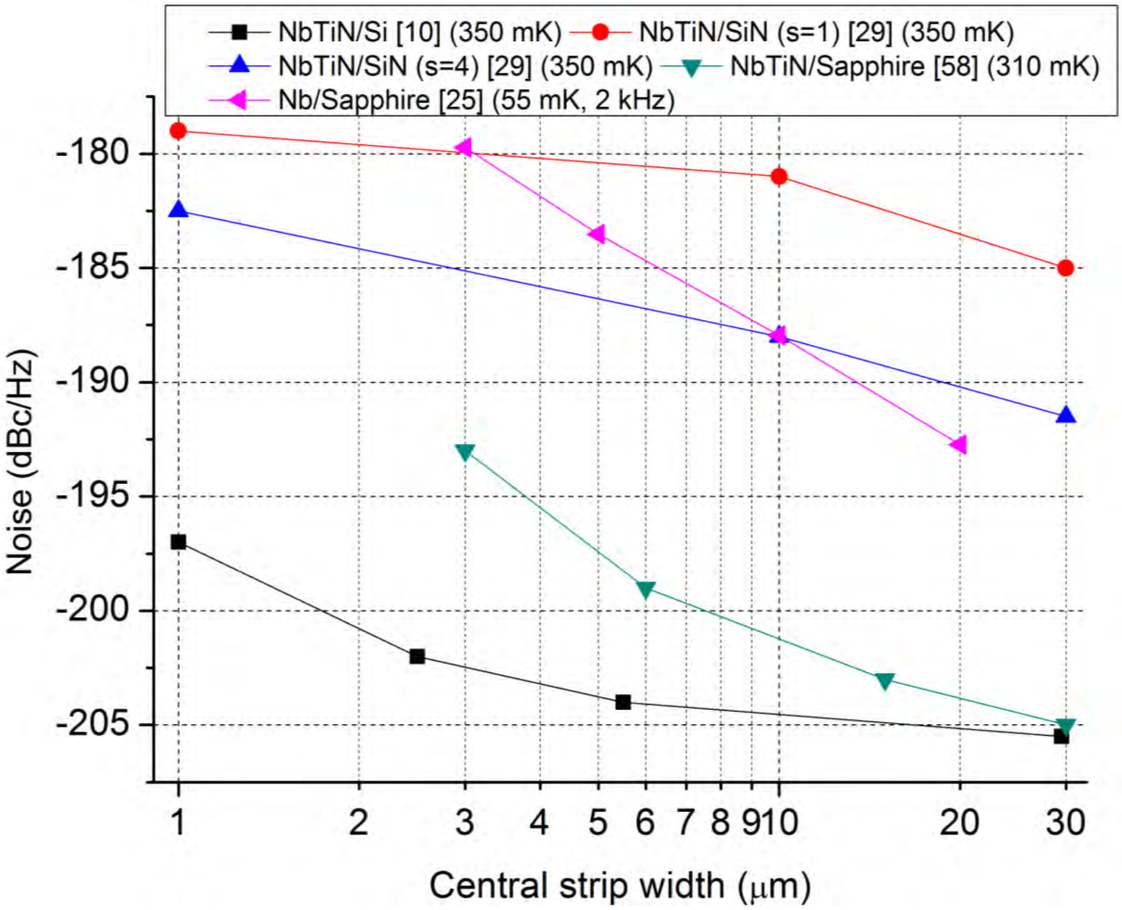


Figure 49 Noise in $\mathrm{dBc/Hz}$ versus central strip width w in $\mu\mathrm{m}$ for five different resonators, all CPWs except the NbTiN/SiN ones, which are microstrips. The NbTiN/Si CPW has a constant gap width of $2\ \mu\mathrm{m}$, the CPWs on sapphire have a gap width of $2w/3$. The Nb film has a thickness of $120\ \mathrm{nm}$, the NbTiN films have a thickness of $300\ \mathrm{nm}$. All resonators are measured at $1\ \mathrm{kHz}$ except Nb/Sapphire and $P_{int} = -30\ \mathrm{dBm}$ (Nb/Sapphire is corrected for that assuming a $\sqrt{P}$ dependence).

What can be said from Figure 48 and Figure 49 is the following:

- The saturation powers for the noise in CPWs and microstrips are below $-50\ \mathrm{dBm}$ and $-45\ \mathrm{dBm}$ respectively.

This is in accordance with the numerical results, see Table 24 and Table 26.

- All resonators display the same $1/\sqrt{P}$ dependence

This validates the use of the TLS expressions for loss and noise, given by (2.1), (2.4) and (2.5).

- For the constant gap NbTiN/Si CPW, the effect of increasing width (if the gap is not scaled accordingly), is limited. If the gap scales simultaneously with the central width, this limit is not very pronounced.

This is in accordance with Figure 33, but this is better illustrated in Figure 50.

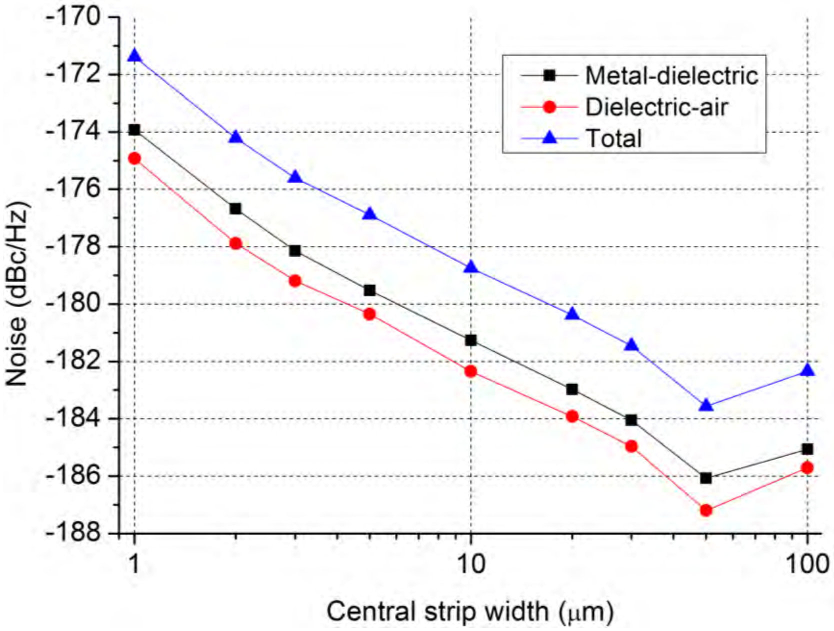


Figure 50 Noise (in $\mathrm{dBc/Hz}$) versus internal resonator power (in dBm) for CPWs with superconducting film thickness $0.3\ \mu\mathrm{m}$ and gap width $2\ \mu\mathrm{m}$, for two interfaces: metal-dielectric (black squares), dielectric-air (red circles) and the total (blue triangles) as calculated by COMSOL model 2 at $1\ \mathrm{kHz}$, $250\ \mathrm{mK}$ and $P_{int} = -25\ \mathrm{dBm}$.

- As stated in [27], overetching greatly reduces the noise in Si.

The influence of overetching was already indicated by model 1 and quantified in Table 26 on model 2. Importantly, the numerical results so far have assumed an overetch of $\leq 2.5\ \mathrm{nm}$, which is very small. All numerical results will therefore likely be an overestimate of the noise, compared to reality.

- Either microstrips are inherently noisier than CPWs or SiN is not a good dielectric

Comparing Figure 33 and Figure 35, which are CPWs and microstrips on the same dielectric, namely Si, at $P_{int} = -30\ \mathrm{dBm}$ would suggest similar performance and would hence indicate that the experimental difference is in the SiN. The underestimation of the noise of SiN even though Si is in the model in Figure 45 is likely to be due to the unknown overetch, which as stated in the previous point, is very influential.

- Silicon as a dielectric is better than sapphire, while NbTiN as a superconductor is better than Nb or Al

Considering that comparing model 1b and model 2 gives similar results in terms of the noise for CPWs, the choice of superconductor will probably not be the determining factor in the numerical model. A good hypothesis for the indirect effect of that choice would be that different superconductors and dielectrics yield a different lattice mismatch (see section 2.3 Other loss mechanisms), so that the interface layers are not comparable. This would imply a different value of κ for the use of different superconductors and/or different dielectrics. The use of other materials also has an influence on the fabrication, which may cause different extends of overetching in different combinations of superconductors with dielectrics.

- The overetches in the resonators from literature are typically not known, except in the NbTiN/Si CPW with grooves, which has an overetch of $0.9\ \mu\mathrm{m}$. Then there is a $7\ \mathrm{dBc/Hz}$ reduction of the noise compared to the regular NbTiN/Si CPW.

This is compatible with the results regarding the influence of overetch on the noise on CPWs from Table 26, from which follows that the overetch in the CPW without grooves an overetch of $40\ \mathrm{nm}$ should be present. In that case, the $6\ \mathrm{dBc/Hz}$ to Al/Si can also be explained by the overetch, as the fit on numerical results would this time suggest an overetch of a few nm, which is almost nothing. Wet-etching a Al/Si resonator as in [10] is known to give almost no overetch, so this is very compatible with what is seen in the numerical results.

However, the Nb/Sapphire data is still above the Al/Si data, so it must be concluded that the difference between sapphire and Si is not overetching, but rather a different κ. From the numerical calculations in chapter three, the κ in sapphire was estimated to be $7 \cdot 10^{-27}\ [\mathrm{Vm}^2/\mathrm{Hz}]$. Then for Si, κ should be less than that (depending on the overetch in sapphire).

It is difficult to determine κ for SiN and sapphire, as there both the overetch and the κ are unknown. However, the following can be said: sapphire and SiN are worse than Si, so this gives a lower limit for κ. However, an overetch can realistically only compensate about $9\ \mathrm{dBc/Hz}$, so this will give an upper bound on the κ as well. Furthermore, one could think of two strategies to get a better estimate on the overetch for SiN in particular. One would be to incorporate a large overetch resonator on a SiN chip which can be compared to the normal resonators, or the chip could be inspected to find an overetch estimate.

5.2 Experiment

As described in the previous chapter in the section on chip design, a total of five chips are measured, each containing a set of eight different resonator geometries.

5.2.1 Al-Si CPW ($> 10\ \mathrm{k\Omega cm}$, good cleaning)

Table 7 shows that the resonators have been designed properly in the sense that the resonance frequencies are close to expected. The small difference is mostly caused by fabrication, where too much of the Al has been etched away, so that the central strip is $0.5\ \mu\mathrm{m}$ narrower on each side and similarly for the the ground planes. This means that $t \equiv w + 2g$ is $1\ \mu\mathrm{m}$ too large.

Table 7 Design parameters for the 8 Al-SI CPWs, including the radiation loss upper limit set by [45].

CPW	1	2	3	4	5	6	7	8
Design t [μm]	7.00	9.33	14.00	18.67	25.67	37.33	51.33	70.00
Actual t [μm]	8.00	10.33	15.00	19.67	26.67	38.33	52.33	71.00
Design f_{res} [GHz]	6.100	6.200	6.300	6.400	6.500	6.600	6.700	6.800
Actual f_{res} [GHz]	5.855	6.009	6.183	6.324	6.465	6.609	6.749	6.898
Q_{rad} limit ($\cdot\ 10^6$)	3.42	1.95	0.87	0.49	0.25	0.12	0.06	0.03

The power law dependencies of the loss and the noise on total width t, internal power and temperature are given in Table 8. As there are only measurements from three different temperature, the latter dependency is only indicative. Together with the plots at $100\ \mathrm{mK}$ given in Figure 53 and Figure 55, the following may be concluded:

- **Loss:** The quality factors are on the order of 10^6, as expected very competitive with values from e.g. [11].

- The Q initially increases with increasing width, but for $t \geq 30\ \mu\text{m}$ flips sign. Considering Table 7, this will be caused by radiation losses, which become more prominent in wider resonators.

- The internal power dependence of Q is not completely flat, but what is certain is that no saturation effects are visible (as the saturation slope is much steeper than any slope in Figure 54), limiting the satuation power to $P_s \geq -30\ \text{dBm}$.

- **Noise:** The raw spectrum has to be corrected to obtain TLS noise, as at low powers the system noise, dominated by the low noise amplifier becomes a significant noise contribution, as it scales as $1/P$ while the TLS dominated phase noise only scales with $1/\sqrt{P}$. Because the spectrum itself is noisy, the system noise level is estimated by taking the mean value in amplitude noise (where no TLSs are visible) as proxy for the system noise between 1 and $10\ \text{kHz}$. An example of this correction is given in Figure 51 and Figure 52.

- The absolute value fot the noise is the best ever measured for Al on Si. The standard $t = 7$ configuration is 3 to $4\ \text{dBc/Hz}$ better than the Nb on Si CPW (and the similar performing Al on sapphire) from [58], $5\ \text{dBc/Hz}$ better than Al on Si from [10] and $12\ \text{dBc/Hz}$ better than Al on Si from [58]. This can only be attributed to the effect of proper cleaning of the Si surface before sputtering the Al, marking the importance of executing all of these steps.

- The total width dependence is in agreement with [25], which had a -1.58 dependence. As from numerical calculations followed that the metal-air and edge contributions are orders lower than the substrate-air and metal-substrate contributions, only the latter two have to be considered as relevant surface contributions, both having an approximately t^{-2} dependence. As the bulk noise contribution has a t^{-1} dependence, a fit can be made to determine the relative importance of both contribution types, as shown in Table 9 and Figure 54. This suggest a ratio of $\kappa_{surf}/\kappa_{bulk}$ of about 100, with not a large temperature dependence, suggesting that both TLS natures are similar.

- The TLS model is validated by the power dependence, which is in line with TLS theory, namely -0.47 ± 0.01 against -0.50 predicted.

- While indicative, the temperature dependence is completely different from the -1.73 value of [38]. This would suggest different TLS natures from the TLS in [38].

Table 8 Power law indices of the dependencies on loss and noise for the constant impedance Al-Si CPW of the power law fits of total width (in μm), internal power (in dBm) and temperature (in K) with standard error.

Al-Si CPW	Total width $[\mu\text{m}]$	Internal power $[\text{dBm}]$	Temperature $[\text{K}]$
Q	Non-monotonous	Approximately flat	-0.23 ± 0.15
Noise	-1.51 ± 0.04	-0.47 ± 0.01	1.62 ± 0.57

Table 9 Fitted values for the noise spectral density coefficient $\kappa(f_{res} = 6\ \mathrm{GHz}, \nu = 1\ \mathrm{kHz})$ for various temperatures, resulting from fitting numerically calculated surface and bulk noise contributions. Standard errors are in parentheses.

Temperature $[\mathrm{mK}]$	$\kappa_{surf}(1\ \mathrm{kHz}) \cdot 10^{29}\ [\mathrm{Vm^2/Hz}]$	$\kappa_{bulk}(1\ \mathrm{kHz}) \cdot 10^{29}\ [\mathrm{Vm^2/Hz}]$
60	9.78 (1.65)	0.12 (0.02)
100	15.03 (2.99)	0.13 (0.03)
200	14.66 (2.15)	0.12 (0.02)

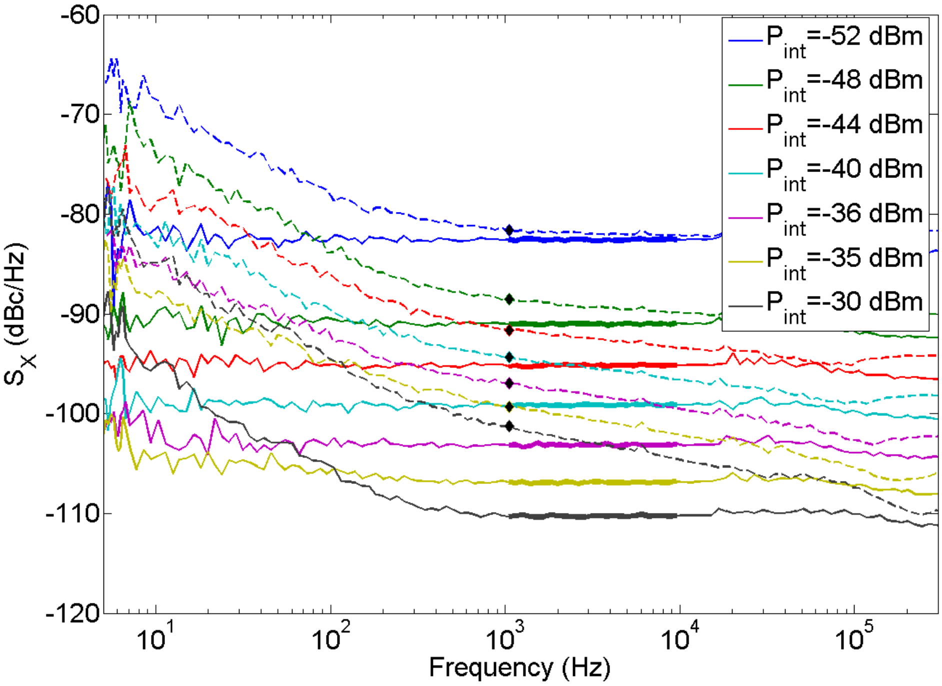


Figure 51 Example of the noise spectrum of the $t = 52.33\ \mu\mathrm{m}$ Al-Si CPW, with the solid lines representing amplitude noise and the dashed represent phase noise (in $\mathrm{dBc/Hz}$). The diamonds are points at $1\ \mathrm{kHz}$. The part of the solid lines that is thicker (between 1 and $10\ \mathrm{kHz}$) are the values of which the mean is taken to get an estimate on the setup noise.

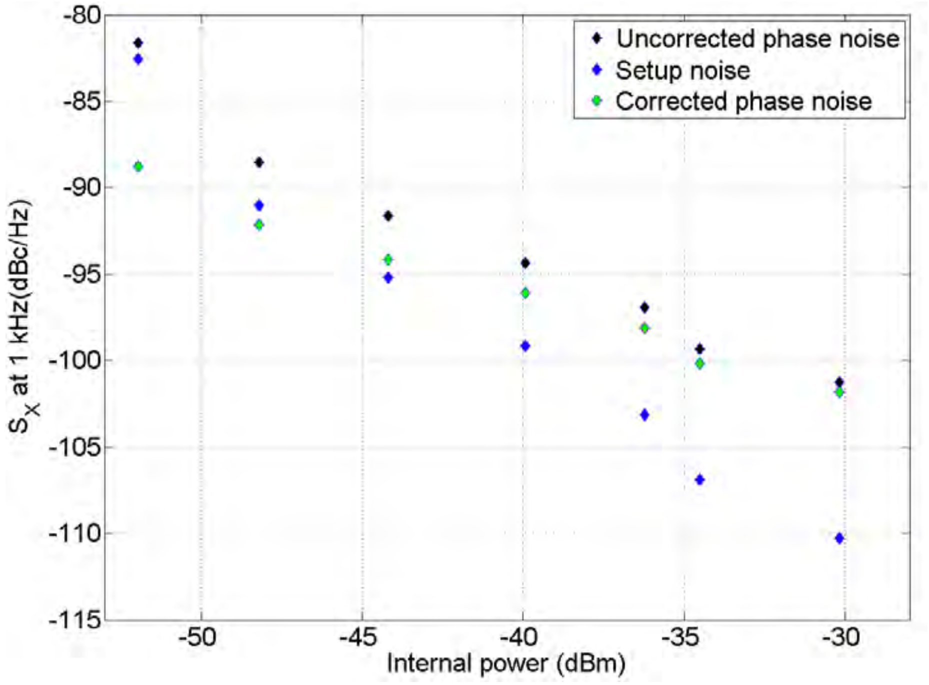


Figure 52 Uncorrected phase noise, setup noise and the phase noise (in $\mathrm{dBc/Hz}$) corrected for this setup contribution as a function of internal power, for the $t = 52.33\ \mu\mathrm{m}$ Al-Si CPW.

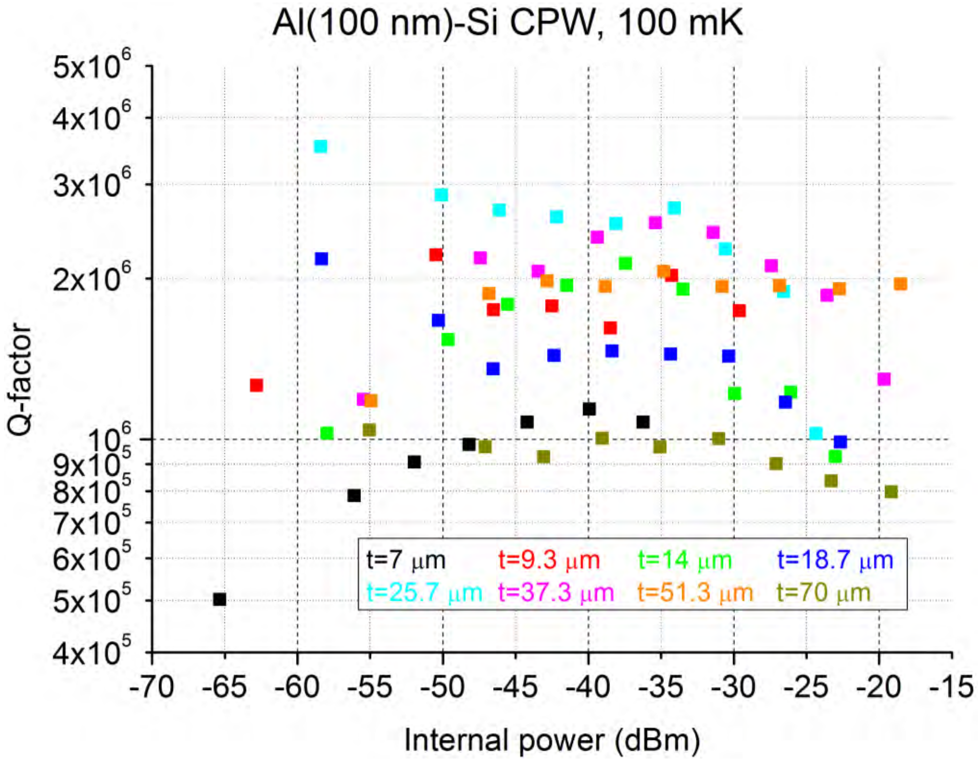


Figure 53 Internal quality factor versus internal power in dBm for the constant impedance Al-Si CPW resonator set with total width (in $\mu\mathrm{m}$) of 7 (black), 9.3 (red), 14 (green), 18.7 (dark blue), 25.7 (cyan), 37.3 (magenta), 51.3 (orange) and 70 (olive) at $100\ \mathrm{mK}$. The inset shows the dependency on the total width and temperature respectively with standard error, fitted at $P_{int} = -40\ \mathrm{dBm}$.

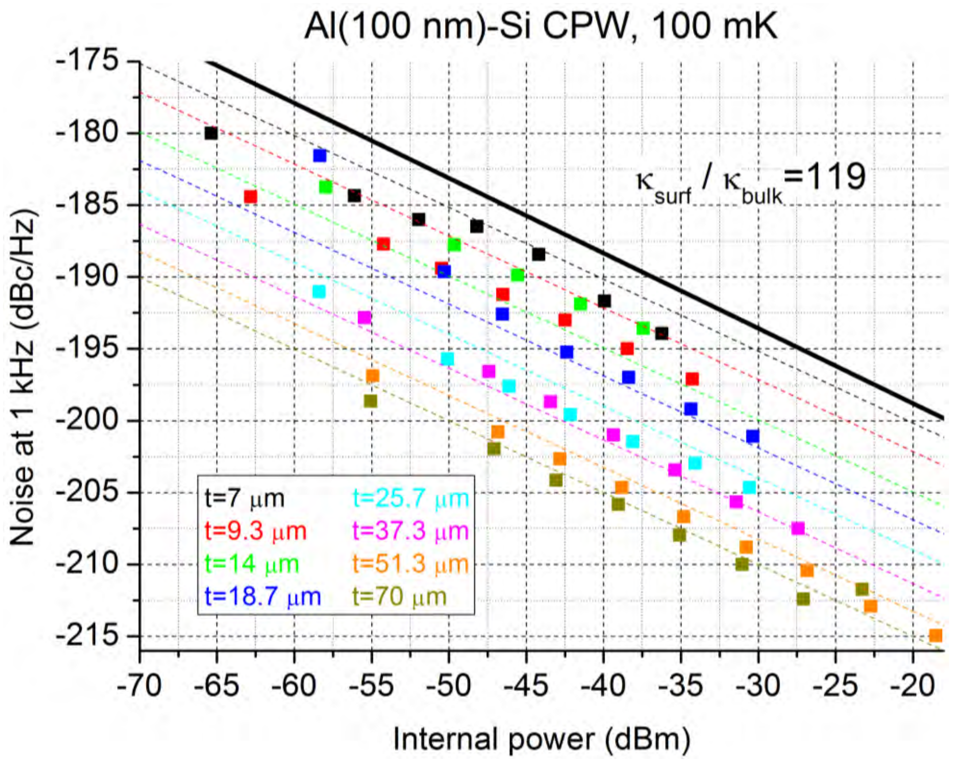


Figure 54 Noise measured at $1\ \mathrm{kHz}$ in $\mathrm{dBc/Hz}$ versus internal power in dBm for the constant impedance Al-Si CPW resonator set with total width (in $\mu\mathrm{m}$) of 7 (black), 9.3 (red), 14 (green), 18.7 (dark blue), 25.7 (cyan), 37.3 (magenta), 51.3 (orange) and 70 (olive) at $100\ \mathrm{mK}$. The black line indicates the noise of the $t = 7\ \mu\mathrm{m}$ Nb on Si CPW from [58]. The dashed lines represent the fit with the numerical data for the surface and dielectric bulk contributions, while the inset shows the ratio between their respective noise spectral coefficients.

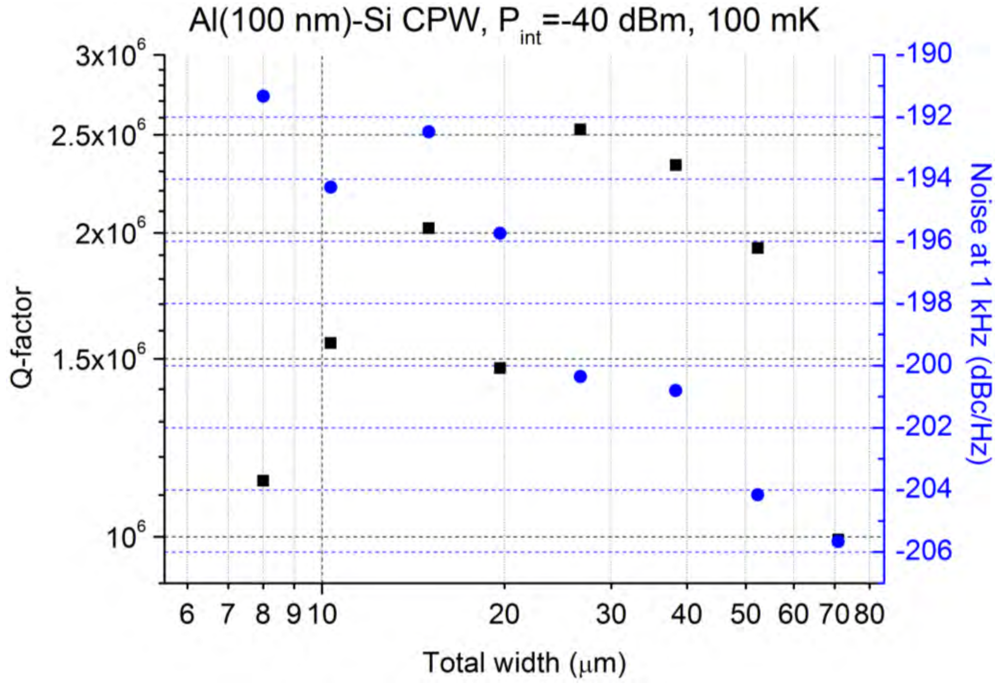


Figure 55 Dependency of Q-factor (black squares) and noise (blue circles) at $1\ \mathrm{kHz}$ in $\mathrm{dBc/Hz}$ versus on the total width in $\mathrm{\mu m}$ for the constant impedance Al-Si CPW resonator set at $P_{int} = -40\ \mathrm{dBm}$ and $100\ \mathrm{mK}$.

5.2.2 Al-Si CPW ($> 10\ \mathrm{k\Omega cm}$, basic cleaning)

Table 10 shows that the resonators have been designed properly. The loss and noise with respect to power and total width t are given in Figure 56 to Figure 58 for $T = 100\ \mathrm{mK}$. The power law dependencies of the loss and noise on t, power and temperature are given in Table 11. The graphs for $T = 60$ and $200\ \mathrm{mK}$ are found in the Appendix: Al-Si CPW (high resistivity, imperfect fabrication).

Table 10 Design parameters for the 8 Al-SI CPWs, including the radiation loss upper limit set by [45].

CPW	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
t [μm]	7.00	9.33	14.00	18.67	25.67	37.33	51.33	70.00
Design f_{res} [GHz]	6.100	6.200	6.300	6.400	6.500	6.600	6.700	6.800
Actual f_{res} [GHz]	5.048	5.368	5.705	5.936	6.150	6.366	6.555	6.738
Q_{rad} **limit** ($\cdot 10^6$)	6.01	2.99	1.18	0.61	0.30	0.13	0.07	0.03

- **Loss:** The absolute values of the Q-factors are unaffected by the imperfect cleaning and remain on the order of 10^6. The observed width dependency is negative, -0.97.

- At low powers there are some artificial increases in Q, which originate from the transmission dips being so deep ($\geq 30\ \mathrm{dB}$) that the signal is on the order of the IQ-mixer calibration error. At extremely low powers (with the modified setup), the dips get very shallow, and therefore the Q drops significantly. This was an issue with the additionally connected amplifier.

- For the smallest widths saturation in power may appear to be present in the loss, but it is much more likely that this is quasiparticle loss, considering this effect becomes stronger with increasing temperature and it is on the correct order of magnitude [59].

- **Noise:** In absolute terms, there is about $8\ \mathrm{dBc/Hz}$ more noise when compared to the data from [58]. This means that imperfect cleaning can lead to a noise increase of $12\ \mathrm{dBc/Hz}$.

Table 11 Power law indices for the dependencies on loss and noise for the constant impedance Al-Si CPW in the power law fits of total width (in $\mu\mathrm{m}$), internal power (in dBm) and temperature (in K) with standard error.

Al-Si CPW	Total width $[\mu\mathrm{m}]$	Internal power $[\mathrm{dBm}]$	Temperature $[\mathrm{K}]$
Q	-0.97 ± 0.21	Approximately flat	0.68 ± 0.25
Noise	-1.58 ± 0.03	-0.50 ± 0.01	0.25 ± 0.40

- The width dependence on the internal power is again in line with TLSs. Additionally, compared to the previous Al-Si CPWs, the width dependency is not significantly different and remains consistent with results from [58]. This means that the nature of the remaining TLSs is the same as the TLS that have been removed if properly cleaned.

- Even more interesting are the results for the κ's estimates, which are given for 60, 100, $200\ \mathrm{mK}$ in Table 12. Not only the surface contribution has increased compared to Table 9, which is what would be expected as the cleaning treatment only applies to the surfaces, but the bulk TLS contribution has increased accordingly, which is rather surprising.

Table 12 Fitted values for the noise spectral density coefficient $\kappa(f_{res} = 6\ \mathrm{GHz}, \nu = 1\ \mathrm{kHz})$ for various temperatures, resulting from fitting numerically calculated surface and bulk noise contributions. Standard errors are in parentheses.

Temperature $[\mathrm{mK}]$	$\kappa_{surf}(1\ \mathrm{kHz}) \cdot 10^{29}\ [\mathrm{Vm^2/Hz}]$	$\kappa_{bulk}(1\ \mathrm{kHz}) \cdot 10^{29}\ [\mathrm{Vm^2/Hz}]$
60	138 (19)	0.9 (0.2)
100	178 (16)	1.2 (0.1)
200	116 (11)	1.2 (0.1)

- In contrast to the loss, the ultra-low power measurements seem to still useful for the noise. Some resonators seem to indicate saturation at $-80\ \mathrm{dBm}$, but it is definitely not decisive.

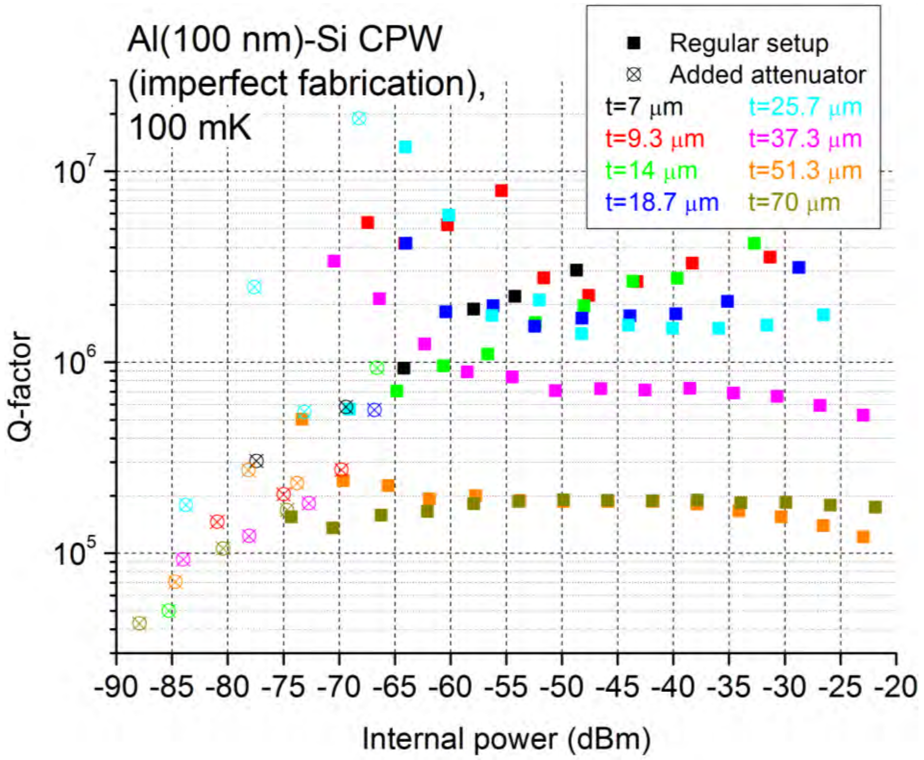


Figure 56 Internal quality factor versus internal power in dBm for the constant impedance Al-Si CPW resonator set with total width (in $\mu\mathrm{m}$) of 7 (black), 9.3 (red), 14 (green), 18.7 (dark blue), 25.7 (cyan), 37.3 (magenta), 51.3 (orange) and 70 (olive) at $100\ \mathrm{mK}$ (solid squares are with regular setup, open circles with cross are with added attenuator). The inset shows the dependency on the total width and temperature respectively with standard error, fitted at $P_{int} = -40\ \mathrm{dBm}$.

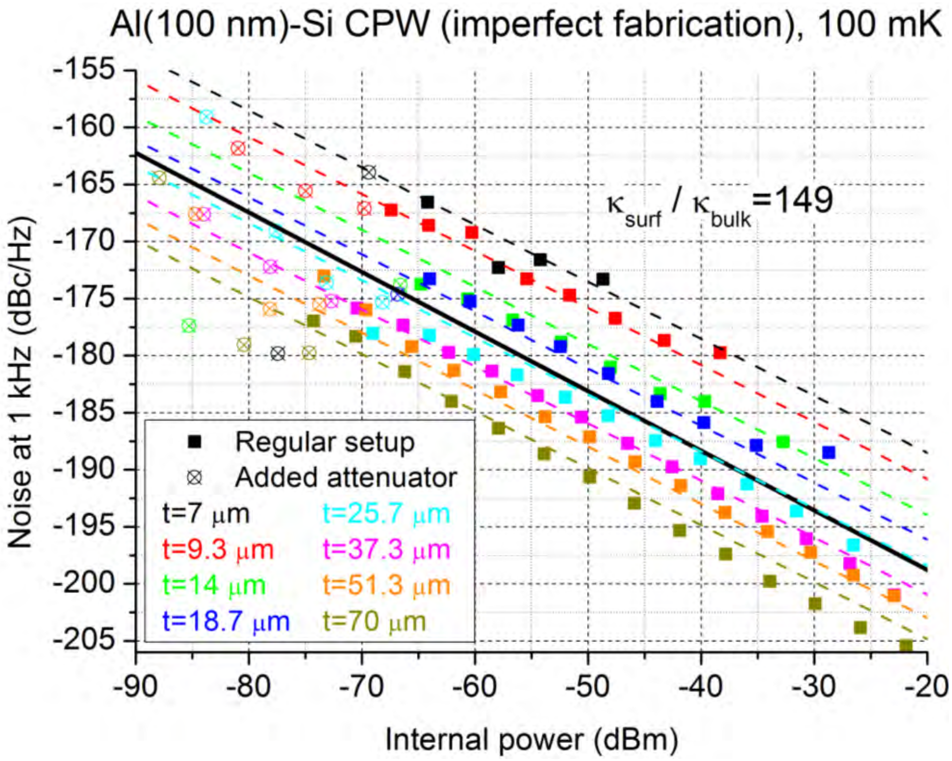


Figure 57 Noise measured at $1\ \mathrm{kHz}$ in $\mathrm{dBc/Hz}$ versus internal power in dBm for the constant impedance Al-Si CPW resonator set with total width (in $\mu\mathrm{m}$) of 7 (black), 9.3 (red), 14 (green), 18.7 (dark blue), 25.7 (cyan), 37.3 (magenta), 51.3 (orange) and 70 (olive) at $100\ \mathrm{mK}$ (solid squares are with regular setup, open circles with cross are with aded attenuator). The black line indicates the noise of the $t = 7\ \mu\mathrm{m}$ Nb on Si CPW from [58]. The dashed lines represent the fit with the numerical data for the surface and dielectric bulk contributions, while the inset shows the ratio between their respective noise spectral coefficients.

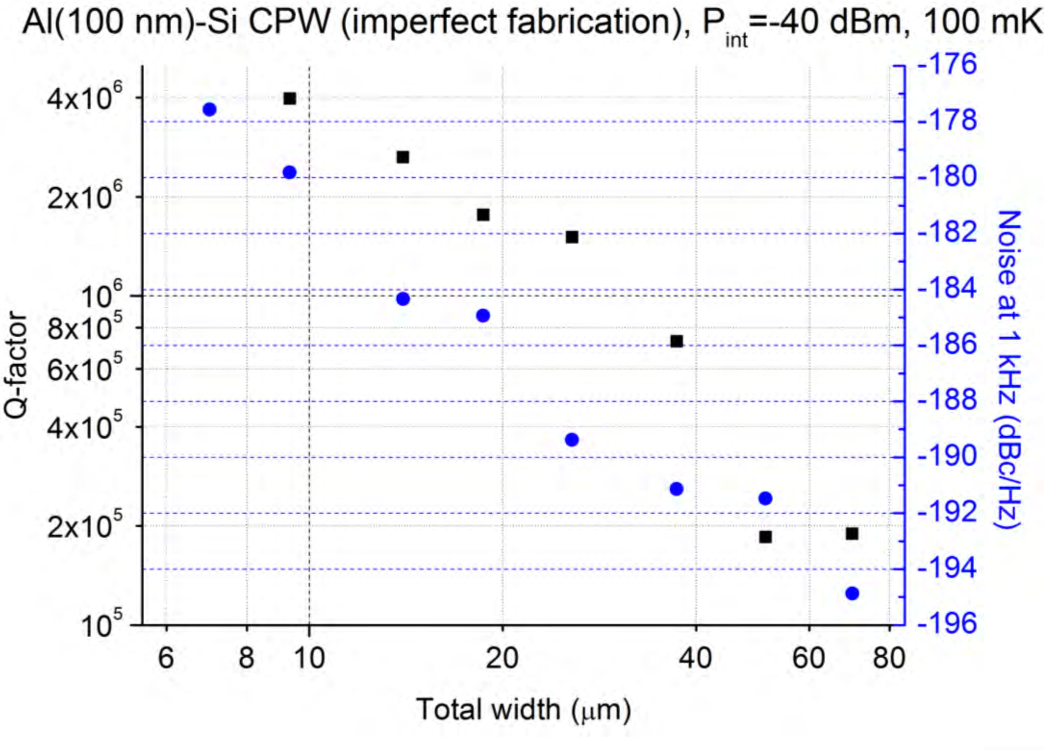


Figure 58 Dependency of Q-factor (black squares) and noise (blue circles) at $1\ \mathrm{kHz}$ in $\mathrm{dBc/Hz}$ versus on the total width in $\mu\mathrm{m}$ for the constant impedance Al-Si CPW resonator set at $P_{int} = -40\ \mathrm{dBm}$ and $100\ \mathrm{mK}$.

5.2.3 Al-Si CPW (< 10 kΩcm, basic cleaning)

Incidentally, the same configurations have been measured, only using low resistivity Si instead of the standard high resistivity Si. While the loss is not very affected by this change, the presence of the additional impurities deteriorates the noise by roughly a factor 1000. Also, while the power dependency on the noise still appears to be of the TLS form $P^{-0.5}$ when seen on a large range, the curve is very irregular. Possibly, the additional impurities cause more irregularities of the lattice. This creates more local potential minima or energy states with their own saturation level, modifying the field scaling from $1/\sqrt{1+E^2/E_s^2}$ to e.g. a more complicated $1/\sqrt{1+\sum_{i=1}^{n}(E-E_i)^2/E_{s,i}^2}$. Because of its practical unsuitability, this data is not analyzed further, but for completion the graphs can be found in Appendix: Al-Si CPW (low resistivity).

5.2.4 Al-SiN-Si CPW

Two batches have been prepared, one with thorough cleaning and one with basic cleaning. As shown in Figure 61, there is no improvement using the thorough cleaning, so only the basic cleaning batch is presented. The loss and noise with respect to power and total width are given in Figure 59 to Figure 61 for $T = 100$ mK. The graphs for 60 and 200 mK can be found in the Appendix: Al-SiN-Si CPW.

Table 13 shows that the resonators have been designed properly. The resonance dips were easily identified as the expected resonance frequencies were close to the actual values, with the small difference caused by uncertainty in the dimensions of the resonator introduced at the fabrication and by the approximations used in [47].

Table 13 Design parameters for the 8 Al-SiN-SI CPWs, including the radiation loss upper limit set by [45].

CPW	1	2	3	4	5	6	7	8
t [μm]	7.00	9.33	14.00	18.67	25.67	37.33	51.33	70.00
Design f_{res} [GHz]	6.100	6.200	6.300	6.400	6.500	6.600	6.700	6.800
Actual f_{res} [GHz]	5.948	6.129	6.309	6.444	6.571	6.699	6.825	6.959
Q_{rad} limit	4.96	2.63	1.10	0.59	0.30	0.14	0.07	0.04

The power law dependencies of the loss and the noise on total width t, internal power and temperature are given in Table 14. From the results at 100 mK the following can be stated:

Table 14 Power law indices for the dependencies on loss and noise for the constant impedance Al-SiN-Si CPW in the power law fits of total width (in μm), internal power (in dBm) and temperature (in K) with standard error.

Al-SiN-Si CPW	Total width [μm]	Internal power [dBm]	Temperature [K]
Q	0.43 ± 0.02	Approximately flat	0.07 ± 0.02
Noise	-1.50 ± 0.03	-0.50 ± 0.02	1.54 ± 0.47

- **Loss:** Compared to the Al-Si CPWs, the Q's are about an order of magntiude lower. The two widest resonators have much lower Q's, which also appear to be completely power insensitive. As the noise of the widest resonators appears to be normal, this problem must have an origin exclusively in loss. As seen in Table 13, radiative losses are a likely candidate to be limiting the resonators. Excluding these from the fit yields 0.43 ± 0.02 for the width dependence. From numerical results, the dominant contributions are from the metal-substrate and substrate-air surfaces on one hand and the dielectric bulk on the other. Table 15 shows loss tangent estimates obtained through fitting the experimental data on the numerically calculated participation ratios (far in the unsaturated regime, as the experimental data is power independent). A clear temperature dependence is not seen.

- **Noise:** While cleaning improved the noise dramatically for Al-Si, this is not the case this time, leaving the noise roughly $8\ \mathrm{dBc/Hz}$ higher than in [58]. This also suggests that this is a bulk SiN effect. Still the internal power dependence of the noise is close to the predicted value of -0.5 from the TLS model and the total width dependence is similar to the Al-Si CPWs.

- Fitting the noise coefficients κ of the surface and bulk noise contributions yields the results as shown in Figure 60 and Table 15, although these results must be interpreted with caution considering that the SiN layer is very thin. This makes it difficult to see the difference between a bulk SiN and a surface SiN effect. The ratio between κ_{surf} and κ_{bulk} remains comparable to the Al-Si CPW κ's, namely around 100. A clear temperature dependence is not seen.

Table 15 Fitted values for loss tangent $tan\ (\delta)$ and the noise spectral density coefficient $\kappa(f_{res} = 6\ \mathrm{GHz}, \nu = 1\ \mathrm{kHz})$ for various temperatures, resulting from fitting numerically calculated surface and bulk loss and noise contributions. Standard errors are in parentheses.

Temperature $[\mathrm{mK}]$	$tan\ (\delta)_{surf} \cdot 10^6$	$tan\ (\delta)_{bulk} \cdot 10^6$	$\kappa_{surf} \cdot 10^{29}\ [\mathrm{Vm^2/Hz}]$	$\kappa_{bulk} \cdot 10^{29}\ [\mathrm{Vm^2/Hz}]$
60	842 (57)	3.2 (0.2)	173 (17)	1.7 (0.2)
100	867 (87)	3.2 (0.3)	215 (25)	2.0 (0.3)
200	1020 (91)	3.2 (0.3)	203 (22)	2.1 (0.3)

- TLS saturation in noise is always visible up to $-60\ \mathrm{dBm}$, while in the loss the saturation is not seen, restricting the saturation power to $\geq -35\ \mathrm{dBm}$.

- The temperature dependency estimates can be improved upon, as the large range between 60 and $200\ \mathrm{mK}$ is only covered by three points. However, it would seem that there is a significant positive correlation between noise and temperature, contrary to results from [38].

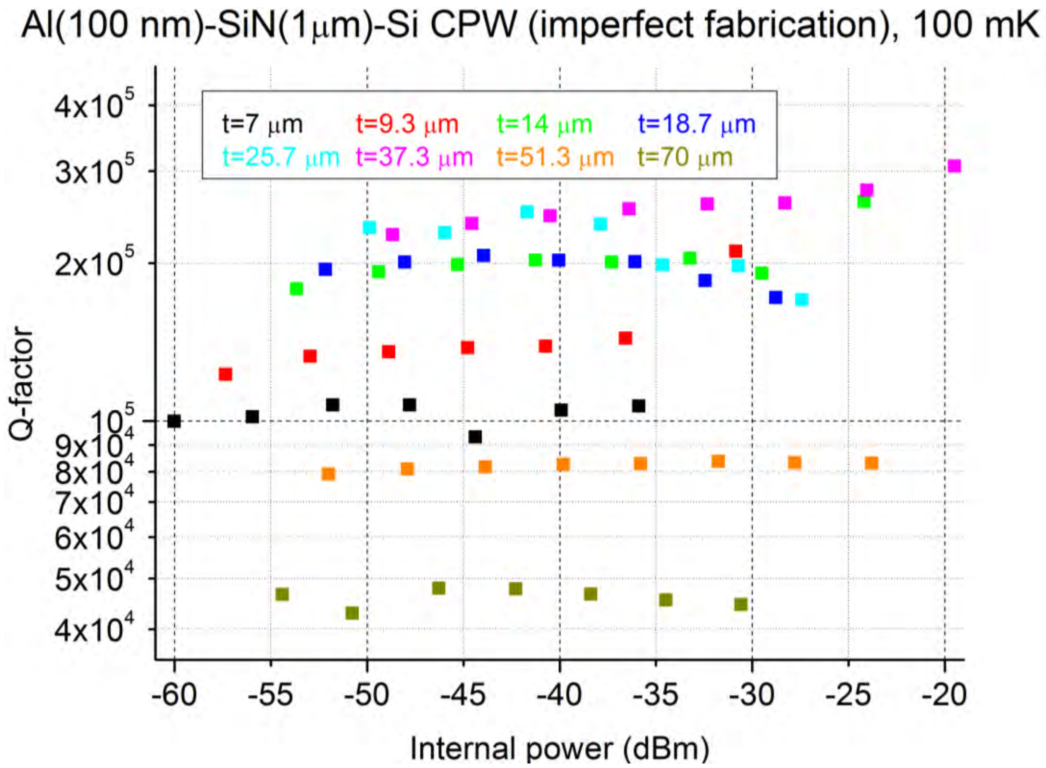


Figure 59 Internal quality factor versus internal power in dBm for the constant impedance Al-SiN-Si CPW resonator set with total width (in $\mu\mathrm{m}$) of 7 (black), 9.3 (red), 14 (green), 18.7 (dark blue), 25.7 (cyan), 37.3 (magenta), 51.3 (orange) and 70 (olive) at $100\ \mathrm{mK}$ The inset shows the dependency on the total width and temperature respectively with standard error.

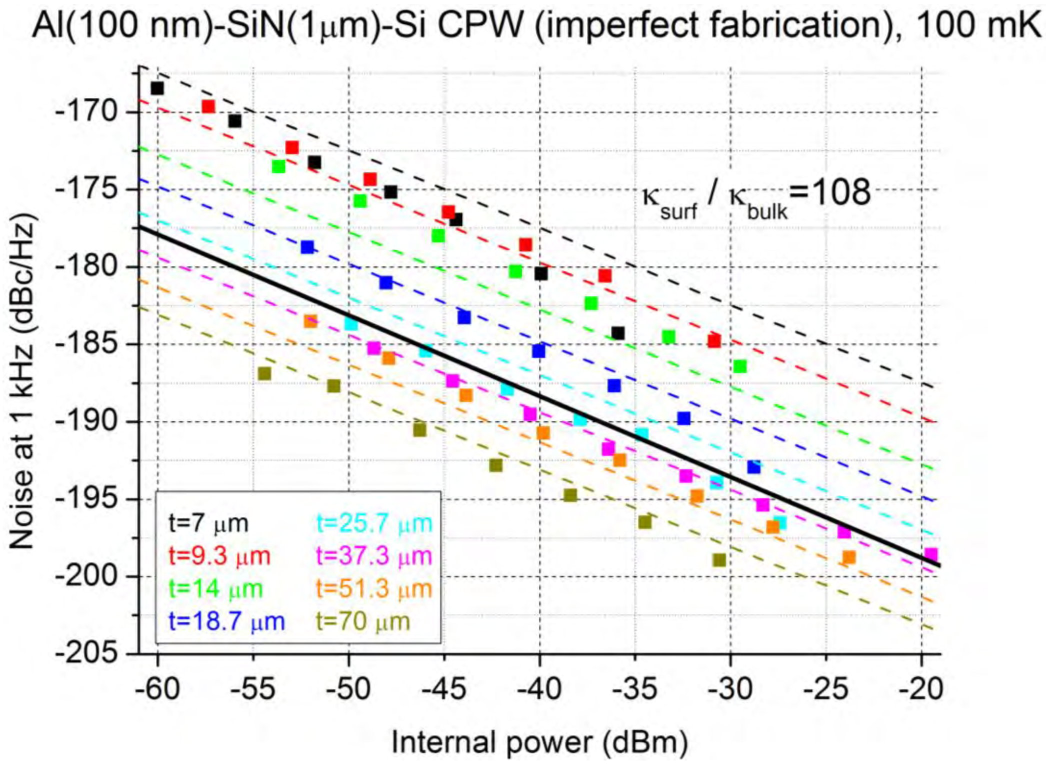


Figure 60 Noise measured at $1\ \mathrm{kHz}$ in $\mathrm{dBc/Hz}$ versus internal power in dBm for the constant impedance Al-SiN-Si CPW resonator set with total width (in $\mu\mathrm{m}$) of 7 (black), 9.3 (red), 14 (green), 18.7 (dark blue), 25.7 (cyan), 37.3 (magenta), 51.3 (orange) and 70 (olive) at $100\ \mathrm{mK}$. The black line indicates the noise of the $t = 7\ \mu\mathrm{m}$ Nb on Si CPW from [58]. The dashed lines represent the fit with the numerical data for the surface and dielectric bulk contributions, while the inset shows the ratio between their respective noise spectral coefficients.

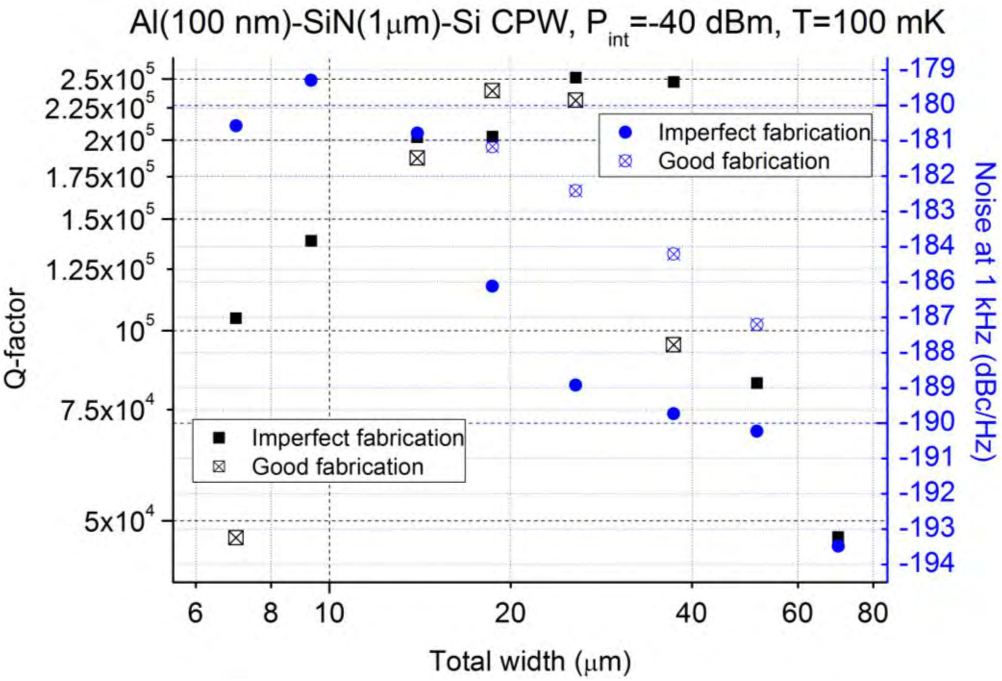


Figure 61 Dependency of Q-factor (black squares) and noise (blue circles) at $1\ \mathrm{kHz}$ in $\mathrm{dBc/Hz}$ versus on the total width in $\mu\mathrm{m}$ for the constant impedance Al-SiN-Si CPW resonator set at $P_{int} = -40\ \mathrm{dBm}$ and $100\ \mathrm{mK}$. The filled symbols show the data without thorough cleaning, the symbols with a cross the data with thorough cleaning.

5.2.5 Al-SiN CPW

This chip has only been fabricated without the thorough cleaning. Due to a design flaw, only three resonators are within the limit where the amplifier works reliably, namely the narrowest two resonators and the reference CPW on SiN and Si, see Table 16. It is also not trivial to determine which of the resonator dips corresponds to the reference CPW, but the one closest to the equivalent structure in the Al-SiN-Si chip is assumed to be the reference CPW. The design error eliminates the possibility to determine width dependencies, limiting the analysis of Figure 62 and Figure 63 on loss and noise respectively at $T = 100\ \mathrm{mK}$. . The graphs for $T = 60$ and $200\ \mathrm{mK}$ can be found in the Appendix: Al-SiN CPW.

Table 16 Design parameters for the 8 Al-SIN CPWs, including the radiation loss lower limit set by [45].

CPW	1	2	3	4	5	6	7	8	Reference CPW
t [μm]	7.00	9.33	14.00	18.67	25.67	37.33	51.33	70.00	7.00
Design f_{res} [GHz]	6.100	6.200	6.300	6.400	6.500	6.600	6.700	6.800	5.000
Actual f_{res} [GHz]	8.180	8.981	–	–	–	–	–	–	5.000
Q_{rad} limit ($\cdot 10^6$)	1.29	1.90	–	–	–	–	–	–	7.02

- The absolute value of the loss (see Figure 62) is slightly better for Al-SiN than for Al-SiN-Si, but still close to an order of magnitude worse than for Al-Si.

- The absolute value of the noise (see Figure 63) is slightly better than for the Al-SiN-Si. The noise flattens out at large powers for the reference CPW, which is likely due to g-r noise. Otherwise, the power dependency is consistent with TLS.

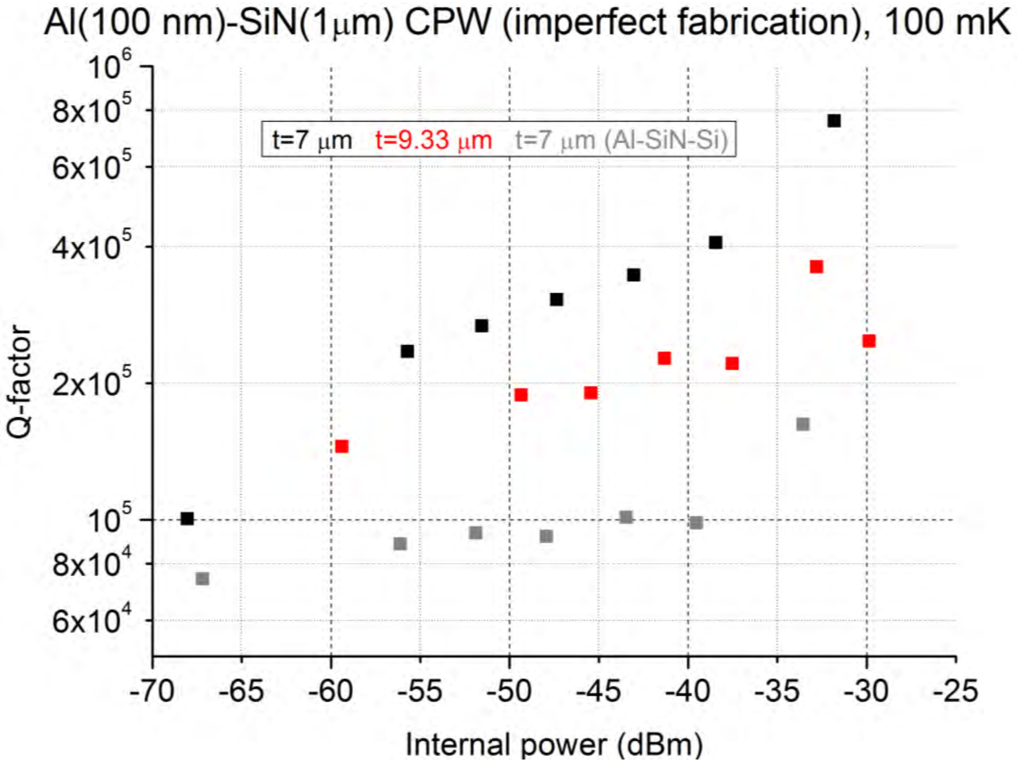


Figure 62 Internal quality factor versus internal power in dBm for the constant impedance Al-SiN CPW resonator set with Al-SiN-Si reference CPW with total width (in $\mu\mathrm{m}$) of 7 (black, CPW in grey) and 9.33 (red) at $100\ \mathrm{mK}$.

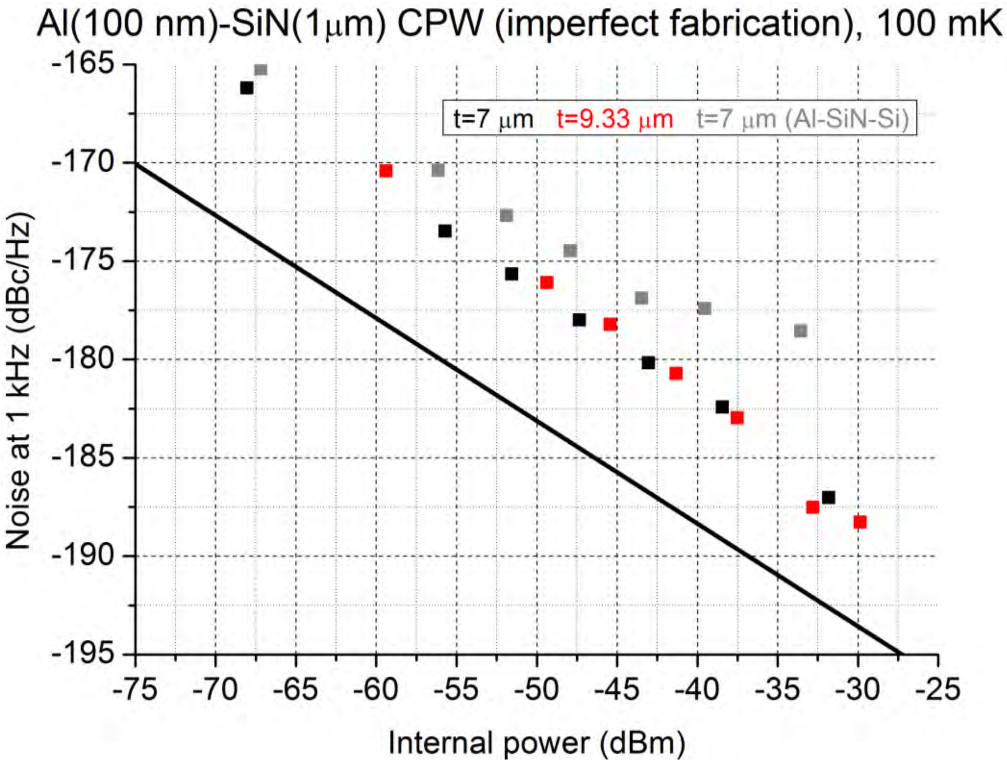


Figure 63 Noise measured at $1\ \mathrm{kHz}$ in $\mathrm{dBc/Hz}$ versus internal power in dBm for the constant impedance Al-SiN CPW resonator set with Al-SiN-Si reference CPW with total width (in $\mu\mathrm{m}$) of 7 (black, CPW in grey) and 9.33 (red) at $100\ \mathrm{mK}$. The black line indicates the noise of the $t = 7\ \mu\mathrm{m}$ Nb on Si CPW from [58].

Al-SiN microstrip

The Al on SiN membrane microstrips with and without thorough cleaning have both been measured. As the microstrips that have undergone the good fabrication method have better Q and slightly better noise ($1-3\ \mathrm{dBc/Hz}$), that data is presented first. However, the cleaning also slightly affected thethe width dependencies, which is why the one with inferior performance in loss and noise is also presented.

Table 17 Design parameters for the 8 Al-SiN microstrips, including the reference Al-SiN-Si CPW. Radiation loss is not a problem in these microstrips and is hence not reported.

Microstrip	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**Reference CPW**
$\boldsymbol{w}$ $[\mathbf{\mu m}]$	3	4	6	8	11	16	22	30	3
Design $\boldsymbol{f_{res}}$ $[\mathbf{GHz}]$	6.100	6.200	6.300	6.400	6.500	6.600	6.700	6.800	7.000
Actual $\boldsymbol{f_{res}}$ $[\mathbf{GHz}]$	5.796	6.000	6.048	6.213	6.221	6.302	6.384	6.485	–

Figure 17 shows that the resonators have been designed reasonably well, but the reference CPW is not found. The loss and noise with respect to power and total width are given in Figure 64 to Figure 66 for $T = 100\ \mathrm{mK}$.

Table 18 Power law indices for the dependencies on loss and noise for the Al-SiN microstrips in the power law fits of total width (in $\mathbf{\mu m}$), internal power (in $\mathbf{dBm}$) and temperature (in $\mathbf{K}$) with standard error.

Al-SiN Microstrip	**Total width** $[\mathbf{\mu m}]$	**Internal power** $[\mathbf{dBm}]$	**Temperature** $[\mathbf{K}]$
$\boldsymbol{Q}$	Approximately flat	Approximately flat	–
Noise	-0.69 ± 0.03	-0.51 ± 0.01	–

- **Loss:** The absolute value for the loss ($2-3 \cdot 10^5$) is below that of the Al-Si CPW ($2 \cdot 10^6$), but very comparable to the loss in the Al-SiN CPW and hence slightly better than the Al-SiN-Si CPW. This means microstrips do not have more loss than CPWs in comparable circumstances.

- All resonators have about the same loss, except for the two narrowest resonators. The $w = 3\ \mathrm{\mu m}$ has a very shallow transmission dip, while the $w = 4\ \mathrm{\mu m}$ resonator has a very assymetric transmission dip, which makes it difficult to fit with a Lorentzian, making the loss values for the other widths are more reliable.

- The loss dependence is flat, both in power and in width, meaning that the metal-substrate interface or the dielectric bulk dominates for $w \geq 6\ \mathrm{\mu m}$, with a saturation power $P_s \geq -20\ \mathrm{dBm}$. The positive width dependence seen in the imperfectly cleaned sample (Figure 67) indicative of substrate-air interface TLSs cannot be seen in this sample, due to the aforementioned problems with the resonance dips of the two smallest dips.

- **Noise:** The absolute value of the noise of the $w = 3\ \mu\text{m}$ is $4\ \text{dBc/Hz}$ worse than the Al-SiN-SI $t = 7\ \mu\text{m}$ CPW, about $6\ \text{dBc/Hz}$ worse than the Al-SiN $t = 7\ \mu\text{m}$ CPW and $12\ \text{dBc/Hz}$ worse than the standard $t = 7\ \mu\text{m}$ line from [58]. Considering that twice as thick dielectric would be better comparable to a CPW with a gap width of $2\ \mu\text{m}$ accounts for $2\ \text{dBc/Hz}$ difference. Still, the microstrip is slightly worse in terms of noise than a comparable CPW, which is also reflected in its width dependence, which is less steep. However, assuming the same jump in performance as seen in CPWs with Si, using Al-Si microstrip would still remain a viable option.

- The width dependence is -0.69 ± 0.03, which in contrast to the imperfectly cleaned sample, is in line with numerical calculations. This shows that the Al-SiN microstrip noise is bulk dominated. Fitting the noise coefficients κ of the surface and bulk noise contributions yields the results as shown in Figure 65 and Table 19.

Table 19 Fitted values for loss tangent $tan\ (\delta)$, resulting from fitting numerically calculated surface and bulk loss contributions. Standard errors are in parentheses.

Temperature $[\text{mK}]$	$\kappa_{surf} \cdot 10^{29}\ [\text{Vm}^2/\text{Hz}]$	$\kappa_{bulk} \cdot 10^{29}\ [\text{Vm}^2/\text{Hz}]$
100	89 (23)	21 (1)

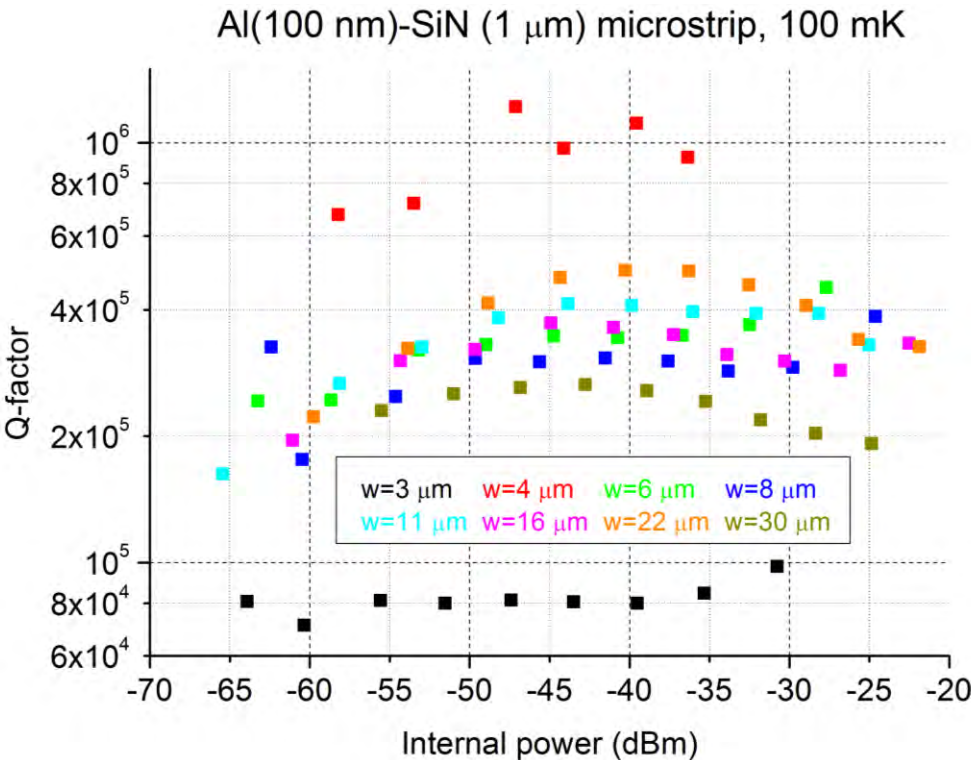


Figure 64 Internal quality factor versus internal power in dBm for the Al-SiN microstrip resonator set with central width (in μm) of 3 (black), 4 (red), 6 (green), 8 (dark blue), 11 (cyan), 16 (magenta), 22 (orange) and 30 (olive) at $100\ \text{mK}$.

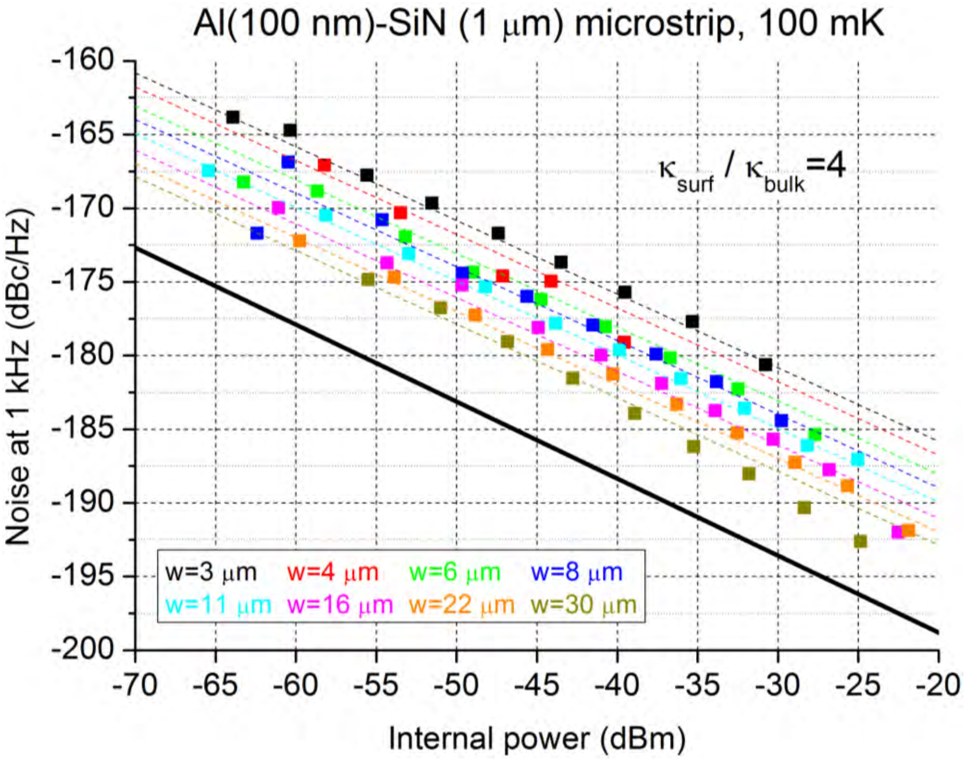


Figure 65 Noise measured at $1\ \mathrm{kHz}$ in $\mathrm{dBc/Hz}$ versus internal power in dBm for the Al-SiN microstrip resonator set with central width (in $\mu\mathrm{m}$) of 3 (black), 4 (red), 6 (green), 8 (dark blue), 11 (cyan), 16 (magenta), 22 (orange) and 30 (olive) at $100\ \mathrm{mK}$. The black line indicates the noise of the $t = 7\ \mu\mathrm{m}$ Nb on Si CPW from [58]. The dashed lines represent the fit with the numerical data for the surface and dielectric bulk contributions, while the inset shows the ratio between their respective noise spectral coefficients.

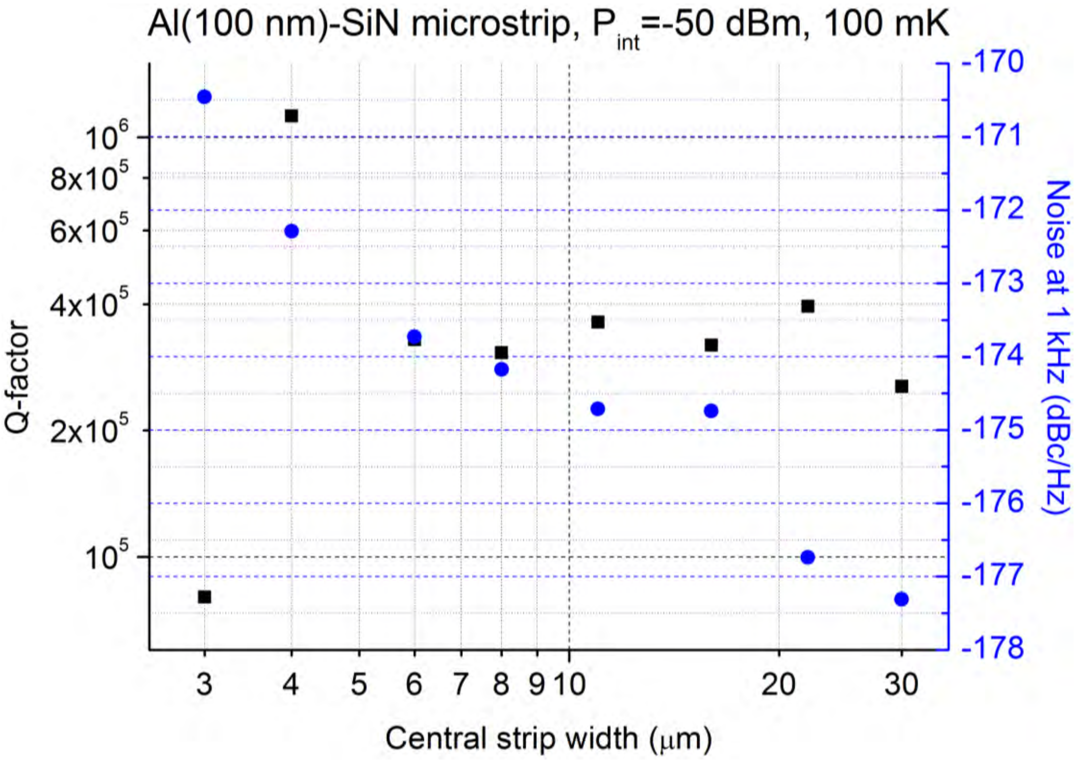


Figure 66 Dependency of Q-factor (black squares) and noise (blue circles) at $1\ \mathrm{kHz}$ in $\mathrm{dBc/Hz}$ versus on the total width in $\mu\mathrm{m}$ for the constant impedance Al-SiN microstrip resonator set at $P_{int} = -50\ \mathrm{dBm}$ for $T = 100\ \mathrm{mK}$.

5.2.6 Al-SiN microstrip (imperfect fabrication)

Table 20 shows that the resonators have again been designed properly. The loss and noise with respect to power and total width are given in Figure 67 to Figure 69 for $T = 100\ \mathrm{mK}$. The graphs for $T = 60$ and $200\ \mathrm{mK}$ can be found in the Appendix: Al-SiN microstrip (imperfect fabrication).

Table 20 Design parameters for the 8 Al-SiN microstrips, including the reference Al-SiN-Si CPW. Radiation loss is not a problem in these microstrips and is hence not reported.

Microstrip	1	2	3	4	5	6	7	8	Reference CPW
$w\ [\mu\mathrm{m}]$	3	4	6	8	11	16	22	30	3
Design f_{res} $[\mathrm{GHz}]$	6.100	6.200	6.300	6.400	6.500	6.600	6.700	6.800	7.000
Actual f_{res} $[\mathrm{GHz}]$	5.775	5.917	6.051	6.096	6.165	6.226	6.351	6.550	6.631

Table 21 Power law indices for the dependencies on loss and noise for the Al-SiN microstrips in the power law fits of total width (in $\mu\mathrm{m}$), internal power (in dBm) and temperature (in K) with standard error.

Al-SiN microstrip	Total width $[\mu\mathrm{m}]$	Internal power $[\mathrm{dBm}]$	Temperature $[\mathrm{K}]$
Q	1.03 ± 0.21	Approximately flat	0.30 ± 0.12
Noise	-0.47 ± 0.04	-0.48 ± 0.01	0.80 ± 0.47

- **Loss:** The loss shows no TLS saturation and non-monotonous behaviour when widening the resonator. Motivated by Table 23, the data from the first three widths for which the loss decreases monotonously is fitted to a power law with power index 1.03 ± 0.21, in accordance with substrate-air interface dominating at small widths (numerically expected: 0.70 ± 0.04). At larger widths, the curve flattens out. Fitting the experimental data to the participation ratios calculated numerically at $P_{int} = -50\ \mathrm{dBm}$ (where according to Figure 34, a miniscule saturation slope is present much like in the experimental data) yields loss tangent estimates as given in Table 22 for 60, 100 and $200\ \mathrm{mK}$.

- The quality factor of the reference CPW is about 20 % lower than in the equivalent structure in the Al-SiN-Si CPW chip.

- **Noise:** The absolute value of the noise is comparable with the microstrip data from [29] and the TLS picture still holds, considering that the power dependency is close to the theoretical -0.5 value. However the width dependence is more difficult to interpret as it is lower (-0.47 ± 0.04) than can be expected from any contribution and is actually quite marginal. Even more troubling is that the reference CPW on Al-SiN-Si has higher noise than in the Al-SiN-Si CPW chip. Considering the poor quality factor as mentioned in the previous point, there may be another factor influencing the resonators.

Table 22 Fitted values for loss tangent $tan\ (\delta)$, resulting from fitting numerically calculated surface and bulk loss contributions. Standard errors are in parentheses.

Temperature $[\mathrm{mK}]$	$tan\ (\delta)_{substrate-air} \cdot 10^6$	$tan\ (\delta)_{bulk} \cdot 10^6$
60	1080 (773)	5.9 (0.8)
100	1060 (755)	6.0 (0.8)
200	1570 (1060)	8.7 (1.0)

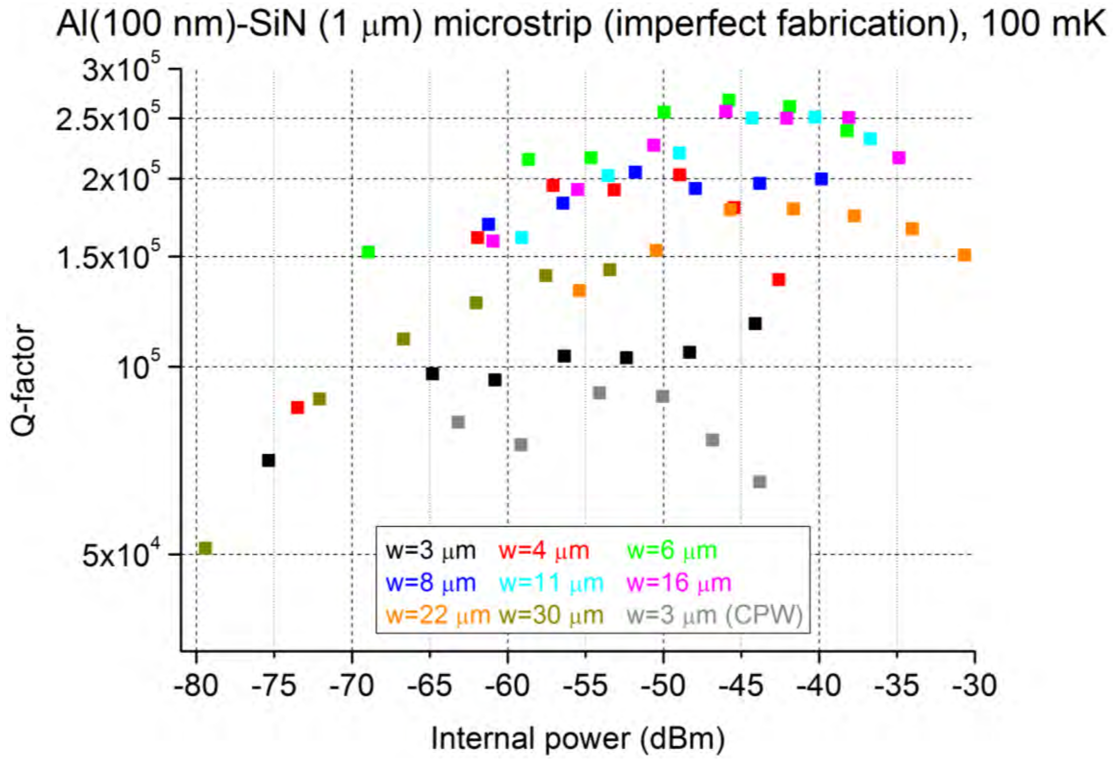


Figure 67 Internal quality factor versus internal power in dBm for the Al-SiN microstrip resonator set with Al-SiN-Si reference CPW with central width (in $\mu\mathrm{m}$) of 3 (black, CPW in grey), 4 (red), 6 (green), 8 (dark blue), 11 (cyan), 16 (magenta), 22 (orange) and 30 (olive) at $100\,\mathrm{mK}$. The inset shows the dependency on the central width and temperature respectively for the narrowest three resonators with standard error.

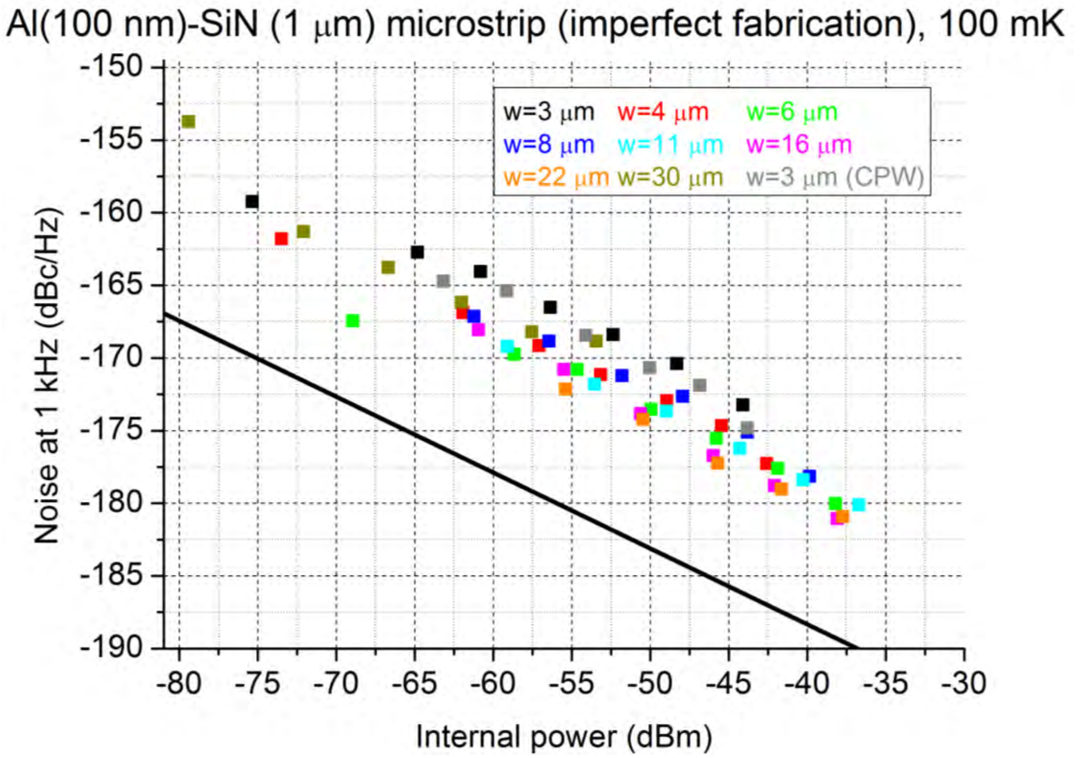


Figure 68 Noise measured at $1\,\mathrm{kHz}$ in $\mathrm{dBc/Hz}$ versus internal power in dBm for the Al-SiN microstrip resonator set with Al-SiN-Si reference CPW with central width (in $\mu\mathrm{m}$) of 3 (black, CPW in grey), 4 (red), 6 (green), 8 (dark blue), 11 (cyan), 16 (magenta), 22 (orange) and 30 (olive) at $100\,\mathrm{mK}$. The black line indicates the noise of the $t = 7\,\mu\mathrm{m}$ Nb on Si CPW from [58]. The inset shows the dependency on the total width and internal power respectively with standard error, omitting the $w = 30\,\mu\mathrm{m}$ data.

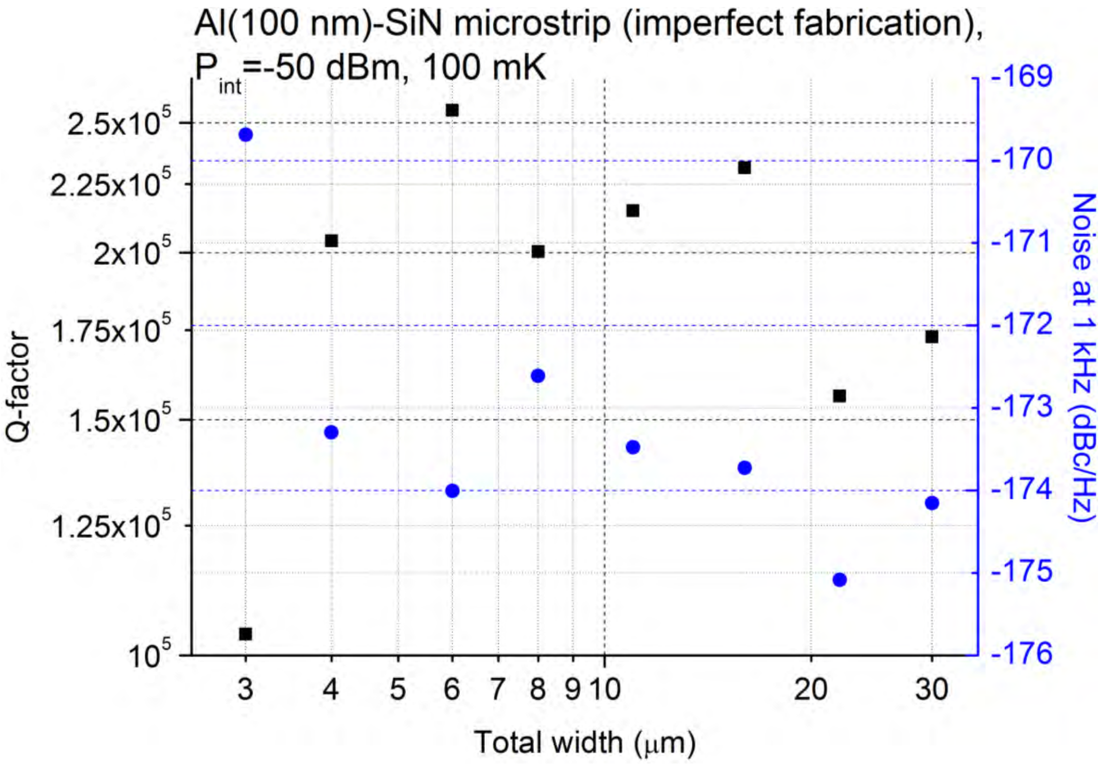


Figure 69 Dependency of Q-factor (black squares) and noise (blue circles) at $1\ \mathrm{kHz}$ in $\mathrm{dBc/Hz}$ versus on the total width in $\mu\mathrm{m}$ for the constant impedance Al-SiN microstrip resonator set at $P_{int} = -50\ \mathrm{dBm}$ for $T = 100\ \mathrm{mK}$.

6 Discussion

To draw conclusions from the experimental data, the compatibility with the numerical results of model 2 from chapter 3 must be checked. This is summarized below:

- The dependence of the noise on internal power is always within 0.03 of the predicted -0.50 power law for TLSs, hence showing excellent agreement.

- The flatness in Q with respect to internal power is also compatible with model 2, as this simply requires a higher (and hence different) saturation power for the loss than for the noise.

- The width dependencies on the noise can be accounted for by a combination of bulk and surface contributions (also implying different noise coefficients κ and TLS distributions), while for the Q, this is not always possible due to the presence of radiation loss.

Overall, the applicability of model 2 is therefore justified and can be used to interpret the experimental data:

- **Loss:** Using Si, the Q-factors are consistently more than 10^6, rather independently of the total width, until for very wide resonators with $t \geq 40\ \mu\mathrm{m}$ radiation loss becomes a factor. From numerical calculations, this is to be attributed to a balance between bulk and surface TLSs, while the upper limit on radiation loss is compatible with the behaviour at $t \geq 40\ \mu\mathrm{m}$. The observation of the latter is relevant to address in future research to fully exploit the low noise property of wide CPWs in single or hybrid configurations.

  The mere presence of SiN increases the loss by an order of magnitude, whether there is Si below the added SiN membrane or not. This would exclude the SiN-Si interface as the origin of the problem. The benefit of the lower Q in Al-SiN-Si is that the presence of radiation loss is less felt, making the loss tangent estimates of Al-SiN-Si reliable. Surface TLS are five times less more lossy than expected from [36] (namely $9 \cdot 10^{-4}$), while the bulk TLS loss tangent from [56] for Si is more or less accurate (namely $3 \cdot 10^{-6}$). This causes the contribution of both types substrate surfaces (metal-substrate and substrate-air, between which it is impossible to distinguish in CPWs) to become on the same order of the bulk contribution. The width dependency of 0.43 ± 0.02 is about half way between bulk dominated (-0.4) and surface dominated (-1.2) TLS loss.

  Additionally, the microstrip data suggests that for narrow resonators, the SiN-air interface dominates, while for wider ones either bulk SiN or the SiN-Al interfaces dominate. Also taking into account that through cleaning has mixed results on the loss, it is concluded that a combination of bulk and interface effects occurs due to the presence of SiN. A measurement with Al-SiN (bulk) CPWs can be used to further strengthen that conclusion.

- **Noise:** Using Si, the addition of a thorough cleaning step during fabrication reduces rather remarkably the TLS noise by more than $10\,\mathrm{dB}$ (about $-192\,\mathrm{dBc/Hz}$ for $t = 7\,\mu\mathrm{m}$, $P_{int} = -40\,\mathrm{dBm}$ and $T = 100\,\mathrm{mK}$) to and reduces, when considering the width dependences, not only surface TLSs but bulk TLSs as well in about equal measure. Exactly how surface cleaning could affect bulk properties as well is mysterious. The -1.58 ± 0.03 power for the width dependence in the imperfectly cleaned Si shows that the bulk has a non-negligle contribution, as about -2 is expected from simulations on surface contributions.

  Interestingly, the addition of the SiN membrane does not change the balance between surface and bulk contributions, given that the width dependencies hardly change (-1.50 ± 0.03 this time) and also the noise (about $-180\ \mathrm{dBc/Hz}$ for $t = 7\ \mu\mathrm{m}$, $P_{int} = -40\ \mathrm{dBm}$ and $T = 100\,\mathrm{mK}$) does not increase compared to the improperly cleaned Si. Unfortunately, thorough cleaning does not give much of an improvement this time. Note that this SiN layer is thin ($1\ \mu\mathrm{m}$) compared to t, meaning that the SiN is effectively a thin layer, so this deterioration cannot be attributed yet to a bulk or surface effect. In any case, SiN has inferior properties in terms of noise as well as loss and Si should be the dielectric of choice in these resonators.

  By contrast, the optimal choice of resonator type cannot be concluded yet. Microstrips, which have the benefit of high responsiity due to its smaller detector volume, are (for the same dielectric, SiN) not *that much* worse than CPWs. Furthermore, their noise is bulk dominated considering the shallow width dependence (-0.69 ± 0.03), so this motivates efforts to fabricate a microstrip on a Si membrane, which also considering the excellent results for the Al-Si CPWs with good cleaning, should display the best performance seen for microstrips so far. Also, because of this width dependence, narrow microstrips should still perform reasonably, namely $-176\,\mathrm{dBc/Hz}$ for a $w = 3\ \mu\mathrm{m}$ Al-SiN microstrip compared to $-193\,\mathrm{dBc/Hz}$ for a $t = 70\ \mu\mathrm{m}$ Al-SiN-Si CPW at $P_{int} = -40\ \mathrm{dBm}$ and $T = 100\ \mathrm{mK}$.

  The values of the noise coefficients in all chips satisfy the upper limit of 10^{-26} for Si set by the literature analysis in the previous section. This ratio (around 100) is more or less temperature independent, suggesting that only the TLS distribution is different in the bulk and the interfaces, and not the nature, compatible with the positive effect of surface cleaning on bulk Si.

  The temperature dependencies should be further examined with a chip containing NbTiN-SiN-Si resonators instead of Al, as these can provide a larger temperature range along which may be measured. However, the data on all chips indicate positive temperature dependences, which would be in contrast with the findings of [38] for Nb on Si in a slightly higher temperature range. Fabrication methods may very well influence the temperature dependence that is encountered.

7 Conclusion

In this thesis a model has been developed to numerically calculate the loss and noise based on TLS theory in microstrips and CPWs with arbitrary configurations. This model includes superconductivity, which is shown to be more general and accurate than a model using the perfect metal approximation. Summarizing these results into power laws for each geometric parameter has provided sufficient predictive capabilities to sensibly design microwave resonators. Furthermore, it allowed the determination of crucial unknowns from experimental data, such as noise spectral density coefficient κ and the loss tangents, which are necessary to conclude which TLS source dominates the loss and noise, so that depending on the application, the optimal configuration for microstrips and CPWs may be found.

From numerical calculations, contributions from the metal-air interface and metal edge can be neglected, leaving the metal-substrate, the substrate-air and the dielectric bulk as the main contributors. After measuring the loss and noise from the complex transmission of constant impedance CPW resonators containing Al on Si, a SiN membrane (the microstrip version as well) and SiN-Si at 60, 100 and $200\ \mathrm{mK}$, the following conclusions can be formulated for Si and SiN:

- **Si, noise:** the best Al CPW has been measured, with the Si thoroughly cleaned, yielding $-192\ \mathrm{dBc/Hz}$ with $t = 7\ \mu\mathrm{m}$, at $P_{int} = -40\ \mathrm{dBm}$ and $T = 100\ \mathrm{mK}$, with a $t^{-1.6}$ dependence. The noise is interface dominated, but still has some contribution of the bulk. The noise difference with NbTiN is likely to be accounted for by overetching, which does not occur for Al.

- **Si, loss:** typical values for the Q are $2 \cdot 10^6$, with a mix of surface and bulk contributions. The upper limit of the bulk loss tangent that follows from the data is below the reference value of [56], and also given that cleaning does not affect the loss that much, it is probable that the dielectric bulk dominates the loss.

- **SiN, noise:** Between $178\ \mathrm{dBc/Hz}$ (Microstrip: $w = 3\ \mu\mathrm{m}$, twice the dielectric thickness measured here) and $-180\ \mathrm{dBc/Hz}$ (CPW: $t = 7\ \mu\mathrm{m}$) at $P_{int} = -40\ \mathrm{dBm}$ and $T = 100\ \mathrm{mK}$. For microstrips, the noise is clearly bulk dominated. Because for CPWs, the SiN is a thin layer compared to t, it is difficult to distinguish a bulk SiN effect from a surface SiN effect. Experiments of Al on thicker SiN are necessary to fully determine whether the SiN is inferior due to its bulk properties or its surface properties.The measured width dependence is at least not in contradiction with bulk SiN dominance in CPW as well. It would also explain why the surface cleaning did not decrease the CPW noise.

- **SiN, loss:** typical values for the Q are $2 \cdot 10^5$, originating from a mix between the dielectric bulk and the substrate-air. For narrow microstrips, the substrate-air limits the losses, while for the wider strips, the bulk limits the losses. For CPWs, there is always a mix between bulk and surface TLSs, but by analogy to the microstrip, the surface contribution will likely come from the substrate-air interface as well.

Some other, general conclusions can be drawn:

- This TLS model can effectively describe the observed behaviour in loss and noise. That the loss is typically flat with respect to power, while the noise always exhibits the $\sqrt{P}$ saturation, can be accounted for by assigning different saturation fields. For different geometries, there may be different dominant sources for the loss and the noise. Also considering that the Si-cleaning only benefits the noise and not the loss, it must be concluded that the TLS loss and the TLS noise must be treated independently.

- This means that it remains problematic to lift the degeneracy between the surface contribution to CPW noise. The substrate-air interface dominates the loss in narrow to moderately wide microstrips. While the substrate-air interface dominance in microstrip loss is good evidence for the substrate-air to dominate the surface contributions to CPW loss as well, extrapolating this conclusion to CPW noise is invalid.

- As the width dependency is not fully determined by surfaces alone, low noise CPWs (single of hybrid) will have to be relatively wide to improve performance. However, as the Q-factor is limited by radiation losses from a total width of $40\ \mu\mathrm{m}$, that problem will have to be addressed, e.g. by the use of hybrids. Fortunately, microstrips that do not suffer from radiation losses seem to perform similar to CPWs on the same substrate. Placing microstrips on Si membranes would provide a good test for the applicability of microstrips in future detectors.

The suggestions to progress towards background limited detection in sub-mm astronomy from space are hence as follows:

- Si is the best dielectric to use, but it msut be cleaned thoroughly to maximize its performance.

- Microstrips remain viable alternatives to CPWs, but to confirm this a microstrip on a Si membrane would have to show similar noise to the CPW on Si.

- The working numerical model allows for reliable predictions of loss and noise, which will be very useful in future designs

- As Al shows such good noise performance, it becomes very likely that the remaining difference with NbTiN is due to overetching, The next logical step would be to overetch Al resonator to determine from experiments the limit to which Al resonator can be improvement by this method.

Nevertheless, more progress will have to be made to reach the photon noise limit for spectroscopy in space and therefore more suggestions for possible routes towards that goal are given in the outlook in the next chapter.

8 Outlook

As the substrate-air is the dominant surface contribution in microstrip loss and may very well contribute to the noise as well, it would be worthwhile to overetch (and/or undercut) this away as much as possible, or to put a protective layer on top of the substrate-air interface, as done in [60]. The advantage of the former is also that part of the dielectric bulk is removed, which has been shown to be important as well.

The extent to which the loss and noise may be improved by this method will have to be investigated. This experimental approach to the TLS problem also sets a short-term limit on the performance of the low noise part of so-called hybrid CPWs. These consist of a wide, long CPW to minimize noise [25], while the small central strip volume in the other part ensures high responsivity [35]. Such a KID is always preferred above a single CPW to combine responsivity with low noise, as optimizing geometrical parameters are shown to yield limited enhancements.

One may also seriously think about redirect efforts from hybrids to lumped element MKIDS (LEKIDS), shown in [35], which separate the inductance from the capacitance part by connecting one superconducting strip to a interdigitated capacitor. The idea is the same as for the hybrid CPWs, but with the benefit of easy fabrication [61]. The downside is that the capacitance per unit area is very low, meaning that LEKIDS occupy more physical space. However, as the capacitive part almost feels no electric field at all, the noise contribution would be lower than would be possible with the small, narrow responsive part of a hybrid KID.

An experimental approach could also aim to generate more theoretical understanding of the TLS nature, to discover the actual physical mechanism that is behind the remaining TLSs and then possibly resolve it. A start would be to determine the temperature dependency further by using NbTiN instead of Al, which allows for a wider temperature range. The second step would be to rethink the whole fabrication procedure, possibly imaging the structure after each step.

Finally, a route towards better sensitivity could be the use of other, low T_c materials for lower noise and materials with high kinetic inductance fractions such as in TiN [13].

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Appendix

Determination of best system size

The selection procedure of the “best” system size is as follows:

- 5 numbers, ε_{eff}, $p_{metal-air}$, $p_{metal\ edge}$, $p_{metal-substrate}$ and $p_{substrate-air}$, are calculated for 9 central strip widths with two different gap widths each, so 17 geometries (one is duplicate). For each geometry, 8 different system widths heights are used, so 64 different combinations of system sizes per geometry for which these five numbers are calculated.
- Per geometry, the values of these 5 numbers are put in 8 by 8 matrices, representing varying system width in one dimension and varying system height in the other. When meshing failed for a particular combination of system height and width, these values are set to NaN.
- The difference in values of the numbers is taken with combinations that have either one step bigger or smaller in system height or system width, divided by the latter value, as a measure of convergence towards a value. Smaller differences are better, so weights are assigned for each value of a number by the inverse of those differences, limited to a value of 1000.
- Weights are multiplied by a factor reflecting the system size, e.g. the 3rd smallest system width combined with the 4th smallest system height gets factor $3 \cdot 4 = 12$, to favour large system sizes which in principle should be more reliable. However, for model 2 this factor was limited to six per system dimension (so $6 \cdot 6 = 36$ in total), to limit the bonus for very large system sizes, which could deform the geometry (see Figure 70). This was mainly an issue in model 2, where more of the large geometries were successfully meshed.

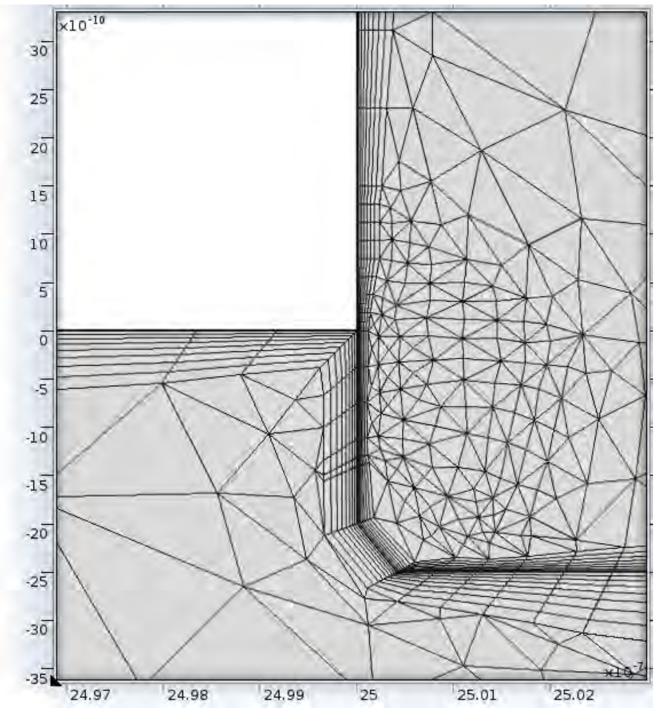

Figure 70 Meshing at corner of microstrip (model 1b). In white is the perfect metal, below is the dielectric and right is air. The thick black line indicates the boundary. Visible is the deformed corner which is not at 90 degrees, contrary to the way the geometry is programmed.

- The five values of the numbers with largest weights are assigned as the reference numbers.
- The system size that minimizes the sum of absolute relative differences between its values of the numbers compared to the reference numbers is the best system size. Differences in effective dielectric constant, metal-substrate and substrate-air participation ratios are weighted ten times more heavily than the others, because from model 1 and 2, these are normally dominant (and ε_{eff} is an important global parameter). The combinations with either or both the smallest system height or system width cannot be selected.

Model 2 – constant voltage figures

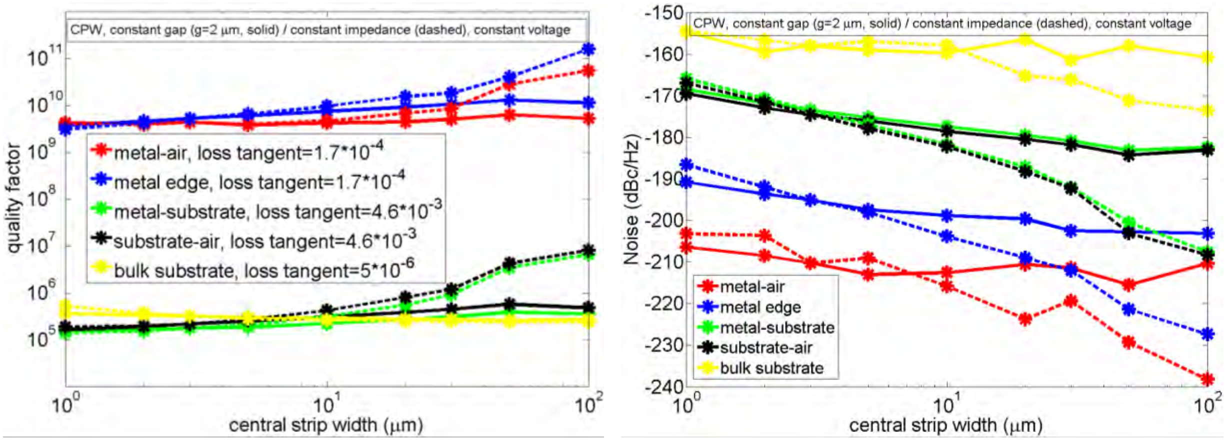

Figure 71 Left: Quality factors versus central strip width w for CPWs with superconducting film thickness $0.3\ \mu\mathrm{m}$, gap width $2\ \mu\mathrm{m}$ (solid) and $2w/3$ (dashed), for four interfaces: substrate-air (black), metal (top side)-air (red), substrate-metal (green) and metal edge–air (blue) and dielectric bulk (yellow) at constant voltage $V = 50\ \mathrm{mV}$ as calculated by COMSOL. Right: Noise (in $\mathrm{dBc/Hz}$) versus w for CPWs with gap width $2\ \mu\mathrm{m}$ (solid) and $2w/3$ (dashed) at $V = 50\ \mathrm{mV}$.

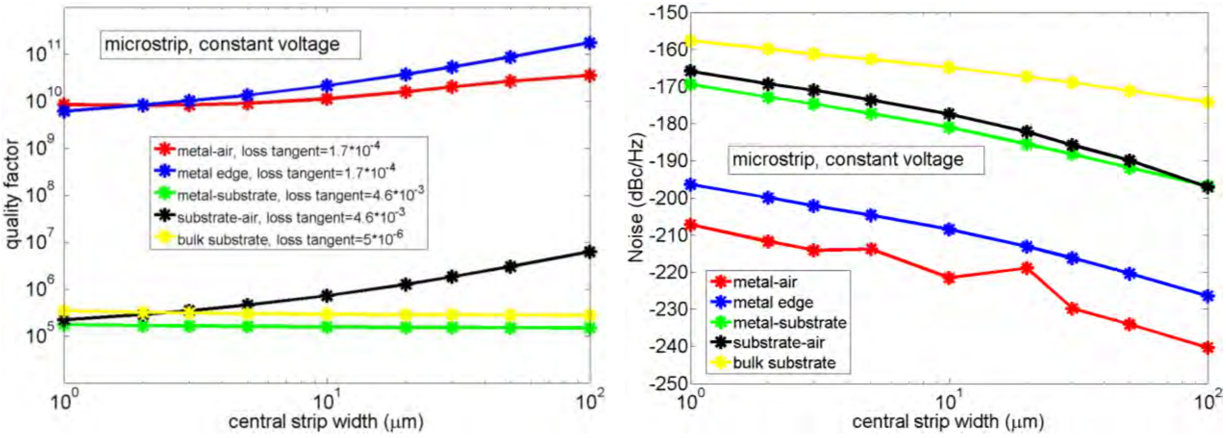

Figure 72 Left: Quality factors versus central strip width for microstrips with dielectric thickness $4\ \mu\mathrm{m}$ and film thickness $0.3\ \mu\mathrm{m}$, for four interfaces: substrate-air (black), metal (top side)-air (red), substrate-metal (green) and metal edge–air (blue) and dielectric bulk (yellow) at constant voltage $V = 50\ \mathrm{mV}$ as calculated by COMSOL. Right: Noise (in $\mathrm{dBc/Hz}$) versus central strip width (in $\mu\mathrm{m}$) for microstrips at constant voltage $V = 50\ \mathrm{mV}$.

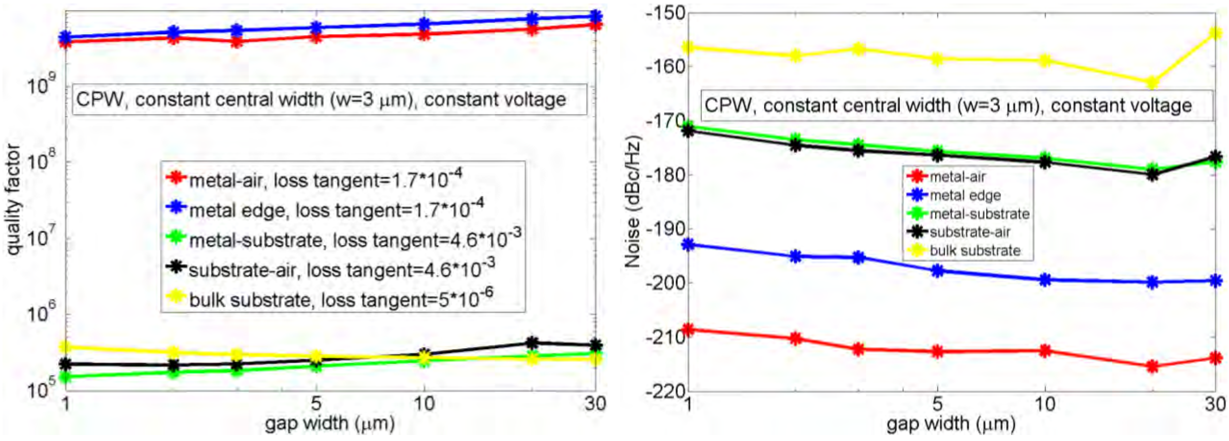

Figure 73 Left: Quality factors versus gap width (in μm) for CPWs with superconducting film thickness $0.3\ \mu m$ and film width $3\ \mu m$, for four interfaces: substrate-air (black), metal (top side)-air (red), substrate-metal (green) and metal edge–air (blue) and bulk (yellow) at constant voltage $V = 50\ mV$ as calculated by COMSOL. Right: Noise (in dBc/Hz) versus gap width (in μm) for the same CPWs at constant voltage $V = 50\ mV$.

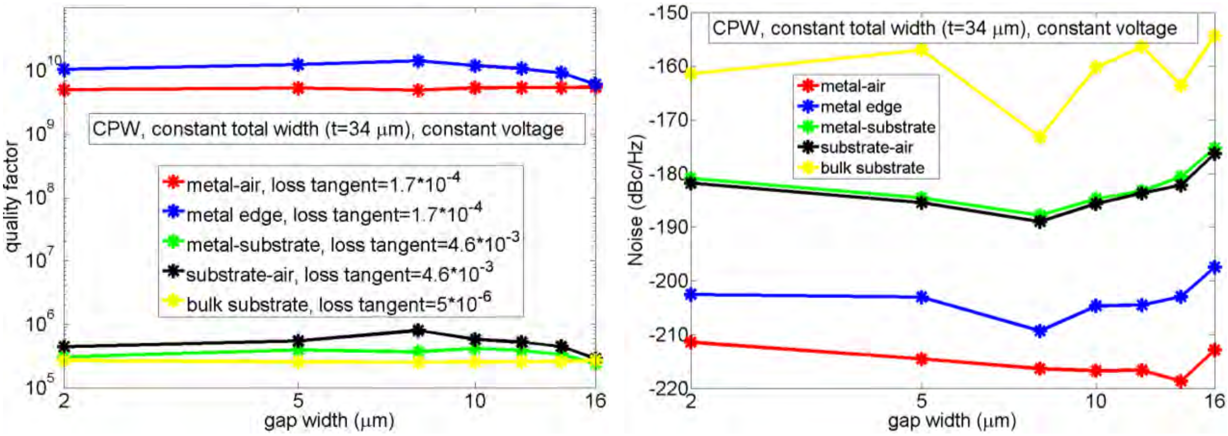

Figure 74 Left: Quality factors versus gap width (in μm) for CPWs with superconducting film thickness $0.3\ \mu m$ and total width $w + 2g = 34\ \mu m$, for four interfaces: substrate-air (black), metal (top side)-air (red), substrate-metal (green) and metal edge–air (blue) and bulk (yellow) at constant voltage $V = 50\ mV$ as calculated by COMSOL. Right: Noise (in dBc/Hz) versus gap width (in μm) for the same CPWs at constant voltage $V = 50\ mV$.

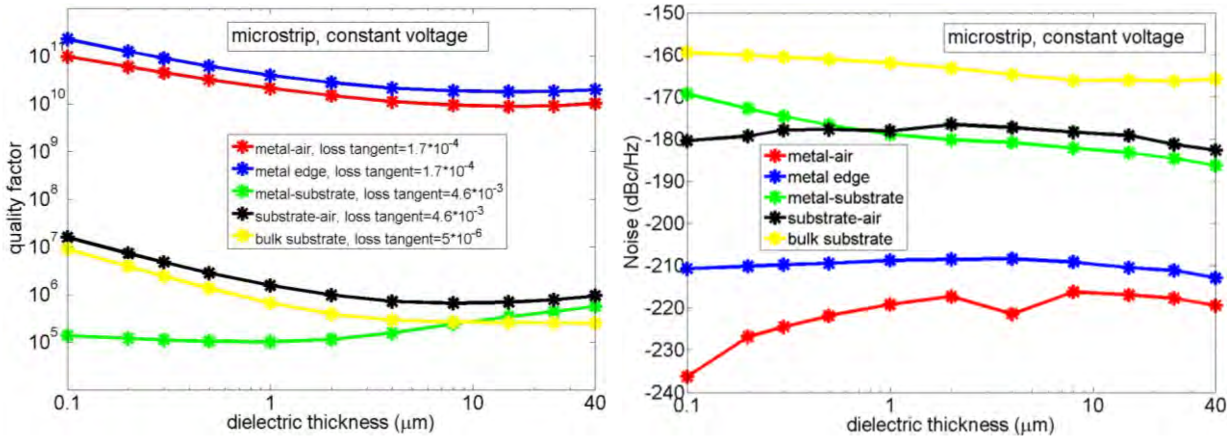

Figure 75 Left: Quality factors versus dielectric thickness (in μm) for microstrips with superconducting film thickness $0.3\ \mu m$ and central strip width $10\ \mu m$, for four interfaces: substrate-air (black), metal (top side)-air (red), substrate-metal (green) and metal edge–air (blue) and bulk (yellow) at constant voltage $V = 50\ mV$ as calculated by COMSOL. Right: Noise (in dBc/Hz) versus dielectric thickness (in μm) for the same microstrips at constant voltage $V = 50\ mV$.

Model 2 – constant current figures

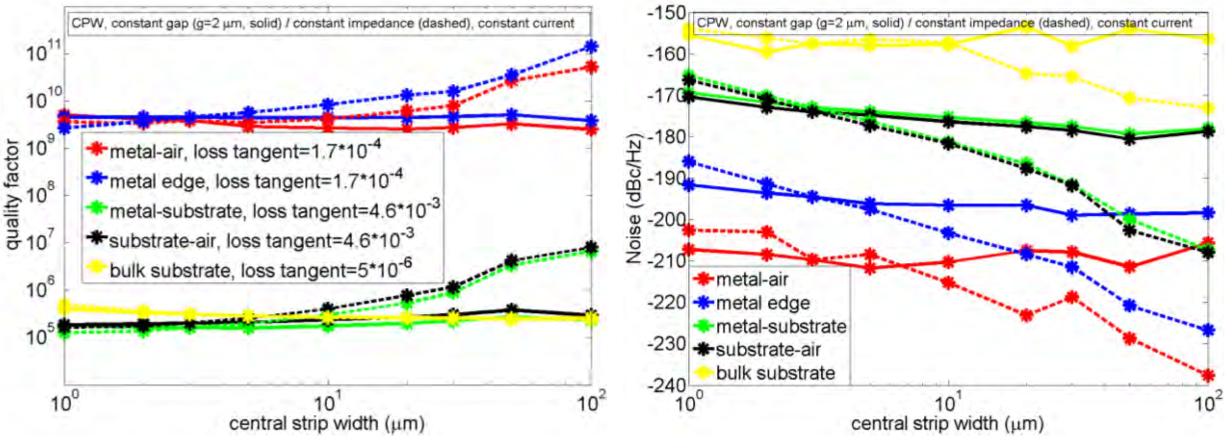

Figure 76 Left: Quality factors versus central strip width w for CPWs with superconducting film thickness $0.3\ \mu\mathrm{m}$, gap width $2\ \mu\mathrm{m}$ (solid) and $2w/3$ (dashed), for four interfaces: substrate-air (black), metal (top side)-air (red), substrate-metal (green) and metal edge–air (blue) and dielectric bulk (yellow) at constant current $I = 0.56\ \mathrm{mA}$ as calculated by COMSOL. Right: Noise (in $\mathrm{dBc/Hz}$) versus w for CPWs with gap width $2\ \mu\mathrm{m}$ (solid) and $2w/3$ (dashed) at $I = 0.56\ \mathrm{mA}$.

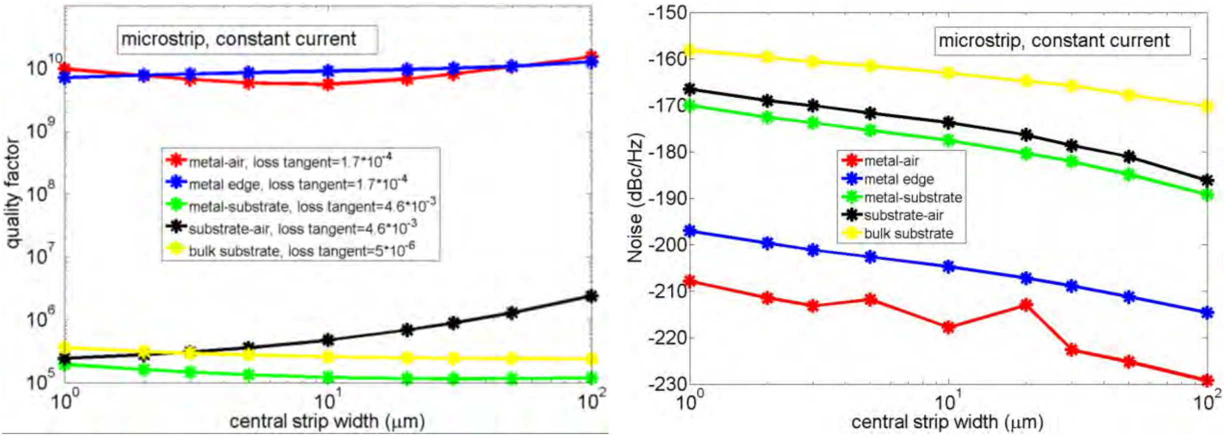

Figure 77 Left: Quality factors versus central strip width for microstrips with dielectric thickness $4\ \mu\mathrm{m}$ and film thickness $0.3\ \mu\mathrm{m}$ for four interfaces: substrate-air (black), metal (top side)-air (red), substrate-metal (green) and metal edge–air (blue) and dielectric bulk (yellow) at constant current $I = 0.56\ \mathrm{mA}$ as calculated by COMSOL. Right: Noise (in $\mathrm{dBc/Hz}$) versus central strip width for microstrips at constant current $I = 0.56\ \mathrm{mA}$.

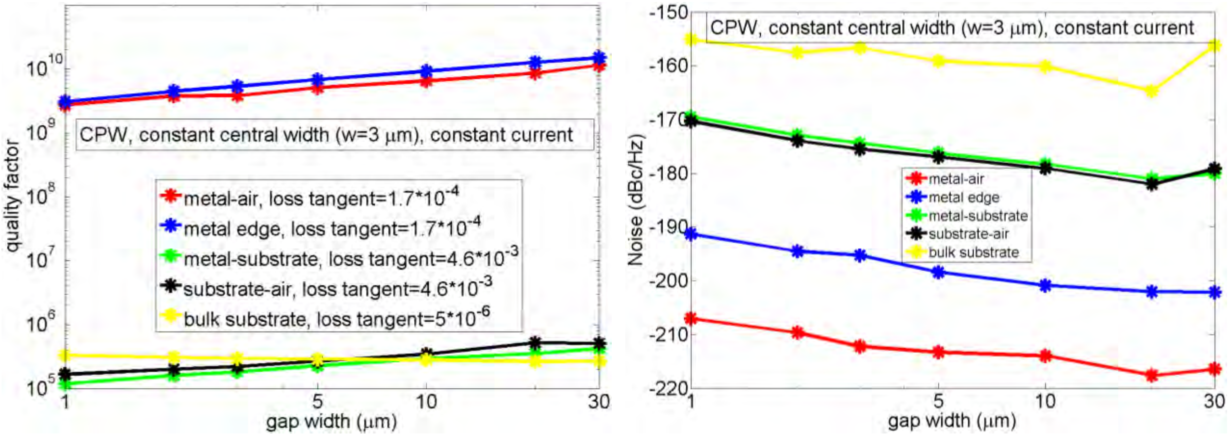

Figure 78 Left: Quality factors versus gap width (in $\mu\mathrm{m}$) for CPWs with superconducting film thickness $0.3\ \mu\mathrm{m}$ and film width $3\ \mu\mathrm{m}$, for four interfaces: substrate-air (black), metal (top side)-air (red), substrate-metal (green) and metal edge–air (blue) and bulk (yellow) at constant current $I = 0.56\ \mathrm{mA}$ as calculated by COMSOL. Right: Noise (in $\mathrm{dBc/Hz}$) versus gap width at constant current $I = 0.56\ \mathrm{mA}$.

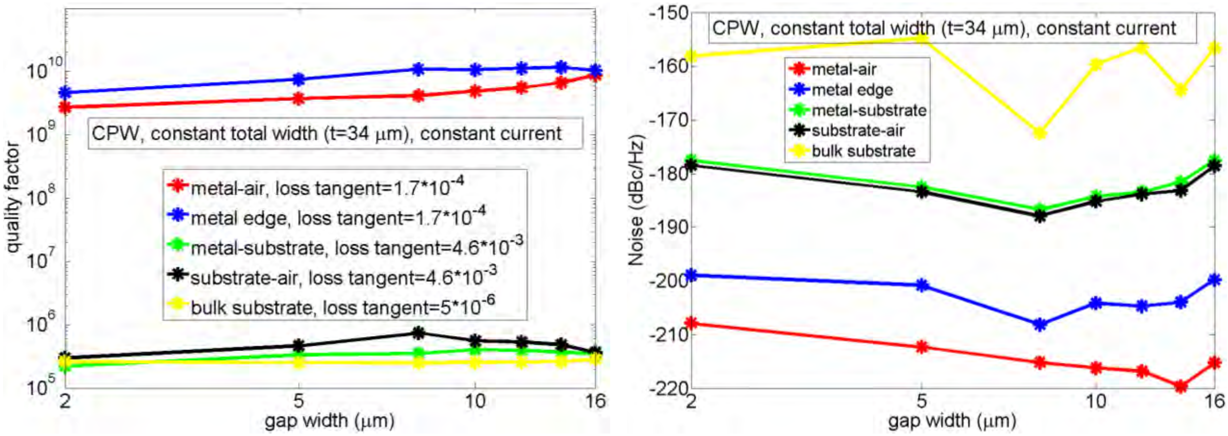

Figure 79 Left: Quality factors versus gap width (in $\mu\mathrm{m}$) for CPWs with superconducting film thickness $0.3\ \mu\mathrm{m}$ and total width $w + 2g = 34\ \mu\mathrm{m}$, for four interfaces: substrate-air (black), metal (top side)-air (red), substrate-metal (green) and metal edge–air (blue) and bulk (yellow) at constant current $I = 0.56\ \mathrm{mA}$ as calculated by COMSOL. Right: Noise (in $\mathrm{dBc/Hz}$) versus gap width at constant current $I = 0.56\ \mathrm{mA}$.

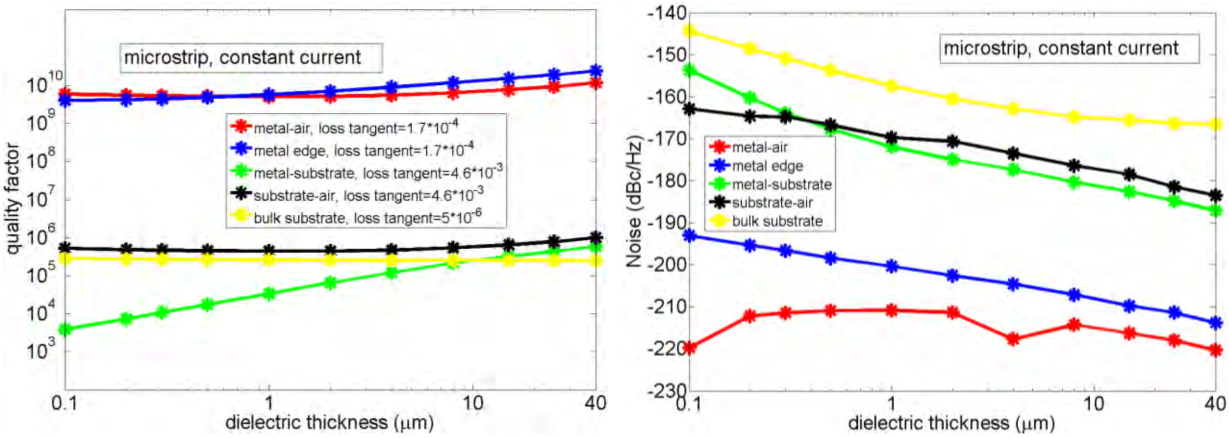

Figure 80 Left: Quality factors versus dielectric thickness (in $\mu\mathrm{m}$) for microstrips with superconducting film thickness $0.3\ \mu\mathrm{m}$ and central strip width $10\ \mu\mathrm{m}$, for four interfaces: substrate-air (black), metal (top side)-air (red), substrate-metal (green) and metal edge–air (blue) and bulk (yellow) at constant current $I = 0.56\ \mathrm{mA}$ as calculated by COMSOL. Right: Noise (in $\mathrm{dBc/Hz}$) versus dielectric thickness at constant current $I = 0.56\ \mathrm{mA}$.

Model 2 – Fit summary

For the quality factor and the noise as a function of power, the most important parameter is the "saturation power" P_s, after which a rise in Q and a drop in noise with the square root of internal power is seen. For the geometrical dependencies, the most important parameter is the power n, m, o or r with which the loss or noise scales with the relevant length scale (central strip width, gap width/dielectric thickness, overetch or total width t). These parameters are hence the only ones reported in Table 23 to Table 26 from the fitting functions (A.7) to (A.24), with a as the other fitting parameter indicating the absolute level of loss or noise at no power, $w = 1\ \mu\text{m}$, $s = 1\ \mu\text{m}$, $g = 1\ \mu\text{m}$, $d = 1\ \text{nm}$ or $t = 1\ \mu\text{m}$ and X as the physical quantity that is kept constant, which is internal power P, voltage V or current I. A complete overview of all fitting parameters is given in Table 28 to Table 32. The justification of the fitting formulae is as follows:

From (3.3), it can be seen that $\frac{1}{Q} \propto \frac{E^2/\sqrt{1+E^2/E_s^2}}{E^2} \propto \frac{1}{\sqrt{1+E^2/E_s^2}}$. As the power is given in dBm, the conversion of E to P is $P = 10\log_{10} cE^2$ with c as a constant, so that:

$$Q \propto \sqrt{1+\frac{10^{P/10}}{cE_s^2}} \propto \sqrt{1+10^{\frac{P-P_s}{10}}} \tag{A.1}$$

where $P_s \equiv 10\log_{10}(cE_s^2)$, the saturation power in dBm. This yields the fitting formula

$$Q(P) = a\sqrt{1+10^{\frac{P-P_s}{10}}} \tag{A.2}$$

where fitting parameter a represents the Q at no power (or $P = -\infty$ in dBm). Similarly, from (3.5):

$$\frac{S}{f_r^2} \propto \frac{1}{\sqrt{1+E^2/E_s^2}} \tag{A.3}$$

but as $\frac{S}{f_r^2}\left(\frac{\text{dBc}}{\text{Hz}}\right) = 10\log_{10}\frac{S}{f_r^2}$:

$$\frac{S}{f_r^2}\left(\frac{\text{dBc}}{\text{Hz}}\right) = a + 10\log_{10}\left(\frac{1}{\sqrt{1+E^2/E_s^2}}\right) = a - 5\log_{10}\left(1+\frac{E^2}{E_s^2}\right) \Rightarrow$$

$$\frac{S}{f_r^2}\left(\frac{\text{dBc}}{\text{Hz}}\right) = a - 5\log_{10}\sqrt{1+10^{\frac{P-P_s}{10}}} \tag{A.4}$$

where a is the noise level at no power.

Loss and noise as function of (central strip or gap) width, dielectric thickness or overetch are expected to be well approximated by simple power laws, e.g.:

$$Q(w) = aw^n \tag{A.5}$$

Because of the conversion of $\frac{S}{f_r^2}$ in units of$(\mathrm{dBc/Hz})$, for the noise this power law translates to:

$$\frac{S}{f_r^2}(\mathrm{dBc/Hz}) = a + 10 \cdot n \log_{10}(w) \tag{A.6}$$

The Q's and S's are a function of only one parameter at a time, given in parenthesis, keeping all others constant. Only for the dependence on the total width $t = w + 2g = 7w/3$, which only applies to the constant impedance data, both w and g vary, but as w/g is fixed, there is still only one degree of freedom, as in the other cases.

$$Q_{MSL}(P) = a_{MSL-Q}\sqrt{1 + 10^{\frac{P-P_{s,MSL-Q}}{10}}} \tag{A.7}$$

$$Q_{MSL-X}(w) = a_{MSL-QX1}w^{n_{MSL-QX}} \tag{A.8}$$

$$Q_{MSL-X}(s) = a_{MSL-QX2}s^{m_{MSL-QX}} \tag{A.9}$$

$$Q_{MSL-X}(d) = a_{MSL-QX3}d^{o_{MSL-QX}} \tag{A.10}$$

$$\frac{S_{MSL}}{f_r^2}(P)\left[\frac{\mathrm{dBc}}{\mathrm{Hz}}\right] = a_{MSL-N} - 5\log_{10}\sqrt{1 + 10^{\frac{P-P_{s,MSL-N}}{10}}} \tag{A.11}$$

$$\frac{S_{MSL-X}}{f_r^2}(w)\left[\frac{dBc}{Hz}\right] = a_{MSL-NX1} + 10\, n_{MSL-NX}\log_{10}(w) \tag{A.12}$$

$$\frac{S_{MSL-X}}{f_r^2}(s)\left[\frac{dBc}{Hz}\right] = a_{MSL-NX2} + 10\, m_{MSL-NX}\log_{10}(s) \tag{A.13}$$

$$\frac{S_{MSL-X}}{f_r^2}(d)\left[\frac{dBc}{Hz}\right] = a_{MSL-NX3} + 10\, o_{MSL-NX}\log_{10}(d) \tag{A.14}$$

$$Q_{CPW}(P) = a_{CPW-Q}\sqrt{1 + 10^{\frac{P-P_{s,CPW-Q}}{10}}} \tag{A.15}$$

$$Q_{CPW-X}(w) = a_{CPW-QX1}w^{n_{CPW-QX}} \tag{A.16}$$

$$Q_{CPW-X}(g) = a_{CPW-QX2}g^{m_{CPW-QX}} \tag{A.17}$$

$$Q_{CPW-X}(d) = a_{CPW-QX3}d^{o_{CPW-QX}} \tag{A.18}$$

$$Q_{CPW-X}(t) = a_{CPW-QX4}t^{r_{CPW-QX}} \tag{A.19}$$

$$\frac{S_{CPW}}{f_r^2}\left[\frac{dBc}{Hz}\right] = a_{CPW-N} - 5\log_{10}\sqrt{1+10^{\frac{P-P_{s,CPW-N}}{10}}} \tag{A.20}$$

$$\frac{S_{CPW-X}}{f_r^2}(w)\left[\frac{dBc}{Hz}\right] = a_{CPW-NX1} + 10\, n_{CPW-NX}\log_{10}(w) \tag{A.21}$$

$$\frac{S_{CPW-X}}{f_r^2}(g)\left[\frac{dBc}{Hz}\right] = a_{CPW-NX2} + 10\, m_{CPW-NX}\log_{10}(g) \tag{A.22}$$

$$\frac{S_{CPW-X}}{f_r^2}(d)\left[\frac{dBc}{Hz}\right] = a_{CPW-NX3} + 10\, o_{CPW-NX}\log_{10}(d) \tag{A.23}$$

$$\frac{S_{CPW-X}}{f_r^2}(t)\left[\frac{dBc}{Hz}\right] = a_{CPW-NX4} + 10\, r_{CPW-NX}\log_{10}(t) \tag{A.24}$$

Table 23 Fit parameters P_s (saturation power in dBm) and power indices n, m and o for constant power P and constant voltage V for microstrip loss for four surfaces (metal-air, metal-edge, metal-substrate and substrate-air), the dielectric bulk and the total of those. Power index o at constant voltage is the same as at constant power, as the impedance does not change when overetching. Standard errors are in parentheses.

MSL-Q	$P_{s,MSL-Q}$	n_{MSL-QP}	m_{MSL-QP}	o_{MSL-QP}	n_{MSL-QV}	m_{MSL-QV}
Metal-air	−52.26 (1.18)	0.08 (0.04)	−0.08 (0.03)	−0.03 (0.00)	0.29 (0.02)	−0.66 (0.04)
Metal-edge	−69.29 (0.44)	0.47 (0.02)	−0.07 (0.04)	0.05 (0.00)	0.94 (0.03)	−0.75 (0.06)
Metal-substrate	−33.51 (0.27)	−0.24 (0.01)	0.55 (0.01)	0.02 (0.00)	−0.05 (0.01)	0.02 (0.03)
Substrate-air	−34.90 (0.48)	0.70 (0.04)	−0.44 (0.06)	−0.06 (0.01)	0.95 (0.04)	−1.10 (0.02)
Dielectric bulk	−25.57 (0.10)	−0.17 (0.01)	−0.63 (0.04)	0.03 (0.01)	0.01 (0.00)	−1.20 (0.01)
Total	−31.90 (0.29)	−0.12 (0.00)	0.21 (0.01)	−0.01 (0.00)	0.05 (0.00)	−0.28 (0.01)

Table 24 Fit parameters P_s (saturation power in dBm) and power indices n, m and o for constant power P and constant voltage V for microstrip noise for four surfaces (metal-air, metal-edge, metal-substrate and substrate-air), the dielectric bulk and the total of those, excluding the bulk. Power index o at constant voltage is the same as at constant power, as the impedance does not change when overetching. Standard errors are in parentheses.

MSL-Noise	$P_{s,MSL-N}$	n_{MSL-NP}	m_{MSL-NP}	o_{MSL-NP}	n_{MSL-NV}	m_{MSL-NV}
Metal-air	−82.30 (0.30)	−1.27 (0.17)	0.15 (0.13)	−0.01 (0.03)	−1.58 (0.18)	0.51 (0.14)
Metal-edge	−76.26 (0.09)	−1.16 (0.04)	−0.41 (0.03)	−0.35 (0.01)	−1.48 (0.06)	−0.05 (0.05)
Metal-substrate	−51.57 (0.07)	−1.07 (0.03)	−0.92 (0.05)	−0.40 (0.01)	−1.31 (0.03)	−0.56 (0.04)
Substrate-air	−57.56 (0.07)	−1.21 (0.07)	−0.44 (0.05)	−0.49 (0.02)	−1.52 (0.08)	−0.08 (0.06)
Dielectric bulk	−40.63 (0.38)	−0.59 (0.03)	−0.61 (0.03)	−0.04 (0.00)	−0.73 (0.03)	−0.20 (0.00)
Total	−55.50 (0.09)	−1.16 (0.05)	−0.73 (0.04)	−0.45 (0.02)	−1.43 (0.06)	−0.37 (0.03)

Table 25 Fit parameters P_s (saturation power in dBm) and power indices n, m, o and r for constant power P and constant voltage V for CPW loss for four surfaces (metal-air, metal-edge, metal-substrate and substrate-air), the dielectric bulk and the total of those. Power indices o and r at constant voltage are the same as at constant power, as the impedance does not change when overetching and varying the total width. Standard errors are in parentheses.

CPW-Q	$P_{s,CPW-Q}$	n_{CPW-QP}	m_{CPW-QP}	o_{CPW-QP}	r_{CPW-QP}	n_{CPW-QV}	m_{CPW-QV}
Metal-air	−53.57 (0.20)	−0.09 (0.03)	0.29 (0.04)	−0.06 (0.01)	0.95 (0.14)	0.03 (0.03)	0.11 (0.05)
Metal-edge	−66.76 (0.19)	0.13 (0.02)	0.32 (0.00)	0.01 (0.01)	1.65 (0.13)	0.25 (0.03)	0.18 (0.01)
Metal-substrate	−37.93 (0.25)	0.07 (0.03)	0.25 (0.03)	0.09 (0.02)	1.21 (0.13)	0.07 (0.02)	0.08 (0.06)
Substrate-air	−38.25 (0.17)	0.15 (0.03)	0.20 (0.04)	−0.03 (0.00)	1.18 (0.12)	0.24 (0.03)	−0.11 (0.05)
Dielectric bulk	−23.26 (0.18)	−0.19 (0.02)	−0.19 (0.02)	0.02 (0.00)	−0.40 (0.06)	−0.29 (0.01)	−0.44 (0.02)
Total	−33.87 (0.39)	0.00 (0.01)	0.06 (0.01)	0.02 (0.01)	0.14 (0.03)	−0.08 (0.01)	−0.22 (0.02)

Table 26 Fit parameters P_s (saturation power in dBm) and power indices n, m, o and r for constant power P and constant voltage V for CPW noise for four surfaces (metal-air, metal-edge, metal-substrate and substrate-air), the dielectric bulk and the total of those, excluding the bulk. Power indices o and r at constant V are the same as at constant P, as the impedance does not change when overetching or varying the total width. Standard errors are in parentheses.

CPW-Noise	$P_{s,CPW-N}$	n_{CPW-NP}	m_{CPW-NP}	o_{CPW-NP}	r_{CPW-NP}	n_{CPW-NV}	m_{CPW-NV}
Metal-air	-73.72 (0.27)	-0.09 (0.11)	-0.52 (0.08)	0.08 (0.08)	-1.69 (0.18)	-0.24 (0.12)	-0.38 (0.08)
Metal-edge	-87.68 (0.08)	-0.49 (0.05)	-0.62 (0.07)	-0.44 (0.05)	-2.00 (0.10)	-0.63 (0.05)	-0.48 (0.07)
Metal-substrate	-55.14 (0.06)	-0.59 (0.05)	-0.61 (0.07)	-0.56 (0.01)	-2.00 (0.12)	-0.73 (0.05)	-0.46 (0.06)
Substrate-air	-56.03 (0.07)	-0.58 (0.05)	-0.53 (0.11)	-0.55 (0.03)	-2.02 (0.13)	-0.72 (0.06)	-0.39 (0.11)
Dielectric bulk	-57.61 (0.26)	-0.05 (0.09)	-0.21 (0.21)	-0.24 (0.02)	-0.98 (0.12)	-0.20 (0.09)	-0.06 (0.20)
Total	-56.39 (0.11)	-0.59 (0.05)	-0.57 (0.09)	-0.56 (0.02)	-2.01 (0.12)	-0.73 (0.05)	-0.43 (0.08)

Regarding the experimental unknowns, namely the loss tangent of each surface, the saturation fields and the κ for the noise, it is interesting to consider the influence on the parameters. The saturation power is positively correlated to the saturation field, while the a's contain information about the loss tangents and κ for the noise. Interestingly, the geometrical power dependencies are more or less material independent, given that fitting the results from model 1b (perfect metal) mostly gives values reasonably similar to model 2 (with superconductivity) (except for the constant impendance CPW loss) and the dielectric constants typically have a limited range of 7 (SiN, [62]) to 11.9 (Si, [63]).

Table 27 Fit parameters power indices n and t for constant power P for perfect metal (model 1b) microstrip and CPW loss and noise for four surfaces (metal-air, metal-edge, metal-substrate and substrate-air), and the total of those. Standard errors are in parentheses.

Perfect metal	n_{MSL-QP}	n_{MSL-NP}	n_{CPW-QP}	r_{CPW-QP}	n_{CPW-NP}	r_{CPW-NP}
Metal-air	0.48 (0.09)	-1.25 (0.16)	0.02 (0.04)	0.56 (0.10)	-0.18 (0.19)	-1.27 (0.18)
Metal-edge	0.48 (0.02)	-1.15 (0.05)	0.23 (0.01)	0.54 (0.07)	-0.65 (0.05)	-1.51 (0.06)
Metal-substrate	-0.22 (0.01)	-1.05 (0.03)	0.20 (0.04)	0.61 (0.05)	-0.69 (0.02)	-1.55 (0.01)
Substrate-air	0.71 (0.04)	-1.15 (0.06)	0.27 (0.02)	0.69 (0.07)	-0.67 (0.02)	-1.50 (0.03)
Total	-0.08 (0.01)	-1.10 (0.04)	0.23 (0.03)	0.65 (0.05)	-0.68 (0.02)	-1.52 (0.02)

Model 2 – All fit parameters

Table 28 Fitting parameters for the geometrical dependencies of microstrip loss at $250\ \mathrm{mK}$ of the metal-air (ma), metal edge (me), metal-substrate (ms) and substrate-air (sa) interfaces, dielectric bulk (db) and the total (to) following formulae (A.8) to (A.10).

		$a_{MSL-QX1}$	n_{MSL-QX}	$a_{MSL-QX2}$	m_{MSL-QX}	$a_{MSL-QX3}$	o_{MSL-QX}
Constant power	**ma**	1.73E+10 (1.82E+09)	0.08 (0.04)	2.37E+10 (1.18E+09)	-0.08 (0.03)	1.92E+10 (2.67E+08)	-0.03 (0.00)
	me	1.23E+10 (1.02E+09)	0.47 (0.02)	4.88E+10 (3.47E+09)	-0.07 (0.04)	2.14E+10 (2.31E+08)	0.05 (0.00)
	ms	3.62E+05 (4.78E+03)	-0.24 (0.01)	1.02E+05 (4.19E+03)	0.55 (0.01)	2.67E+05 (3.70E+03)	0.02 (0.00)
	sa	1.88E+05 (3.40E+04)	0.70 (0.04)	1.84E+06 (2.06E+05)	-0.44 (0.06)	6.79E+05 (3.60E+04)	-0.06 (0.01)
	db	5.25E+05 (5.81E+03)	-0.17 (0.01)	6.85E+05 (5.19E+04)	-0.63 (0.04)	4.01E+05 (1.13E+04)	0.03 (0.01)
	to	1.48E+05 (1.13E+03)	-0.12 (0.00)	8.01E+04 (1.73E+03)	0.21 (0.01)	1.34E+05 (1.85E+03)	-0.01 (0.00)
Constant voltage	**ma**	5.09E+10 (4.41E+09)	0.29 (0.02)	1.85E+11 (1.36E+10)	-0.66 (0.04)	7.19E+10 (9.95E+08)	-0.03 (0.00)
	me	2.04E+10 (2.70E+09)	0.94 (0.03)	3.55E+11 (4.08E+10)	-0.75 (0.06)	8.57E+10 (9.21E+08)	0.05 (0.00)
	ms	9.62E+05 (1.30E+04)	-0.05 (0.01)	1.01E+06 (6.24E+04)	0.02 (0.03)	8.49E+05 (1.87E+04)	0.02 (0.00)
	sa	3.80E+05 (5.82E+04)	0.95 (0.04)	1.05E+07 (4.93E+05)	-1.10 (0.02)	2.08E+06 (1.03E+05)	-0.05 (0.01)
	db	1.22E+06 (1.26E+04)	0.01 (0.00)	5.16E+06 (7.44E+04)	-1.20 (0.01)	1.04E+06 (6.59E+04)	0.05 (0.01)
	to	3.84E+05 (4.32E+03)	0.05 (0.00)	6.56E+05 (1.11E+04)	-0.28 (0.01)	4.00E+05 (1.20E+03)	0.00 (0.00)
Constant current	**ma**	5.34E+10 (3.01E+09)	-0.24 (0.03)	1.94E+10 (9.97E+08)	0.30 (0.02)	4.11E+10 (5.67E+08)	-0.03 (0.00)
	me	4.58E+10 (3.50E+08)	0.09 (0.00)	3.66E+10 (1.99E+09)	0.37 (0.02)	4.78E+10 (5.14E+08)	0.05 (0.00)
	ms	8.40E+05 (1.62E+04)	-0.45 (0.02)	1.18E+05 (7.68E+03)	0.65 (0.02)	5.04E+05 (9.07E+03)	0.02 (0.00)
	sa	6.06E+05 (1.14E+05)	0.39 (0.05)	1.65E+06 (9.85E+04)	0.01 (0.03)	1.26E+06 (6.51E+04)	-0.06 (0.01)
	db	1.07E+06 (1.96E+04)	-0.36 (0.01)	6.10E+05 (1.70E+03)	-0.21 (0.00)	6.59E+05 (3.28E+04)	0.04 (0.01)
	to	3.30E+05 (7.54E+03)	-0.33 (0.01)	8.04E+04 (9.68E+03)	0.30 (0.04)	2.42E+05 (1.48E+03)	0.00 (0.00)

Table 29 Fitting parameters for the geometrical dependencies of microstrip noise at $250\ \mathrm{mK}$ and $1\ \mathrm{kHz}$ of the metal-air (ma), metal edge (me), metal-substrate (ms) and substrate-air (sa) interfaces, dielectric bulk (db) and the total (to) excluding the bulk following formulae (A.12) to (A.14).

		$a_{MSL-NX1}$	n_{MSL-NX}	$a_{MSL-NX2}$	m_{MSL-NX}	$a_{MSL-NX3}$	o_{MSL-NX}
Constant power	**ma**	-211.41 (1.95)	-1.27 (0.17)	-223.67 (1.15)	0.15 (0.13)	-216.47 (0.71)	-0.01 (0.03)
	me	-200.99 (0.51)	-1.16 (0.04)	-210.20 (0.28)	-0.41 (0.03)	-205.68 (0.23)	-0.35 (0.01)
	ms	-174.07 (0.38)	-1.07 (0.03)	-177.61 (0.50)	-0.92 (0.05)	-178.08 (0.25)	-0.40 (0.01)
	sa	-169.90 (0.79)	-1.21 (0.07)	-179.11 (0.42)	-0.44 (0.05)	-175.96 (0.52)	-0.49 (0.02)
	db	-161.74 (0.36)	-0.59 (0.03)	-162.44 (0.25)	-0.61 (0.03)	-164.73 (0.07)	-0.04 (0.00)
	to	-168.55 (0.62)	-1.16 (0.05)	-174.62 (0.35)	-0.73 (0.04)	-173.90 (0.40)	-0.45 (0.02)
Constant voltage	**ma**	-216.07 (2.08)	-1.58 (0.18)	-233.80 (1.26)	0.51 (0.14)	-222.49 (0.71)	-0.01 (0.03)
	me	-205.64 (0.72)	-1.48 (0.06)	-220.34 (0.43)	-0.05 (0.05)	-211.70 (0.23)	-0.35 (0.01)
	ms	-179.06 (0.39)	-1.31 (0.03)	-187.68 (0.37)	-0.56 (0.04)	-184.17 (0.27)	-0.39 (0.01)
	sa	-174.56 (1.00)	-1.52 (0.08)	-189.24 (0.57)	-0.08 (0.06)	-182.12 (0.55)	-0.48 (0.03)
	db	-166.65 (0.32)	-0.73 (0.03)	-172.12 (0.04)	-0.20 (0.00)	-170.19 (0.06)	-0.03 (0.00)
	to	-173.38 (0.71)	-1.43 (0.06)	-184.72 (0.31)	-0.37 (0.03)	-180.02 (0.43)	-0.44 (0.02)
Constant current	**ma**	-216.25 (1.84)	-0.96 (0.16)	-223.05 (1.05)	-0.21 (0.12)	-219.95 (0.71)	-0.01 (0.03)
	me	-205.84 (0.31)	-0.84 (0.03)	-209.57 (0.14)	-0.78 (0.02)	-209.16 (0.23)	-0.35 (0.01)
	ms	-178.77 (0.30)	-0.78 (0.03)	-176.99 (0.63)	-1.28 (0.07)	-181.62 (0.26)	-0.39 (0.01)
	sa	-174.73 (0.59)	-0.89 (0.05)	-178.48 (0.28)	-0.80 (0.03)	-179.56 (0.55)	-0.48 (0.02)
	db	-165.84 (0.48)	-0.34 (0.04)	-161.63 (0.38)	-0.92 (0.04)	-167.77 (0.06)	-0.03 (0.00)
	to	-173.32 (0.47)	-0.85 (0.04)	-174.00 (0.43)	-1.08 (0.05)	-177.47 (0.43)	-0.44 (0.02)

Table 30 Fitting parameters for the power dependencies of microstrip and CPW loss and noise at $250\ \mathrm{mK}$ and $1\ \mathrm{kHz}$ of the metal-air (ma), metal edge (me), metal-substrate (ms) and substrate-air (sa) interfaces, dielectric bulk (db) and the total (to) excluding the bulk noise following formulae (A.7), (A.11), (A.15) and (A.20).

		a_{MSL-Q}	$P_{s,MSL-Q}$	a_{MSL-N}	$P_{s,MSL-N}$	a_{CPW-Q}	$P_{s,CPW-Q}$	a_{CPW-N}	$P_{s,CPW-N}$
Constant power	**ma**	7.18E+08	-52.26	-188.20	-82.30	3.71E+08	-53.57	-190.97	-73.72
		(9.62E+07)	(1.18)	(0.12)	(0.30)	(8.58E+06)	(0.20)	(0.10)	(0.27)
	me	1.43E+08	-69.29	-182.75	-76.26	1.00E+08	-66.76	-168.59	-87.68
		(7.01E+06)	(0.44)	(0.04)	(0.09)	(2.12E+06)	(0.19)	(0.03)	(0.08)
	ms	8.07E+04	-33.51	-167.94	-51.57	6.62E+04	-37.93	-163.19	-55.14
		(2.43E+03)	(0.27)	(0.02)	(0.07)	(1.88E+03)	(0.25)	(0.02)	(0.06)
	sa	1.37E+05	-34.90	-163.91	-57.56	8.41E+04	-38.25	-163.82	-56.03
		(7.44E+03)	(0.48)	(0.02)	(0.07)	(1.60E+03)	(0.17)	(0.02)	(0.07)
	db	2.62E+05	-25.57	-157.39	-40.63	2.74E+05	-23.26	-146.46	-57.61
		(2.88E+03)	(0.10)	(0.10)	(0.38)	(5.13E+03)	(0.18)	(0.09)	(0.26)
	to	4.29E+04	-31.90	-162.44	-55.50	3.46E+04	-33.87	-160.08	-56.39
		(1.40E+03)	(0.29)	(0.03)	(0.09)	(1.54E+03)	(0.39)	(0.04)	(0.11)

Table 31 Fitting parameters for the geometrical dependencies of CPW loss at $250\ \mathrm{mK}$ of the metal-air (ma), metal edge (me), metal-substrate (ms) and substrate-air (sa) interfaces, dielectric bulk (db) and the total following formulae (A.16) to (A.19).

		$a_{CPW-QX1}$	n_{CPW-QX}	$a_{CPW-QX2}$	m_{CPW-QX}	$a_{CPW-QX3}$	o_{CPW-QX}	$a_{CPW-QX4}$	r_{CPW-QX}
Constant power	**ma**	1.04E+10	-0.09	7.27E+09	0.29	1.00E+10	-0.06	4.08E+08	0.95
		(6.27E+08)	(0.03)	(7.78E+08)	(0.04)	(4.05E+08)	(0.01)	(3.02E+08)	(0.14)
	me	1.09E+10	0.13	9.68E+09	0.32	1.23E+10	0.01	3.97E+07	1.65
		(8.55E+08)	(0.02)	(1.26E+08)	(0.00)	(5.80E+08)	(0.01)	(2.70E+07)	(0.13)
	ms	3.15E+05	0.07	2.73E+05	0.25	2.43E+05	0.09	1.05E+04	1.21
		(2.52E+04)	(0.03)	(1.93E+04)	(0.03)	(2.50E+04)	(0.02)	(6.97E+03)	(0.13)
	sa	3.64E+05	0.15	3.58E+05	0.20	4.36E+05	-0.03	1.51E+04	1.18
		(3.29E+04)	(0.03)	(3.76E+04)	(0.04)	(6.39E+03)	(0.00)	(9.23E+03)	(0.12)
	db	5.53E+05	-0.19	5.02E+05	-0.19	4.15E+05	0.02	1.12E+06	-0.40
		(1.97E+04)	(0.02)	(1.50E+04)	(0.02)	(9.05E+03)	(0.00)	(1.40E+05)	(0.06)
	to	1.31E+05	0.00	1.23E+05	0.06	1.20E+05	0.02	1.02E+05	0.14
		(4.33E+03)	(0.01)	(3.00E+03)	(0.01)	(3.09E+03)	(0.01)	(1.13E+04)	(0.03)
Constant voltage	**ma**	3.40E+10	0.03	3.15E+10	0.11	3.73E+10	-0.06	7.65E+09	0.53
		(2.42E+09)	(0.03)	(3.79E+09)	(0.05)	(1.61E+09)	(0.01)	(3.80E+09)	(0.10)
	me	3.82E+10	0.25	4.08E+10	0.18	4.75E+10	0.01	2.20E+08	1.57
		(4.63E+09)	(0.03)	(5.47E+08)	(0.01)	(2.23E+09)	(0.01)	(1.41E+08)	(0.12)
	ms	1.01E+06	0.07	1.02E+06	0.08	8.77E+05	0.07	4.51E+04	1.00
		(4.94E+04)	(0.02)	(1.36E+05)	(0.06)	(7.33E+04)	(0.01)	(3.25E+04)	(0.14)
	sa	1.21E+06	0.24	1.63E+06	-0.11	1.66E+06	-0.06	7.56E+04	0.93
		(1.44E+05)	(0.03)	(1.54E+05)	(0.05)	(6.74E+04)	(0.01)	(5.41E+04)	(0.14)
	db	1.31E+06	-0.29	1.35E+06	-0.44	9.84E+05	0.00	4.45E+06	-0.73
		(3.29E+04)	(0.01)	(3.71E+04)	(0.02)	(1.42E+04)	(0.00)	(3.00E+05)	(0.05)
	to	4.08E+05	-0.08	4.44E+05	-0.22	3.82E+05	-0.01	5.95E+05	-0.22
		(1.10E+04)	(0.01)	(1.58E+04)	(0.02)	(4.14E+03)	(0.00)	(3.45E+04)	(0.02)
Constant current	**ma**	2.86E+10	-0.26	1.48E+10	0.41	2.26E+10	-0.06	2.70E+09	0.67
		(1.39E+09)	(0.03)	(2.86E+09)	(0.07)	(9.56E+08)	(0.01)	(1.66E+09)	(0.12)
	me	2.86E+10	-0.01	2.07E+10	0.45	2.86E+10	0.01	1.20E+08	1.59
		(1.36E+09)	(0.02)	(4.19E+08)	(0.01)	(1.34E+09)	(0.01)	(7.87E+07)	(0.12)
	ms	8.33E+05	-0.14	5.13E+05	0.36	5.36E+05	0.07	2.24E+04	1.10
		(6.08E+04)	(0.03)	(1.28E+05)	(0.09)	(4.74E+04)	(0.02)	(1.56E+04)	(0.13)
	sa	9.18E+05	0.00	7.59E+05	0.20	9.96E+05	-0.05	3.37E+04	1.06
		(4.83E+04)	(0.02)	(7.04E+04)	(0.04)	(3.46E+04)	(0.01)	(2.26E+04)	(0.13)
	db	1.09E+06	-0.37	8.18E+05	-0.24	6.85E+05	0.00	2.70E+06	-0.63
		(4.00E+04)	(0.03)	(2.08E+04)	(0.02)	(1.08E+04)	(0.00)	(2.59E+05)	(0.06)
	to	3.15E+05	-0.19	2.43E+05	0.02	2.44E+05	0.00	3.06E+05	-0.09
		(1.22E+04)	(0.02)	(1.14E+04)	(0.02)	(2.83E+03)	(0.00)	(2.70E+04)	(0.03)

Table 32 Fitting parameters for the geometrical dependencies of CPW noise at $250\ \mathrm{mK}$ and $1\ \mathrm{kHz}$ of the metal-air (ma), metal edge (me), metal-substrate (ms) and substrate-air (sa) interfaces, dielectric bulk (db) and the total (to) excluding the bulk following formulae (A.21) to (A.24).

		$a_{CPW-NX1}$	n_{CPW-NX}	$a_{CPW-NX2}$	m_{CPW-NX}	$a_{CPW-NX3}$	o_{CPW-NX}	$a_{CPW-NX4}$	r_{CPW-NX}
Constant power	**ma**	-213.98 (1.36)	-0.09 (0.11)	-213.67 (0.71)	-0.52 (0.08)	-214.28 (1.70)	0.08 (0.08)	-198.58 (2.65)	-1.69 (0.18)
	me	-197.34 (0.58)	-0.49 (0.05)	-197.79 (0.63)	-0.62 (0.07)	-198.92 (1.09)	-0.44 (0.05)	-182.51 (1.55)	-2.00 (0.10)
	ms	-174.96 (0.57)	-0.59 (0.05)	-176.12 (0.59)	-0.61 (0.07)	-175.72 (0.22)	-0.56 (0.01)	-161.12 (1.74)	-2.00 (0.12)
	sa	-176.06 (0.63)	-0.58 (0.05)	-177.34 (1.00)	-0.53 (0.11)	-175.13 (0.63)	-0.55 (0.03)	-161.91 (2.01)	-2.02 (0.13)
	db	-161.76 (1.11)	-0.05 (0.09)	-161.20 (1.91)	-0.21 (0.21)	-161.40 (0.34)	-0.24 (0.02)	-153.25 (1.80)	-0.98 (0.12)
	to	-172.45 (0.60)	-0.59 (0.05)	-173.68 (0.79)	-0.57 (0.09)	-172.39 (0.41)	-0.56 (0.02)	-158.48 (1.84)	-2.01 (0.12)
Constant voltage	**ma**	-219.17 (1.38)	-0.24 (0.12)	-219.94 (0.69)	-0.38 (0.08)	-220.13 (1.70)	0.08 (0.08)	-204.45 (2.64)	-1.69 (0.18)
	me	-202.52 (0.61)	-0.63 (0.05)	-204.06 (0.60)	-0.48 (0.07)	-204.77 (1.09)	-0.44 (0.05)	-188.37 (1.55)	-2.00 (0.10)
	ms	-180.14 (0.60)	-0.73 (0.05)	-182.38 (0.56)	-0.46 (0.06)	-181.71 (0.18)	-0.54 (0.01)	-167.16 (1.67)	-1.98 (0.11)
	sa	-181.24 (0.66)	-0.72 (0.06)	-183.59 (0.97)	-0.39 (0.11)	-181.24 (0.52)	-0.53 (0.02)	-167.96 (1.93)	-1.99 (0.13)
	db	-166.67 (1.05)	-0.20 (0.09)	-167.25 (1.79)	-0.06 (0.20)	-167.15 (0.28)	-0.21 (0.01)	-158.95 (1.83)	-0.98 (0.12)
	to	-177.63 (0.63)	-0.73 (0.05)	-179.93 (0.76)	-0.43 (0.08)	-178.44 (0.33)	-0.53 (0.02)	-164.52 (1.77)	-1.98 (0.12)
Constant current	**ma**	-218.30 (1.34)	0.05 (0.11)	-216.89 (0.73)	-0.66 (0.08)	-217.92 (1.70)	0.08 (0.08)	-202.24 (2.64)	-1.69 (0.18)
	me	-201.65 (0.55)	-0.34 (0.05)	-201.01 (0.66)	-0.76 (0.07)	-202.56 (1.09)	-0.44 (0.05)	-186.16 (1.55)	-2.00 (0.10)
	ms	-179.27 (0.53)	-0.45 (0.05)	-179.33 (0.61)	-0.74 (0.07)	-179.48 (0.18)	-0.55 (0.01)	-164.91 (1.69)	-1.98 (0.11)
	sa	-180.36 (0.60)	-0.44 (0.05)	-180.55 (1.02)	-0.67 (0.11)	-178.98 (0.54)	-0.53 (0.03)	-165.70 (1.95)	-2.00 (0.13)
	db	-165.83 (1.07)	0.08 (0.09)	-164.26 (1.82)	-0.33 (0.20)	-164.96 (0.29)	-0.22 (0.01)	-156.74 (1.82)	-0.98 (0.12)
	to	-176.76 (0.56)	-0.44 (0.05)	-176.89 (0.81)	-0.71 (0.09)	-176.19 (0.34)	-0.54 (0.02)	-162.26 (1.79)	-1.99 (0.12)

Al-Si CPW fabrication

Good fabrication

1. Wafer cleaning

1.1 Organic contaminants removal

$3:1\ H_2SO_4:H_2O_2$ mixture, 10 min., 95 °C (rinse with ultra-pure water)

1.2 Particles removal

$1:1:5\ NH_4OH:H_2O_2:H_2O$ mixture, 10 min., 70 °C (rinse with ultra-pure water)

1.3 Surface oxide removal and hydrogen passivation

$2:3\ HF:H_2O$ mixture, 30 s, room temperature

1.4 Inspection

Check for particles by using inspection light

2. Al deposition

2.1 Al sputtering ($100\ nm$)

LLS, pressure 5 mTorr, power 876 W, Base pressure $< 5 \cdot 10^{-6}$mbar, substrate rotation: oscillating drum

2.2 Inspection

By naked eye to check the deposited layer for stains, scratches, other particles or defects

3. Photolithography: Al layer patterning

3.1 De-hydration bake

120 s, 110°C

3.2 Resist coating

AZ6612/AZ6632 for 30 s at 4000 rpm, then soft bake on hotplate for 120 ± 10 s at 110 ± 5 °C.

3.3 HMDS vapor on Mask

Place mask in vapours of heated beaker containing HDMS for a few minutes

3.4 Pattern exposure

$5\ \mathrm{s}\ 15\ \mathrm{mW/cm^2}$, wait $10\ \mathrm{s}$, $5\ \mathrm{s}\ 15\ \mathrm{mW/cm^2}$, wait $10\ \mathrm{s}, 5\ \mathrm{s}\ 15\ \mathrm{mW/cm^2}$

3.5 *Pattern development*

$1:1$ AZ developer: H_2O mixture, $50\ \mathrm{s}$, $95\ ^\circ\mathrm{C}$

3.6 Inspection

With an optical microscope, check alignment and pattern definition and if necessary make pictures of at least five locations at top, center, bottom, left and right.

3.7 Hard bake / reflow bake

$75\ \mathrm{s}$, $125^\circ\mathrm{C}$

4. Al wet etching

4.1 *Oxygen plasma cleaning*

O_2 etch, $15\ \mathrm{s}$, $100\ \mathrm{sccm}$ flow, pressure $100\ \mathrm{mTorr}$, power $50\ \mathrm{W}$, bias $260\ \mathrm{V}$

4.2 *Al etching*

$16:1:1:2$ $H_3PO_4:CH_3COOH:HNO_3:H_2O$ mixture, $29\ ^\circ\mathrm{C}$. Target etch depth is $100\ \mathrm{nm}$.

4.3 *Inspection*

With an optical microscope, check at least locations at top, center, bottom, left and right and if necessary make pictures. Then using a probe station, measure Ohmic resistance from bondpad to ground for all chips. Values should be OL. Check for shorted transmission lines.

4.4 *Resist removal*

Spin wafer at $4000\ \mathrm{rpm}$ for 30 s, then spray acetone for 20 s, spin until dry.

4.5 *Inspection*

With an optical microscope, check If residue is visible. If so, use an O2 plasma cleaning step, similar to step 4.1 ($30-60\ \mathrm{s}$). Check and make pictures of at least five locations at top, center, bottom, left and right. Check Al resolution grids for rough estimate of the overetch. Then using a Dektak profilometer, measure Al thickness over antenna at 5 locations top, center, bottom, left and right and/or measure witness sample.

5. Dicing

5.1 Resist coating

$\mathrm{AZ6612/AZ6632}$ for $30\ \mathrm{s}$ at $4000\ \mathrm{rpm}$, then soft bake on hotplate for $50 \pm 10\ \ \mathrm{s}$ at $110 \pm 5\ {}^{\circ}\mathrm{C}$.

5.2 Dicing

Dice using Disco DAD 3310.

5.3 Inspection

With an optical or stereo microscope, check if chips are damaged due to dicing, check for scratches in transmission line (low magnification) and estimate which chips may be problematic and which should work.

Imperfect fabrication

The procedure is very similar as in the good fabrication, with the exception of the cleaning step.

$< 100 >$ Si wafer ($375\ \mu\mathrm{m}$ thick, $100\ \mathrm{mm}$ diameter) with Resistivity: $> 10000\ \Omega\mathrm{cm}$ and with Resistivity: $< 10000\ \Omega\mathrm{cm}$

1. **Wafer cleaning**

1.1 *Organic contaminants removal*

Aceton, $> 30\ \mathrm{s}$, room temperature, IPA, $> 20\ \mathrm{s}$, room temperature (rinse with ultra-pure water)

1.2 *Inspection*

Check for particles by using inspection light

1.3 *Surface oxide removal and hydrogen passivation*

$5\ \%$ or $10\ \%\ \ \mathrm{HF{:}H_2O}$ mixture, $90\ \mathrm{s}$, room temperature (rinse with ultra-pure water)

1.4 *Inspection*

Check for particles by using inspection light

2. **Al deposition**

2.1 *Al sputtering ($100\ nm$)*

LLS, pressure $5\ \mathrm{mTorr}$, substrate rotation: shuttle

3. **Photolithography: Al layer patterning**

3.1 De-hydration bake

$120\ \mathrm{s}$, $110℃$

3.2 Resist coating

$\mathrm{AZ6612}$ for $30\,\mathrm{s}$ at $4000\,\mathrm{rpm}$, then soft bake on hotplate for 60 ± 10 s at 110 ± 5 ℃.

3.3 Pattern exposure

2.6 s $16.7\ \mathrm{mW/cm^2}$, wait, 2.6 s $16.7\ \mathrm{mW/cm^2}$, wait, 2.6 s $16.7\ \mathrm{mW/cm^2}$

3.4 Pattern development

$1:1$ AZ developer: H_2O mixture, $40 - 45$ s (rinse with ultra-pure water, spin dry)

3.5 Inspection

With an optical microscope with IM filter, check alignment and pattern definition and if necessary make pictures of at least five locations at top, center, bottom, left and right.

3.6 Hard bake / reflow bake

75 s, $125℃$

4. Al wet etching

4.1 Oxygen plasma cleaning

O_2 etch, 15 s, 100 sccm flow, pressure $100\ \mathrm{mTorr}$, power 50 W, bias 260 V

4.2 Al etching

$16:1:1:2$ $H_3PO_4:CH_3COOH:HNO_3:H_2O$ mixture, 160 s, 29 ℃. Target etch depth is $100\ \mathrm{nm}$ (rinse with ultra-pure water, blow dry with N_2)

4.3 Inspection

With an optical microscope, check at least locations at top, center, bottom, left and right and if necessary make pictures.

4.4 Resist removal

Rinse with aceton, > 30 s, rinse with IPA, > 20 s.

4.5 Inspection

With a Dektak profilometer, measure Al thickness over antenna at 5 locations top, center, bottom, left and right and/or measure witness sample.

5. Dicing

5.1 Resist coating

$\mathrm{AZ6612/AZ6632}$ for $30\ \mathrm{s}$ at $4000\ \mathrm{rpm}$, then soft bake on hotplate for $50 \pm 10\ \ \mathrm{s}$ at $110 \pm 5\ ℃$.

5.2 Dicing

Dice using Disco DAD 3310.

5.3 Inspection

With an optical or stereo microscope, check if chips are damaged due to dicing, check for scratches in transmission line (low magnification) and estimate which chips may be problematic and which should work.

Al-SiN-Si CPW fabrication

The procedure for this chip is almost identical to that of the Al-SiN microstrip, with the exclusion of the RIE and KOH etching of the backside of the wafer and the subsequent Al sputtering on the back side.

Al-SiN CPW fabrication

The procedure for this chip is almost identical to that of the Al-SiN microstrip, with the exclusion of the Al sputtering on the back side of the wafer.

Al-SiN microstrip fabrication

Good fabrication

$< 100 >$ Si wafer ($375\ \mu\mathrm{m}$ thick, $100\ \mathrm{mm}$ diameter) with $1000\,\mathrm{nm}$ nitride with Resistivity: $> 10000\ \Omega\mathrm{cm}$

1. **<u>Wafer cleaning</u>**

1.1 Organic contaminants removal

Aceton, 300 s, room temperature

1.2 Inspection

Check for particles and stains by using inspection light and / or optical microsope

2. Photolithography: Al layer patterning

2.1 Resist coating (front side)

AZ6632 for 30 s at 4000 rpm, then soft bake on hotplate for 120 ± 10 s at 110 ± 5 °C.

2.2 Oxygen plasma cleaning (back side)

O_2 etch, $120 - 300$ s, 100 sccm flow, pressure 100 mTorr, power 100 W, bias 260 V

2.3 HMDS vapor on wafer (back side)

Place wafer in vapours of heated beaker containing HDMS for a few minutes

2.4 Resist coating (back side)

AZ6632 for 30 s at 4000 rpm, then soft bake on hotplate for 120 ± 10 s at 110 ± 5 °C.

2.5 Pattern exposure

5 s 15 mW/cm^2, wait 10 s, 5 s 15 mW/cm^2, wait 10 s, 5 s 15 mW/cm^2

2.6 Pattern development

5: 1 AZ developer: H_2O mixture, 60 s (rinse with ultra-pure water, spin dry)

2.7 Inspection

With an optical microscope, check alignment and pattern definition and if necessary make pictures of at least five locations at top, center, bottom, left and right.

2.8 Pattern exposure to harden resist (not using a mask)

15 s 15 mW/cm^2

2.9 Hard bake / reflow bake

75 s, 125°C

3. RIE etching of SiN layer (back side)

3.1 SiN layer etching

~35 min. for 1000 nm etch

3.2 Inspection

With a Dektak profilometer, check complete etch of SiN.

3.3 Resist removal

Spin wafer at 4000 rpm for 30 s, then spray acetone for 20 s, spin until dry.

3.4 Inspection

With a Dektak profilometer, measure etch depth at 5 locations top, center, bottom, left and right.

3.5 Cleaning

Acetone bath for 2 min., spray with clean acetone, rinse in IPA and spin dry.

4. **KOH etching (back side)**

4.1 KOH etching

25 % solution with 1000 g : 3 l $\mathrm{KOH:H_2O}$ at 75°C, etch until no bubbles are visible (then rinse in ultra-pure water).

4.2 Ionic contaminants removal

$1:1:5$ $\mathrm{HCl:H_2O_2:DI}$ mixture, 10 min., 95 °C (rinse in ultra-pure water).

4.3 Inspection

Check for particles.

5. **Wafer cleaning**

5.1 Organic contaminants removal

$3:1$ $\mathrm{H_2SO_4:H_2O_2}$ mixture, 10 min., 95 °C (rinse with ultra-pure water)

5.2 Particles removal

$1:1:5$ $\mathrm{NH_4OH:H_2O_2:H_2O}$ mixture, 10 min., 70 °C (rinse with ultra-pure water)

5.3 Surface oxide removal and hydrogen passivation

10 % $\mathrm{HF:H_2O}$ mixture, 10 s, room temperature (rinse with ultra-pure water)

6. **Al deposition (front side and back side)**

6.1 Al sputtering (100 nm)

LLS, pressure 5 mTorr, power 876 W, Base pressure $< 5 \cdot 10^{-6}$mbar, substrate rotation: oscillating drum

6.2 Inspection

By naked eye to check the deposited layer for stains, scratches, other particles or defects

7. Resist protection (back side)

7.1 Resist coating (back side)

$\mathrm{AZ6632}$ for $30\,\mathrm{s}$ at $4000\,\mathrm{rpm}$, then soft bake on hotplate for 120 ± 10 s at 110 ± 5 ℃.

7.2 Flood exposure

15 s at $15\ \mathrm{mW/cm^2}$

7.3 Pattern development

$1:1\ \ \mathrm{AZ\ developer: H_2O}$ mixture, 60 s (rinse with ultra-pure water, spin dry)

7.4 Inspection

With an optical microscope, check for resist residues.

8. Photolithography: Al layer patterning (front side)

8.1 De-hydration bake

120 s, 110℃

8.2 Resist coating

$\mathrm{AZ6612}$ for $30\,\mathrm{s}$ at $4000\,\mathrm{rpm}$, then soft bake on hotplate for 60 ± 10 s at 110 ± 5 ℃ (rinse with ultra-pure water, spin dry).

8.3 HMDS vapor on mask

Place mask in vapours of heated beaker containing HDMS for a few minutes

8.4 Pattern exposure

6 s at $15\ \mathrm{mW/cm^2}$

8.5 Pattern development

$1:1\ \ \mathrm{AZ\ developer: H_2O}$ mixture, 42 s (rinse with ultra-pure water, spin dry)

8.6 Inspection

With an optical microscope, check alignment and pattern definition and if necessary make pictures of at least five locations at top, center, bottom, left and right.

8.7 Hard bake / reflow bake

$75\ \mathrm{s}, 125°\mathrm{C}$

9. **Al wet etching**

9.1 Oxygen plasma cleaning

$\mathrm{O_2}$ etch, $30\ \mathrm{s}$, 100 sccm flow, pressure $100\ \mathrm{mTorr}$, power $50\ \mathrm{W}$, bias $260\ \mathrm{V}$

9.2 Al etching

Commercial etchant mixture, $153\ \mathrm{s}$, $29\ °\mathrm{C}$. Target etch depth is $100\ \mathrm{nm}$ (rinse with ultra-pure water, spin dry)

9.3 Inspection

With an optical microscope, check at least locations at top, center, bottom, left and right and if necessary make pictures. Then using a probe station, measure Ohmic resistance from bondpad to ground for all chips. Values should be OL. Check for shorted transmission lines.

9.4 Resist removal

Rinse with aceton, rinse with IPA. Spin dry.

9.5 Inspection

With an optical microscope, check Al resolution grids to get rough estimate on overetch. Check and make pictures of at least five locations at top, center, bottom, left and right With a Dektak profilometer, measure Al thickness over antenna at 5 locations top, center, bottom, left and right and/or measure witness sample.

10. **Dicing**

10.1 Resist coating

$\mathrm{AZ6612/AZ6632}$ for $30\ \mathrm{s}$ at $4000\ \mathrm{rpm}$, then soft bake on hotplate for $50 \pm 10\ \ \mathrm{s}$ at $110 \pm 5\ °\mathrm{C}$.

10.2 Dicing

Dice using Disco DAD 3310.

Imperfect fabrication

$< 100 >$ Si wafer ($375\ \mu\mathrm{m}$ thick, $100\ \mathrm{mm}$ diameter) with $1000\ \mathrm{nm}$ nitride with Resistivity: $> 10000\ \Omega\mathrm{cm}$

1. Wafer cleaning

1.1 Organic contaminants removal

Aceton, > 30 s, room temperature, IPA, > 20 s, room temperature (rinse with ultra pure water)

1.2 Inspection

Check for particles by using inspection light

2. Photolithography: Al layer patterning

2.1 Resist coating (front side)

$\mathrm{AZ6612}$ for $30\,\mathrm{s}$ at $4000\,\mathrm{rpm}$, then soft bake on hotplate for 60 ± 10 s at 110 ± 3 °C.

2.2 HMDS vapor on wafer (back side)

Place wafer in vapours of heated beaker containing HDMS for a few minutes

2.3 Resist coating (back side)

$\mathrm{AZ6612}$ for $30\,\mathrm{s}$ at $4000\,\mathrm{rpm}$, then soft bake on hotplate for 90 ± 10 s at 110 ± 3 °C.

2.4 Pattern exposure

$130\ \mathrm{mJ/cm^2}$

2.5 Pattern development

$5:1$ AZ developer: $\mathrm{H_2O}$ mixture, $35 - 40$ s (rinse with ultra-pure water, blow dry with $\mathrm{N_2}$)

2.6 Inspection

With an optical microscope, check alignment and pattern definition and if necessary make pictures of at least five locations at top, center, bottom, left and right.

2.7 Pattern flood exposure to harden resist (not using a mask)

$150\ \mathrm{mJ/cm^2}$

2.8 RIE of SiN (Target etch depth is $100\ nm$)

15 min. at 150 W, after that continue while checking every 2 min. with microscope if etch is 1000 nm.

3. KOH etching (back side)

3.1 KOH etching

25 % solution with $1000\ \mathrm{g} : 3\ \mathrm{l}\ \mathrm{KOH}:\mathrm{H_2O}$ at 85℃, etch 15 min. (then rinse in ultra-pure water, blow dry with N_2).

3.2 Ionic contaminants removal

$1:1:5$ $\mathrm{HCl}:\mathrm{H_2O_2}:\mathrm{DI}$ mixture, 10 min., 95 ℃ (rinse in ultra-pure water).

3.3 Inspection

Check for particles.

4. Etching of SiN-Si (back side)

4.1 Resist coating (front side)

AZ6612 for 30 s at 4000 rpm, then soft bake on hotplate for 60 ± 10 s at 110 ± 5 ℃.

4.2 HMDS vapor on wafer (back side)

Place wafer in vapours of heated beaker containing HDMS for a few minutes

4.3 Resist coating (back side)

AZ6612 for 30 s at 4000 rpm, then soft bake on hotplate for 90 ± 10 s at 110 ± 3 ℃.

4.4 Clean mask

Aceton or $3:1$ $\mathrm{H_2SO_4}:\mathrm{H_2O_2}$ mixture.

4.5 Pattern exposure

$130\ \mathrm{mJ/cm^2}$

4.6 Pattern development

$5:1$ AZ developer: $\mathrm{H_2O}$ mixture, $35 - 40$ s (rinse with ultra-pure water, blow dry with N_2)

4.7 Inspection

With an optical microscope, check for spots, sharp lines and pattern definition.

4.8 Pattern flood exposure to harden resist (not using a mask)

$150\ \mathrm{mJ/cm^2}$

4.9 RIE of SiN (Target etch depth is $100\ nm$)

At $150\ \mathrm{W}$, etch rate of $60 - 70\ \mathrm{nm/min}$. Make patterns in centre of the mask for end point detection.

4.10 Resist removal

Rinse with aceton (rinse with ultra-pure water), dry.

4.11 KOH etching of Si

$25\ \%$ solution with $1000\ \mathrm{g} : 3\ \mathrm{l}\ \mathrm{KOH}{:}\ \mathrm{H_2O}$ at $85\mathrm{°C}$, etch $\sim 3\ \mathrm{h}$. for $400\ \mathrm{\mu m}$, check etch rate every hour. Then rinse in ultra-pure water, blow dry with $\mathrm{N_2}$.

5. Wafer cleaning

5.1 Organic contaminants removal

Aceton, $> 30\ \mathrm{s}$, room temperature, IPA, $> 20\ \mathrm{s}$, room temperature (rinse with ultra pure water)

5.2 Surface oxide removal and hydrogen passivation

$5\ \%\ \mathrm{HF}{:}\ \mathrm{H_2O}$ mixture, $10\ \mathrm{s}$, room temperature (rinse with ultra-pure water)

5.3 Inspection

Check for particles by using inspection light

6. Al deposition (front side and back side)

6.1 Al sputtering ($100\ nm$)

LLS, pressure $5\ \mathrm{mTorr}$, substrate rotation: shuttle

7. Resist protection (back side)

7.1 Resist coating (back side)

$\mathrm{AZ6632}$ for $30\ \mathrm{s}$ at $4000\ \mathrm{rpm}$, then soft bake on hotplate for $120 \pm 10\ \mathrm{s}$ at $110 \pm 5\ \mathrm{°C}$.

8. Photolithography: Al layer patterning (front side)

8.1 HMDS vapor on wafer

Place wafer in vapours of heated beaker containing HDMS for $15\ \mathrm{s}$

8.2 Resist coating

$\mathrm{AZ6612}$ for $30\ \mathrm{s}$ at $4000\ \mathrm{rpm}$, then soft bake on hotplate for $60 \pm 10\ \mathrm{s}$ at $110 \pm 5\ \mathrm{°C}$ (rinse with ultra-pure water, spin dry).

8.3 Pattern exposure

$2.6\ \mathrm{s}\ 16.7\ \mathrm{mW/cm^2}$, wait, $2.6\ \mathrm{s}\ 16.7\ \mathrm{mW/cm^2}$, wait, $2.6\ \mathrm{s}\ 16.7\ \mathrm{mW/cm^2}$

8.4 Pattern development

$1:1$ AZ developer: H_2O mixture, $40 - 45\ \mathrm{s}$ (rinse with ultra-pure water, spin dry)

8.5 Inspection

With an optical microscope with IM filter, check alignment and pattern definition and if necessary make pictures of at least five locations at top, center, bottom, left and right.

8.6 Hard bake / reflow bake

$75\ \mathrm{s}$, $125°\mathrm{C}$

8.7 Resist removal

RIE etch, $30\ \mathrm{s}$

8.8 Al etching

Commercial etchant mixture ($16:1:2:1$ $H_3PO_4:CH_3COOH:HNO_3:H_2O$), $165\ \mathrm{s}$, room temperature. Target etch depth is $100\ \mathrm{nm}$ (rinse with ultra-pure water, blow dry).

8.9 Inspection

With an optical microscope, check if Al has been etched away completely.

8.10 Resist removal

Rinse with aceton $> 30\ \mathrm{s}$, rinse with IPA $> 20\ \mathrm{s}$.

8.11 Inspection

With a Dektak profilometer, measure Al thickness over antenna at 5 locations top, center, bottom, left and right and/or measure witness sample.

9. Dicing

9.1 Resist coating

AZ6612/AZ6632 for $30\ \mathrm{s}$ at $4000\ \mathrm{rpm}$, then soft bake on hotplate for $50 \pm 10\ \mathrm{s}$ at $110 \pm 5\ °\mathrm{C}$.

9.2 Dicing

Dice using Disco DAD 3310.

Al-Si CPW (high resistivity)

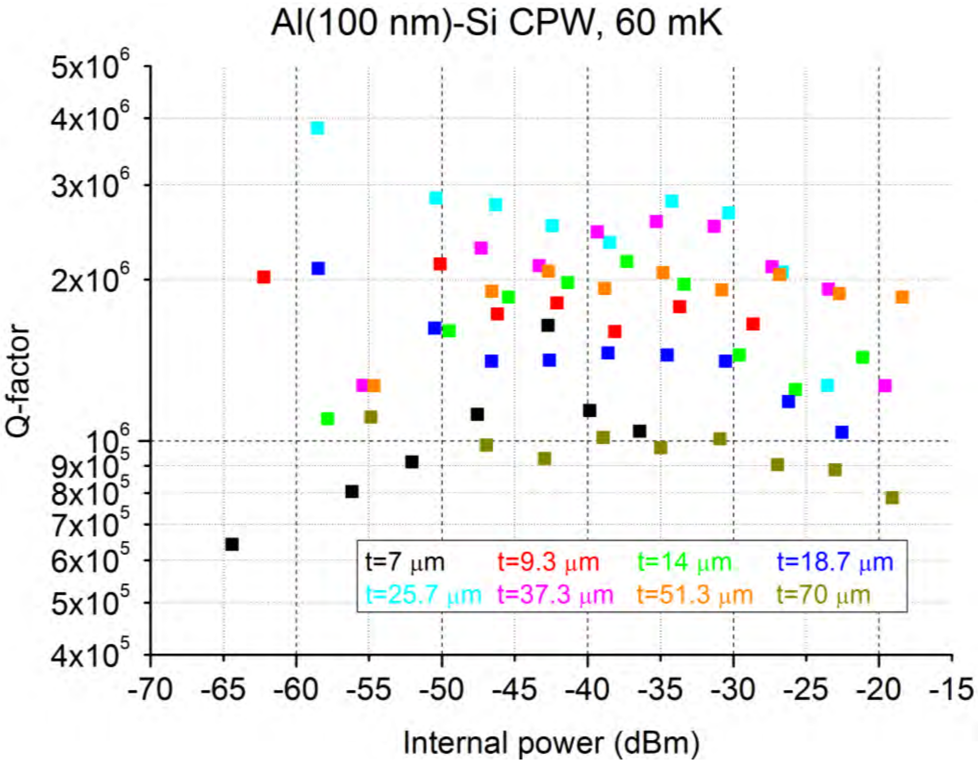

Figure 81 Internal quality factor versus internal power in dBm for the constant impedance Al-Si CPW resonator set with total width (in $\mu\mathrm{m}$) of 7 (black), 9.3 (red), 14 (green), 18.7 (dark blue), 25.7 (cyan), 37.3 (magenta), 51.3 (orange) and 70 (olive) at $60\ \mathrm{mK}$.

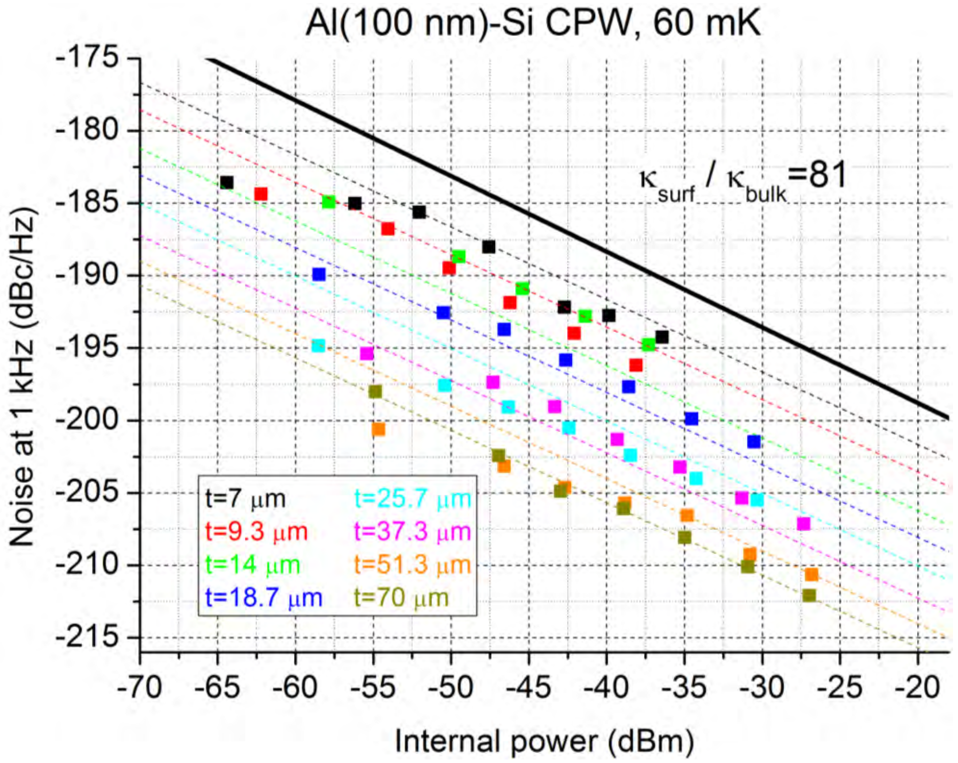

Figure 82 Noise measured at $1\ \mathrm{kHz}$ in $\mathrm{dBc/Hz}$ versus internal power in dBm for the constant impedance Al-Si CPW resonator set with total width (in $\mu\mathrm{m}$) of 7 (black), 9.3 (red), 14 (green), 18.7 (dark blue), 25.7 (cyan), 37.3 (magenta), 51.3 (orange) and 70 (olive) at $60\ \mathrm{mK}$. The black line indicates the noise of the $t = 7\ \mu\mathrm{m}$ Nb on Si CPW from [58]. The dashed lines represent the fit with the numerical data for the surface and dielectric bulk contributions, while the inset shows the ratio between their respective noise spectral coefficients.

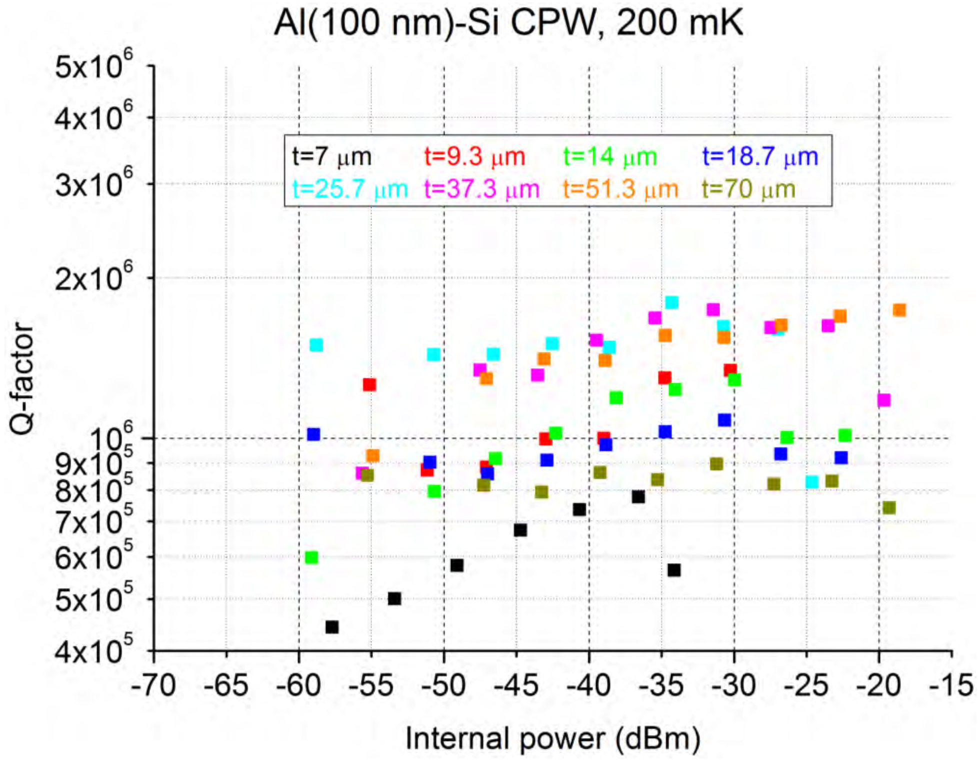

Figure 83 Internal quality factor versus internal power in dBm for the constant impedance Al-Si CPW resonator set with total width (in $\mu\mathrm{m}$) of 7 (black), 9.3 (red), 14 (green), 18.7 (dark blue), 25.7 (cyan), 37.3 (magenta), 51.3 (orange) and 70 (olive) at $200\ \mathrm{mK}$.

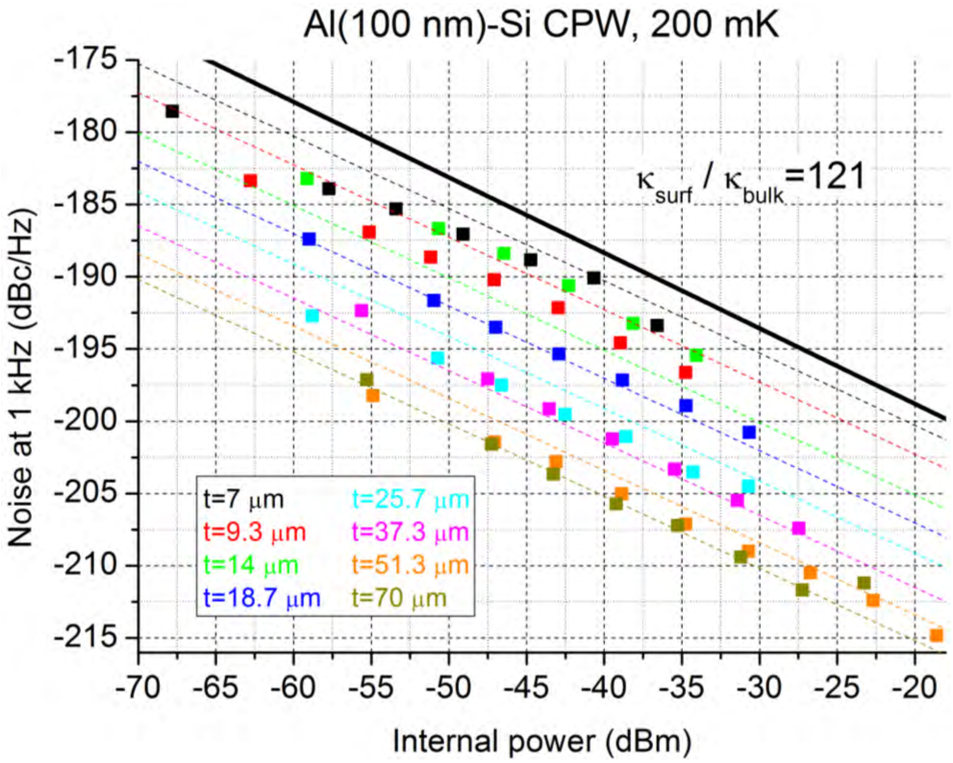

Figure 84 Noise measured at $1\ \mathrm{kHz}$ in $\mathrm{dBc/Hz}$ versus internal power in dBm for the constant impedance Al-Si CPW resonator set with total width (in $\mu\mathrm{m}$) of 7 (black), 9.3 (red), 14 (green), 18.7 (dark blue), 25.7 (cyan), 37.3 (magenta), 51.3 (orange) and 70 (olive) at $200\ \mathrm{mK}$. The black line indicates the noise of the $t = 7\ \mu\mathrm{m}$ Nb on Si CPW from [58]. The dashed lines represent the fit with the numerical data for the surface and dielectric bulk contributions, while the inset shows the ratio between their respective noise spectral coefficients.

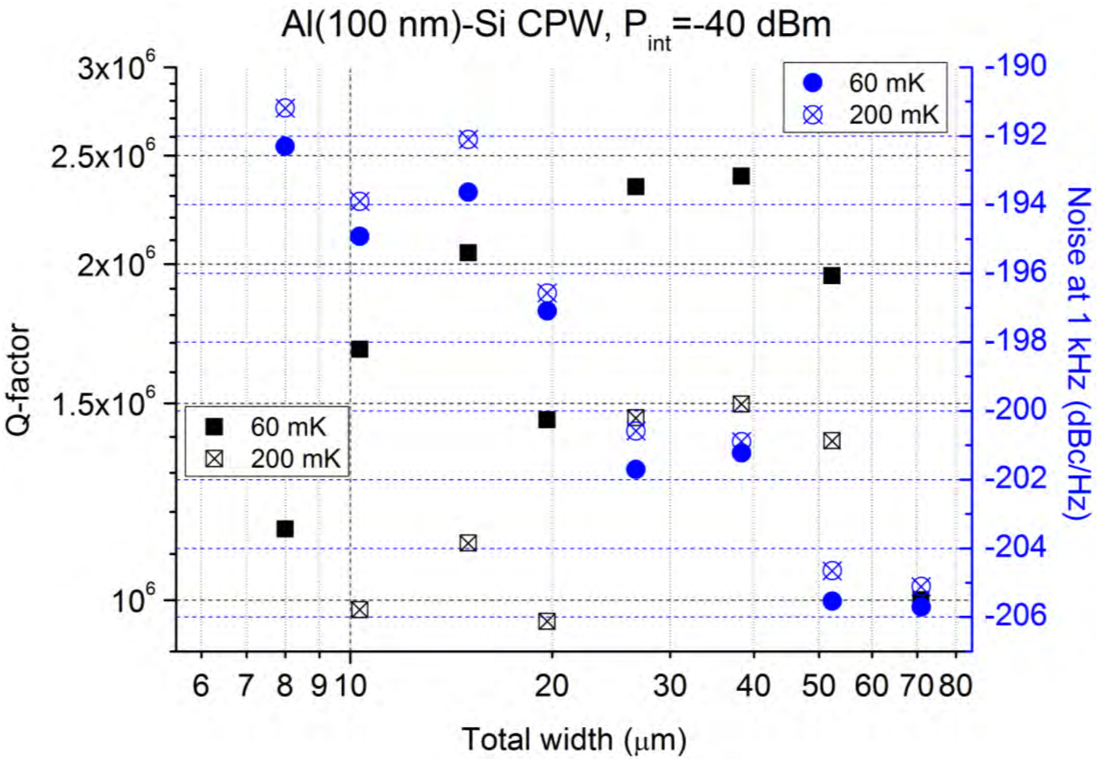

Figure 85 Dependency of Q-factor (black squares) and noise (blue circles) at $1\ \mathrm{kHz}$ in $\mathrm{dBc/Hz}$ versus on the total width in $\mu\mathrm{m}$ for the constant impedance Al-Si CPW resonator set at $P_{int} = -40\ \mathrm{dBm}$ for $T = 60$ (filled symbols) and $200\ \mathrm{mK}$ (symbols with cross).

Al-Si CPW (high resistivity, imperfect fabrication)

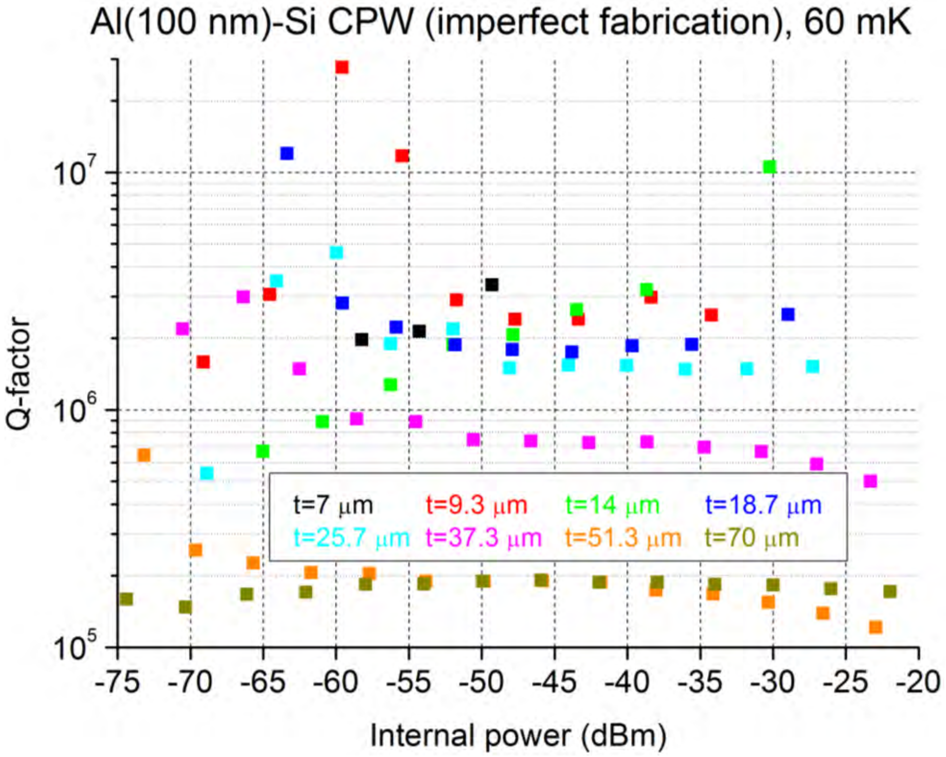

Figure 86 Internal quality factor versus internal power in dBm for the constant impedance Al-Si CPW resonator set with total width (in $\mu\mathrm{m}$) of 7 (black), 9.3 (red), 14 (green), 18.7 (dark blue), 25.7 (cyan), 37.3 (magenta), 51.3 (orange) and 70 (olive) at $60\ \mathrm{mK}$.

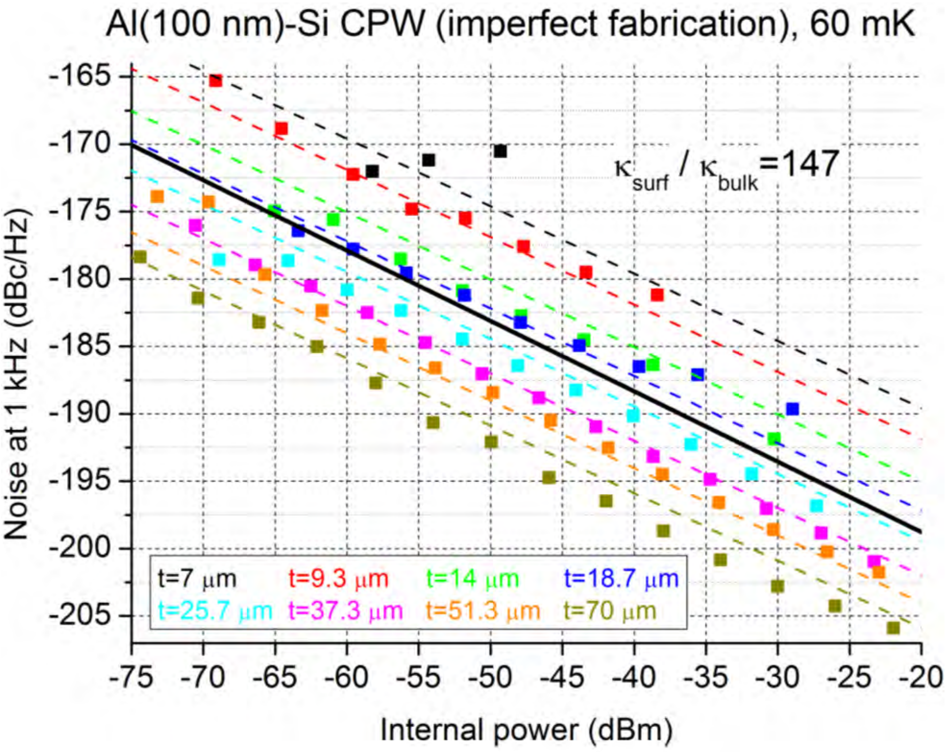

Figure 87 Noise measured at $1\ \mathrm{kHz}$ in $\mathrm{dBc/Hz}$ versus internal power in dBm for the constant impedance Al-Si CPW resonator set with total width (in $\mu\mathrm{m}$) of 7 (black), 9.3 (red), 14 (green), 18.7 (dark blue), 25.7 (cyan), 37.3 (magenta), 51.3 (orange) and 70 (olive) at $60\ \mathrm{mK}$. The black line indicates the noise of the $t = 7\ \mu\mathrm{m}$ Nb on Si CPW from [58]. The dashed lines represent the fit with the numerical data for the surface and dielectric bulk contributions, while the inset shows the ratio between their respective noise spectral coefficients.

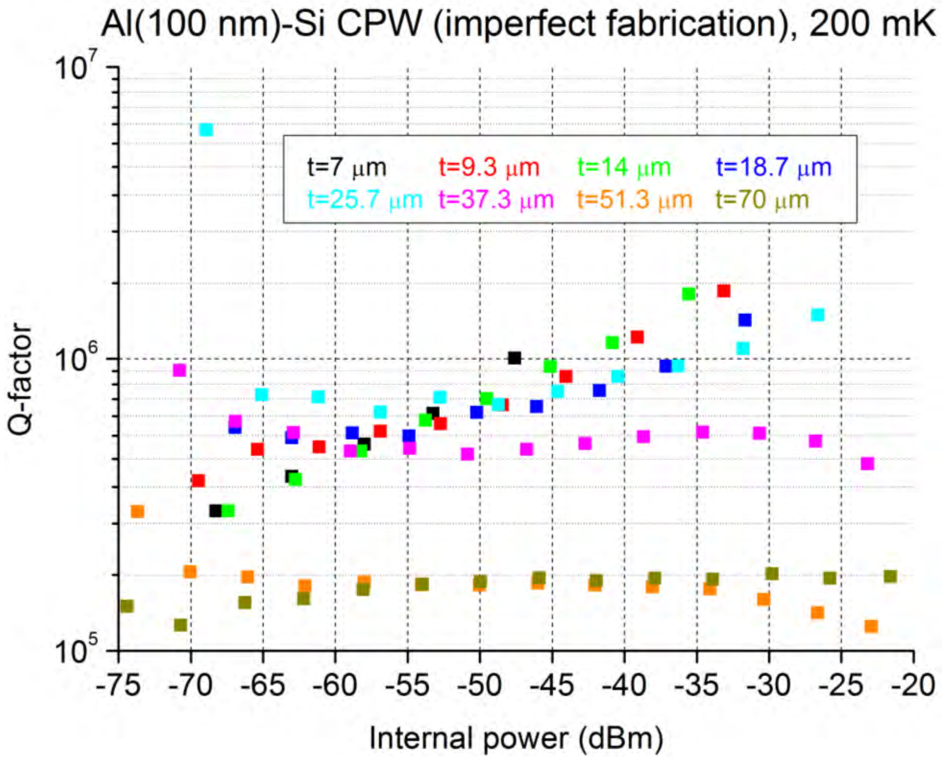

Figure 88 Internal quality factor versus internal power in dBm for the constant impedance Al-Si CPW resonator set with total width (in $\mu\mathrm{m}$) of 7 (black), 9.3 (red), 14 (green), 18.7 (dark blue), 25.7 (cyan), 37.3 (magenta), 51.3 (orange) and 70 (olive) at $200\ \mathrm{mK}$.

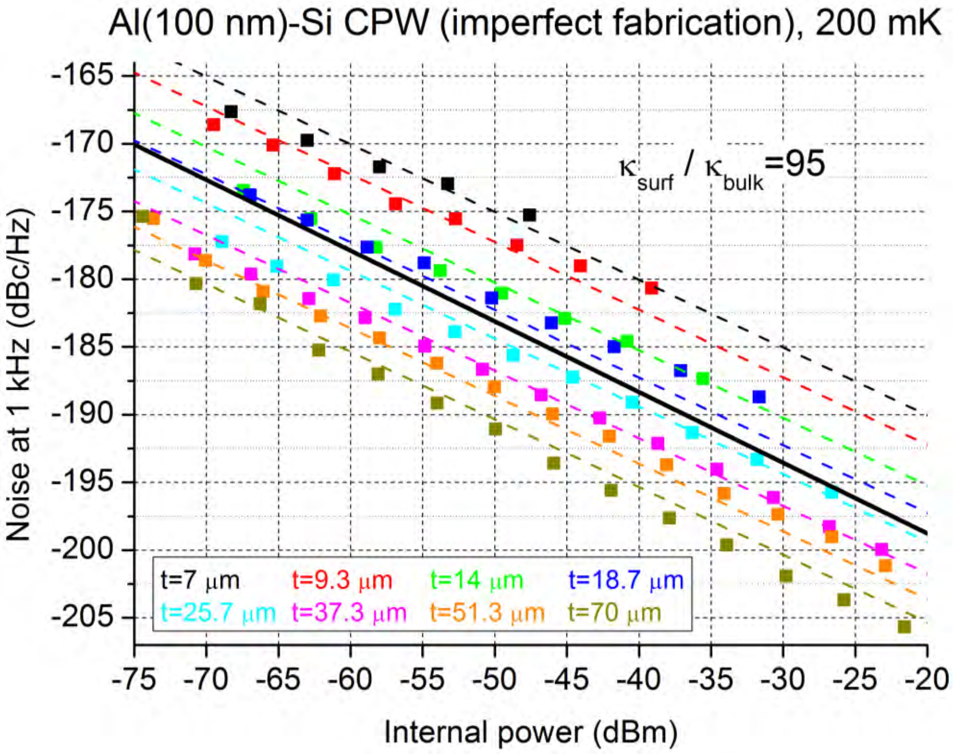

Figure 89 Noise measured at $1\,\mathrm{kHz}$ in $\mathrm{dBc/Hz}$ versus internal power in dBm for the constant impedance Al-Si CPW resonator set with total width (in $\mu\mathrm{m}$) of 7 (black), 9.3 (red), 14 (green), 18.7 (dark blue), 25.7 (cyan), 37.3 (magenta), 51.3 (orange) and 70 (olive) at $200\,\mathrm{mK}$. The black line indicates the noise of the $t = 7\,\mu\mathrm{m}$ Nb on Si CPW from [58]. The dashed lines represent the fit with the numerical data for the surface and dielectric bulk contributions, while the inset shows the ratio between their respective noise spectral coefficients.

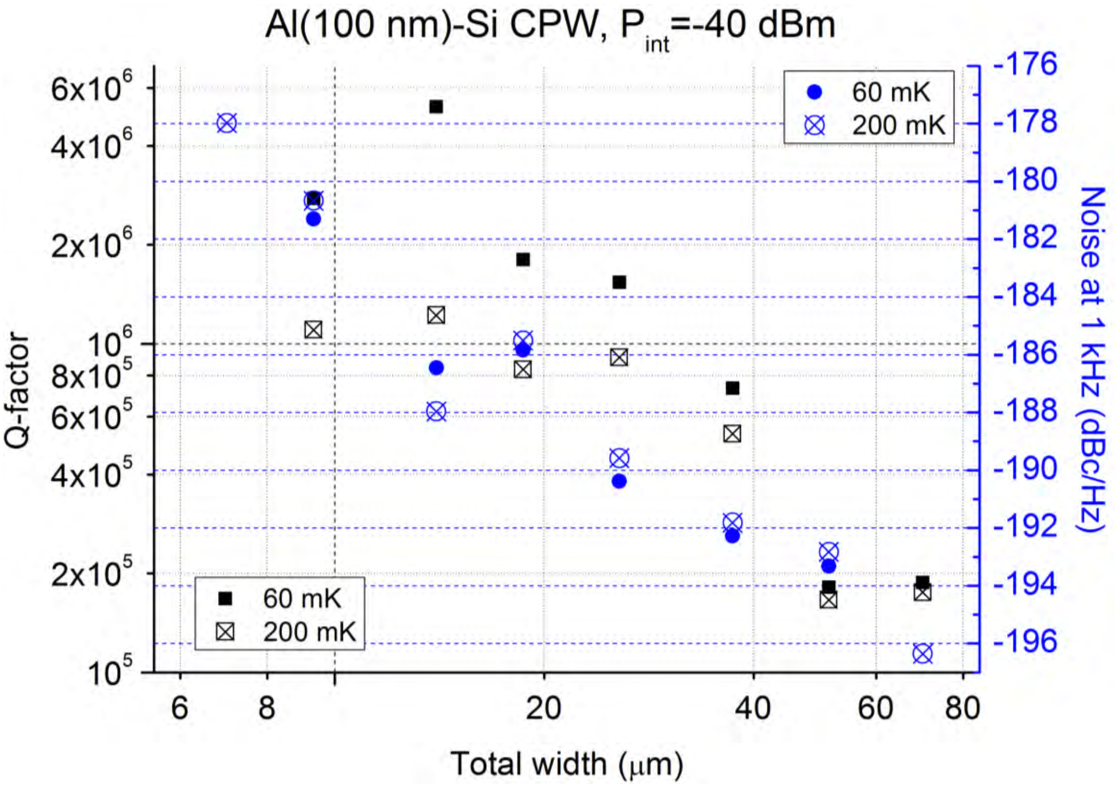

Figure 90 Dependency of Q-factor (black squares) and noise (blue circles) at $1\,\mathrm{kHz}$ in $\mathrm{dBc/Hz}$ versus on the total width in $\mu\mathrm{m}$ for the constant impedance Al-Si CPW resonator set at $P_{int} = -40\,\mathrm{dBm}$ for $T = 60$ (filled symbols) and $200\,\mathrm{mK}$ (symbols with cross).

Al-Si CPW (low resistivity)

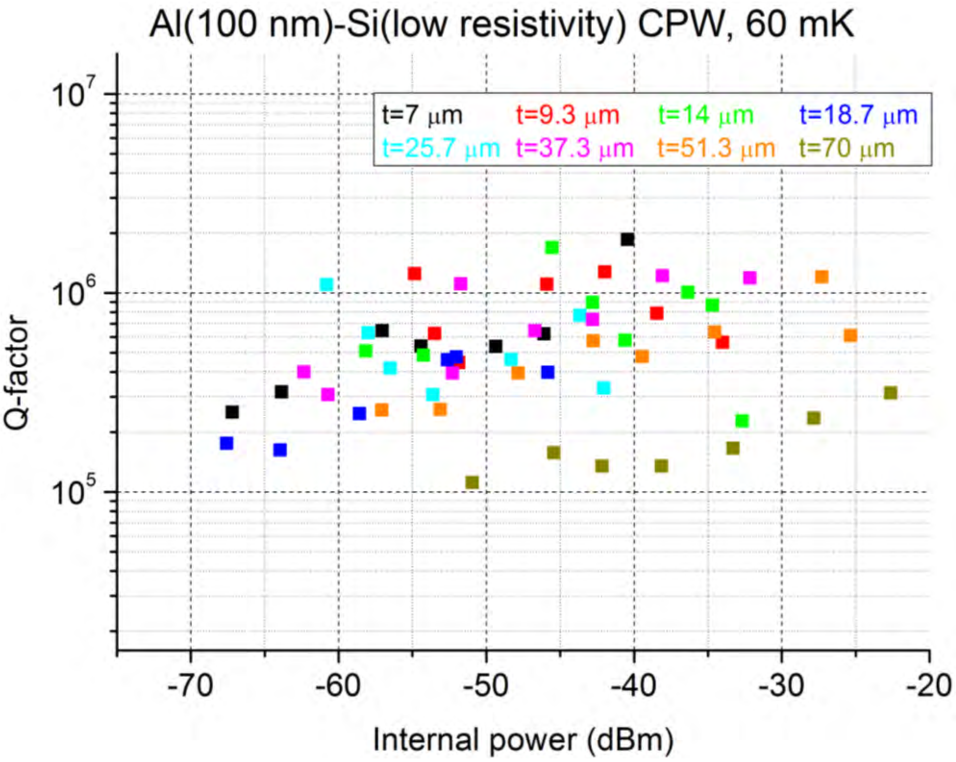

Figure 91 Internal quality factor versus internal power in dBm for the constant impedance Al-Si (low resistivity) CPW resonator set with total width (in $\mu\mathrm{m}$) of 7 (black), 9.3 (red), 14 (green), 18.7 (dark blue), 25.7 (cyan), 37.3 (magenta), 51.3 (orange) and 70 (olive) at $60\ \mathrm{mK}$.

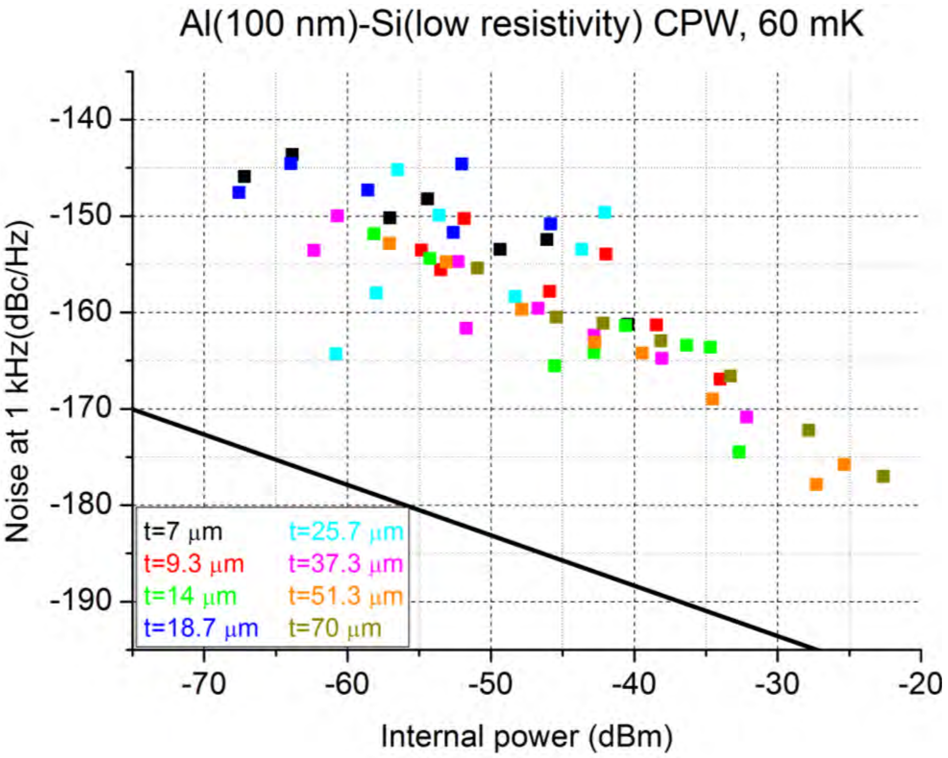

Figure 92 Noise measured at $1\ \mathrm{kHz}$ in $\mathrm{dBc/Hz}$ versus internal power in dBm for the constant impedance Al-Si (low resistivity) CPW resonator set with total width (in $\mu\mathrm{m}$) of 7 (black), 9.3 (red), 14 (green), 18.7 (dark blue), 25.7 (cyan), 37.3 (magenta), 51.3 (orange) and 70 (olive) at $60\ \mathrm{mK}$. The black line indicates the noise of the $t = 7\ \mu\mathrm{m}$ Nb on Si CPW from [58]. The dashed lines represent the fit with the numerical data for the surface and dielectric bulk contributions, while the inset shows the ratio between their respective noise spectral coefficients.

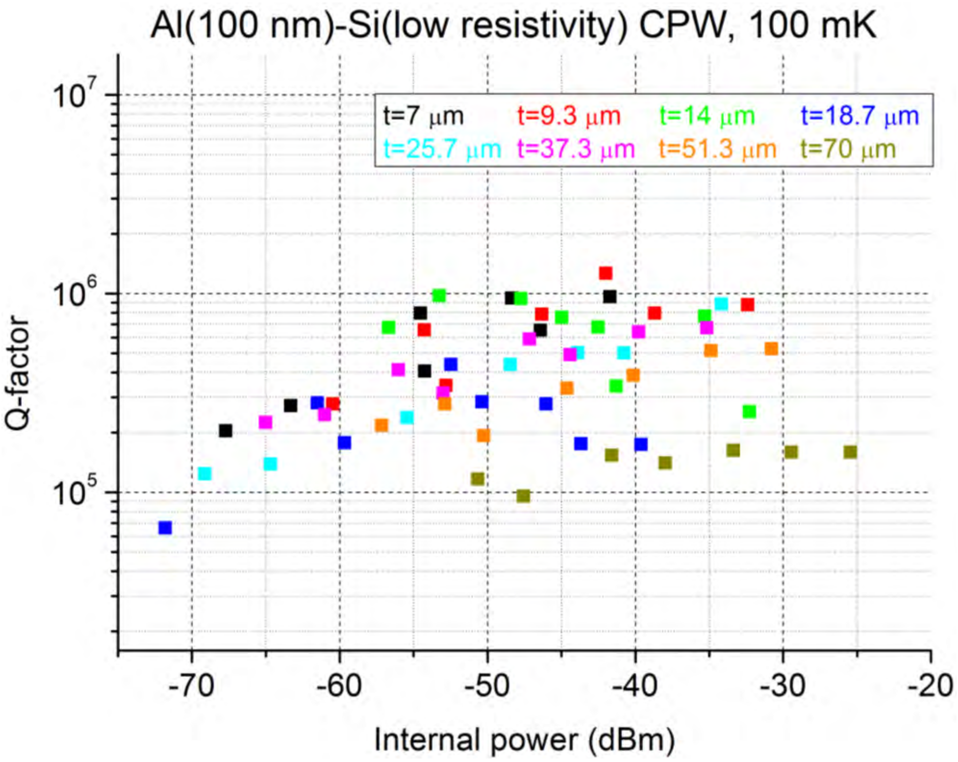

Figure 93 Internal quality factor versus internal power in dBm for the constant impedance Al-Si (low resistivity) CPW resonator set with total width (in $\mu\mathrm{m}$) of 7 (black), 9.3 (red), 14 (green), 18.7 (dark blue), 25.7 (cyan), 37.3 (magenta), 51.3 (orange) and 70 (olive) at $100\ \mathrm{mK}$.

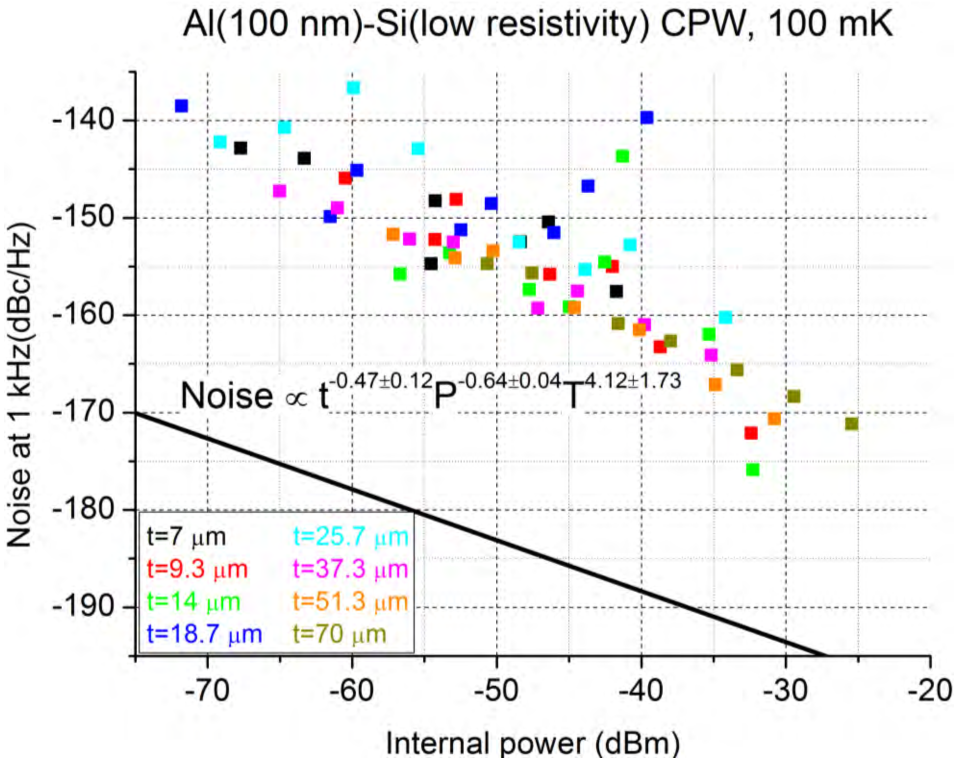

Figure 94 Noise measured at $1\ \mathrm{kHz}$ in $\mathrm{dBc/Hz}$ versus internal power in dBm for the constant impedance Al-Si (low resistivity) CPW resonator set with total width (in $\mu\mathrm{m}$) of 7 (black), 9.3 (red), 14 (green), 18.7 (dark blue), 25.7 (cyan), 37.3 (magenta), 51.3 (orange) and 70 (olive) at $100\ \mathrm{mK}$. The black line indicates the noise of the $t = 7\ \mu\mathrm{m}$ Nb on Si CPW from [58]. The dashed lines represent the fit with the numerical data for the surface and dielectric bulk contributions, while the inset shows the ratio between their respective noise spectral coefficients.

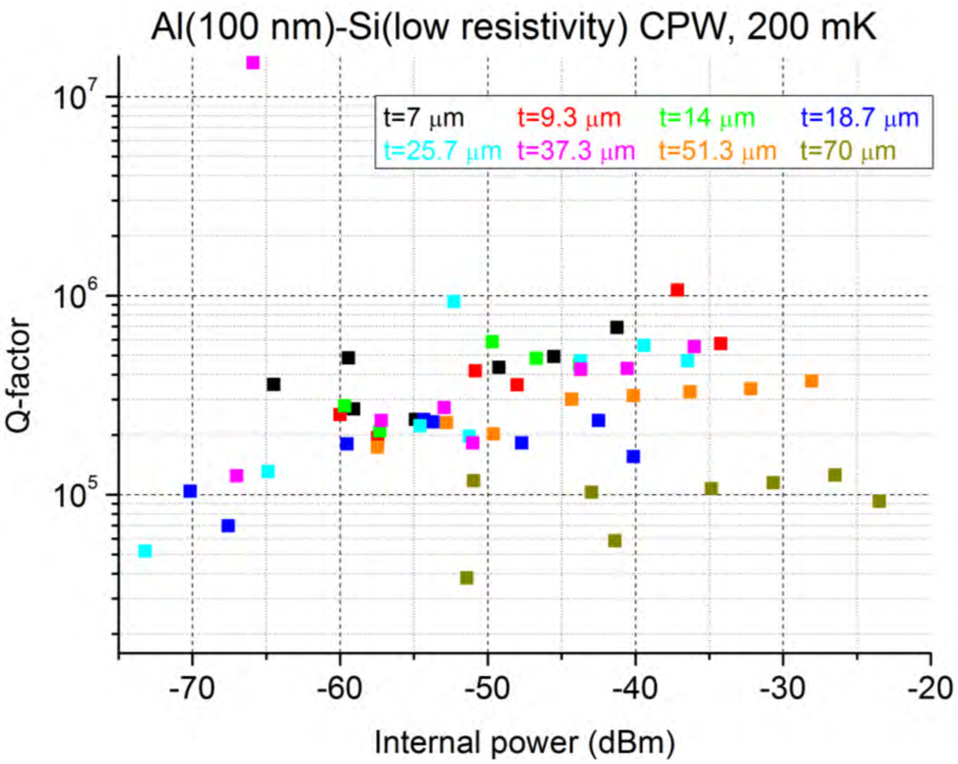

Figure 95 Internal quality factor versus internal power in dBm for the constant impedance Al-Si (low resistivity) CPW resonator set with total width (in $\mu\mathrm{m}$) of 7 (black), 9.3 (red), 14 (green), 18.7 (dark blue), 25.7 (cyan), 37.3 (magenta), 51.3 (orange) and 70 (olive) at $200\ \mathrm{mK}$.

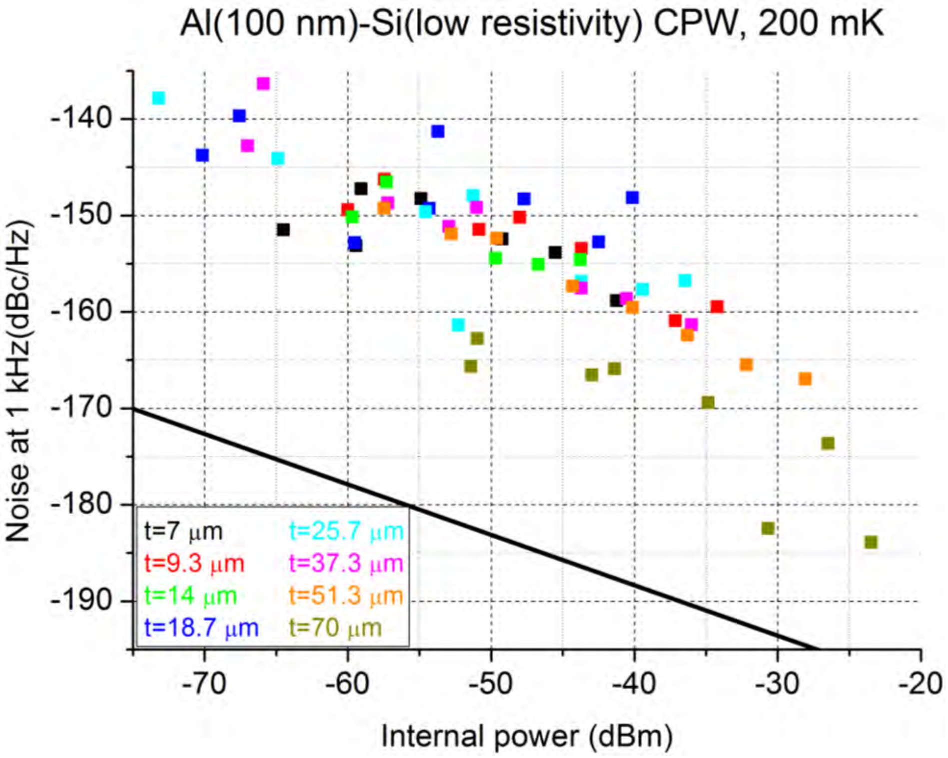

Figure 96 Noise measured at $1\ \mathrm{kHz}$ in $\mathrm{dBc/Hz}$ versus internal power in dBm for the constant impedance Al-Si (low resistivity) CPW resonator set with total width (in $\mu\mathrm{m}$) of 7 (black), 9.3 (red), 14 (green), 18.7 (dark blue), 25.7 (cyan), 37.3 (magenta), 51.3 (orange) and 70 (olive) at $200\ \mathrm{mK}$. The black line indicates the noise of the $t = 7\ \mu\mathrm{m}$ Nb on Si CPW from [58]. The dashed lines represent the fit with the numerical data for the surface and dielectric bulk contributions, while the inset shows the ratio between their respective noise spectral coefficients.

Al-SiN-Si CPW

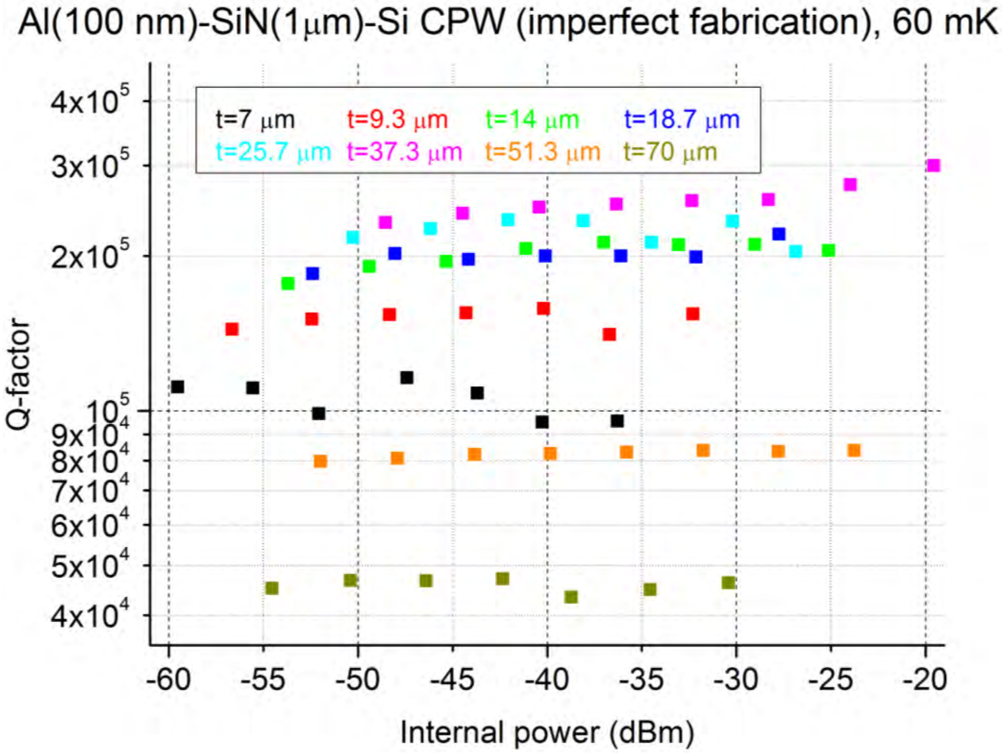

Figure 97 Internal quality factor versus internal power in dBm for the constant impedance Al-SiN-Si CPW resonator set with total width (in $\mu\mathrm{m}$) of 7 (black), 9.3 (red), 14 (green), 18.7 (dark blue), 25.7 (cyan), 37.3 (magenta), 51.3 (orange) and 70 (olive) at $60\ \mathrm{mK}$.

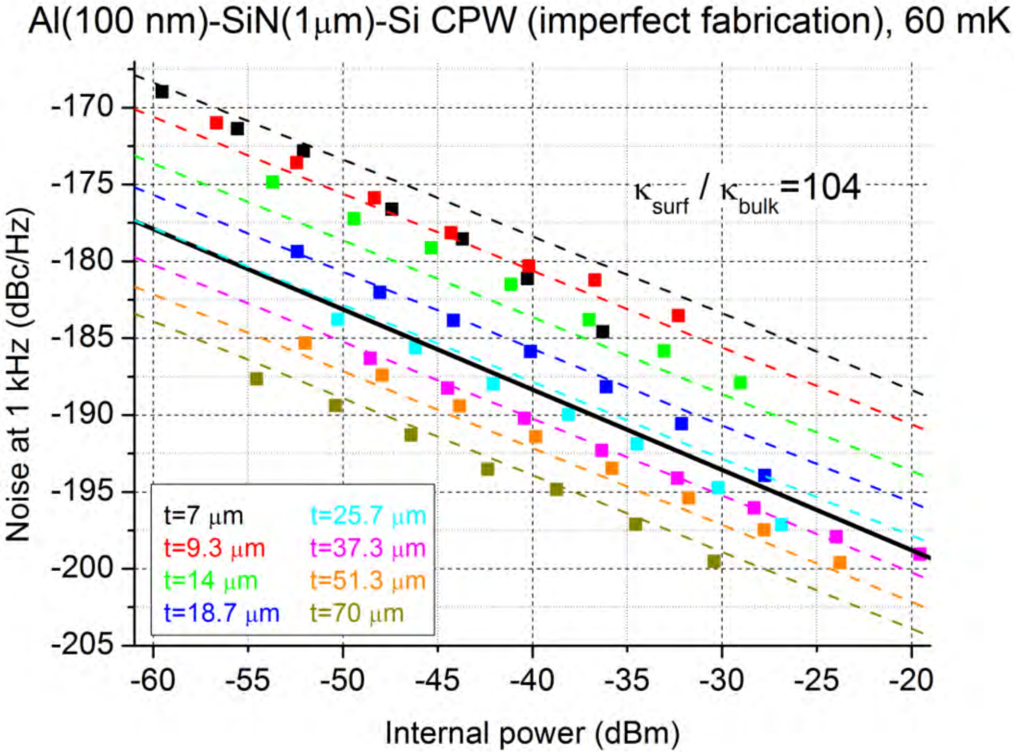

Figure 98 Noise measured at $1\ \mathrm{kHz}$ in $\mathrm{dBc/Hz}$ versus internal power in dBm for the constant impedance Al-SiN-Si CPW resonator set with total width (in $\mu\mathrm{m}$) of 7 (black), 9.3 (red), 14 (green), 18.7 (dark blue), 25.7 (cyan), 37.3 (magenta), 51.3 (orange) and 70 (olive) at $60\ \mathrm{mK}$. The black line indicates the noise of the $t = 7\ \mu\mathrm{m}$ Nb on Si CPW from [58]. The dashed lines represent the fit with the numerical data for the surface and dielectric bulk contributions, while the inset shows the ratio between their respective noise spectral coefficients.

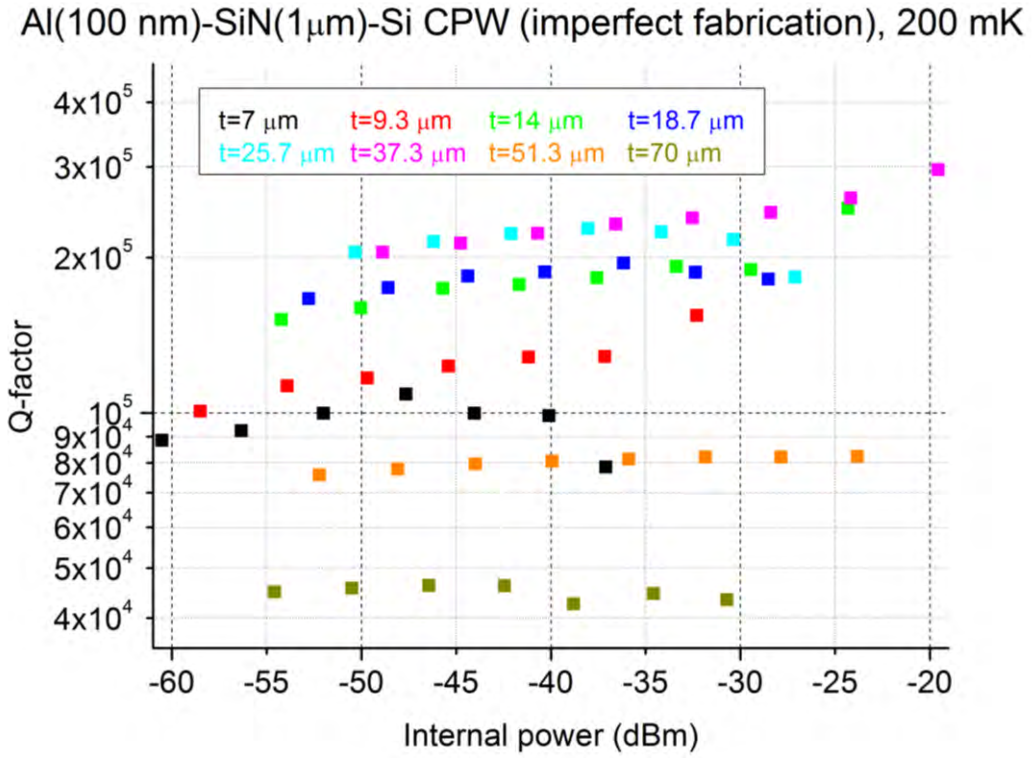

Figure 99 Internal quality factor versus internal power in dBm for the constant impedance Al-SiN-Si CPW resonator set with total width (in $\mu\mathrm{m}$) of 7 (black), 9.3 (red), 14 (green), 18.7 (dark blue), 25.7 (cyan), 37.3 (magenta), 51.3 (orange) and 70 (olive) at $200\ \mathrm{mK}$.

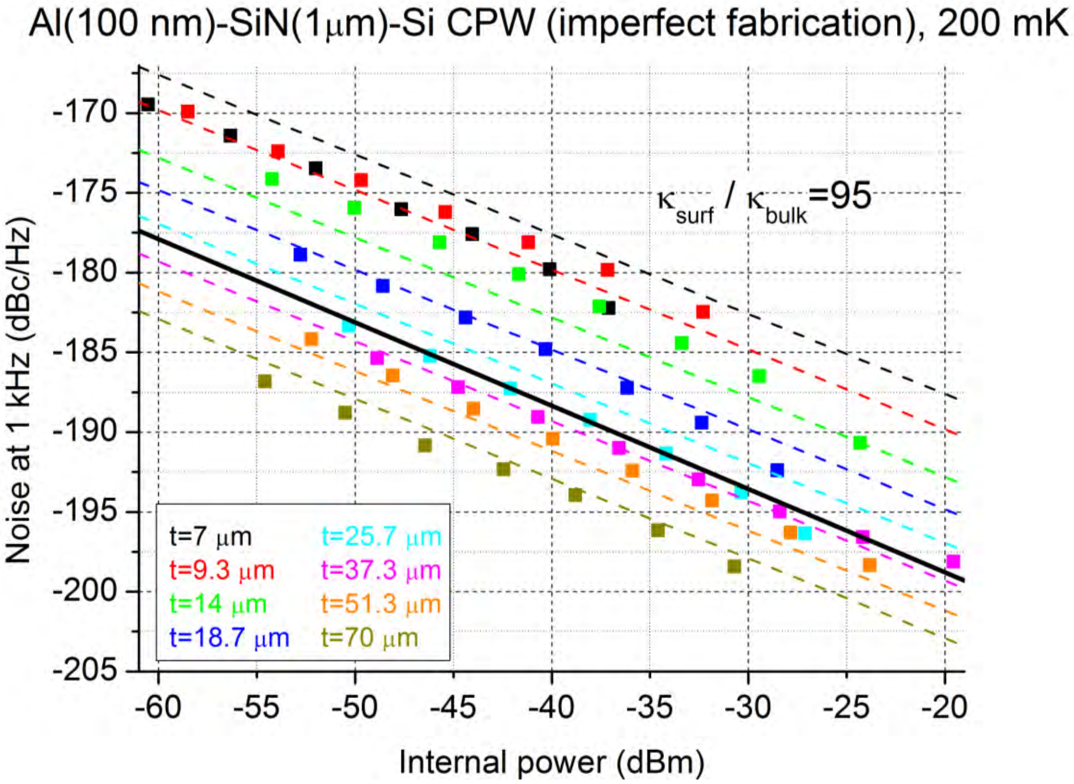

Figure 100 Noise measured at $1\ \mathrm{kHz}$ in $\mathrm{dBc/Hz}$ versus internal power in dBm for the constant impedance Al-SiN-Si CPW resonator set with total width (in $\mu\mathrm{m}$) of 7 (black), 9.3 (red), 14 (green), 18.7 (dark blue), 25.7 (cyan), 37.3 (magenta), 51.3 (orange) and 70 (olive) at $200\ \mathrm{mK}$. The black line indicates the noise of the $t = 7\ \mu\mathrm{m}$ Nb on Si CPW from [58]. The dashed lines represent the fit with the numerical data for the surface and dielectric bulk contributions, while the inset shows the ratio between their respective noise spectral coefficients.

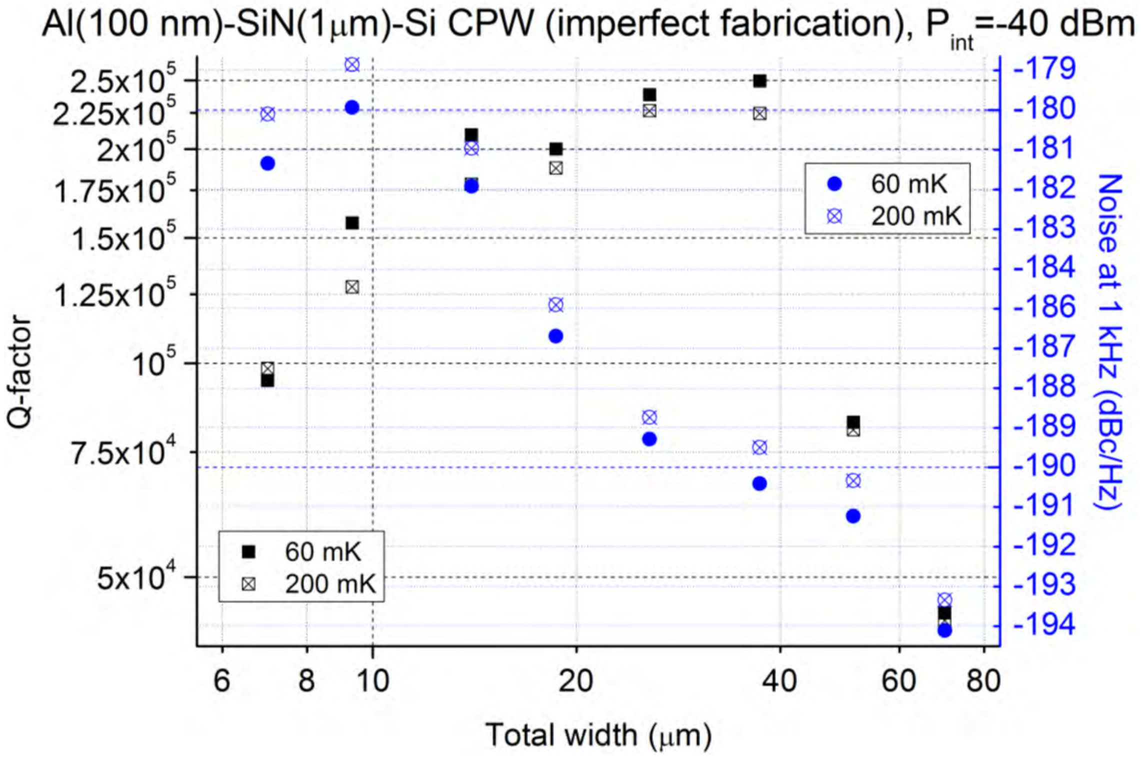

Figure 101 Dependency of Q-factor (black squares) and noise (blue circles) at $1\ \mathrm{kHz}$ in $\mathrm{dBc/Hz}$ versus on the total width in $\mu\mathrm{m}$ for the constant impedance Al-Si CPW resonator set at $P_{int} = -40\ \mathrm{dBm}$ for $T = 60$ (filled symbols) and $200\ \mathrm{mK}$ (symbols with cross).

Al-SiN CPW

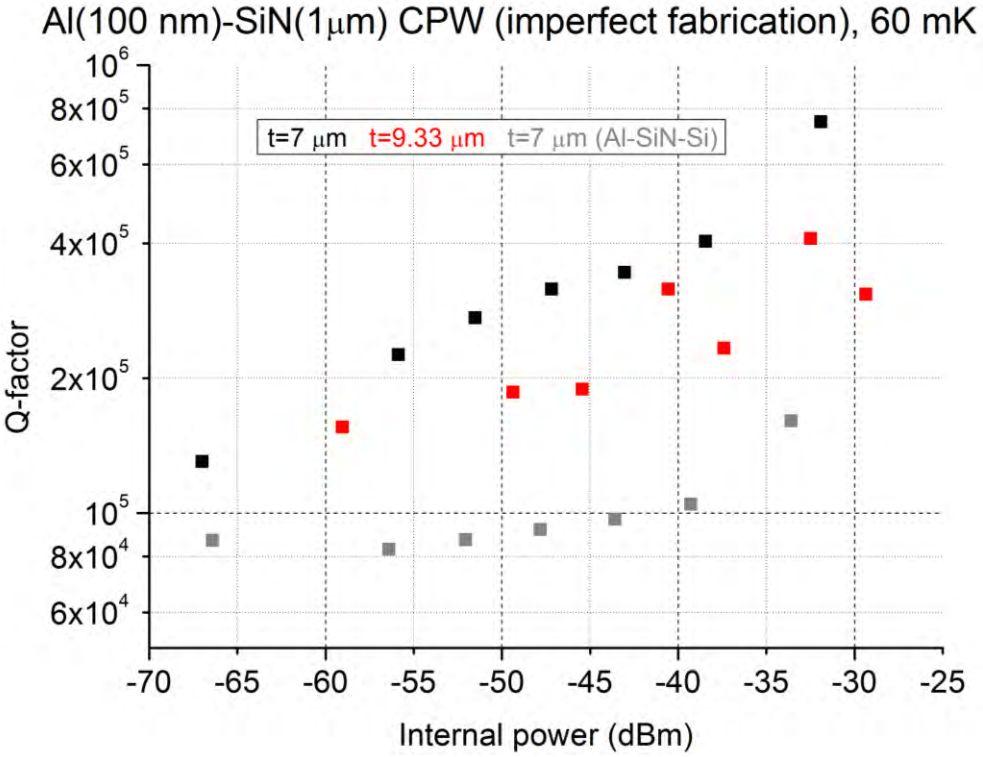

Figure 102 Internal quality factor versus internal power in dBm for the constant impedance Al-SiN CPW resonator set with Al-SiN-Si reference CPW with total width (in $\mu\mathrm{m}$) of 7 (black, CPW in grey) and 9.33 (red) at $60\ \mathrm{mK}$ (filled squares), $100\ \mathrm{mK}$ (open circles with cross) and $200\ \mathrm{mK}$ (filled triangle).

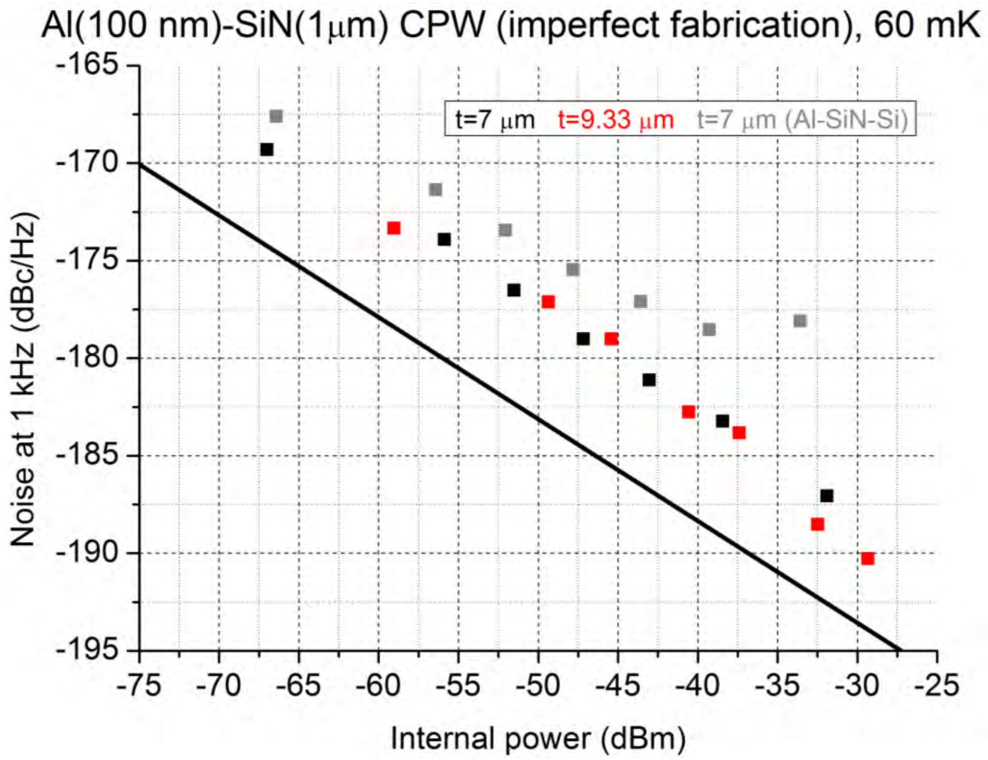

Figure 103 Noise measured at $1\ \mathrm{kHz}$ in $\mathrm{dBc/Hz}$ versus internal power in dBm for the constant impedance Al-SiN CPW resonator set with Al-SiN-Si reference CPW with total width (in $\mu\mathrm{m}$) of 7 (black, CPW in grey) and 9.33 (red) at $60\ \mathrm{mK}$ (filled squares), $100\ \mathrm{mK}$ (open circles with cross) and $200\ \mathrm{mK}$ (filled triangle). The black line indicates the noise of the $t = 7\ \mu\mathrm{m}$ Nb on Si CPW from [58].

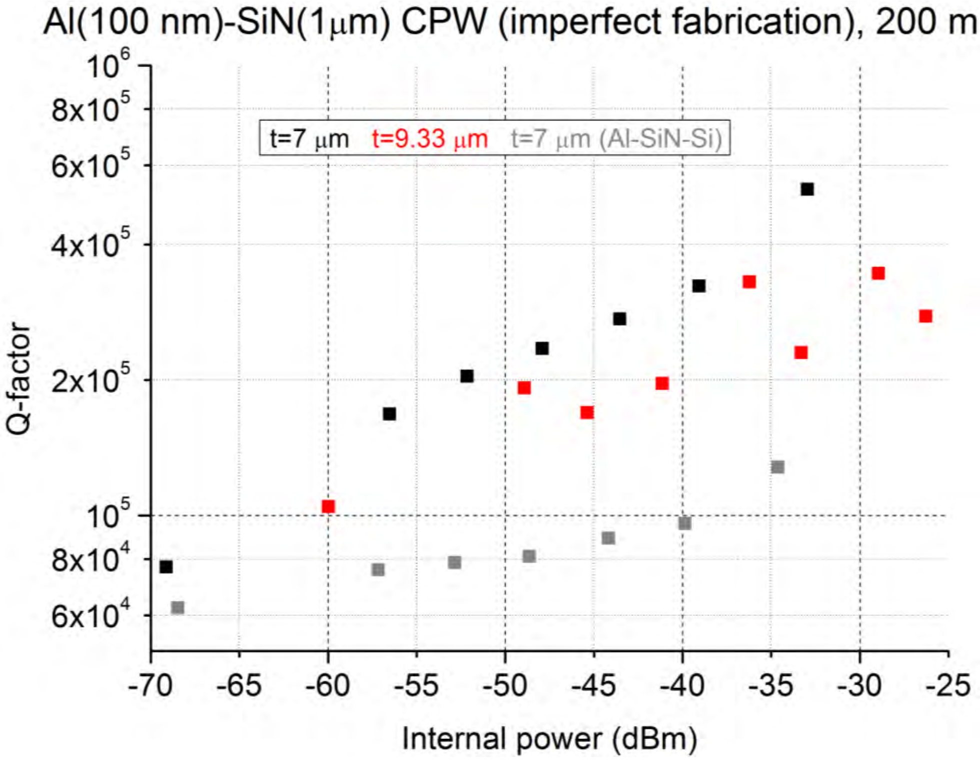

Figure 104 Internal quality factor versus internal power in dBm for the constant impedance Al-SiN CPW resonator set with Al-SiN-Si reference CPW with total width (in $\mu\mathrm{m}$) of 7 (black, CPW in grey) and 9.33 (red) at $60\ \mathrm{mK}$ (filled squares), $100\ \mathrm{mK}$ (open circles with cross) and $200\ \mathrm{mK}$ (filled triangle).

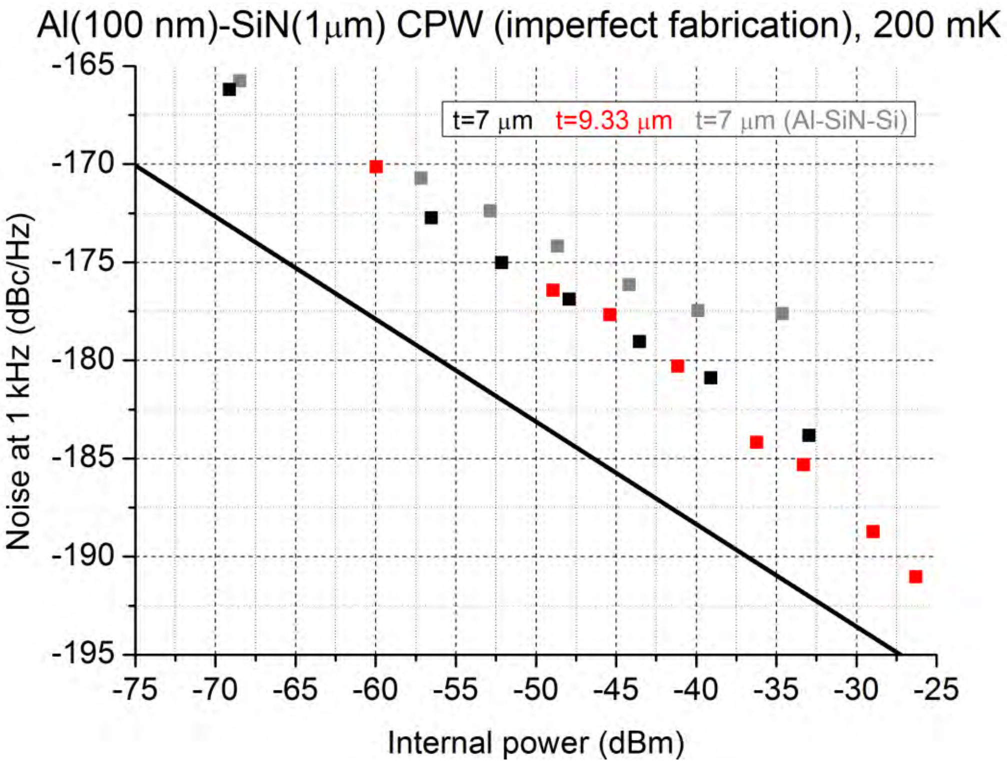

Figure 105 Noise measured at $1\ \mathrm{kHz}$ in $\mathrm{dBc/Hz}$ versus internal power in dBm for the constant impedance Al-SiN CPW resonator set with Al-SiN-Si reference CPW with total width (in $\mu\mathrm{m}$) of 7 (black, CPW in grey) and 9.33 (red) at $60\ \mathrm{mK}$ (filled squares), $100\ \mathrm{mK}$ (open circles with cross) and $200\ \mathrm{mK}$ (filled triangle). The black line indicates the noise of the $t = 7\ \mu\mathrm{m}$ Nb on Si CPW from [58].

Al-SiN microstrip (imperfect fabrication)

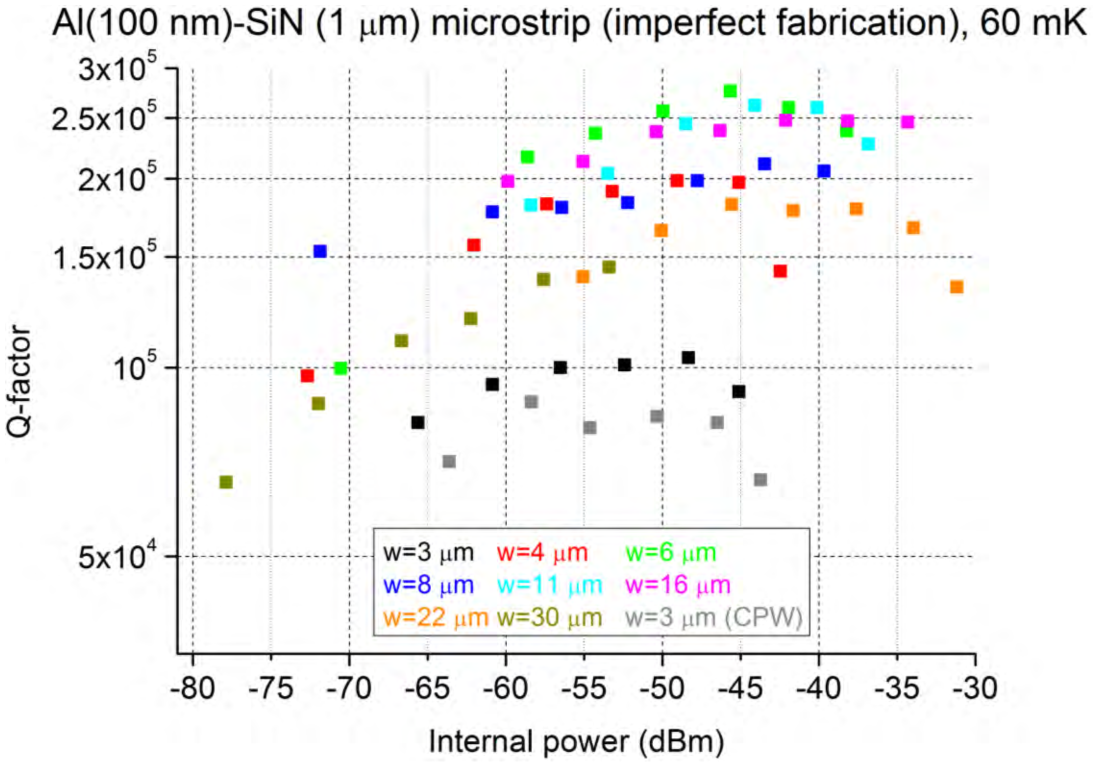

Figure 106 Internal quality factor versus internal power in dBm for the Al-SiN microstrip resonator set with Al-SiN-Si reference CPW with central width (in $\mu\mathrm{m}$) of 3 (black, CPW in grey), 4 (red), 6 (green), 8 (dark blue), 11 (cyan), 16 (magenta), 22 (orange) and 30 (olive) at $60\ \mathrm{mK}$.

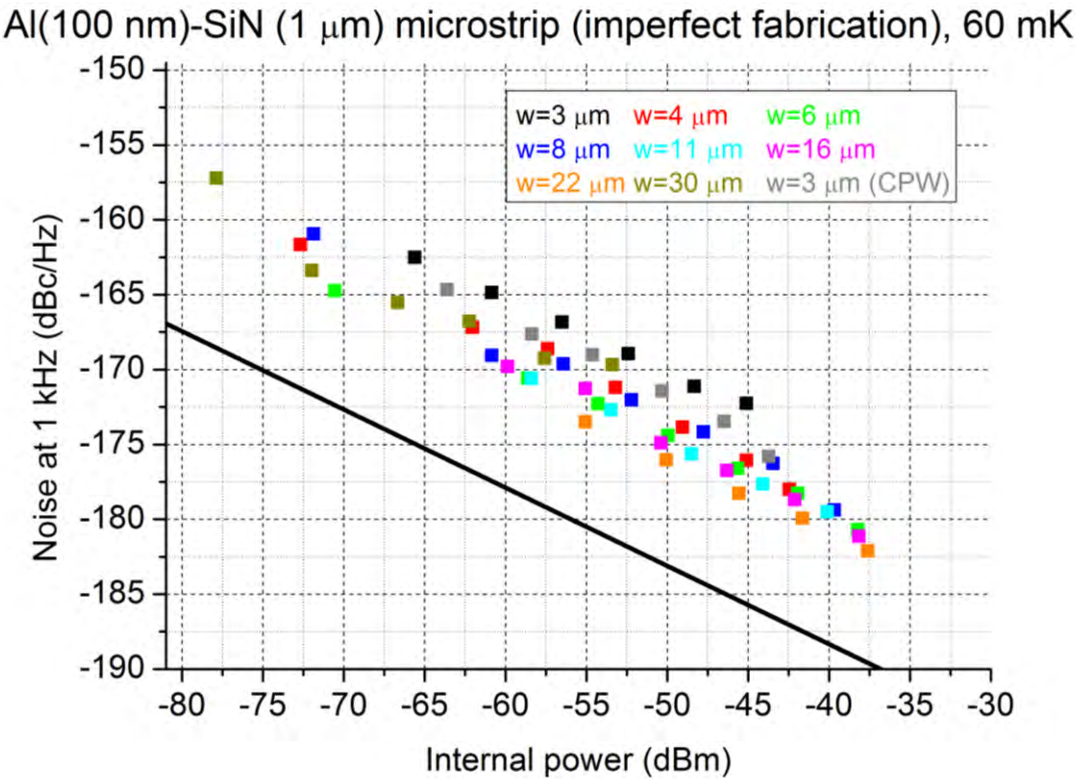

Figure 107 Noise measured at $1\ \mathrm{kHz}$ in $\mathrm{dBc/Hz}$ versus internal power in dBm for the Al-SiN microstrip resonator set with Al-SiN-Si reference CPW with central width (in $\mu\mathrm{m}$) of 3 (black, CPW in grey), 4 (red), 6 (green), 8 (dark blue), 11 (cyan), 16 (magenta), 22 (orange) and 30 (olive) at $60\ \mathrm{mK}$. The black line indicates the noise of the $t = 7\ \mu\mathrm{m}$ Nb on Si CPW from [58].

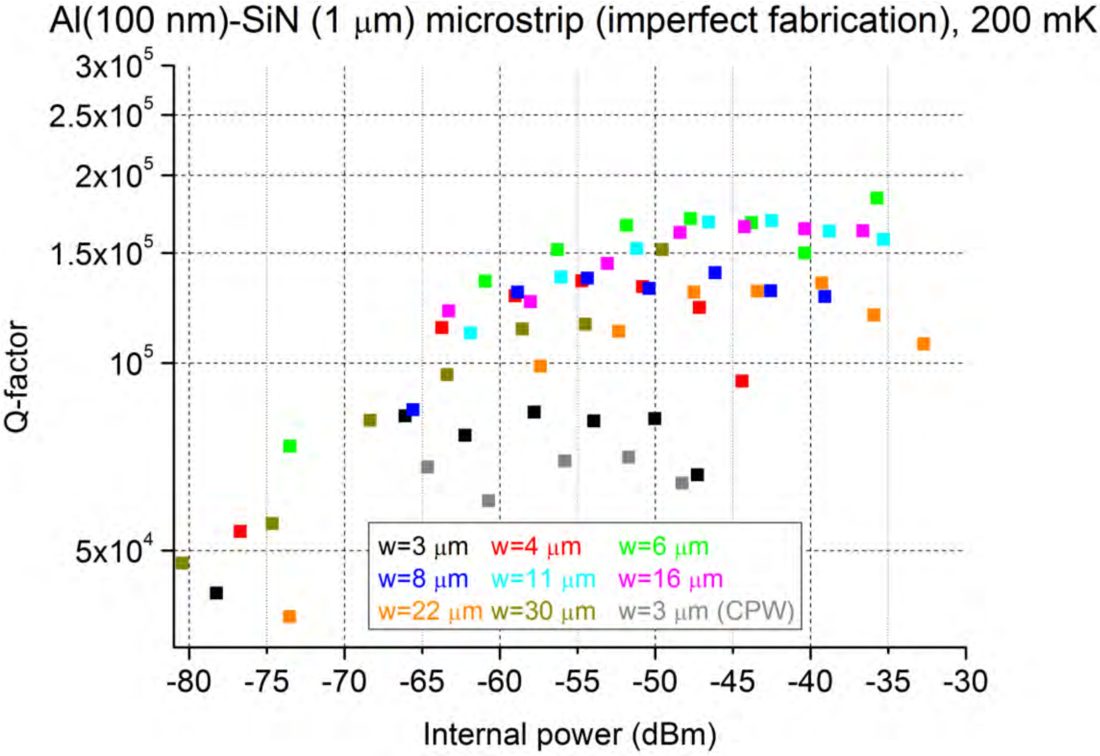

Figure 108 Internal quality factor versus internal power in dBm for the Al-SiN microstrip resonator set with Al-SiN-Si reference CPW with central width (in $\mu\mathrm{m}$) of 3 (black, CPW in grey), 4 (red), 6 (green), 8 (dark blue), 11 (cyan), 16 (magenta), 22 (orange) and 30 (olive) at $200\ \mathrm{mK}$.

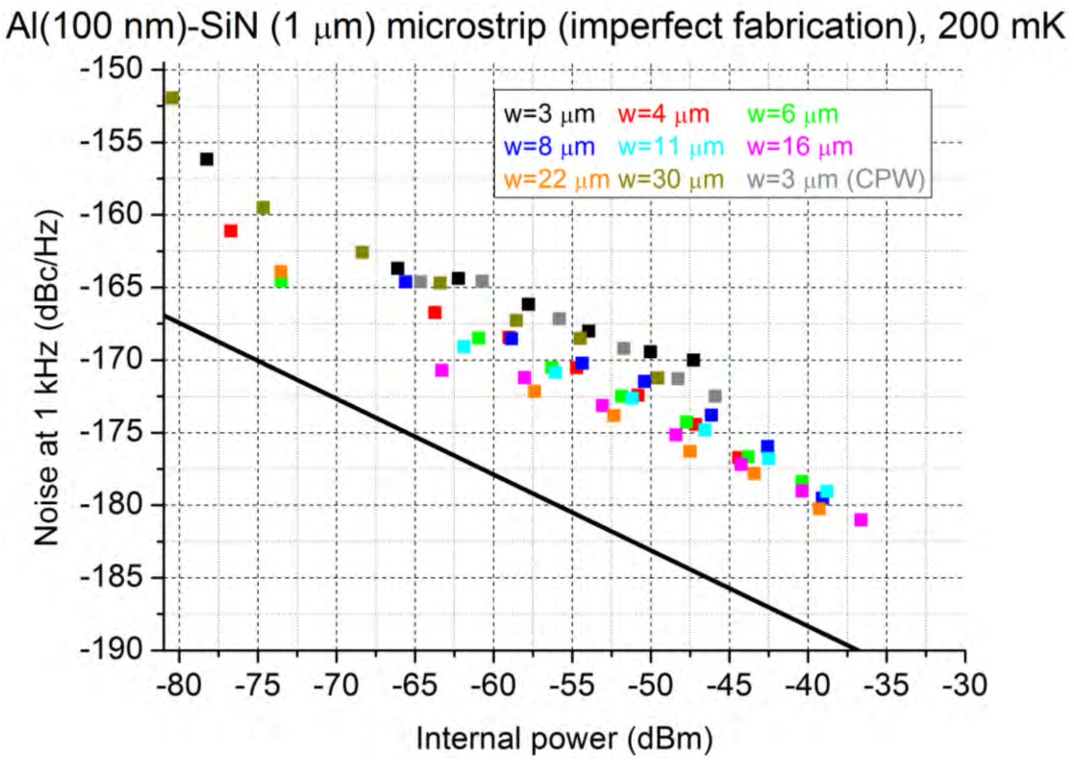

Figure 109 **Noise measured at $1\ \mathrm{kHz}$ in $\mathrm{dBc/Hz}$ versus internal power in dBm for the Al-SiN microstrip resonator set with Al-SiN-Si reference CPW with central width (in $\mu\mathrm{m}$) of 3 (black, CPW in grey), 4 (red), 6 (green), 8 (dark blue), 11 (cyan), 16 (magenta), 22 (orange) and 30 (olive) at $200\ \mathrm{mK}$. The black line indicates the noise of the $t = 7\ \mu\mathrm{m}$ Nb on Si CPW from [58].**

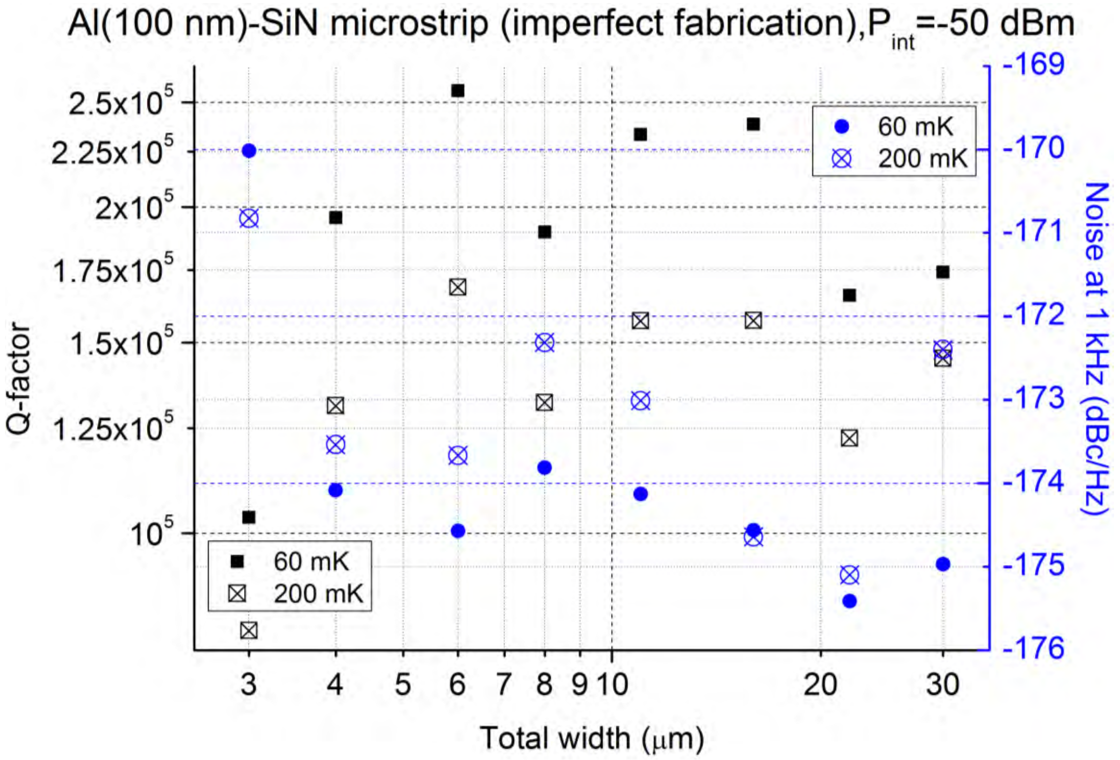

Figure 110 **Dependency of Q-factor (black squares) and noise (blue circles) at $1\ \mathrm{kHz}$ in $\mathrm{dBc/Hz}$ versus on the total width in $\mu\mathrm{m}$ for the constant impedance Al-SiN microstrip resonator set at $P_{int} = -50\ \mathrm{dBm}$ for $T = 60$ (filled symbols) and $200\ \mathrm{mK}$ (symbols with cross).**