FM Transceiver for Wireless Communication

RF Power amplifier & Low Noise Amplifier

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RF Power Amplifier & Low Noise Amplifier

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Abstract

This thesis explains the design process of two subsystems of a radio transmitter and receiver. The goal of the project is to transmit audio over a distance using FM modulation.

This report will focus on the power amplifier leading to the transmitting antenna and the low noise amplifier connected to the receiving antenna. A design process for a class E power amplifier and a low noise amplifier will be discussed.

Preface

For the bachelor graduation project, the group decided to go for designing and building an FM transceiver from scratch with discrete components. This project not only required knowledge of everything radio and FM signals but also other aspects of electrical engineering itself, for example, amplifiers, signal processing, and linear circuit analysis. Not to mention the whole process of designing on paper to simulation and finally prototyping. All these requirements intrigued the group as junior electrical engineers and were therefore motivated to accept the challenge so to speak. The whole process as named before together with four other team members is documented in a set of 3 thesis's of which this is one. To say the least this project in its totality would not have been possible if it weren't for the help of our supervisors Morteza Alavi and Marco Pelk, whose doors were always open to us in case we needed any help. To which we offer our sincerest of gratitude. Last but not least, the band of brothers that stuck through and through the last period of our journey especially this project which wasn't particularly simple. Thank you and godspeed.

-Darshan & Ruben

Contents

Chapter 1

Introduction

For our final Bachelor graduation project, an FM transceiver needs to be designed and built. What this means is that a signal at the input, preferably voice captured with a microphone, needs to be transmitted (over a minimum distance of 5 meters) using a Frequency Modulated (FM) signal and played back on a speaker at the receiving end. A complete overview of the system to be designed can be found in figure 1.1. The whole system is split into eight different modules, indicated by three colors in figure 1.1. The audio amplifier needs to sufficiently amplify the incoming signal (from a microphone) for the modulator. The modulator is in charge of modulating its input signal into an FM-signal. The final stage on the transmit side, the RF power amplifier, needs to make the signal "transmit ready" by amplifying it enough to be received over a distance of (at least) 5 meters. At the receiver side, the LNA needs to amplify the incoming signal far above the noise levels while adding little noise to the signal itself. The mixer is in charge of shifting the FM band to an intermediate frequency (IF) band. The next stage, IF amplifier, needs to amplify the signal sufficiently enough for the demodulator which demodulates the FM- signal. The final module at the receiver side is the speaker amplifier which amplifies the signal enough to drive the speaker. The RF power amplifier (PA) and the low noise amplifier (LNA) will be discussed in this thesis.

Part of the project assignment was to design the whole system with discrete components. This was purely for educational purposes and not a design choice made by the group.

For the simulation of all designed circuits, Keysight ADS [1] was used.

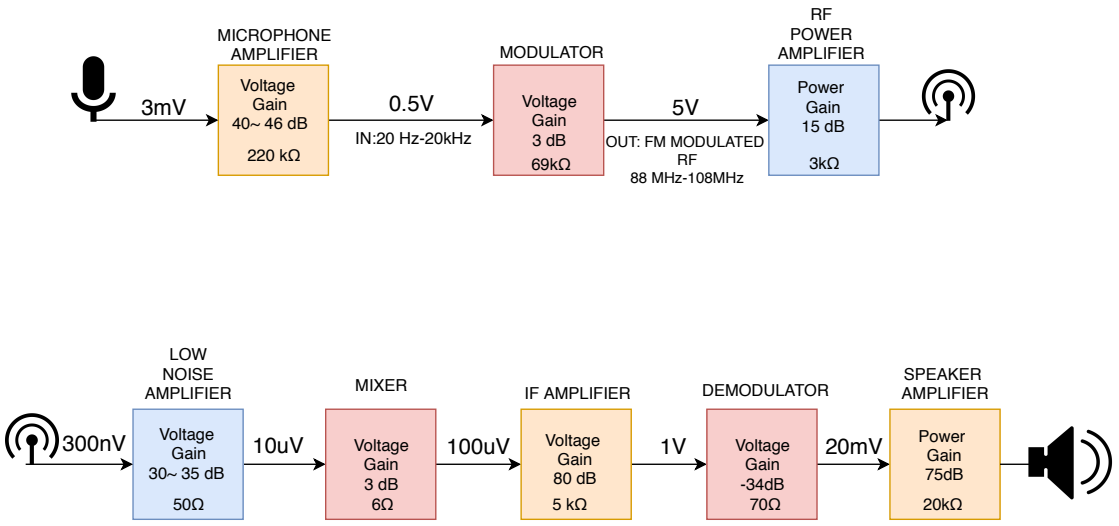


Figure 1.1: Overview of the complete system

State of the art analysis

Although we won't use it current FM transceivers often utilize some form of digital signal processing. An example schematic can be seen in figure 1.2. For this project, no digital signal processing is used. Besides the digital processing, commonly used transceiver radio systems of today use relatively more advanced modulation techniques than frequency (and amplitude) modulation. Digital systems provide high reliability and a higher signal to noise ratio. An example of a digital implementation of frequency modulation would be frequency shift keying (FSK). This modulation type uses different frequencies, added to a carrier frequency, to represent discrete signal values (bits) instead of continues values. Such a digital radio system would also involve analog to digital and digital to analog converters [2]. The FSK technique is attractive for short-range communication between two or more "digital" devices. For example, in smart cities or applications of IoT [3].

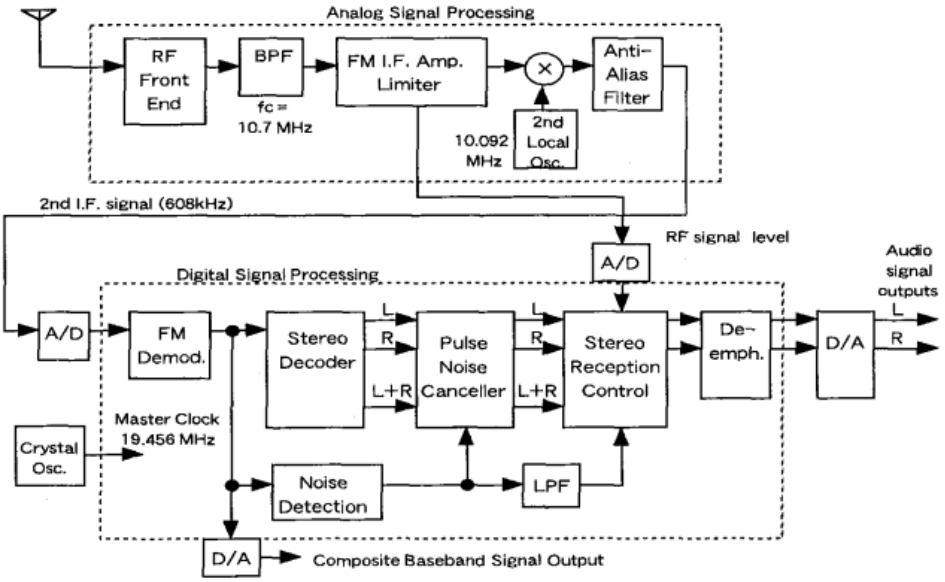


Figure 1.2: An FM receiver using DSP [4]

Long range audio broadcasting FM is being replaced by DAB+ (Digital Audio Broadcasting) [5]. This broadcasting type involves Orthogonal Frequency Division Multiplexing (OFDM) modulation. In OFDM the available bandwidth is split into multiple frequency bands to carry separate signals simultaneously over a single medium. The sub-carrier frequencies are orthogonal to each other, which means that interference between the multiple frequency bands is eliminated.

Chapter 2

Requirements for the RF PA

The power amplifier is the last stage of the FM transmitter, it takes the output from the modulator and amplify it enough to be detectable by the low noise amplifier at the input of the receiver side. The goal is to build it only using discrete components.

The modulator is able to supply a 5V amplitude signal to a load of 3000 Ω, this results in an input power of $\sim$4.2 mW.

The antenna at the output of the amplifier is assumed to have an impedance of 50 Ω. The complete system will have to transmit a signal correctly over a distance of 5 meters.

The LNA will be able to receive a 50 µV signal, with an input impedance of 50 Ω, requiring the receiver to receive at least 25 pW. To achieve this input voltage, the required transmitting power using isotropic antennas is found in equation 2.2. This equation is derived from equation 2.1 [6], relating the transmitted and received power, and the directivity of an isotropic antenna $D = 1$.

$$\frac{P_r}{P_t} = \frac{D_t D_r \lambda^2}{16R^2} \tag{2.1}$$

$$P_t = \frac{16\pi^2 R^2 P_r}{\lambda^2} \approx 11 \text{ nW} \tag{2.2}$$

Although this value is low, the actual required power will be higher, since the used antennas will not be ideal and will cause more losses.

The supply voltage is set at 12 V, this voltage is used for all stages of the transmitter and receiver so that all stages can be fed by just one power supply.

Summary of requirements

- Accept an input signal of 5 V amplitude
- $Z_{in} \geq 3000\ \Omega$
- $Z_{load} = 50\ \Omega$
- $P_{out} \gg 11$ nW
- $V_{DC} = 12$ V

Chapter 3

Design of the RF power amplifier

3.1 Selection of the amplifier type

There are many classes of amplifiers, A class A amplifier is the simplest type of amplifier, they consist of a single transistor which is used as a voltage controlled current source (VCCS). They have the lowest efficiency, because this utilization of the transistor requires a constant DC current.

A class B amplifier consists of two transistors, each conducting for (slightly less than) 50% of the signal. Because both transistors are off when there is no incoming signal, there is no DC current flowing, allowing for a higher frequency to be achieved. However, the transistors will still dissipate part of the supplied power, due to which 100% efficiency can't (theoretically or practically) be achieved.

Since the incoming signal is FM modulated, variations in amplitude are not an important part of the signal, only the frequency of the signal is important. Therefore, the amplifier does not have to be linear, and thus a switching amplifier can be used. An ideal switch switches between acting as a short circuit and an open circuit, and therefore never dissipates any power. If the topology is chosen correctly, no power is dissipated outside of the load. Of course a transistor can't behave as an ideal switch, and therefore can't achieve perfect efficiency, but this behaviour can be approached with transistors.

Class D is the first type to use the transistor as a switch instead of a current source. It consists of two transistors, one connected to a DC voltage source, one to ground. The two transistors should be driven 180° out of phase, resulting in a square wave, this wave is turned into a sine wave using a band-pass filter at the output. However, due to the parasitic capacitances in such a circuit, this type of amplifier isn't suitable for frequencies above 30 MHz [7], making it unusable for our system. Further disadvantages include degradation of efficiency if the switching between the transistors is mismatched [8]. Class E is another class of switching amplifiers. It's able to achieve 100% efficiency due to it's non-overlapping current and voltage waveform when correctly tuned. It functions similarly to a boost converter.

This last type was chosen for the design, mainly for the efficiency it's able to achieve. The next sections will elaborate about the design of a class E amplifier.

3.2 Design using an ideal switch

The amplifier consists of a switch, a capacitor in parallel to the switch, an inductor in series with the switch and a band-pass filter to the output. This circuit can be seen in figure 3.1. The amplifier functions similar to a boost converter, first the switch closes, this causes a current to flow through the switch, charging up L_1. After a moment the switch opens and the inductor current is pushed into capacitor C_1. Subsequently the charge built up in the capacitor is discharged to the output of the amplifier.

To prevent power being dissipated by the switch the switch should satisfy the zero voltage switching condition (No voltage over the switch when it closes).

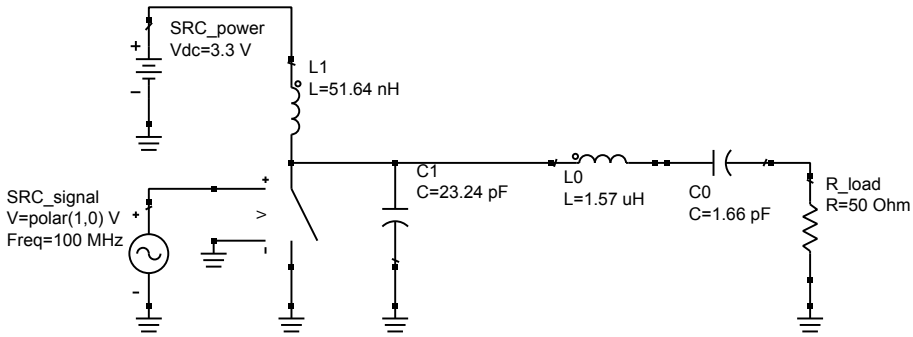


Figure 3.1: Class E amplifier using an ideal switch

3.2.1 Band-pass filter

The amplifier needs to equally amplify signals from 88 to 108 MHz, therefore a center frequency of 98 MHz was chosen. The -3 dB bandwidth was set to 40 MHz, resulting in an attenuation of -1 dB at the edges (88 and 108 MHz) of the desired band.

Equations 3.3 and 3.4 were used to calculate the inductance and capacitance required for this band-pass filter, these equations are derived from equations 3.1 and 3.2 for the Q-factor and resonance frequency of the filter. In these equations BW refers to the -3 dB bandwidth. 98 MHz was chosen as center frequency since it lies at the center of the 88-108 MHz band.

$$Q = \frac{f_0}{BW} = \frac{2\pi f_0 L_0}{R_{load}} \tag{3.1}$$

$$f_0 = \frac{1}{2\pi\sqrt{L_0 C_0}} \tag{3.2}$$

$$L_0 = \frac{R_{load}}{2\pi BW} \tag{3.3}$$

$$C_0 = \frac{BW}{2\pi R_{load} f_0^2} \tag{3.4}$$

3.2.2 The series inductance and parallel capacitance

For a parallel circuit class E amplifier the following design equations were derived in [9]:

$$L_1 = 0.732\frac{R_{load}}{\omega} \tag{3.5}$$

$$C_1 = \frac{0.685}{\omega R_{load}} \tag{3.6}$$

$$P_{out} = 1.365\frac{V_{cc}^2}{R_{load}} \tag{3.7}$$

$$V_{switch,max} = 3.647 V_{cc} \tag{3.8}$$

In equations 3.7 and 3.8 it's shown that the power output, supply voltage and the maximum voltage over the transistor are directly related. Since a transistor will only allow a certain voltage over it before breaking down, this is an important limiting factor in what the maximum power output will be.

3.2.3 Results

As can be seen in figure 3.2, the switch closes (and current starts flowing) at the moment that the voltage over the switch returns to $0V$. The slightest mismatch will cause a current peak at the moment that the switch closes. If the components have the correct values, then the amplifier will have an efficiency of 100%.

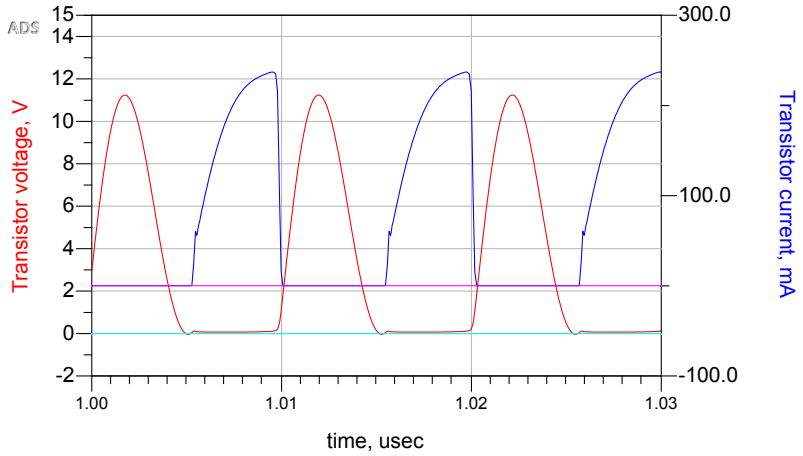


Figure 3.2: Current and voltage behaviour of the switch

3.3 Using the model of a real transistor

The final design is shown in figure 3.3, and is discussed in the following subsections.

3.3.1 Selection of the transistor

For the selection of a transistor, the options were limited to those available through Farnell. The transistor needs to have a transition frequency of at least 10 times the transmitting frequency and a maximum collector current as large as available. A list of available NPN transistors is shown in table 3.1. Although the BFR106 advertises a higher maximum nominal current, the BFU590 advertise a higher absolute maximum current, implying that these transistors are more robust. In the end, the BFU590G was chosen because, while the BFU590G and BFU590Q have very similar specifications, it has a larger package, making it easier to handle when building the prototype.

Model	f_t	$I_{c,max}$	$I_{c,absolute\ max}$	P_d	β
NXP BFU590G [10]	8.5 GHz	200 mA	300 mA	2 W	60
NXP BFU590Q [11]	8 GHz	200 mA	300 mA	2 W	60
INFINEON BFR106 [12]	5 GHz	210 mA	210 mA	700 mW	70

Table 3.1: Transistors available through Farnell

3.3.2 Input biasing

The input (at the right side of capacitor C_4) is biased with 1 V. R_1 and R_2 are chosen such that for no input signal V_{be} of the transistor is 0.7 V, at this voltage I_b is small enough to be negligible, resulting in equation 3.9. For this input voltage and lower the transistor is considered to be a closed switch. For larger voltages, the base-emitter junction can be considered a short circuit, and the current is only limited by R_1, this directly impacting the input impedance.

$$V_{be} = \frac{R_2}{R_1 + R_2} V_{in,bias} - I_b R_1 = \frac{R_2}{R_1 + R_2} V_{in,bias} \tag{3.9}$$

With the biasing of the transistor a compromise had to be made between minimizing the required input power, and maintaining the behaviour of the transistor as an ideal switch. The highest input impedance achieved, with the amplifier still functioning adequately, is 500 Ω.

Inductor L_5 is placed to prevent R_4 from decreasing the input impedance of the amplifier.

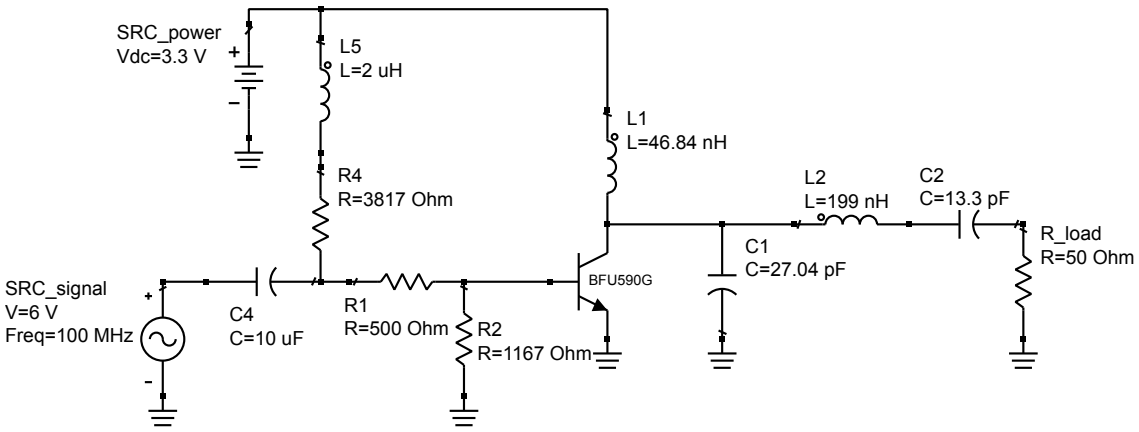


Figure 3.3: Class E amplifier using a real transistor

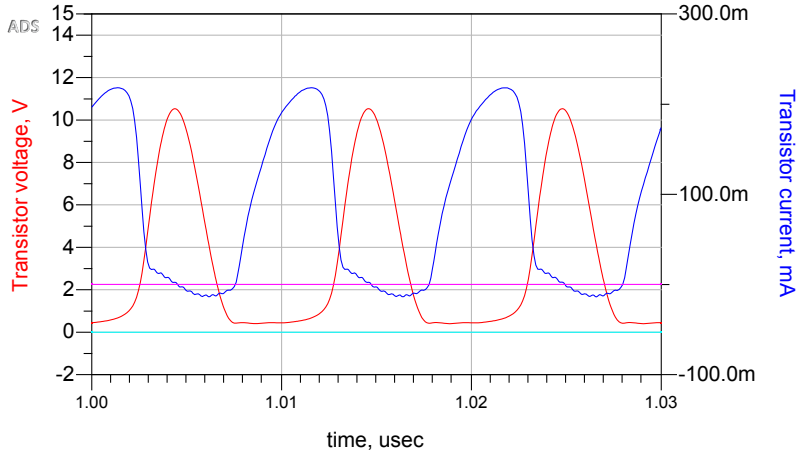


Figure 3.4: Current and voltage behaviour with a real transistor model

3.4 Pre-amplifier

In the previous section it was mentioned that the input impedance is 500 Ω. The modulator can supply a signal with a 5 V amplitude to a load resistance of 3000 Ω, this amplifier requires a higher input impedance. Therefore a pre-amplifier has to be placed between the stages. For this amplifier a common-collector circuit was chosen for it's simplicity. The voltage gain of such a circuit is unity, the current gain depends on the used transistor. The final circuit is shown in figure 3.5.

3.4.1 Emitter current biasing

The oscillator signal should result in a 5 V amplitude output, which gives a peak output current of 10 mA and -10 mA, assuming a load impedance of 500 Ω.

To prevent the transistor from turning off due to a negative current R_4 and L_1 are placed to act as a current source supplying 10 mA, which results in an emitter current swing of 10 mA. To determine R_4, it's assumed that $V_{e,dc} = 6V$, and calculated using the following equation:

$$R_4 = \frac{V_{e,dc}}{I_{e,dc}} = \frac{6\text{ V}}{10\text{ mA}} = 600\ \Omega \tag{3.10}$$

According to the datasheet of the BFU550A [13], $I_c = 10mA$ corresponds to $V_{be} = 0.85V$ and $I_b = 100\mu A$.

3.4.2 Emitter voltage biasing

The emitter voltage (6 V) is to be biased at half of the supply voltage (12 V). To achieve this the base is biased at 6 V + V_{be}. The following equations are used to determine the values for R_1 and R_2:

$$R_\pi = \frac{V_b}{I_b} \tag{3.11}$$

$$\frac{V_b}{V_{source}} = \frac{R_2 \parallel R_\pi}{R_1 + (R_2 \parallel R_\pi)} = \frac{6.85}{12} \tag{3.12}$$

$$R_{in} = R_1 \parallel R_2 \parallel R_\pi = \frac{R_1(R_2 \parallel R_\pi)}{R_1 + (R_2 \parallel R_\pi)} = 3000\ \Omega \tag{3.13}$$

From the above equations the following formulas are derived for R_1 and R_2:

$$R_1 = R_{in}\frac{V_{source}}{V_b} \tag{3.14}$$

$$R_2 \parallel R_\pi = \frac{R_1 V_b}{V_{source} - V_b} \tag{3.15}$$

$$R_2 = \frac{(R_2 \parallel R_\pi)R_\pi}{R_\pi - (R_2 \parallel R_\pi)} \tag{3.16}$$

3.4.3 Efficiency

Although the amplifier is able to replicate the input signal with few to no distortions, the efficiency is very low. With a DC current of 10 mA, the power source needs to supply 120 mW (assuming the current through R_1 is negligible), while the output only receives 25 mW, resulting in a maximum efficiency of 21%.

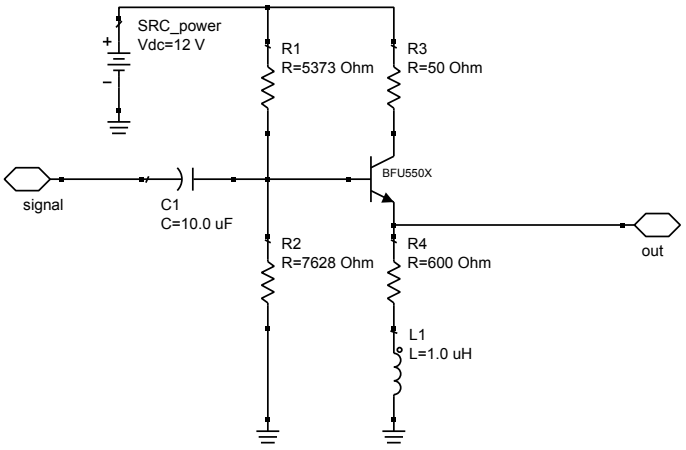


Figure 3.5: Common collector mode pre-amplifier

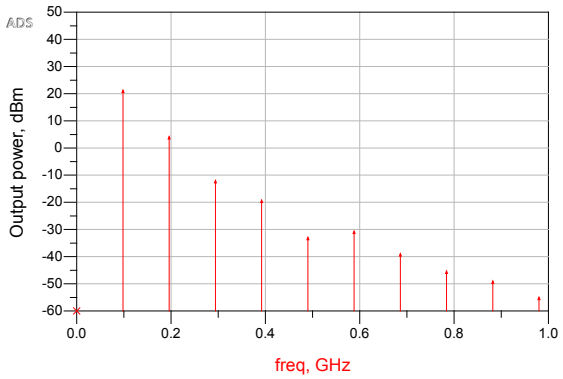
3.5 Simulation results

Table 3.6a shows details about the power consumption and output power of the amplifier, found using simulations in ADS. As shown in figure 3.6b, the amplifier also produces harmonics but these compose only about 2% of the total output power. The power at the second harmonic is at most 14 dB lower than the power at the desired frequency.

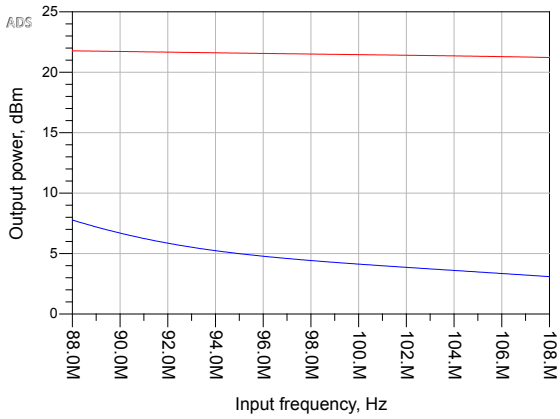
Attaching the modulator circuit to the input of the PA results in similar results to simulations where the modulator is modelled as a voltage source. This leads to the conclusion that the PA functions correctly.

P_{signal}	4.86 mW
P_{out}	186 mW
$P_{in,pre-amp}$	136 mW
$P_{in,power-amp}$	260 mW
$P_{in,total}$	396 mW
η_{total}	47.0%
Gain	15.8 dB

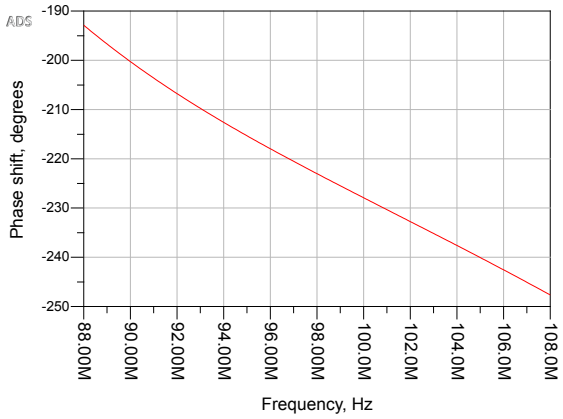
(a) Power measurements at 98 MHz



(b) Harmonics generated by the amplifier



(c) Desired frequency gain (red) and second harmonic gain (blue) of the amplifier



(d) Phase shift between the input and output of the amplifier

Figure 3.6: Various simulation results

Chapter 4

LNA Requirements

The Low Noise Amplifier (LNA) is the first stage at the receiving end of the FM transceiver. The main requirement of the LNA is amplifying the incoming FM signal (from the antenna) far above the noise levels. This can be dissected into three main requirements or rather goals the LNA has to achieve.
The first is to amplifying the incoming FM signal as stated before. According to the literature, the average typical gain of the LNA is around 15 dB [14, p. 167]. This is also the gain requirement set for the LNA.
Impedance matching to the antenna's impedance of 50 ohms is important for two reasons. The maximum power transfer from the antenna to the LNA is achieved when the loads are matched. A second reason is to minimize signal reflections which will cause signal quality degradation when it's too severe. The reflection coefficient which gives the amount of signal reflection based on load and source impedance's is given by equation 5.7. Thus, in other words, the second requirement for the LNA is achieving an input impedance of 50 ohms.
The third requirement of the LNA is to introduce as little noise as possible. Being the first stage of a series of amplifiers (other modules in the receiver side) it's crucial to keep the noise figure as low as possible. According to the literature study, the typical average noise figure (NF) of LNA's is around 2 dB. Thus the third and final requirement of the LNA is to not exceed a maximum NF of 2dB.

Summarizing the requirements:

- A gain of at least 15 dB for the whole FM-band.
- An input impedance of 50 ohms with a reflection coefficient of 0.
- A maximum noise figure of 2 dB.

One extra requirement is that the LNA should be connected to a voltage source of 12V. This value is set by the group that needs the highest value for its module to function. This is done to connect all the modules to one source instead of using different sources with different values.

In table A.1 gives a broader overview of some of the key typical values which set the benchmark. And ultimately the LNA requirements are based upon that standard.

Chapter 5

LNA design

The design of the LNA follows the same order as the requirements. First, the main focus was placed on designing a circuit that can provide optimal gain. Thereafter adding to the design to match with an antenna with a source impedance of 50 Ω. During the designing of these two ”sub-modules” measurements were taken to assure a minimal NF.

5.1 Gain

The gain-requirement for the LNA was set to 15 dB. For LNA's designed with BJT transistors, there are typically two circuit topologies used. The common-emitter and common-base. According to [14, p. 177] the common-base topology is more sensitive for noise. For this reason, the amplifier is designed based upon a common-emitter topology.

5.1.1 DC Biasing

The full schematic of the gain-stage is shown in figure 5.1. Where the antenna is modeled as a Thevenin voltage source and a resistor of 50 Ω. The BJT transistor used is the NXP BFU550A NPN transistor. One of the applications this transistor is used for is RF applications like low noise amplifiers [13]. The used transistor is rated for a maximum collector current (Ic) of 50mA. Suppose the transistor is modeled as a closed switch and the full 12V source is placed on resistor 1 (R1) then the maximum current flowing through this resistor must be lower than 50mA. Conform to Ohm's law this R1 needs to be at least higher than 240 Ω. R1 was chosen to be 400 Ω. The maximum Ic with the chosen R1 is 30mA. Which is lower than the maximum rated Ic by a safe margin.

The next step for the design process of the amplification is selecting a correct operating point and biasing the transistor around the chosen operating point. According to the datasheet of the transistor, there exists a relation between Ic and NF [13], The NF increases rapidly when the Ic increases. This form of noise can be stated as shot noise and the general formula is given in equation 5.1.

$$I^2_{noise(RMS)} = 2qIcF \tag{5.1}$$

This relationship forms the basis for selecting the operating point. For both an optimum Ic and NF the Ic needs to be biased around 10mA according to the datasheet.
Figure 5.2 shows the characteristics of I-V curves for the used transistor. This graph shows the relationship between Ic, collector-emitter voltage (Vce) and base current (Ib). The diagonal line shows the 400 Ω load line. The intersection points between the load line and I-V curves are the correct operating points for the chosen transistor. If the Ic needs to be around 10 mA then the best operating point (considering the NF-Ic relation) is given by the marker in the graph. Thus, an Ic of 11mA, Vce of 7.56V and an Ib of 125uA. The current gain β is 88 at this operating point.

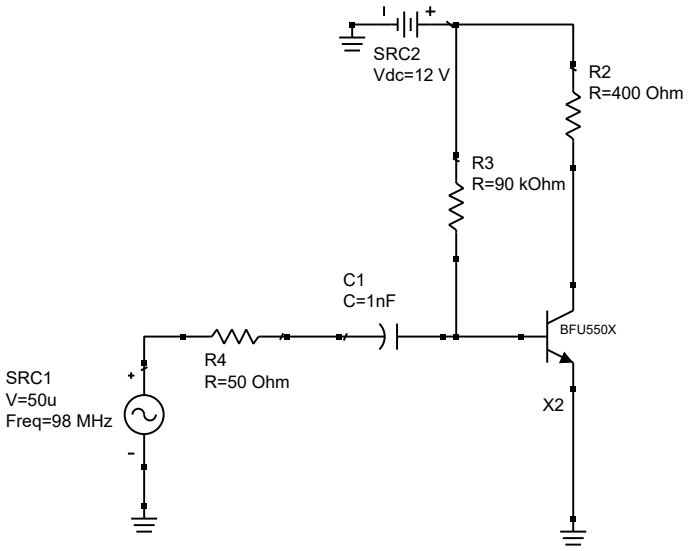


Figure 5.1: Schematic gain stage

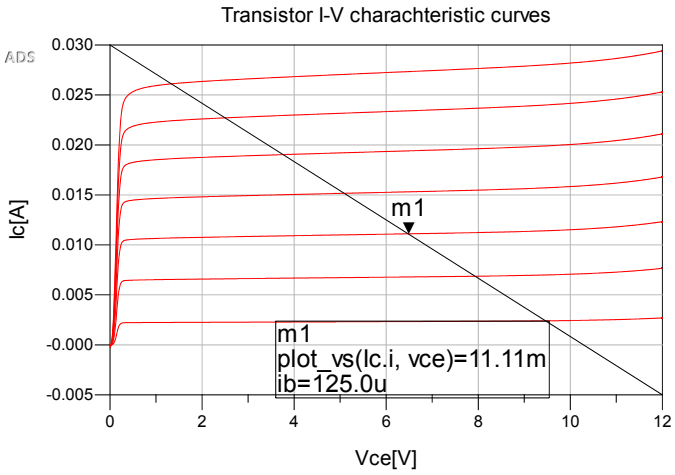


Figure 5.2: Charachteristic I-V curves

With 12V source and a base-emitter voltage of 0.7V (characteristic for BJT transistors) R2 needs to be

approximately 90 kΩ conform 5.2.

$$R2 = \frac{12V - Vce}{Ib} \tag{5.2}$$

C1 is placed as a DC- block, to force the Ib into the base instead into the antenna side. The value is chosen to be 1 nF. For a minimal frequency of 88MHz (FM-Band), the impedance of this 1 nF becomes 1.8086 Ω, which is considered small for the AC signal.

5.1.2 Theoretical values

With the chosen components, it's now possible to calculate the maximum theoretical achievable gain. To analyze the proposed circuit the π-model is used. The equivalent circuit (with the π-model incorporated) is given in figure 5.3.

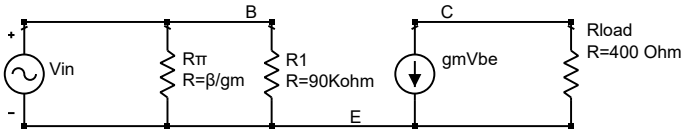


Figure 5.3: The amplifier stage with the π-model as transistor

It's important to note that with the used π-model certain aspects of the BJT-transistor aren't modeled and therefore aren't taken into consideration. These are the base-emitter capacitance, base-collector resistance, and capacitance. This is done due to the assumption that these factors are negligible for the gain and can thereby simplify calculations greatly.
The gain can be derived by a Kirchhoff's current loop at the output and is given by equation 5.3.

$$Vout = gmVbe \times Rload \tag{5.3}$$

$$G = \frac{Vout}{Vin} = \frac{gmVbe \times Rload}{Vin}$$

This can be simplified further with the following assumptions:

$$Vbe = Vin$$

$$gm = \frac{Ic}{Vt}$$

Then the gain becomes:

$$G = gm \times Rload = \frac{Ic}{Vt} \times Rload \tag{5.4}$$

Filling in the values for the components a theoretical maximum gain of 176 approximately 45dB is obtained. The values of the various components are summarized in table 5.1. In conclusion with the used setup and chosen components for biasing, the gain is sufficient enough and therefore fulfills the requirement for gain which was set upon 15 dB.

5.1.3 Buffer

As seen in the derivation of the gain in section 5.1.2, it's load dependent. In other words if the input impedance of the next stage, which is the mixer, is low (approximately 6 Ω) then the gain of LNA will be low as well . To elaborate suppose the mixer is modeled as an 6 Ω resistor (figure 5.4). Plugging this resistor (R5) in the pi-model in the previous section then it will appear as a parallel connection with R1 (Rload in the π-model figure). This will influence the Rload conform equation 5.6.

$$\frac{1}{R_{loadnew}} = \frac{1}{Rload} + \frac{1}{R5} \tag{5.5}$$

$$R_{loadnew} = \frac{Rload \times R5}{Rload + R5} \tag{5.6}$$

If Rload $>>$ R5 then the equation becomes :

$$R_{loadnew} = R5$$

Plugging $R_{loadnew}$ in the previously derived equation for the gain one can see that the input impedance of the mixer can heavily influence the gain of the LNA. The input impedance of mixer needs to be very large for it to have little influence. Unfortunately this is not the case.

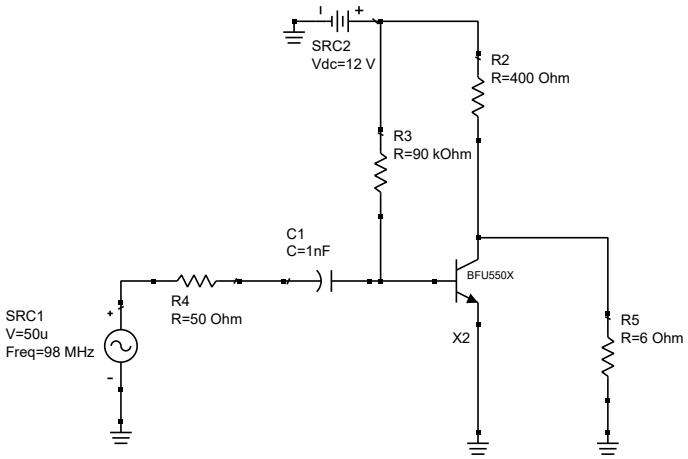


Figure 5.4: Schematic gain stage with modeled mixer

To bypass this issue a common-collector voltage buffer is placed in between the LNA and mixer stage. This buffer has a high input impedance. For the buffer, the same transistor with the same operating point is used. The full schematic (LNA with buffer) is shown in figure 5.5. When 11mA flows through the 400 Ω resistor then the voltage at the base of the second transistor is approximately 7V. If the same Q-point is used for the second transistor then it can be assumed that the current through the emitter of the second transistor also needs to be 11 mA. This emitter current can be controlled with resistor R4. If the Vce of the second transistor is 0.7V then the voltage over R4 needs to be approximately 6.5V. With 11mA flowing through this resistor the value of this resistor needs to be roughly 600 Ω.

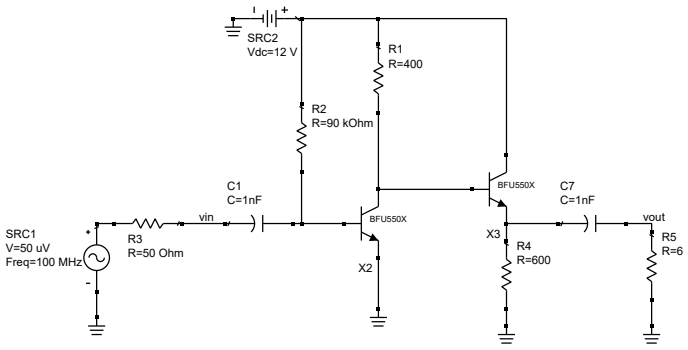


Figure 5.5: The amplifier stage with an the voltage buffer

5.2 Impedance Matching

For the LNA impedance matching is an important aspect. The most important reason for this is to minimize signal reflections back to the antenna. The reflection coefficient gives the amount of reflection based on

antenna and load impedance's and is given in equation 5.7. Here Zin is the impedance of the antenna and RL is the impedance of the amplification stage. When the two are matched, which is ideal, the reflection coefficient becomes zero.

$$\Gamma = \frac{Z_{in} - RL}{Z_{in} + RL} \tag{5.7}$$

It's assumed that the impedance of the antenna is a standard of 50 Ω. The LNA is therefore designed to match to this 50 Ω "source" impedance of the antenna, To start matching the amplification stage to the antenna it's important to know what the input impedance of the amplification system is.

5.2.1 Matching Theory

In order to match the impedance of the amplification stage to the 50 Ω impedance of the antenna there needs to be an additional network between the antenna and the amplification stage. This additional network will cause the impedance to be matched at 50 Ω when looking into the network from the antenna side. Figure 5.7 reflects this theory. In simpler terms: the matching network will cause the total impedance of the amplification stage to be matched at 50 Ω. Which is equal to that of the antenna.
However, it should be noted that typical LNA's have 4 distinctive topologies used for matching [15]. The resistor termination, the $\frac{1}{gm}$ termination, the resistive feedback, and inductive degeneration. The 4 distinctive topologies are shown in figure 5.6. The resistor termination adds noise to the signal while the $\frac{1}{gm}$ used an extra transistor. For these reasons, they aren't seen as an improvement. However, the resistive feedback and inductive degeneration topologies are good candidates when one wants to improve the proposed LNA circuit. These topologies don't use an extra matching network. These topologies were initially considered in the earliest stages of the design process. But because of the complexities, these topologies introduce they were disregarded. Some of the complexities are mentioned in the discussion part of the thesis.

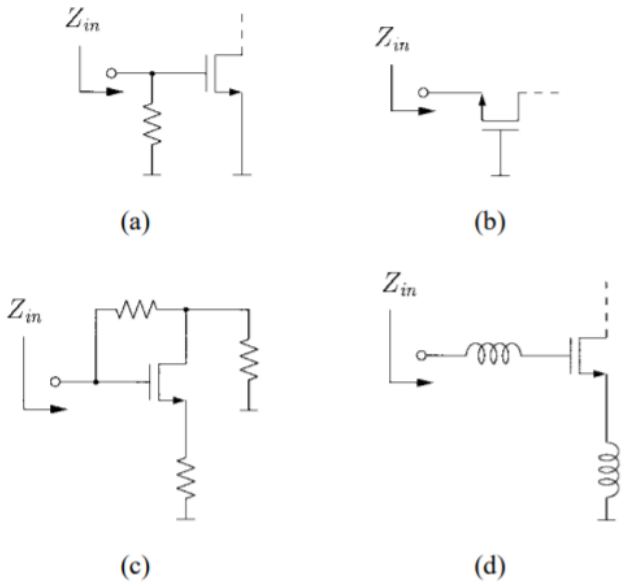


Figure 5.6: 4 distinctive topologies: (a) Resistive termination, (b) $\frac{1}{gm}$ termination, (c) Resistive feedback, (d) Inductive degeneration

5.2.2 Theoretical values

Before starting developing the matching network it's important to know the impedance of the amplification stage itself. Revisiting the pi-model in figure 5.3 it can be concluded that the input impedance of the

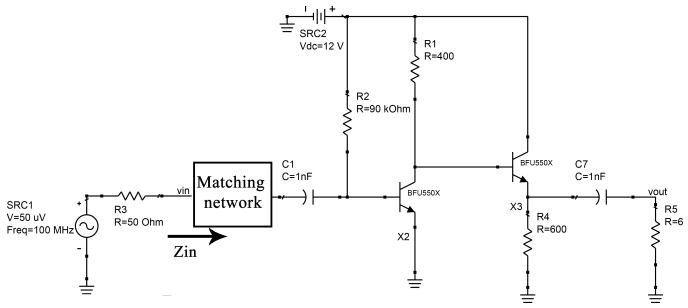


Figure 5.7: Input matching

amplifier stage is equal to RB1 and Rpi in parallel.

$$\frac{1}{Zin} = \frac{1}{RB1} + \frac{1}{R\pi} \tag{5.8}$$

$$\frac{1}{Zin} = \frac{R\pi + RB1}{RB1 \times R\pi}$$

$$Zin = \frac{RB1 \times R\pi}{R\pi + RB1} \tag{5.9}$$

$$RB1 >> R\pi$$

$$Zin = Rpi = \frac{\beta}{gm} \tag{5.10}$$

Where β is defined as

$$\beta = \frac{Ic}{Ib} \tag{5.11}$$

Filling in the values for the components an input impedance of 200 Ω is obtained. As mentioned before the used pi-model is greatly simplified and certain aspects aren't modeled. To prevent mismatch due to this simplification ADS simulation measurements and results are used in the process of matching. This because the model which is used for the simulation is much more comprehensive than the one used for hand calculations. The simulation results can be found in section 5.3.1. By adding a buffer at the end of the LNA hand calculations become even more tedious. For these reasons simulation results from ADS are used for impedance matching.

Table 5.1 gives the values and the results of derived expressions.

Parameters	Value
RB1	90 kΩ
Rload	400 Ω
Ib	125μA
Ic	11 mA
β	88
Vt	25 mV
gm	0.44 $\frac{A}{V}$
Rpi	200 Ω
Zin	200 Ω
Gain	176 ≈ 45dB

Table 5.1: Component values for the LNA

5.2.3 Matching network

The input impedance without matching according to ADS simulation results ranges from 42 to 36 Ω for the FM spectrum respectively as can be seen from graph 5.10. Matching is done with the aid of Smith charts. The reflection coefficient without matching can be found in figure 5.9. For a perfect match, the red curve needs to be in the center on the real axis of the Smith chart. This can be done by adding passive components to the circuit. It should be noted that resistors add thermal noise and will be therefore excluded from being used. The matching is done solely with inductors and capacitors. By adding inductors one can move up on the Smith chart while capacitors do the opposite. A parallel connection will cause the graph to move on the admittance lines of the Smith chart while adding in series will cause it to move on the impedance lines. To match the first step would be to move upwards towards the impedance line that intersects the real axis in the center of the Smith chart. This is done by adding an inductor in parallel to the circuit. Afterward, a second capacitor is added to the circuit to move down towards the center point. The values of these two components are based upon how much the graph needs to be moved in a specific direction. It's also dependent on the chosen frequency for which the matching is being done. Note that the impedance's of inductors and capacitors are frequency dependent. That being said a perfect match for the whole FM spectrum isn't done, instead just for one specific frequency, or a relatively small range in a best-case scenario. The chosen frequency for which matching is done is 98 MHz. This specific frequency is chosen because it's in between 88 and 108 MHz. By choosing the perfect match for 98 MHz we can have also have an optimal result for the other frequencies. The calculation can be found in equations 5.12 and 5.13. Where Y_{Lnorm} and X_{Cnorm} is the amount one moves on the normalized smith chart.

$$Y_{Lnorm} = 1.435 \tag{5.12}$$

$$X_{Lnorm} = \frac{1}{Y_{Lnorm}}$$

$$X_L = X_{Lnorm} \times 50$$

$$L = \frac{X_L}{2\pi F_o} = 56.5 \text{ nH} \approx 55 \text{ nH}$$

$$X_{Cnorm} = 0.552 \tag{5.13}$$

$$X_C = X_{Cnorm} \times 50$$

$$C = \frac{1}{2\pi F_o X_c} = 58.8 \text{ pF} \approx 60 \text{ pF}$$

The current setup (full schematic), which can be seen in figure 5.8, matched the amplification stage with two components (inductor and capacitor). In other words, the matching is done in two "steps". One could also plot a Smith chart with Q-lines(quality factor lines). By staying in a specific "Q- region" on the Smith chart the impedance of the total system will be less fluctuating.The curve in figure 5.12 can be "flattened". In other words, the impedance will deviate less aggressively when the frequency changes and a better match can be obtained for not just one small range of frequency. If one wants to stay in one specific Q-region than more "steps" are required and therefore more components making the matching network effectively larger. This is a trade-off for the proposed matching network. A trade-off between the amount of components and how well one wants to match for a frequency range.

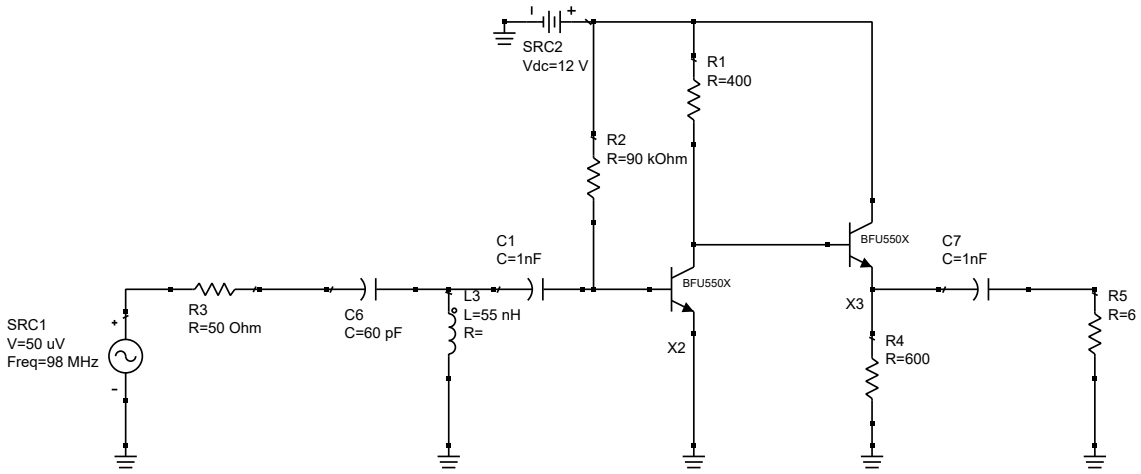


Figure 5.8: LNA with buffer and matching network

5.3 Simulation Results

5.3.1 S-Parameter simulations

The S-parameter simulations are important for the matching of the amplifier. The input reflection coefficient without any matching can be found in the Smith chart given in figure 5.9. This value is different from that of the derived theoretical value. As stated before in section 5.1.2 the π-model used is a simplified version and does not model every aspect of the transistor. And the buffer stage was also not included in the theoretical impedance calculation from 5.1.2. While ADS uses a more comprehensive model to simulate parasitic effects. This is the reason for the mismatch in the derived expression vs the simulated one. Graph 5.10 plots the input impedance against the FM-band. Figure 5.11 and 5.12 shows the matched amplifier conform the steps discussed in the previous section. One can note that at 98 MHz the match still isn't perfect. The reason for this is approximations made in the calculations. The simulation setup is given in section A.2. The S-Parameter simulation can also calculate noise figures. This is shown figure 5.13. The forward and reverse transmission can be found in figure 5.14 and 5.15. The forward transmission shows how much the incoming signal is amplified while the reverse transmission or isolation is a measure of how well a signal applied to the device output is "isolated" from its input. The input in case of the lNA is the antenna.

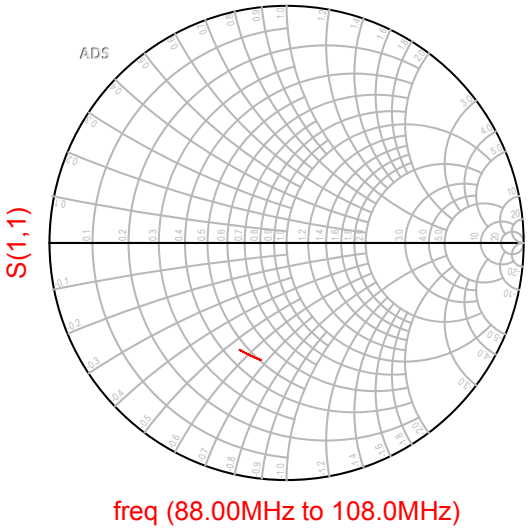


Figure 5.9: Reflection coefficient without impedance matching network.

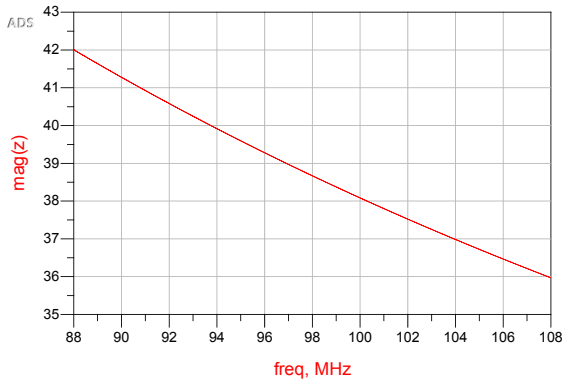


Figure 5.10: Input impedance against FM frequency band without impedance matching network

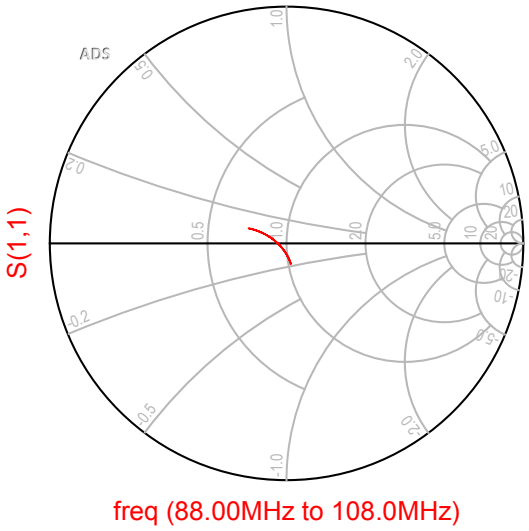


Figure 5.11: Reflection coefficient with impedance matching network.

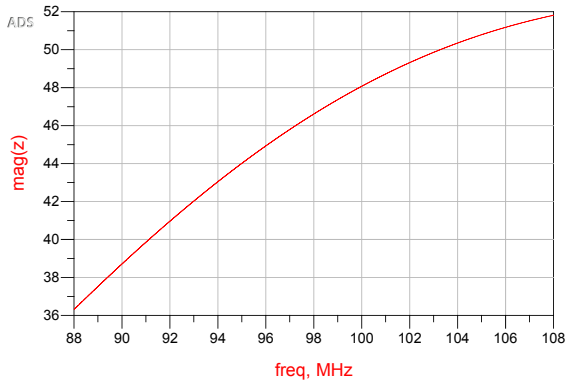


Figure 5.12: Input impedance against FM frequency band with matching network

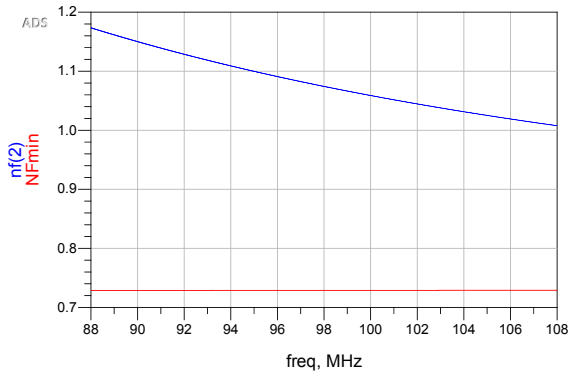


Figure 5.13: Both the minimum NF and calculated NF

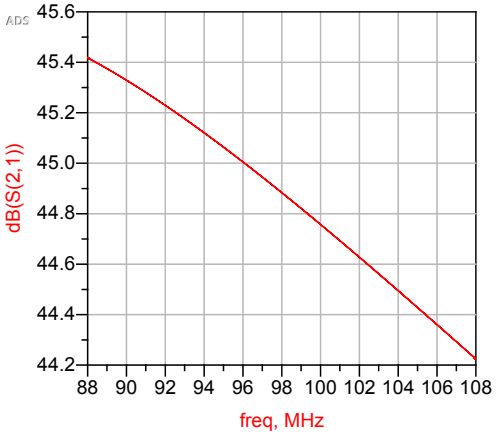


Figure 5.14: Forward transmission

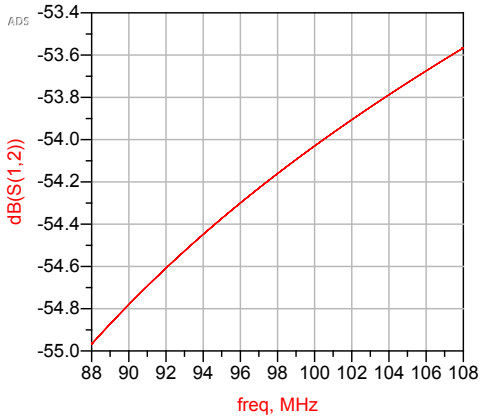


Figure 5.15: Reverse transmission

5.3.2 Transient simulations

Transient simulations are simulations in time domain. The transient simulations are done with the matching network at 98 MHz. The simulation setup can be found section A.2.The gain in this graph is approximately 30 or approximately 29 dB.

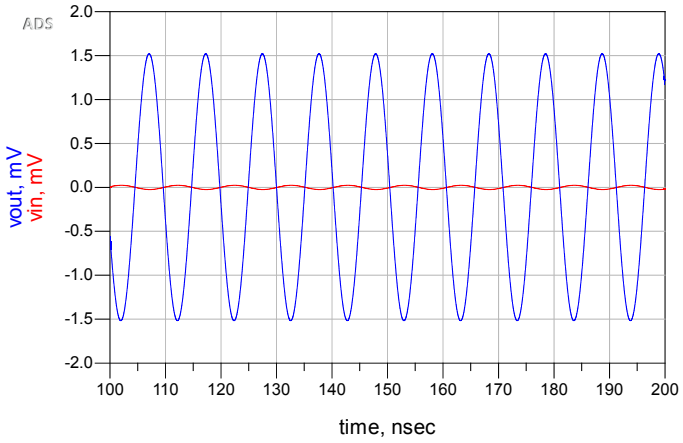


Figure 5.16: Both input voltage and output of the LNA plotted against time

5.3.3 Harmonic balance simulations

For the harmonic balance simulations the gain and the impedance over the frequency range are plotted in figure 5.18 and 5.17.

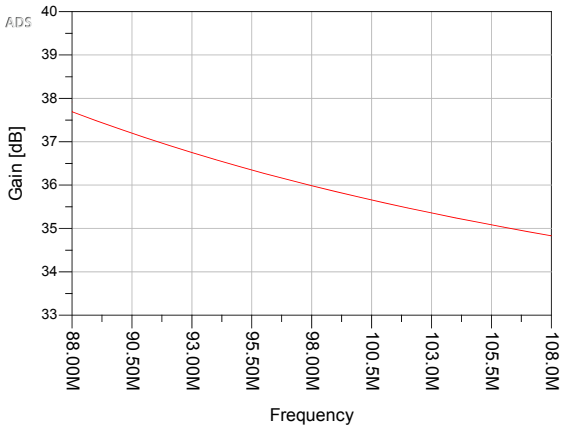


Figure 5.17: Gain against frequency

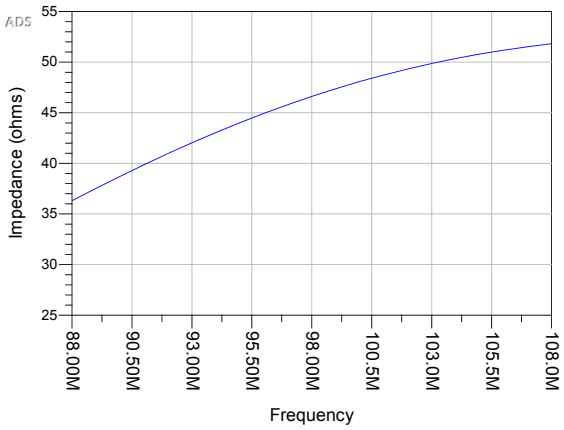


Figure 5.18: Input impedance against frequency

Chapter 6

Creating a prototype

6.1 Power amplifier

6.1.1 Measurement setup

A prototype for the PA has been constructed, it is shown in figure 6.1. A schematic overview of the testing setup is shown in figure 6.2, and the actual setup can be seen in figure 6.4.

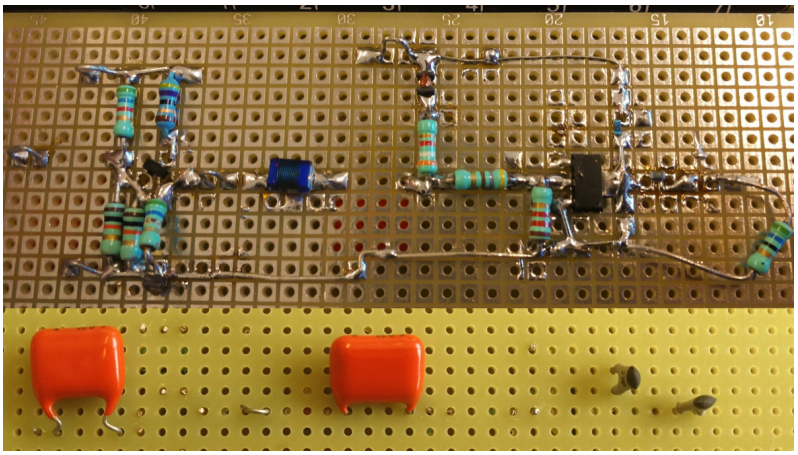


Figure 6.1: Prototype version of the PA, front and backside

6.1.2 Measurement results

The results are shown in figure 6.3. At 98 MHz and 108 MHz the amplifier behaves as expected, although with a lower output power than the ideal simulations. For an 88 MHz input signal interestingly an output occurs at both half the frequency and 1.5 times the frequency, this is most likely caused by a feedback loop created by parasitics, making the circuit behave as a frequency divider.

6.2 Low noise amplifier

The prototype of the LNA is still under construction and is therefore not finished yet. Figure 6.5 shows the latest version of the prototype, The test setup which will be used for testing is shown in figure 6.6

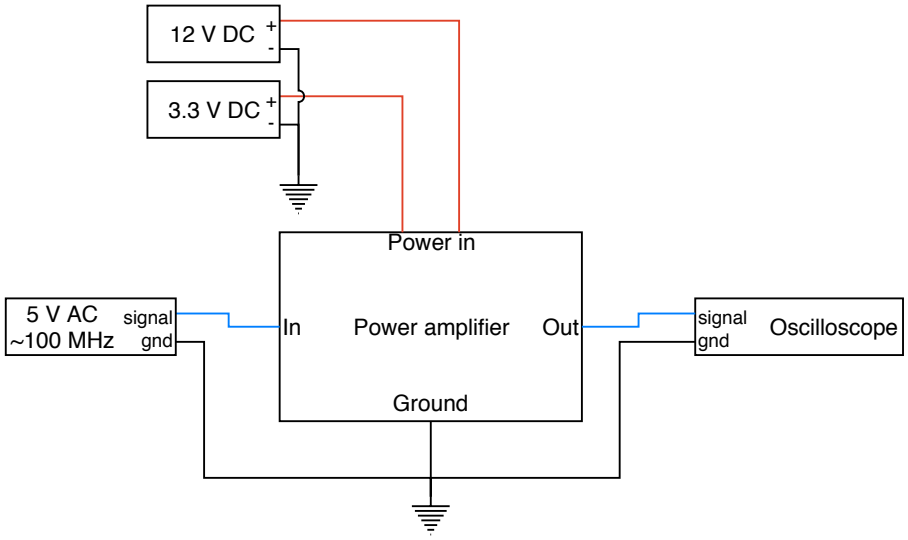
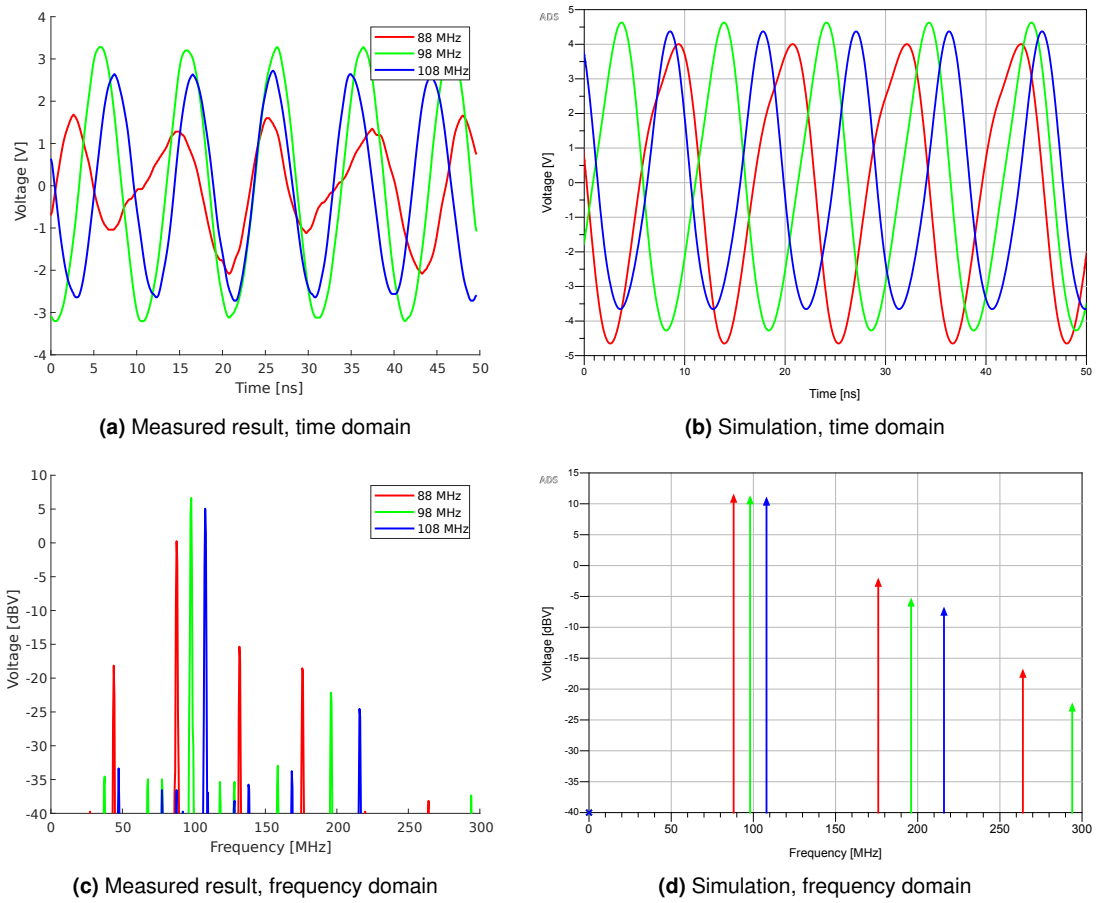


Figure 6.2: Schematic overview of the measurement setup for the PA



(a) Measured result, time domain

(b) Simulation, time domain

(c) Measured result, frequency domain

(d) Simulation, frequency domain

Figure 6.3: Measurement results compared to simulations

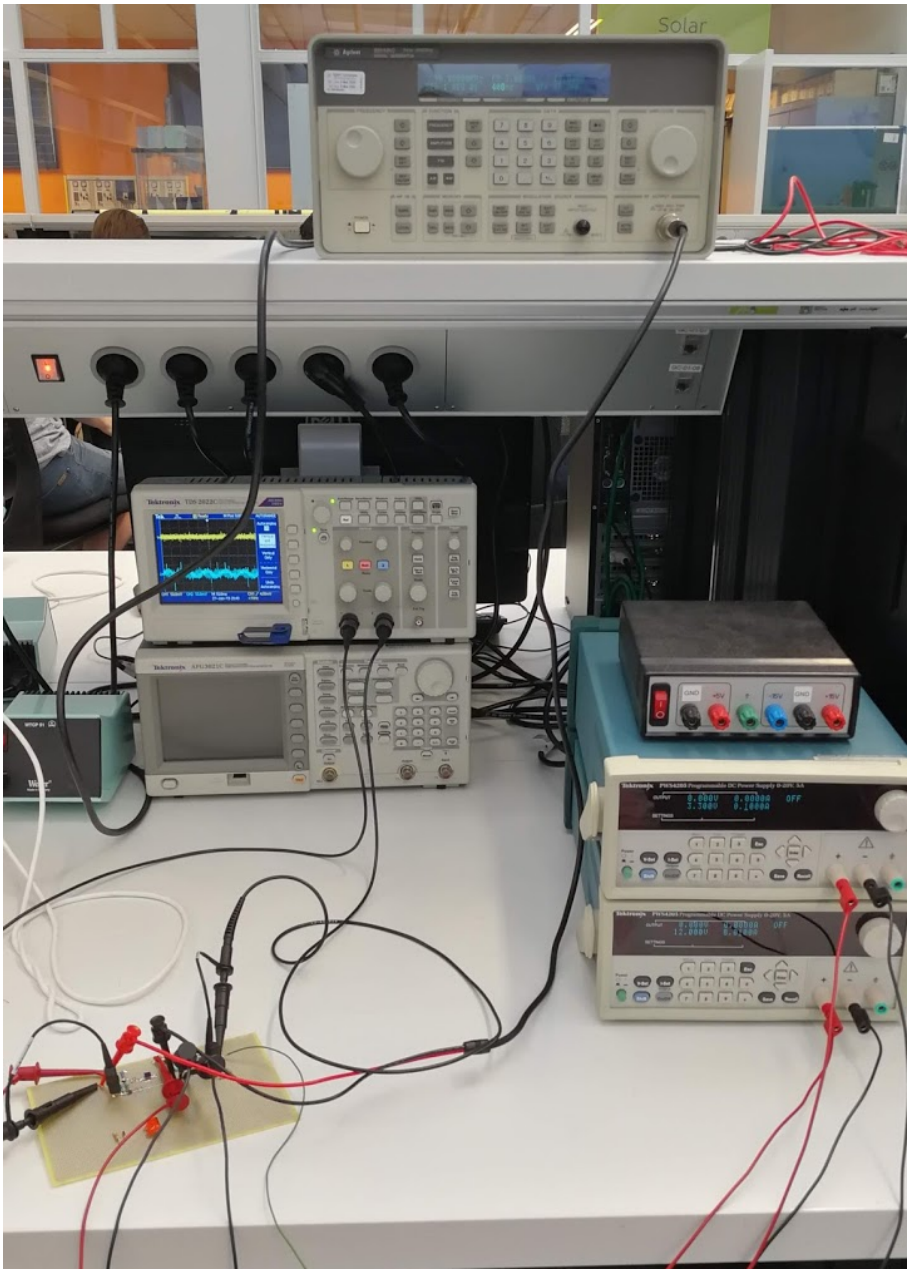


Figure 6.4: Measurement setup for the PA

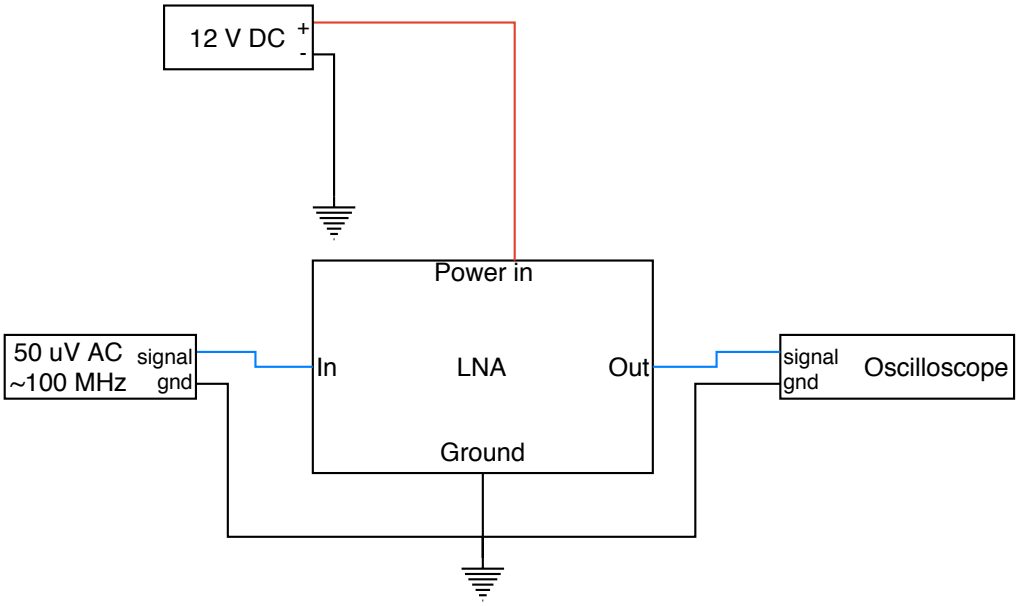


Figure 6.5: Possible measurement setup for the LNA

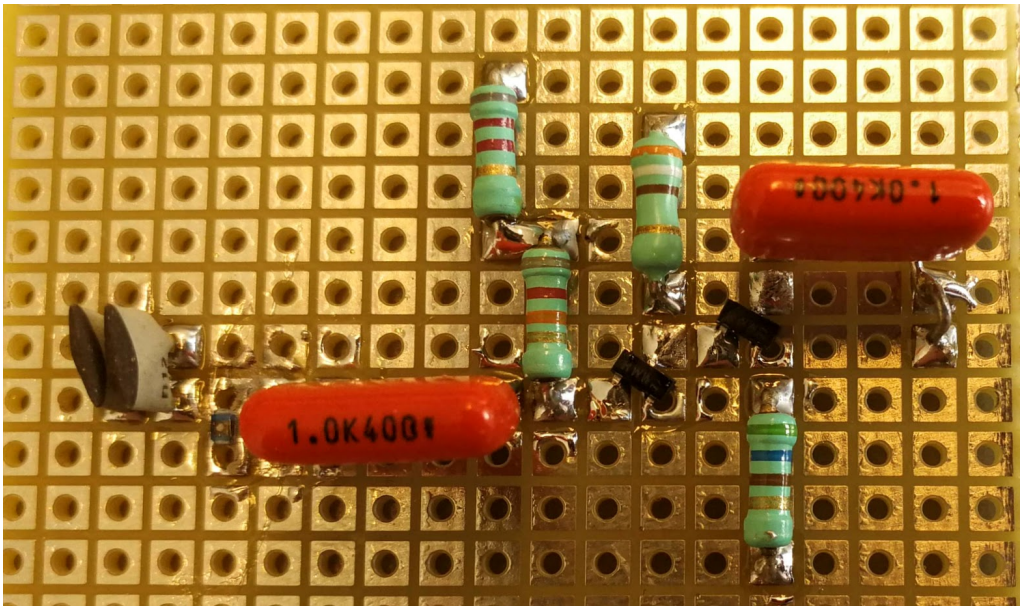


Figure 6.6: Prototype version of the LNA (unfinished)

Chapter 7

Discussion

7.1 Power amplifier

A few things could've been executed better.

The antenna is assumed to have a 50 Ω impedance, while this might be true for a specific frequency, it won't be correct for the entire frequency range. This might cause the functioning of the prototype to differ from the simulations.

While we did consider other amplifier topologies, we never simulated those other topologies. We decided it was more important to perfect one design than to spend time experimenting with a variety designs.

Better results might be achieved using a different type of transistor, however we chose to use bipolar transistors to stay in line with the rest of the design, which also uses bipolar transistors.

7.2 Low noise amplifier

The proposed LNA is in its elemental form with the gain stage and matching stage seen as two different sub-modules. As stated before in chapter 5.2.1 there are 4 distinctive topologies of which two could be a possible improvement on the current design. These topologies were considered. But they introduced other complexities like not getting sufficient gain . Introducing cascaded amplifiers to solve this issue only increased the complexity of the LNA. Time being a valuable resource during the whole project it was necessary to make comprises with the design and fall back to the current LNA design.

Another fact worth mentioning is that the impedance matching is sub-optimal for frequencies deviating from 98 MHz. Because of the fact that the prototype isn't finished yet and no testing have been done as of when this thesis was written, there is no way to tell whether or not the matching is good enough and what its influence is on the incoming signal. An improvement could be implementing the matching stage with smaller steps as described in section 5.2.3. But this is a trade-off with having more components for a better match or fewer components for a suboptimal match. Pricing wasn't a requirement for the design but one can imagine scenarios where keeping design below a certain threshold is a must.

Chapter 8

In conclusion

8.1 The power amplifier

From the results in section 3.5 it can be concluded that the amplifier can deliver a large enough output (186 mW $\gg$ 11 nW) given the specified input signal. The prototype functions as expected for the higher range of the desired bandwidth, for lower frequencies the prototype still functions, but worse than expected. Although the requirement of a 12 V supply voltage hasn't fully been met (a 3.3 V source is also needed), this could still be solved with a voltage dropping circuit, using for example a zener diode.

The entire schematic of the transmitter can be found in figure 8.1.

8.2 LNA Conclusion

Based on simulation results the obtained (figures 5.14, 5.16,5.17) gain was higher than the set requirement of 15 dB. The second required being matching with a source impedance of 50 Ω was met for a small range of frequencies and sub-optimal matching for the rest of the FM-band (figures 5.18 5.11 5.12), Finally according to simulations the NF obtained was lower than the set value of 2 dB (figure 5.13). Based on the results one can finally conclude that the set requirements where met .The LNA implemented in the receiver can be found in figure 8.2.

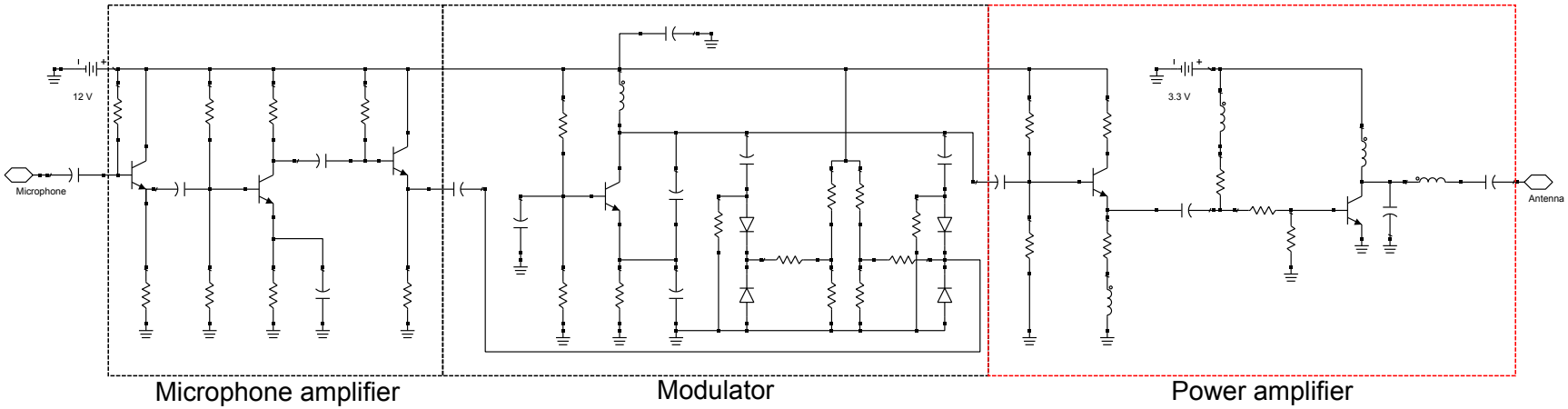


Figure 8.1: The complete transmitter schematic, the PA is marked in red

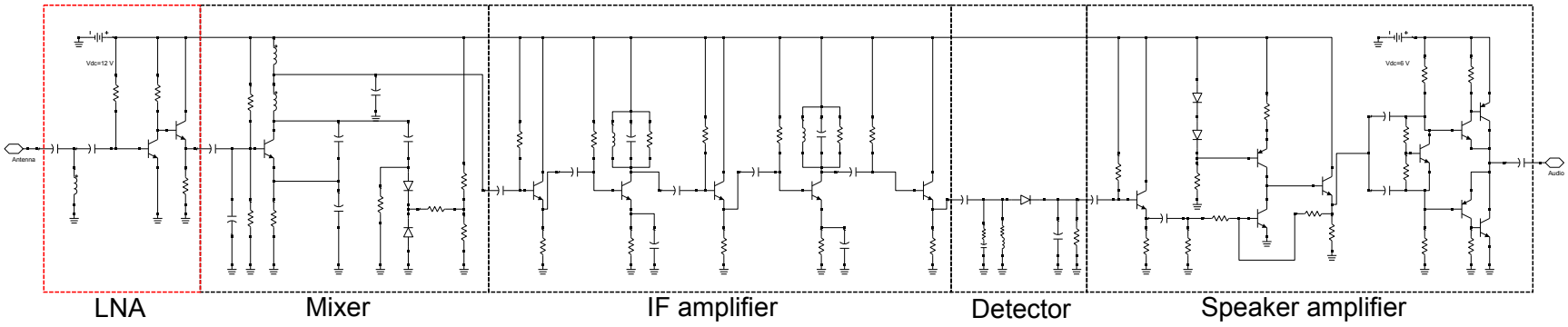


Figure 8.2: The complete receiver schematic, the LNA is marked in red

Appendices

Appendix A

LNA

A.1 Typical values for LNA

Author	NF (dB)	Gain (dB)	Sup.Voltage (V)	GHz	Technology
Meyer [16]	2.2	16	5	0.9	BiCMOS
Shaeffer [16]	3.5	22	1.5	1.5	CMOS
Fouad [16]	1.87	14.3	2	1.0	Bipolar
Razavi [14]	2	15	N/A	N/a	N/A

Table A.1: typical values for the LNA

A.2 Simulations

A.2.1 S-Parameter

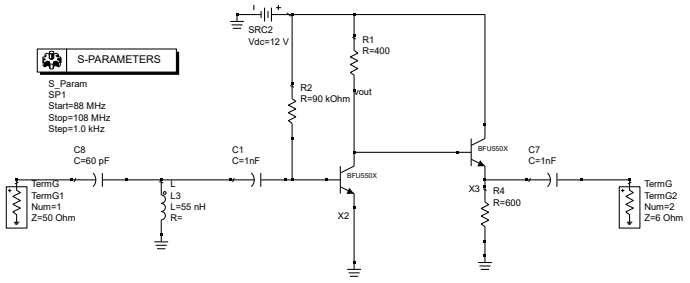


Figure A.1: S-Parameter simulation setup

A.2.2 Transient

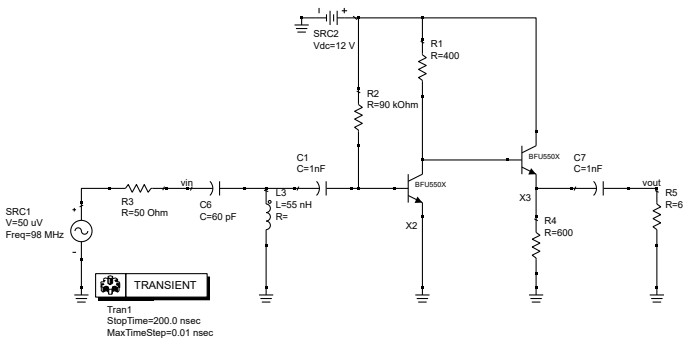


Figure A.2: Transient simulation setup

A.2.3 Harmonic Balance

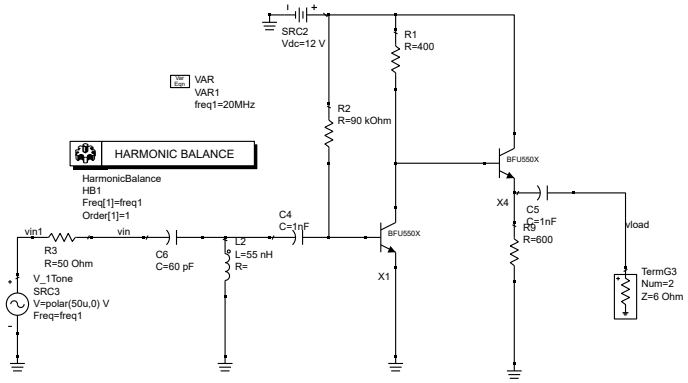


Figure A.3: Harmonic balance simulation setup

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