An Ultra-Low-Power, Low-Voltage Electronic Audio Delay Line for Use in Hearing Aids

L. P. L. van Dijk, A. C. van der Woerd, J. Mulder, and A. H. M. van Roermund

***Abstract*—In this paper, the design of an electronic audio delay line, realized with a second-order all-pass filter, is presented. The designed filter is primarily intended for use in hearing aids, to provide directivity by a specially designed microphone array. The filter operates at a supply voltage of as low as 1.8 V. The simulated and measured total quiescent current is 0.9 μA. Owing to current companding and class-AB operation, the dynamic range is 62 dB at a total harmonic distortion (THD) below 7%, i.e., at maximum output. The delay time is adjustable by control currents. The filter has been integrated in a standard bipolar process. The total measured delay time of the all-pass filter is approximately 110 μs over a bandwidth of 4 kHz.**

***Index Terms*—Active filters, biomedical sensors, low power, low voltage.**

I. Introduction

RESEARCH in directional hearing aids has clearly shown that it is possible to realize very well-functioning devices based on a microphone array and several delay lines. Medical tests with people who are hard of hearing have revealed that speech intelligibility is almost completely recovered with use of such apparatus [1].

The final goal of this long-term project, i.e., the development of a directional adapter for hearing aids, is to house all electronics and the microphones in a feather of a pair of spectacles, as depicted in Fig. 1. As shown, the adapter will be fully self-supporting. A feasibility study of the complete power consumption has indicated that one delay line must consume less than 3 μA. The project has started with the design of a suitable delay line. The total delay time is approximately 440 μs as the length of a feather is approximately 12 cm. Since five microphones will be implemented, we need four delay lines, each with a delay of 110 μs.

II. Design of a Suitable Audio Delay Line

From the foregoing sections we see that suitable audio delay lines must have very small dimensions and use minimum power. Despite the typical problems with all-pass filters, i.e., sensitivity to parasites, etc., the use of such filters as delay lines has appeared to be the most promising. After a literature investigation, we found that a log-domain or translinear circuit would be suitable in the design of a delay line which meets our specifications [3]–[5]. To increase the dynamic range versus the quiescent current, we chose for a class-AB implementation. Section III deals with the theory and the design of the all-pass filter. In Section III-C the biasing is discussed in more detail.

Manuscript received March 11, 1997; revised July 25, 1997.

The authors are with the Department of Electrical Engineering, Delft University of Technology, 2628 CD Delft, The Netherlands.

Publisher Item Identifier S 0018-9200(98)00730-6.

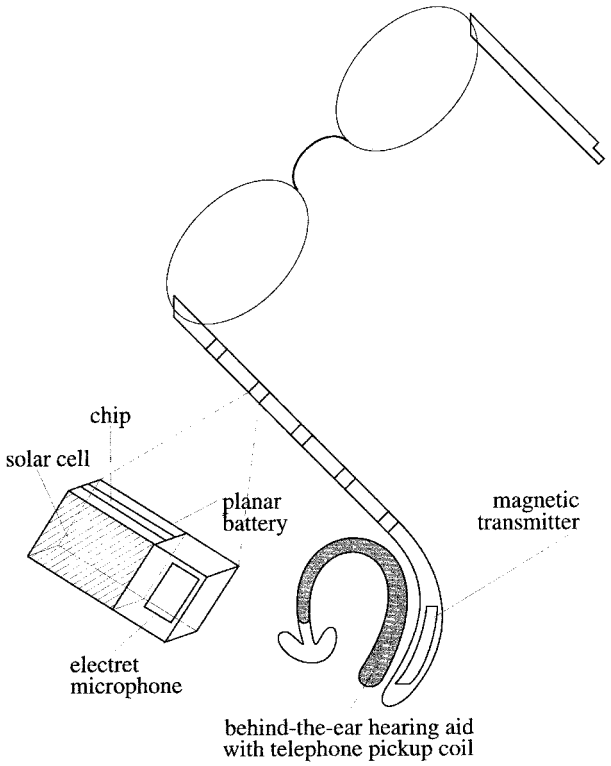

Fig. 1. The directional hearing aid adapter in a pair of spectacles.

Section IV compares the requirements with the simulations and the measured results.

A. Theory

As known, the transfer function of a second-order all-pass filter can be derived from the transfer function of a second-order bandpass filter [2], as is easily demonstrated in (1), where Q is the quality factor and ω_0 is the center frequency of the bandpass filter

$$H(s) = -\frac{s^2 - (\omega_0/Q)s + \omega_0^2}{s^2 + (\omega_0/Q)s + \omega_0^2} = 2\frac{(\omega_0/Q)s}{s^2 + (\omega_0/Q)s + \omega_0^2} - 1. \tag{1}$$

The left-hand side of (1) represents the desired transfer function, apart from a sign inversion. Apart from the factor of two and the subtraction of one, the right-hand side contains the transfer function of a second-order bandpass filter. The group delay is found by differentiating the phase response $\beta(\omega)$ of (1) to the angular frequency

$$\tau_{\mathrm{gd}} = -\frac{d\beta(\omega)}{d(\omega)} = \frac{2Q\omega_0\left(\omega^2 + \omega_0^2\right)}{Q^2\left(\omega^2 - \omega_0^2\right)^2 + \omega^2\omega_0^2} \tag{2}$$

where Q has to equal $1/\sqrt{3}$ for a maximally flat delay.

0018–9200/98$10.00 © 1998 IEEE

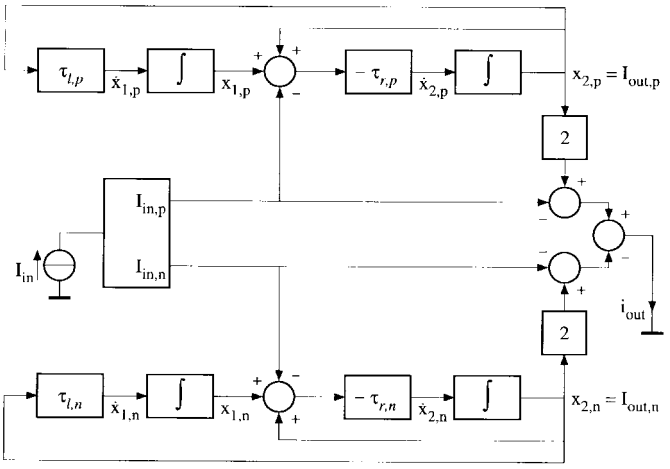

Fig. 2. Block diagram of the second-order all-pass filter.

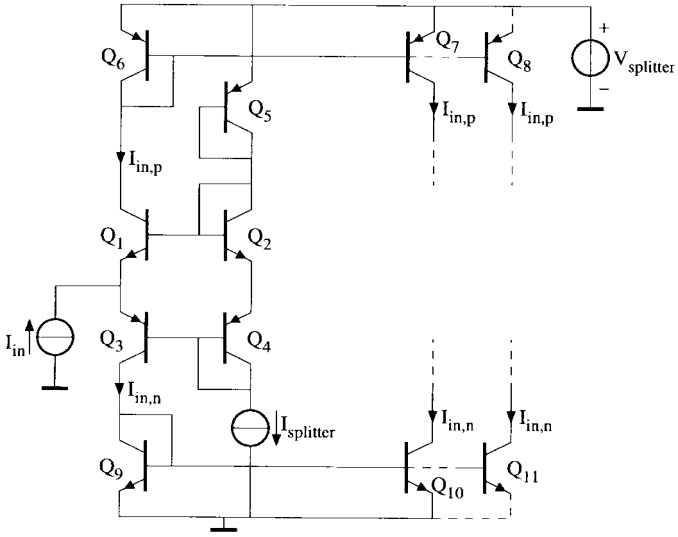

Fig. 3. Translinear current splitter.

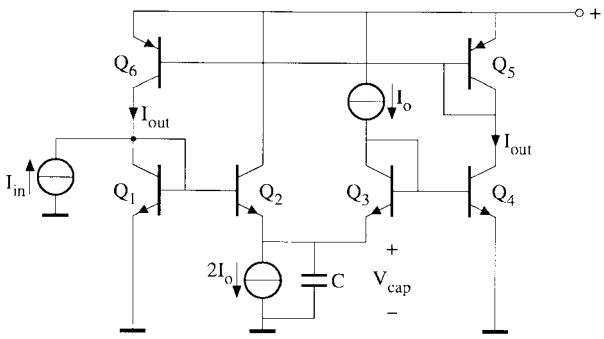

Fig. 4. Translinear integrator.

B. Implementation at Circuit Level

Fig. 2 is a direct Class-AB implementation of (1) and (2). The input current $I_{\rm in}$ is split into two, always positive, components $I_{{\rm in},p}$ and $I_{{\rm in},n}$. The output currents $I_{{\rm out},p}$ and $I_{{\rm out},n}$ are transformed into the output current $I_{\rm out}$. The major building blocks are the translinear current splitter and the integrators. At this point, it is important to note that we prefer no cross-coupled signal processing halves in the integrators. Although we found some in literature, it is because of the cross-coupled signal processing halves that positive feedback loops occur in those kinds of integrators. This can cause latching problems, especially in the case of mismatch or signal overload. An early realization of such an integrator has proven this.

The *current splitter* is depicted in Fig. 3. The main translinear loop in the *current splitter* is formed by $Q_1 \cdots Q_4$ and, when base currents are neglected and perfectly matched transistors are assumed, the following equations are implemented

$$I_{{\rm in},p} I_{{\rm in},n} = I_{\rm splitter}^2 \tag{3}$$

$$I_{\rm in} = I_{{\rm in},p} - I_{{\rm in},n}. \tag{4}$$

The dc source $I_{\rm splitter}$ and Q_5 ensure the complete biasing of the splitter (the latter prevents Q_1 from saturating).

The *integrator*, whose design was inspired by [5], is depicted in Fig. 4. The transistors $Q_1 \cdots Q_4$ form a translinear loop, yielding

$$(I_{\rm in} + I_{\rm out}) I_0 = I_{\rm out}\left(I_0 + C\dot{V}_{\rm cap}\right) \tag{5}$$

or, according to the voltage-definitions in Fig. 4

$$(I_{\rm in} + I_{\rm out}) I_0 = I_{\rm out}\left(I_0 + C(\dot{V}_{{\rm be},q^4} - \dot{V}_{{\rm be},q^3})\right). \tag{6}$$

We now denote the relation between the base-emitter voltage $V_{\rm be}$ and collector current I_C of a bipolar junction transistor (BJT)

$$V_{\rm be} = V_t \ln(I_C/I_S) \tag{7}$$

where I_S is the saturation current and V_t is the thermal voltage. Equations (5), (6), and (7) yield, after rewriting

$$I_{\rm out} = \frac{I_0}{CV_t} \int I_{\rm in}\, dt \tag{8}$$

where I_0 is a normalizing current which can be used to control the time constant, which can be made temperature independent by making I_0 proportional to absolute temperature (PTAT). A low-pass filter can be derived from this integrator by removing the positive feedback formed by Q_5 and Q_6. Equation (6) then becomes

$$I_{\rm in} I_0 = I_{\rm out}\left(I_0 + C\dot{V}_{\rm cap}\right) \tag{9}$$

which can be rewritten with (7) as

$$\frac{I_{\rm out}}{I_{\rm in}} = \frac{1}{1 + sCV_t/I_0} \tag{10}$$

which is the transfer function of a linear first-order low-pass filter.

For the *time constants* $\tau_{l,r}$ of the left and right hand integrators in Fig. 2, we find

$$\tau_{l,r} = \frac{I}{Q\omega_0} = \frac{C_{l,r} V_t}{I_{ol,r}} \tag{11}$$

where $C_{l,r}$ and $I_{ol,r}$ are the left- and right-hand capacitors and normalizing currents, respectively.

Combining (11) with the Q-value of $1/\sqrt{3}$, i.e., for maximally flat delay (Bessel), yields

$$\frac{I_{ol}}{I_{or}} = \frac{1}{3}\frac{C_l}{C_r}. \tag{12}$$

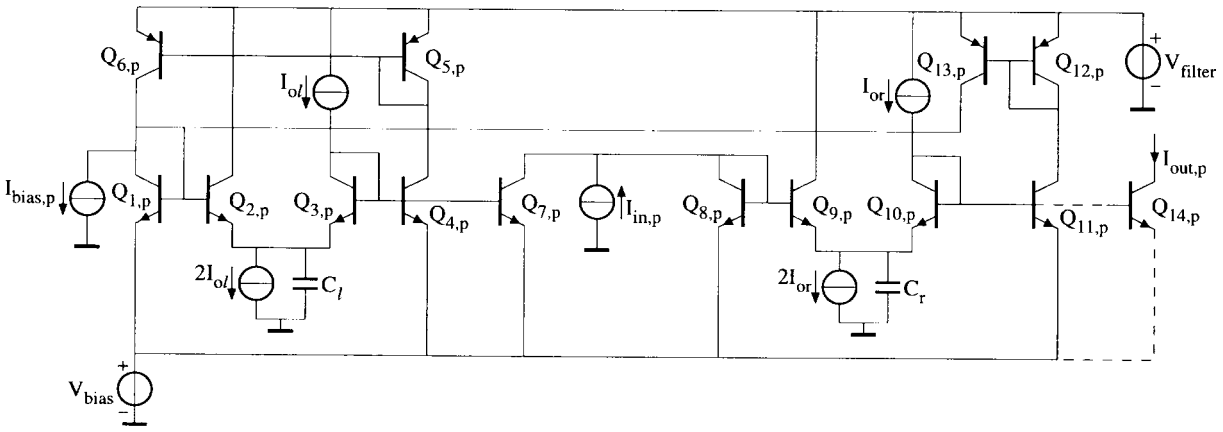

Fig. 5. One signal-processing half of the all-pass filter.

C. Biasing

In Fig. 5, one signal processing half of the class-AB all-pass filter is depicted, except for the circuitry needed to transform the output current into the output current of an all-pass filter. The biasing equations for one signal half are obtained by setting the capacitance currents and the input signal current to zero. This yields

$$(I_{q11,p} - I_{\text{bias},p} + I_{q4,p})I_{ol} = I_{q4,p}I_{ol} \tag{13}$$

$$(I_{\text{splitter}} - I_{q4,p})I_{or} = I_{q11,p}I_{ol} \tag{14}$$

where $I_{q11,p}$ and $I_{q4,p}$ are the collector currents of $Q_{11,p}$ and $Q_{4,p}$, respectively. The current sources I_{ol} and I_{or} can be used to control the time constants of the left-hand and the right-hand integrators. I_{splitter} is the quiescent current of the current splitter, it is the dc term of the currents $I_{\text{in},p}$ and $I_{\text{in},n}$. The voltage source V_{bias} makes sure that the voltages across the current sources $2I_{ol}$ and $2I_{or}$ have the right polarity. The bias source $I_{\text{bias},p}$ is needed at the input of the integrator, because otherwise the integrator could only integrate in one direction. This is because any integrator needs both a current source and a current sink at its input. In (13) and (14) we can set the values of I_{splitter} and $I_{\text{bias},p}$ such that the collector currents $I_{q11,p}$ and $I_{q4,p}$ will equal about 30 nA. This is a minimal value, because otherwise the transit frequencies of the transistors would decrease too much, resulting in serious distortion. Clearly, (13) and (14) have only one dc solution. This could not have been guaranteed if we had used cross-coupled signal processing halves.

III. Simulation and Measured Results

1) Simulation Results: The circuit has been simulated in PSPICE using parameters of the standard semi-custom BJT process from DIMES.[1] Fig. 6 shows a photomicrograph of the chip. Die size is 2.4 × 3.4 mm^2. However, later versions will be integrated in a full-custom process with much smaller dimensions. We have chosen $I_{\text{splitter}} = 70$ nA, $I_{\text{bias},p} = I_{\text{bias},n} = 20$ nA, and $I_{ol} = I_{or} = 30$ nA. The values of C_l and C_r are 60 pF and 20 pF, according to (12). Figs. 7 and 8 show the simulated time delay and the transfer, respectively.

[1]Delft Institute of Microelectronics and Sub-micron Technology.

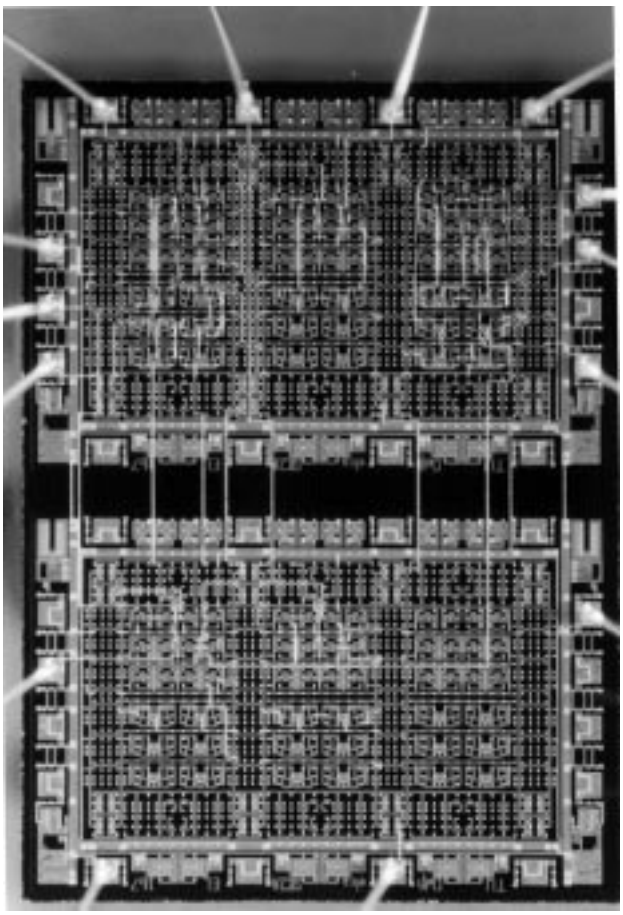

Fig. 6. Photomicrograph of the chip.

In Fig. 7 we observe considerable deviations from the ideal values. Intentional changes in parameter values have shown that this is mainly caused by the low values of the F_Ts of the lateral PNP's. Simulation results of the delay time with fast PNP's are also shown in Fig. 7. Nevertheless, the results with lateral PNP's are acceptable for the present application [1].

2) Measured Results: The delay times, the transfer, and the dynamic range have been measured. The dynamic range is defined as the rms input current at the maximal admissible total harmonic distortion (THD), i.e. 7%, divided by the equivalent A-weighted rms input noise current. The results

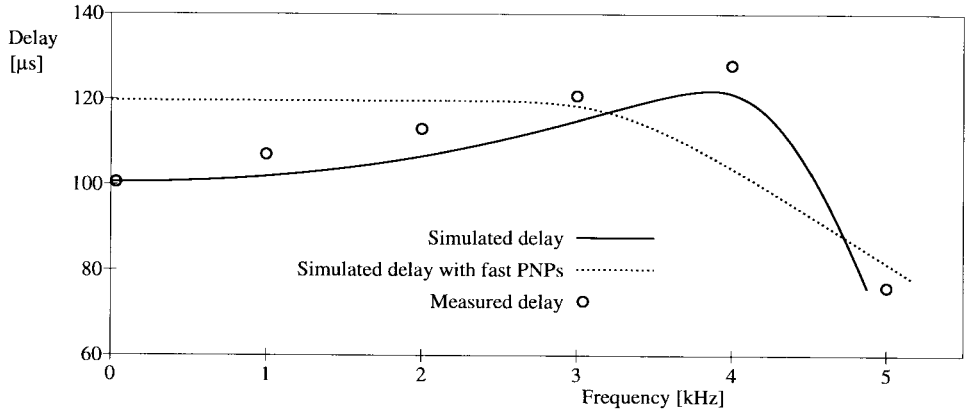

Fig. 7. Simulated and measured delay time.

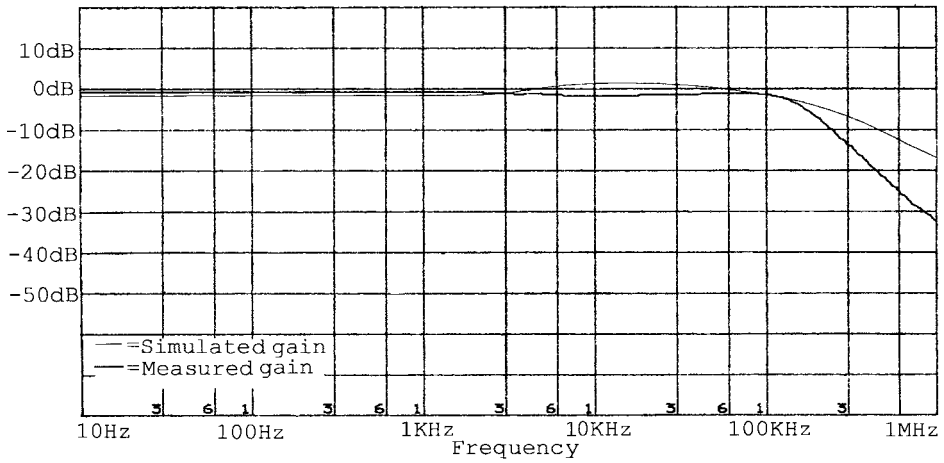

Fig. 8. Simulated and measured transfer.

TABLE I
REQUIREMENTS, SIMULATION, AND MEASURED RESULTS

Specifications	Requirements	Simulated	Measured
Supply voltage	1.2–2 V	1.8 V	1.8 V
Quiescent total supply current	<3 μA	0.9 μA	0.9 μA
Total supply current ($I_{\text{in,top}} = 200mA$)	<3 μA	1.1 μA	1.1 μA
Bandwidth	200 Hz–4 kHz	200 kHz	155 kHz
Dynamic range	>56 dB	62 dB	59 dB
Delay time	110 μs	See Fig. 7	See Fig. 7
Magnitude of the transfer function	Flat within ±1 dB in the specified bandwidth	See Fig. 8	See Fig. 8

have been added in Figs. 7 and 8 and in Table I, respectively. The deviations between the measured and the simulated bandwidth/delay time must presumably be ascribed to insufficiently accurate models. The main simulation results, together with the measured results and the requirements, are listed in Table I.

IV. CONCLUSION

In this paper, we have shown a structured way of designing a dynamic translinear second-order all-pass filter for low-voltage/ultra-low-power applications, such as directional hearing aids. The filter was derived from a second-order bandpass filter. Class-AB operation extends the dynamic range and reduces the current consumption. The resulting signal-processing halves are not cross-coupled, hence, one stable dc solution is guaranteed. The measured delay shows strong deviations from the ideal. However, the circuit was found to operate acceptably for the present application. To improve its properties, redesigns will be carried out in a BiCMOS process, employing vertical PNP's with much larger $F_T s$.

REFERENCES

[1] W. Soede, "Improvement of speech intelligibility in noise," Ph.D. dissertation, Delft University of Technology, The Netherlands, Nov. 1990.
[2] M. S. Ghausi and K. R. Laker, *Modern Filter Design*. New York: Prentice-Hall, 1981.
[3] R. W. Adams, "Filtering in the log-domain," presented at 63rd AES Conf., New York, May 1979.
[4] D. R. Frey, "Log-domain filtering: An approach to current-mode filtering, " *Proc. Inst. Elec. Eng. Pt. G*, Dec. 1993, vol. 140, pp. 406–416.
[5] J. Mulder, A. C. van der Woerd, W. A. Serdijn, and A. H. M. van Roermund, "General current-mode analysis method for translinear filters," *IEEE Trans. Circuits Syst.*, vol. 44, no. 3, Mar. 1997.