An Auto-Zero-Stabilized Voltage Buffer With a Quiet Chopping Scheme and Constant Sub-pA Input Current

Rooijers, Thije; Huijsing, Johan H.; Makinwa, Kofi A.A.

DOI
10.1109/JSSC.2021.3127462

Publication date
2022

Document Version
Final published version

Published in
IEEE Journal of Solid-State Circuits

An Auto-Zero-Stabilized Voltage Buffer With a Quiet Chopping Scheme and Constant Sub-pA Input Current

Thije Rooijers, *Graduate Student Member, IEEE*, Johan H. Huijsing, *Life Fellow, IEEE*, and Kofi A. A. Makinwa, *Fellow, IEEE*

***Abstract*— This article describes an auto-zero stabilized voltage buffer that achieves low offset and low noise with sub-pA input current. A high gain stabilization loop is used to periodically cancel the buffer's offset. The loop itself is periodically disconnected from the buffer and auto-zeroed, during which its bandwidth is reduced to reduce the associated noise folding. However, this also reduces its offset correction range, and so to avoid overloading, its initial offset is digitally trimmed. To break up the correlation between the residual low-frequency (LF) noise of the auto-zero and stabilization phases, the loop is periodically chopped, which significantly reduces the buffer's LF noise. Finally, the duty-cycle of the two phases is optimized to bring the buffer's LF noise density close to $\sqrt{2}$ times its white noise density (14 nV/$\sqrt{\text{Hz}}$), which is the fundamental limit of an AZ amplifier. The buffer also achieves a constant and low input current (0.8 pA), as well as a state-of-the-art offset (0.4 μV).**

***Index Terms*— Auto-zero, digitally assisted AZ loop, low input current, low offset, noise correlation, noise folding.**

I. Introduction

SAMPLED voltage references [1]–[4] (Fig. 1) can achieve low-power operation by storing the output of a conventional voltage reference on a hold capacitor (C_H). As shown in Fig. 1, the voltage reference then only needs to be briefly turned on (via SW_2) to refresh the voltage on C_H. To drive a load (R_L), however, this voltage must be buffered. Since the power dissipation of a buffer will typically be lower than that of a voltage reference for the same noise level, this approach delivers significant power savings. This is especially true of band-gap voltage references, which are generally not very noise efficient, because their output voltage is generated by amplifying the difference between two base–emitter voltages ΔV_{BE}, together with the associated noise, and adding it to a base–emitter voltage V_{BE} [1]–[4].

The buffer used in a sampled voltage reference must achieve low noise, low offset, and low offset-drift. To achieve this, dynamic offset compensation (DOC) techniques, such as chopping and auto-zeroing can be used. However, they require the use of input switches, whose activity gives rise to significant input current, in the order of tens of pAs [5]–[7]. As shown in Fig. 1, this current will cause the voltage stored on C_H to drift, thus limiting the allowable hold time and thus the amount of power that can be saved by duty-cycling. Furthermore, input switching activity typically causes output-referred spikes, making it difficult to interface the buffer to a subsequent ADC. Although the effect of such spikes can be mitigated by synchronizing them to the ADC's sampling clock [8], this is not feasible in a stand-alone reference.

Another application that requires low-offset amplifiers with low input currents is the readout of high impedance sensors

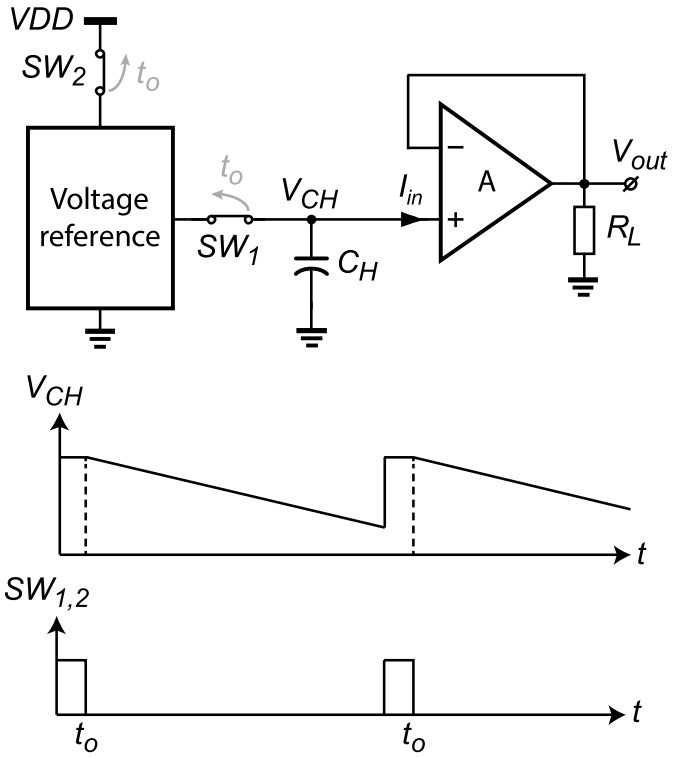

Fig. 1. Simplified block diagram of a sampled voltage reference with the waveform of the output voltage over time and the sampling switches.

Manuscript received 5 August 2021; revised 8 October 2021; accepted 29 October 2021. Date of publication 24 November 2021; date of current version 25 July 2022. This article was approved by Associate Editor Pui-In Mak. *(Corresponding author: Thije Rooijers.)*

The authors are with the Department of Microelectronics, Delft University of Technology, 2628 Delft, The Netherlands (e-mail: c.t.rooijers@tudelft.nl).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/JSSC.2021.3127462.

Digital Object Identifier 10.1109/JSSC.2021.3127462

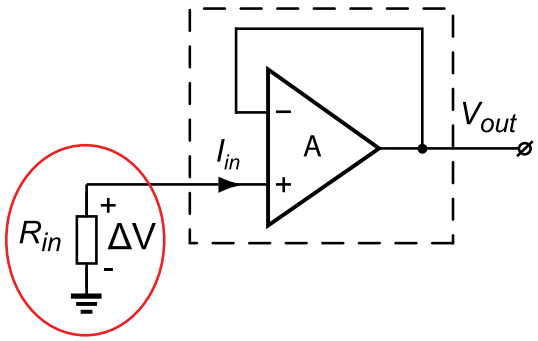

Fig. 2. High impedance sensor readout.

(Fig. 2). Such sensors, e.g., dry electrodes, photodiodes, and pH probes, can have impedances of several MΩs [9]–[10]. Input currents (I_{in}) of several pAs then lead to voltage errors (ΔV) of several μVs, thus nullifying the benefits of DOC techniques.

Previous amplifiers targeting a combination of low input current and low offset have relied on trimming to avoid the input current associated with DOC techniques. An op-amp with a single-temperature trimming scheme that corrects both V_{TH} and β mismatch of its MOSFET-based differential input pair is presented in [11]. However, its offset (30 μV) and offset drift (0.33 μV/°C) are still high compared to that of typical chopper or auto-zero amplifiers (<10 μV and <10 nV/°C). Moreover, unlike the use of chopping and auto-zeroing, the use of trimming does not mitigate $1/f$ noise.

Amplifiers with JFET input stages have low $1/f$ noise and relatively low input current [12]. However, compared to amplifiers with MOS input stages, their input current is still rather high (~10 pA), and increases exponentially with temperature, making them unsuitable for high-temperature applications. Furthermore, their offset (~150 μV) and offset drift (1.5 μV/°C) are still quite high compared to that of typical chopper or auto-zero amplifiers [13], [14].

To lower the input current of amplifiers using DOC techniques: trimming [15] and nested chopping [16] have been used. In [15], a high effective chopping frequency (4.8 MHz) was used to achieve a large glitch-free signal bandwidth. This requires trimming to lower the input current from 1.5 nA to 150 pA. Nested chopping [16] utilizes a second chopper to chop the charge injection mismatch of the first chopper. The input current of the second chopper is minimized by using a much lower chopping frequency. This reduces the overall input current, as well as the residual offset, at the expense of reducing the ripple-free bandwidth.

This article presents an auto-zero stabilized voltage buffer that achieves low input current, low offset, and low noise [17], [18]. It has an input current of 0.8 pA, state-of-the-art offset (0.4 μV), and a low-frequency (LF) noise density close to $\sqrt{2}\times$ its white noise density (14 nV/$\sqrt{\text{Hz}}$), which is the fundamental limit of an AZ amplifier [20].

The rest of the article is organized as follows. The chosen architecture and its design considerations are described in Section II. Measurement results are shown and discussed in Section III, and the article ends with conclusions.

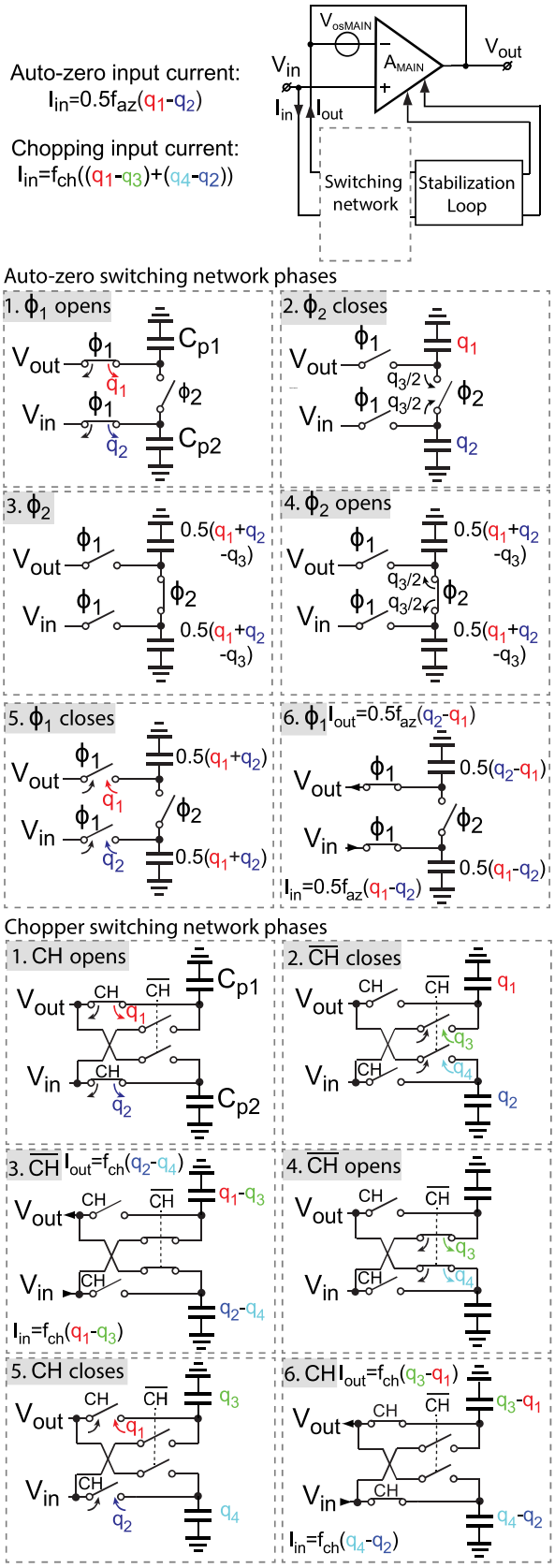

Fig. 3. Comparison of the input current of an auto-zero and a chopper amplifier.

II. Architecture Design

When the low input current is required, auto-zeroing is preferred over chopping, since it requires less input switch-

ing. This can be understood by considering the associated switching sequences in Fig. 3. The switches introduce charge injection (CI) when they open and charge absorption (CA) when they close. Only the CI/CA into/from the parasitic capacitors C_{p1} and C_{p2} are considered since the opening CI into V_{in} (and V_{out}) ideally cancels the closing CA. In the case of auto-zeroing, the CI of the opening ϕ_1 switches (q_1 and q_2) is stored on C_{p1} and C_{p2}. The ϕ_2 switch has symmetric impedances on both sides, so when it closes, its CA will equally split ($-q_3/2$) between the capacitors. The charge is shared during ϕ_2, resulting in $0.5(q_1 + q_2 - q_3)$ on each capacitor. The CI of the opening ϕ_2 switch ($q_3/2$) will then cancel $-q_3/2$, leaving $0.5(q_1 + q_2)$ on each capacitor. When the ϕ_1 switches close again, the charge on C_{p1} and C_{p2} is combined with the CA ($-q_1$ and $-q_2$), leading to an average input current (I_{in}) of 0.5 $f_{\text{az}}(q_1 - q_2)$ and output current (I_{out}) of 0.5 $f_{\text{az}}(q_2 - q_1)$. It is important to note that due to the charge sharing in ϕ_2, the CI and CA of the ϕ_1 switches cannot completely cancel.

In the case of chopping, the CI of the opening CH switches (q_1 and q_2) is stored on C_{p1} and C_{p2}. This is then combined with the CA of the closing $\overline{CH}$ switches ($-q_3$ and $-q_4$). This results in an I_{in} of $f_{\text{ch}}(q_1 - q_3)$ and I_{out} of $f_{\text{ch}}(q_2 - q_4)$ in $\overline{CH}$. Similarly, the CI of the closing CH switches ($-q_1$ and $-q_2$) gets stored and combined with the CI of the opening $\overline{CH}$ switches (q_3 and q_4). This results in an I_{in} of $f_{\text{ch}}(q_4 - q_2)$ and I_{out} of $f_{\text{ch}}(q_3 - q_1)$. After a complete chopping cycle, the result is a total average I_{in} of $f_{\text{ch}}((q_1 - q_3) + (q_4 - q_2))$ and I_{out} of $f_{\text{ch}}((q_3 - q_1) + (q_2 - q_4))$. Due to the chopping action, CI mismatch $q_1 - q_3$ gets supplied by V_{in} in $\overline{CH}$ and the opposite $q_3 - q_1$ gets supplied by V_{out} in CH, leading to incomplete cancellation. Assuming the same CI/CA mismatch for all switches and $f_{\text{ch}} = f_{\text{az}}$, the conclusion is that chopping generates four times more input current than auto-zeroing.

A simplified schematic of the proposed auto-zero (AZ) stabilized buffer is shown in Fig. 4. It consists of a three-stage buffer with a folded-cascode input stage ($G_{m\text{MAIN}}$), a folded-cascode intermediate stage with Class AB output stage (A_{OUT}), nested Miller compensation (30 and 7 pF, not shown), and Miller-zero compensation resistors (6 and 8 kΩ, not shown). The offset of the main amplifier (V_{osMAIN}) and $1/f$ noise are periodically canceled by an AZ stabilization loop consisting of an active integrator ($G_{m\text{INT}}$, $C_{\text{int11}-12}$ and $C_{\text{int21}-22}$) and two OTAs: G_{m1} and G_{m3}.

During phase ϕ_2, G_{m1} is auto-zeroed. Its input is shorted, and so its offset is converted by its transconductance ($\sim$230 μS) into an output current. This is integrated on capacitors $C_{\text{int21}-\text{int22}}$(10 pF each), leading to a correction voltage across nodes E and F. G_{m2} then converts this into a correction current that cancels V_{os1}.

Due to negative feedback, the buffer's offset appears across its input terminals. During phase ϕ_1, this is sensed by G_{m1}. Its output current is then integrated on capacitors $C_{\text{int11}-\text{int12}}$(10 pF each), resulting in a correction voltage across nodes G and H, and a corresponding cancellation current generated by G_{m3}. To achieve sub-μV offset, while generating correction voltages of several hundred millivolts, each stabilization loop should have a high (>120 dB) gain. In this work,

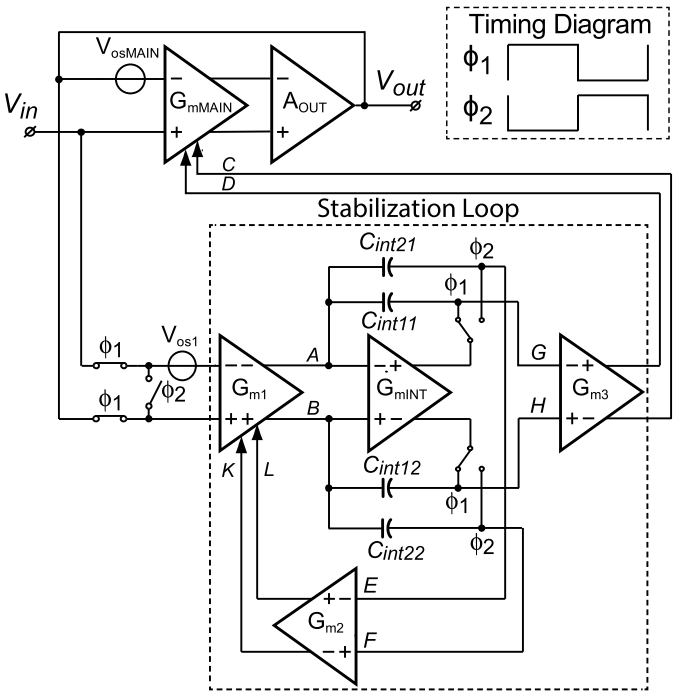

Fig. 4. Simplified block diagram of an auto-zero stabilized voltage buffer.

this is realized by multiplexing a single gain-boosted OTA ($G_{m\text{INT}}$) between the two loops, each with its own integration capacitors.

A. Noise Folding in Auto-Zero Amplifiers

The main drawback of auto-zeroing is that it causes undersampled thermal noise to fold back to low frequencies [19]. As a result, the LF noise density after auto-zeroing is typically larger than the original thermal noise density. The amount of noise folding is determined by the ratio of the bandwidth of the auto-zeroing loop (BW_{AZ}) and the auto-zeroing frequency (f_{AZ}). To achieve low input current, f_{AZ} should be as low as possible, i.e., somewhat higher than the $1/f$ corner frequencies of G_{m1} and $G_{m\text{MAIN}}$.

During the AZ phase ϕ_2, BW_{AZ} is given by [20]

$$\text{BW}_{\text{AZ}} = \frac{G_{m2}}{2\pi\, C_{\text{int21}-\text{in22}}} \tag{1}$$

where G_{m2} is the transconductance of G_{m2} and $C_{\text{int21}-\text{int22}}$ are the individual values of the corresponding integration capacitors. During phase ϕ_1, BW_{AZ} is determined by the transconductances of $G_{m\text{MAIN}}$, G_{m1}, and G_{m3}. To equalize their noise contributions, the transconductances of $G_{m\text{MAIN}}$ and G_{m1} are made the same, as are the transconductances of G_{m2} and G_{m3}. In this case, the bandwidth of the AZ loop can be expressed as

$$\text{BW}_{\text{AZ}} = \frac{G_{m3}}{2\pi\, C_{\text{int11}-\text{in12}}} \tag{2}$$

where G_{m3} is the transconductance of G_{m3} and $C_{\text{int11}-\text{int12}}$ are the values of the corresponding integration capacitors.

Limiting the bandwidth of the stabilization loop, therefore, requires either large integration capacitors or small transconductances (G_{m2} and G_{m3}). The latter approach is the most attractive since it has the least impact on the chip area. In a

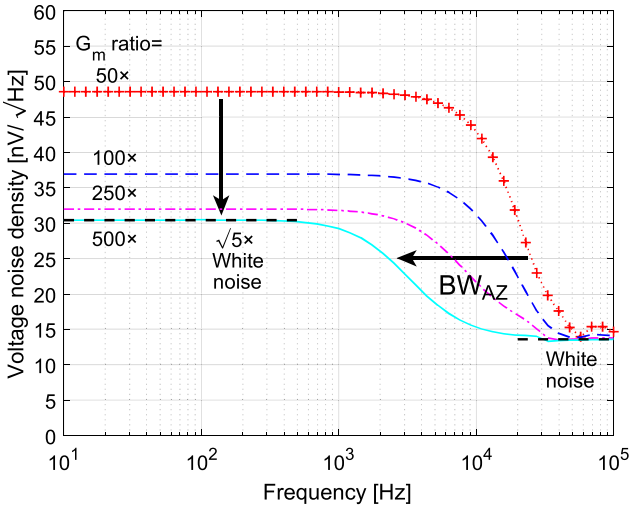

Fig. 5. Simulated voltage noise densities for a fixed $f_{AZ} = 15$ kHz and different transconductance (G_m) ratios of G_{m1} & G_{mMAIN} and G_{m2} & G_{m3}, respectively (50×, 100×, 250×, and 500×).

well-optimized design, the buffer's input-referred voltage noise density will then be determined by G_{mMAIN} ($=G_{m1}$), and so for a given integration capacitance, the LF noise density due to folding will be inversely proportional to the G_m ratio $\alpha = G_{mMAIN}/G_{m3}$ ($= G_{m1}/G_{m2}$).

Fig. 5 shows the simulated input-referred voltage noise density of the buffer for a fixed G_{mMAIN} (=230 μS), integration capacitors (10 pF), and $f_{AZ} = 15$ kHz but different gm ratios. As the gm ratio increases, the bandwidth BW_{AZ} decreases, the noise folding decreases, as does the voltage noise density at low frequencies. At large G_m ratios, however, the voltage noise density eventually stops decreasing and converges to a limit. As will be shown later, this limit is equal to $\sqrt{5} \times e_n$, where e_n is the voltage noise density associated with G_{mMAIN}. From Fig. 5, it can be seen that the gm ratio has to be at least 500× to reach this limit.

B. Digitally Assisted Auto-Zero-Stabilized Loop

Using a gm ratio of 500× means that the combined offset of G_{mMAIN} and G_{m1} will be amplified by 500× at the output of the integrator. The maximum offset voltage that can be corrected by the stabilization loop is then limited to $V_{swing}/500$, where V_{swing} is the integrator's maximum output swing. In this work, $V_{swing} \sim \pm 0.6$ V, which corresponds to a maximum correctable offset voltage of ±1.2 mV. From Monte-Carlo simulations, however, the expected offsets of G_{m1} and G_{mMAIN} are about 1.8 mV (6σ). On top of this, offset drifts of several hundreds of μVs may be expected over the intended operating temperature range (−40 to 85 °C) [11].

In prior work [20], an additional g_m stage driven by a voltage derived from an on-chip bandgap reference was used in order to trim the initial offset. In [21], a digitally assisted calibration loop is used to lower the ripple of a chopper amplifier. In this work a similar approach is used, where the initial offset of both G_{mMAIN} and G_{m1} is trimmed at startup by a digital AZ loop, to handle worst-case offset and drift levels. As shown in Fig. 6, this consists of a comparator,

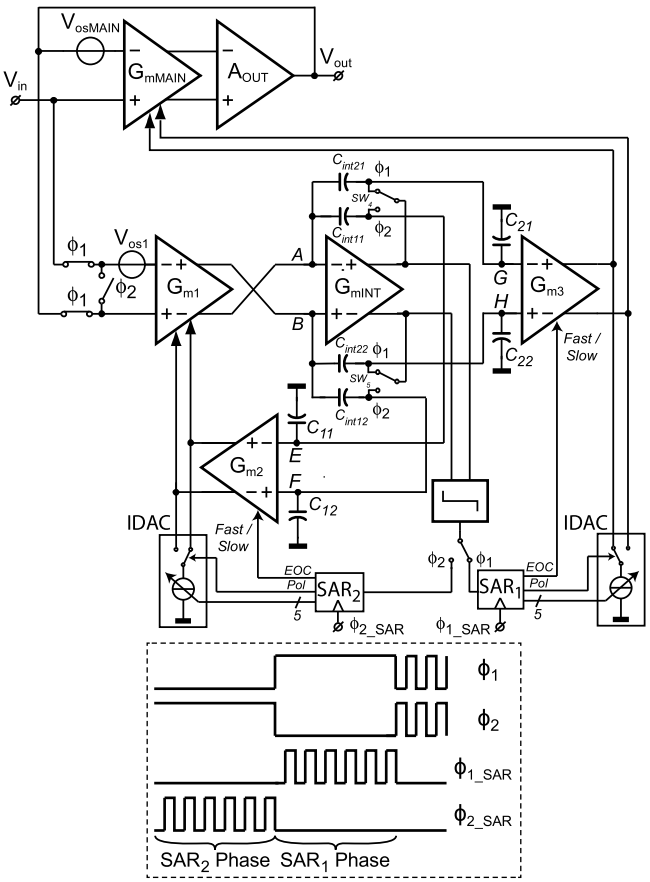

Fig. 6. Digitally assisted auto-zero-stabilized loop.

a successive approximation register (SAR), and two current DACs (IDACs) in parallel with the outputs of G_{m2} and G_{m3}. At startup, G_{m1} is first auto-zeroed by shorting its inputs and using a comparator to sample the integrator output and thus detect its offset polarity. This information is used to update the SAR, whose output drives the IDAC. Next, G_{mMAIN} is auto-zeroed in the same way by sensing its offset at the input of G_{m1} due to the feedback. As a result, the stabilization loop only has to cancel the offset drift and the residual offset corresponding to the LSB of the IDAC.

To ensure fast settling after each bit trial, the auto-zeroing bandwidth BW_{AZ} is temporarily increased. This is achieved by increasing the transconductances of G_{m2} and G_{m3} by ~4× during the operation of the digital AZ loop. This is implemented by switching both the bias current and the degeneration of G_{m2} and G_{m3} (Fig. 7). After the SAR bits are fixed, BW_{AZ} is decreased (via the end of conversion (EOC) bit) and the analog stabilization loop is enabled.

For robustness, the 5 bit IDAC is slightly over-designed, with the maximum current of 1 μA corresponding to an offset of 4.3 mV. Its MSB then corresponds to an offset of 2.5 mV, while its LSB corresponds to roughly 150 μV. A polarity bit is used to steer the DAC current to the appropriate output, and thus compensate for both positive and negative offsets.

Since the offsets of G_{m1} and G_{mMAIN} are amplified by the G_m ratio, the offset of the comparator can be quite relaxed. During startup, the G_m ratio is about 120, which means that the LSB of the IDAC corresponds to an integrator output of

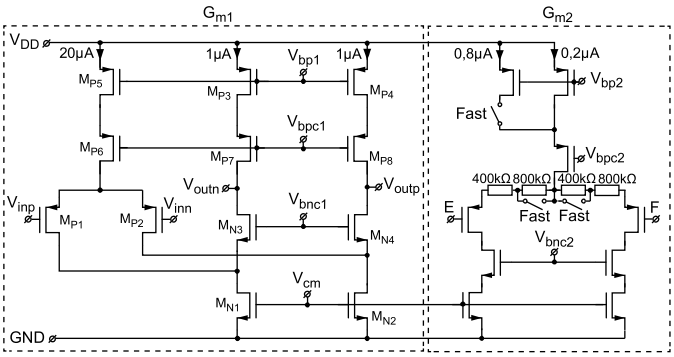

Fig. 7. Simplified schematic of $G_{m1}/G_{m\mathrm{MAIN}}$ and G_{m2}/G_{m3}.

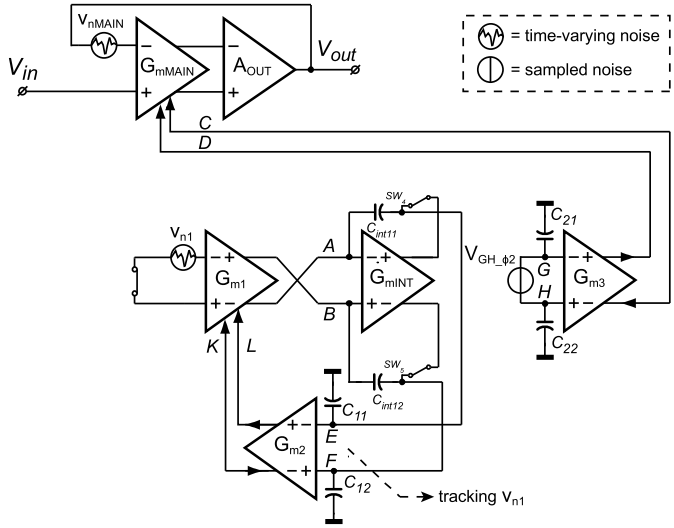

Fig. 8. Noise sources of the auto-zero stabilized voltage buffer in phase ϕ_2.

18 mV. This is much greater than the simulated comparator offset (5 mV).

A further benefit of the digital AZ loop is that it reduces the amplitude of the switching spikes associated with the multiplexed operation of the integrator. It does this by reducing the integrator's output swing, which in turn, reduces the charge injection mismatch of its output switches. It also reduces the transient currents required to drive the integrator's load capacitors to the two different offset levels of G_{m1} and $G_{m\mathrm{MAIN}}$. Due to the 500 × G_m ratio, any spikes that still appear on nodes G and H will be attenuated by 500× when referred to the output.

C. Low-Frequency Noise Analysis

As shown in Fig. 5, even after minimizing $\mathrm{BW_{AZ}}$, the LF noise density is still limited to about $\sqrt{5}\times$ the white noise level, which is higher than the $\sqrt{2}\times$ fundamental limit. To understand the reasons for this, in this section, the proposed amplifier's LF noise performance will be analyzed. At first, it will be assumed that all noise sources are uncorrelated. All noise sources refer to voltage noise densities, and capitalization will be used to denote sampled sources, while lowercases will be used for time-varying sources.

In phase ϕ_2(Fig. 8), the input of G_{m1} is shorted and the voltage across nodes E and F tracks the (500× amplified) offset. It also tracks the noise of G_{m1} (v_{n1}). At the end of phase ϕ_2, this noise will be sampled across E and F ($V_{n1\mathrm{EF}}$) and held there during the following ϕ_1 phase.

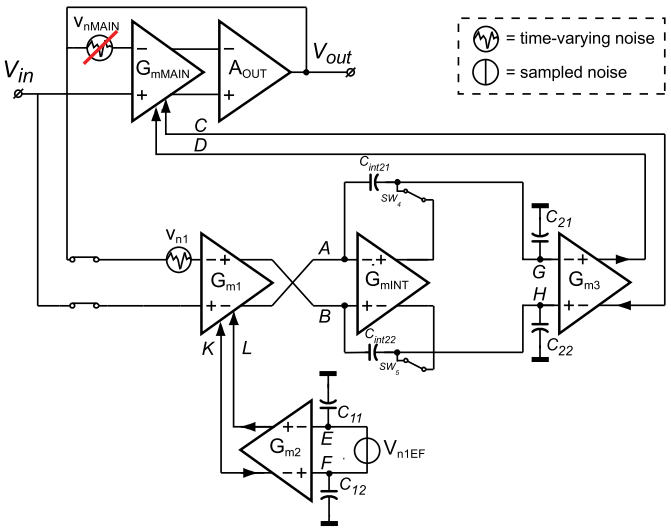

Fig. 9. Noise sources of the auto-zero stabilized voltage buffer in phase ϕ_1.

In phase ϕ_1 (Fig. 9) the voltage across node G and H tracks and cancels the noise of $G_{m\mathrm{MAIN}}$ ($v_{n\mathrm{MAIN}}$), in the same way as its offset. This is done by G_{m1}, whose offset is still being nulled by the voltage across E and F. This means that the voltage across G and H is the sum of the voltage needed to track the time-varying noise sources $v_{n\mathrm{MAIN}}$ and v_{n1}, and the sampled noise from E and F ($V_{n1\mathrm{EF}}$), which are both amplified by α. As a result, the noise density across G and H during phase ϕ_1 can be expressed as

$$v_{\mathrm{GH\_}\phi 1} = \alpha\sqrt{v_{n\mathrm{MAIN}}^2 + v_{n1}^2 + V_{n1\mathrm{EF}}^2}. \tag{3}$$

Assuming that the AZ stabilized loop has enough gain, it will completely cancel the LF noise of $G_{m\mathrm{MAIN}}$, and so during ϕ_1 the buffer's output-referred noise density, referred to V_{out}, will be given by

$$v_{\mathrm{out\_}\,\phi 1} = \sqrt{v_{n1}^2 + V_{n1\mathrm{EF}}^2} = \sqrt{2}e_n. \tag{4}$$

This shows that in phase ϕ_1 the buffer's LF output-referred noise density is fully determined by the noise of G_{m1}, which is also in good agreement with the results of Pnoise simulations.

In phase ϕ_2 (Fig. 8), the noise across G and H due to the contributions of $v_{n\mathrm{MAIN}}$, v_{n1}, and $V_{n1\mathrm{EF}}$ will be frozen. This leads to a total noise density across G and H during phase ϕ_2 of

$$V_{\mathrm{GH\_}\phi 2} = \alpha\sqrt{V_{n\mathrm{MAINGH}}{}^2 + V_{n1\mathrm{GH}}{}^2 + V_{n1\mathrm{EF}}{}^2} \tag{5}$$

where $V_{n\mathrm{MAINGH}}$ and $V_{n1\mathrm{GH}}$ are the sampled noise sources across G and H from $v_{n\mathrm{MAIN}}$ and v_{n1}, respectively. Referred to the buffer's output, these contributions across G and H add to the noise $v_{n\mathrm{MAIN}}$, and so the buffer's output-referred noise density in phase ϕ_2 is given by

$$v_{\mathrm{out\_}\phi 2} = \sqrt{v_{n\mathrm{MAIN}}^2 + V_{n\mathrm{MAINGH}}^2 + V_{n1\mathrm{GH}}^2 + V_{n1\mathrm{EF}}^2} = 2e_n. \tag{6}$$

This result shows that in phase ϕ_2 the buffer's LF output-referred noise is equally determined by G_{m1} and $G_{m\mathrm{MAIN}}$, which is also supported by the result of Pnoise simulations.

If phase ϕ_1 and ϕ_2 have a 50% duty-cycle, then the buffer's output noise over the two phases is the average of their respective noise contributions. The buffer's output noise is therefore determined by the average of (4) and (6) and is given by

$$v_{\mathrm{out}} = \sqrt{\frac{1}{2}\left({v_{\mathrm{out}\_\phi 1}}^2 + {v_{\mathrm{out}\_\phi 2}}^2\right)}. \tag{7}$$

Filling-in the earlier expressions for the output noise in phase ϕ_1 (4) and ϕ_2 (6) gives an output noise of

$$v_{\mathrm{out}} = \sqrt{\frac{1}{2}\left(v_{n\mathrm{MAIN}}^2 + V_{n\mathrm{MAINGH}}^2 + v_{n1}^2 + V_{n1\mathrm{GH}}^2 + 2V_{n1\mathrm{EF}}^2\right)}. \tag{8}$$

Removing the distinction between sampled and time-varying noise, this can be simplified to

$$v_{\mathrm{out}} = \sqrt{v_{n\mathrm{MAIN}}^2 + 2v_{n1}^2} = \sqrt{3}e_n. \tag{9}$$

The final result in (9) shows that without correlation, the output noise will be $\sqrt{3e_n}$. However, $V_{n1\mathrm{EF}}$, $V_{n1\mathrm{GH}}$, and $V_{n\mathrm{MAINGH}}$ in (8) are sampled versions of v_{n1} and $v_{n\mathrm{MAIN}}$, which leads to a partial correlation. Pnoise simulations show that these correlations increase the noise to $\sqrt{5e_n}$.

Based on this LF analysis, there are two possible ways to further reduce the total LF noise. One is to remove the dominant $V_{n1\mathrm{EF}}$ term in (7), the other is to extend phase ϕ_1 relative to phase ϕ_2, noting that the output noise in phase ϕ_1 (4) is much lower than phase ϕ_2 (6). These two approaches will be further explored in Sections II-D and II-E.

D. Chopped Stabilization Loop

To remove the $V_{n1\mathrm{EF}}$ term in (7), $V_{n1\mathrm{EF}}$ should not be allowed to propagate to G & H, and eventually to the output, in the same way during the two phases. To achieve this, a chopper placed between nodes E & F and G & H ($\mathrm{CH_{out}}$ in Fig. 10) is used to periodically invert the polarity of the $V_{n1\mathrm{EF}}$ on its way to nodes G and H in phase ϕ_1. In this way, $V_{n1\mathrm{EF}}$ will reach the output with opposite polarities and thus cancel over one chopping period. In this case, the output noise would be given by

$$v_{\mathrm{out}} = \sqrt{\frac{1}{2}\left(v_{n\mathrm{MAIN}}^2 + V_{n\mathrm{MAINGH}}^2 + v_{n1}^2 + V_{n1\mathrm{GH}}^2\right)} = \sqrt{2}e_n \tag{10}$$

where the partial correlation still exists between $V_{n1\mathrm{GH}}$ and v_{n1} as well as $V_{n\mathrm{MAINGH}}$ and $v_{n\mathrm{MAIN}}$. Pnoise simulations show that for a 50% duty-cycle, the partial correlation limits the noise floor to about $\sqrt{3}e_n$. To preserve the correct loop polarity, a second Chopper $\mathrm{CH_{in}}$ is inserted at the input of G_{m1}. This chopper is switched in phase ϕ_2 when it is disconnected from the input by the AZ switches. This prevents its switching activity from generating transients, and thus introducing spikes in the amplifier's input current.

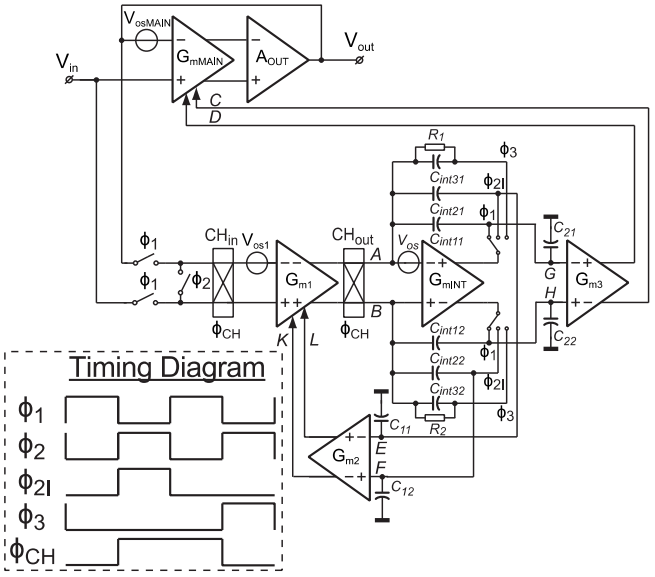

Fig. 10. Auto-zero-stabilized buffer with a chopped stabilization loop.

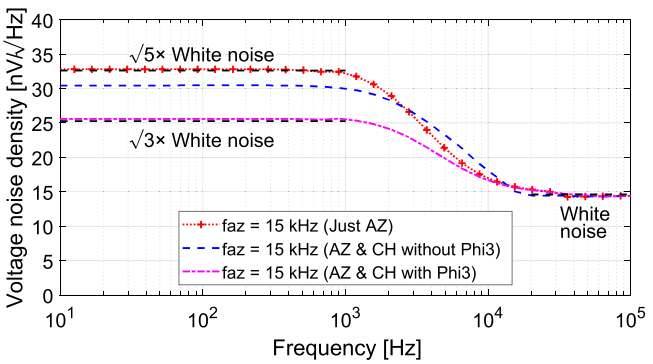

Fig. 11. Voltage noise density simulation for different configurations (AZ, AZ, & CH without and with ϕ_3).

One issue is that the AZ loop is still active in between the two chopping phases. Therefore, $V_{n1\mathrm{EF}}$ will slowly change during chopping and so will not be perfectly canceled. The amount of change depends on the duration of the chopping period and hence on the AZ frequency f_{AZ}. Setting $f_{\mathrm{AZ}} =$ 15 kHz, which is enough to cancel the buffer's $1/f$ noise, only reduces the LF noise floor slightly (Fig. 11). To approach the $\sqrt{3} \times e_n$ limit, simulations show that f_{AZ} would have to be some $3\times$ higher, resulting in significantly more input switching, and hence, more input current.

To preserve the noise across nodes E and F during a chopping period, extra capacitors $C_{\mathrm{int31-int32}}$(1 pF each) are used to implement a modified ϕ_2 phase, denoted by ϕ_3 (Fig. 10). During ϕ_3, the output of $G_{m\mathrm{INT}}$ is not connected to either AZ loop. Also, resistors R_{1-2} (2 MΩ) limit the gain of $G_{m\mathrm{INT}}$, preventing it from clipping due to the residual output current of G_{m1}. $V_{n1\mathrm{EF}}$ can then be fully chopped-out without changing f_{AZ} (Fig. 11). The chopping transitions are arranged to occur in phase ϕ_2, when the input chopper is disconnected from the input by the AZ switches. With these two measures, the AZ stabilization loop can be chopped, lowering the LF noise to $\sqrt{3e_n}$, without introducing extra spikes or input current.

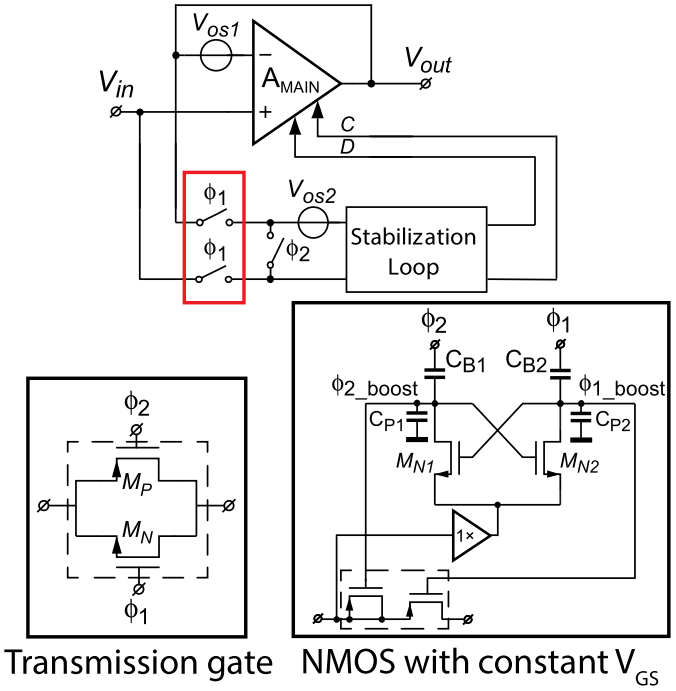

Fig. 12. Two implementations of the AZ switches. Transmission gates and NMOS switches with a constant Vgs drive.

Another issue is the integrator's own offset, which, via the chopper at its input, gives rise to a square-wave ripple voltage at the output of G_{m1}. This will be translated into a ripple voltage at the input of the buffer ripple voltage by dividing it by the transconductance and finite output impedance at f_{ch} of G_{m1}. With an expected integrator offset of about 2 mV, the output impedance of G_{m1} then needs to be quite high (>150 MΩ) to ensure that the resulting ripple is negligible (<100 nV). This requirement is met by implementing G_{m1} as a folded cascode OTA.

E. Duty-Cycling the AZ Clock

With the $V_{n1\text{EF}}$ term removed, the buffer's LF noise level can be further reduced by adjusting the ϕ_1: ϕ_2 duty-cycle. From the noise analysis, we can note that the output noise in phase ϕ_1 ($\sqrt{2} \times e_n$) is less than the noise in phase ϕ_2 ($2 \times e_n$). The correlation will also be affected by the duty-cycle, and the more time the buffer spends in phase ϕ_1, the lower the noise gets. Since some settling time is required for ϕ_2, the resulting noise level in Pnoise simulations will then be somewhere between $\sqrt{3} \times e_n$ and $\sqrt{2} \times e_n$.

F. Implementation of the AZ Switches

The input current of the AZ amplifier is determined by the charge injection mismatch of the two input switches driven by ϕ_1 (Fig. 12). Two implementations of the AZ switches were tested and compared: transmission gate switches [17] and NMOS switches with a constant V_{GS} drive [18].

The constant V_{GS} drive consists of two latching transistors M_{N1} and M_{N2} which pre-charges boosting capacitors C_{B1} and C_{B2} to the input voltage. A fraction of the clock signal is then boosted on top of this to get a V_{GS} driving the switches that

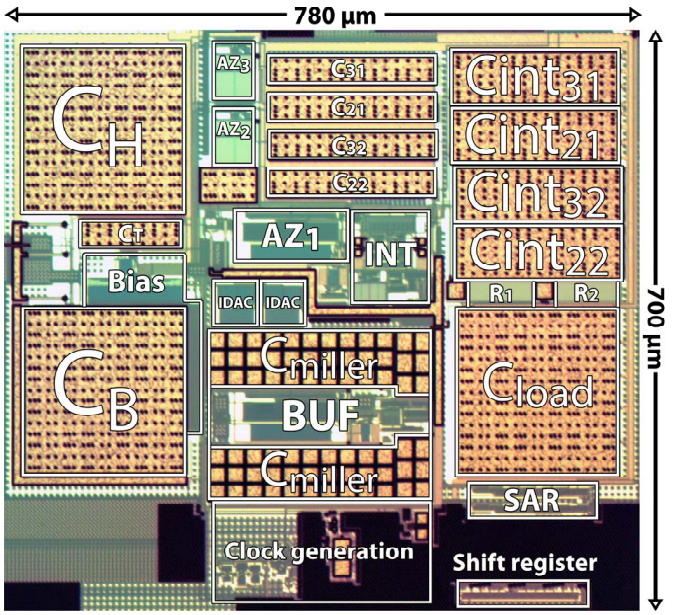

Fig. 13. Chip micrograph of the auto-zero-stabilized voltage buffer.

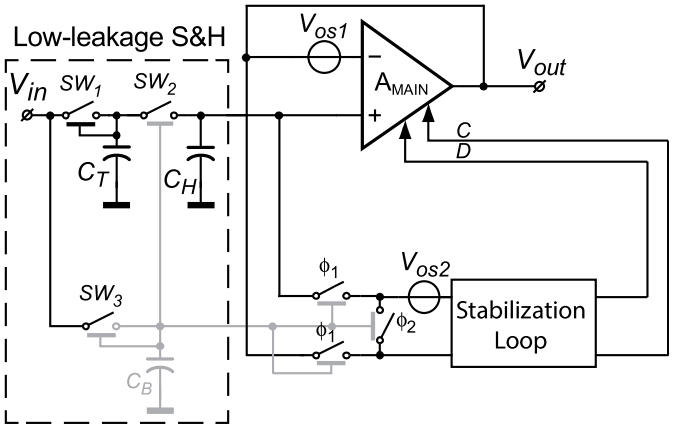

Fig. 14. Low-leakage S&H used to evaluate the input current.

are independent of the input voltage. The amplitude of the resulting clock signal $\Phi_{1,2\_\text{bo}}$ is determined by the ratio of the boosting capacitor (C_{B1-B2}) to the parasitic capacitance to the ground (C_{P1-P2}). A simple buffer is used to make sure that the constant V_{GS} drive switching is not loading the input.

III. Measurement Results

The auto-zero-stabilized buffer was realized in a 0.18 μm CMOS technology (Fig. 13). It draws 210 μA from a 1.8 V supply and has an active area of 0.55 mm^2, 0.12 mm^2 of which is occupied by the low-leakage S&H circuit.

A. Measuring the Input Current

To evaluate the extremely low input current of the buffer, a circuit similar to the sampled voltage reference is used (Fig. 14). An on-chip hold capacitor C_H (36 pF) is pre-charged to an input voltage through a low-leakage sampling network consisting of switches $\text{SW}_{1,2}$. The input is then disconnected

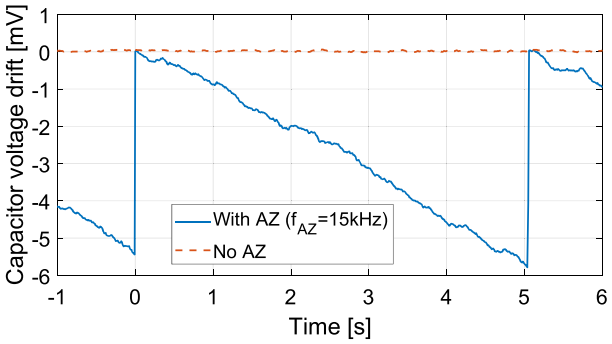

Fig. 15. Capacitor voltage drifts with and without AZ & CH.

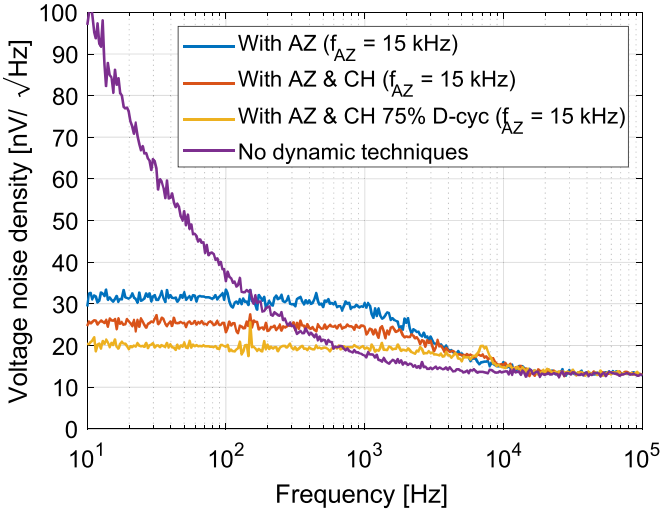

Fig. 16. Measured voltage noise density versus frequency for different scenarios.

and the voltage drift over time of the hold capacitor is observed to deduce the input current.

To minimize the leakage of the sampling switch, extra hold capacitors C_T (3 pF) and, via SW_3, C_B (36 pF) ensure that the channel and body-diodes of SW_2 are operated at zero reverse bias. The same technique is applied to G_{m1}'s input switches SW_{4-6}, as the body diode leakage of these switches would cause the hold capacitor to discharge. All capacitors are implemented with custom MOM capacitors to minimize their leakage.

The voltage drift across C_H is shown for a typical sample with a 1 V input (Fig. 15). With AZ off, there is negligible leakage, illustrating the effectiveness of the low-leakage techniques.

The voltage drift across CH is an accurate measure of the buffer's input current. In a general-purpose buffer, another challenge, when interfacing off-chip sensors, is the leakage of the ESD devices, which is usually >1 pA. To suppress this leakage, special bootstrapped ESD structures can be used [22]. These protection devices are outside the scope of this work. Instead, this article focuses on showing that the input current of an AZ amplifier can be reduced to the sub-pA level.

B. Voltage Noise Density

With all dynamic techniques turned off, at low frequencies, the $1/f$ noise can be seen with a corner frequency of about 700 Hz (Fig. 16). At higher frequencies, the white noise level can be seen with a level of 14 nV/$\sqrt{\text{Hz}}$. With auto-zeroing only, an LF noise density of 31 nV/$\sqrt{\text{Hz}}$ is achieved, which equals the earlier discussed $\sqrt{5}\times$ white noise. When chopping with the extra Φ_3 phase enabled, the LF noise drops to 25 nV/$\sqrt{\text{Hz}}$, which equals the $\sqrt{3}\times$ white noise. Finally, when a 75% duty-cycle is used, an LF noise of 20 nV/$\sqrt{\text{Hz}}$ is achieved, which is very close to the $\sqrt{2}\times$ noise limit. This reduction from $\sqrt{5}\times$ to $\sqrt{2}\times$ noise corresponds to a $2.5\times$ power saving in the input stages. All the noise reduction techniques lead to a competitive NEF of 7.3, due to the low increase in noise floor over a small bandwidth, which leads to an NEF that outperforms even many chopper amplifiers. No tones at f_{AZ} or f_{CH} can be seen, demonstrating that the use of auto-zeroing and chopping does not add spikes and a quiet output is achieved.

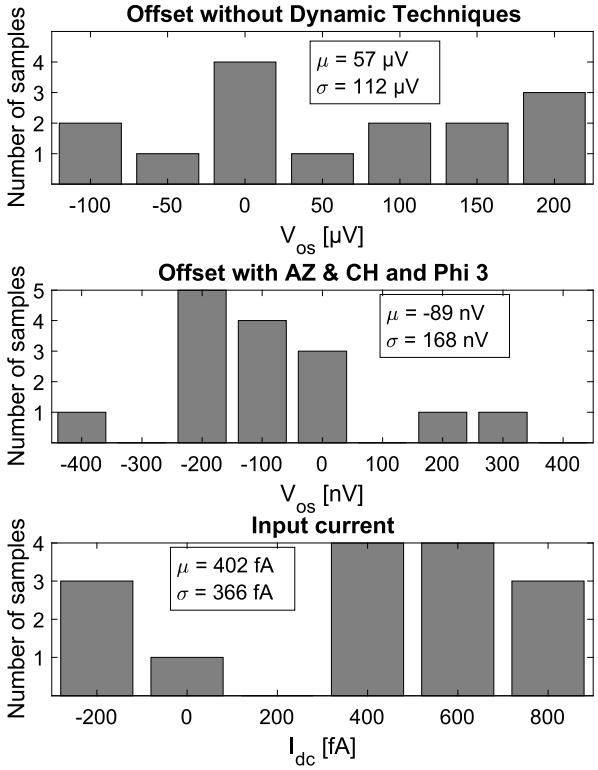

Fig. 17. Histograms (15 samples) of the measured offset (without and with AZ) and input current with AZ & CH and ϕ_3 ($f_{AZ} = 15$ kHz, $V\text{in} = 1$ V).

C. Offset and Input Current

To evaluate the offset and the input current of the buffer, measurements were done on 15 samples (Fig. 17). Without any dynamic techniques, the offset is below 200 μV. When all the dynamic techniques are switched on, the offset is reduced to a maximum value of 0.4 μV. Finally, the input current with all dynamic techniques and the NMOS input switches with a constant V_{GS} drive has a maximum value of 0.8 pA. The 75% duty-cycle of the AZ clock does not change the offset or input current performance. The low input current of this design can be attributed to several design choices. First, auto-zeroing is used instead of chopping, so that the input current only depends on the CI mismatch of one pair of switches.

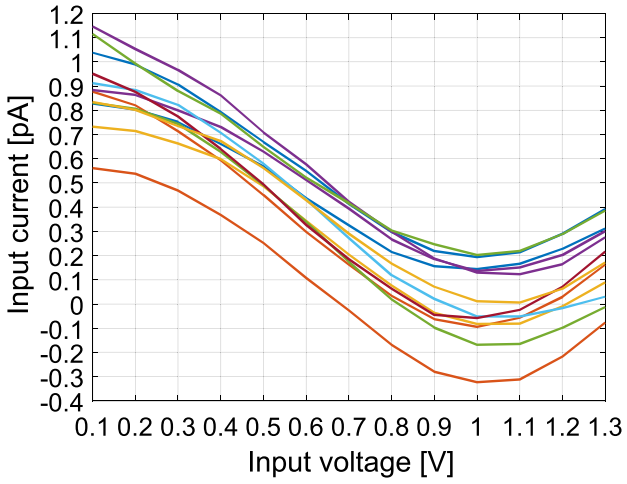

Fig. 18. Input current versus input voltage for transmission gate switches.

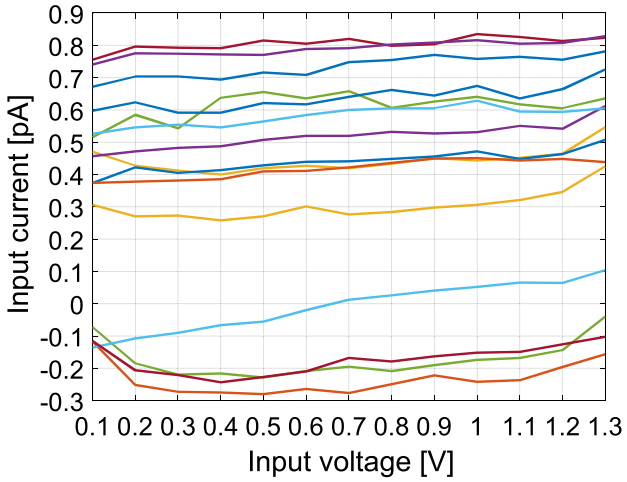

Fig. 19. Input current versus input voltage for NMOS with constant Vgs.

Making f_{AZ} low (15 kHz) also lowers the input current. The additional chopping is done during auto-zeroing phases, and so does not increase the input current. Finally, compared to most prior art [5]–[7], the use of finer technology (180 nm) allows the use of smaller switches with less CI. In general, for a given minimum dimension L, CI scales with L^2, while CI mismatch scales with L [23].

For the two implementations of the AZ switches, the input current versus input voltage was measured for up to 15 samples. The implementation with transmission gates shows a large variation of the input current versus input voltage changing up to 0.9 pA over the full range of the buffer (0.1 to 1.3 V) (Fig. 18).

This change in input current can be attributed to the PMOS and NMOS being active for the different input voltages. For low input voltages, the charge injection of the NMOS is only contributing to the input current and for higher input voltages, the PMOS is contributing. Around halfway the supply, both switches will contribute which leads to a partial cancellation of the charge injection and therefore the lowest input current.

The implementation of the NMOS switches with a constant V_{GS} drive shows a much more constant input current over input voltage, where the worst-case sample changes around 0.2 pA (Fig. 19).

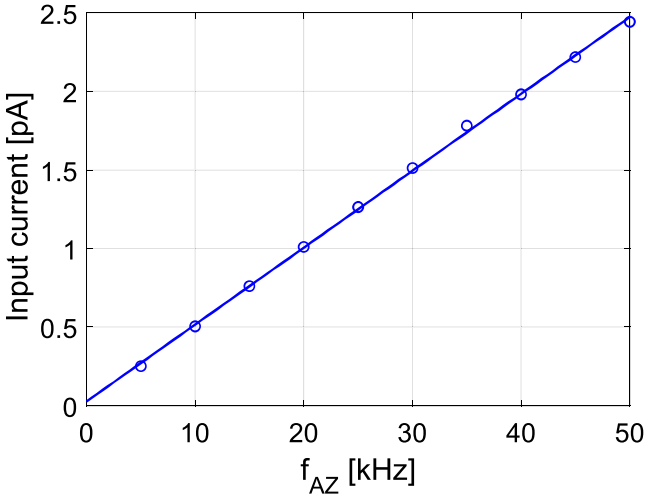

Fig. 20. Input current versus auto-zeroing frequency (f_{AZ}).

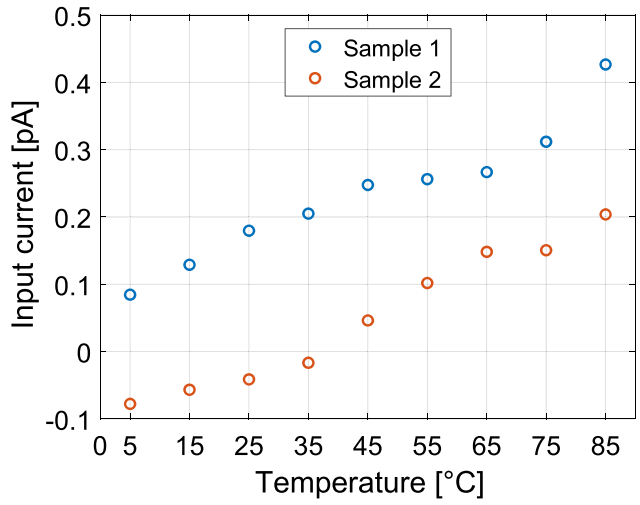

Fig. 21. Input current versus temperature for a fixed input voltage of 1 V.

A measurement of the input current versus f_{AZ} shows a linear relationship (Fig. 20), which extrapolates to zero, which indicates that charge injection is the dominant source of input current.

The input current drift over temperature (from 5 °C to 85 °C) was characterized for two typical samples at a fixed input voltage of 1 V (Fig. 21). The input current drifts around 0.3 pA over 80 °C. This input current is still well below the expected ESD leakage. At higher temperatures, a part of this drift can be attributed to the increased leakage of the S&H circuit.

The input current versus input voltage is also measured for the case of AZ and AZ & CH for a typical sample (Fig. 22). For both cases the input current is similar, showing that the chopping can be done without adding input current.

D. Comparison With the Prior Art

In Table I, the performance of the AZ Stabilized Voltage Buffer is summarized and compared with the state of the art. A 50× reduction in input current is achieved, while also achieving state-of-the-art offset (0.4 μV) and competitive LF voltage noise (20 nV/$\sqrt{\text{Hz}}$). The NEF of this AZ design is

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH THE STATE OF THE ART

	This work	Q. Fan [5]	Y. Kusuda [6]	A.T.K Tang [7]	M. A. P. Pertijs [20]	AD8551 [24]	S. Sakunia [25]
Dynamic technique(s)	**Auto-zeroing and Chopped Stabilization**	Chopping	Chopping	Chopping and Auto-zeroing	Chopping and Auto-zeroing	Auto-zeroing	Chopping and Auto-zeroing
Input current (Max)	**0.8 pA**	110 pA	72 pA	40 pA	-	50 pA	-
Offset (Max)	**0.4 µV**	1 µV	0.78 µV	3 µV	2.8 µV	5 µV	4 µV
Voltage noise (nV/√Hz)	**31 (AZ) 25 (AZ&CH) 20 (75% AZ&CH)**	10.5	5.9	20	38 (AZ) 27 (CH&AZ)	75	140 (AZ) 28 (CH&AZ)
GBW (MHz)	**1.45**	1.8	4	2.5	0.8	1	-
NEF	**7.3**	4.8	8.7	21.8	43.5	-	-
PSRR (dB)	**125**	120	142	-	138	130	128
Frequency (kHz)	**15 (f_{AZ}) / 7.5 (f_{CH})**	30	200	15 (f_{CH}) / 7.5 (f_{AZ})	28 (f_{AZ}) / 14 (f_{CH})	4	11 (f_{CH}) / 7.33 (f_{AZ})
Supply current	**210 µA**	143 µA	1.47 mA	800 µA	1.7 mA	750 µA	480 µA
Supply voltage	**1.8 V**	5 V	2.5 - 5.5 V	5 V	2.7 - 5.5 V	2.7 V	3.3 - 5.5 V
Technology	**0.18 µm**	0.7 µm	0.35 µm	0.6 µm	0.5 µm	-	0.5 µm
Die area (mm^2)	**1.4**	1.8	1.26	0.67	2.5	-	1.48

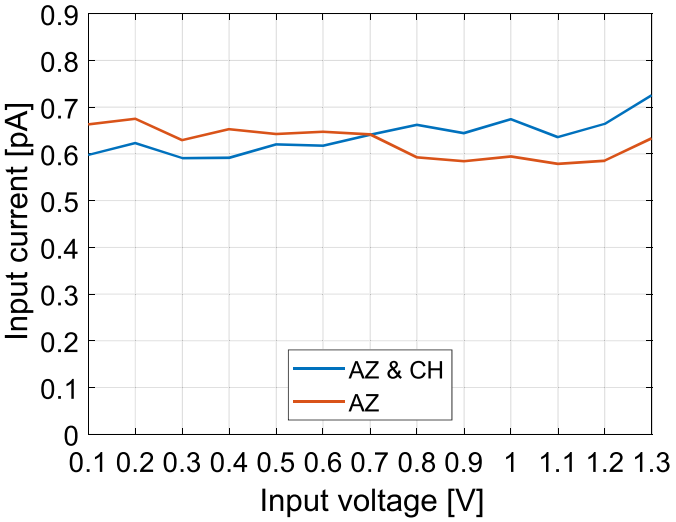

Fig. 22. Input current versus input voltage for a typical sample in the case of AZ and AZ & CH.

comparable with some CH amplifiers [6], due to the introduced LF noise reduction techniques.

IV. CONCLUSION

An auto-zero-stabilized voltage buffer is presented that achieves a combination of low noise (20 nV/$\sqrt{\text{Hz}}$), low offset (0.4 μV max), and low input current (0.8 pA max). The elevated LF noise density associated with auto-zeroing is minimized by using a combination of: a digitally assisted AZ loop, chopping to remove correlation, and an optimized duty-cycle for the AZ clock. This allows the buffer to reach an LF noise density close to $\sqrt{2}$ times its white noise density (14 nV/$\sqrt{\text{Hz}}$), which is the fundamental limit of an AZ amplifier. This is the first design to demonstrate that dynamic offset correction techniques can be used to realize a buffer with both sub-pA input current and sub-μV offset.

REFERENCES

[1] V. Ivanov, R. Brederlow, and J. Gerber, "An ultra low power bandgap operational at supply from 0.75 V," *IEEE J. Solid-State Circuits*, vol. 47, no. 7, pp. 1515–1523, Jul. 2012.

[2] Y. Chen, M. Fojtik, D. Blaauw, and D. Sylvester, "A 2.98 nW bandgap voltage reference using a self-tuning low leakage sample and hold," in *Proc. Symp. VLSI Circuits (VLSIC)*, Jun. 2012, pp. 200–201.

[3] M. Liu, P. Harpe, R. van Dommele, and A. van Roermund, "A 0.8 V 10 b 80 kS/s SAR ADC with duty-cycled reference generation," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2015, pp. 1–3.

[4] S. Wen, K. Chen, C. Hsiao, and Y. Chen, "A −105 dBc THD+N (−114 dBc HD2) at 2.8 VPP swing and 120 dB DR audio decoder with sample-and-hold noise filtering and poly resistor linearization schemes," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2019, pp. 294–295.

[5] Q. Fan *et al.*, "A 21 nV/$\sqrt{\text{Hz}}$ chopper-stabilized multi-path current-feedback instrumentation amplifier with 2 μV offset," *IEEE J. Solid-State Circuits*, vol. 47, no. 2, pp. 464–475, Feb. 2012.

[6] Y. Kusuda, "A 5.9 nV/$\sqrt{\text{Hz}}$ chopper operational amplifier with 0.78 μV maximum offset and 28.3 nV/°C offset drift," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2011, pp. 242–244.

[7] A. T. K. Tang, "A 3 μV-offset operational amplifier with 20 nV/$\sqrt{\text{Hz}}$ input noise PSD at DC employing both chopping and autozeroing," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2001, pp. 386–387.

[8] R. Wu, Y. Chae, J. H. Huijsing, and K. A. A. Makinwa, "A 20-b ± 40-mV range read-out IC with 50-nV offset and 0.04% gain error for bridge transducers," *IEEE J. Solid-State Circuits*, vol. 47, no. 9, pp. 2152–2163, Sep. 2012.

[9] Y. M. Chi, T.-P. Jung, and G. Cauwenberghs, "Dry-contact and noncontact biopotential electrodes: Methodological review," *IEEE Rev. Biomed. Eng.*, vol. 3, pp. 106–119, 2010.

[10] W. Kester, *Practical Design Techniques for Sensor Signal Conditioning*. Upper Saddle River, NJ, USA: Prentice-Hall, 1999.

[11] M. Bolatkale, M. A. P. Pertijs, W. J. Kindt, J. H. Huijsing, and K. A. A. Makinwa, "A single-temperature trimming technique for MOS-input operational amplifiers achieving 0.33 μV/°C offset drift," *IEEE J. Solid-State Circuits*, vol. 46, no. 9, pp. 2099–2107, Sep. 2011.

[12] M. Snoeij, "A 36 V 48 MHz JFET-input bipolar operational amplifier with 150 μV maximum offset and overload supply current control," in *Proc. IEEE 44th Eur. Solid State Circuits Conf. (ESSCIRC)*, Dresden, Germany, Sep. 2018, pp. 290–293.
[13] Texas Instruments. (Jun. 2021). *OPA140 Data Sheet*. [Online]. Available: http://www.ti.com/lit/ds/symlink/opa140.pdf
[14] Analog Devices. *ADA4625 Data Sheet*. Accessed: Aug. 4, 2021. [Online]. Available: https://www.analog.com/media/en/technical-documentation/data-sheets/ADA4625-1-4625-2.pdf
[15] Y. Kusuda, "A 60 V auto-zero and chopper operational amplifier with 800 kHz interleaved clocks and input bias current trimming," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 2804–2813, Dec. 2015.
[16] A. Bakker, K. Thiele, and J. H. Huijsing, "A CMOS nested-chopper instrumentation amplifier with 100-nV offset," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1877–1883, Dec. 2000.
[17] T. Rooijers, J. H. Huijsing, and K. A. A. Makinwa, "A quiet digitally assisted auto-zero-stabilized voltage buffer with 0.6 pA input current and 0.6 μV offset," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2018, pp. 50–52.
[18] T. Rooijers, J. H. Huijsing, and K. A. A. Makinwa, "An auto-zero stabilized voltage buffer with a quiet chopping scheme and constant input current," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2019, pp. 298–299.
[19] C. C. Enz and G. C. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: Autozeroing, correlated double sampling, and chopper stabilization," *Proc. IEEE*, vol. 84, no. 11, pp. 1584–1614, Nov. 1996.
[20] M. A. P. Pertijs and W. J. Kindt, "A 140 dB-CMRR current-feedback instrumentation amplifier employing ping-pong auto-zeroing and chopping," *IEEE J. Solid-State Circuits*, vol. 45, no. 10, pp. 2044–2056, Oct. 2010.
[21] J. Xu, R. F. Yazicioglu, P. Harpe, K. A. A. Makinwa, and C. Van Hoof, "A 160 μW 8-channel active electrode system for EEG monitoring," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Nov. 2011, pp. 300–302.
[22] Analog Devices. *ADA4530 Data Sheet*. Accessed: Aug. 4, 2021. [Online]. Available: https://www.analog.com/en/products/ada4530-1.html?doc=ada4530-1.pdf
[23] M. Pelgrom, *Analog-to-Digital Conversion*, 3rd ed. Cham, Switzerland: Springer, 2009, p. 172.
[24] Analog Devices. (Jun. 2015). *AD8551 Data Sheet*. [Online]. Available: http://www.analog.com/media/en/technical-documentation/datasheets/AD8551_8552_8554.pdf
[25] S. Sakunia *et al.*, "A ping-pong-pang current-feedback instrumentation amplifier with 0.04% gain error," in *Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2011, pp. 60–61.

Thije Rooijers (Graduate Student Member, IEEE) was born in Leiden, The Netherlands, in 1991. He received the B.Sc. and M.Sc. degrees in electrical engineering from the Delft University of Technology, Delft, The Netherlands, in 2013 and 2016, respectively. He is currently pursuing the Ph.D. degree with the Delft University of Technology, focusing on reducing the imperfections of dynamic offset compensated amplifiers.

Mr. Rooijers was a recipient of the ADI Outstanding Student Designer Award in 2018, the ProRISC Best Oral Presentation Award in 2019, and the ProRISC Best Poster Award in 2021.

Johan H. Huijsing (Life Fellow, IEEE) received the M.Sc. degree in electrical engineering and the Ph.D. degree from the Delft University of Technology, Delft, The Netherlands, in 1969 and 1981, respectively.

He has been an Assistant Professor and an Associate Professor of electronic instrumentation with the Faculty of Electrical Engineering, Delft University of Technology, since 1969. In 1990, he joined the Chair of Electronic Instrumentation, as a Full Professor. He has been a Professor Emeritus since 2003. From 1982 to 1983, he was a Senior Scientist with Philips Research Laboratories, Sunnyvale, CA, USA. From 1983 to 2005, he was a Consultant with Philips Semiconductors, Sunnyvale. Since 1998, he has been a Consultant with Maxim, Sunnyvale. He has supervised 30 Ph.D. students. He has authored or coauthored over 300 scientific articles, 40 U.S. patents, and 15 books. In 1992, he initiated the International Workshop on Advances in Analog Circuit Design. He co-organized it yearly until 2003. His research work is focused on operational amplifiers, analog-to-digital converters, and integrated smart sensors.

Dr. Huijsing was a Program Committee Member of the European Solid-State Circuits Conference from 1992 to 2002. He was awarded the title of Simon Stevin Meester by the Dutch Technology Foundation. He was the Chair of the Dutch STW Platform on Sensor Technology and the Biannual National Workshop on Sensor Technology from 1991 to 2002.

Kofi A. A. Makinwa (Fellow, IEEE) received the B.Sc. and M.Sc. degrees from Obafemi Awolowo University, Ife, Nigeria, in 1985 and 1988, respectively, the M.E.E. degree from the Philips International Institute, Eindhoven, The Netherlands, in 1989, and the Ph.D. degree from the Delft University of Technology, Delft, The Netherlands, in 2004.

From 1989 to 1999, he was a Research Scientist with Philips Research Laboratories, Eindhoven, where he worked on interactive displays and digital recording systems. In 1999, he joined the Delft University of Technology, where he is currently an Antoni van Leeuwenhoek Professor and the Head of the Microelectronics Department. This has led to 16 books, more than 300 technical articles, and more than 30 patents. His research interests include the design of mixed-signal circuits, sensor interfaces, and smart sensors.

Dr. Makinwa is also a member of the Royal Netherlands Academy of Arts and Sciences. He is also one of the organizers of the Advances in Analog Circuit Design Workshop and the IEEE Sensor Interfaces Meeting. He is also an ISSCC Top-10 Contributor (with more than 60 articles), and a co-recipient of 16 Best Paper Awards, from the JSSC, ISSCC, VLSI, ESSCIRC, Transducers, and among others. He was the Analog Subcom Chair of ISSCC. He has served on the program committee for several other IEEE conferences. He has also served the Solid-State Circuits Society as a Distinguished Lecturer and an Elected Member of its Adcom.