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A Front-End ASIC with High-Voltage Transmit Switching and Receive Digitization for Forward-Looking Intravascular Ultrasound

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***Abstract*—This paper presents a front-end ASIC for forward-looking intravascular ultrasound (IVUS) imaging. The ASIC is intended to be mounted at the tip of a catheter and can interface a total of 80 piezo-electric transducer elements with an imaging systems using only 4 cables, thus significantly reducing the system complexity compared to the prior art. It is capable of switching high-voltage transmit pulses to 16 transmit elements, and capturing the resulting echo signals using 64 multiplexed receive elements. The ASIC digitizes the received signals locally, providing more robust communication than prior analog approaches. Measurements show that the ASIC effectively switches transmit pulses up to 30 V, and digitizes echo signals with a bandwidth of 16 MHz, while consuming only 10 mW. Acoustic measurements in combination with a prototype transducer array demonstrate pulse transmission and reception. Finally, a B-mode image of a needle phantom demonstrates the imaging capability.**

Keywords—instravascular ultrasound imaging, piezo-electric transducer, high-voltage switching, receive digitization, cable-count reduction

I. Introduction

Forward-looking intra-vascular ultrasound (IVUS) imaging is needed for the diagnosis and treatment of complex arterial diseases, such as chronic total occlusions in the coronary arteries of the heart [1]. Conventional IVUS catheters are sideways-looking devices that employ either a mechanically-rotated single-element transducer, or a ring-shaped transducer array [2]. With both types, an image of the cross-section of the artery can be obtained. To achieve real-time forward-looking 3D imaging without rotation, a 2D array of transducer elements can be placed at the tip of the catheter. However, connecting the required 50-100 elements using micro-coax cables within the catheter diameter of < 2 mm is extremely challenging.

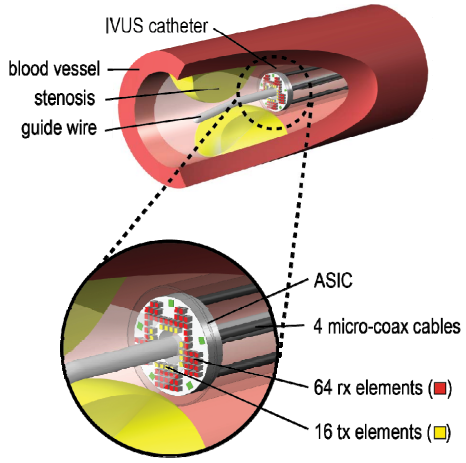

Fig. 1. A conceptual diagram of the forward-looking IVUS system.

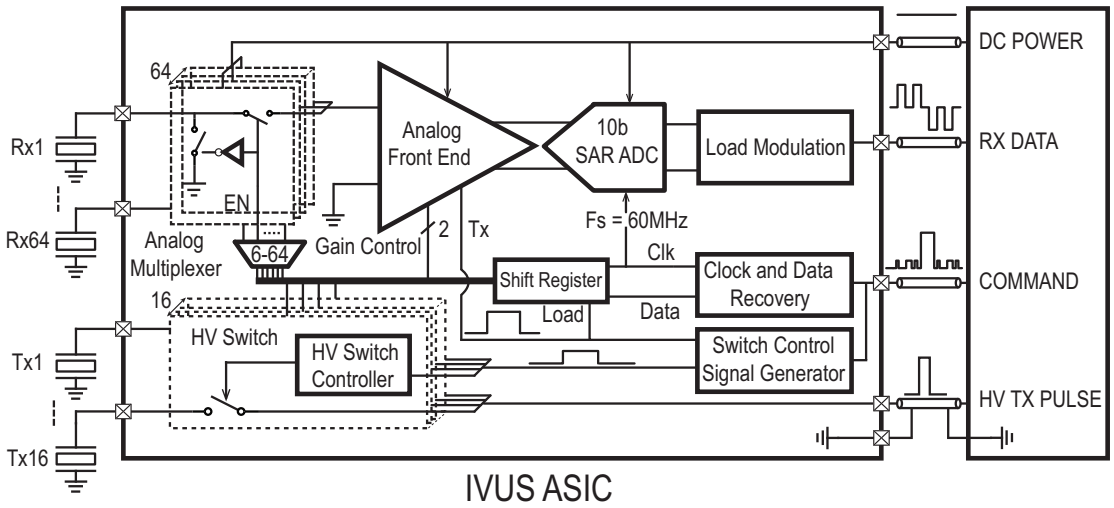

Fig. 2. Block diagram of the IVUS ASIC.

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Integrated circuits have been reported that employ pulsers and multiplexers to reduce the number of cables, but these still require at least 13 connections [3, 4].

In this work, we present an ASIC that requires only 4 micro-coax cables to interface with a total of 80 piezoelectric transducer elements fabricated on top of the ASIC: 64 receive (RX) elements and 16 transmit (TX) elements. Fig. 1 illustrates conceptually how the ASIC will be mounted at the tip of a catheter. The ASIC will be laser-cut into a donut shape, with an outer diameter of 1.5 mm and an inner hole of 0.5 mm for the guide wire.

The ASIC enables synthetic aperture imaging, in which acoustic pulses are transmitted using one or multiple TX elements, and the resulting echoes received by the RX elements are recorded one element at a time. The ASIC digitizes the received echo signals locally, allowing them to be transmitted in a robust form to an external imaging system.

To do so, as shown in Fig. 2, a multiplexer connects one of the 64 RX elements to an analog front-end, where the received signal is amplified with a programmable gain and then digitized using a 10-bit 60 MS/s SAR ADC. The ADC's serial output is transferred to the system using load modulation. A set of high-voltage (HV) switches connect one or multiple of the 16 TX elements to an external pulser. Compared to the use of on-chip pulsers [3, 4], this approach reduces the on-chip power dissipation and allows arbitrary transmit waveforms. A multi-functional command line from the system carries pulse-width encoded switch and gain settings to an on-chip shift register, provides a sampling clock for the ADC, and provides the voltage needed to switch on the selected HV switches. A fourth cable provides the ASIC with a supply voltage (V_{DD}) of 1.9 V.

II. Front-end ASIC Design

A. High-Voltage Switches

The HV NMOS switches are turned on by storing charge on a bootstrap capacitor C_{bs} at their gates (Fig. 3). To do so, the command line V_{cmd} is pulled to 5 V by the system and C_{bs} is charged to that level through transistors M4, M10 and MH2. M4 is turned on when V_{cmd} exceeds V_{DD} at the start of the TX

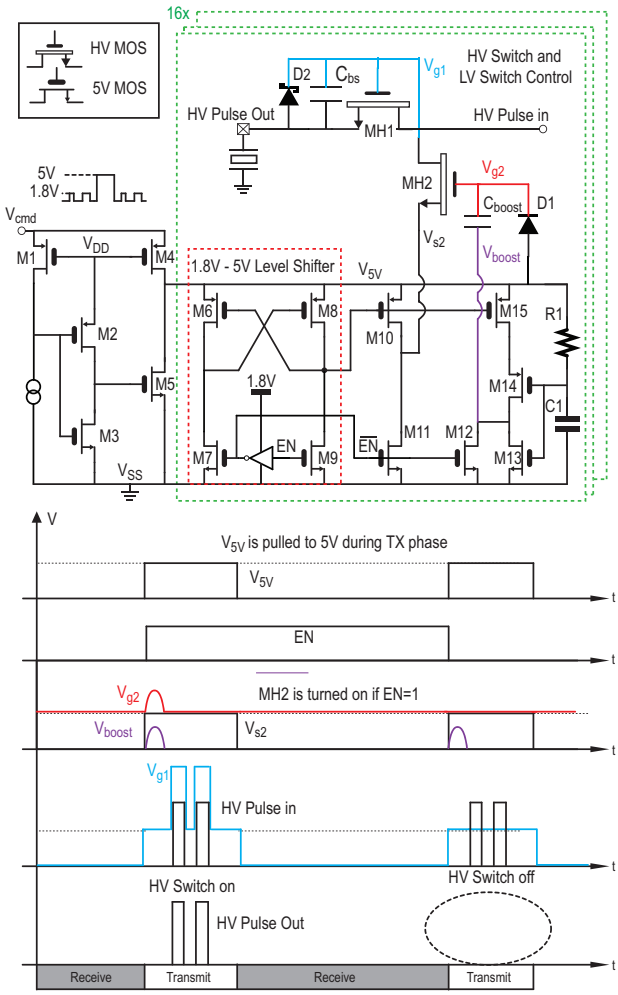

Fig. 3. Circuit diagram of the switch controller and high-voltage switches, with the corresponding timing diagram.

phase. M10 is turned on via a level-shifter only if the enable bit (EN) in the shift register is set to 1. Finally, MH2 is a HV NMOS that is turned on through a capacitor C_{boost} at the start of the TX phase during a short period defined by R1 and C1. After that, the gate of MH1 is pulled back to 5 V, isolating the charge on C_{bs} and keeping the switch on during the subsequent HV pulse, which can exceed the supply of the chip up to 30 V. Finally, when V_{cmd} drops back to V_{DD}, C_{bs} is discharged through MH1, turning off the switch.

B. Clock and Data Recovery

To use V_{cmd} to also transfer a clock and serial data, a 5V NMOS clamps the signal on V_{cmd} to a threshold below V_{DD}, after which a comparator reshapes it to logic levels (Fig. 4). During the RX phase, the rising edges of the resulting signal serve as the sampling clock for the ADC, while the pulse width encodes data bits for the shift register. These are recovered by a flip-flop clocked by a delayed version of the signal. The shift register is latched, so that the loaded bits will only become effective at the start of the next TX phase.

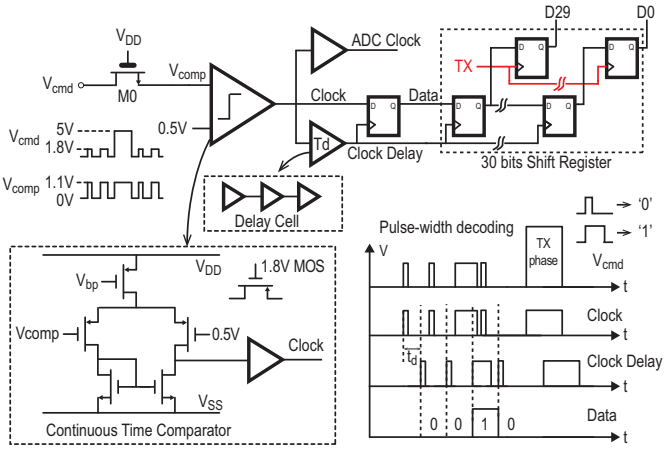

Fig. 4. Circuit diagram of the clock and data recovery circuit.

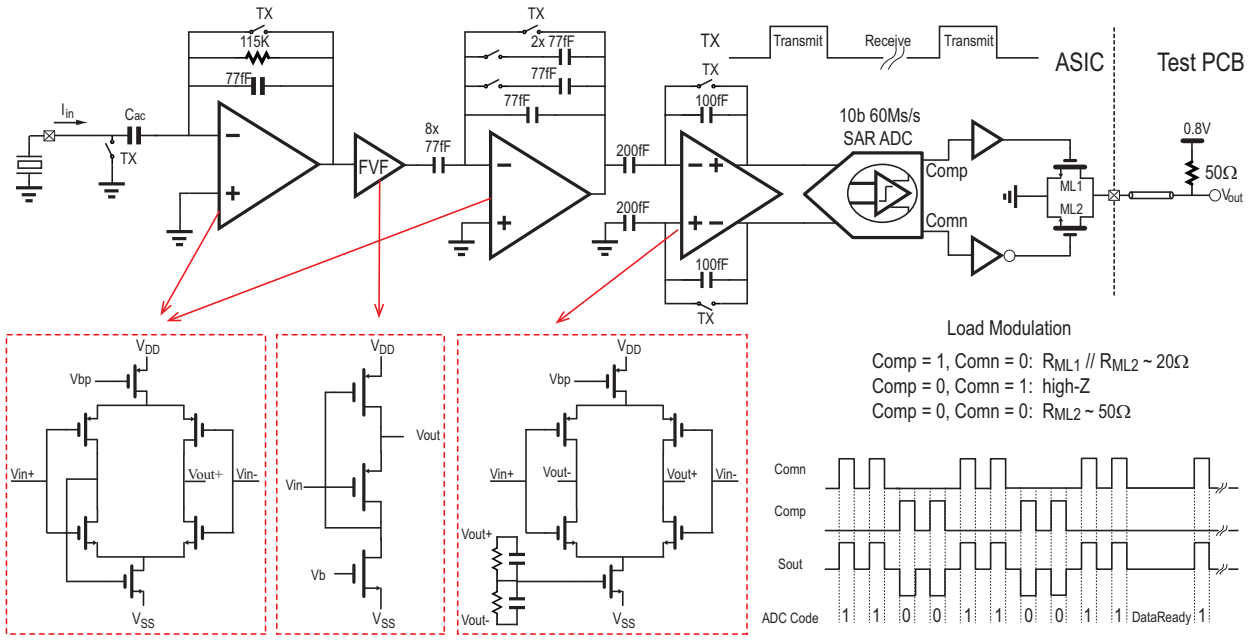

Fig. 5. Details of the receive chain: multiplexer, analog front-end, ADC and load modulation.

C. Receive Signal Chain

Fig. 5 shows the receive signal chain. Because of the relatively high impedance (< 1 pF) of the transducer elements, an AC-coupled TIA built around a current-reuse OTA is used to amplify the motional current of the transducer in a power-efficient manner with a bandwidth of more than 15 MHz. An inverting amplifier with a switchable capacitive feedback network, built around a similar OTA, provides an additional gain of 6 dB, 12 dB or 18 dB. A flipped voltage-follower (FVF) [5] prevents its input capacitance from loading the TIA. Finally, the signal is turned into a differential input for the SAR ADC using a gain stage built around a fully differential current-reuse OTA. During the TX phase, the input of the receive path is grounded and the amplifiers are switched in unity-gain feedback to provide a well-defined bias point.

The SAR ADC is a charge-sharing design similar to [6]. To avoid an external oversampling clock, it employs self-timed logic, which proceeds to the next bit when the dynamic comparator has reached a decision. Thus, after an edge of the sampling clock, the comparator's differential outputs successively represent the ADC's output bits, alternated with evaluation phases in which both outputs are low (Fig. 5). To transfer the output bits to the external system via a single cable, the comparator's outputs drive two differently-sized NMOS load-modulation switches, allowing the bits to be recovered from the resulting three-level waveform observed on a termination resistor on the system side.

III. Prototype Chip

The ASIC was fabricated in a 0.18 µm HV CMOS process (Fig. 6). The circular layout has a 1.5 mm outer diameter and a central hole with a 0.5 mm diameter, so that it can be laser-cut into a donut shape to fit at the tip of a catheter. Five bond pads provide electrical connections for the four micro-coaxial cables; 80 bondpads are positioned to connect to transducer

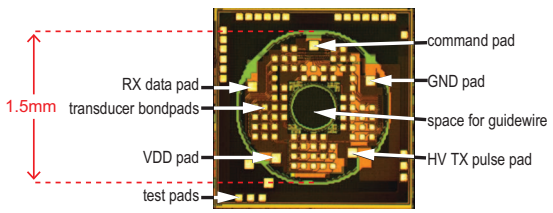

Fig. 6. Chip micrograph.

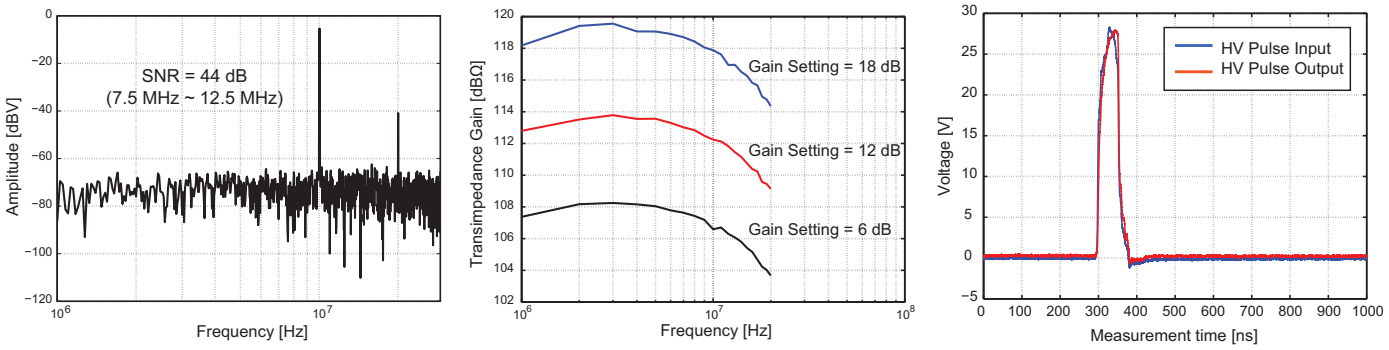

Fig. 7. Measured output spectrum and transfer function of the receive path and measured output waveform at a transmit bondpad.

elements that will be fabricated on top of the die using an approach similar to [7]. The die area around the donut is used for test circuits, which are not connected in the acoustic experiments reported below.

IV. Experimental Results

A. Electrical Measurements

The receive path has been characterized electrically by applying an input current to a test input of the receive multiplexer and recording the ADC output using an oscilloscope. The measured transfer function at the three gain settings shows a -3 dB bandwidth of 16 MHz (Fig. 7). An output spectrum recorded at the highest gain shows an SNR of 44 dB, giving an overall DR of 55 dB in combination with the 11.3 dB programmable gain, suitable for the IVUS application. Fig. 7 also shows that the HV switches successfully pass a 30 V 50 ns pulse to a transducer bondpad.

B. Acoustical Measurements

For initial acoustical characterization, 9 transmit pads and 16 receive pads of the ASIC have been wirebonded to an array of transducers with a 10 MHz center frequency (Fig. 8), on top of which a small water bag was mounted. As shown in Fig. 9, the acoustic pressure measured using a hydrophone placed at 2.5 mm in front of the array increases with the number of transmit switches that are closed, demonstrating effective switching of the 30 V pulses applied. When the array is insonified at an angle using a separate transmitter, the digitized echoes received through the ASIC show the expected relative time delays. Finally, a B-mode image, generated by successively pulsing the 9 transmit elements and capturing the received data of the 16 receive elements, clearly shows three needles placed in front of the array.

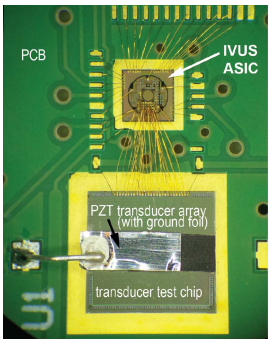

Fig. 8. A prototype ASIC wirebonded to a test transducer array.

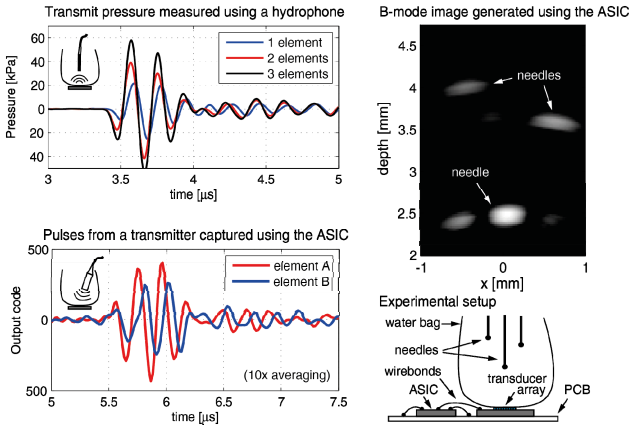

Fig. 9. Acoustical measurement setup and results.

TABLE I. Comparison with the Prior Art

	[2]	[3]	This work
Transducer type	CMUT	CMUT	PZT
Process	0.35 µm HV CMOS	0.35 µm HV CMOS	0.18 µm HV CMOS
Supply voltage	3.3 V	3.3 V	1.9 V(V_{DD}) + 5 V(V_{cmd})
#Transmit	56	64	16
#Receive	48	64	64
Center frequency	10 MHz	12 MHz	10 MHz
Receive output	Analog	Analog	Digital
Receive bandwidth	40 MHz	N/A	16 MHz
Transmit circuit	Pulser	Pulser	Switch
Max.transmit amplitude	25 V	12.5 V	30 V
Power consumption	20 mW	N/A	10 mW
Cable count	13	13	4*

* 4 micro-coax cables, so 5 connections including ground.

V. Conclusions

A front-end ASIC has been developed for forward-looking intravascular ultrasound imaging. Table I summarizes the ASIC's performance and compares it to the prior art. The ASIC is capable of interfacing with an array of PZT transducer elements (64 receivers and 16 transmitters) through only four cables, 3× less than the prior art. The ASIC includes high-voltage transmit switches controlled through a multi-functional command line. It is the first ASIC for catheter-based ultrasound that digitizes the received signal locally, allowing robust signal transmission to an imaging system. The ASIC's functionality has been demonstrated by both electrical and acoustic measurements.

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