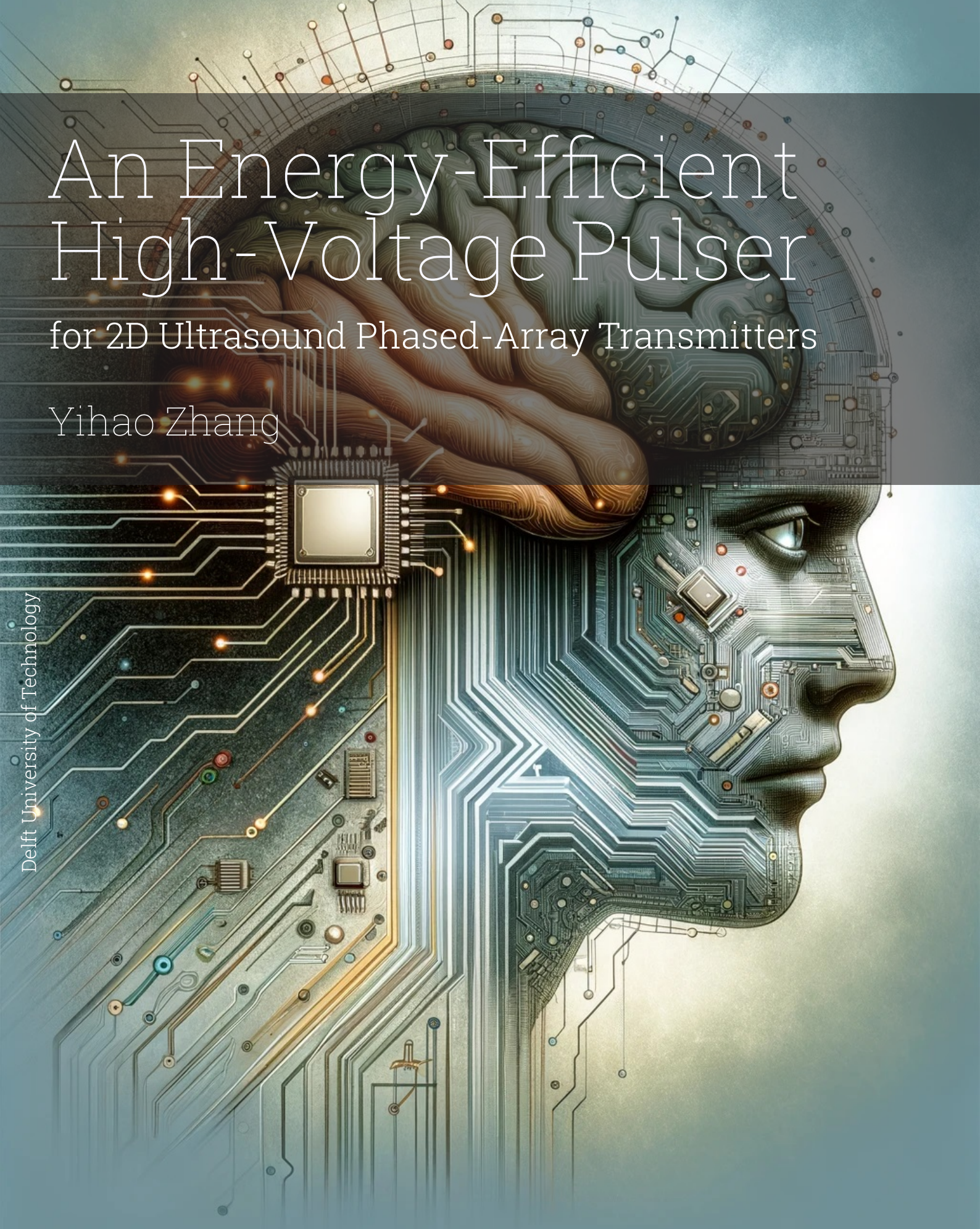
An Energy-Efficient High-Voltage Pulser

for 2D Ultrasound Phased-Array Transmitters

Yihao Zhang



Delft University of Technology

TU Delft

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by

Yihao Zhang

A thesis submitted to the Delft University of Technology in partial fulfillment of the requirements for the degree of Master of Science in Microelectronics.

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Acknowledgement

Three years ago in a same cold winter, I was working out of office with my leader to visit an invested project. He was in a good mood and taught me some life wisdom. He said that every thing we do has already been written in the book of destiny. I did not say anything but thought, "am I just breaking that book?"

After graduating from university in 2015, I went to work for a state-owned energy supply company in my home city. That was my destiny. People in that company usually let their children to work in the same company. My father works there, so I had no reason to reject him. That was a decent and stable job, which was admired by most of my friends. However, I was not really satisfied by myself. I am a person with great curiosity and I always want to explore something new with creativity, while the work was comparatively repeated and tedious in that huge state-owned system. So there were grasses of doing something different growing in my heart.

My life went into this brand new chapter after coming to TU Delft. I would admit that studying in Microelectronics is pretty hard for me. I was not in the field of electronics both during my bachelor's period and the working experience, so a lot of basic knowledge was waiting me to learn. The most terrible part is that I had not studied for 6 years, meaning that I needed to take more time than others to get back to the student mode. However, it is the challenge that makes life out of my destiny charming. The courses require strong logical thinking ability. Each part of a circuit must be planned and integrated under a clear framework based on their functions, and all kinds of trade-off in the circuit design seems really interesting for me. I feel more refreshed as analog circuit design gives me a sense of clear logic, modularity, and order, from which the sense of accomplishment is what I went all the way to pursue during the 6 years. I am really proud of my past two years and feel so grateful to TU Delft for giving me this opportunity to change my destiny.

My grandmother was diagnosed with Alzheimer's disease when she took a physical check-up by chance. People know very little about Alzheimer in my small town and no one can tell what was wrong with her earlier. This is the reason why I always have an ambition that using my circuit design knowledge to provide some help for the medical-related area. It's my great honour to join the MIND group in the team of Bioelectronics. I would like to extend my deepest gratitude to my supervisor, Tiago and the entire MIND group for the invaluable support throughout my thesis journey. Tiago has been a mentor and a friend. He dedicates to creating a warm, familial atmosphere within our group. His unconditional support and insightful feedback have been important to me. I would also like to express my sincere gratitude to the thesis committee member Michiel. I am truly thankful for his involvement and support in my academic journey. I am also immensely grateful to my daily supervisor Hassan. He has profound knowledge in circuit design, and he is always ready to help me at any moment—this has been pivotal in my learning and progress. His patient explanations and hands-on guidance have enriched my understanding and skill in the field of analog circuit design. I would also like to thank all the members of the MIND group. Their friendly and humorous nature has created an environment that felt like home, making every challenge more approachable and

every success more enjoyable. The collaborative spirit has not only enhanced my professional skills but have also left me with fond memories that I will cherish forever.

My Mom and Dad, who will be present at my defense online, would definitely not understand a single word about what I'm doing, but they would still be there to support me, just like when I decided to come to the Netherlands in 2021—— they didn't understand why I was trying to rewrite the destiny, but they still drove me to the TOEFL examination. I love them so much.

Thank you all for your support, guidance, and the unforgettable journey.

Yihao Zhang
Delft, December 2023

Abstract

Ultrasound (US) neuromodulation is a widely-used technique in the field of neuroscience and medical therapy that uses ultrasound waves to non-invasively modulate neural activity. The miniaturization of modern ultrasonic systems has an intimate relation with system power consumption. As the advancement of Integrated Circuits (ICs) represents a powerful stride in achieving the compactness and integration of ultrasound systems, power efficiency is always a challenge in ICs. The pulser is a power-consuming part in the transmitter stage, because a considerable power should be used to charge and discharge the parasitic capacitor of the US transducer.

This project aims to design a power-efficient pulser for an ultrasound transducer, which is adopted in a 2D ultrasound phased-array transmitter (TX). The area of the TX circuit in a 2D phased array is limited to half of the sound wavelength, requiring an area limitation for the circuit. The transducer element used in this case has an area of $100 \times 100\ \mu m^2$. Thus, the area occupation is also considered as an important aspect through the design process.

This work designs a power-efficient 3-level high-voltage pulser with TSMC 180-nm BCD Technology. The proposed pulser interfaces an ultrasound PZT transducer with a resonant frequency of 8.15 MHz. A bootstrap structure is utilized in this design to double the 10-V supply voltage. Five switches are controlled open and close to determine the voltage level at the output node, where three control signals are needed. The design adopts stacked standard CMOS transistors instead of HV transistors for the switches. As the transistors inevitably act as one of the power-hungry parts in the circuit, a smart design of shortly close one of the switches is proposed to save more energy. The 3 levels of the output voltage level from the proposed pulser are near 0, 8 V and 15 V. Thus, as a reference for comparison, a conventional class-D pulser with a supply voltage of 15 V is also presented. It is worth mentioning that to make the comparison as fair as possible, the conventional pulser is also designed in its most power-efficient condition. The simulation result shows a 35.4% power efficiency enhancement of the proposed design compared with the conventional class-D pulser.

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1 Introduction

1.1. Introduction for ultrasound neuromodulation

Brain stimulation techniques play a crucial role in treating neurological disorders. While these methods are indispensable, the choice of technique depends on various factors. In humans studies, optogenetics-based approaches that require genetic manipulation and injections are inherently invasive, limiting it to broader use [1]. Moreover, deep brain stimulation [1] is not viable for probing neural function in healthy volunteers, while successful in treating conditions such as Parkinson's disease [2].

To overcome these limitations, non-invasive brain stimulation (NIBS) methods [3] have been presented, providing tools for modulating neural activity in healthy individuals. Current noninvasive neuromodulatory approaches like transcranial electric stimulation (tES) [4], transcranial magnetic stimulation (TMS) [2] and transcranial direct current stimulation (tDCS) [4] show promise in modulating the neural activities in both human and animals. However, these technologies also have constraints. They have limited spatial resolution, experience a tradeoff between depth and focality, and encounter significant attenuation when targeting deep neural tissue beneath the cortex [5].

Focused ultrasound (FUS) has been emerging as a non-invasive method, can deliver mechanical forces, which is in the form of an acoustic wave, to cells deep within the body [6]. This approach can precisely focus acoustic waves on specific locations, achieving spatial resolution on the order of the wavelength of the acoustic waves. High-intensity focused ultrasound (HIFU), has been applied for treating brain cancers and other neurologic disorders, in the way of permanently destroying a region of tissue in human body [2]. In contrast, transcranial focused ultrasound (tFUS) is a nonsurgical and low-energy method for inducing transient neural activities with high spatial resolution and adjustable focus [7]. tFUS targets deep neural structures with great precision. Focused ultrasound waves can inhibit the amplitude of somatosensory evoked potentials (SEPs) when targeted at the cortical regions responsible for generating these potentials [5]. [5] provides promising evidence that focused ultrasound can be utilized to noninvasively modulate subcortical areas of the human brain with better spatial precision and resolution (Figure 1.1). Unlike HIFU used for ablation, tFUS utilizes energy in an order of magnitude lower than HIFU, administered in short pulses [8]. By comparing all the methods above, we could see tFUS has great potential in the field of electroceutical therapies.

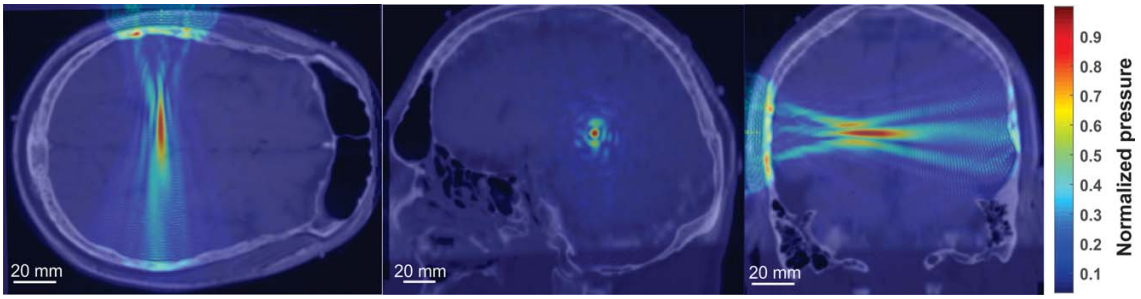


Figure 1.1: Acoustic modeling of ultrasound wave propagation [5].

1.2. Power-efficiency in wearable ultrasound systems

Modern ultrasonic systems are becoming increasingly complex and powerful and requiring the miniaturization of ultrasound system. The laptop-sized ultrasound systems have now reached a level of performance that rivals traditional cart-sized machines. The emergence of handheld devices like the GE Vscan exemplifies a growing trend towards highly integrated ultrasonic imaging solutions [9]. The development of ultrasound medical applications aim to facilitate portable and potentially wearable ultrasound devices, both within hospital settings and at home. Figure 1.2 shows the wearable low-intensity therapeutic ultrasound device proposed by [10]. It is approximately the size of a digital music player and provides a nominal 0.44 W of 2.95-MHz ultrasound pressure for 5 to 6 hours on a single charge.

Figure 1.2: A wearable self-applied therapeutic ultrasound device [10].

The miniaturization has an intimate relation with system power consumption. For example, smaller devices must use smaller batteries, which inherently have a lower energy capacity due to the small size. Some miniaturized devices have less surface area for dissipating heat, while high energy consumption typically generates more heat, requiring effective cooling mechanism, otherwise, the heat can damage the components. For wearable or portable ultrasound (US) devices, long-term mobility without the need for recharging or battery replacement is crucial. This mobility requires power-efficient devices so that they can operate longer on a sin-

gle charge. Thus, the trend towards miniaturization in ultrasonic systems while maintaining or improving performance creates a strong demand for enhanced power efficiency. It ensures the smaller designs does not come at the expense of functionality or lower pulsing duration, which are critical for medical devices.

The advancement of Integrated Circuits (ICs) represents an important stride in achieving the compactness and integration of ultrasound systems, which is attributed to the rapid development of the CMOS industry [11]. Power efficiency is always a challenge in ICs. For example, as ICs become more compact and powerful, they generate more heat. Efficiently dissipating the heat is crucial to avoid damaging the circuitry, but dissipating the heat also means energy loss. Even when a transistor is in the off state, there is some minimal current flowing as leakage current, leading to wasted power. Dynamic power consumption is related to the charging and discharging of capacitors in ICs. Increasing clock frequencies can significantly increase dynamic power. This is also the main power consumption in a pulser in US system, which would be explained in following chapters.

In an ultrasound transmitter, the pulser drives the US transducer with high voltage (HV) pulses to generate ultrasound pressure. However, the pulser could be seen as the most power-consuming part in the transmitter stage. There are several reasons for this. Ultrasound transducers typically require high voltage signals to generate the ultrasonic waves. The pulser circuit is responsible for generating these high-voltage pulses, consuming a large amount of power. Moreover, the ultrasound transducers have parasitic capacitance. To convert the electrical energy to acoustic energy, a considerable power would be used to charge and discharge the parasitic capacitor of the US transducer. In order to avoid overheating, the ultrasound transducer should be discharged to the ground in every cycle.

Because of the requirements for generating bursts of continuous waves with high voltages and high frequencies in neuromodulation applications, pulsers remain a power-consuming block in the system. Efforts have been made to improve the power efficiency for the pulser circuits in ultrasonic system. [12] proposed an energy-replenishing pulser. It could ideally eliminate the dynamic power loss on the capacitor in the transducer by replenishing the supplied energy from the magnetically stored energy in an inductor. While having ideally zero energy loss, most of these circuits need large inductors, which would significantly increase the system volume. [13] introduced a charge redistribution technique. The general principle is to re-use half of the charge at each cycle by connecting both plates of the transducer together. However, the requirement for bimorph pMUT leaves this pulser a comparatively narrower application. [2] utilizes the multilevel pulsing with charge recycling to improve pulser's power efficiency. However, the capacitors it uses in the dc-dc converter are large and have to be off-chip. In conclusion, the published designs could not be perfect in all aspects. One can never design a pulser with low power consumption, low area, high-voltage operation, simplicity and wild application in the same time. This work aims to strike a balance between power consumption, high-voltage operation and low area to fit in a 2D pitch-matched architecture.

1.3. Thesis organization

This thesis project aims to design a power-efficient pulser for 2D ultrasound phased-array transmitters. As the circuit area is limited by the resonant frequency of the transducer, the area-efficiency is also focused as an important aspect. This thesis is organized as follows:

Chapter 2 presents the research background and prior works. A system-level study of an ultrasound transceiver is presented. There's also a detailed description for the US transducer used

in this project, including the Lead Zirconate Titanate (PZT) electrical model and the working principle of the 2D-Array US transducer. Then a specific analysis for the power consumption in the conventional class-D pulser based on the BVD model is introduced. This chapter also reviews some prior arts from previous work and scientific publications, reformulating the research questions complying with the state of the art.

Chapter 3 presents the proposed power-efficient high-voltage pulser. The system-level design is first described. In this part, the operation of the 5 switches are elaborated. Then the circuit implementation is presented, including the choice for the PZT transducer model, and the design process for the stacked CMOS switches and the level-shifter.

Chapter 4 presents the simulation results. The results from Parametric Analysis are presented first to show the choice-making process for the width of the transistors and the capacitor. Then the transient waveform is shown. This chapter also presents several comparison between the proposed pulser and other design choices.

Chapter 5 concludes the thesis with the summarization for the main contributions of the thesis, a reflection on the project, and provides recommendations and suggestions for future work.

2

Background and prior works

2.1. Ultrasound transceiver system

2.1.1. The system-level study

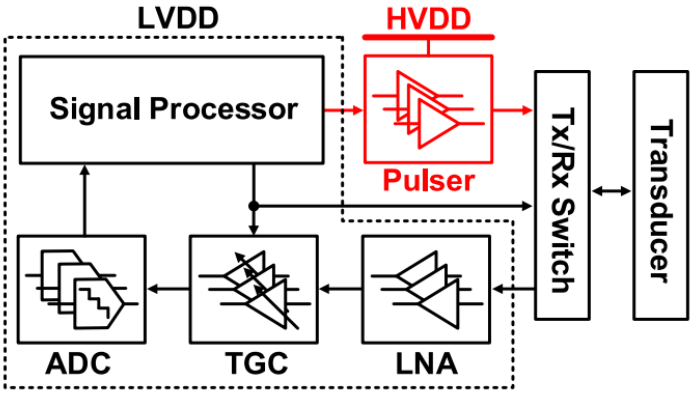


Figure 2.1: Block diagram of the ultrasound transceiver system [14].

It's necessary to understand the system as a whole to enhance one's cognition for how the individual modules interrelate. Figure 2.1 illustrates the architecture of a standard US transceiver [14]. Ultrasound imaging applications require transmit chain, including pulser and Tx/Rx switch, and a receive chain, including LNA, TGC, ADC, and signal processor. In ultrasound neuromodulation applications, only pulser and a controlling system, in this system the signal processor, are required. A detailed description for every block is presented here.

- **Transducer:** This is the device that converts electrical signals into ultrasound waves and vice versa. In the application of ultrasound imaging, it sends ultrasound waves into the body tissue and receives the echoes to form an image of the tissue. In ultrasound neuromodulation, the transducer only converts the electrical pulses to ultrasound waves.
- **Tx/Rx Switch:** It directs the high-voltage pulses from the pulser to the transducer during the transmit mode and protects the low-voltage supplied receiving circuitry from these high-voltage pulses. During the receive mode, it allows the returning ultrasound signals to be passed to the receiver circuitry. This switch is only required for ultrasound imaging applications.

- **Pulser:** The pulser generates the electrical pulses to drive the transducer to generate ultrasound waves. These pulses are typically high-voltage pulses to form a high-intensity ultrasound focal spot which is required for US neuromodulation applications.
- **LNA (Low Noise Amplifier):** This component amplifies the small electrical signals that are received back from the transducer after the ultrasound waves have been reflected back from the tissue. It amplifies these signals while enabling the noise to be as small as possible, ensuring a clear signal is sent to the next stage in ultrasound imaging applications.
- **TGC (Time Gain Compensation):** As ultrasound waves penetrate deeper into tissue, they lose energy and the echoes become weaker. TGC could increase the amplification gain of received echoes that take longer to return, compensating for the loss of signal strength over time/distance.
- **ADC (Analog-to-Digital Converter):** ADC converts the received analog signals into digital data, to form an image using a signal processor.
- **Signal Processor:** During the transmit mode, the signal processor is responsible to initiate a new process by sending pulses to the pulser unit. During the receive mode, this digital processor handles the digital signals from the ADC. It processes the data to create the image in ultrasound imaging applications.

The process begins with a signal processor directing the pulser to generate high-voltage pulses. The output of the pulser could be various shapes, such as square pulses, sine waves and Gaussian pulses [11]. These pulses are sent to the transducer via the Tx/Rx switch. The pulser drives the transducer to emit ultrasound waves by transforming electrical pulses into acoustic waves, which are then emitted into the body for neuromodulation or imaging purposes. For ultrasound neuromodulation, these waves are focused on specific neural structures to modulate their activity.

During receive mode for ultrasound imaging, the reflected echoes from the tissue are captured by the transducer and converted back into electrical signals. The Tx/Rx switch now directs these weak signals to the RX chain. The returned signal is amplified by a low-noise amplifier (LNA), adjusted for signal strength over time with a time gain compensation (TGC) amplifier, and finally transformed into a digital format by an analog-to-digital converter (ADC) for post processing [15, 16].

The delay between the transmitted US waves and received echoes is related to the object's distance from the transducer. Additionally, the amplitude of the echo's signal not only varies with the distance but also depends on the object's acoustic properties. Using the timing and strength of these echoes, the signal processor form an image.

In the receiver (RX) chain and the signal processor, a low supply voltage ranging from 1.8 to 5 volts is typically used to maintain system efficiency [14]. In contrast, the pulser operates on a high supply voltage, for example, ten to several tens of volt, which is essential for achieving a high signal-to-noise ratio in US imaging applications and forming a high-intensity focal spot in neuromodulation applications. HV pulser is the most power-consuming block in neuromodulation applications. That's because the pulser is needed to generate bursts of continuous waves, keeping ON for most of the time during stimulation. Therefore, the design of the pulser is critical and must be carefully optimized for lower power consumption in ultrasound neuromodulation systems. Developing high-voltage, an energy-efficient pulser is one of the keys

in enabling further miniaturization of ultrasound technology in both therapeutic and diagnosis applications.

2.1.2. The ultrasound transducer

2.1.2.1 Bulk piezoelectric transducers

Ultrasound waves can be generated by different kinds of US transducers. Piezoelectric material transducers, capacitive micromachined ultrasonic transducers(CMUTs) and piezoelectric micromachined ultrasonic transducers (PMUTs) are the three main classes of ultrasound transducers. Table 2.1 provides a comparison for these three kinds of transducers [11]. Since bulk piezoelectric transducers have higher transmit efficiency, they can improve the overall power efficiency of the system. In this regard, this research thesis aims to develop a power-efficient pulser which is compatible with the bulk piezoelectric transducers.

Table 2.1: COMPARISON OF ULTRASOUND TRANSDUCERS

	PZT	PMUT	CMUT
Pros	Higher transmit efficiency	CMOS compatible No need for large dc bias	CMOS compatible High bandwidth
Cons	Not CMOS compatible Lower bandwidth	Low transmit efficiency	Needs large dc bias

The bulk piezoelectric material is the most commonly used commercial transducer. It consists of a top electrode and a bottom electrode at two sides separately, and a piezoelectric material core in the middle, as shown in Figure 2.2. Lead zirconate titanate (PZT) stands out as the preferred piezoelectric material for its exceptional longitudinal piezoelectric coefficient [17]. PZT transducers work on the piezoelectric effect: they can convert a changed mechanical pressure into an electric field and vice versa, whereby a changed electric field could induce mechanical strain from a thickness modulation of the piezoelectric layer [11].

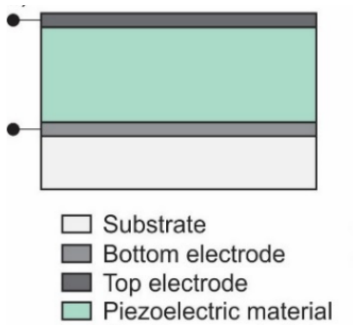


Figure 2.2: A bulk piezoelectric material transducer.

There's usually a separate layer, named impedance matching layer, placed on top of the piezoelectric material. This matching is crucial for maximizing the transfer of ultrasonic energy between the transducer and the human body. A backing layer is usually located on the bottom of piezoelectric material, improving the transmit efficiency. For specific uses, designing external impedance matching circuits may also be necessary to optimize the transducer's performance.

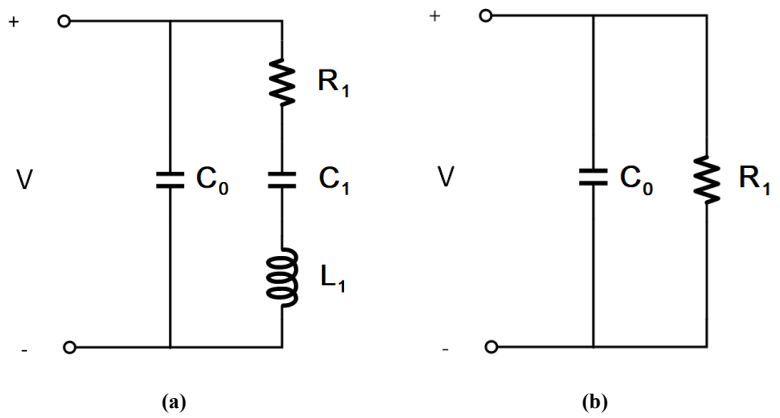


Figure 2.3: (a) BVD model for a single resonant frequency PZT transducer (b) Simplified BVD model.

2.1.2.2 PZT Transducer equivalent circuit model

There has been plenty of works dedicated to modeling the PZT transducer into an equivalent circuit. The Mason, Redwood, and Butterworth-Van Dyke (BVD) models are commonly used equivalent circuits for a piezoelectric ultrasound transducer [18]. Figure 2.3a is a BVD model to represent an equivalent circuit of a single resonant frequency transducer.

The whole BVD model can be seen as a band-pass filter highlighting the resonant nature of PZTs [11]. In this model, the clamping capacitor C_0 represents the equivalent capacitance due to piezoelectric elements and cables, connections, etc. The resistor R_1 models the mechanical and radiation loss. As the mechanical power losses are negligible, the power supplied to R_1 could mimic the acoustic power dissipation. The capacitor C_1 and the inductor L_1 models the transducer's resonant performance. When a pulse is applied to the transducer, the electrical energy is converted into acoustic energy, which corresponds to the current flowing into the motional branch composed of C_1, L_1 and R_1 [14]. The value of all components in the motional branch should be determined carefully, such that the resonant frequency and the Q factor of this RLC circuit could match the PZT transducer's mechanical resonance.

The admittance of a single-frequency BVD is calculated in Equation (2.1).

$$Y = \frac{j\omega^2 C_1 R_1 C_0 - (\omega C_0)(\omega^2 L_1 C_1 - 1) + \omega C_1}{R_1 \omega C_1 + j(\omega^2 L_1 C_1 - 1)} \tag{2.1}$$

The magnitude of this admittance could achieve the maximum value at the series resonance, which means the series angular frequency can be calculated by setting the imaginary part of the denominator of Equation (2.1) to zero [19].

$$\omega_s = \frac{1}{\sqrt{L_1 C_1}} \tag{2.2}$$

At $\omega = \omega_s$, Equation (2.1) is reduced to

$$Y(\omega_s) = \frac{1}{R_1} + j\omega_s C_0 \tag{2.3}$$

At this resonant frequency, the BVD transducer model is usually simplified as a capacitor in parallel with a resistor, as shown in Figure 2.3b.

2.1.2.3 2D phased-array Ultrasound Transducer

Ultrasound technology is undergoing a revolutionary shift from traditional imaging to advanced applications such as neuromodulation and power delivery for medical implants. Traditional single-element ultrasound transducers have been commercially utilized thanks to their simple structure [20]. However, these transducers come with significant limitations, including large sizes, fixed focal spots, and the need for physical repositioning to change the focal spot. The 2D ultrasound phased array transducer is the promising generation of ultrasound transducers, allowing developing advanced ultrasound applications.

The necessity for 2D ultrasound phased-array transducers stems from their multiple advantages over single-element transducers. Most importantly, phased arrays can electronically steer and focus ultrasound beams without moving the probe, offering greater control and precision in targeting [21]. This ability benefits applications like neuromodulation, where precise targeting is required to modulate neural activity non-invasively. Furthermore, phased arrays with their electronic beam steering can achieve high spatial resolution and power efficiency necessary for both neuromodulation and power delivery [22]. This is due to their capability to produce focused ultrasound waves with configurable parameters for each array element.

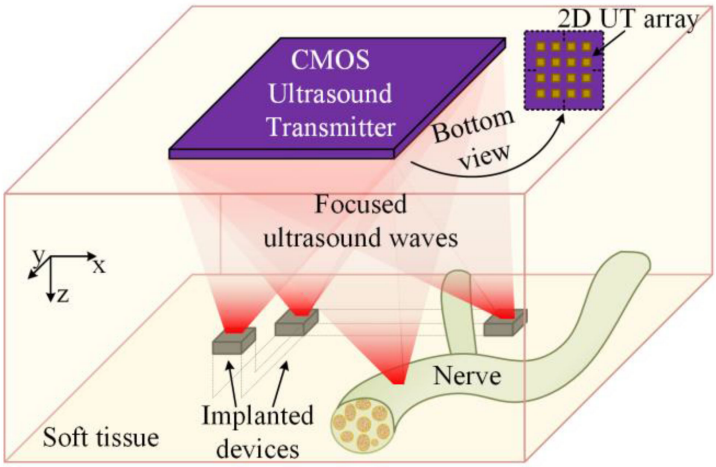


Figure 2.4: Conceptual diagram showing operation of a 2D array with 3D control of focal spots [20].

Figure 2.4 is a conceptual diagram showing operation of a 2D array with 3D control of focal spots [20]. The architecture of a 2D phased array transducer comprises a grid of transducer elements, each individually controlled by an integrated circuit (IC). This configuration facilitates a dense array of small, highly sensitive piezoelectric transducer elements, typically made of lead zirconate titanate (PZT), which can be electronically managed to generate ultrasound waves with high precision and variable focal depths. By integrating the transducers directly onto complementary metal-oxide-semiconductor (CMOS) ICs with microfabrication techniques, the array benefits from reduced size and parasitics, enhanced performance at higher frequencies, and scalability in terms of array dimensions and frequency ranges.

When designing the ICs for these 2D phased array transducers, designers face a set of challenges.The specific wave parameters are required for high-resolution volumetric control. To enable the fine-tuning of these wave parameters, the design must accommodate the precise control of the delay and pulse duration for each transmitter within the array [20]. Additionally, the IC must maintain low parasitic capacitance while allowing for high-frequency operation, which is vital for reducing the focal spot size and achieving the resolution required for targeted

medical therapies. The pursuit of a single-chip integration in line with the "more-than-Moore" paradigm further demands innovation in overcoming physical and manufacturing constraints, which includes balancing transmitter aperture size with resolution and sensitivity. [20] proposed a 10 MHz 26x26 2D phased array ultrasound transmitter in a single chip. This design utilizes continuous-wave signals, which not only enable higher power for ultrasound-powered implants but also fulfill the pulse duration demands of neuromodulation.

2.1.3. Pulsers

2.1.3.1 Pulsers in US system

Pulser generates high-voltage pulses to drive the ultrasound transducer. These pulses are then converted into mechanical waves by the ultrasound transducer, which in turn become the sound waves that propagate through the body's tissues. The function of the pulser is to initiate the ultrasound waves and to control the timing and intensity of their emission. It ensures the precise moments when the transducer elements send out sound waves and these elements are activated in the right sequence and with the proper voltage. This sequential firing is crucial for steering the ultrasound beam to deliver acoustic energy to targeted tissues.

High-voltage pulsers are commonly used in medical ultrasound applications, because the intensity of the ultrasound wave is proportional to the driving voltage, while the former determines the depth the ultrasound wave can penetrate and the resolution of the images. Higher voltage translates into higher energy ultrasound waves, which in an ultrasound neuromodulation system can deliver more concentrated acoustic energy to a specific location within the body. Usually, the use of high-voltage pulsers must be carefully balanced with patient safety and the specific application requirements. For example, in ultrasound neuromodulation applications, high-voltage pulses enable the modulation of the neural activity in a controlled manner. In diagnostic imaging applications, higher voltages are typically used to penetrate deeper into body tissues and obtain high-resolution images.

2.1.3.2 Power consumption analysis for the conventional class-D pulser

Normally, pulser is the component consuming the most power within ultrasound system in neuromodulation applications, primarily because of the parasitic capacitance associated with the transducer and the requirement for continuous waves [12].

Let's look back to Figure 2.3, the equivalent circuit model of a PZT transducer. The power dissipated by R1, due to the electrical pulse's fundamental frequency component, models the useful acoustic power delivered into the medium [9]. The power dissipated on C0, on the other hand, does not contribute to the acoustic output, but is wasted during the charging and discharging phases. That is because the energy charged on C0 must be discharged. Otherwise, the charged energy should be dissipated within the transducer, resulting in a heating problem [14]. With a conventional ultrasound pulser, during the charging phase, the top electrode of the transducer is connected directly to the supply voltage. During the discharging phase, the top electrode is connected to the ground. In this case, all the charges gathered on the electrodes are discharged to the ground, which results in a total power consumption as shown in Equation (2.4).

$$P_{TOTAL} = C_0 V^2 f \tag{2.4}$$

For higher acoustic energy that the transducer transforms, a larger size of the piezoelectric transducer is necessary, which leads to an inevitably larger parasitic capacitance. This is the

reason why the capacitor C0 is the main culprit of the large power consumption [13].

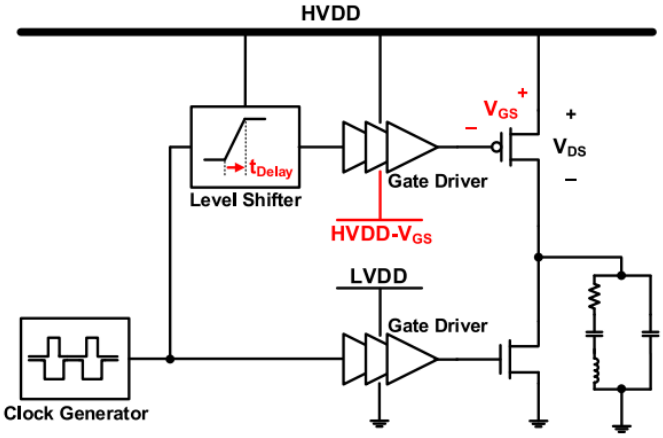


Figure 2.5: Conventional class-D pulser using HV transistors [14].

Among different ultrasound pulsers, the conventional class-D pulser is the most commonly used one. As shown in Figure 2.5, a class-D pulser is based on a simple inverter structure, implemented using two HV CMOS transistors. The principal of the operation of this circuit is as follows. When the high-voltage PMOS is turned on and the high-voltage NMOS is turned off, the transducer is directly connected to HVDD and the parasitic capacitor of the transducer is fully charged. When the high-voltage NMOS is turned on and the high-voltage PMOS is turned off, the transducer is connected to the ground and the parasitic capacitor of the transducer is discharged to the ground.

Although the conventional class-D pulser has a simple structure and operation principle, the power loss $CHVDD^2f$ could be a critical problem. Moreover, as the high-voltage transistors have lower on-resistances by being implemented with large sizes, their large gate capacitors introduce even more power burden that can not be neglected.

The high-voltage NMOS transistor is driven by a low-voltage signal with logic levels 0 and LVDD, where the LVDD is the low-voltage power supply. To properly trigger the gate of the high-voltage PMOS, a level-shifter is needed to convert the low-voltage signal to a signal between HVDD and HVDD-V_{th}. One advantage of high-voltage transistors is that they could tolerate higher drain-source voltage V_{ds}. However, the limited gate-source voltage does not become larger.

Previous works [23, 24] have integrated a T/R switch in a conventional class-D pulser to reduce the amount of transistors and the occupied area. The proposed HV pulser is shown in Figure 2.6. M1 and M2 are HV transistors, acting as pull-up and pull-down switches, respectively. As M2 could prevent the node RX from being above a specific breakdown voltage, they implemented M3 by a small 5-V transistor. During the transmission mode, M3 remains on. M1 and M2 work in the same way as the high voltage transistors in Figure 2.5. During the receive mode, M2 is turned on to conduct incoming signals to the receive electronics while M1 and M3 are turned off [23].

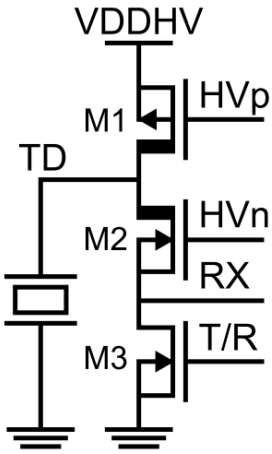


Figure 2.6: Structure of a unipolar pulser [9].

2.2. State-of-the-art power-efficient HV pulsers

2.2.1. Power-efficient HV drivers

To improve the power efficiency of a pulser, many related works were dedicated to this field. In this section, some energy-efficiency enhancement methods will be described. In ideal cases, the energy spectrum of the transmitted pulse should be concentrated within the effective bandwidth of the transducer' s transfer function to achieve the best possible response [11]. Thus, a key point which impacts the energy distribution in the transmitted pulse's spectrum, the level of acoustic energy transformation, and the dynamic power utilization is the pulse shape. Some works show that there are potential benefits to improve the power efficiency in utilizing different pulse shapes beyond the standard digital square-wave format, for example, multi-level waves and continuous sine waves. This section delves into a discussion of two classes of pulsers: square-wave pulsers and multi-level pulsers.

2.2.1.1 Square-wave output drivers

A. Energy replenishing ultrasound pulser

To harvest the energy from the supply and reduce the dynamic power consumption, some designs utilized inductors in theirs pulsers [12][25, 26].

The energy-replenishing (ER) pulser proposed in [12] could ideally eliminate CV^2f loss by replenishing the supplied energy from the magnetically stored energy in an inductor. As Figure 2.7 shows, the ER pulser comprises four high-voltage power switches, an inductor, and a switching time controller. Its operation involves four phases, namely Φ_1 to Φ_4.

During Φ_1, M_{P2} is turned on, and current I_{IND} flows from HVDD to the transducer, enabling the charging of energy in both L and C_P with ideally none energy loss. When V_{OUT} attains HVDD, all power switches are turned off, marking the begin of Φ_2. In Φ_2, inductor energy compels I_{IND} to pass through the parasitic junction diodes of M_{N2} and M_{P1}, thereby returning the energy stored during Φ_1 to the power supply.

Subsequently, between Φ_2 and Φ_3, M_{P1} and M_{P2} are simultaneously turned on to ensure complete depletion of stored energy in L. At the declining edge of CLK_{EXT}, Φ_3 initiates, converting the electrical energy stored in C_P into magnetic energy within L by turning on

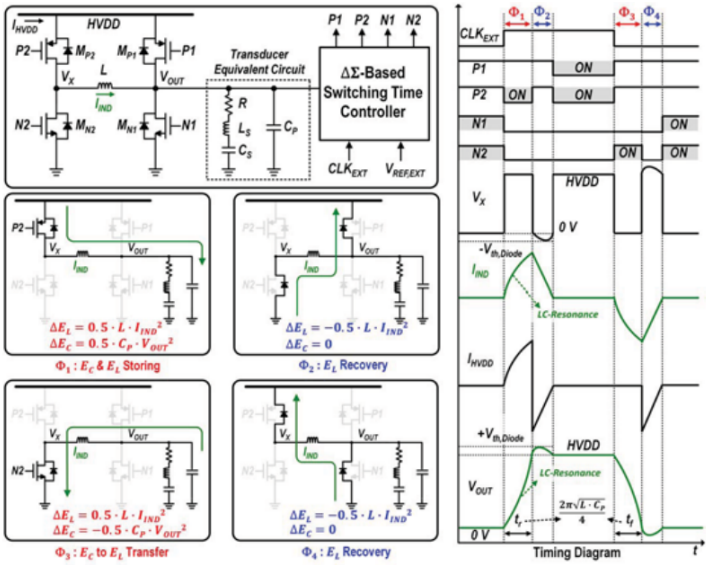


Figure 2.7: Operation of the ER pulser in 4 phases-Φ_1:E_C & E_L storing, Φ_2: E_L recovery, Φ_3:E_C to E_L transfer, Φ_4: E_L recovery [12].

M_{N2}. When V_{OUT} reaches 0V, Φ_4 is triggered, facilitating the return of energy accumulated in L during Φ_3 back to the power supply. Consequently, the entire energy drawn from the power supply to charge C_P in Φ_1 is reimbursed to the supply during Φ_2 and Φ_4. After Φ_4, both M_{N1} and M_{N2} are turned on to ensure the thorough discharge of energy stored in both L and the transducer.

The measurement results showed this design has a 73.1% of power efficiency enhancement, which is a drastic improvement compared to conventional pulsers. The energy-replenishing circuit has ideally no-charge wastage though, most of these circuits require large inductors, which would significantly increase the system volume. In systems that have a stringent requirement for the area limitation, this idea can not be utilized.

B. Charge redistribution technique

Although the energy-replenishing pulser using inductors is one of the most energy-efficient circuits with ideally no energy wastage, the large inductors most of these reported pulsers required occupy a large system volume, which is not desirable for portable applications. There's a charge redistribution technique proposed for driving PMUT array at a wide frequency range [13].

The general principle is to re-use half of the charge at each cycle by connecting both plates of the transducer together. As shown in Figure 2.8, during the charging mode, the DRIVING electrode is charged to VDDH, while the GROUND electrode is connected to the GND. When discharging mode starts, the DRIVING and GROUND electrode are shorted with each other. This action causes both electrodes to approach a voltage close to VDD/2. Consequently, there is no voltage applied across the piezoelectric layer, leading to relaxation of the material and the membrane. In next charge mode, each electrode only need to charge/discharge by VDD/2, instead of charging up a full VDDH swing. By recycling half of the initial charges, theoretically the total power dissipation for this capacitor driving is reduced to:

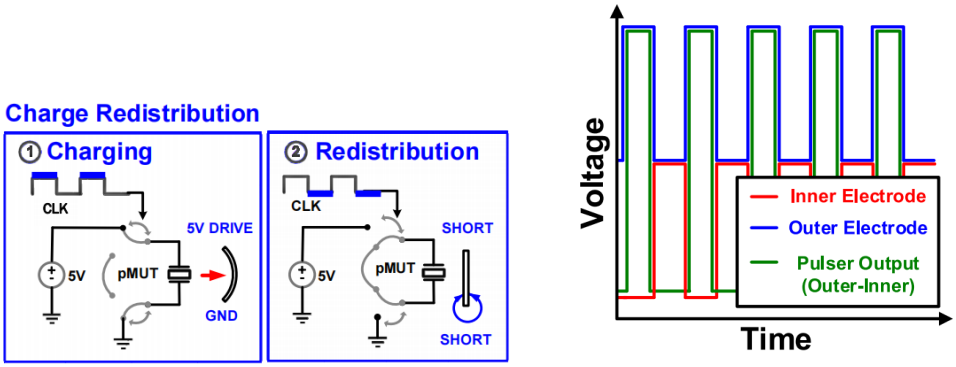


Figure 2.8: (a) Charge redistribution scheme and (b) operation wave forms.

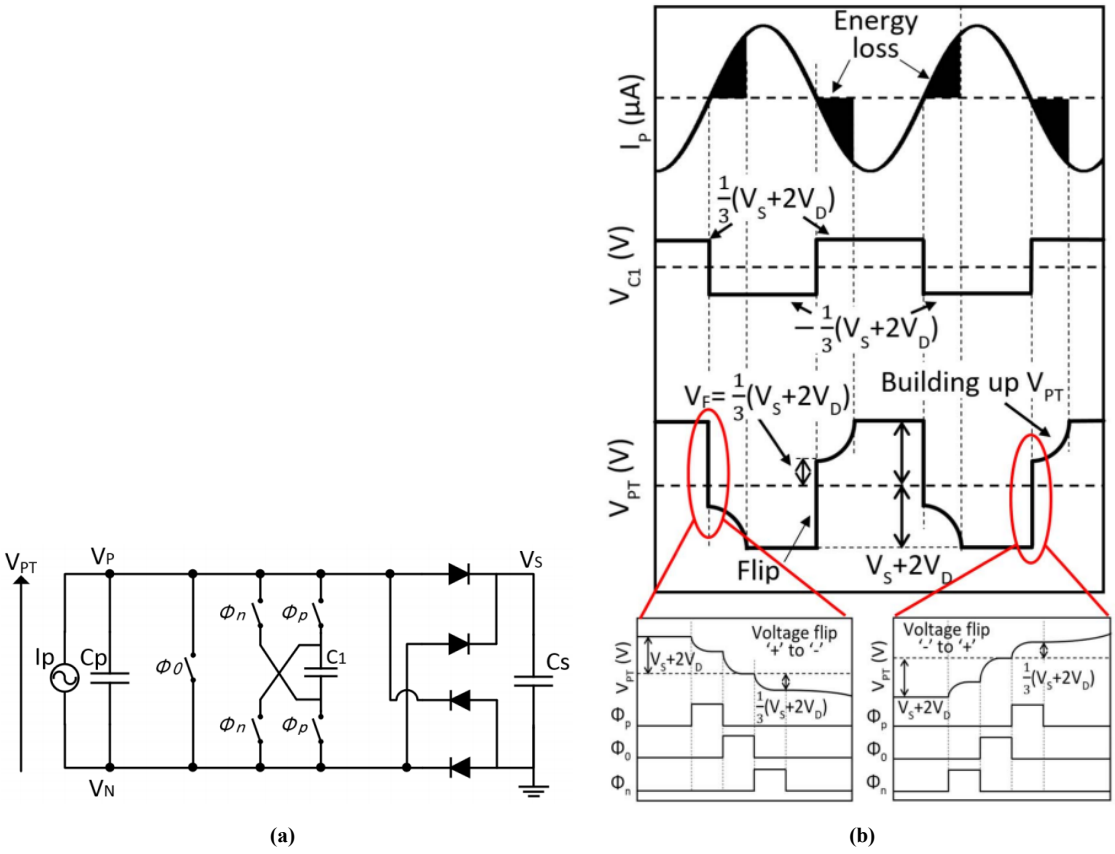


Figure 2.9: (a) SSHC interface circuit with one charge-swap capacitor (b) Waveform [27].

$$P_{TOTAL} = \frac{1}{2}CV^2f \tag{2.5}$$

According to the measurement in real circuit, a total power reduction of 32.8% is achieved.This design has an on-chip implementation. However, as both electrodes require switching circuit, this pulser needs more complex control blocks. In addition, the requirement for bimorph PMUT leaves this pulser a comparatively narrower application.

[27] proposed an energy harvesting circuit for piezoelectric transducer. Essentially this is also a charge redistribution method to save dynamic power consumed by transducers. Figure 2.9a shows the circuit diagram of the proposed SSHC (synchronized switch harvesting on

capacitors) interface circuit, and Figure 2.9b shows the waveform of I_p, V_{C1}, V_{PT} and the three pulse signals driving the 5 switches.

The piezoelectric transducer is modeled as a current source I_p in parallel with a capacitor C_p. During each zero-crossing moment of the current signal I_P, three pulse signals, namely Φ_P, Φ_0, and Φ_n, are generated sequentially to change the voltage across V_{PT}. Assuming that V_{PT} is initially equal to $V_S + 2V_D$ before the switching event, we intend to reverse the polarity of V_{PT} to the negative side. In this scenario, the pulse signal Φ_P is the first to be generated, diverting a portion of the charge from capacitor C_P to the charge-swap capacitor C_1. Subsequently, the pulse signal Φ_0 clears any remaining charge in capacitor C_P, and the pulse signal Φ_n transfers charge from C_1 back to C_P in the opposite direction, thereby partially flipping the voltage across the transducer. To change V_{PT} from $-(V_S + 2V_D)$ towards a positive polarity, the order of generation for the three pulses is reversed.

After the operation of these three pulse signals, V_{PT} could achieve near -/+ 1/3 ($V_S + 2V_D$), which means 33.3% of power is saved here.

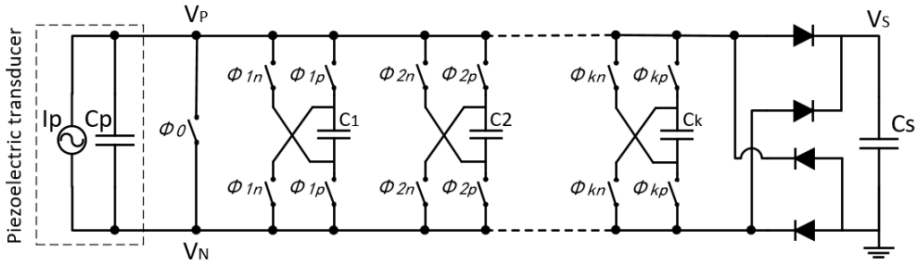


Figure 2.10: SSHC interface circuit with k SCs [27].

By adding more synchronized swap capacitors, more charge could be transferred, so, more power would be saved. Figure 2.10 is the SSHC interface circuit with k SCs. According to calculations, $C_k = C_P$ is the condition when transferred energy from C_P to C_k is maximum [27]. In the case of 8 SCs in the circuit, the power efficiency could achieve 80%, theoretically.

C. Supply-doubled technique

In addition to energy replenishing techniques and charge redistribution techniques, the supply-voltage-doubled technique is also a way to reduce power consumption. [28] utilizes bootstrapping technique to double the supply voltage in a pulser interfacing with CMUT.

The proposed pulser utilizes double-diffused metal oxide semiconductor (DMOS), Schottky diodes, and Zener diodes, as shown in Figure 2.11 The supply voltage HV_{DD} is 45 V. Two N-DMOS, M_1 and M_3 are driven by 0-5 V control signals. Two P-DMOS M_2 and M_6 are driven by 40-45 V signals generated by level-shifters. M_4 and M_5 are dynamically gate biased.

During the 1st phase, M_3 is turned on so that V_{out} is 0 V. M_4 is connected with pull-up resistor to LV_{DD}=5 V. In phase 2, M_1 and M_6 are turned on, and C is charged up to $HV_{DD} - (V_{D2} + V_{D3} + V_{D4})$. M_5 remains off because of the existence of D_2. During the 3rd phase, M_2 and M_5 are turned on while other transistors are turned off. The output voltage V_{out} is bootstrapped to near $2HV_{DD}$. M_5 is turned on because D_2 is reversed biased with a 5-V voltage. D_3 and D_4 are added to make sure M_6 operates in the safe region during the voltage doubling phase. The V_{out} is calculated as follows:

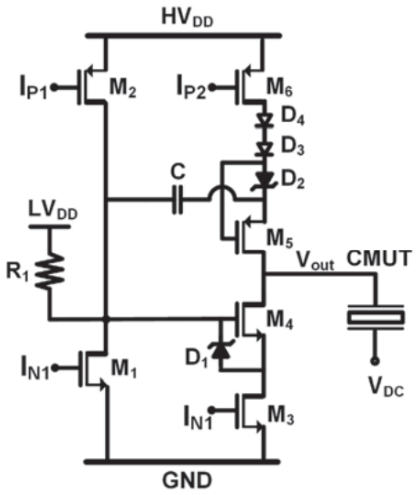


Figure 2.11: Voltage doubled pulser [28].

$$V_{cap} = HV_{DD} - (V_{D2} + V_{D3} + V_{D4}), \tag{2.6}$$

$$V_{out} = HV_{DD} + V_{cap} \times \frac{C}{C + C_{CMUT}}, \tag{2.7}$$

where C_{CMUT} is the equivalent capacitance of the CMUT. In the 4th phase, V_{out} is pulled down to 0V by M_3, leading to the completion of the sharp two-level pulse generation.

The supply-doubled technique requires lower supply voltage, so that it consumes lower power compared with the conventional pulser. However, in practice C is always chosen $\sim 12 \times C_{CMUT}$ [28], making it hard to be implemented on chip.

D. Stacked CMOS architectures

All the pulsers mentioned above utilize high voltage process technology to facilitate high-voltage operation. Problems of increased process cost, bulkier physical area capitation with larger parasitic components and the incompatibility with the most advanced process nodes are inevitable. To avoid these troubles, many works like [28-30] proposed high voltage pulsers adopting stacked transistors that are fully compatible with standard CMOS process, while the safety operation of transistors has to be guaranteed by dynamic gate biasing techniques. The gate biasing technique will be discussed in 2.2.2.2.

Figure 2.12 displays the high-voltage output driver circuit used in the pulser proposed by [29]. This pulser is capable of consistently generating 15 V_{pp} pulses. The biasing circuit ensures that the voltage difference between the terminals of the stacked transistors under 3.3 V. External bias voltages, labeled as VB1 to VB4, are applied. The design employs five sets of 3.3-V PMOS and NMOS transistors. When the NMOS input terminal IN_N transitions from a LOW to a HIGH state, M_{N1} is turned on, subsequently turning on M_{N2}. This causes the drain node of M_{N2} to discharge, turning on M_{P6} and shorting the gate of M_{N3} to VB1, which is held at 3.3 V. This, in turn, turns on M_{N3}. A similar sequence of events applies to M_{P7}, M_{N4}, M_{P8}, and M_{N5}. While the NMOS stack is fully turned on, the PMOS stack is turned off, and vice versa.

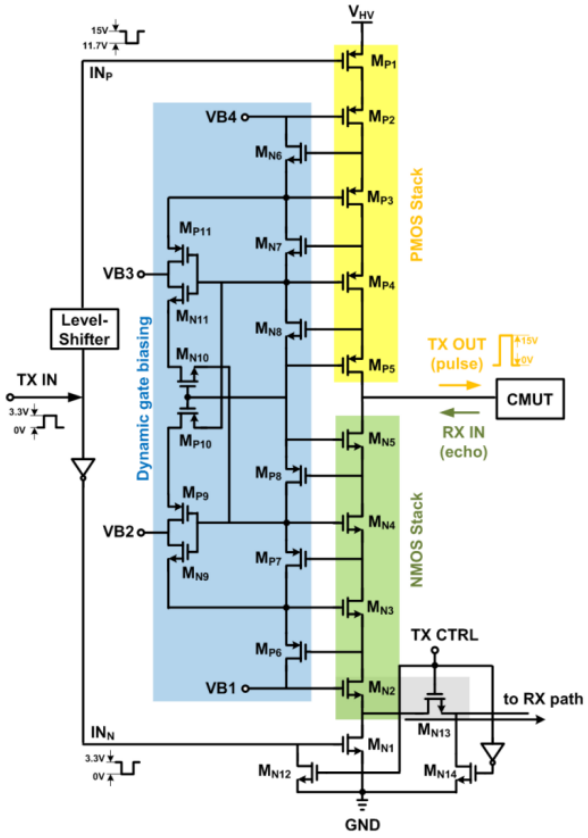


Figure 2.12: Pulser with stacked standard CMOS transistors [29].

Embedded within the reconfigurable output driver, transistors M_{N2} to M_{N5} and M_{N13} function as isolation switches to prevent high voltage from affecting the RX circuits during the TX mode.

As shown in Figure 2.13, [30] adopts a similar stacked architecture, except for utilizing a bipolar output current driver. By the control of digital signals, this output current driver can generate the stimulation current through the tissue to produce cathodic and anodic current pulses. Compared with monopolar output drivers, the desired voltage compliance is achieved with less supply voltage.

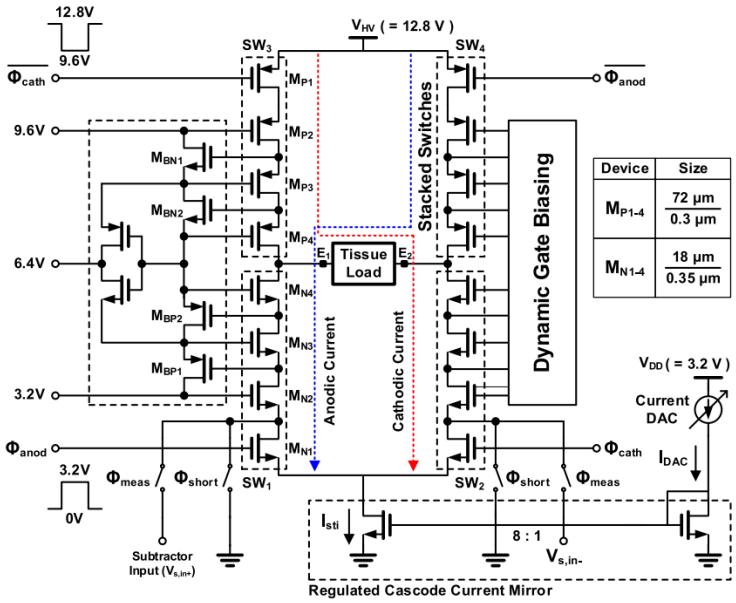


Figure 2.13: Bipolar output current driver with stacked standard CMOS transistors [30].

The pulser proposed in [31] combines the stacked architecture with the charge redistribution technique mentioned in subsection B. As shown in Figure 2.14, $M_1 - M_6$ are stacked with staggered potentials driving a PMUT in standard CMOS progress. The two operation phases including the charging phase and the redistribution phase have been introduced in B.

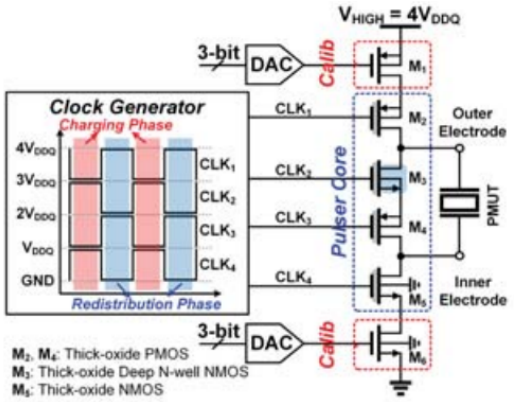


Figure 2.14: Charge redistributed pulser with stacked architecture [31].

2.2.1.2 Multilevel-wave drivers

A. Three-level pulse shaping

A three-level pulse-shaping pulser is presented in [9]. This work utilizes the multilevel pulsing with charge recycling to improve pulser's power efficiency. The power saving mechanism is as follows: in an N-level pulser, during the discharge operation when the load capacitor is switched from one voltage level to the next lower one, instead of discarding all the charge CV to ground as in conventional square-wave pulsers, a charge packet of CV/(N-1) is recycled back to the power supply [32]. When the last packet is dumped to ground, total

charge of (N-2)*CV/(N-1) is recycled. This method reduced the dynamic power from CV^2f to $CV^2f/(N-1)$.

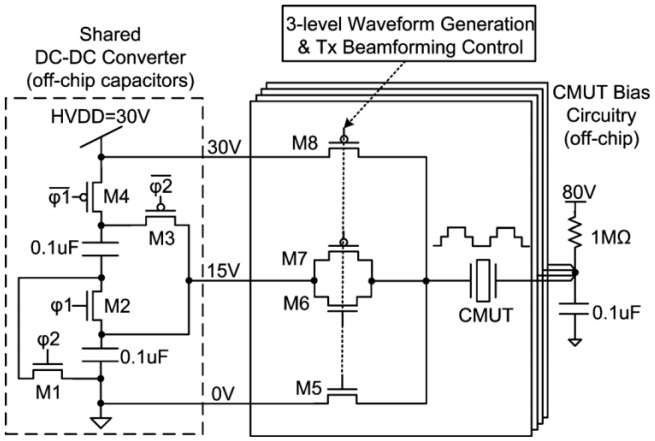


Figure 2.15: A four-channel three-level pulser with the middle-voltage generation [9].

Figure 2.15 shows the three-level (30, 15, and 0 V) pulser implementation. A switched-capacitor dc-dc converter consisting of M1-M4 is used to generate the 15-V middle voltage. This converter is shared between channels. In each channel, there are four high-voltages switches M5-M8 to implement pulse-shaping. M5 and M6 are responsible for transitions of $15 \rightarrow 0V$ and $0 \rightarrow 15V$, respectively. M7 and M8 are used for the transitions of $30 \rightarrow 15V$ and $15 \rightarrow 30V$, respectively.

According to the measurement results, this design successfully reduced 38% power compared with the conventional 2-level pulsers. However, the two capacitor in the dc-dc converter should be large enough to be served as stable voltage sources, so off-chip components are inevitable.

B. Supply-Doubled Three-Level Pulser

A supply-doubled 3-level pulser employing bootstrap circuit combined with dynamic gate biasing technique is presented for CMUT in [33]. The circuit operation is similar to the bootstrapping circuit in subsection C in 2.2.1.1 .

As shown in Figure 2.16, in the charging mode, by turning on transistors M_1 and M_5, the external capacitor C is charged to a voltage level of V_{DD} - ($V_{D2} + V_{D3}$), where ($V_{D2} + V_{D3}$) represents the combined forward voltage drop across D2 and D3. Once the capacitor C is fully charged, by turning on M2 while turning off all other transistors, Vout reaches to a level of $2V_{DD}$ - ($V_{D2} + V_{D3}$). During the third phase, the transistors' operation is same as the charging phase, so that the output voltage shows V_{DD} - ($V_{D2} + V_{D3}$) again.

In the process this design used, the drain-source junction breakdown voltage for the DMOS is 60V, while the gate-source breakdown voltage is 5V. D_2 and D_3 are HV Schottky diodes that are used to prevent excessive V_{DS} during doubling mode. The two stacked N-type DMOS M_3 and M_4 are also used for the safe operation when V_{out} is doubled.

The required C in this design is suggested to be at least $4 \times C_{CMUT}$ by theoretical equation, but in practice this capacitance is often 10 to 15 times larger than C_{CMUT}. Using off-chip components would be inevitable. A potential advantage of the proposed pulser is that this

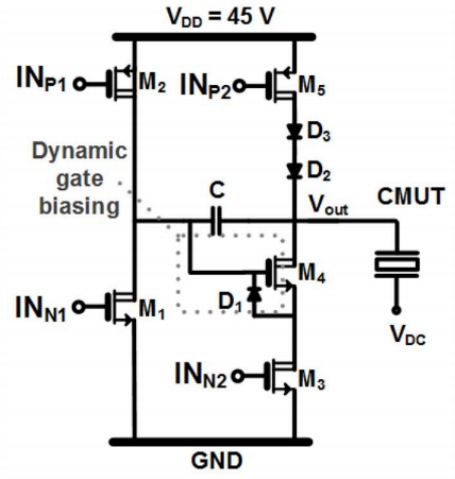


Figure 2.16: Supply-double 3-level pulser.

capacitor can be implemented together with the CMUT microfabrication. For example, if a high-K dielectric is utilized, this capacitor can be fabricated underneath the CMUT within the same area by replacing the vacuum gap. However, this method does not work for a bulk piezoelectric transducer.

C. Seven-level supply multiplying pulser

DC-DC converter for HV supply generation limits the overall power efficiency. This is the main reason why the real-circuit power efficiency achieved by subsection A of 2.2.1.2 mentioned above is always far away from theoretical calculation. A modular design approach for the step-wise 7-level supply multiplying pulser is presented in [34]. This design avoids the large self-loading issue and is able to reap a greater percentage power saving.

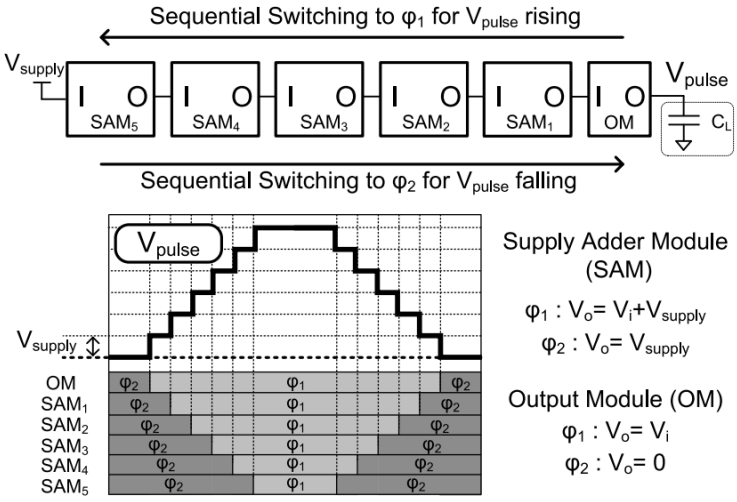


Figure 2.17: The 7-level supply multiplying pulser and operational concept.

As shown in Figure 2.17, the pulser is comprised of five Supply Adder Modules (SAMs) and an Output Module (OM) connected in series. During $\phi 1$, each SAM adds V_{supply} to its

input for the output and supplies V_{supply} to the output during $\phi 2$. The OM forwards the input to the output during $\phi 1$ and provides a ground voltage output during $\phi 2$. The rising edge of V_{pulse} is generated by sequentially switching OM and SAM1-5 in a forward order ($OM \rightarrow SAM1 \rightarrow \cdots \rightarrow SAM4 \rightarrow SAM5$) from $\phi 2$ to $\phi 1$. The falling edge is created by reversing this order.

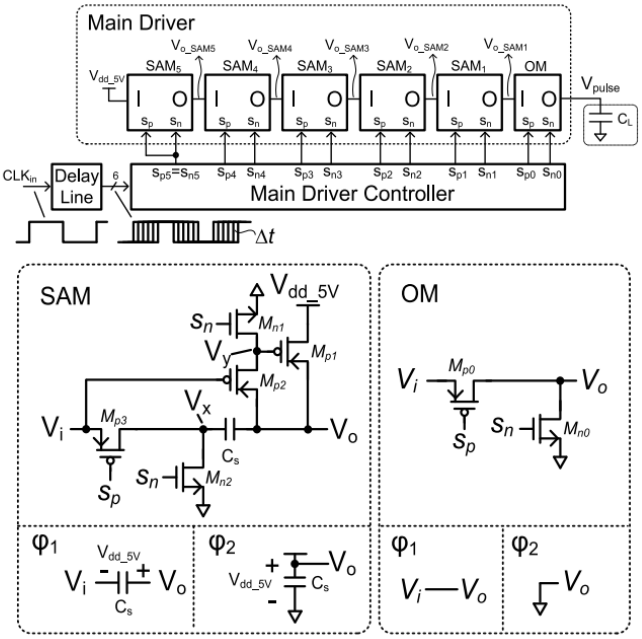


Figure 2.18: Circuit schematics of the modulars for the 7-level supply multiplying pulser.

In the proposed circuit shown in Figure 2.18, HV CMOS with a low $|V_{GS}|$ of 5V and a high $|V_{DS}|$ of up to 30V in BCD process was used. In the OM, when M_{n0} is on and M_{p0} is off, the ground is connected to V_o. Conversely, when M_{n0} is off and M_{p0} is on, V_i is connected to V_o. In the SAM, C_s is connected between V_i and V_o or between V_{dd5V} and the ground. During $\phi 2$, M_{p1} drives V_o to V_{dd5V}, charging Cs to 5V. During $\phi 1$, M_{p3} is turned on to connect V_x to V_i. Thus, V_o is driven to $V_i + V_{dd5V}$.

Although the operation of this pulser asks a really complicated controller, the effect of power reduction is significant. Measurement results show two prototypes with C_L of 55pF and 1nF being fabricated. In the case of the 55pF load prototype, an on-chip design incorporating 3nF MIM capacitors as storage capacitors was introduced. This design led to 58% reduction in power dissipation when compared to fCV^2. For the 1nF load prototype, a 60 nF external storage capacitor was utilized. This design achieved an impressive peak power reduction of 75.4% compared to fCV^2, marking one of the most significant power reductions reported thus far.

2.2.2. Level-shifter

To produce substantial square wave voltages from control signals, level-shifters are needed. A level-shifter can transform the low-voltage signals into high-voltage signals, which are used at high-path transistors' gates in output drivers and dc-dc converters.

Although the stacked standard CMOS output driver achieves lower area-occupation and cost, things get more complicated as to properly bias every transistor in the stack. In the

output drivers using stacked CMOS structure mentioned in D of 2.2.1.1, dynamic gate biasing technique is necessary to keep the voltage across each terminal of stacked transistors within the corresponding breakdown voltage.

This section focuses on how to make the gate voltages in a pulser be in proper ranges. 2.2.2.1 shows some different level-shifters that are published recently. 2.2.2.2 presents the commonly used dynamic gate biasing techniques.

2.2.2.1 Level-shifters

A. Conventional level-shifter

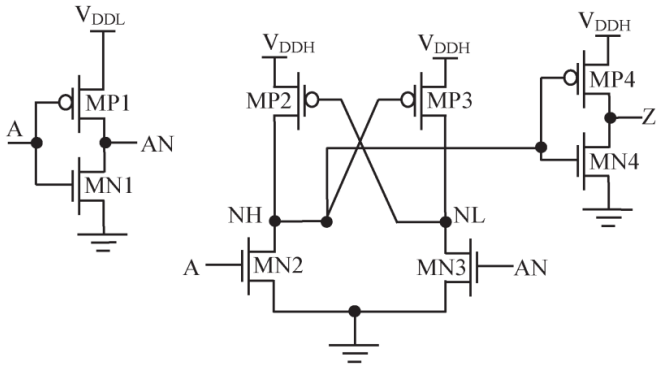


Figure 2.19: Conventional DCVS level converter.

A basic implementation of a differential cascade voltage switch (DCVS) level-shifter is shown in Figure 2.19 [35].

When the input signal A (AN) goes from low (high) to high (low), MN2 (MN3) is turned on (off), pulling down the voltage at node NH (NL) and leading MP3 (MP2) to be turned on. This occurs when NH (NL) voltage reaches $V_{DDH} - V_{th,MP3}$ ($V_{DDH} - V_{th,MP2}$). The node NL (NH) starts to be charged when MP3 (MP2) is turned on, weakening MP2 (MP3).

The conventional level-shifter has several drawbacks. It's necessary to make the NMOS transistors significantly larger to overpower the PMOS load. This is because the PMOS load is driven with a substantially higher gate-to-source voltage due to the high-voltage supply. However, larger size of the input NMOS pair results in a higher input capacitance, which, in turn, imposes limitations on the maximum operational speed while also increasing power dissipation. Moreover, the circuit experiences dynamic power dissipation due to the crow-bar current during transitions when both NMOS and PMOS transistors are in a conducting state. This phenomenon particularly prevails during operations at the typical MHz frequency used in medical ultrasound applications, contributing to the overall power dissipation.

B. Low-Power Level-Shifter

[35] proposed a novel low-power level-shifter as shown in Figure 2.20. This low-power design uses the 90nm-CMOS ST Microelectronics process technology, which enables designers to use low-voltage threshold (lvt), standard voltage threshold (svt), and high-voltage threshold (hvt) transistors.

In the main voltage conversion stage, MN2 and MN3 are designed by using lvt transistors to increase the strength of the pull-down network. Addressing concerns about the crow-bar current during the transition from high to low at nodes NH and NL, the design incorporates MP2 and MP3 as two lvt PMOS device to mitigate this effect. hvt transistors MP4 and MP5 are chosen for weakening the pull-up networks within the main voltage conversion stage, thus leading to a reduction in contention at nodes NH and NL, which is accompanied by a decrease in leakage current when the pull-up networks are turned off. The design integrates two diode-connected hvt PMOS MP6 and MP7 between the pull-up logic and the supply rail V_{DDH} to ensure a reliable voltage conversion. These devices moderate the pull-up strength while significantly reducing static power consumption.

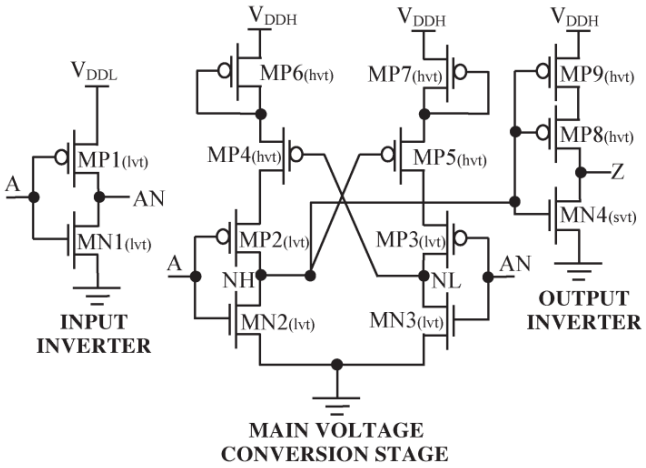


Figure 2.20: Low-power level-shifter [35].

C. Dynamic level-shifter

To solve drawbacks of conventional level-shifters mentioned in A, [36] proposed a dynamic level-shifter, which achieves high switching speed and low-power operation.

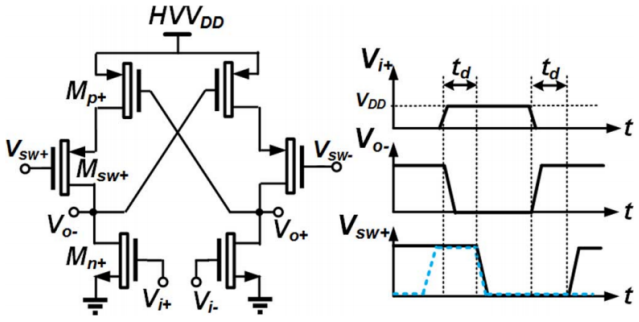


Figure 2.21: Level-shifter with crow-bar current suppression.

Figure 2.21 shows a level-shifter with crow-bar current suppression. Similar with design B in this section, it adds a pair of additional high-voltage devices in series with the latching transistors. Unlike the design in B, the additional PMOS transistors have different gate signals.

Take the switch M_{sw+} as an example, it should open before the low-to-high transition of Vi+ and close after the output has settled. This design removes the pull-up M_{p+} from the output during transitions, enabling a small NMOS pull-down M_{n+} to be used with low parasitic capacitance, which permits a high-speed operation. Moreover, when M_{sw+} is open, the crow-bar current is suppressed.

The complete architecture of the proposed dynamic level-shifter is shown in Figure 2.22. As the switch control signals are simply delayed and inverted version of the input signals, it could be generated by an identical level-shifter driven with a delayed input $V_{i,d}$, so that $V_{o+,d}$ and $V_{o-,d}$ provided by cell B is used to control switches M_{sw+} and M_{sw-} in cell A. Also, V_{o-} and V_{o+} from cell A can be used to control cell B switches.

When V_{o-} is high and M_{sw+} turns off to prepare for the next cycle, V_{o-} will be floating and eventually discharging. The recharge circuit is introduced to circumvent this. When $V_{recharge}$ goes high, the HV-PMOS is turned on to recharge V_{o-} back to HVV_{DD} and vice versa for V_{o+}.

This design successfully suppresses the crow-bar current while achieving high switching speed and low-power operation. However, two level-shifters and one recharge circuit make the whole circuit more complex. In addition, $V_{recharge}$ is generated off-chip with an FPGA, making the control of this level-shifter more complicated.

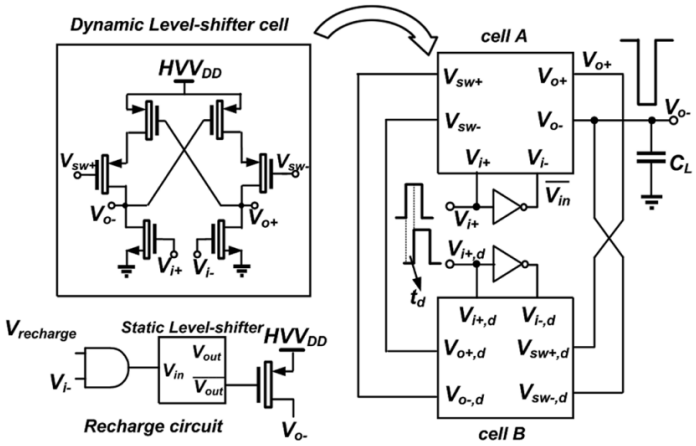


Figure 2.22: Complete architecture of the proposed dynamic level-shifter [36].

D. Stacked-CMOS level-shifter

The level-shifters for high-voltage pulsers mentioned above all use HV transistors. With low-cost consideration, it could also be designed in stacked CMOS structure.

The driver with stacked CMOS structure is introduced in [29]. Figure 2.23 further shows the level-shifter it uses for the HV output driver. This level-shifter can convert the 0-to-3.3 V swinging signal to a 11.7-to-15 V trigger signal. Like the output driver, similar stacking approach is used for the level-shifter, which enables standard 3.3-V transistors being reliable in the HV operation.

The output current driver introduced in [30] also uses a similar stack-structured level-shifter (Figure 2.24). This level-shifter performs the conversion of a 0-3.2 V digital control signal into a 9.6-12.8 V signal, which is then supplied to the PMOS stack input in the output driver. The output signal $\overline{\Phi_{anod/cath}}$ ensures maintaining gate-source voltage variations of all devices within the output current driver to a maximum of 3.2V.

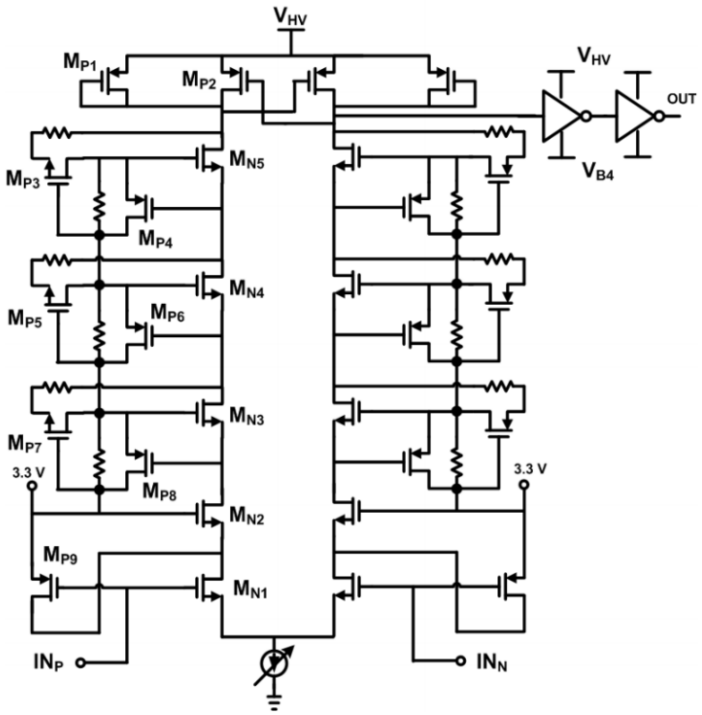


Figure 2.23: A level-shifter using stacked CMOS structure [29].

Similar with the output driver, the stack-structured level-shifters provides lower-cost and lower area-occupation option, while the safety operation of transistors has to be guaranteed by dynamic gate biasing techniques, making the design more complex than the simple level-shifters using HV devices.

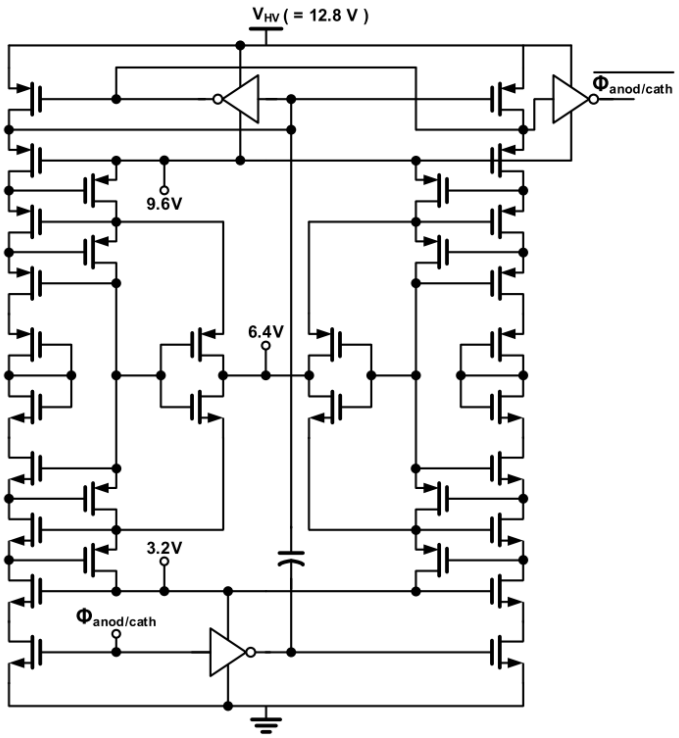


Figure 2.24: A level-shifter using stacked CMOS structure [30].

E. Zener-diode level-shifter

Level-shifters introduce extra time delays to signal paths during signal transitions. In applications with high frequencies, there's a demand for high-speed level-shifters, which can contribute to increased power consumption. To tackle these challenges, the level-shifters based on Zener diodes can be used [37].

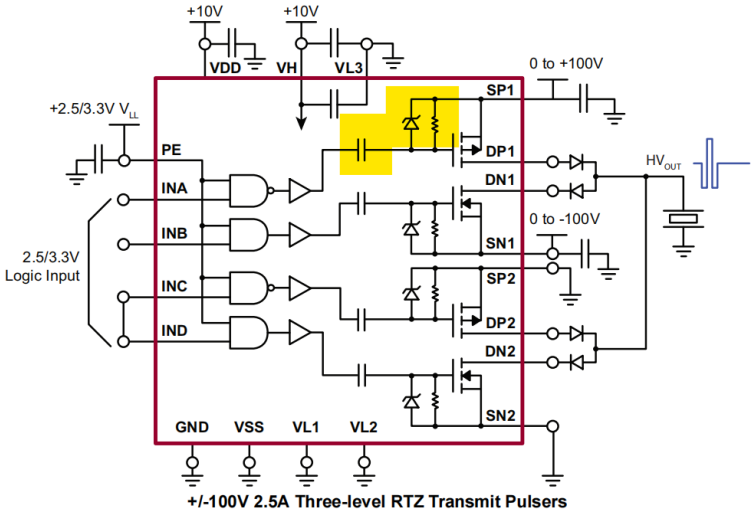


Figure 2.25: Zener-diode level-shifter (yellow part) [36].

Figure 2.25 shows a three-level pulser. The yellow part is a Zener-diode level-shifter. The reverse voltage characteristics of Zener diodes serve to safeguard the transistor gates from voltage surges, while a series-connected capacitor boosts the DC level. The function of the resistor is to limit the current charging speed and provide the steady-state bias operating point voltage for the PMOS. This method obviates the need for the previously mentioned floating ground and is characterized by low power consumption. However, it's important to note that not all IC fabrication processes support the incorporation of Zener diodes.

2.2.2.2 Dynamic gate biasing techniques

As mentioned before, in HV pulsers or level-shifters using stacked CMOS architectures, dynamic gate biasing circuit is necessary to correctly bias the gate of the stacked transistors during transitions and also limit the internal nodes within the allowable voltage range.

Figure 2.26 shows a HV output driver with its dynamic gate biasing circuit, which is marked within the red dashed box. As the stacked output driver has been introduced in 2.2.1.1, this part would give a brief operation analysis focusing on the dynamic gate biasing as follows.

When IN_N becomes logic "high" , this will turn on M_{N1}, M_{N2}, M_{P5}, M_{N3}. The voltage at the output node is discharged to $GND_{HV} + V_{DS\_MN1,2,3}$, where $V_{DS\_MN1,2,3}$ represents the voltage drop resulting from the dynamic current flowing through the output drain terminals, multiplied by the combined ON-resistance of M_{N1}, M_{N2}, and M_{N3}. In this case, both M_{P4} and M_{P6} remain OFF as their source–gate voltage is nearly equal.

When IN_N switches to logic "low" state, it turns off M_{N1} but turns on M_{P4}, subsequently biasing both the gate and source nodes of M_{N2} to V_{DD5}, which turns off M_{N2}. During the transition of the output node from "low" to "high," M_{P6} is turned on. The gate voltage of M_{N3} is determined by the resistive division of R_4, R_{ON_MP6}, and R_3 between the output node and

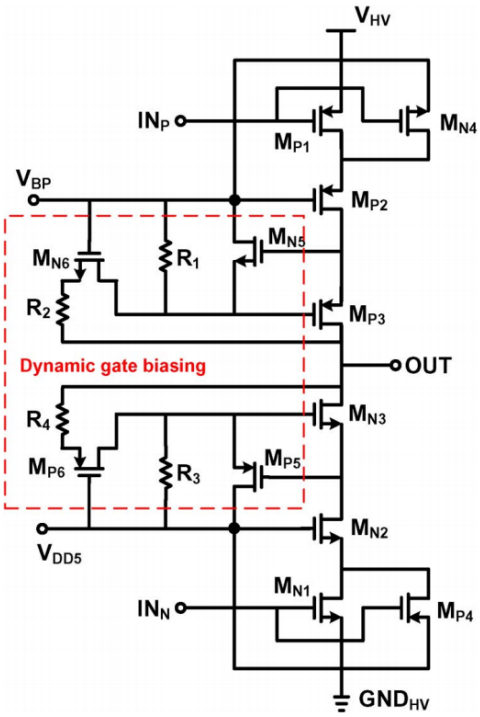


Figure 2.26: HV output driver with gate-biasing part proposed by [38].

V_{DD5}. Throughout the push-pull operation, the HV output voltage is distributed among the drain-to-source terminals of the stacked transistors.

This dynamic gate biasing circuit is similar with what [29] used for its stacked-structure level-shifter, which has been shown in Figure 2.23.

In the dynamic gate biasing circuit utilized in [30], which has been presented in Figure 2.13, when Φ_{anod} transitions from 0 to 3.2V, voltages at drain nodes of $M_{N1} \sim M_{N4}$ are all 0. The dynamic gate biasing circuit makes sure M_{BP1} and M_{BP2} are turned on, so that voltages at the gate of $M_{N1} \sim M_{N4}$ are all within 3.2V. On the PMOS side, $M_{P1} \sim M_{P4}$ distributes 12.8V at the output branch, making the source-drain voltage of these PMOS transistors within 3.2V. Meanwhile, M_{BN1} and M_{BN2} in the dynamic gate biasing circuit are turned off, sharing voltage of 6.4 V between the drain of M_{BN1} and the source of M_{BN2}, making the gate-source voltages of all the PMOS transistors within 3.2V.

Although the multi-level pulser proposed by [33] does not use stacked standard CMOS architecture, due to two stacked HV transistors, there's also a dynamic biasing design inside the pulser, which has been shown in Figure 2.16. During doubling mode, the gate of M_4 undergoes dynamic biasing to V_{DD}, whereas M_3 is turned off. To ensure that the gate-source voltage (V_{GS}) of M_4 remains below 5 V, a Zener diode labeled as D_1 is employed. This precaution allows M_3 and M_4 to proportionally divide the doubled output voltage without exceeding their specified drain-source voltage limits.

2.2.3. Discussion

The state-of-art designs mentioned above achieve different levels of power efficiency with different methods. Some of them have a really high power efficiency, such as the energy replenishing pulser in [8] and the 7-level supply multiplying pulser in [34]. However, both of these two designs suffer from a large-area occupation. Some of the designs have a milder power-

efficiency improvement with on-chip implementation such as [13] and the stacked CMOS designs. However, issues like narrow application and circuit complexity are inevitable. Table 2.2 lists all the designs reviewed in this section and provides a comparison for their pros and cons. In conclusion, the published designs could not be perfect in all aspects. One can never design a pulser with low power consumption, low area, high-voltage operation, simplicity and wild application at the same time. It's better to specify the application scenarios and strike a balance between different performance requirements. Inspiring from these works, to design a pulser that fits in a 2D pitch-matched architecture, a pulser with good power efficiency combined with feature of high-voltage operation and low area occupation is proposing.

Table 2.2: PROS AND CONS FOR THE REVIEWED DESIGNS

Designs	Pros	Cons
Conventional class-D pulser	Simplicity	High power consumption
Energy replenishing technique [12]	Very high power efficiency	Large-area occupation
Charge redistribution technique [13]	On-chip implementation and power efficiency	Narrow application scenario
Supply doubled bootstrapped pulser [28]	High-voltage operation	Complexity and having off-chip component
Stacked CMOS technique [29][30][31]	Lower power consumption, lower area occupation and lower process cost	Complexity in gate biasing
3-level pulse shaping technique [9]	Good power efficiency	Off-chip design
Supply doubled 3-level pulser [33]	Good power efficiency	Large area-occupation
7-level Modular Supply Multiplying Pulser [34]	Very high power efficiency	Large area-occupation and complexity

3

The proposed energy-efficient high-voltage pulser

3.1. The system-level design

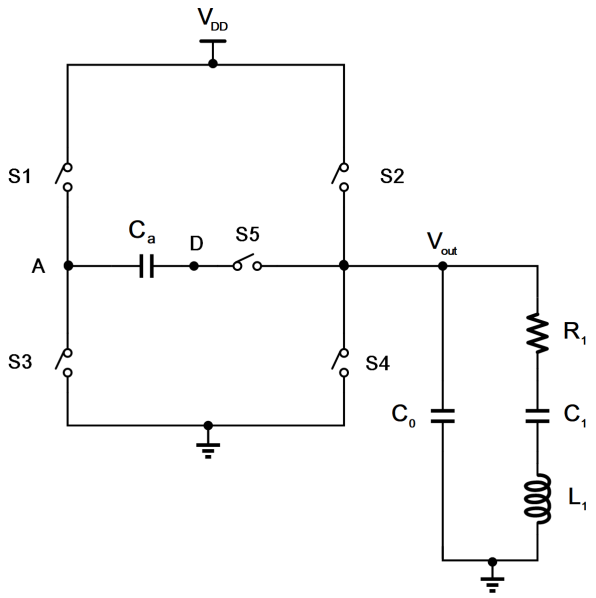
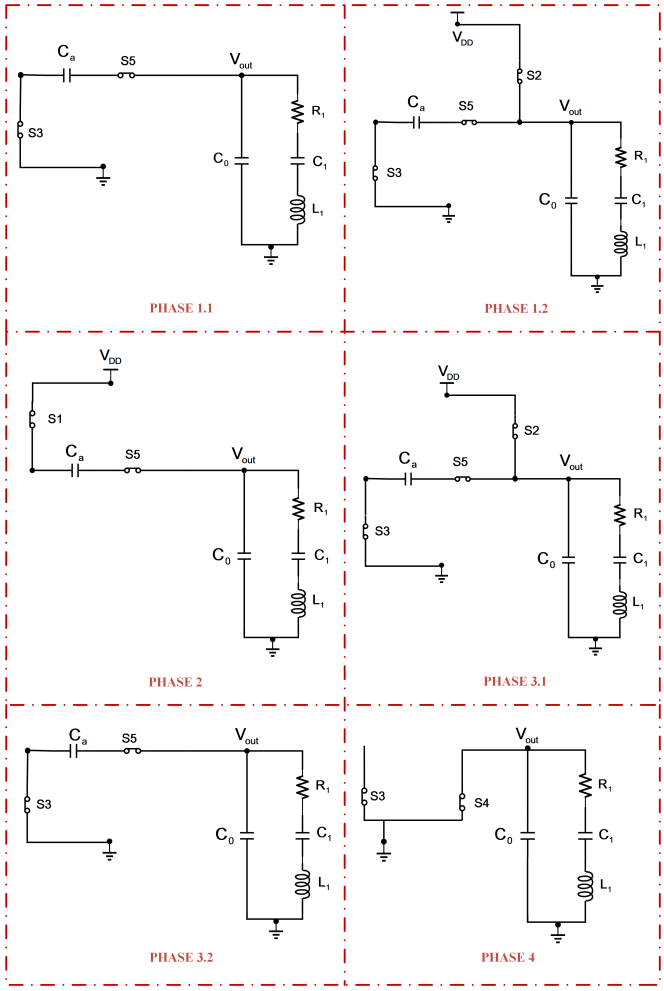


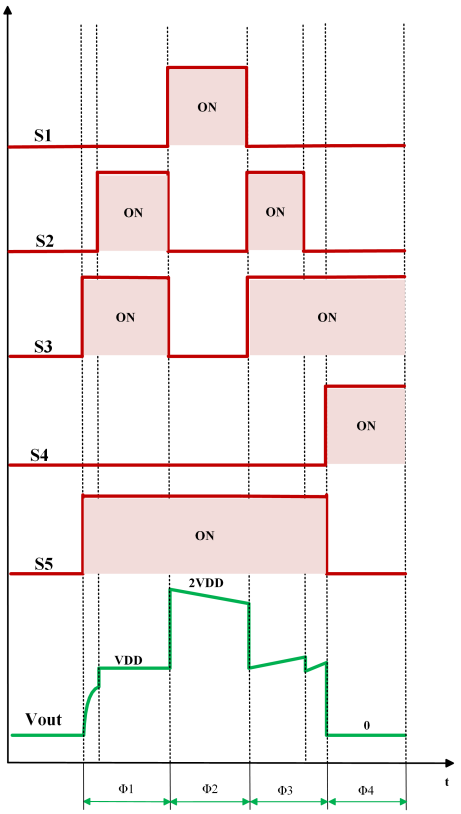
Figure 3.1: System-level schematic diagram of the proposed power-efficient HV pulser.

The system-level circuit diagram of the proposed 3-level high-voltage pulser is shown in Figure 3.1. C_0, R_1, C_1 and L_1 form the equivalent circuit for a PZT transducer. This transducer model is same as the BVD model introduced in Chapter 2. V_{DD} is a 10-V DC supply voltage. S1, S2, S3, S4 and S5 are switches that control the charging and discharging operation for the PZT transducer by regular opening and closing. C_a is a capacitor that is a part of a bootstrap circuit, aiming for boosting the output voltage to two times of V_{DD}.

The consideration for the system-level design is as follows. First of all, a capacitor is a superior choice compared with an inductor, taking the area limitation into account in the context of this project. Then, for the switch implementation, the stacked standard CMOS structure is the first choice, since it has low power consumption and low area occupation. However, to



(a) 4 phases of a pulse period in the circuit. Both phase 1 and phase 3 have 2 sub-phases.



(b) States of S1 to S5 and the corresponding output wave.

Figure 3.2: Operation process of this 3-level pulser.

make sure that the gate biasing part is as simple as possible, a comparatively lower supply voltage-level should be chosen. On the other hand, a high-voltage operation should be guaranteed. Thus, a 10-V supply voltage is selected, and for the output voltage, a bootstrap structure is utilized to double the supply voltage. The 3-level design is under the consideration for the acoustic operation feature of the PZT transducer. As the transmitted pulse should be at the frequency where the transducer resonates, the pulser should generate pulses that concentrate within an effective bandwidth. Actually, the more sinusoidal the pulse waveform is, the more effective conversion of the electrical energy into the acoustic energy. This indicates the superiority of the multi-level pulse compared with the conventional square-wave pulse, since it looks like a sine wave and has less harmonics in the frequency spectrum. Ideally, with the help of the bootstrap structure, the three levels of the output voltage are 0, 10 V and 20 V. In this case, the dynamic power CV^2f is effectively reduced, because the supply voltage could be lower than that in the conventional design.

A whole pulse period has 4 phases, each of which equally occupies 1/4 of one period. Operation process of this 3-level pulser is shown at Figure 3.2. The circuit diagrams on the left present the four phases of the operation of a pulse period. The timing diagram on the

right shows the on and off states of S1 to S5 in red lines, and the corresponding output voltage waveform in green line.

In the charging phase Φ_1, switches S2, S3 and S5 are closed while S1 and S4 are opened. The 10-V supply charges both the transducer and C_a, keeping the output voltage at V_{DD}.

In the second phase, which is the voltage-doubling phase Φ_2, S2 and S3 are opened and S1 and S5 is closed. As C_a was charged to have a voltage potential of V_{DD} during Φ_1, the right electrode of C_a is pushed to $2 \times V_{DD}$ by connecting its left electrode from ground to V_{DD}. However, the voltage at the output node is not fixed to $2 \times V_{DD}$, instead, it has a slight descending slope. This is because without constant voltage supply, charges on capacitors have a trend of flowing to the ground rapidly through the resistor in the PZT equivalent circuit model.

Then phase Φ_3 starts. Similar with Φ_1, S2, S3 and S5 are closed while S1 and S4 are opened to keep the output at a comparative stable level of V_{DD}. A slightly rising slope shows up in the output wave. This is because during Φ_2, charge accumulated on C_0 was $2V_{DD}C_0$. At the moment when V_{out} turns to V_{DD} with the connection to the supply, the additional charges on C_0 are pushed to the branch consisting of R_1, C_1 and L_1, and the working mechanism of the inductor L_1 leads to a rising trend in V_{out}. When this phase reaches near 2/3 of it, S2 opens. This move functions for reducing the power consumption. For one thing, opening S2 for a while effectively reduces the running time of S2, which, in the transistor-level circuit is achieved by PMOS with a comparatively large width. Reducing running time of these PMOS can reduce the energy consumed on them. Moreover, the opening S2 leads to charges on C_a and C_0 running fast through R_1 to the ground, reducing the voltage level at the output node. This abrupt voltage drop compensates the previous rising trend of V_{out}, so that the value of V_{out} at the end of phase 3 would not be overlarge. In this sense, the dynamic power loss of C0 is reduces in the fourth phase..

The discharging move happens in Φ_4, when S3 and S4 are closed and the other switches are opened. In this phase, charges accumulated on the transducer flow to the ground as the upper electrode of the transducer is connected to the ground. S3 in this phase is closed to keep the left electrode connecting to the ground. This is because the left side of C_a comes to a tiny minus voltage level when Φ_4 starts. Connecting to ground helps keep the left electrode being at 0, guaranteeing the gate-drain voltage of transistors in S1 being within the break-down voltage limitation. S5 in this phase is opened, making the right side of C_a floating, such that charges accumulated on C_a still remains on it. In the next charging phase, the supply does not need to charge C_a from 0, avoiding wasting charges on C_a.

At the beginning of next Φ_1, instead of directly closing S2, S3 and S5, only S3 and S5 are closed first for a short time. This move enables C_a to charge C_0 to a specific level. If all the switches are ideal, this does not improve the power-efficiency, since both C_a and C_0 will be charged to VDD in the end of this phase. However, as mentioned before, S2 is achieved by large PMOS transistors. Charge sharing between C_a and C_0 allows reducing the operation time of S2, resulting in reducing the switching losses over S2 and improving the overall power efficiency.

3.2. Circuit implementation

Figure 3.3 shows the whole output driver circuit without the level-shifters included.

There are stacks of PMOS or NMOS transistors to form the 5 switches, which correspond to S1, S2, S3, S4 and S5 in Figure 3.2. The 5 signals, which, are named as Sig1 to Sig5, are

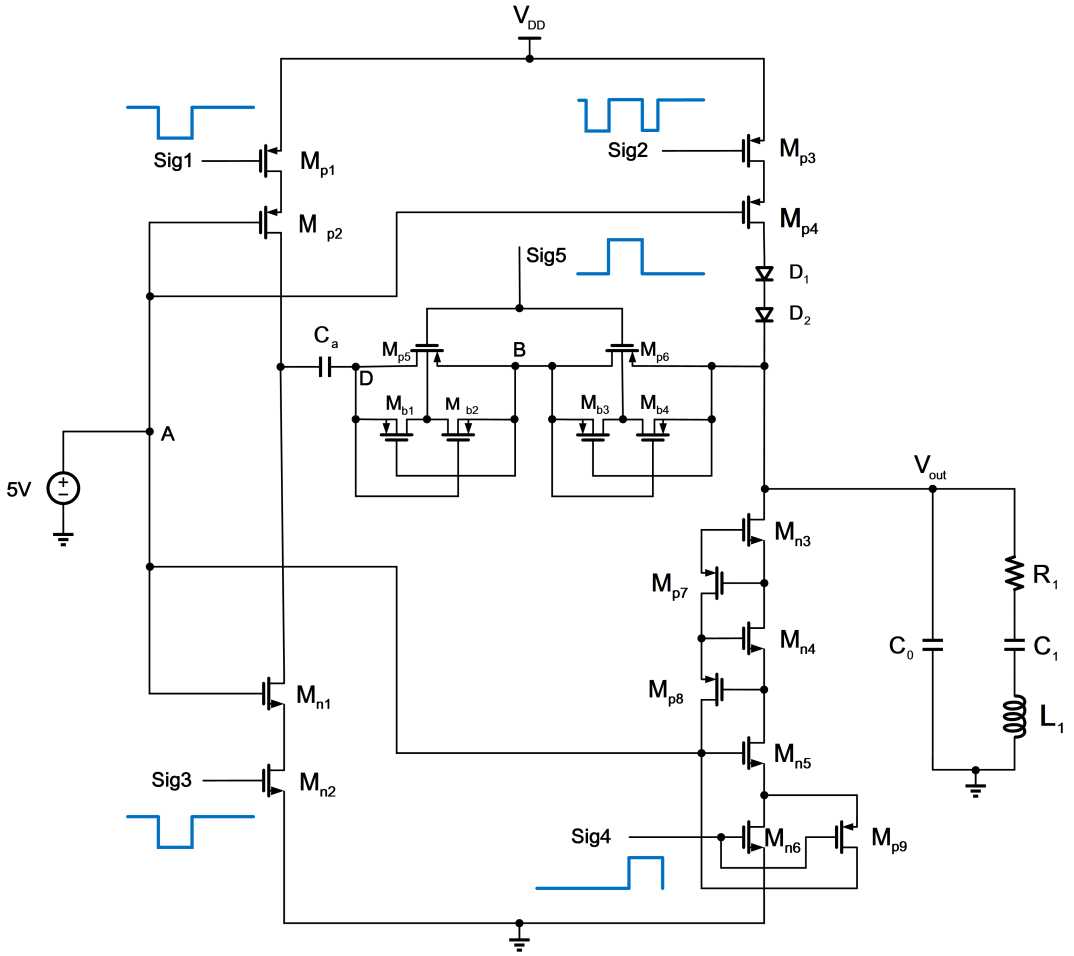


Figure 3.3: The output driver implementation.

connected to gates of the PMOS and NMOS transistors. It is worth mentioning that Sig5 in this design is the inverse of Sig1 and Sig1 is the level-shifted Sig3, indicating that there are 3 control signals in total are needed in this design.

The supply voltage V_{DD} is 10 V, meaning that in this design a 3-level output voltage wave including 0, 10 V and 20 V is expected. In real circuit, the output voltage levels are not exact 0, 10 V and 20 V since the switches are not ideal. To be specific, during Φ_1, the output voltage is $V_{DD} - (V_{DSp3} + V_{DSp4} + V_{D1} + V_{D2})$. The output voltage level could be higher by increasing the width of M_{p3} and M_{p4}, for the on-resistance of CMOS could be expressed inversely proportional to the width of the device, so that the voltage drop on M_{p3} and M_{p4} could be smaller. However, larger PMOS causes larger power and area consumption, this is one of the reasons why during the designing process there's always a trade-off between the output level and power consumption. In Φ_2, the output voltage goes to $2V_{DD} - (V_{DSp1} + V_{DSp2} + V_{DSp3} + V_{DSp4} + V_{DSp5} + V_{DSp6} + V_{D1} + V_{D2})$. The output during Φ_3 is similar with that in Φ_1. During Φ_4, the output voltage is determined by the discharging speed of the RLC circuit consisted by the transducer and the stacked S4. Due to the consideration for the need of power-efficiency, widths of the 4 stacked NMOS could not be too large, so that the output-level at Φ_4 is not exact 0 but slightly higher than 0.

For the following section, every single part within the circuit would be introduced by further elaborating the thought of design.

3.2.1. PZT transducer model

Since measuring the impedance of a PZT transducer was out of the scope of this project, we have adopted an equivalent circuit from a circuit model of a 250 $\mu m\times$ 250 μm PZT transducer with a thickness of 267 μm which is provided in [39]. In this work, we have utilized a 100 $\mu m\times$ 100 μm PZT with the thickness of 267 μm, corresponding to a pitch-matched 8.15 MHz 2D PZT phased-array transducer.

In an electrical model of a PZT transducer element with the same resonant frequency, the capacitance scales proportional to the area, while the resistance and inductance are inversely proportional to the area. In the 250 $\mu m\times$ 250 μm model, $C_{0,250}$=2.70 pF, $R_{1,250}$=1.13 kΩ, $C_{1,250}$=0.72 pF, $L_{1,250}$= 0.53 mH. The scaling calculation is shown below:

$$\begin{aligned} C_0 &= \frac{100\mu m \times 100\mu m}{250\mu m \times 250\mu m} \times 2.70pF = 432fF \\ C_1 &= \frac{100\mu m \times 100\mu m}{250\mu m \times 250\mu m} \times 0.72pF = 115.2fF \\ R_1 &= \frac{250\mu m \times 250\mu m}{100\mu m \times 100\mu m} \times 1.13k\Omega = 7.06k\Omega \\ L_1 &= \frac{250\mu m \times 250\mu m}{100\mu m \times 100\mu m} \times 0.53mH = 3.31mH \end{aligned} \tag{3.1}$$

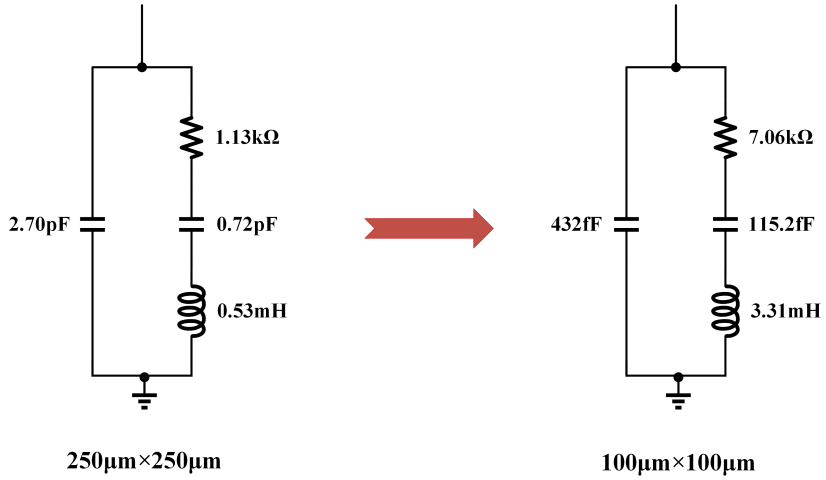


Figure 3.4: Scaling the $100\mu m \times 100\mu m$ PZT transducer element from a $250\mu m \times 250\mu m$ model.

3.2.2. Stacked CMOS transistors

The switches in the proposed circuit utilize stacked CMOS in $0.18\mu m$ BCD process. In conventional class-D pulsers, high-voltage (HV) transistors are usually used. The proposed design uses standard CMOS as an alternative based on some reasonable considerations. For examples, HV transistors usually require specialized process technologies, leading to more cost for the chip manufacturing, while standard processes wouldn't cost too much. Another advantage of the stacked standard CMOS is that stacking allows for a more compact design. As the area of the TX circuit in a 2D phased array is limited to half of the sound wavelength in order to avoid appearance of grating lobes in the beam profile, the area occupation of the IC is a crucial

parameter. The stacking structure can reduce the chip area required for the same functionality achieving by HV technologies.

A. Stacked S1

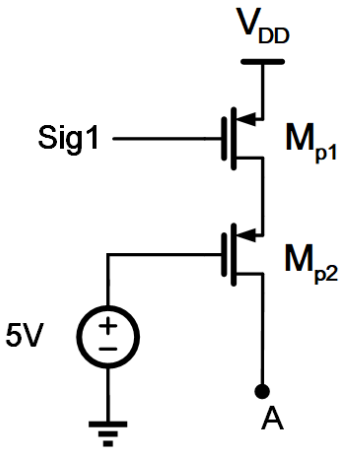


Figure 3.5: The stacked S1.

Figure 3.5 shows the stacked PMOS transistors M_{p1} and M_{p2}, taking an example to further explore the design idea behind. M_{p1} and M_{p2} are chosen with standard 5 V PMOS transistors. The voltage at node A changes between 0 and 10 V, so using two 5-V transistor stacked together is enough to guarantee the drain-source voltages of the PMOS transistors are within the safe range.

The gate of M_{p1} is connected to Sig1, which is a control signal ranges from 5 V to 10 V, coming from the output of a level-shifer with a 0 to 5 V input signal. A 5-V DC voltage source is directly connected to the gate of M_{p2}. When Sig1 is 5 V, the gate-source voltage of M_{p1} reaches 5 V, enabling M_{p1} to be turned on, making voltage at the source node of M_{p2} reach to 10 V, turning M_{p2} on. When Sig1 changes to 10 V, M_{p1} is turned off as its V_{GS} is 0 now. M_{p2} is thus turned off and the two transistors could equally divide the near-10V voltage difference. The theoretical principle is as follows.

When V_{GS} goes below the threshold voltage (V_{TH}), these two transistors get into the "sub-threshold" mode with conducting a very small leakage current. This current is calculated as:

$$I_D = \frac{W}{L} I_0 exp(\frac{V_{GS} - V_{TH}}{\eta V_T}) \times (1 - exp(-\frac{V_{DS}}{V_T})), \tag{3.2}$$

where

$$I_0 = \mu C_{ox}(\eta - 1) \times {V_T}^2. \tag{3.3}$$

Here M_{p1} and M_{p2} are set in the same width and length. If both the gate of M_{p1} and M_{p2} are connected to Sig1, what happens is that $V_{GS2} < V_{GS1}$. To make sure the current I_{D1} equals to I_{D2}, V_{DS2} would be much larger than V_{DS1}, reaching out the break-down limitation of the 5 V PMOS transistor. By connecting the gate of M_{p2} to a constant 5 V voltage source, V_{GS2} increases, such that V_{DS2} could be very near V_{DS1}. The same thing happens on the stacking S1 and S3, explaining the reason why the gate of M_{p4} and M_{n1} are connected to a 5 V DC voltage source. If the voltage-exceeding problem still happens, proper sizing for the transistors can

guarantee the drain-source and gate-source voltages never exceed the limitation 5.5 V. It is worth mentioning that all the bulks of these transistors are connected to their own source, so that the gate-bulk voltages of M_{p2}, M_{p4}, and M_{n1} would not run out of the safety range and the V_{TH} of each transistors in the stacked couple could be approximately the same.

B. Stacked S2

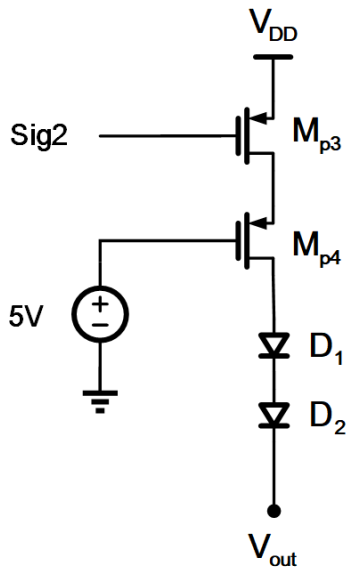


Figure 3.6: The stacked S2.

Figure 3.6 shows the stacked PMOS transistors M_{p3} and M_{p4}. M_{p3} and M_{p4} are also chosen with standard 5 V PMOS transistors. As the output voltage changes from 0 to near $2V_{DD}$, using two 5-V transistor stacked together is enough to guarantee the drain-source voltages of the PMOS transistors are within the safe range.

The gate of M_{p3} is connected to Sig2, which is a control signal ranges from 5 V to 10 V, coming from the output of one of the level-shifers with a 0 to 5 V input signal. A 5-V DC voltage source is directly connected to the gate of M_{p4}, as explained above. When Sig2 comes to 5 V, the gate-source voltage of M_{p3} reaches 5 V, enabling M_{p3} to be turned on, making voltage at the source node of M_{p4} reach to 10 V, turning M_{p4} on. When Sig2 becomes 10 V, M_{p3} is turned off as its V_{GS} is 0 now. M_{p4} is thus turned off. The two transistors could equally divide the voltage difference when $|V_{DD} - V_{out}|$ reaches near 10 V.

D_1 and D_2 are 5-V Schottky diodes, and they are added in series with M_{p3} and M_{p4}. Connecting D_1 and D_2 together can prevent against a 10 V of reverse voltage during the doubling phase, ensuring the gate-drain voltage of M_{p4} to be within the limitation.

C. Stacked S3

Figure 3.7 shows the stacked NMOS transistors M_{n1} and M_{n2}. M_{n1} and M_{n2} are chosen with standard 5 V PMOS transistors. As the voltage at node A changes from 0 to 10 V, using two 5-V transistor stacked together is enough to guarantee the drain-source and gate-source voltages of theses transistors are within the safe range.

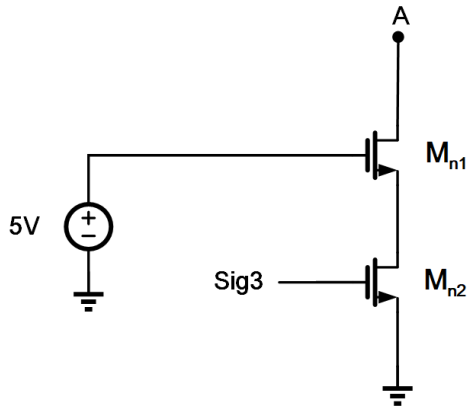


Figure 3.7: The stacked S3.

The gate of M_{n2} is connected to Sig3, which is a control signal ranges from 0 V to 5 V. A 5-V DC voltage source is directly connected to the gate of M_{n1}, as explained above. When Sig3 comes to 5 V, the gate-source voltage of M_{n2} reaches 5 V, enabling M_{n2} to be turned on, shorting the source node of M_{n1} to the ground, turning M_{n1} on. When Sig3 changes to 0, M_{n2} is turned off as its V_{GS} is 0 now. M_{n1} is thus turned off. The two transistors could equally divide the voltage difference that is near 10 V.

D. Stacked S4

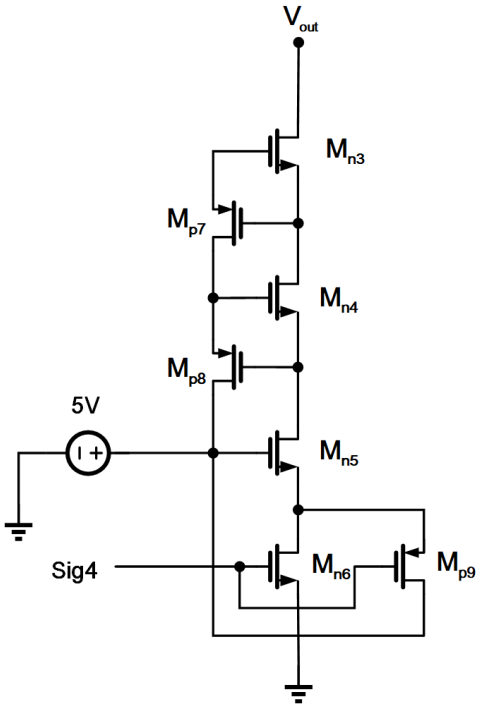


Figure 3.8: The stacked S4.

The output voltage during the doubling phase is around 15 V, putting forward requirements on the design of S4, which is shown in Figure 3.8. In this design, four 5-V standard NMOS are

stacked to share the large voltage. Another three PMOS are employed to form a gate biasing part. The gate biasing circuit ensures that the voltage differences between the terminals of the stacked transistors remain within 5.5 V. The working principle of this stacked structure is as follows.

When the pulser needs S4 to be closed at the forth phase to discharge the transducer, a 0 to 5 V signal Sig4 presents at the gate of M_{n6}. M_{n6} is turned on and M_{p9} is turned off, subsequently turning on M_{n5}, as the gate of M_{n5} is always connected to a constant 5-V voltage source. The drain of M_{n5} is discharged, turning on M_{p8} and shorting the gate of M_{n4} to the 5-V voltage source. M_{n4} is thus turned on. The similar process applies to M_{p7} and M_{n3}. So the NMOS stack is fully turned on.

During the doubling phase, the control signal Sig4 is 0, so that M_{n6} is turned off and M_{p9} is turned on. The source node of M_{n5} is charged to 5 V. M_{n3}, M_{n4}, M_{n5} divide the voltage of around 10 V. During this phase, the gate of Mn3 and Mn4 is floating. The parasitic capacitors of C_{gd} of M_{n3} and C_{ds} of M_{p7} form a capacitive voltage divider and set the gate of M_{n3} to a portion of the output node. Proper sizing of the transistors guarantees that the V_{DS} and V_{GS} of the transistors in the switch never exceed 5.5 V.

E. Stacked S5

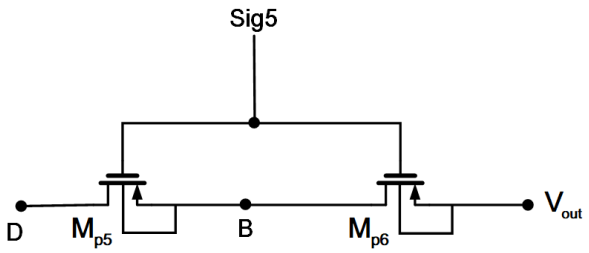


Figure 3.9: The stacked S5.

Figure 3.9 shows stacked PMOS transistors M_{p5} and M_{p6}, which are chosen with standard 5 V PMOS transistors. As the voltage difference between node D and the output node never exceeds 10 V, using two 5-V transistor stacked together is enough to guarantee the drain-source and gate-source voltages of theses transistors are within the safe range.

The gates of both M_{p5} and M_{p6} are connected to a control signal Sig5, which is the inverse signal of S1. In the first phase, Sig5 are 5 V and the output voltage is near V_{DD}, so that M_{p5} and M_{p6} are turned on. In the second phase, Sig5 changes to 10 V when the output voltage is boosted to around 15 V, making sure that both of them are on. Situation in the third phase is similar with the first phase. In the fourth phase, the output node is discharged to 0 and Sig5 keeps at 5 V, enabling M_{p5} and M_{p6} to be turned off.

Latch-up problem is a short circuit problem in CMOS. It is a condition where a low-impedance path is created between the power supply rails, leading to a high current flow that can cause overheating and destruction of IC. The latch-up problem also exists in the structure of M_{p5} in series with M_{p6}. As shown in Figure 3.9, during the third phase, M_{p5} and M_{p6} are turned on and V_{out} is near V_{DD}, so that the potential at the middle point of two transistors B should be near V_{DD}. As the circuit goes into phase 4, the right terminal and the body of M_{p6}

discharged to 0. However, as there's a potential at node B, which is the p-type terminal of M_{p5} and M_{p6}, a diode will form, breaking the device.

The essential of the problem above is that source nodes of these PMOS are not fixed. For PMOS, the higher voltage determines the source. Due to this pulser's operation mechanism, both the left and right terminals could be the voltage-higher one, meaning that the body of the PMOS is not always connect to the source of the PMOS. To solve this problem, a self body biasing circuit could be utilized.

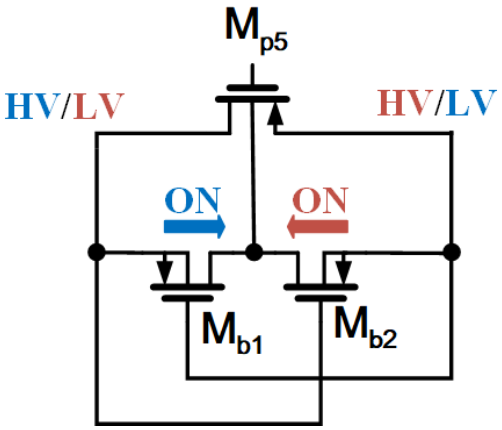


Figure 3.10: The self body biasing circuit.

As shown in Figure 3.10, two additional PMOS transistors are connected in series between the source and drain of M_{p5}. When the left terminal of M_{p5} is a higher voltage, M_{b1} is turned on while M_{b2} is turned off. The body of M_{p5} is thus connected to the left terminal. When the right side of M_{p5} is a higher voltage, the body of M_{p5} is connected to the right terminal. The self body biasing circuit guarantees the body of the main transistor is always connected to the higher-voltage terminal, which is the source, such that the latch-up problem mentioned above is perfectly solved. The complete implementation of S5 is presented in Figure 3.11.

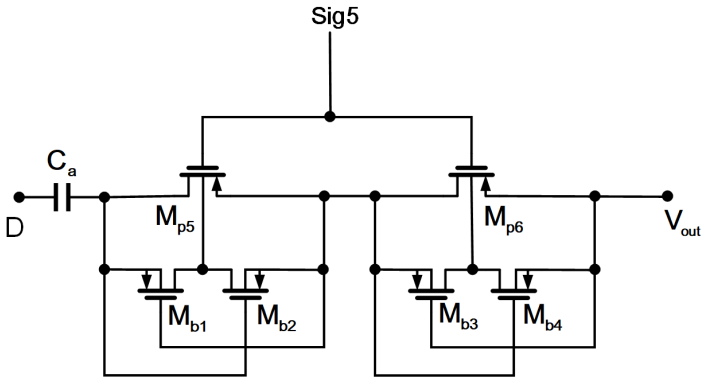


Figure 3.11: The complete implementation of S5.

3.2.3. Level shifter

The control signals Sig3 and Sig4 change between 0 and 5 V, while Sig1, Sig2 and Sig5 change between 5 V and 10 V, making it necessary to have level shifters for properly biasing the high side transistors. The level shifter used in this design is presented in Figure 3.12.

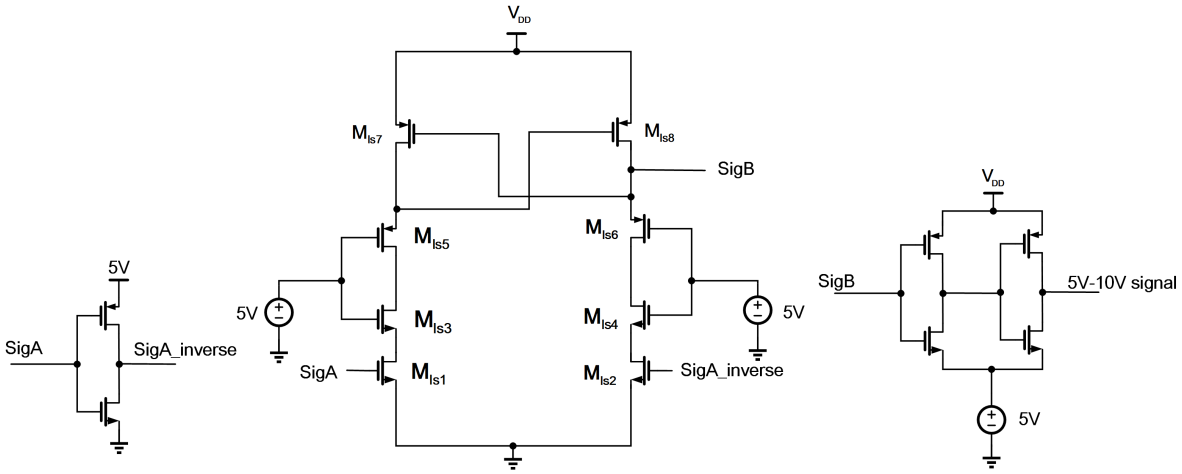


Figure 3.12: The level shifter used in the proposed design.

The level shifter in Figure 3.12 also utilizes the stacked standard 5 V CMOS. When the control signal SigA goes from low (0) to high (5 V), NMOS M_{ls1} is turned on and M_{ls2} is turned off, pulling down the source node of M_{ls3} and the drain of M_{ls5}. At this moment, PMOS M_{ls5} and M_{ls7} equally divide V_{DD}, triggering M_{ls8} by making its gate voltage near 5 V. M_{ls8} is turned on and the output signal SigB becomes $V_{DD} - V_{DS8}$. M_{ls6} is also turned on, so that M_{ls4} and M_{ls2} divide a voltage of $V_{DD} - V_{DS8} - V_{DS6}$. When the control signal SigA goes from high (5 V) to low (0), M_{ls2} and M_{ls4} are turned on, discharging the node between M_{ls4} and M_{ls6} to 0. As M_{ls6} and M_{ls8} are at the cut-off mode, M_{ls6} and M_{ls8} equally divide V_{DD}, tuning on M_{ls7} by making its gate voltage near 5 V. The output signal SigB at this moment becomes $\frac{1}{2}(V_{DD} + V_{DS2} + V_{DS4})$. M_{ls1} and M_{ls3} in this case divide a voltage of $V_{DD} - V_{DS5} - V_{DS7}$.

There's always a buffer, which consist of 2 pairs of inverters, following the main level-shifter. This is because the output signals of the level-shifter are not exact 5 V and 10 V due to the influence of the drain-source voltage of the transistors in the level-shifter. The simulation result shows that the level-shifter's output signal changes between 5.55 V and 10 V. The buffer can restore the signal to its proper logical levels, avoiding it becomes too deviated for the following circuit.

3.2.4. The conventional class-D pulser

The conventional class-D pulser is used to do a comparison with the proposed design. However, there is not a fixed conventional class-D pulser to be referred, as it still could have different level-shifters. To make the comparison as fair as possible, we still need to explore the most power-efficient version of conventional class-D pulser to be compared.

Figure 3.13 shows the conventional class-D pulser used in this project as a reference for the power performance. M_p and M_n are both HV transistors, with the V_{GS} limitation of 5 V and the V_{DS} limitation of 20 V. Signal 2 is the control signal ranges from 0 to 5 V. To make a proper 10 V to 15 V control signal, Signal 1, a power efficient level shifter is employed as discussed in Chapter 2.

The reverse voltage characteristics of Zener diodes keep the gate of the HV-PMOS transistor within the safe range, while a high-pass RC filter boosts the voltage level. The function of the resistor is to limit the current charging speed and provide the steady-state bias operating point voltage for the PMOS. This method obviates the need for the floating ground and is

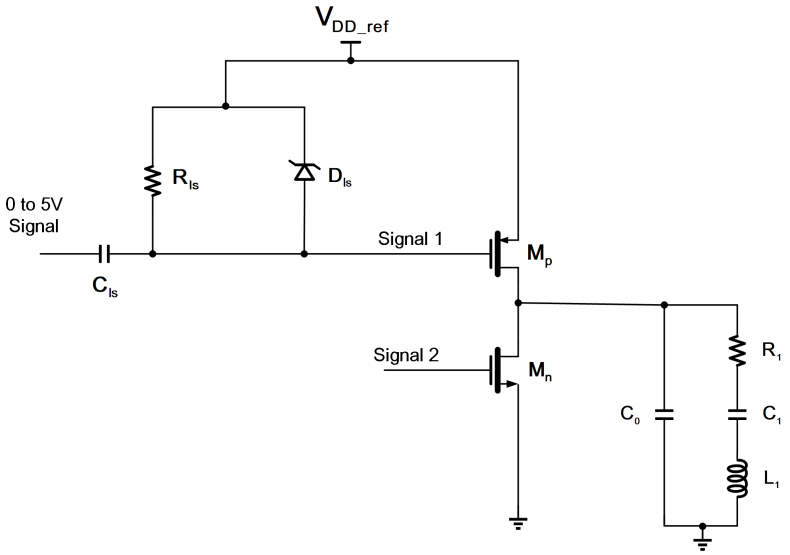


Figure 3.13: The conventional class-D pulser to as the comparison.

characterized by low power consumption. In order to fairly compare the conventional class-D pulser with the proposed one, the conventional pulser is also optimized for the power efficiency. In this regard, a dead time between Signal 1 and Signal 2 is applied to prevent the dynamic transition losses.

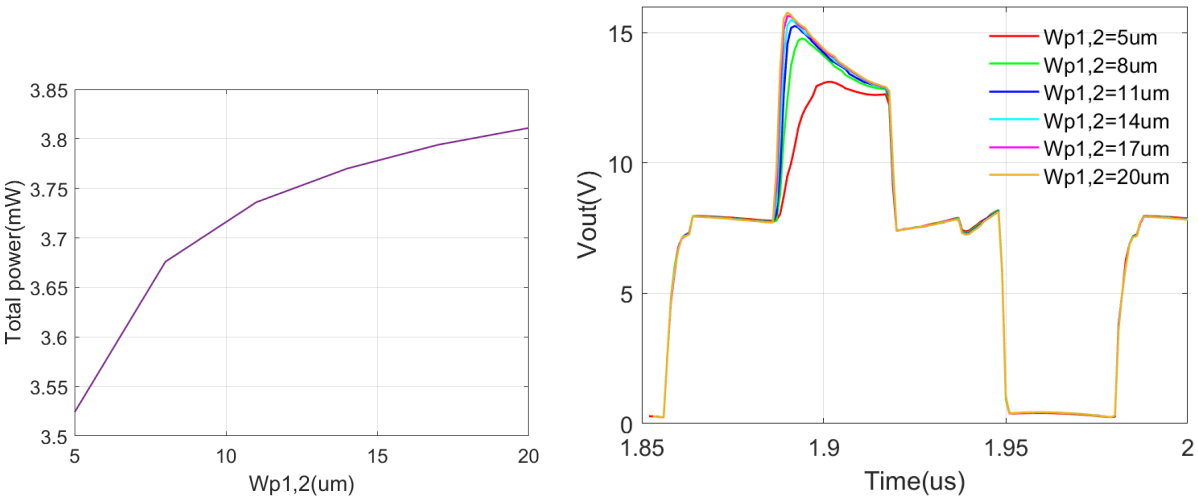
4

Simulation results and discussion

4.1. Sizing of the proposed circuit

4.1.1. Sizing of the HV driver

As mentioned in Chapter 3, there's always a trade-off between the sizes of the devices and the output voltage level, and, of course, the power efficiency. One can not enable the pulser to have both highest output voltage level and a minimum power consumption. Thus, determining sizes of every transistor and the capacitor is a crucial step in the design. To make the most balanced choice of the device sizes, Parametric Analysis is used to sweep different choices for the devices with the output waveform and the total power consumption.



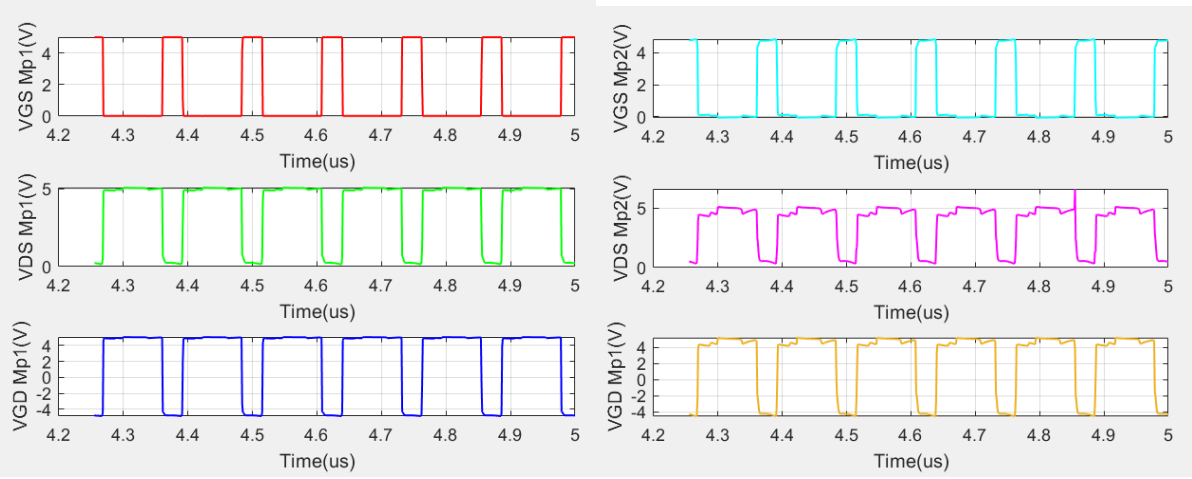
(a) Total power v.s. width of M_{p1} and M_{p2}.

(b) Output wave v.s. width of M_{p1} and M_{p2}.

Figure 4.1: Different width of M_{p1} and M_{p2} with different power consumption and V_{out}.

A. Sizing of switch S1 Figure 4.1 shows the total power and output wave with different width of M_{p1} and M_{p2}, which were noted in Figure 3.3. The larger the widths of M_{p1} and M_{p2} are, the larger total power the pulser consumes. The widths of M_{p1} and M_{p2} relate to the maximum value of V_{out}, the larger width of M_{p1} and M_{p2} enable a larger output voltage level during the doubling phase Φ_2. To get a larger output voltage level as well as a comparatively lower power consumption, $W_{p1,2}$ which presents the width of M_{p1} and M_{p2} is chosen as 12 μm. However,

the simulation result shows the drain-source voltage V_{DS} of M_{p1} has the danger of exceeding the limitation. Thus, according to the Equation (3.2), the width chosen for M_{p1} should be larger than M_{p2}. Thus, the width of M_{p1} is chosen as 16 μm while 8 μm is chosen for M_{p2}.

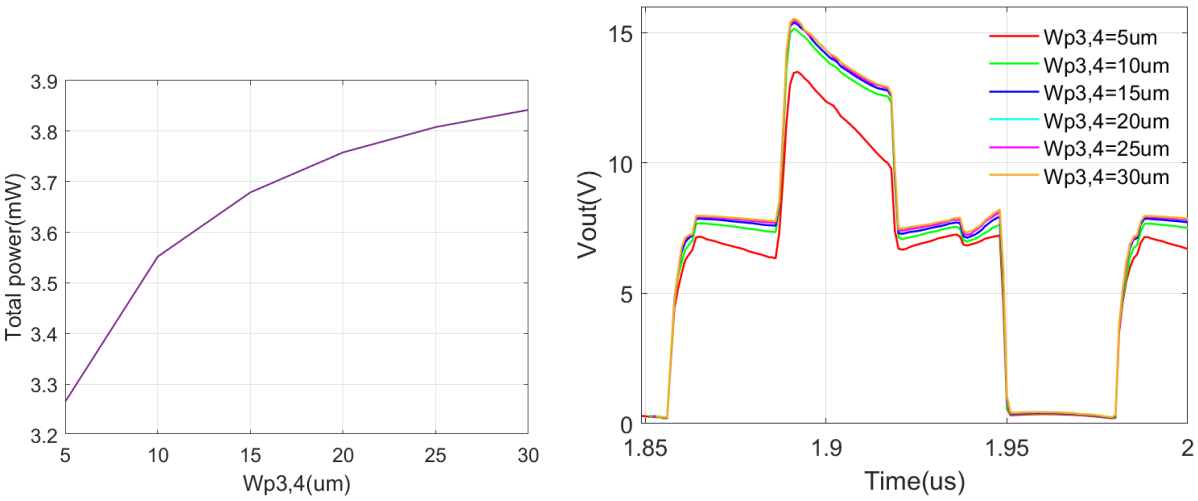


(a) V_{GS}, V_{DS}, and V_{GD} of M_{p1}.

(b) V_{GS}, V_{DS}, and V_{GD} of M_{p2}.

Figure 4.2: Voltages between terminals of M_{p1} and M_{p2}.

Simulation results for V_{GS}, V_{DS}, and V_{GD} of M_{p1} and M_{p2} are shown in Figure 4.2. The figures shows that terminal voltages of M_{p1} and M_{p2} are in the safe region.



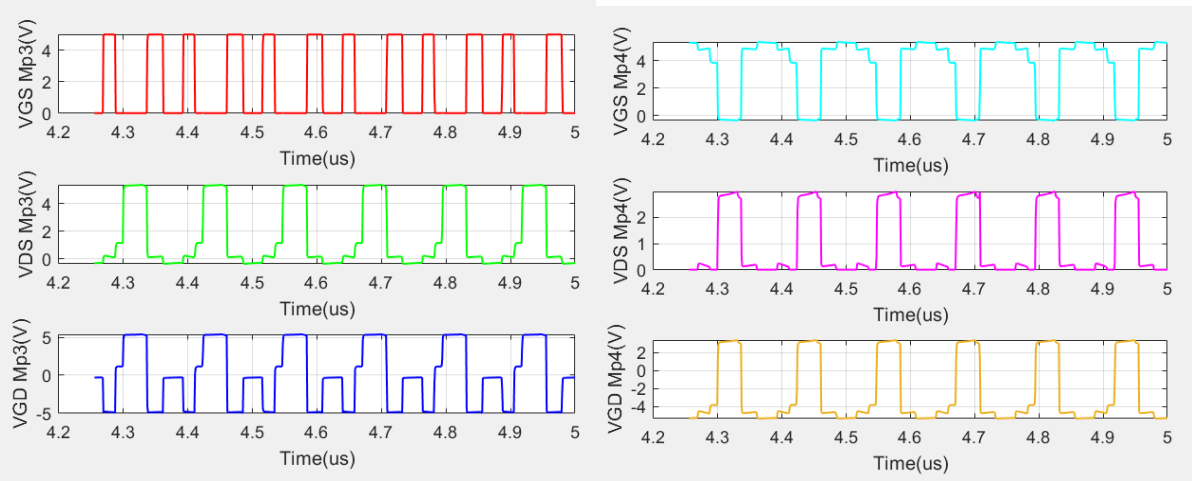
(a) Total power v.s. width of M_{p3} and M_{p4}.

(b) Output wave v.s. width of M_{p3} and M_{p4}.

Figure 4.3: Different width of M_{p3} and M_{p4} with different power consumption and V_{out}.

B. Sizing of switch S2 Figure 4.3 shows the total power and output wave with different width of M_{p3} and M_{p4}. The larger the widths of M_{p3} and M_{p4} are, the larger total power the pulser consumes. The widths of M_{p3} and M_{p4} influence the value of V_{out} in 3 different phases, which are Φ_1, Φ_2, and Φ_3. The larger widths of M_{p3} and M_{p4} enable larger output voltage levels. Both the width of M_{p3} and M_{p4} are chosen as 21 μm.

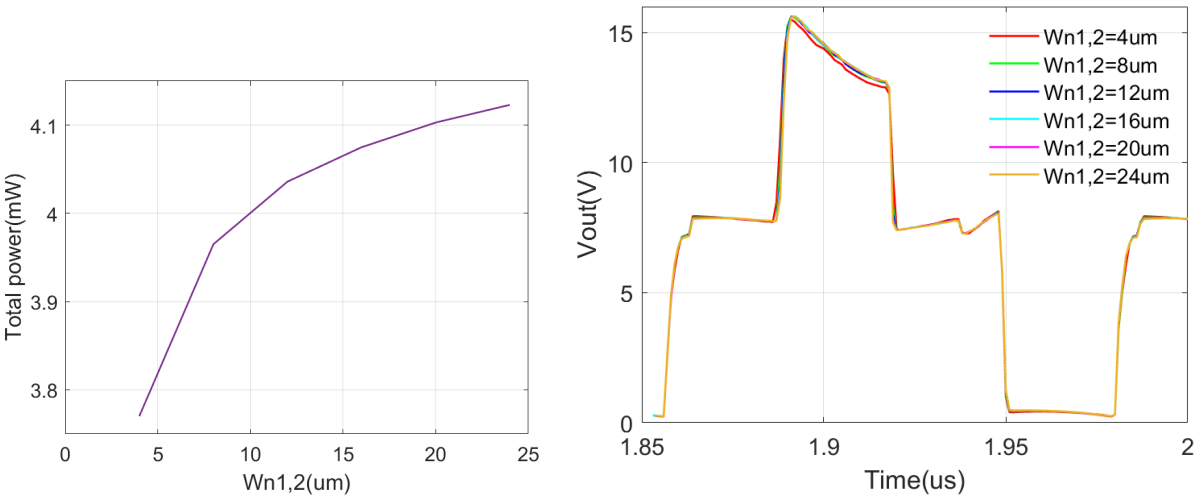
Simulation results for V_{GS}, V_{DS}, and V_{GD} of M_{p3} and M_{p4} are shown in Figure 4.4. The figures shows that terminal voltages of M_{p3} and M_{p4} are in the safe region.



(a) V_{GS}, V_{DS}, and V_{GD} of M_{p3}.

(b) V_{GS}, V_{DS}, and V_{GD} of M_{p4}.

Figure 4.4: Voltages between terminals of M_{p3} and M_{p4}.



(a) Total power v.s. width of M_{n1} and M_{n2}.

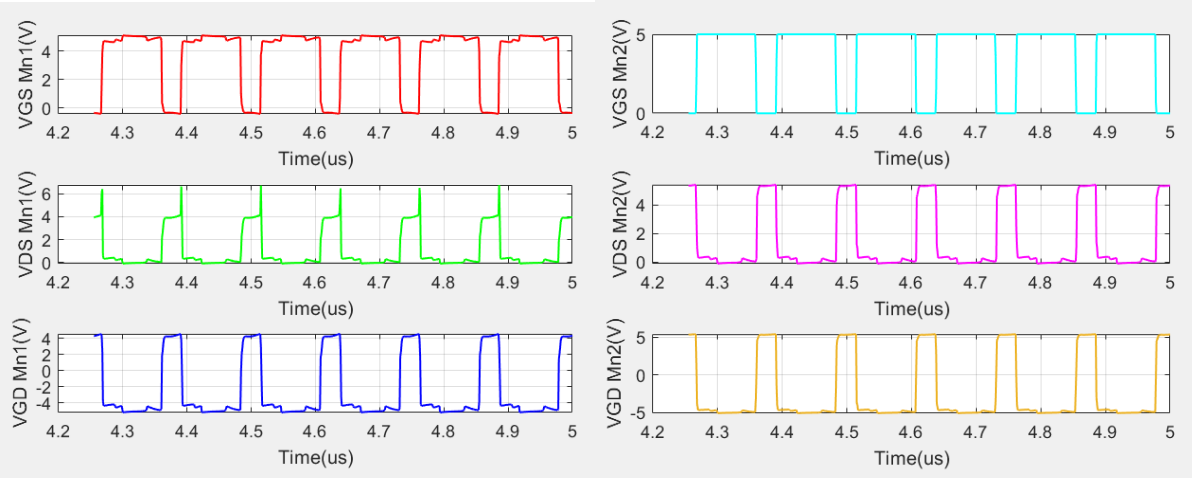
(b) Output wave v.s. width of M_{n1} and M_{n2}.

Figure 4.5: Different width of M_{n1} and M_{n2} with different power consumption and V_{out}.

C.Sizing of switch S3 Figure 4.5 shows the total power and output wave with different width of M_{n1} and M_{n2}. The larger the widths of M_{n1} and M_{n2} are, the larger total power the pulser consumes. The widths of M_{n1} and M_{n2} have very little influence on the output wave of the pulser. To save power, both the width of M_{n1} and M_{n2} could be chosen smaller, like 4 μm.

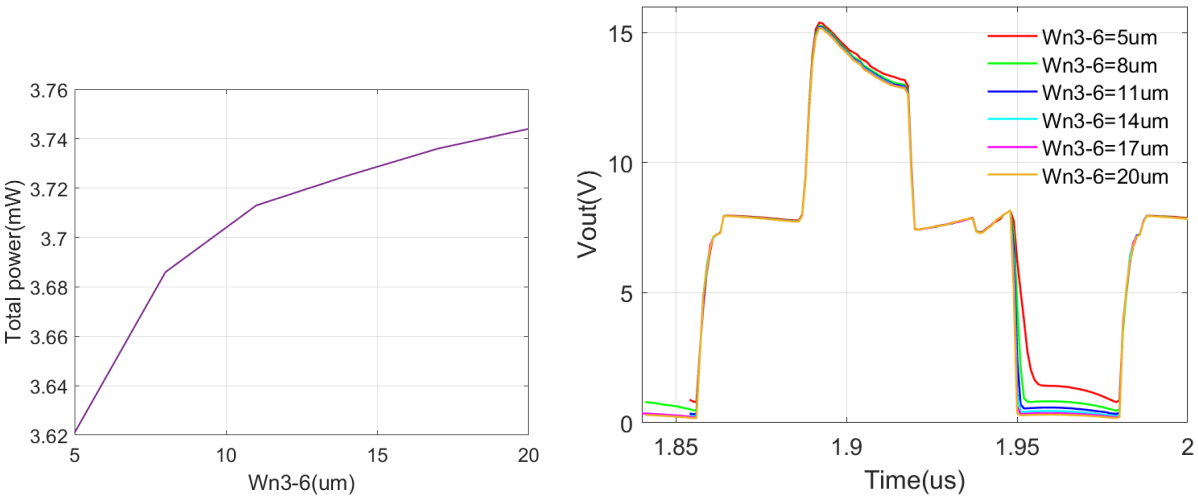
Simulation results for V_{GS}, V_{DS}, and V_{GD} of M_{n1} and M_{n2} are shown in Figure 4.6. The figures shows that terminal voltages of M_{n1} and M_{n2} are in the safe region.

D. Sizing of switch S4 Figure 4.7 shows the total power and output wave with different width of M_{n3} to M_{n6}, which are the four stacked NMOS noted in Figure 3.3. Still, the larger widths relate to a larger power consumption. However, the power consumption for different widths of these NMOS is mild. The widths of M_{n3} to M_{n6} influence the value of V_{out} during the last phase when the voltage on the transducer is supposed to be completely discharged. Considering these, widths of M_{n3} to M_{n6} should be set larger. In order to avoid any exceeding voltage over



(a) V_{GS}, V_{DS}, and V_{GD} of M_{n1}. **(b)** V_{GS}, V_{DS}, and V_{GD} of M_{n2}.

Figure 4.6: Voltages between terminals of M_{n1} and M_{n2}.



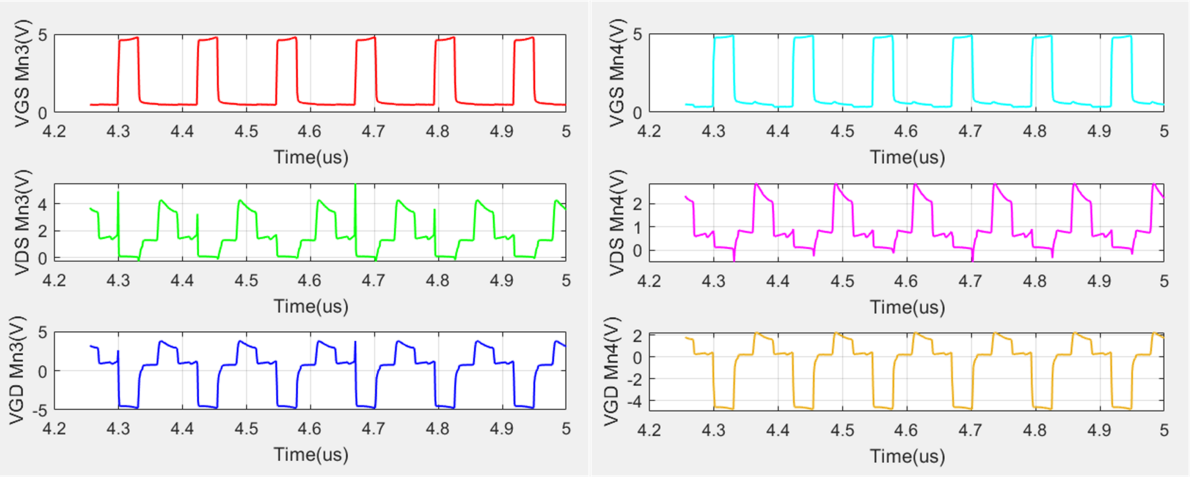
(a) Total power v.s. width of M_{n3} to M_{n6}. **(b)** Output wave v.s. width of M_{n3} to M_{n6}.

Figure 4.7: Different width of M_{n3} to M_{n6} with different power consumption and V_{out}.

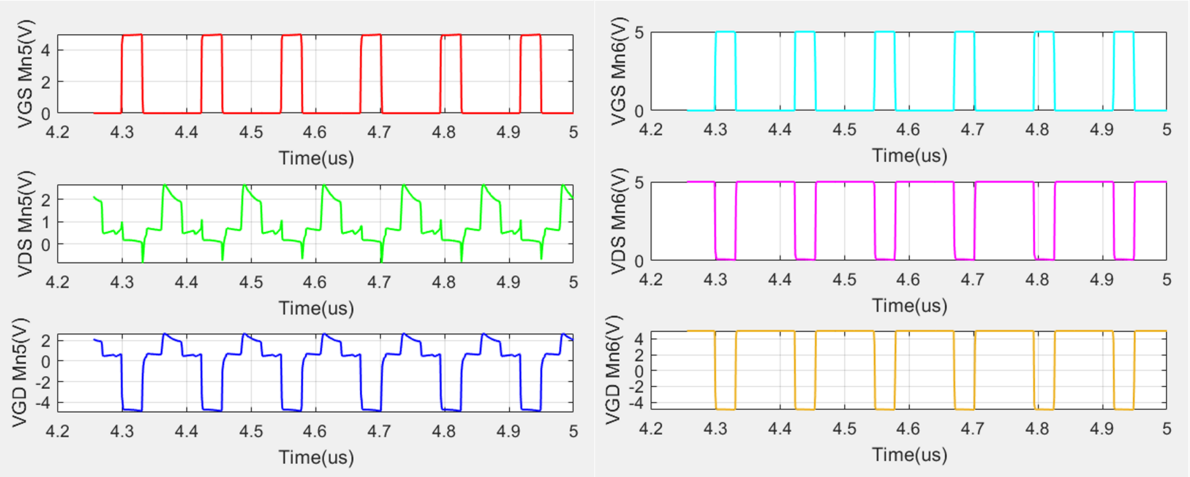
the transistors, and to divide the output voltage over four NMOS transistors, widths of M_{n3} to M_{n6} are set as 20 μm, 15 μm, 10 μm and 18 μm, respectively.

Simulation results for V_{GS}, V_{DS}, and V_{GD} of M_{n3} to M_{n6} and M_{p7} to M_{p9} are shown in Figure 4.8. The figures shows that terminal voltages of M_{n3} to M_{n6} and M_{p7} to M_{p9} are in the safe region.

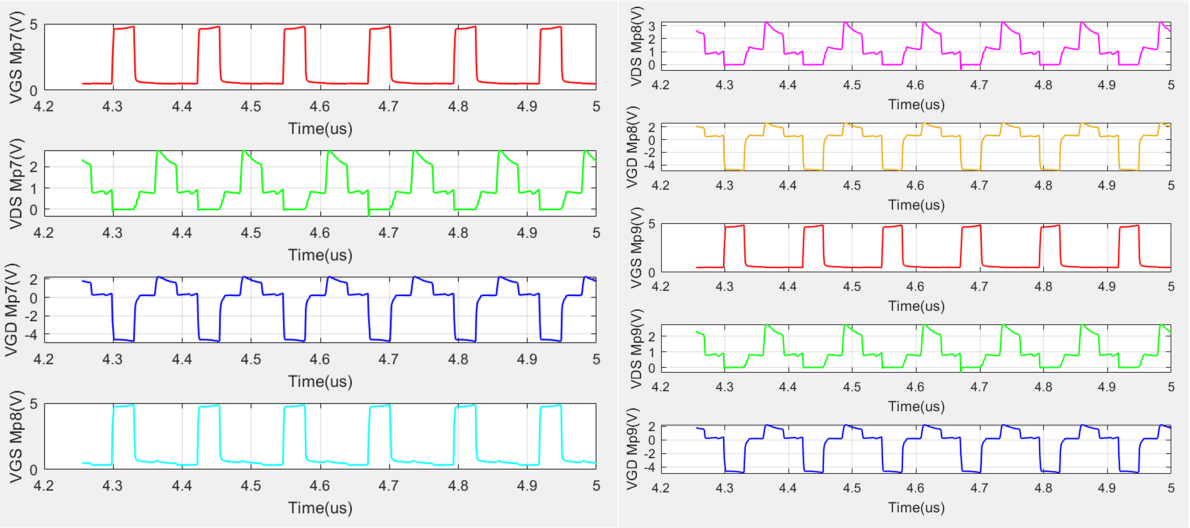
E. Sizing of switch S5 Figure 4.9 shows the total power and output wave with different width of M_{p5} and M_{p6}, which were noted in Figure 3.3. As all the situations mentioned above, the larger widths of these two PMOS lead to a larger power consumption of the whole pulser. V_{out} during the doubling phase is also related to the widths of M_{p5} and M_{p6}. When the widths are too small, the voltage level of V_{out} would not be enough for the application. As long as the widths of M_{p5} and M_{p6} are larger than 11 μm, the difference between different level of the output voltage becomes smaller. In order to avoid any exceeding voltage over the transistors, and to eqully divide the voltage difference over the two PMOS transistors, widths of M_{p5} and



(a) V_{GS}, V_{DS}, and V_{GD} of M_{n3} and M_{n4}.



(b) V_{GS}, V_{DS}, and V_{GD} of M_{n5} and M_{n6}.

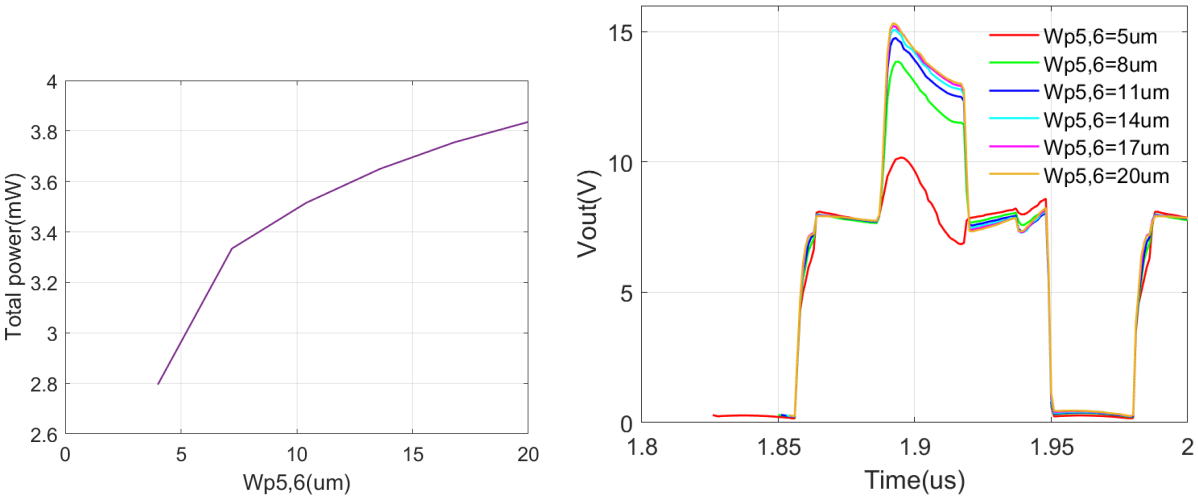


(c) V_{GS}, V_{DS}, and V_{GD} of M_{p7} to M_{p9}.

Figure 4.8: Voltages between terminals of switch S4.

M_{p6} are set as 10 μm and 24 μm, respectively.

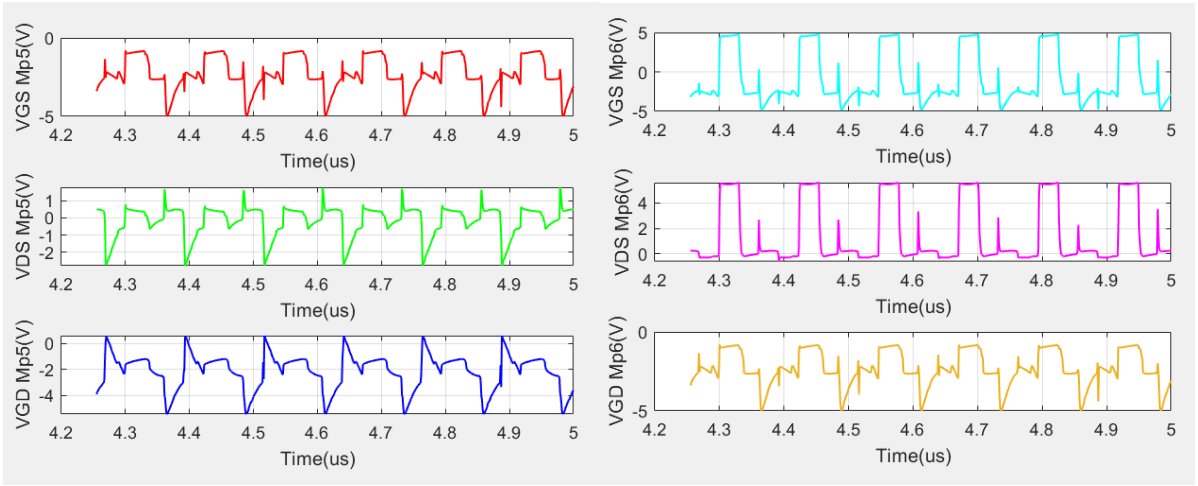
Simulation results for V_{GS}, V_{DS}, and V_{GD} of M_{p5} and M_{p6} are shown in Figure 4.10. The



(a) Total power v.s. width of M_{p5} and M_{p6}.

(b) Output wave v.s. width of M_{p5} and M_{p6}.

Figure 4.9: Different width of M_{p5} and M_{p6} with different power consumption and V_{out}.



(a) V_{GS}, V_{DS}, and V_{GD} of M_{p5}.

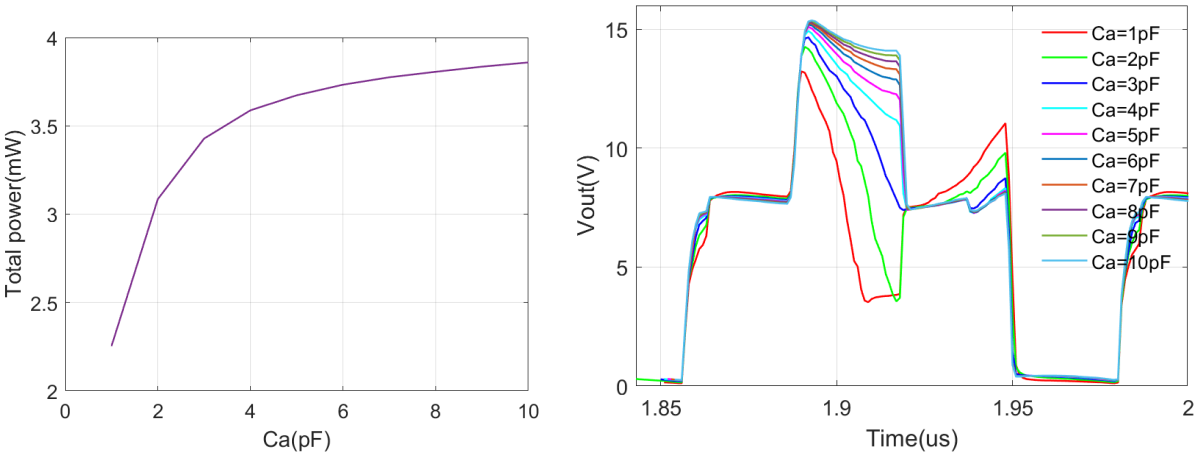
(b) V_{GS}, V_{DS}, and V_{GD} of M_{p6}.

Figure 4.10: Voltages between terminals of M_{p5} and M_{p6}.

figures shows that terminal voltages of M_{p5} and M_{p6} are in the safe region.

F. Sizing of bootstrap capacitor C_a The power consumption of the pulser and the output wave are shown in Figure 4.11 by sweeping different value of C_a from 1 pF to 10 pF. Figure 4.11 (a) shows the power consumption changes greatly with C_a, meaning that this capacitor is the most power-consumed part in the pulser circuit. A smaller C_a guarantees a lower power consumption. However, if the capacitance of C_a is not large enough, capacitors would be rapidly discharged during the doubling phase, making the output voltage wave not work, like the wave in green line in Figure 4.11 (b). Thus, C_a should not be chosen too small. On the other hand, a large capacitor requires a large area on the chip, requiring C_a not to be too large. The capacitance is determined as 6 pF, considering the power, area, and the output wave shape.

Table 4.1 shows all the widths of the devices in the HV driver.



(a) Total power v.s. capacitance of C_a.

(b) Output wave v.s. capacitance of C_a.

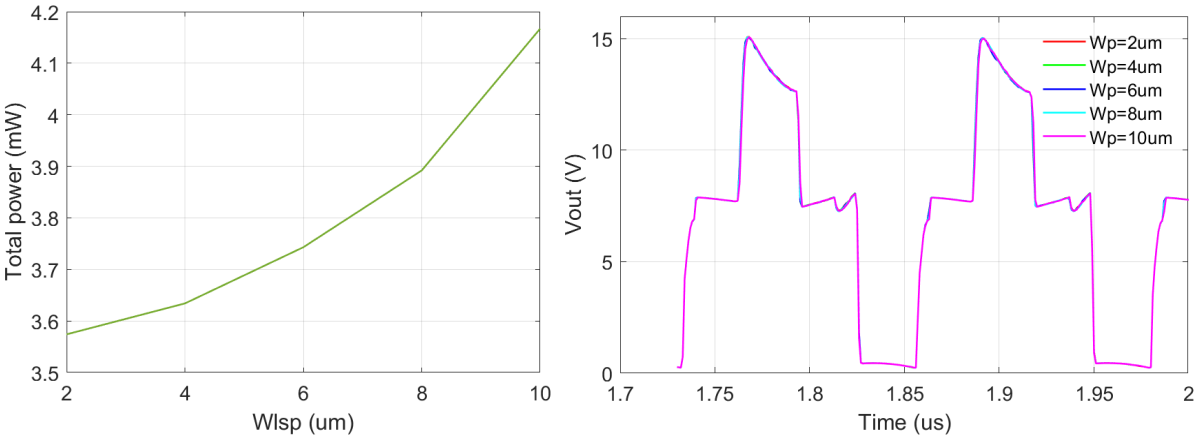
Figure 4.11: Different capacitance of C_a with different power consumption and V_{out}.

Table 4.1: SELECTIONS OF WIDTHS AND CAPACITANCE IN THE HV DRIVER

M_{p1}	M_{p2}	M_{p3}, M_{p4}	M_{p5}	M_{p6}	M_{p7}	M_{p8}	M_{p9}
16 μm	8 μm	21 μm	10 μm	24 μm	10 μm	14 μm	18 μm
M_{n1}, M_{n2}	M_{n3}	M_{n4}	M_{n5}	M_{n6}	M_{b1}, M_{b2}	M_{b3}, M_{b4}	C_a
4 μm	20 μm	15 μm	10 μm	18 μm	1 μm	1 μm	6 pF

4.1.2. Sizing of the level shifter

It's necessary to also size transistors in the two level shifters (Figure 3.12) to minimize the whole power consumption. Parametric Analysis is also used to sweep the width of PMOS and NMOS transistors to see how different widths of transistors influence the whole power and output wave.



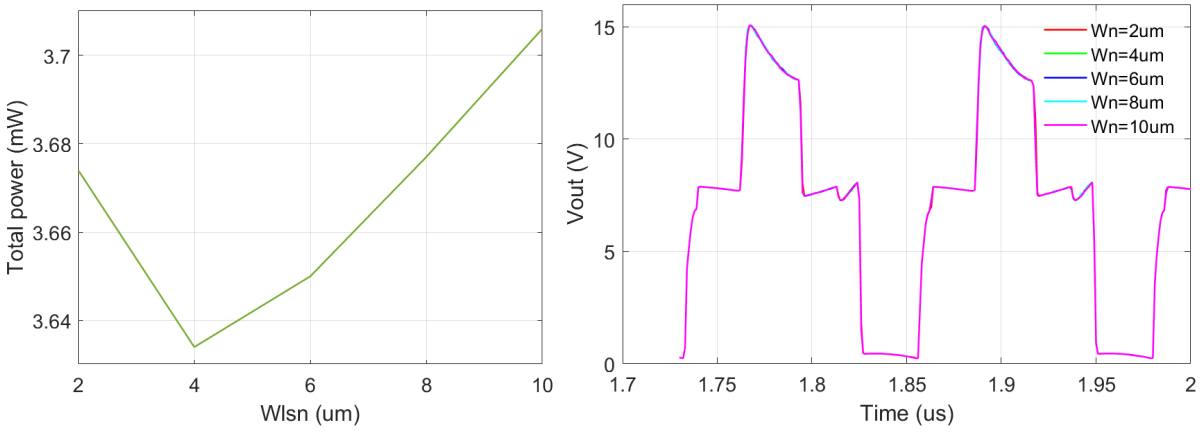
(a) Total power v.s. width of M_{lsp}.

(b) Output wave v.s. width of M_{lsp}.

Figure 4.12: Different width of M_{lsp} with different power consumption and V_{out}.

Figure 4.12 shows the total power and output wave with different widths of PMOS transistors in the level shifter. Figure 4.12 (a) shows the larger the PMOS transistors are, the larger power the pulser consumes. There's no influence on the output waveform from different widths of the PMOS transistors in the level shifter, according to Figure 4.12 (b). Thus, the width of

PMOS transistors could be chosen smaller. In this case, they are chosen as 4 μm.



(a) Total power v.s. width of M_{lsn}.

(b) Output wave v.s. width of M_{lsn}.

Figure 4.13: Different width of M_n with different power consumption and V_{out}.

Figure 4.13 shows the total power and output wave with different widths of NMOS transistors in the level shifter. There's also no influence on the output waveform from different widths of the NMOS transistors in the level shifter. When the widths of PMOS transistors are fixed at 4 μm, the total power consumption meets the lowest point when the widths of the NMOS transistors are also 4 μm. Here, in order to equally divide the output voltage over the two NMOS transistors, the widths of the upper NMOS transistors are chosen at 2 μm, and 4 μm is chosen for the bottom NMOS transistors.

Table 4.2 shows the sizing results for the level shifter.

Table 4.2: SELECTIONS OF WIDTHS FOR THE LEVEL SHIFTERS

M_{ls1}, M_{ls2}	M_{ls3}, M_{ls4}	M_{ls5}-M_{ls8}
4 μm	2 μm	4 μm

4.1.3. Sizing of the conventional class-D pulser

In the conventional class-D pulser shown in Figure 3.13, the width of the HV transistor, the resistance of R_{ls}, and the capacitance of C_{ls} can influence the total power consumption. For example, when the supply voltage is 15 V and we want a 10 V to 15 V Signal 1 at the gate of HV PMOS, if the capacitance of C_{ls} is too small, the output values of the zener diode level-shifter are not exact 10 V and 15 V, leading to a larger power consumption. However, in the conventional design we also should take the area limitation into consideration, meaning that C_{ls} could not be too large. Thus, C_{ls} is chosen as 6 pF as well.

Table 4.3 shows the device selections for the width of the transistors, the capacitance and resistance of the zener diode level-shifter in the conventional class-D pulser shown in Figure 3.13.

Table 4.3: SELECTIONS OF WIDTHS AND CAPACITANCE FOR THE CONVENTIONAL PULSER

M_p	M_n	C_{ls}	R_{ls}
50 μm	25 μm	6 pF	1 $M\Omega$

4.2. Simulation results of the proposed pulser

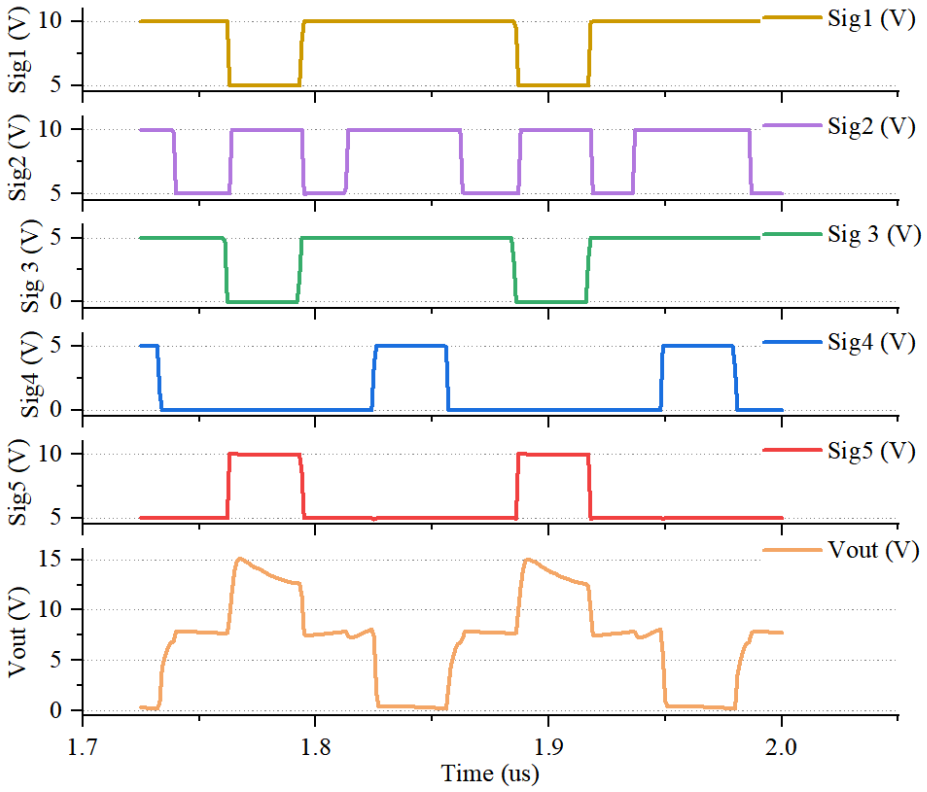


Figure 4.14: Transient waveform of control signals and the output voltage wave of the proposed pulser.

The proposed pulser has been implemented using the sizes in Table 4.1. The transient simulation result is shown in Figure 4.14. At the beginning of Φ_1, Sig2 keeps being at 10V for 6 ns, so that some charges on C_a flow to C_0 in the transducer. V_{out} increases to 7 V after this short charge-redistribution period. During the next part of Φ_1, V_{out} keeps a voltage level around 8 V. During the doubling phase Φ_2, V_{out} first increases to 15.5 V, then decreases to near 12.8 V because charges on capacitors flow into ground through the resistor R_1. Then it comes to Φ_3 where V_{out} decreased to 7.5 V, increasing with a slight slope. There's a 12-ns' slot after Sig2 goes from 5 V to 10 V, making V_{out} have a quick drop and then increase to 8.1 V with a slope. In Φ_4 Sig4 turns from 0 to 5V, connecting the transducer to the ground. Sig3 keeps being at 5V so that the left node of C_a is connected to the ground.

The power consumption of the whole pulser is 4.588 mW.

4.3. Discussion

4.3.1. Measuring the power efficiency

The output waveform reaches the maximum value of 15.5 V during the voltage-doubling phase. To make a fair comparison, a conventional class-D pulser with a supply voltage of 15 V should be set for comparison. Figure 4.15 presents the transient simulation results of the control signal Signal1 and Signal 2, as well as the output voltage V_{con}.

The power consumption of this 15-V conventional class-D pulser is 7.104 mW. Compared with this, the proposed pulser shows an improvement of power efficiency as 35.4% when

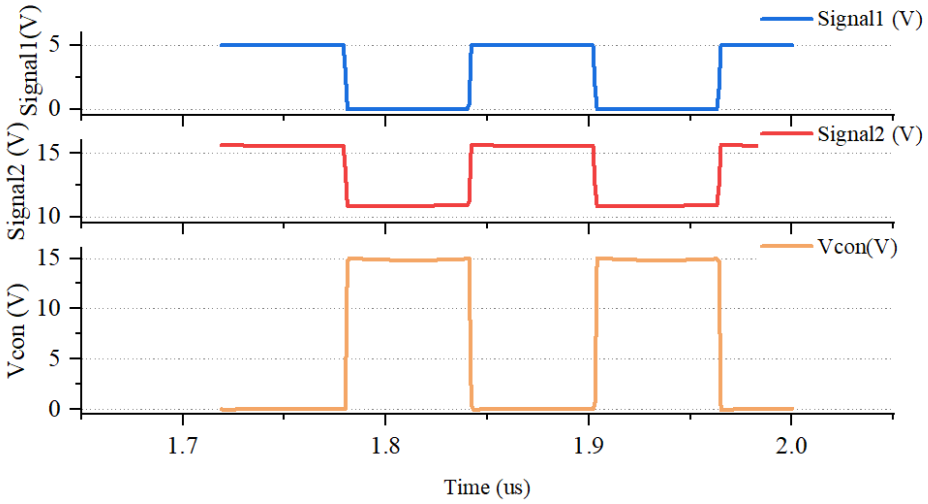
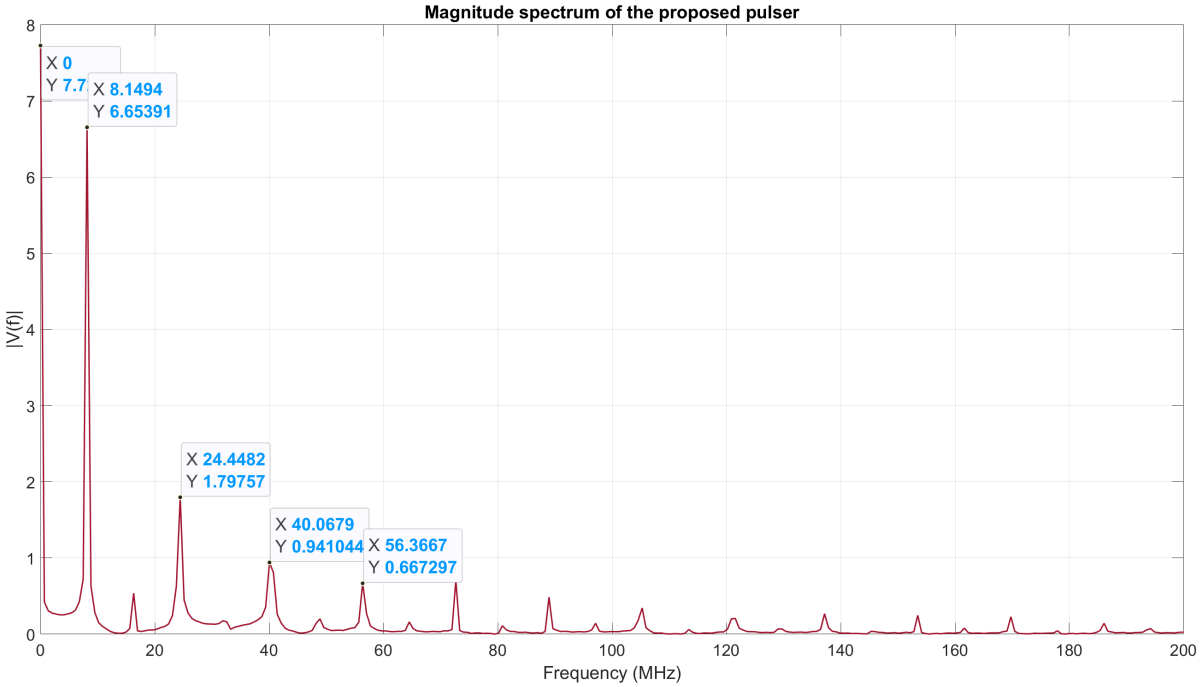


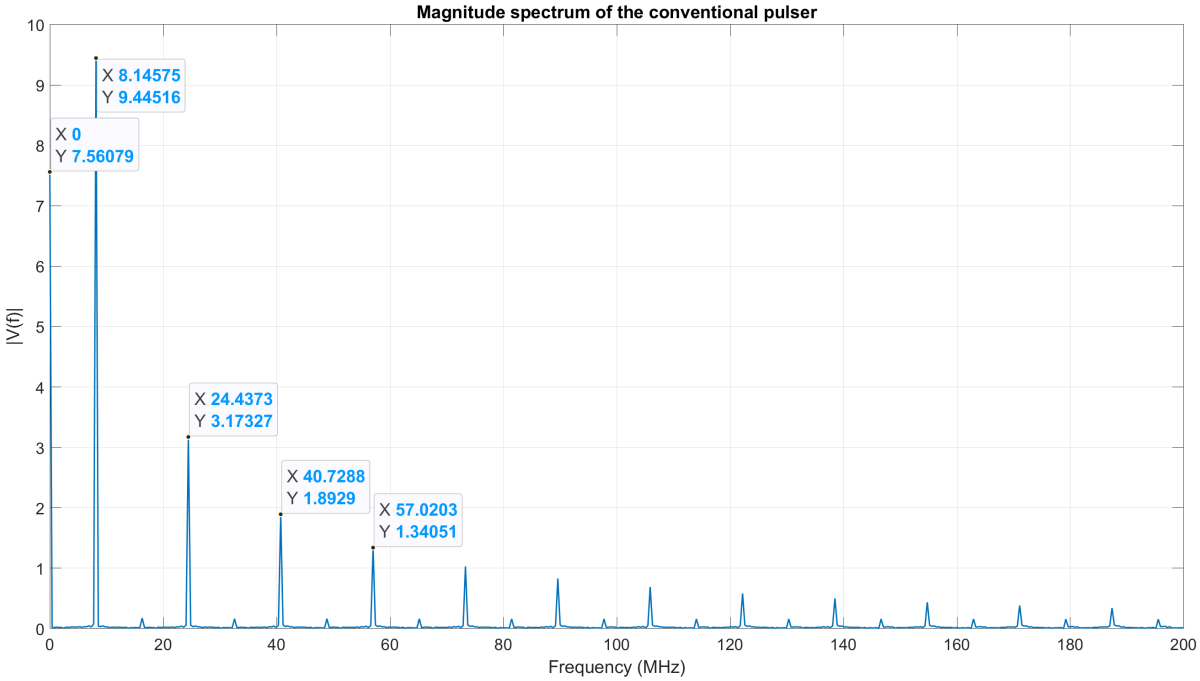
Figure 4.15: Transient waveform of control signals and the output voltage of the conventional class-D pulser with 15-V supply voltage.

driving a PZT transducer.

To further verify the power efficiency of the proposed pulser, the output spectrums of the proposed pulser and the conventional pulser are drawn in Figure 4.16. The output voltage waves of the proposed pulser and the conventional pulser have similar DC component. On the other hand, the conventional pulser's output has a larger magnitude of the basic harmonic near 8.15 MHz, which may relate to a better triggering on the transducer. However, the other harmonics in the spectrum, which are the odd harmonics, are larger than those of the conventional one. The output voltage wave of the proposed pulser has the basic harmonic as the main harmonic, and the other harmonics have much lower magnitudes, verifying the power efficiency of the proposed pulser.



(a) The output wave spectrum of the proposed pulser.



(b) The output wave spectrum of the conventional pulser with 15-V supply voltage.

Figure 4.16: The output wave spectrum distribution.

As this design was supposed to work at 20 V, to make a completer comparison, a conventional class-D pulser with a supply voltage of 20 V is also used for comparison. Figure 4.17 presents the transient simulation results of the control signal Signal 1 and Signal 2, as well as the output voltage V_{con20}.

The power consumption of this 20-V conventional class-D pulser is 12.59 mW. Compared with this, the proposed pulser shows an improvement of power efficiency as 63.56% when driving a PZT transducer. However, as the proposed design could not achieve effective 20 V

voltage at the output, the real improved power efficiency should be divided by 20/15, equalling to 42.37%.

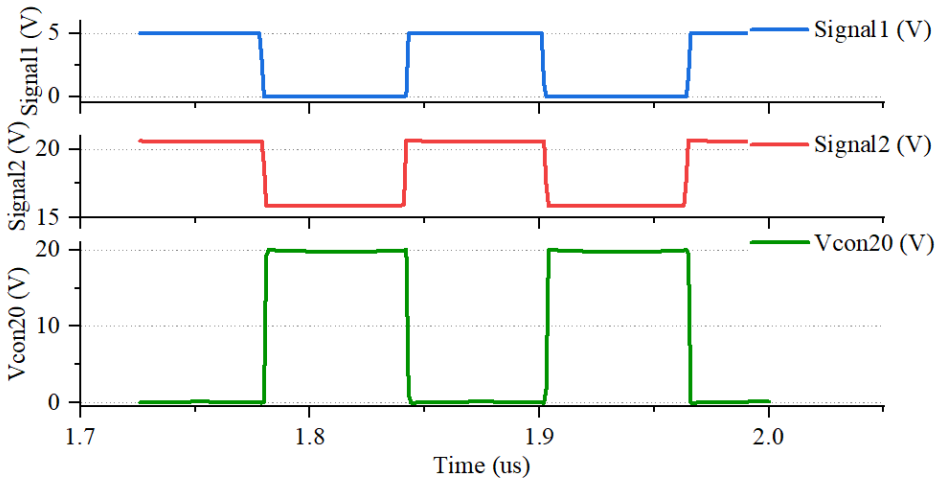


Figure 4.17: Transient waveform of control signals and the output voltage of the conventional class-D pulser with 20-V supply voltage.

4.3.2. Different operation of S2

One way of saving power in this design is to shortly open the switch S2 during Φ_1 and Φ_3. In this part, the case where S2 is not opened during the two phases is simulated for a comparison. Figure 4.18 shows the transient waveform of control signals and the output voltage. It's clear that there's no short pre-charging period in Φ_1 and the output wave has a smooth ascending slope in Φ_3. The waveform is also transformed to the frequency domain to see if it works effectively. Figure 4.19 shows the output voltage spectrum without shortly opening the switch S2. The DC component is larger than that of the proposed one, and the basic harmonic is slightly smaller. Moreover, the third harmonic shows slightly larger magnitude.

The total power consumption of this pulser is 4.988 mW, demonstrating that opening the switch S2 for a short time helps to save energy, while does not affect the output spectrum of the proposed design, which, actually seems better with larger basic harmonic at 8.15 MHz and smaller third harmonic at 24.45 MHz compared with the spectrum in Figure 4.19. In this case, 3 control signals are still needed.

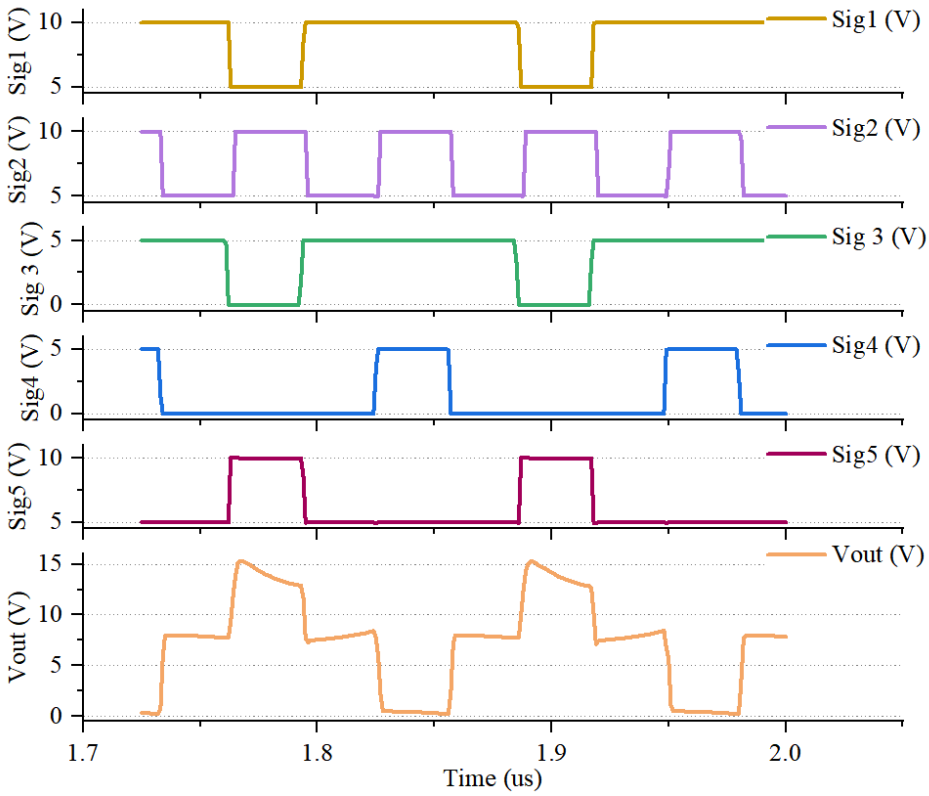


Figure 4.18: Transient waveform of control signals and the output voltage where S2 is not opened during Φ_1 and Φ_3.

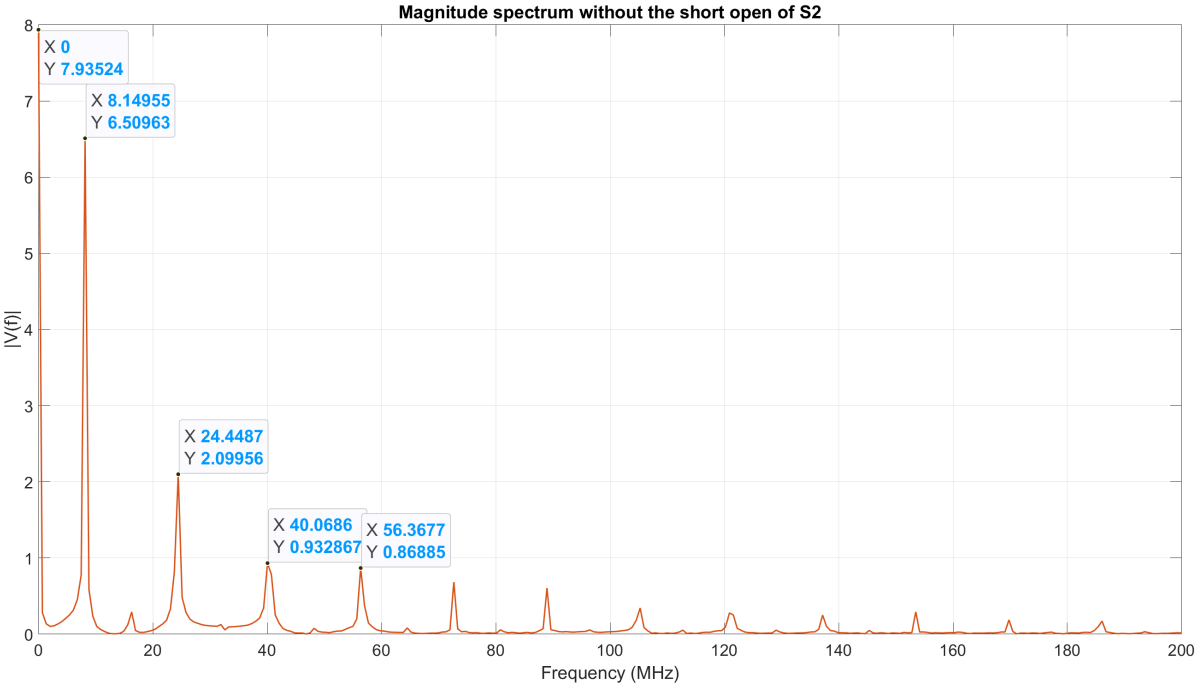


Figure 4.19: Spectrum of the output wave without the short open of S2.

5

Conclusion

This thesis presents a power-efficient 3-level high-voltage pulser with TSMC 0.18-μm technology. The proposed pulser drives an ultrasound PZT transducer with a resonant frequency of 8.15 MHz. To make the design more power efficient, the circuit utilizes a bootstrap structure to double the 10-V supply voltage, and saves energy by cleverly controlling the closing of individual switches according to the physical characteristics of the PZT transducer model. The simulation results shows a 35.4% power efficiency improvement of the proposed design, compared with the conventional class-D pulser.

5.1. Main contribution

The goal of the project is to design a power-efficient pulser for an ultrasound transducer, which is adopted in a 2D ultrasound phased-array transmitters (TX). The area of the TX circuit in a 2D phased array is limited to half of the sound wavelength, posing an area limitation for the circuit. The transducer element used in this case has an area of 100$\times$ 100 μm^2. Thus, consideration for the area efficiency is also an important aspect through the design process. As a pulser is usually the most power-hungry block in an ultrasound transmitter, there have been plenty of works dedicated to improve the power efficiency of a pulser in ultrasound applications. At the first period of this project, many power-efficient methods were reviewed. For example, [12] proposed an energy-replenishing pulser. It could ideally eliminate the dynamic power loss on the capacitor in the transducer by replenishing the supplied energy utilizing an inductor. [13] introduced a charge redistribution technique. The general principle is to re-use half of the charge at each cycle by connecting both plates of the transducer together. [2] utilizes the multilevel pulsing with charge recycling to improve pulser's power efficiency. In all the reviewed works, designers have to strike a balance between power consumption and other performance requirements of the system to design a suited pulser to match the corresponding situations. The reviewed different methods provide inspirations for this project, from when method of doubling the supply voltage and making multi-level output voltage waves planted a seed for this project.

This work utilizes a capacitor to construct a bootstrap circuit to double the supply voltage. By effectively controlling the open and close of 5 switches, a 3-level output voltage wave is generated. The design adopted stacked standard CMOS transistors instead of HV transistors for the 5 switches. To make the whole phases of charging and discharging the transducer operate effectively, stacked transistors as switches are inevitably large. Thus, an idea that shortly turn

off two of the largest transistors is proposed. Ideally, the 3 levels of V_{out} are expected as 0, 10 V and 20 V. However, due to the influence of parasitics and on-resistance of the transistors, the 3 levels' V_{out} in this design are around 0, 8 V, 15 V. The resistance in the BVD model of the PZT transducer is small, resulting charges on capacitors flow through the resistor to the ground with a rapid speed. To solve this, on one hand, the complete BVD model is utilized instead of the simplified model, which is not accurate at presenting energy storage and release of the transducer. On the other hand, a larger capacitor C_a could help to stable the voltage at the output node, though occupying a larger area is unavoidable. The V_{out} wave still has a slight descending slope during the doubling phase. By converting the time-domain output waveform to frequency domain, the V_{out} spectrum shows the basic harmonic at 8.15 MHz is still the dominant one, and the other harmonics are smaller than those of the conventional class-D puler, so the proposed pulser could effectively drive the transducer. To make the comparison as fair as possible, the conventional pulser as a reference is also designed in its most power-efficient condition. For example, the level-shifter used in the conventional pulser is an RC high-pass filter level-shifter, guaranteeing the lowest power consumption. The simulation results shows a 35.4% power efficiency enhancement of the proposed design compared with the conventional class-D pulser with a 15-V supply voltage. Compared with the conventional pulser with a 20-V supply voltage, the proposed design shows a 42.37% power-efficiency improvement.

5.2. Discussion

The conventional class-D pulser is still the simplest puler without a doubt. As mentioned in the literature review part, all the fancy designs for a pulser are to make a balance between power consumption and other performance requirements. There is not a design that could own power efficiency, area efficiency, simplicity and wild application in the same time. This also applies in the proposed design. The proposed pulser has 3 control signals for 5 switches, making the circuit more complex than the conventional design.

The project was concentrated on the schematic design phase. Due to time-limitation, several critical follow-up processes were not fully realized. One such process is the layout phase, which involves the physical arrangement of the components in the proposed circuit. The Design Rule Check (DRC), Layout Versus Schematic (LVS), and Post-layout (PEX) simulations, which are essential for ensuring the reliability and functionality of the IC, could not be thoroughly performed. The whole design could be better evaluated if an opportunity of tapeout could be grasped. Tapeout is a critical phase, as it allows for the practical evaluation of the design in a real-world context, providing invaluable feedback that are not apparent in simulations alone. This missed opportunity limits the practical assessment of the design's effectiveness.

In conclusion, while the project successfully achieved 35.4% of power-efficiency improvement by designing a multi-level power-efficient pulser, the circuit could not be as simple as the conventional pulser anymore. Moreover, the lack of critical post-schematic phases limits the extent to which the design could be validated and refined.

5.3. Suggestions for prospective works

- The proposed design may achieve better power efficiency when utilized in higher voltage-level applications, such as when using a 20-V supply voltage. In higher-voltage conditions, more sophisticated stacked CMOS structure is needed to guarantee all voltages

between terminals are within the limitation. Also, more fancy level-shifters are necessary.

- Making more output voltage levels is a promising direction for power efficiency. On one hand, more voltage levels means more energy is saved and reused in the circuit. The premise is that the additional power consumption on additional circuit for making more output levels is not larger than the saved power. On the other hand, voltage wave with more levels has a shape that is more like a sine wave, making the trigger on the transducer more effective. [33] proposed a 7-level high-voltage pulser, achieving an impressive power reduction of 75.4% compared to fCV^2, becoming one of the most significant power reduction reported so far. More storage capacitors and more complex circuit set a barrier for area-efficiency, especially from the capacitors that could not be on-chip. Further works are expect to release this conflict of power-efficiency and area-efficiency in a multi-level high-voltage pulser.
- Inductors would help in a pulser. An inductor has theoretically 0 energy-loss in a pulser during charging and discharging for a transducer. For example, [8] proposed an energy-replenishing circuit achieving 73.1% power efficiency. However, this work does not utilize an inductor because inductors are usually area-occupied, considering the 2D ultrasound phased-array is under the area-limitation from half of the sound wavelength. However, a comparatively small inductor combined with storage capacitors is a way to explore.
- Allocating additional time for the post-schematic phases and incorporating a tapeout process is highly recommended. This stage not only provides an assessment of the design's practical application but also offers invaluable insights into real-world performance and potential areas for improvement.

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