A 3-by-3 400-MHz LC microsensor array for wireless capacitive biosensing

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A 3-BY-3 400-MHZ LC MICROSENSOR ARRAY FOR WIRELESS CAPACITIVE BIOSENSING

Thesis

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ABSTRACT

Biosensing has been developed rapidly for a number of biomedical applications, including neural monitoring, protein detection, bacteria detection and blood glucose monitoring. Among the branches of bio-sensing, capacitive sensing is a promising technique and utilized widely, since it is rapid, simple, label free and inexpensive. Compared with traditional capacitance sensing front end, capacitance to frequency (CFC) based front-end can be utilized to measure the capacitance change based on the frequency shift in the output. LC voltage-controlled oscillator (VCO) based CFC benefits from low power, low cost, high sensitivity, embedded wireless capability and miniaturized characterization, and it can be based on passive or active approaches. The limitation of cutting edge LC VCO based system is they are single channel. This thesis presents the design of a 3-by-3 400-MHz LC VCO based microsensor array for measuring bacteria concentration and related bio-analyte which behave capacitively in that frequency range. This would allow for high-resolution wireless capacitive sensing in a power-efficient way. The wireless capacitive microsensor array has been designed in a standard 0.18 µm CMOS process. The sensor array is comprised of 3-by-3 pixels, and it is implemented by customized interdigitated capacitors. Each pixel has two customized 10.5 µm * 10.5 µm capacitors with 100fF capacitance value. A class-B VCO is implemented with 300fF buried metal-oxide-metal (MOM) capacitor and 300nH off-chip inductor. The class-B oscillator converts the capacitance change in the sensor array into frequency shift and transmits the signal through wireless inductance link. The central frequency varies within ±3.3 MHz, with less than 1.4% RMS phase noise in process corners. By post-layout extraction, the circuit has 417 kHz/fF responsivity, 99.8%R^2 value and 1.5% RMS phase noise. Each pixel occupies and area of 30 µm * 25 µm area. In total, the whole front-end core circuit takes 140 µm * 160 µm chip area. This project contributes to further development of the multi-channel LC VCO based sensing system, which could be utilized as a multi-channel low-power capacitance sensing technique in a long-term vision with combined detection and wireless transmission in the same front-end.

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To the sleepless nights. To the fallen hairs. The most important, to the unforgettable dream of my young age.

Shengjie Chen
Delft, September 20, 2020

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INTRODUCTION

In this chapter, the background and principles of bio-capacitive sensing will be introduced. The introduction is written by a top-down approach, from bio-sensing to capacitve sensing, including introduction and comparison between different sensing techniques. At the end of this chapter, the specification of design will be generated.

1.1. BIO-SENSING

Recently, wireless chemical sensors(WCSs) is developed rapidly. The development is driven by the rising demand of healthcare, food-chain, miniaturized sensing system, and advanced (bio)chemical sensing methods from academia [1]. A biosensor is a kind of device which is capable to detect the selected biological analyte information quantitatively or semi-quantitatively. In addition, the biosensor should be able to convert the biological signal into a processable signal [14]. Figure 1.1 shows the general system diagram of wireless biochemical sensing system, which contains the sensor interface, the wireless link and the data analysis part, which is the most general and top-level system diagram. However, the system diagram varies based on applications and detailed designs, which will be discussed in chapter 1.2.

Generally, there are two methods to classify the biosensors. The first method is by classifying the target bio-analyte, such as whole cells, enzymes, glucose and antibodies. An alternative method is to classified the biosensors according to the transconduction mechanism, i.e., electrochemical, optical, electrical and mass sensitive [1, 14]. Further discussion will follow the second method of classification, i.e., according to the transconduction mechanism.

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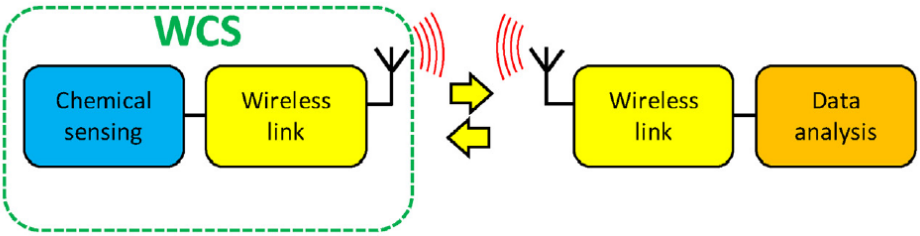

Figure 1.1: Wireless (bio)chemical sensor system diagram [1]

Electrochemical sensors are abundantly used in pH sensing[15], Na^+ sensing[16] and glucose monitoring[17]. Among the transduction mechanisms, potentiometry and amperometry are the two most widely used mechanisms. These system can realize the sweat monitoring[16], aquaculture fish monitoring[17], saliva monitoring[18]. Depend on applications, these systems are embedded with various wireless transmission protocols, such as ZigBee, bluetooth and ISM/SRD.

The optical sensor is suitable for designing miniaturized devices. Classified by transduction mechanism in the topic of optical sensors, absorbance[19], fluorescence[20] and reflectance[21] are three most widely applied mechanism. The optical sensors can be applied to different scenarios, such as point-of-care-test (POCT)[22], implantable glucose testing [23] and food quality monitoring [24]. However, to obtain high sensitivity and limit of detection (LOD), a laser source might be needed, which increases the cost of settings. Thus, currently the light emitting diode (LED) is applied to the systems to reduce the cost an get a satisfactory result[1].

The mass sensitive WCS is usually applied with a mass-sensitive sensor such as a quartz crystal microbalance (QCM)[25] and a tuning fork with coated material[26]. The mass of sensor is sensitive to the concentration change of material under test (MUT). This kind of sensor is usually applied for special application cases.

Electrical sensors are flexible to be applied in different application scenarios, such as greenhouse detection [27], ethanol vapour in air[28] and human health monitoring [29]. The crucial part of electrical sensing system is the sensors, which determined by applications. For example, ZnO-graphene modified electrodes are utilized to detect the concentration of acetone in [29]. Electrical sensors are most widely applied with conductometric [30], capacitive[31] and impedimetric transduction mechanism[29].The electrical sensors are usually mounted on print circuit board(PCB) and work with signal processing or wireless transmission circuitry[32] or embedded with the standard CMOS process and fabricated in a lab-on-chip (LoC) system[12].

The figure 1.2 compares the available (bio)chemical sensing mechanisms. The green area represents the electrical sensing methods. 3% of the sensing system utilizes capacitive sensing mechanisms. Focusing on the electrical sensing method, $\frac{1}{7}$ of the electrical mechanism utilized the capacitive sensing. It can be concluded that the capacitive sensing is an attractive trend of development in the topic of bio-sensing. In the following section 1.2, the techniques utilized in capacitive sensing will be discussed, which mainly focus on the circuitry and functionality of the measurement systems.

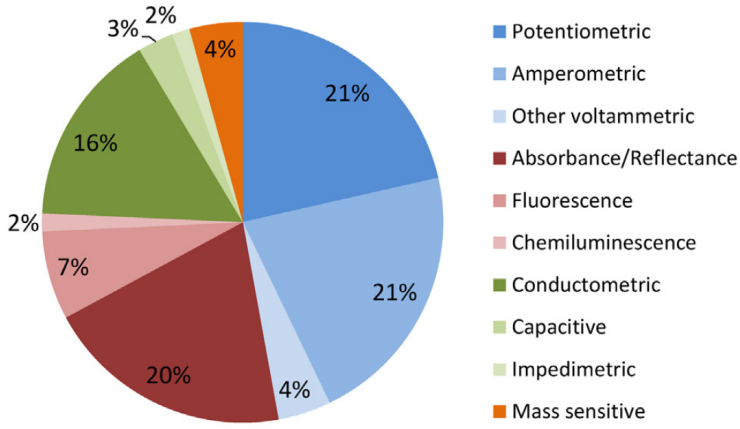

Figure 1.2: Chemical sensor mechanism comparison (blue – electrochemical, red – optical, green – electrical, orange – mass sensitive) [1]

1.2. CAPACITIVE SENSING METHOD

As discussed in 1.1, the conventional sensing system contains (bio)chemical sensing, wireless link (TX and RX port) and digital signal processing (DSP) parts. An alternative is that the sensing system directly embedded the DSP processor with the sensing part on chip (or on PCB board). In this case the wireless link is no longer required. In this section, several kinds of capacitive sensing techniques are discussed, including traditional wired sensing system and wireless sensing system.

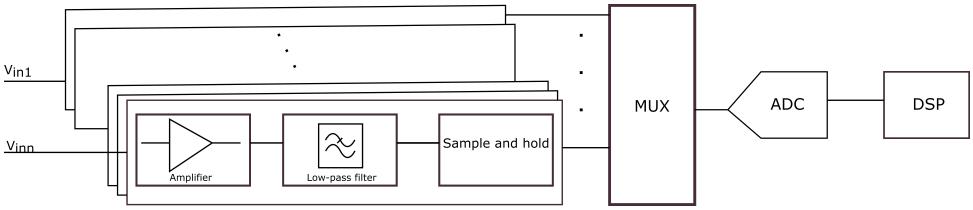

Figure 1.3: Conventional sensing system [2]

Conventionally in the wired bio-sensing system, the data acquisition and processing are all embedded on the same chip. Figure 1.3 shows the complete analog front-end, which includes analog front-end (amplifier), analog-to-digital converter(ADC) and digital signal processing(DSP) parts.

Another methodology is embedded with electromagnetic (EM) biosensor, including radio frequency (RF), microwave (MW), millimeter wave (mmW), tera-Hertz (THz) and optical bio-sensors [33]. Figure 1.4 shows the EM spectrum and nomenclature defined according to IEEE standard [3]. The fundamental of EM sensing is to observe the unique permittivity spectrum generated by cells, tissues or other biological particles. For example, the permittivity spectrum of cancerous cells is different from the healthy cells, so the technique can be utilized in cancer detection. Another application is to measure the permittivity spectrum change caused by the concentration variation of a kind of biological analyte such as glucose, biotin, serotonin, prostate specific antigen. The dis-

1

ease and disorder diagnosis can be helped by measuring the concentration of these analytes. The RF,Microwave (MW),Millimeter wave (mmW),Tera-Hertz (THz) realizes capacitive sensing (measuring permittivity in terms of capacitance change, or directly measure the capacitance change) by applying interdigitated capacitors, resonators and microstrip structures [33]. Currently, since the electrochemical and electrical biosensors dominate the commercial market [1], the EM wave biosensors are becoming more and more attractive due to the benefit of low cost, miniaturized, invasive and label-free detection.

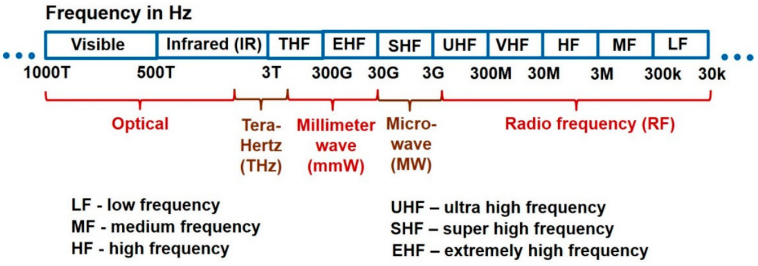

Figure 1.4: The EM spectrum showing RF, MW, mmW, THz and optical band ranges[3]

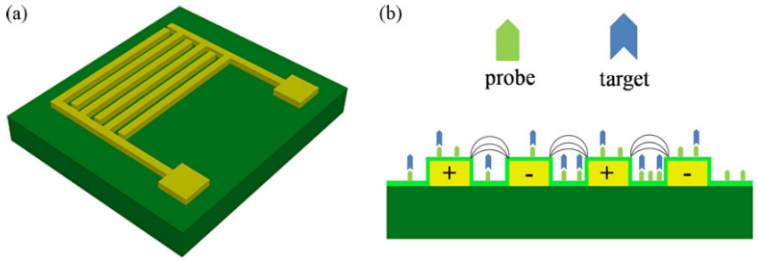

Figure 1.5: Interdigital capacitive (IDC) biosensor (a) General overview (b) Cross secition view [4]

The figure 1.5 shows the interdigital capacitive (IDC) biosensor mentioned above. The IDCs are usually fabricated on silicon and have electrode with typical length and spacing. The electrode is usually fabricated with Au, Ti, Al materials. The surface of interdigital sensor is coated with a thin passivation layer, which reduces the fareadaic current. On the surface of sensor, the probe element is attached and immobilized. When the target molecule binds with the probe element, the capacitance between the electrodes will be changed, which can be measured.

Most capacitive bio-sensors utilized the electrode-solution interface since it is rapid, simple, label free and inexpensive. The figure 1.6 depicted the detailed bio-sensing interface between the electrode and solution. The C_{ins} represents the capacitance of insulation layer, the C_{rec} represent the active functionalization layer of sensor interface, and the C_d represent the capacitance in diffusion layer (buffer solution W/ or W/O target molecules). After the biological analyte is applied, the probe element is bound with the analyte, which leads to the change of C_{rec}. The total capacitance value C_{tot} is determined by the smallest value in these three capacitors. Hence, the passivation

layer should be as small as possible to provide a high dielectric constant and larger capacitor so that the capacitance change on C_{rec} could be measured [4].

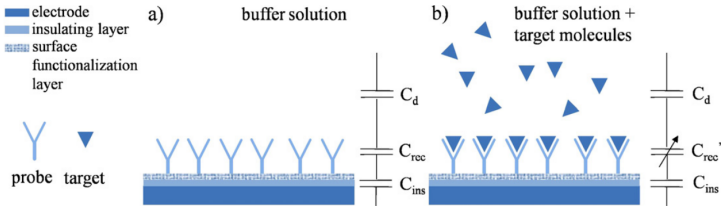

Figure 1.6: Electrode-solution interface (a) W/O target molecules (b)W/ target molecules[4]

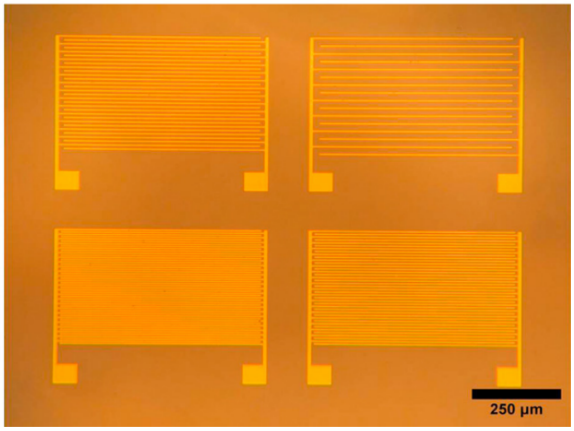

Figure 1.7: A 2-by-2 electrode array with different space[4]

The development of miniaturized microelectrode array is crucial because of the rising demand to run a large number of test concurrently and obtain precise measurement result. Moreover, the microelectrode array provides a possibility to measure multi-functionality measurement, i.e., measure different bio-analyte by the same miniaturized system. A micrograph of electrode array is presented in figure 1.7.

Base on the discussion above, the capacitive sensor can be generally classified to capacitance to voltage convertor (CVC), capacitance to frequency converter (CFC). The impedance sensing, such as triangular voltage analysis, lock-in detection, are also capable to sense capacitance because it measures the complex impedance [5]. The triangular voltage analysis and lock-in detection will be discussed briefly together with CVC and CFC sensing methods.

Table 1.1 shows the qualitative comparison between the capacitance to voltage conversion (CVC), capacitance to frequency conversion (CFC) and impedance measurement techniques. The lock-in detection is not energy efficient compared with other methods, while triangular voltage analysis needs extra wireless unit for transmission. Thus, the techniques utilized in impedance measurement is not suitable for this multi-channel measurement scenario. In the following section, the CVC and CFC based sensing system will be discussed.

1

	Capacitance to voltage (CVC)			Capacitance to frequency (CFC)				Impedance measurement	
	Charge sharing	Charge Sensitive Amplifier	CBCM	Relaxation oscillator	Ring oscillator	PLL	LC VCO	Triangular voltage analysis	Lock-in detection
Power consuption	+++	++	+	+++	+	-	++	+++	-
Complexity of circuitry	+++	++	-	+++	+	-	+++	+	-
Resolution	-	+	+++	-	+++	+++	+	+	+++
Wireless extension capability	-	-	-	-	++	+	+++	-	+
Output signal	Analog	Analog	Analog (need extra ADC)	Digital	Digital	Analog (need extra ADC)	Analog	Analog	Analog

Table 1.1: Qualitative comparison table for CFC, CVC and impedance sensing techniques

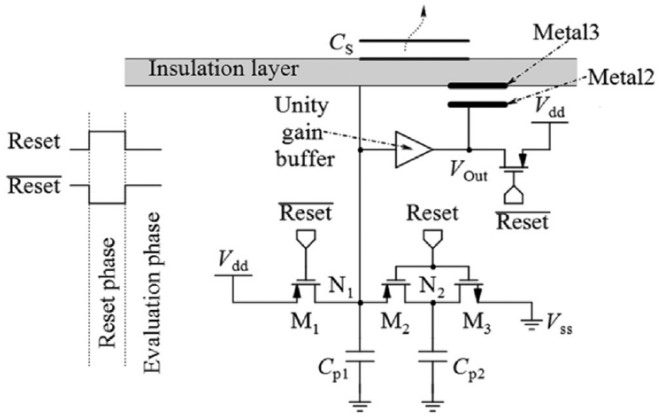

Figure 1.8: Example of charge sharing structure [5]

1.2.1. CAPACITANCE TO VOLTAGE CONVERTER (CVC)

The capacitance to voltage converter includes (1) charge sharing, (2) charge sensitive amplifier based and switched capacitor circuits (SC). (3) charge based capacitance measurement(CBCM), which will be discussed in this section.

CHARGE SHARING

Figure 1.8 shows the circuit based on charge sharing method. C_s is the capacitor under test, as well as C_{p1} and C_{p2} are parasitics of node N_1 and N_2. The circuit has two phases of operation: reset phase and evaluation phase. In the rest phase, the C_s and C_{p1} are charged to V_{dd}, and C_{p2} is charged to V_{ss}. In the evaluation phase, the stored charge is redistributed between the three capacitance. The relationship between output voltage and sensing capacitor is shown in 1.1. The

advantage of the charge sharing method is that the system is simple for implementation. However, the drawback of this kind of system is also obvious. The resolution of system is limited by the stability of V_{dd} and V_{ss}. And the leakage of transistor will also affect the limit of detection. And the sensing is strongly dependent on the measurement accuracy of the parasitic capacitance.

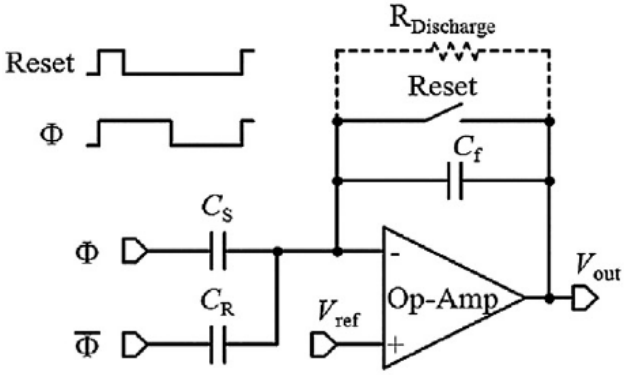

Figure 1.9: Example of charge sensitive amplifier [5]

$$V_{out} = \frac{(C_{p1} + C_S) \cdot V_{dd} + C_{p2} \cdot V_{ss}}{C_{p1} + C_{p2} + C_S} \tag{1.1}$$

CHARGE SENSITIVE AMPLIFIER

Basically, the charge sharing technique is based on the charge redistribution between the capacitance under test(C_s) and reference capacitor (in the case shown in figure 1.8 is parasitic capacitance). The charge sensitive amplifier and switched capacitor (SC) follows a similar principle [5]. Figure 1.9 shows a kind of charge sensitive amplifier. The reset switch keeps the V_{out} the same level as the reference voltage V_{ref} at the beginning of sensing. During the sensing phase, a voltage pulse is applied to C_S, and the inverse of pulse is applied to C_R. Thus, the charge is distributed between these two capacitors. The output voltage V_{out} is calculated by equation 1.2. The C_f and C_R in this diagram can be tunned, so that the output voltage level and the time constant τ can be adjusted according to the change of sensing capacitor value C_S.

$$V_{out} = V_A \frac{C_s - C_R}{C_f} \text{[34]} \tag{1.2}$$

The output signal of charge sensitive amplifier is usually a voltage level change, which can be converted to digital signal by applying an ADC such as pipeline ADC, successive-approximation register (SAR) ADC or sigma-delta ($\Sigma\Delta$) ADC [5, 35, 36]. The advantage of this technique is that the reference and feedback capacitor of the analog front amplifier can be adjusted according to different range of sensing capacitors. The analog to digital converter can therefore provide high accuracy of conversion, which improves the sensing result. However, the drawback of the system is that high-resolution ADC requires complex circuitry, and the ADC usually more power hungry

than the analog frontend. And the sensing result is strongly dependent on the accuracy of the reference capacitance and the feedback capacitor. The parasitics in the inverting port and V_{out} port of Op-amp will also affect the circuit performance, e.g. settling time during the reset phase.

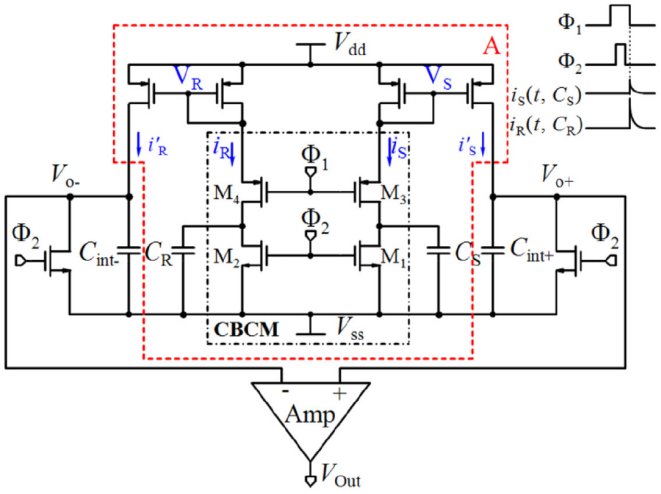

Figure 1.10: Charge based capacitance measurement [5]

CHARGE BASED CAPACITANCE MEASUREMENT (CBCM)

The charge based capacitance measurement is shown in figure 1.10. The reference capacitor C_R and sensing capacitor C_S are places left and right, respectively. The Φ_1 and Φ_2 switches are utilized to charge the discharge the two capacitors. By subtracting the current flowing through the left branch (i_R) and right branch (i_S), the difference between C_R and C_S can be calculated [5]. The design in [37] utilized a 1:N current mirror to amplify the i_R and i_S, and averaged them separately by applying two integrating capacitors. The voltage on the integrating capacitors C_{int+} and C_{int-} are then subtracted and amplified by the differential amplifier (Amp) shown in figure 1.10. This design shows high sensitivity, but limited Dynamic range because of the voltage swing limitation of the amplifier block. To address the issue, a $\Sigma\Delta$ modulator is proposed in [38] to directly convert the voltage on the integration capacitance into digital signal. The CBCM sensing method is capable to work directly with $\Sigma\Delta$ ADCs [39], amplifier [40], amplifier follower by high resolution ADC [41]. The resolution of system mainly depends on the following circuitry for calculating the current difference ($i_S - i_R$) [5].

Based on the discussion above and the qualitative discussion table shown in 1.1, the charge sharing and charge sensitive amplifier benefits from simple circuity and low power consumption. However, the resolution of these sensing methods are low. Although the CBCM method provides better resolution compared with other sensing technique, achieving low-power, small area design on chip is a difficult task. Hence, a good complexity-resolution trade-off is hard to achieve for traditional capacitive sensing system. Additionally, all the three traditional capacitance to voltage conversion are not friendly with wireless transmission extension, which means all of them requires extra wireless transmission unit. In conclusion, the conventional CVC technique is not capable of this multi-channel sensing application.

1.2.2. CAPACITANCE TO FREQUENCY CONVERTER (CFC)

Another trend of capacitive sensing is to convert the capacitance change to the frequency shift. This method contains the following structures (1) Relaxation oscillators (2) Ring oscillator based CFC (3) PLL-based CFC (4)Voltage-controlled oscillator (VCO) based CFC, which will be discussed in this section.

RELAXATION OSCILLATOR

The structure of relaxation oscillator is relatively simple. Figure 1.11 shows the relaxation oscillator utilized in [6]. The current source is charging and discharging the equivalent capacitance of C_{ox} C_{CP} and C_{elec}. When the voltage level of non-inverting input of comparator reaches the threshold voltage V_{SW}, the output is set to high. Consequently, the transistor is on, and the drain of transistor is discharged. The function of the circuit is similar to a timer, whose oscillation frequency is related to the value of capacitance under test. When the capacitance under test increases, the output frequency will decrease, since the system requires more time to charge the capacitance.

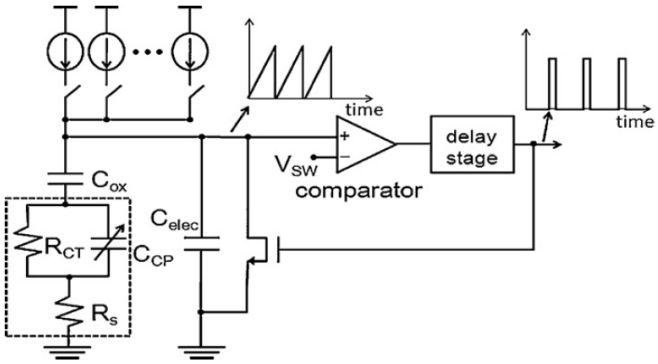

Figure 1.11: Example of relaxation oscillator [6]

The equation 1.3 shows the equation to calculate the output frequency f, where C_S is the sensing capacitor, V_{SW} is the threshold voltage, I_B is the biasing current and τ_d is the delay caused by comparator and delay stage. Neglecting the small τ_d, the frequency is inversely proportional to the sensing capacitor C_S [5].

$$f = (\frac{C_S \cdot V_{SW}}{I_B} + \tau_d)^{-1} \text{[6]} \tag{1.3}$$

The advantage of this kind of system is the simplicity of circuit structure [42, 43]. Nevertheless, the drawback of this system is the circuit needs to charge and discharge whenever running, which causes a lot of energy waste. Moreover, the hysteresis in the delay stage and comparator affects the frequency as well, and the accuracy of I_B and comparator accuracy also affect the frequency of oscillation. The uncertainty makes the structure tricky to achieve high resolution[5].

1

RING OSCILLATOR BASED CFC

The ring oscillator can be utilized as a kind of capacitor to frequency converter. The oscillation period of ring oscillator is determined by the load capacitor of each stage. Thus we could utilize this behaviour to put the sensing capacitor C_S in one of the stages. For example, figure 1.12 shows the 3 stage ring oscillator utilized in [7]. The M_7 M_8 M_9 M_10 forms the current source for every stage and each stage is designed with simple inverter.

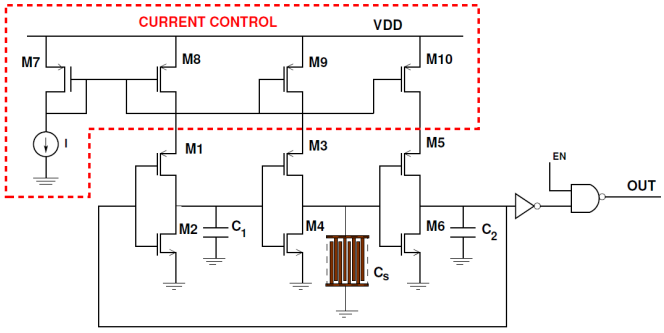

Figure 1.12: Ring oscillator utilized in [7]

Ideally, every stage is identical, thus the total period of the system is given by equation 1.4, where N is the number of stages (here N=3). C_n is the load capacitor in each stage, I is the current flowing through each stage, and V is the voltage swing in the output of each stage.

$$T = 2[\frac{(C_n + \Delta C_s) \cdot V}{I} + (N-1)\frac{C_n \cdot V}{I}][7] \tag{1.4}$$

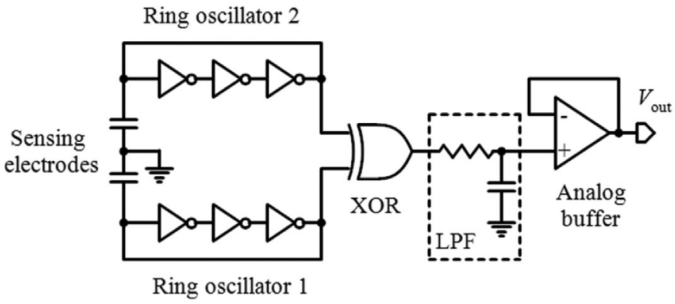

Figure 1.13: Differential ring oscillator utilized in [8]

The ring oscillator can also be utilized differentially [8], shown in figure 1.13. The XOR gate combined with a low pass filter is utilized to detect the frequency difference between the two ring

oscillator. The advantage of ring oscillator is similar to the relaxation oscillator that the output is semi-digital. Thus the system does not require extra ADC, which reduces the power consumption and the circuit complexity. Nevertheless, the drawback of the system is that the inverter on each stage is process-voltage-temperature(PVT) dependent. Therefore, each stage is not fully identical, and the oscillation period may vary from die to die [5].

LC VCO BASED CFC

The LC VCO-based sensor is capable to sense the complex permittivity change in the range of mega- to gigaHertz frequency [5]. In state of the are designs, the sensor is adapt at working in various application case. For example, Chitnis *et al.* [44] designed an ferrofluid-based LC sensor for industrial applications. Wu *et al.* [45] designed a polydimethylsiloxan (PDMS) encapsulated sensor for strain sensing. The LC sensor can also be applied in temperature sensing field[46, 47], gas sensing [48] and position sensing [49]. Focusing on biomedical application of LC sensing, various kinds of sensors are also developed. For example, Chen *et al.* [50] developed a pressure sensor made by polyamide, Cu and a microstructured styrene-butadiene-styrene (SBS) elastomer for health monitoring and critical care. A smart LC based RFID system is designed in [31] for environmental monitoring. An active 433 MHz LC sensor is designed for volatile anesthetic agent sevoflurane [51]. The operation of LC VCO based CFC sensor has two modes, namely active mode and passive mode.

Passive The passive Inductor-Capacitor(LC) sensor was firstly proposed in 1967 [52]. Until 1990's, with the development and population of micro-electro-mechanical-system (MEMS) system, more and more system utilized this kind of sensor [53]. The LC passive wireless sensor has been developed rapidly in the few decades, since it is suitable for miniaturized, remote sensing application cases. The sensor is also suitable for harsh and sealed environments, where physical contact and connection with the sensor is difficult to realize [9]. In addition, the LC sensor can be remotely powered, so no extra power source is required to be embedded with the sensor. This saves area on board and benefits for developing a small volume integrated sensor platform.

The LC passive sensor is simply composed by an inductor, a capacitor and the parasitic resistor caused by the metal path of inductor. The inductor is loosely coupled with the external read-out inductor coil.

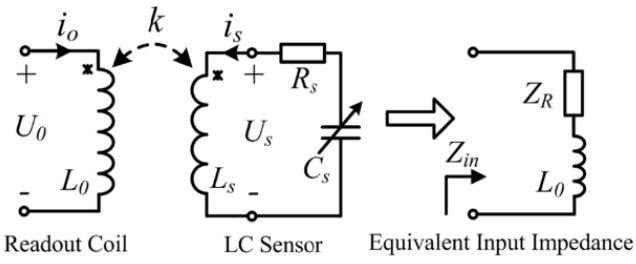

Figure 1.14: Equivalent input impedance from readout coil[9]

The inductance value L, resistance value R and capacitance value C and coupling factor k (determined by the distance between two coupling coils). All of them can be utilized as a sensing

1

variable, and measured through monitoring of the magnitude and phase spectrum in the receiver end [9]. Figure 1.14 shows the equivalent impedance looking from the readout coil. In the resonance frequency, the real part of equivalent impedance reaches the highest point, as well as the phase reaches lowest (figure 1.15). By interrogating and sweeping for the maximum real part of impedance and minimum phase, the resonance frequency can be found. This is so-called the phase dip readout method.

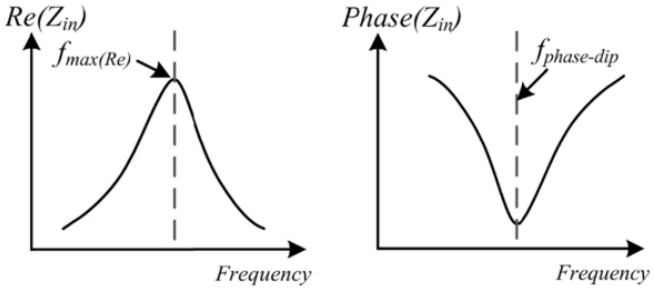

Figure 1.15: Phase dip method [9]

Active In the active mode, the change of sensing capacitor will lead to the oscillation frequency shift, which can be detected by various methods. In the VCO based sensor, the sensing capacitor is inserted to the LC tank of VCO. Figure 1.16 shows an example of LC VCO.

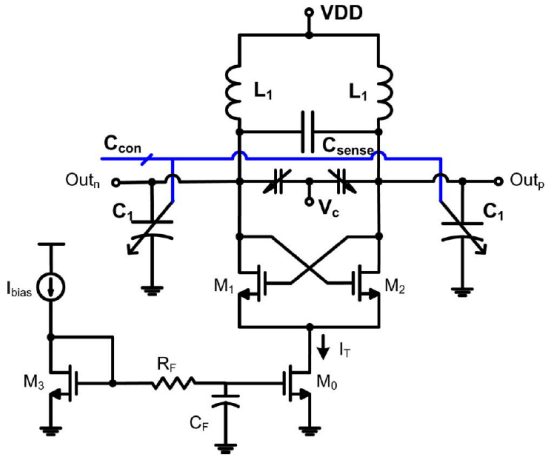

Figure 1.16: Voltage controlled oscillator embedded with sensing capacitor [10]

The relative frequency shift $\frac{\Delta f}{f_0}$ of the LC tank [54] can be expressed with respect to the relative capacitance change $\frac{\Delta C_t}{C_t}$ through equation 1.5. For small $\frac{\Delta C_t(f_0)}{C_t}$, the equation becomes 1.6. Since the equation is also the fundamental of LC VCO based sensing system, it will be further discussed in detail in chapter 2.1.

$$1+\frac{\Delta f}{f_0}=\frac{1}{\sqrt{1+\frac{\Delta C_t(f_0)}{C_t}}}\text{[54]} \tag{1.5}$$

$$\frac{\Delta f}{f_0}\approx-\frac{1}{2}\frac{\Delta C_t(f_0)}{C_t}\text{[54]} \tag{1.6}$$

Some of the design utilized the VCO itself for mmW and MW frequency dielectric relaxations detection [55, 56]. Moreover, the design of [57, 58] utilized novel in injection-locked oscillator (similar structure as VCO but different principle of sensing) for protein conformation detection and single-cell analysis. Moreover, paper [59] provides a novel method to combine the active and passive sensing in the same circuitry by bypassing the active cross-coupled pair. The drawback of the design is that the system is single channel, which is difficult to be applied in large scale measurement. In addition, the VCO is sensitive to PVT variation and drift. Thus, pre-calibration or applying a reference VCO and differentiate the output can help to improve the performance [10]. The advantage of VCO based sensor is also obvious. The circuit can realize radio frequency capacitor measurement ranges from MHz to tens of GHz range [55, 59], where some of the biological analytes behave capacitively. The power consumption is ultra low in both passive and active mode. The system does not require an extra wireless transmission unit, and the powering and measuring can be performed based on the same link.

PLL BASED SENSOR

Some of the VCO based sensor design is placed in a phase-locked loop(PLL) [10, 60], which reduces the phase noise significantly [61]. The figure 1.17 shows the fraction - N PLL utilized in [10]. With a PLL loop, the frequency output of VCO will be therefore stable. Hence, the DC tuning voltage of the system represents the sensing capacitance change, which can be read by an ADC [10].

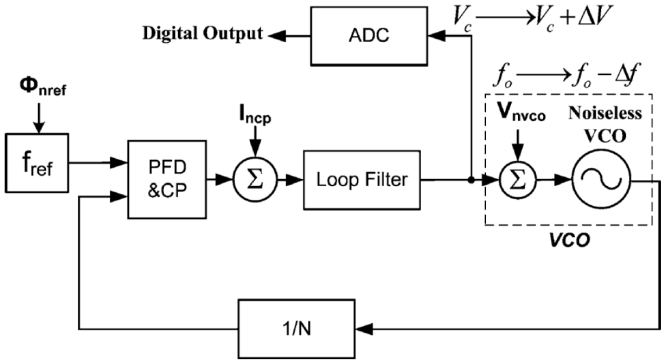

Figure 1.17: Fraction - N PLL embedded with sensing VCO[10]

If the VCO is embedded in the PLL loop, a very accurate reference frequency generator is required, and the circuit needs to be work with extra ADC, which requires more power consumption[10].

The advantage by applying the PLL is the phase noise can be reduced further, which makes the sensing system suitable for high accuracy sensing application.

The comparison table of the CFC sensing method is shown in 1.3. The resolution and dynamic range of relaxation oscillator are worst than the other sensing techniques. Although the PLL based CFC has good resolution, it requires extra ADC to work with, which increases the power consumption and area. Based on table 1.3 and 1.1, the output of ring-oscillator based CFC and VCO based CFC could be directly read as digital signal or by phase dip method. Compared with ring oscillator, the VCO based CFC can direct transmit the frequency signal, which does not require extra wireless units or blocks and provides the best wireless extension capability. Because of the good complexity - resolution balance, the VCO based LC sensor is chosen for this capacitive sensing system, which will be focused on the following design.

1.3. CHALLENGES AND SPECIFICATIONS

Based on the discussion above, LC VCO based sensing is benefit from low power, low area, wireless embedded capability and high resolution performance. Apart from the advantage of miniaturization, high quality factor, high sensitivity, however, challenges also exist in the LC VCO sensor design.

Most of publicated LC sensors are single channel, which means that most of the sensors are capable of measuring only one kind of material during each measurement. Thus there is a potential to extend the single-channel VCO to a multi-channel sensing system, which is suitable for large scale measurement scenarios.

To address the issue existing in the LC VCO based sensor [59], a multi-channel capacitance measuring system targeting for bacteria sensing(S.epidermidis) needs to be developed. How to design a multi-channel sensing system and realizing the switching between channels, is the most challenging aspect for this project. The LC VCO based sensor should have the resonance frequency in hundreds of MHz. The list of specification for design is shown in table 1.2.

Table 1.2: List of specification for the multi-channel measurement system

Number of channels	≥ 4
Oscillation frequency	400+MHz
Voltage swing	>1V
Phase noise @100k	<-85dBc/H
Integrated PN	<2% of full cycle
Linearity	R^2>90%
Power consumption	<1mW

Table 1.3: Comparison table of different Capacitance to frequency sensing techniques,TA:Total area EA:electrode area

Applications	Technology	Method	Array	Resolution	Sensitivity	IDR	Frequency range	Area	Power(Vdd)	Source
Humidity sensing	180nm	LC VCO	1	28fF	Passive 635Hz/%rh Active 1.188kHz/%rh		12-14MHz		72uW-1.44mW	[62]
DNA biodetection	65nm	LC VCO	2x2	500Hz,0.3ppm resolution	0.3ppm	>62dB	1.4/3.7GHz	0.17	5mW	[63]
Dielectric-Relaxations of Biological Water	65nm	LC VCO	1.5mm*1mm (140um*60um each)	-	2.67		60/120GHz	0.014	12.2mW@60GHz	[55]
High-Speed Flow Cytometry	65nm	LC VCO	1	5aF	1.38/1.53aF		6.5-17.5GHz (BW 250kHz)		30mW	[56]
Chemical Sensor (permittivity)	90nm	PLL	1	1.5%max error			10.4GHz	1.68*1.28	22mW	[10]
Counting of particles in laminar flow systems	130nm	PLL		60 aF out of 18fF	70 to 100 ppm (1.43 MHz)		14.3 GHz		3.3V*80mA	[64]
Chemical Permittivity Sensor	90nm	PLL	1	3.5% permittivity error			7-9GHz	2.5*2.5	16.5mW	[61]
Detection of neurotransmitter dopamine	350nm	Relaxation oscillator	5x5	-	21 kHz/fF @ 4.9 MHz @ 123 fF	12 fF-700 fF		-	-	[6]
Detection of DNA	500nm	Relaxation oscillator	8x16	-	23 Hz/pF @7.5 kHz @ 330pF	330 pF- 10 nF		28.8 (TA)	- (5 V)	[42]
Detection of cells and biomolecules (using magnetic bead detection)	350nm	Ring oscillator	8x8	2.5fF	223 kHz/fF @ 5.2 MHz @ 23 fF	-		-	-	[43]
Cell volume growth monitoring	130nm	Ring oscillator	3x4	10aF	235 mV/fF	+/- 100 fF		2.25 (TA), 1 (AA)	-	[7]
Single cell analysis	350nm	Ring oscillator	1	14aF	570 kHz/fF @ 1.37 GHz @ 500fF	-		4 (TA)	-	[65]
Bacteria detection (S.epidermidis)	250nm	Ring oscillator	1	10fF	11 kHz/fF @254 MHz @17.5 fF	-	575MHz	0.05 (AA), 0.0506 (EA)	-	[66]

2

System Architecture, Design and Modeling

This chapter introduces the top-down design from system level to transistor level, including final layout of core circuit.

2.1. System level architecture

System level block diagram The whole capacitive sensing system (shown in 2.1) has 2 parts, LC sensor end and receiver end. The design focused on the LC sensor. The core circuit is implemented by a class-B oscillator. The sensing element is implemented with differential capacitance (see C_s in the diagram). The switches are controlled by 4-to-16(9) digital decoder. There are two common capacitors between VOUTP and VOUTN shown in the left-up and right-down of the capacitance array. The core circuit is supported by trimmable current source shown as I_{BIAS}. The feed inductance is used to decouple the core circuit with the analog VDD and filter out the high frequency noise and distortion from the analog supply. The R_p is utilized to pull up and down the source and drain of NMOS switch. The micro-controller provides 4-bit digital inputs, and the 4-to-16(9) digital decoder receives the 4 bits control signal of external micro-controller. The L_{TX} in the transmitter end is also a common mode inductor between VOUTP and VOUTN, and is coupled with the L_{RX} in the receiver end with the coupling factor M. In the receiver end, the signal can be filtered out, thus oscillation frequency can be detected.

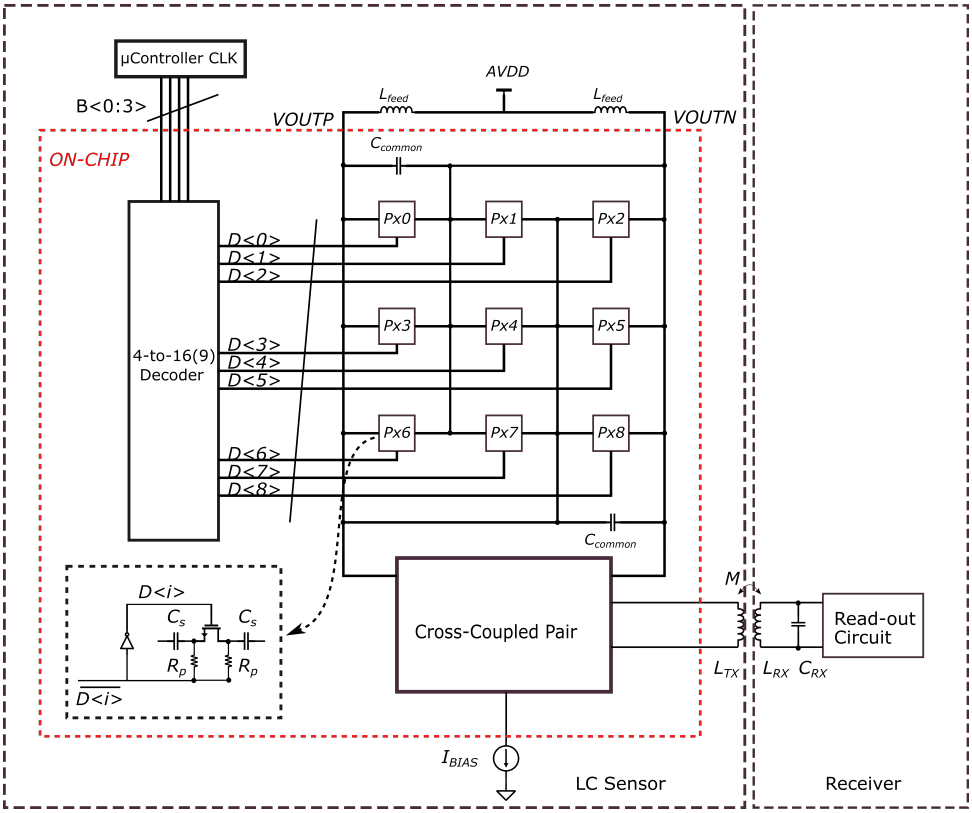

Figure 2.1: General view of the sensing system

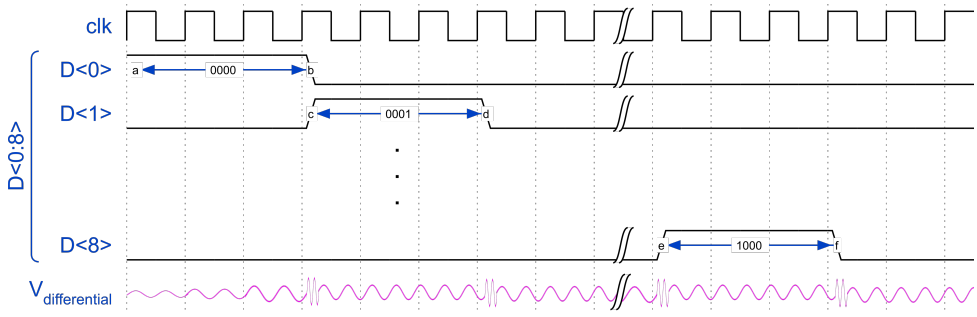

Figure 2.2: Timing sequence

Timing diagram The timing sequence is shown in figure 2.2. The clk signal represents the master clock from the external micro-controller. In the first 3 periods of the clock, channel 0 is switched on. Afterwards, channel 0 is switched off, and channel 1 is switched on. All the 9 channels are switched on successively. There is a small transition period between the on-state of 2 closed channels, where all the channels are switched off, and the system oscillates in baseline frequency

452.407MHz. After the transition time, the rest of the on-state time for each channel is utilized as a measurement time, when the signal is detected in the receiver end.

Input-output relationship The fundamental frequency of voltage-controlled oscillator is determined by the equation2.1. Since the value of inductance L is known for this design, the fundamental frequency becomes a function related only to the change of capacitance ΔC.

$$f_c = \frac{1}{2\pi\sqrt{LC}} \tag{2.1}$$

With the capacitance change, the shifted frequency is shown in equation 2.2.

$$f_c = \frac{1}{2\pi\sqrt{L(C+\Delta C)}} \tag{2.2}$$

The Taylor expansion of equation 2.3:

$$f_c = \frac{1}{2\pi\sqrt{L}} * [\sqrt{\frac{1}{C}} - \frac{1}{2}\left(\frac{1}{C}\right)^{3/2}\Delta C + \frac{3}{8}\left(\frac{1}{C}\right)^{5/2}\Delta C^2 - \frac{5}{16}\left(\frac{1}{C}\right)^{7/2}\Delta C^3 + \frac{35}{128}\left(\frac{1}{C}\right)^{9/2}\Delta C^4 - \frac{63}{256}\left(\frac{1}{C}\right)^{11/2}\Delta C^5 + O\left(\Delta C^6\right)] \tag{2.3}$$

The frequency shift is calculated by:

$$f_{c1} - f_{c2} = \frac{1}{2\pi\sqrt{LC}} - \frac{1}{2\pi\sqrt{L(C+\Delta C)}} = \frac{1}{2\pi\sqrt{LC}} * (1 - \sqrt{\frac{C}{C+\Delta C}}) \tag{2.4}$$

If the first 2 terms of Taylor expansion is taken into calculation, the frequency shift becomes:

$$f_{c1} - f_{c2} = \frac{1}{2\pi\sqrt{LC}} * \frac{\Delta C}{2C} \tag{2.5}$$

Take $C = 100$ and ΔC from 0 to 10, the $1 - \sqrt{\frac{C}{C+\Delta C}}$ and $\frac{\Delta C}{2C}$ are plotted in figure 2.3.

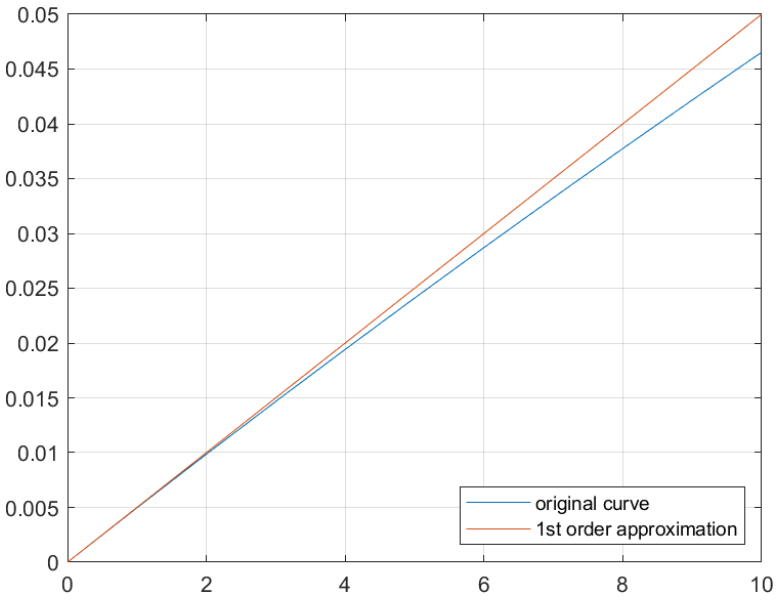

Figure 2.3: Comparing between original curve and Taylor expansion

It can be seen from the figure 2.3 that in a small amount of Capacitance change, the input-output relationship is approximately linear. If the value of C decreases, the non-linearity of input-output relationship will be more pronounced in certain amount of capacitance change. By increasing the value of C and applying this input-output relationship, the system would have a linear behaviour.

2.2. CIRCUIT-LEVEL DESIGN

The circuit-level design is based on TSMC 180nm technology. In this section, the circuit level design will be shown.

2.2.1. PIXEL DESIGN

The model of biosensor impedance can be different combinations of resistance and capacitance, depending on the applications [67]. The design is targeting at detecting the bacteria. The model shown in 2.4 elaborate the capacitance model of the Gram-positive bacteria (S. epidermidis was), and the result can be extended to Gram-negative bacteria (e.g. Escherichia coli) because the outer membranes of Gram-negative bacteria have the same dielectric properties and thicknesses with plasma membranes [11, 68]. E stands for electrolyte, I stands for insulator and M stands for metal. The following model is based on the data provided in table 1 and 2 of [11].

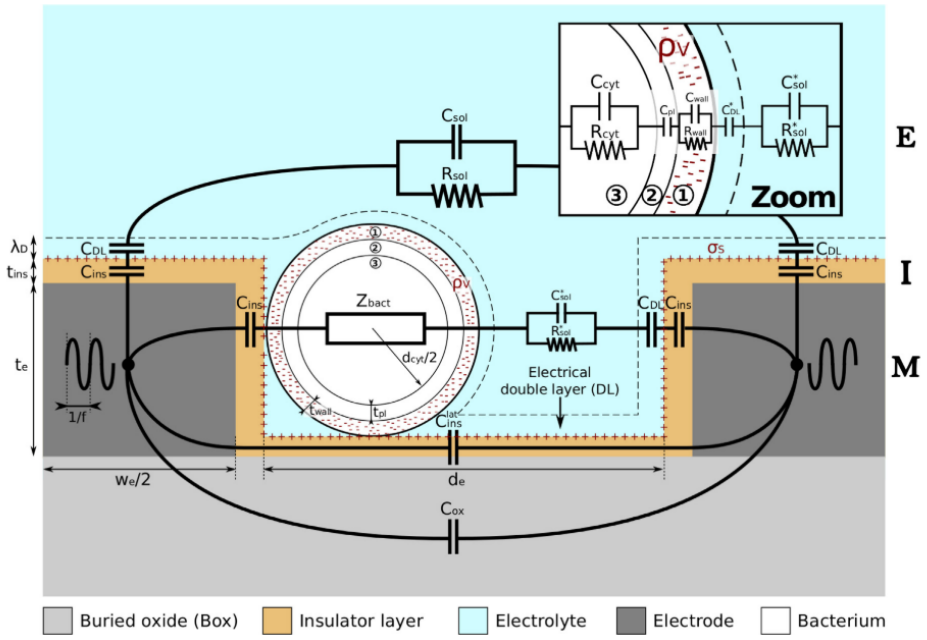

Figure 2.4: Sensor interface modelling [11]

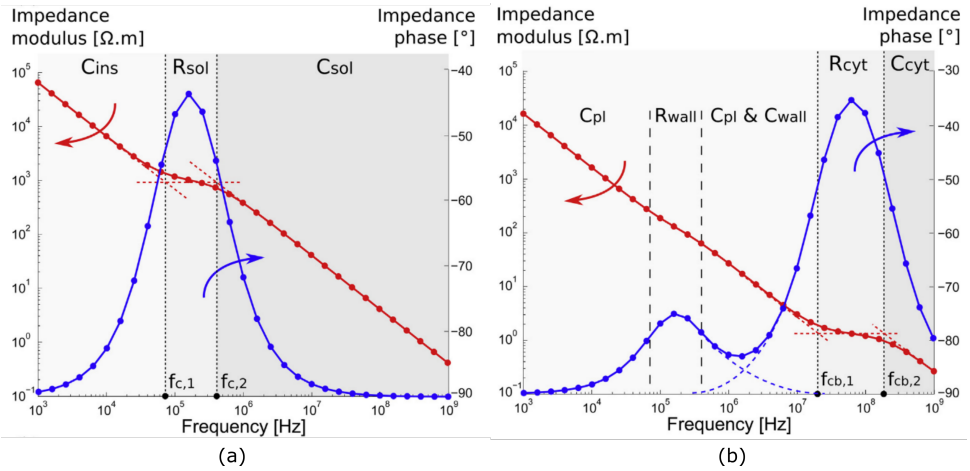

Figure 2.5: Impedance and phase of bacteria sensing [11]

The impedance and phase of bacteria are shown in figure 2.5. Above 100 MHz frequency, the whole sensor interface behaves capacitively. Thus, the operating frequency is suitable for the application of sensor.

Figure 2.6 shows the frequency shift modelled by MATLAB. The detailed code is commented and put into appendix. Assuming the inductance applied to the system is 50 µH, the series resistance of inductor is 10 Ω and the capacitance of protein is 1 fF, the resonance frequency before and after applying the capacitance is $368.255 - 368.205 = 0.05 MHz$. That means per 1fF capacitance change will result in 50kHz resonance frequency shift.

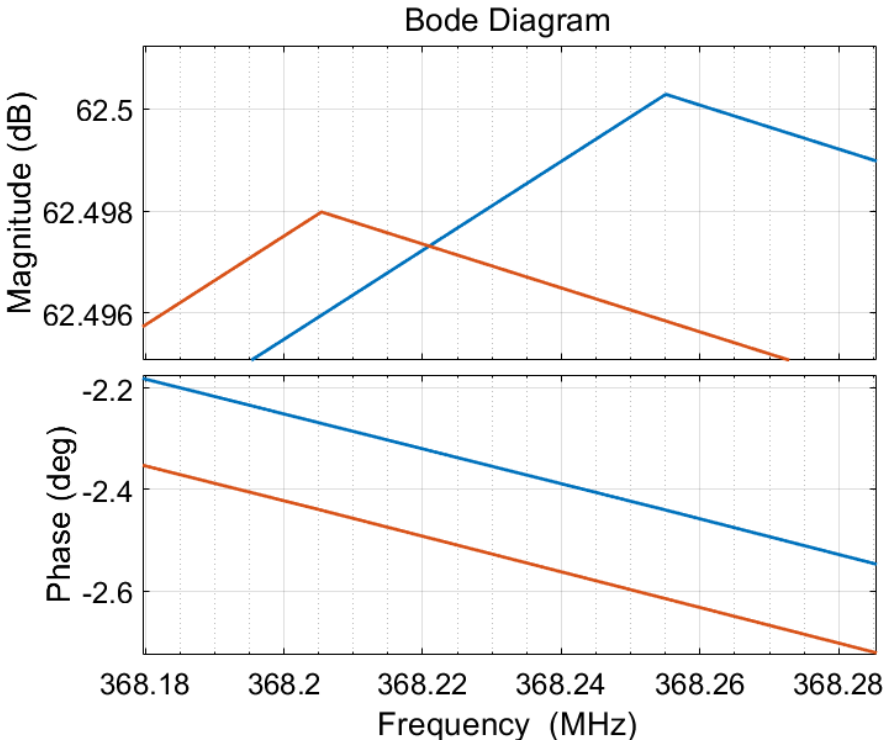

Figure 2.6: Frequency shift modelled by MATLAB

In real case sensing scenario, the interdigitated sensing capacitance is usually embedded on the top metal of sensor 2.7. For the design in [12], the material of top metal (M5) is composed by Al 99.5%/Cu 0.5%, which is different from standard CMOS process. Thus for designing the pixel, knowing the real value of interdigitated capacitance is essential.

For the TSMC miniASIC process, the minimum spacing between two metal is 1.5 µm, and the minimum width for metal is also 1.5 µm. By applying minimum spacing between two metals, the metal capacitance density can be maximized. Thus the top metal is designed to be $10.5\,\mu m * 10.5\,\mu m$. By doing post-layout extraction, the value of top metal capacitance is about 15fF. The capacitance value is indeed very small, which makes the channel extremely sensitive to the parasitics of switches. Thus customized interdigitated capacitance is also designed on metal 1-5 (below metal 6) to increase the capacitance value. The customized capacitance is shown in figure 2.8. The total capacitance of metal 1 to 6 is 100fF based on post-extraction. Thus, in schematic simulation, C_S is designed to be 100fF.

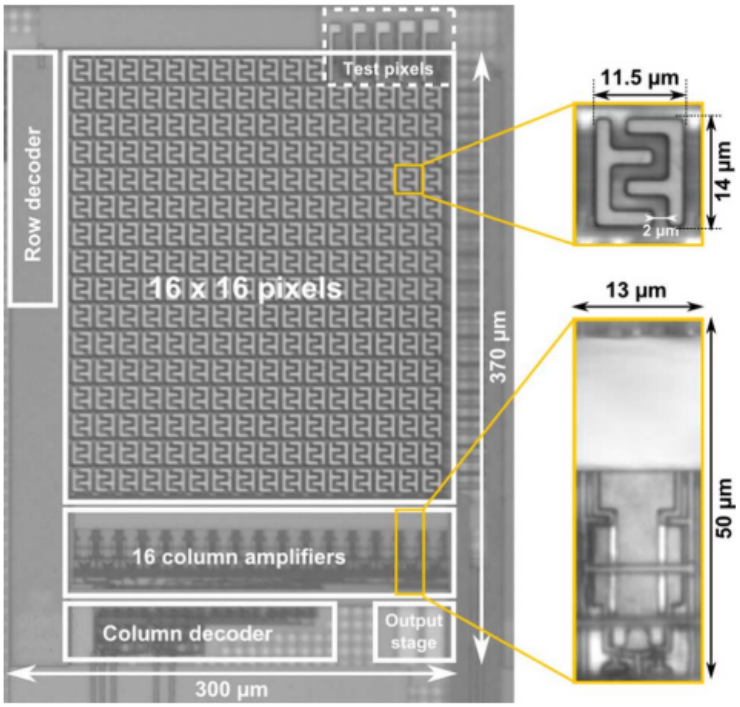

Figure 2.7: Interdigitated capacitance in real case simulation [12]

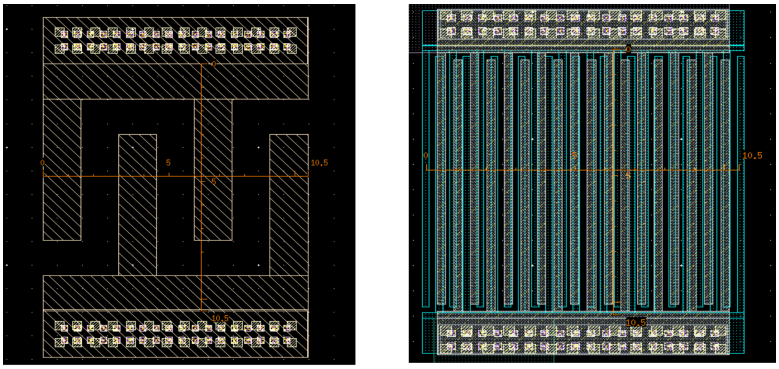

Figure 2.8: Customized Interdigitated capacitance in TSMC 180nm technology (a) Metal 6 capacitance (b) Metal 1-5 capacitance

Another very significant part of the pixel is the switching. Equation 2.6 shows the equation of drain current I_D in triode region, from equation 2.6, the on-resistance of switch can be derived and shown in 2.7. The on-resistance is inversely proportional to the width of switch. To realize small on-resistance, the width of switch should be wider. However, increasing the width of switch also

increases the parasitic capacitance of both sides of switches [69]. Thus the trade-off exists in the design of switches. The switch utilized $\frac{360\,\text{nm}}{180\,\text{nm}}$ as size of unit finger. For designing the switch, the on resistance R_{on} and parasitic capacitance C_{par} vs number of fingers, shown in figure 2.9. The left vertical axis is the number of resistance, while the right vertical is the number of capacitance. The horizontal axis is the number of fingers. The red line represents the parasitics, and the brown line represents the on-resistance. As it is shown in figure 2.9, the on-resistance reaches 85 Ω when the number of fingers = 30. After the number of fingers reaches 20, the on-resistance not decrease significantly. In order to have smaller parasitics of switches, the number of fingers is chosen to be 20. As a result, the total parameter of switch is designed to be $\frac{7.2\,\mu\text{m}}{180\,\text{nm}}$.

$$I_D = \beta_{\text{eff}} \frac{\text{W}}{\text{L}} \left(V_{GS} - V_{TH}\right) V_{DS} \propto \frac{\text{W}}{L} \text{[69]} \tag{2.6}$$

$$R_{on} = \frac{1}{\beta_{\text{eff}} \frac{W}{L} \left(V_{GS} - V_{TH}\right)} \propto \frac{L}{W} \text{[69]} \tag{2.7}$$

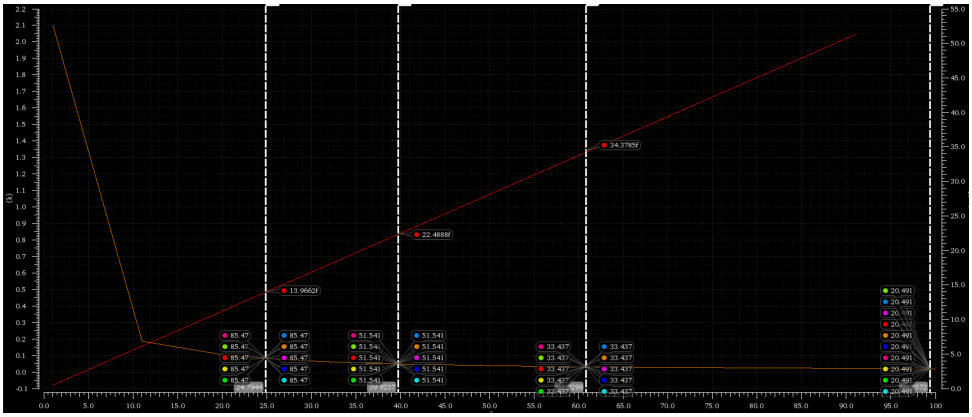

Figure 2.9: On resistance and Parasitics VS number of fingers

The resistance R_p for isolating the bias of switch and the signal path should be large enough. Thus 20 kΩ is chosen as the value. To realize the 20 kΩ resistance in layout, several kinds of resistance are compared in 2.10. The high resistance poly (HRI) resistance has the largest sheet resistance compared with other kinds of resistance, so the area of resistance layout can be reduced. Thus the HRI is chosen to realize the 20 kΩ resistance.

Apart from the single pixel design, the common capacitor C_{common} design is also significant. After post-layout extraction, all the metal of connection will have parasitics to the ground. The single-ended capacitance to the ground can be transferred to an equivalent double-ended capacitance. The estimated single-ended capacitance to ground is around 100 fF. In case of the extension in future, the common capacitor is designed to be 300 fF, which is realized by the MOM capacitor between two output nodes.

PROCESS PARAMETERS	N+	P+	POLY	N+BLK	PLY+BLK	M1	M2	UNITS
Sheet Resistance	6.6	7.5	7.7	61.0	317.1	0.08	0.08	ohms/sq
Contact Resistance	10.1	10.6	9.3				4.18	ohms
Gate Oxide Thickness	40							angstrom

PROCESS PARAMETERS	M3	POLY_HRI	M4	M5	M6	N_W	UNITS
Sheet Resistance	0.08	991.5	0.08	0.08	0.01	941	ohms/sq
Contact Resistance	8.97		14.09	18.84	21.44		ohms

COMMENTS: BLK is silicide block.

Figure 2.10: Sheet resistance comparison

2.2.2. DESIGN CORE CIRCUIT

In this chapter, the design of core circuit will be discussed. Based on the design of pixel capacitor C_S and common capacitor C_{common} and the central oscillation frequency above 400 MHz, the inductor L_{TX} is chosen to be 300 nH with 10 Ω parasitic resistance (for on-chip inductance, 10 Ω is a reasonable value and for off-chip resistance, the parasitic resistance can be even less). The L_{feed} is chosen to be 15 µH each, with 15 Ω series parasitic resistance each (again, real-life case should be better than this prediction). The L_{feed} is utilized to decoupling the high frequency signal from the DC path.

The design of oscillator should satisfy the Barkhausen stability criterion: $(g_m R_p)^2 \geq 1$. Real case design usually follows $(g_m R_p)^2 >> 1$, so that the oscillator is able to work in different fabrication corners. The cross-couple pair is designed with the size $\frac{72\,\mu m}{180\,nm}$.

The single-ended voltage swing of Class B oscillator is calculated by 2.8, where I_{ss} is the supplying current and R_p is the equivalent parallel resistance of LC tank. The voltage swing should be greater than 1V in case of the attenuation in the wireless link, so the supply current is designed to be 300 µA.

$$V_p = \frac{2}{\pi} I_{ss} R_p \text{[70]} \tag{2.8}$$

Consider the channel length modulation, the drain current of transistor can be written as 2.9. For the equation, it can be derived as $\frac{\partial I_D}{\partial V_{DS}} \propto \frac{\lambda}{L} \propto \frac{1}{L^2}$ To minimize the secondary effect and keep the current stable, the length of transistor M2 and M3 are chosen 2 µm. The width of transistor are chosen as 100 µm and 10 µm separately to realize 1:10 current mirror. The external current source is chosen to be 30 µA.

$$I_D = \frac{1}{2}\beta_{\text{eff}} \frac{W}{L} \left(V_{GS} - V_{TH}\right)^2 \left(1 + \lambda V_{DS}\right), where \lambda \propto \frac{1}{L} \text{[69]} \tag{2.9}$$

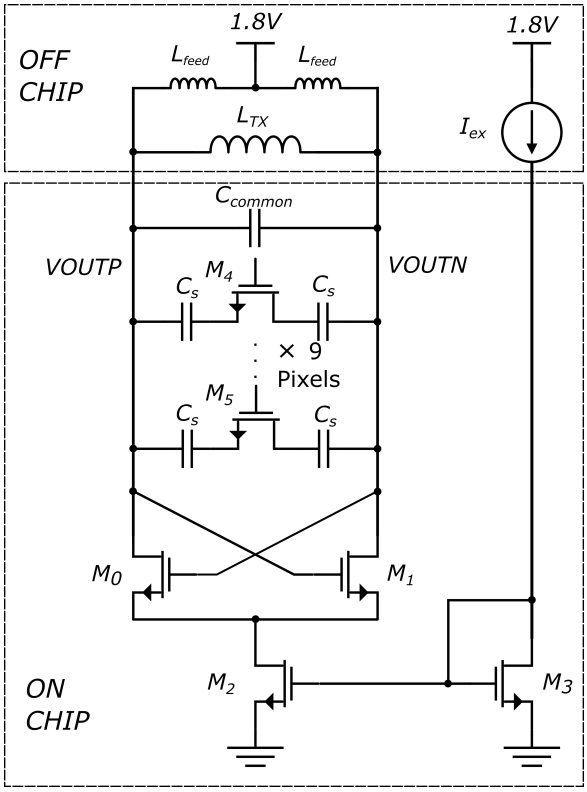

Figure 2.11: Core circuit

$M_{0,1}$	**72μ /0.18μ**
M_2	**100μ/2μ**
M_3	**10μ/2μ**
$M_{4,5}$	**7.2μ/0.18μ**

Table 2.1: Table of device dimensions

Figure 2.11 shows the core circuit of the system. The M_0 and M_1 are the cross-coupled pair of the class-B oscillator. The M_2, M_3 and external current source represent the I_{BIAS} in the system diagram (figure 2.11). The C_s is the differential sensing capacitor in the pixel. The M_4 and M_5 are the switches for the 9 channels. C_{common} represent the common capacitor between VOUTP and VOUTN. The L_{TX} represent the inductor coupled with the receiver end. The L_{feed} is the decoupling inductors for power supply, which decouples high frequency noise from V_{dd}. Table 2.1 shows the dimension of the design.

2.2.3. DECODER

The figure 2.12 shows the circuit of the decoder. The 4 digital inputs are received from the external micro-controller. The 4 bits $D<0:3>$ input is decoded to switching signal of 9 channels.

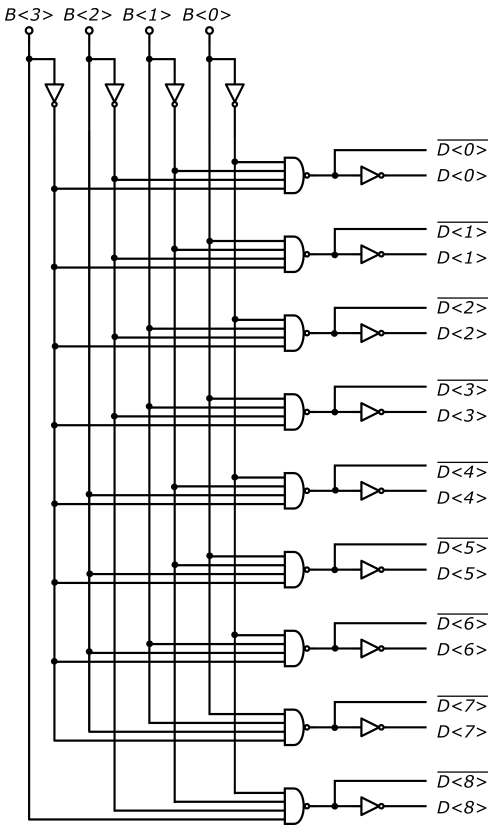

Figure 2.12: 3-to-9 Digital decoder circuit

2.3. LAYOUT

The layout is completed based on common-centroid layout technique, where all the capacitance has the same environment surrounded by them. Figure 2.13 shows the layout of the core circuit, where part A is the layout of a pixel, part B is the common MOM capacitor between VOUTP and VOUN, part C is the cross-coupled pair and part D is the current source. The parts E to H represent the ports. The left top grey path E is the port VOUTP, and the right top grey path F is the port VOUTN. Part G is the digital input ports. Part H is the ports of I_{BIAS} and GND.

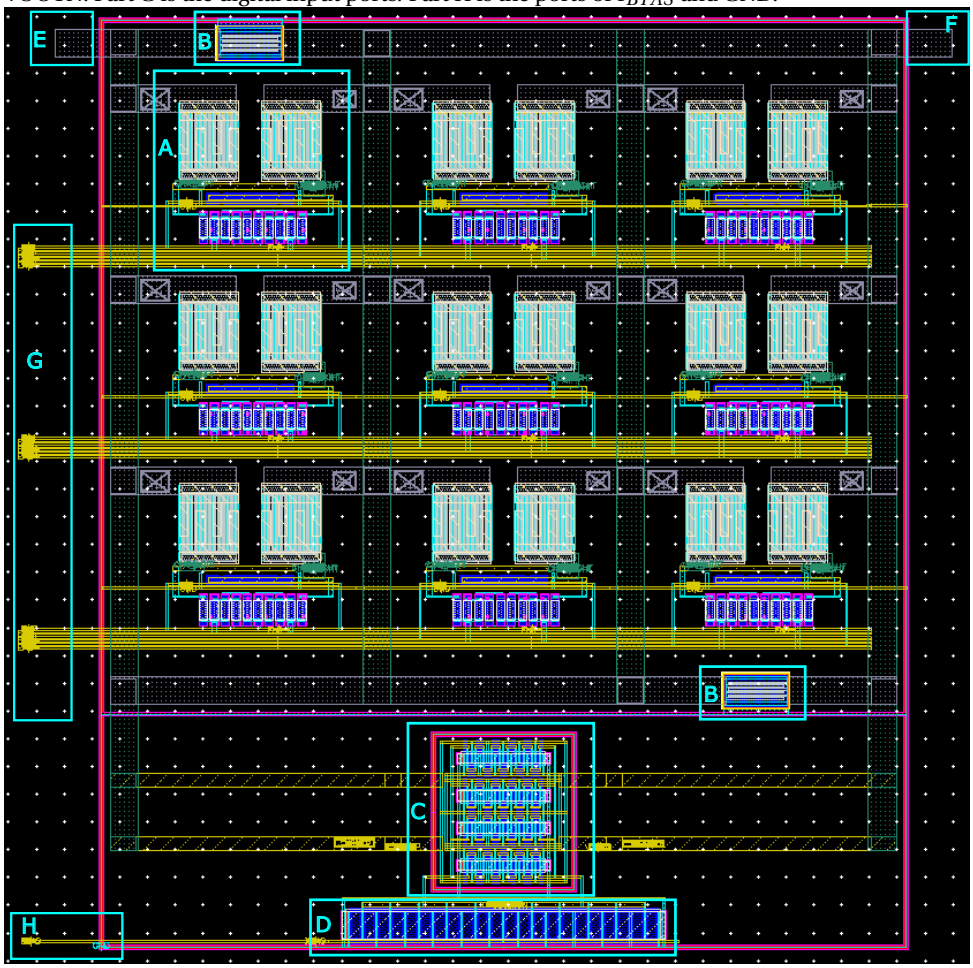

Figure 2.13: Layout or the core circuit

The zoomed view of pixel layout (part A of figure 2.13) is shown in figure 2.14. As it is shown in figure 2.14, part A_1 and A_2 are two customized interdigitated capacitance utilized by Metal 1 to Metal 6. Part B is the switch between two capacitance. Part C is the two pulling up/down resistances, utilized by the high resistance poly. Part D is the digital signal path for controlling switches.

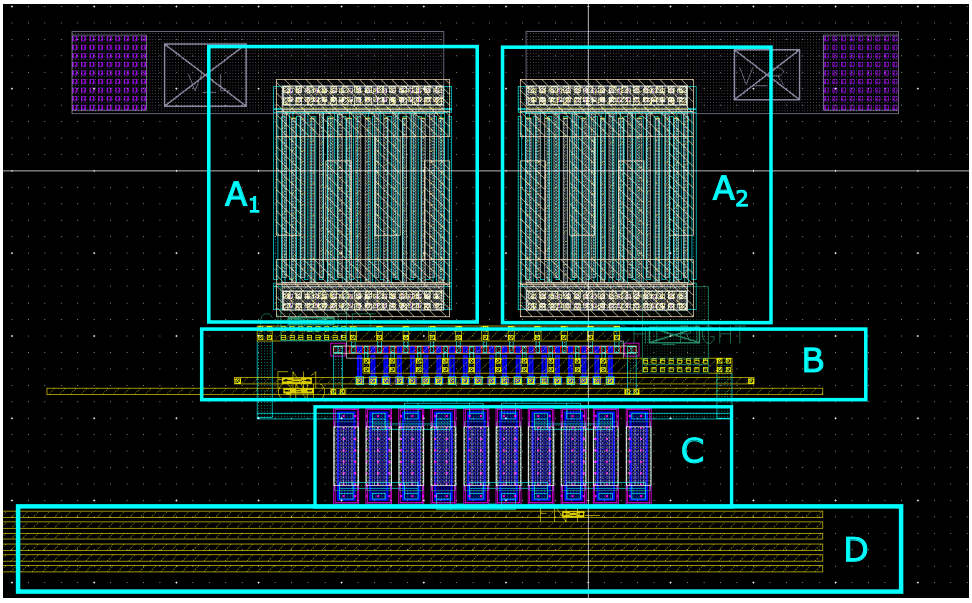

Figure 2.14: Layout of the pixel

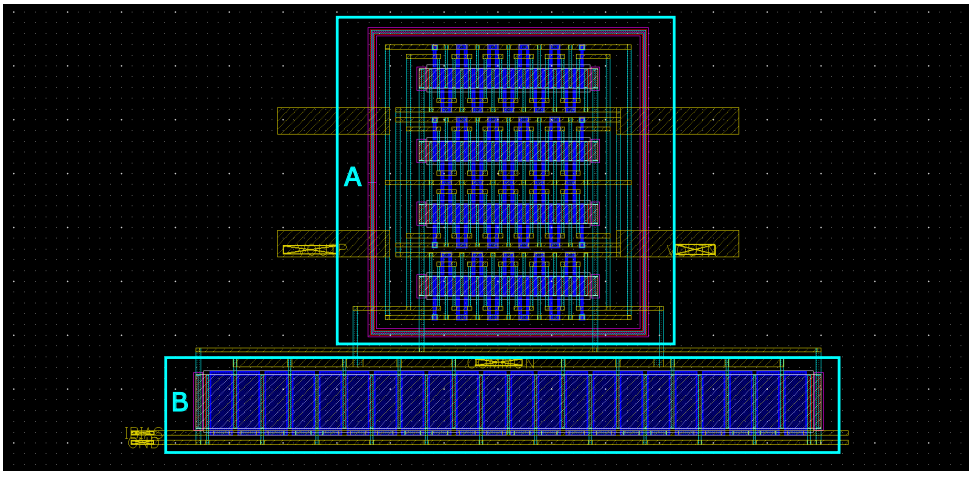

Figure 2.15: Layout of cross-coupled pair and current source

The zoomed view of pixel layout (part C and D of figure 2.13) is shown in figure 2.15. The cross-coupled pair is layouted with common-centroid view, by which the transistor is less affected by the fabrication gradient.

3

RESULTS

In this chapter, the simulated results of the circuit will be shown, including the nominal corner transient, harmonic balance simulation, process-voltage-temperature (PVT) corner simulation, Monte Carlo simulation and post-layout simulation. For classifying the simulation, a list of terms utilized in the simulation is shown below.

3.1. TYPICAL CORNER SIMULATION

The typical corner simulation is running at the following condition: V_{dd} = 1.8V, I_{bias} = 30µA, T = 37°C, capacitance of each channel $C_{left} = C_{right}$ = 100fF, common capacitor between V_{outp} and V_{outn}: 300fF, no C_{test} is applied to the parallel of C_{left} and C_{right}. C_{test} is the parallel capacitance applyed to sensing capacitor C_S, which represent the capacitance change of C_S.

The figure 3.1 shows the transient simulation of the differential output with one channel switched on. The baseline frequency of measurement system is 452.407 MHz (all channels switched off). The oscillation becomes stable after 80ns. The FFT(fast Fourier transform) of the signal shows that the fundamental frequency (one channel is on, no C_{test} applied) of oscillation is 424.49 MHz with 604.72mdB magnitude. The fundamental frequency of FFT is 1.773MHz different from the HB simulation fundamental frequency (426.263MHz), because the transient simulation and HB simulation in Cadence used different simulation engine.

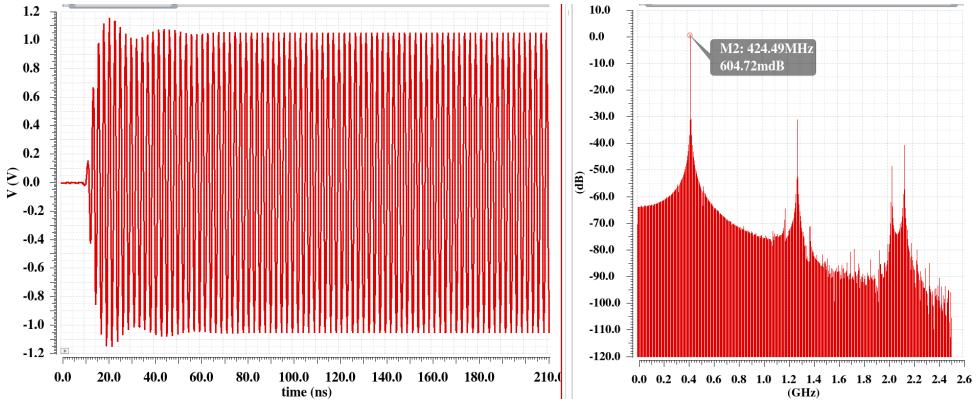

Figure 3.1: Transient simulation and FFT of oscillator with one channel switched on (0-200ns)

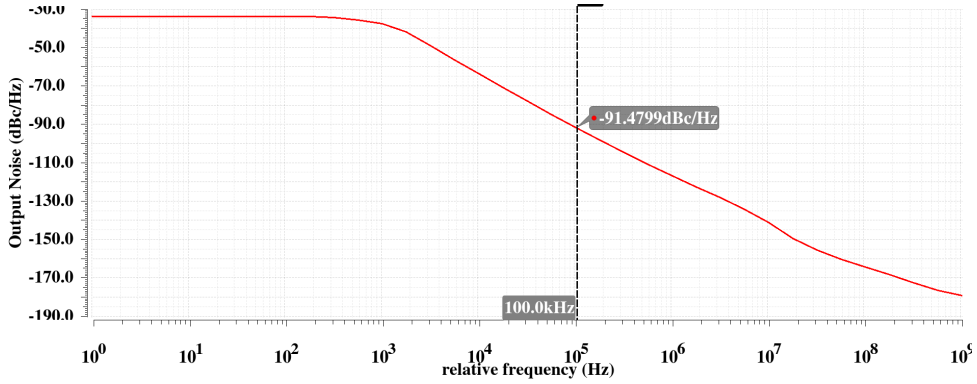

Figure 3.2: Schematic simulation Phase noise vs Relative frequency

The phase noise simulation is shown in figure 3.2. The phase noise reaches -91.4799dBc/Hz @100kHz away from the fundamental frequency. The equation 3.1 shows the relationship between phase noise spectrum $L(f)$ and the RMS jitter per cycle. Particularly in the project, the RMS jitter from fundamental frequency f_0 to $2f_0$ is focused. The equation 3.2 shows how to calculate the jitter in particular spectrum. $J_{per-cycle}$ represent the jitter per cycle.

$$J_{per-cycle} = \frac{1}{2\pi f_c}\sqrt{\theta^2(t)}J_{per} = \frac{1}{2\pi f_c}\sqrt{2\int_0^{\infty} 10^{\frac{L(f)}{10}}\,df} \tag{3.1}$$

$$J_{per-cycle|f_1 to f_2} = \frac{1}{2\pi f_c}\sqrt{2\int_{f_1}^{f_2} 10^{\frac{L(f)}{10}}\,df} \tag{3.2}$$

From the embedded calculator in Cadence Virtuoso software, the integration of phase noise spectrum is calculated from 10 kHz to $2f_0$ as following: $\int_{f_1}^{f_2} 10^{\frac{L(f)}{10}}\,df = 3.263E-3$. The complete calculation of phase noise is shown in equation 3.3.

$$J_{per-cycle|10\text{kHz to }2f_0} = \frac{1}{2\pi f_c}\sqrt{2\int_{f_1}^{f_2} 10^{\frac{L(f)}{10}}\,df} = 30.160\,\text{ps} \tag{3.3}$$

The fundamental frequency from HB simulation is 426.3 MHz. Thus, the period of signal is $\frac{1}{426.3\,\text{MHz}} = 2.35\,\text{ns}$. The complete equation to calculate the percentage of RMS jitter to full cycle is shown in equation 3.4.

$$\text{jitter to the full cycle} = \frac{\text{jitter}}{T_0} = 30.160\,\text{ps} * 426.3\,\text{MHz} * 100\% = 1.286\% \tag{3.4}$$

3.2. CORNER SIMULATIONS

Figure 3.3 shows the input-output relationship in different process corners, namely 'tt','ss','ff','sf' and 'fs' corners. The 'tt' represents the typical corner. The first letter represents the behaviour of NMOS, while the second letter represents the behaviour of PMOS. 'f' represent fast as well as 's' represent slow. In the fast fabrication corners, the transistors have smaller threshold voltage V_{th}, thus the switching and conduction become faster and easier. The transistor behaviour of 's' corner is the contrary of 'f' corner. In different corners, the C_{test} is swept from 0 to 100 fF. For the process corner simulation, all the other circuit parameter setting is the same as the condition shown in 3.1. The fitting curve in all the corners is shown. Only original data points of tt corner are drawn in the green line, whereas the other original data points are not drawn. The C_{test} represents the equivalent differential capacitance change of each pixel, which is half of the capacitance change of the two sensors on the pixel. The coefficient of determination (R^2 value) in tt corner is 0.99768, which represent that the measurement system has high linearity. The responsivity of the system in tt corner is 0.338, which means every 100fF effective capacitor change can result in 33.8 MHz frequency shift.

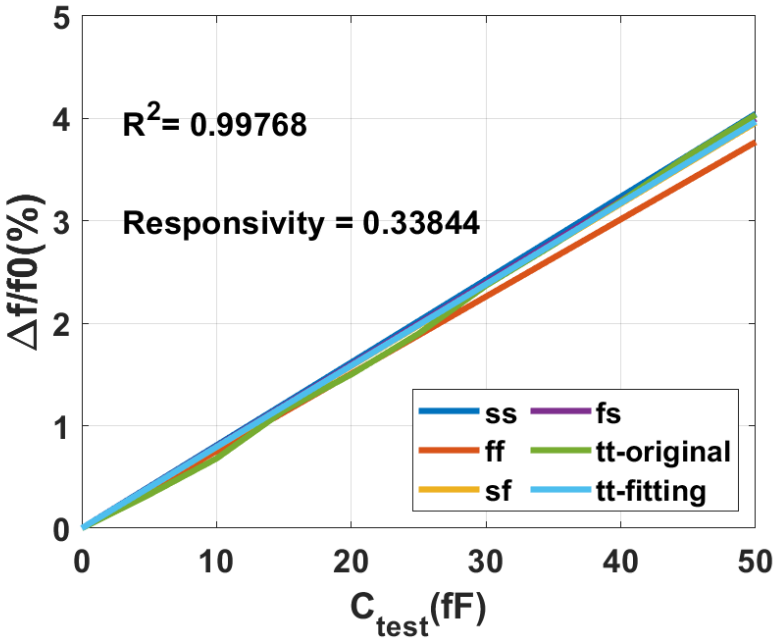

Figure 3.3: Input-output relationship fitting curve in different corners

Table 3.1 shows the rest of the input-output fitting parameters which is not shown in 3.3. It can be seen that the R^2 value in every corner is higher than 99.7, which means the input-output relationship is highly linear correlated. The responsivity of the system is around 0.34 MHz/fF in all the corners except for the ff corner, which means every 100fF capacitance change will lead to 34MHz frequency shift. In the ff corner, the system respond a little bit slower with 0.32 MHz/fF responsivity.

	tt	**ss**	**ff**	**sf**	**fs**
R^2	0.99768	0.99948	0.99532	0.9975	0.99887
Responsivity (MHz/fF)	0.3384	0.3459	0.3199	0.3381	0.3404

Table 3.1: Input-output relationship fitting parameters in different corners

Table 3.2 shows the circuit performance is different process corners. The fundamental frequency in tt corner is 426.3MHz. The Δf_{max} is 3.3 MHz between ss and ff corner, which represents that in worst fabrication case, the fundamental frequency will have 3.3 MHz difference from chip to chip. Thus, calibration needs to be performed for each chip before measurement to trim the frequency offset. From the third row of the table, it can be seen that the peak voltage V_{peak} is around 1.05 V

in tt, sf and fs corners. The worst case happens between ss and ff corners as well, where the peak voltage V_{peak} has 0.271 V difference. The peak voltage level affects the power transferred to the receiver end. Thus when applying the design to the application, a trimmable current source needs to be utilized to take care of the voltage level shift between different chips.

	tt	ss	ff	sf	fs	Δfmax
Oscillation frequency (MHz)	426.3	427.6	424.3	427	425.8	3.3
Vpeak	1.049	1.181	0.910	1.056	1.044	
Phase noise area from 10k to 2f0	3.263E-3	3.493E-3	2.32E-3	3.447E-3	3.033E-3	
RMS Phase noise(ps)	30.160	31.110	25.551	30.948	29.112	
% full cycle (one σ)	1.286%	1.330%	1.084%	1.321%	1.240%	

Table 3.2: Circuit performance in different fabrication corners (37°C,Vdd=1.8V)

The table 3.3 shows the circuit performance in different temperature corners. The rest of simulation settings is the same as the condition shown in 3.1. The oscillation frequency varies 0.237 MHz, and the peak voltage V_{peak} varies 0.016 V between different temperatures. Since the measurement system is utilized for bio-analyte measurement and the body temperature is 37 °C, the temperature should not varies much in the measurement time.

	27°C	**37°C**	**47°C**
Oscillation frequency (MHz)	426.146	426.263	426.026
Vpeak	1.058	1.049	1.042

Table 3.3: Circuit performance in different temperature corners (tt corner, Vdd=1.8V)

The table 3.4 shows the circuit performance in different supply voltages. The rest of simulation settings is the same as the condition shown in 3.1. The oscillation frequency varies 2.4 MHz, and the peak voltage V_{peak} varies 0.013 V between ±10% variation of power supply V_{DD}. It can be seen that the circuit is very sensitive to supply fluctuation. Thus, stable power supply needs to be utilized in test bench of system.

	1.62V(-10%)	**1.8V**	**1.98(+10%)**
Oscillation frequency (MHz)	425	426.3	427.4
Vpeak	1.043	1.049	1.056

Table 3.4: Circuit performance in different supply voltages (tt corner, 37°C)

3.3. MONTE CARLO SIMULATION

The figure 3.4 shows the Monte Carlo simulation of the system. 200 runs of test are performed with process variation. The rest of simulation settings is the same as the condition shown in 3.1. It can be seen from the figure that the mean value of fundamental frequency is 429.252 MHz with 1.79 MHz standard deviation σ, which means the fabricated chip has 68% probability to oscillate within the range 429.252 MHz $\pm$ 1.79 MHz. The fundamental frequency will be in the range of 429.252 MHz $\pm$ 5.37 MHz with 3 σ variation, which means the fundamental frequency of fabricated chip has 99.7% probability to stay within that range.

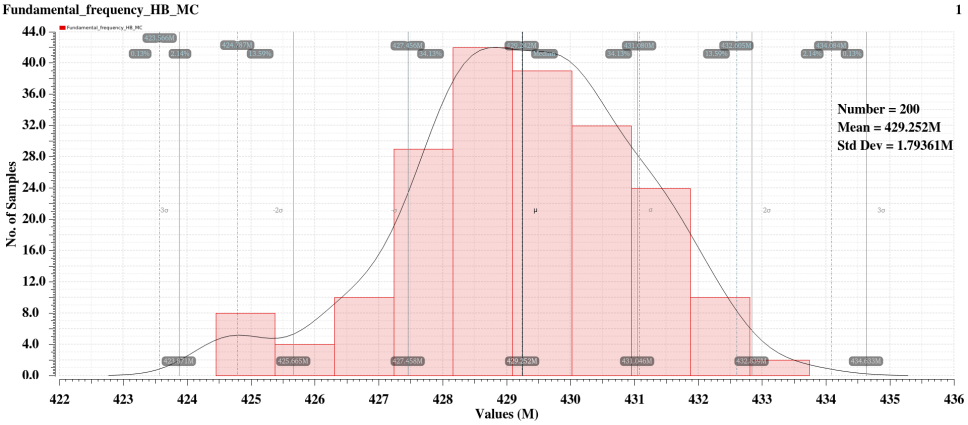

Figure 3.4: Monte Carlo process simulation of the fundamental frequency

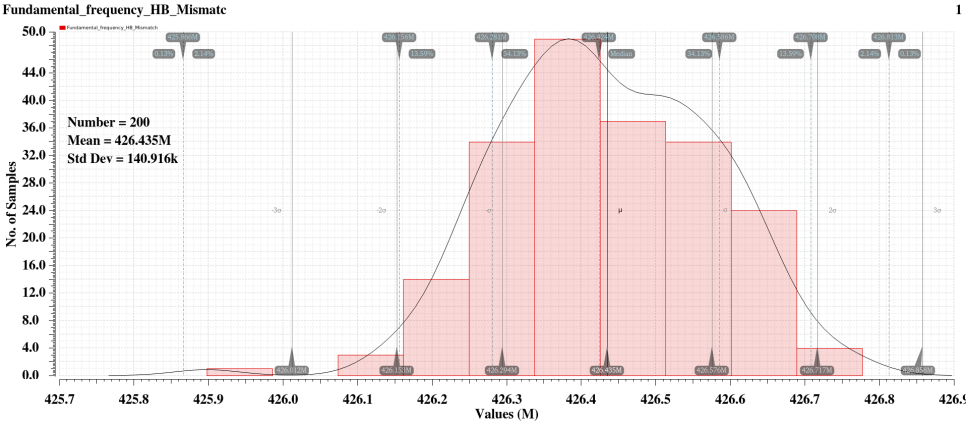

Figure 3.5: Monte Carlo mismatch simulation of the fundamental frequency

Ideally, the mean value of fundamental frequency should be closed to the number of typical corner

(tt corner) simulation results, and the mean value ± standard deviation (σ) should be closed to the results of corner simulations. However, the mean value of fundamental frequency is 3 MHz larger than the typical corner simulation result. This is either because the model library script (.scs file) in the 180nm technology has a certain error, or the Monte Carlo process variation circle is outside the process corner variation range in this technology.

The figure 3.5 shows the Monte Carlo mismatch simulation of the system. 200 runs of test are performed with mismatch of transistors. The rest of simulation settings is the same as the condition shown in 3.1. As it is shown in the figure 3.5, the fundamental frequency is 426.435 MHz with only 140.9 kHz variation (1 σ deviation). The fundamental frequency will be sitting in the range of 426.435 MHz ± 420 kHz (3 σ deviation), which means that the mismatch of transistor affects very little of the fundamental frequency.

	No mismatch	Local mismatch (10%)	Global mismatch(10%)
Fundamental frequency	426.263MHz	426.41MHz	426.47MHz

Table 3.5: Fundamental frequency in different mismatch of resistance

Since the model library script (.scs file) does not include the mismatch data of resistor, the effect of resistor mismatch is manually tested based on the simulation condition shown in typical corner 3.1. The results are shown in table 3.5. The ±10% local mismatch is tested with a 18 kΩ left biasing resistance and 22 kΩ right biasing resistance of the on-state channel. The 10% global mismatch is tested with 20 kΩ resistance in the on-state channel and 18 kΩ resistance in an off-state channel. As a result, the worst case resistance mismatch only contributes to 200kHz fundamental frequency shift, which is lower compared with the frequency shift caused by the corner variation.

In conclusion, the influence of process variation is more significant than the influence of resistance and transistor mismatch in terms of fundamental frequency.

3.4. POST-LAYOUT SIMULATION

The post-layout simulation is running at the following condition: V_{dd} = 1.8V, I_{bias} = 30µA, T = 37°C, capacitance of each channel C_{left}, C_{right} and common capacitor between V_{outp} and V_{outn} are all extracted capacitance.

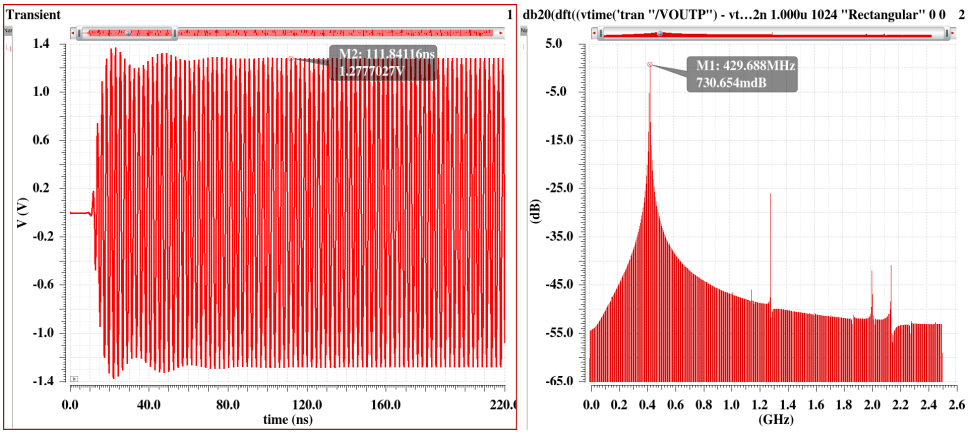

Figure 3.6: Transient post-layout simulation (0-200ns)

Figure 3.6 shows the post-layout transient simulation and the FFT plot. The peak voltage is 1.277 V and the fundamental frequency is 429.688 MHz.

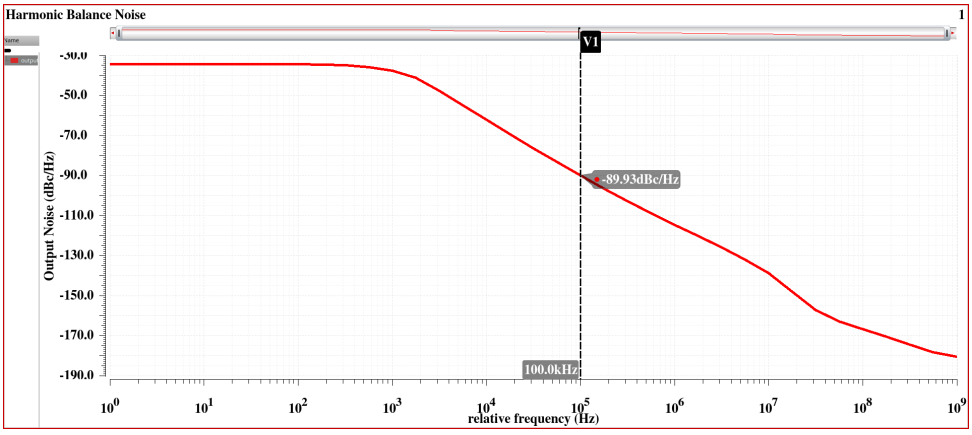

Figure 3.7: Post-layout phase noise simulation

Figure 3.7 shows the post-layout the phase noise simulation. The phase noise reaches −89.93 dBc/Hz @ 100 kHz.

Table 3.6 shows the comparison table between schematic simulation and post-layout simulation. The peak voltage increases from 1.049 V to 1.277 V, whereas the phase noise get larger from −91.48 dBc/Hz to −89.93 dBc/Hz. The RMS phase noise increases from 30.16 ps to 34.983 ps. However, the RMS phase noise still remains in the 1.6% of the oscillation period.

	Oscillation frequency (MHz)	Vp(V)	Phase noise @100k (dBc/Hz)	Integrated Phase noise (ps)	% of the full cycle
Schematic	426.263	1.049	-91.4799	30.160	1.286%
Post-layout	429.413	1.277	-89.93	34.981	1.502%

Table 3.6: Pre-post layout Simulation comparison table

For the system performance simulation, the C_{test} is swept from 0 to 100 fF. Figure 3.8 shows the system performance comparison between schematic simulation and post-layout simulation. As it is shown in the figure, the responsivity of post-layout simulation is $0.41751-0.33844 \approx 0.08$ MHz/fF higher than the responsivity of the schematic simulation, which means the system is more sensitive to per fF capacitance change.

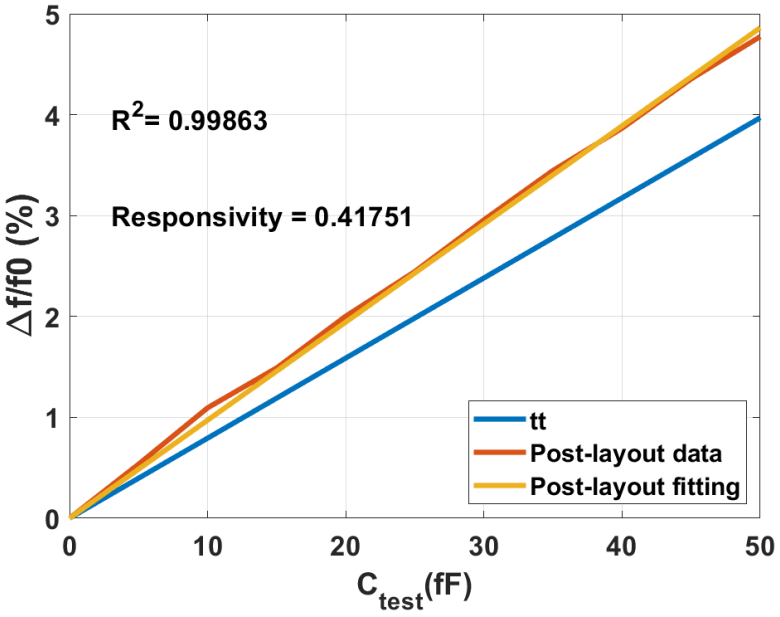

Figure 3.8: Post-layout simulation system

The result of figure 3.8 is generated under the condition in which only the capacitance of the on-state channel is changed. When the capacitance in all the channels are changed, the linearity of system is getting worse. As it is shown in the figure 3.9, the R^2 value of system fitting curve is decreased to 0.817 when the capacitance in the off-state channel is changed corresponding to the on-state channel capacitance change. The result indicates that if the sensor interface is sensitive to the same bio-analyte, the off-state channel capacitance will also change during measurement time, which lead to non-linearity of the system performance. The effect of off-state channel is caused by the leakage of current in the off-state channel. The switches are not completely switched off during the on-state channel measurement time, thus the off-state channel capacitance change still contributes to the frequency shift. This can be solved in future work by increasing the width of NMOS switches and increasing the value of switch biasing resistance (both of them increase the off-state channel resistance). An alternative solution is to limit the measurement dynamic range to make the system perform linearly in a small measurement range. Another possible reason of leakage is the layout of switches. The left part and right part of switches are closed to each other in the layout, thus a relatively small capacitance exists between the left and right part of each switch,

which causes the high frequency leakage. Thus, the layout of switches can be improved by bringing the left metal and right metal of switches more apart.

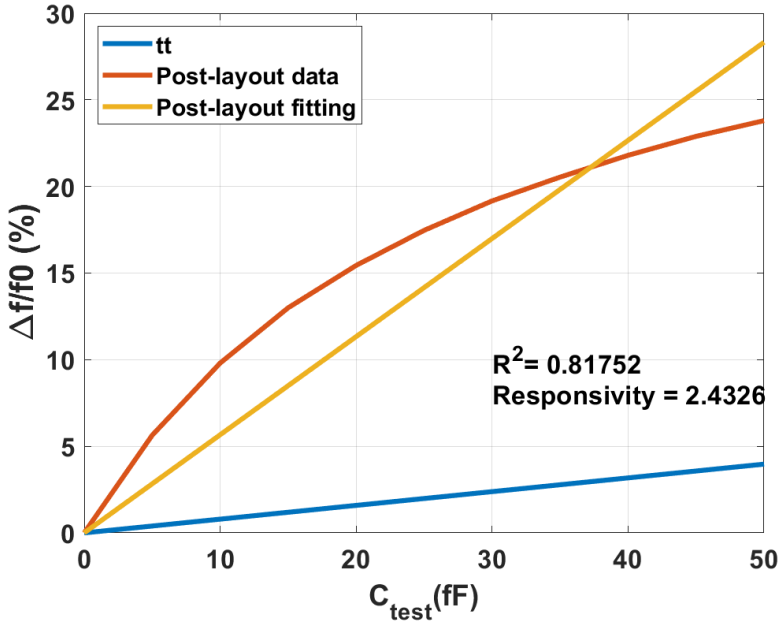

Figure 3.9: Post-layout simulation system

The table 3.7 shows the comparison between the schematic simulation and post-layout simulation. As it is shown in the table, the post-layout simulation verifies the schematic design when the capacitance is changed in one channel. But the post-layout circuit is sensitive to the capacitance change of the off-state channels.

	R^2	Responsivity(MHz/fF)
Schematic	0.99768	0.33844
Post-layout-1 Channel	0.99863	0.41751
Post-layout-all Channel	0.81752	2.4326

Table 3.7: Pre-post layout system performance comparison table

4

DISCUSSION

The bio-sensing is developed rapidly because of the rising demand of the point-of-care, diagnostic of disease, etc. Among all the topics of bio-sensing, capacitive sensing plays an important role. This work follows the top-down approach. By analysing and comparing the different capacitive bio-sensing techniques, the LC VCO based sensing technique shows the advantage of low-power, low-area, high sensitivity, high resolution and wireless transmission capability. Thus, this work focuses on developing and improving the LC VCO based capacitive sensing techniques, targeting at developing a multi-channel LC VCO based bacteria sensing system.

This work is based on TSMC 180nm technology. As the system is targeting at bacteria sensing, the fundamental frequency is designed to be 430 MHz, and the fundamental frequency can be tuned by replacing the off-chip capacitor. The system is designed based on Class B oscillator, with the tuning capacitance bank replaced with the sensing capacitor array. Two feed inductances are coupled with external inductance for power and information transfer. The system utilized the top metal (metal 6) as the interdigitated sensing capacitance, so that the system does not require further electrodes fabrication. The transient simulation and the corner simulation shows that the circuit oscillates in 426 MHz fundamental frequency, with less than 1.5% RMS phase noise. The layout of circuit is based on common centroid layout techniques, the 3-by-3 capacitance array is centrosymmetric. The post-layout simulation result verifies the schematic design and meets the table of specification shown in 1.2. The drawback of circuit is that the circuit is sensitive to the leakage of off-state channel switches, which means that the cross-sensitivity needs to be improved by improving the layout of design or separate the target analyte of electrodes.

Table 4.1 shows the comparison table between this work and the state-of-the-art CFC designs. The potential resolution based on this technique is comparable with the sub-GHz bio-sensing applications (detection of cells, biomolecules[65] and bacteria [66]). Furthermore, the total area required for this technique is smaller than that in [42] and [65]. In addition, the potential sensitivity of the VCO based design is higher than that of relaxation oscillator [6]. This design shows higher resolution and sensitivity because capacitance change directly results in a frequency shift in LC sensor, and this design utilized more advanced nodes than the design shown in [6, 7, 42, 66]. Furthermore, the power consumption is of this design is far lower than the design shown in [6, 7, 42, 66]. The PLL for permittivity detection [61] is designed in 90nm technology, targeting to the 7-9 GHz frequency. By comparison, the phase noise of VCO utilized in PLL [61] is -105 dBc/Hz @ 500kHz

frequency offset, which is comparable with this design (-90 dBc/Hz @ 100kHz). However, the PLL reduce the effect of phase noise effectively, which make the resolution of design [61] limited by the quantization noise of ADC. The power consumption of this work is lower than [61]. The area of this work is also smaller, because fewer blocks are needed in LC VCO based CFC. In addition, this work is multi-channel design, which provides a potential for sensing different analytes and doing large scale analysis. The VCO based LC sensing in [55] is utilized for multi-channel mm-wave frequency dielectric relaxations of biological water detection. Design in[55] utilized separate cross-coupled pair, base-line capacitor, inductor on each sensing element. Although the measured phase noise is -80dBc/Hz @ 1MHz and the phase noise higher than this work, comparing directly based on phase noise is not adequate, since the circuit suffers more from parasitics and mutual inductance in mm-wave frequency. In addition, the area consumed by the [55] is less than this work, whilst the design in [55] consumes more power. Overall, the design in [55] provides guidance of doing EM simulation, dielectric property simulation, multi-channel configuration and measurement setup, which could be potentially utilized in this design.

Table 4.1: Comparison table between this work and other capacitive sensing method

Applications	**Technology**	**Method**	**Array**	**Resolution**	**Sensitivity**	**IDR**	**Frequency range**	**Area (mm^2)**	**Power[mW] (V_{dd})**	**Source**
Detection of neuro-transmitter dopamine*	0.35 um	CFC by Rel.O	5×5	-	21 kHz/fF @ 4.9 MHz @123fF	12fF-700 fF	-	-	-	[6]
Detection of DNA*	0.5 um	CFC by Rel.O	8×16	-	23Hz/pF @7.5 kHz @330pF	330pF-10nF	-	28.8 (TA)	- (5 V)	[42]
Detection of cells and biomolecules (using magnetic bead detection)*	0.35um	CFC by RO	8×8	2.5fF	223kHz/fF @5.2 MHz @23 fF	-	0.7-1.4GHz	-	-	[43]
Bacteria detection (S.epidermidis)*	0.25um	CFC by RO	1	10fF	11 kHz/fF @ 254 MHz @17.5 fF	-	Up to 575 MHz	0.05(AA), 0.0506 (EA)	29@2.5V, 250kS/s	[66]
Chemical permittivity detection*	90nm	CFC by PLL	1	Permittivity error <3.5%		-	7-9GHz	2.5*2.5(AA)	16.5	[61]
Dielectric Relaxations of Biological Water*	65nm	CFC by VCO	12×16 @120GHz 8×16 @60GHz	-	2.87ppm @120GHz, 2.67ppm @60GHz	-	60GHz, 120GHz	0.014 @120GHz, 0.008 @60GHz (AA)	34.8mW @120GHz 12.2mW @60GHz	[55]
Bacteria detection	0.18um	CFC by VCO	3×3	15.5fF	417kHz/fF @ 430MHz	100fF	Up to 430MHz post-layout	0.025 (AA, total analog)	0.54(Active)	**This work****

CFC: Capacitance to frequency conversion, Rel.O: Relaxation oscillator, RO: Ring oscillator, VCO: Voltage-controlled oscillator, PLL: Phase-locked loop, IDR: Input dynamic range *Measured on chip **Simulated in post-layout simulation, AA:Active area, EA:Electrode(s) area, TA: Total area, V_{dd}: Supply voltage

5

CONCLUSION AND FUTURE WORK

In conclusion, this work presents a 3-by-3 LC VCO based array targeting bacteria sensing in 400 MHz frequency. The circuit has low power (0.54 mW) and small area (0.025 mm^2) characterization, with 417kHz/fF sensitivity and more than 99% linearity in single-channel post-layout simulation. The simulated circuit performance shows the potential for increasing the number of channels for further applications. This work provides a multi-channel structure and layout for sub-GHz frequency bio-capacitance sensing applications.

List contributions

- In the field of LC sensing - provide a novel multi-channel LC sensor structure and layout with active transmission mode
- In the field of capacitance to frequency converter - developed the active multi-channel LC VCO for low power, low cost, miniaturized capacitance to frequency sensing technique
- In the field of (bio-)capacitive sensing - provide a wireless multi-channel LC VCO based capacitve sensing method for bacteria sensing or similar capacitive bio-analyte in the frequency range of few hundereds MHz
- In the field of bio-sensing sensing - provided a wireless sensing technique which is capable to measure the concentration of bacteria

There are still some aspects that could be improved for the design. Firstly, the chip can be improved by integrating an integrated on-chip inductor. For the sensor part, developing a high responsivity and high linearity sensor interface between chip and bio-analyte is essential as well. For developing a multi-functional system, different kinds of electrodes need to be designed. The cross-sensitivity between each channel can be reduced by rearranging the layout. In real-life measurement, the biological capacitance also varies during measurement due to the activity of bio-analyte. Thus pre-calibration and trimming need to be done between the measurement of each channel. A varactor can be applied to the circuit so that the center frequency can be tuned not only by replacing inductors. In future, the whole link can be designed, so that the powering and information transmission can be both realized by applying the same link.

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A

APPENDIX

A.1. IMPEDANCE MEASUREMENT TECHNIQUES

TRIANGULAR VOLTAGE ANALYSIS (IMPEDANCE)

The triangular voltage analysis is utilized for impedance measurement. A pulse or triangular voltage signal is generated and applied to the impedance under test. By measuring the output peak value and slope, the resistance and capacitance can be calculated [71, 72]. Compared with lock-in detection (will be discussing in A.1), the setup of triangular voltage analysis is relatively simple. However, the accuracy of detection is limited by the voltage reference generator, which requires further complex circuitry[71].

LOCK-IN DETECTION (IMPEDANCE)

The lock-in detection is usually utilized for measuring impedance spectroscopy rather than capacitive sensing. The priciple of lock-in detection is similar with the IQ modulation utilized in radio frequency communications. Figure A.1 shows the architecture of lock-in detection utilized in [13]. The original signal generated by the frequency synthesizer is synchronous demodulated and low-pass filtered [13, 73].

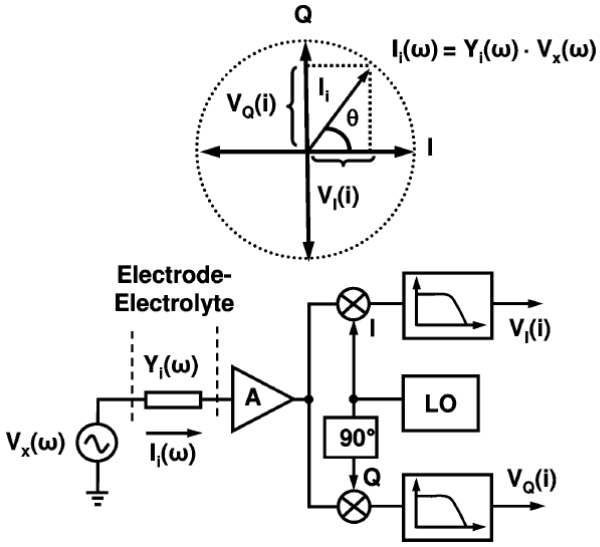

Figure A.1: Architecture of lock-in detection[13]

The low-pass filtered dc value of I and Q channel can be used to calculate the amplitude and phase of admittance by equation A.1 and A.2.

$$\left|Y_i(\omega)\right| = \frac{\sqrt{V_I^2(i) + V_Q^2(i)}}{A \cdot |V_x(\omega)|} \text{[13]} \tag{A.1}$$

$$\angle Y_i(\omega) = \tan^{-1}\left(\frac{V_Q(i)}{V_I(i)}\right) \text{[13]} \tag{A.2}$$

The advantage of this kind of system is high accuracy and capability of impedance measurement. However, the system requires very high accuracy local oscillator, which requires more complex circuitry and higher cost. Otherwise, the system would suffer from synchronization and mismatch errors2 [74].

A.2. MATLAB CODE

```
% %% Analyzing the Frequency Response of the Circuit
% % The Bode plot is a convenient tool for investigating the
% % bandpass characteristics of the RLC network. Use |tf| to
% % specify the circuit's transfer function for the values
% %|R=L=C=1|:
% clear
% clc
% L = 10^-6;
% RL = 10;
% C_before = 10^-12;
% RC = 1;
% C_after = 2*10^-12;
%
% w_res  = 1/sqrt(L*C_before)
% Q_Cseriesbefore = 1/(w_res*C_before*RC)
% Q_Lseries = L*w_res/RL
% Q_Cseriesafter = 1/(w_res*C_after*RC)
%
% % figure (1)
% sys_before=tf([L*C_before*RC (C_before*RL*RC+L) RL],[L*C_before C_before*(RL+RC) 1]);
% bode(sys_before);grid on
% hold on
%
% % figure (2)
% sys_after=tf([L*C_after*RC (C_after*RL*RC+L) RL],[L*C_after C_after*(RL+RC) 1]);
% bode(sys_after);grid on
%
% %h = bodeplot(tf([L*C_before*RC (C_before*RL*RC+L) RL],[L*C_before C_before*(RL+RC) 1]));
grid
%
%
```

```
% %% Modeling the sensor parameters
% clear
% clc
%
% syms C_ins C_DL Epsilon_0 Epsilon_rins Epsilon_rsol t_ins N_e A_e Lambda_D k_B T q N_av C_ions
% syms k
% syms t_e w_e L_e
% syms C_sol G_sol d_e G Sigma_sol
% syms C_ox C_latins
%
%
% Epsilon_0=8.854187817*10^-12; %vacuum constant
% Epsilon_rsol=80;       %from paper
% k_B=1.38*10^-23;       %thermal constant
% q=0.19*10^-18;         %from paper
% N_av=6.02*10^23;       %from paper
% C_ions=0.16*10^-3;     %from paper
% T=300;                 %room temperature
%
%
% t_ins=33*10^-9;        %from paper
% Epsilon_rins=9;        %from paper
%
% t_e=1*10^-6;           %from paper,electrode parameter
% w_e=2*10^-6;           %from paper,electrode parameter
% L_e=250*10^-6;         %from paper,electrode parameter
% A_e=(t_e+w_e/2)*L_e;   %from paper,electrode parameter
% N_e=39;                %from paper,electrode parameter
%
%
% %%%%%%%%%%%%%%Calculate Lambda_D %%%%%%%%%%%%%%
```

```
% Lambda_D=sqrt(Epsilon_0*Epsilon_rsol*k_B*T/(2*q^2*N_av*C_ions*10^3));
%
% %%%%%%%%%%%%%%Calculate C_DL/C_ins %%%%%%%%%%%%%%
%
% k =(t_ins/Lambda_D)*(Epsilon_rsol/Epsilon_rins); %C_DL/C_ins=14(from paper)?even larger when Cion increase
%
% %%%%%%%%%%%%%%Calculate C_ins & C_DL%%%%%%%%%%%%%%
%
% C_ins= (Epsilon_0*Epsilon_rins)/t_ins*(N_e-1)*A_e  %from paper
% C_DL= k*C_ins                              %from paper
%
% %%%%%%%%%%%%%% C_sol & G_sol  %%%%%%%%%%%%%%
%
% d_e=4*10^-6;                               %from paper table
% G=1.28;                                    %from paper p431
% Sigma_sol=1.8*10^-3;                       %from paper ?
% C_sol = (Epsilon_0*Epsilon_rsol)/d_e*(N_e-1)*A_e*G %from paper
% G_sol = Sigma_sol/d_e*(N_e-1)*A_e*G              %from paper
% R_sol=1/G_sol
% %%%%%%%%%%%%%% C_ox  %%%%%%%%%%%%%% C_ox is parallel
% C_ox=0.03*C_sol
% C_latins=C_ox/20.5
%
% %% Modelling Csol Rsol CDL Cins
%
% clear
% clc
% syms s
%
% C_ins = 4.5881e-11
```

```
% C_DL  = 6.5539e-10

% C_sol = 4.3067e-12

% G_sol = 1.0944e-05

% C_ox  = 1.2920e-13

% C_latins = 6.3025e-15

% R_sol=1/G_sol

%

% Z_up = 2*1/(s*C_DL)+2*1/(s*C_ins)+[R_sol/(s*C_sol)]/[1/(s*C_sol)+R_sol]

% % = 2*1/(s*C_ins)+1/(s*C_DL)+1/(s*C_DNA)+[R_msol/(s*C_msol)]/[1/(s*C_msol)+R_msol]

% Z_low=1/(s*C_ox)

%

% Z_eq =simplifyFraction(Z_up,'Expand',true)

%
sys_before=tf([2100406951821989555924141185539905679630169373583218349928483220139100078089282141010003843722392365705945216876298947014551592815169124261627774541758464],[753268735614853357901663332904186675499943338794337339321224865191417397138620193130308439995294594746905070517446306663049054912512001]);

% bode(sys_before);grid on

%

% % Z_eq =simplifyFraction(1/(1/Z_up + 1/Z_low + 1/(s*C_latins)),'Expand',true)

% %
sys_before=tf([5369895646239153288028959828928500409412452784171482656503228484874825519738751973578086809622825851908395426067851800026991317410174972251396509129435245813644280397339404585650997080096768
0],[1995184191709300022112499963008354165798102492847328205881729992615280991556717774932326383177091072739215190386759564813540855415263312635569457166531418210571823087616
8520262826242210480879419292400676219938912819649696771559384757914300763842035300173353201441241202425856
3621713908511769219329739318576672925164933392068862125423355355176650245922290935987339154549790164236105678848]);

% % bode(sys_before);grid on

%

% %% Modelling including all
```

```
% clear
% clc
% % L = 10^-6;
% % RL = 10;
% % C_before = 10^-12;
% % RC = 1;
% % C_after = 2*10^-12;
%
% syms s
%
% C_ins = 4.5881e-11
% C_DL  = 6.5539e-10
% C_sol = 4.3067e-12
% G_sol = 1.0944e-05
% C_ox  = 1.2920e-13
% C_latins = 6.3025e-15
% R_sol=1/G_sol
% W = {10^3,10^9}  %10^9 and 10e9 are different
%
% Z_up = 2*1/(s*C_DL)+2*1/(s*C_ins)+[R_sol/(s*C_sol)]/[1/(s*C_sol)+R_sol]
% %Z_mid = 2*1/(s*C_ins)+1/(s*C_DL)+1/(s*C_DNA)+[R_msol/(s*C_msol)]/[1/(s*C_msol)+R_msol]
% Z_low=1/(s*C_ox)
%
% Z_lat=1/(s*C_latins)
% % Z_eq =simplifyFraction(Z_up,'Expand',true)
% %
sys_before=tf([2100406951821989555924141185539905679630169373583218349928483220139
0007808
89282141010003843722392365705945216876298947014551592815169124261627774541758464]
,[7532687356148533579016633329041866754999433387943373393212248651914173971386201931303084399952945947469050705174463066630490549125120 0]);
% % bode(sys_before);grid on
%
```

```
% Z_eq =simplifyFraction(1/(1/Z_up + 1/Z_low + 1/Z_lat ),'Expand',true)

%
sys_before=tf([8603266874662869221065282295971453663765173754196862361307067269689753919815683656996495769757438869191299315516083253204869716033241709327329756273645230426685544],[3201965158046839893232625173782889951426128030734390077487926749729789000980356468726448514603866571004995485857676831274507211110521975603 2 0]);

% bodeplot(sys_before);grid on

% %bodeplot(sys_before,W);grid on

%

% %% Modelling without adding Material under test, parameters are from above

% clear

% clc

% L = 10^-6;

% RL = 10;

%

% syms s

%

% C_ins = 4.5881e-11

% C_DL  = 6.5539e-10

% C_sol = 4.3067e-12

% G_sol = 1.0944e-05

% C_ox  = 1.2920e-13

% C_latins = 6.3025e-15

% R_sol=1/G_sol

% %these parameters are already been checked

%

% %W = logspace(10^6,10^10,100);

% W = {10^7,10^10};  %10^9 and 10e9 are different

% %W = {5*10^8,0.7*10^9};  %10^9 and 10e9 are different

%

% Z_up = 2*1/(s*C_DL)+2*1/(s*C_ins)+[R_sol/(s*C_sol)]/[1/(s*C_sol)+R_sol]

% Z_low=1/(s*C_ox)
```

```
% Z_lat=1/(s*C_latins)

%

%

% Z_eq =simplifyFraction(1/(1/Z_up + 1/Z_low + 1/Z_lat + 1/(s*L+RL)),'Expand',true)

%
sys_before=tf([860326687466286922106528229597145366376517375419686236130706726968975391981568
896896652423984496495220142590300527209049424116846568547800000266538128433872268544
365699649576975743886919129931551608325320486971603324170932732975627364523042668544000000],[320196515804683989323262517378288995142612803073439007748792674972939909661384033086196811397776494609564216138884112213519951378602509756032
860405587564322568979173081057532023477016924005453919258157448080027589541888000000
365699649576975743886919129931551608325320486971603324170932732975627364523042668544000000]);

%

% P = bodeoptions; P.FreqUnits = 'Hz';

% bodeplot(sys_before,P,W);grid on

% hold on

% % h = bodef(sys_before); grid on

% %

% %    function h = bodef(x)

% %    P = bodeoptions; P.FreqUnits = 'Hz';

% %    h = bodeplot(x,P);

% %    end

% C_protein=10^-15

% Z_add=1/(s*C_protein)

% Z_eqafter =simplifyFraction(1/(1/Z_up + 1/Z_low + 1/Z_lat + 1/Z_add + 1/(s*L+RL)),'Expand',true)

%
sys_after=tf([26255086897774869449051764819248820995377117169790229374106040251738750976000000000000000027371113660399917495581669390573136206330854007472124284295654305009098157771980800000000000000011160267626250480465299045713243152109537368376818949101896140532703471817719808000000000000000000000000],[977424769511201837205423493045802947019196944613589405433367143693838188291011218219920366129334771006774228531267379401531321819518604640399246594891762827
```

```
19808
26257494849283418724027420652060648278580719215657311675237752984294278543034718
177198080000000
11160267626250480465299045713243152109537368376818949101896140532703471817719808
000000000000000000000]);

% bodeplot(sys_after,P,W);grid on

%

% %% Simplified version for testing (demo)

% clear

% clc

% %%%%%%%%%%%%%%%%%%%%%%%%%Given Parameters%%%%%%%%%%%

% L = 10^-6;

% RL = 10;

% C_protein=10^-15;

%

% syms s

%

% C_ins = 4.5881e-11;

% C_DL  = 6.5539e-10;

% C_sol = 4.3067e-12;

% G_sol = 1.0944e-05;

% C_ox  = 1.2920e-13;

% C_latins = 6.3025e-15;

% R_sol=1/G_sol;

% %these parameters are already been checked

%

% %%%%%%%%%%%%%%%%%%%%%%%%%%Equivalent impedance
calculation(before)%%%%%%%%%%%

% Z_up = 2*1/(s*C_DL)+2*1/(s*C_ins)+[R_sol/(s*C_sol)]/[1/(s*C_sol)+R_sol];

% Z_low=1/(s*C_ox);

% Z_lat=1/(s*C_latins);

% Z_eq =simplifyFraction(1/(1/Z_up + 1/Z_low + 1/Z_lat + 1/(s*L+RL)),'Expand',true);

%
```

```
% [numexpr, denexpr] = numden(Z_eq);
% num_coeff = sym2poly(numexpr);
% den_coeff = sym2poly(denexpr);
% sys_before=tf([num_coeff],[den_coeff]);
%
% %%%%%%%%%%%%%%%%%%%%%%%%%Plotting(before)%%%%%%%%%%%
% %W = logspace(10^6,10^10,100);
% W = {10^7,10^10};  %10^9 and 10e9 are different
% %W = {5*10^8,0.7*10^9};  %10^9 and 10e9 are different
% P = bodeoptions; P.FreqUnits = 'kHz';
% bodeplot(sys_before,P,W);grid on
% hold on
%
% %%%%%%%%%%%%%%%%%%%%%%%%%Equivalent impedance calculation
(after)%%%%%%%%%%%
% Z_add=1/(s*C_protein);
% Z_eqafter =simplifyFraction(1/(1/Z_up + 1/Z_low + 1/Z_lat + 1/Z_add + 1/(s*L+RL)),'Expand',true);
%
% %%%%%%%%%%%%%%%%%%%%%%%%%Plotting(after)%%%%%%%%%%%
% [numexpr2, denexpr2] = numden(Z_eqafter);
% num_coeff2 = sym2poly(numexpr2);
% den_coeff2 = sym2poly(denexpr2);
% sys_after=tf([num_coeff2],[den_coeff2]);
% bodeplot(sys_after,P,W);grid on
% hold on
%
% %% Bode plot with/without Material under test
% clear
% clc
% %%%%%%%%%%%%%%%%%%%%%%%%%Given Parameters%%%%%%%%%%%
% L = 50*10^-9;
```

```
% RL = 10;
% C_protein=10^-15;     %the bacteria capacitance
%
% syms s
%
% C_ins = 4.5881e-11;
% C_DL  = 6.5539e-10;
% C_sol = 4.3067e-12;
% G_sol = 1.0944e-05;
% C_ox  = 1.2920e-13;
% C_latins = 6.3025e-15;
% R_sol=1/G_sol;
% %these parameters are already been checked
%
% %%%%%%%%%%%%%%%%%%%%%%%%%Equivalent impedance calculation(before)%%%%%%%%%%%
% Z_up = 2*1/(s*C_DL)+2*1/(s*C_ins)+[R_sol/(s*C_sol)]/[1/(s*C_sol)+R_sol];
% Z_low=1/(s*C_ox);
% Z_lat=1/(s*C_latins);
% Z_eq =simplifyFraction(1/(1/Z_up + 1/Z_low + 1/Z_lat + 1/(s*L+RL)),'Expand',true);
%
% [numexpr, denexpr] = numden(Z_eq);
% num_coeff = sym2poly(numexpr);
% den_coeff = sym2poly(denexpr);
% sys_before=tf([num_coeff],[den_coeff]);
%
% %%%%%%%%%%%%%%%%%%%%%%%%%Plotting(before)%%%%%%%%%%%
% %W = logspace(10^6,10^10,100);
% W = {5*10^8,10^10};  %10^9 and 10e9 are different
% %W = {5*10^8,0.7*10^9};  %10^9 and 10e9 are different
% P = bodeoptions; P.FreqUnits = 'MHz';
```

```
% bodeplot(sys_before,P,W);grid on
% hold on
%
%
%
% %%%%%%%%%%%%%%%%%%%%%%%%%%Equivalent impedance calculation (after)%%%%%%%%%%%
% Z_add=1/(s*C_protein);
% Z_eqafter =simplifyFraction(1/(1/Z_up + 1/Z_low + 1/Z_lat + 1/Z_add + 1/(s*L+RL)),'Expand',true);
%
% %%%%%%%%%%%%%%%%%%%%%%%%%%Plotting(after)%%%%%%%%%%%
% [numexpr2, denexpr2] = numden(Z_eqafter);
% num_coeff2 = sym2poly(numexpr2);
% den_coeff2 = sym2poly(denexpr2);
% sys_after=tf([num_coeff2],[den_coeff2]);
% bodeplot(sys_after,P,W);grid on
% hold on
%
% % Set title, axes labels, and legend font size
% set(findall(gcf,'Type','text'),'FontSize',18)
% % Set data line width and color
% set(findall(gcf,'Type','line'),'LineWidth',2)
% % Set axes tick label font size, color, and line width
% set(findall(gcf,'Type','axes'),'FontSize',18)
%
% datacursormode on
% %xlabel('Frequency','FontSize',20,'FontWeight','bold')
% % % Set title, axes labels, and legend font size
% % set(findall(gcf,'Type','text'),'FontSize',11)
% % % Set data line width and color
% % set(findall(gcf,'Type','line'),'LineWidth',2,'Color','red')
```

```
% % % Set axes tick label font size, color, and line width
% % set(findall(gcf,'Type','axes'),'FontSize',11,'LineWidth',2,'XColor','black','YColor','black')
```