Guest Editorial Memristive-Device-Based Computing

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DOI
10.1109/TVLSI.2018.2878679

Publication date
2018

Document Version
Final published version

Published in
IEEE Transactions on Very Large Scale Integration (VLSI) Systems

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TODAY'S and emerging computing tasks are extremely demanding in terms of storage, energy efficiency, and computing efficiency; data-intensive/big-data applications and Internet-of-Things are couple of examples. In addition, today's computer architectures and device technologies are facing major challenges making them incapable to deliver the required functionalities and features. Computers are facing the three well-known walls [1)]: the memory wall, the instruction level parallelism wall, and the power wall. Similarly, nanoscale CMOS technology is facing three walls [2)]: the reliability wall, the leakage wall, and the cost wall. In order for computing systems to continue to deliver sustainable benefits for the foreseeable future society, alternative computing architectures have to be explored in the light of emerging new device technologies. Using memristive device technology [3)] to enable new computing paradigms such as computation-in-memory architecture [4)-7)] is one of the emerging alternatives that could provide a huge potential in terms of energy and computing efficiency.

This Special Issue aims at presenting novel solutions for any aspect related to memristive-device-based computation-in-memory. From over 100 received submissions from experts in the field, only 24 papers have been accepted to be included in this issue. These 24 papers cover various areas related to memristive-based computing, including memristive devices for memory design, logic circuit design, secure hardware, architecture, accelerators, and even design automation aspect.

Four papers are related to memory design. The paper titled "Two-Phase Read Strategy for Low Energy Variation-Tolerant STT-RAM" by Park and Yim proposes an adaptive two-phase read strategy that allows reliable reads under high variability at a substantially lower energy of spin-transfer torque magnetic random access memory (STT-MRAM) design. The paper titled "A Search Algorithm for the Worst Operation Scenario of a Cross-Point Phase-Change Memory Utilizing Particle Swarm Optimization" by Kim *et al.* addresses precise read margin evaluation for cross-point array of a phase change RAM using the particle swarm optimization algorithm. The paper titled "Experimental Investigation of 4-kb RRAM Arrays Programming Conditions Suitable for TCAM" by Grossi *et al.* provides extensive characterizations of multi-kilobit resistive RAM (RRAM) arrays during forming, set, reset, and cycling operations. The paper titled "A 2M1M Crossbar Architecture: Memory" by Teimoori *et al.* discusses a transistor-less memory cell 2M1M-based crossbar architecture, suitable for both storage and computation-in-memory.

Four papers cover aspects related to logic and circuit design. The paper titled "Three-Dimensional Pipeline ADC Utilizing TSV/Design Optimization and Memristor Ratioed Logic" by Mirzaie *et al.* presents a pipeline ADC architecture with a novel 3-D clock distribution network utilizing through-silicon being able to implement memristor ratioed logic as the basic elements of digital error correction subblock. The paper titled "Design Considerations for Energy-Efficient and Variation-Tolerant Nonvolatile Logic" by Yang *et al.* provides an architecture and a method for variation-tolerant, energy-optimal design of a nonvolatile flip-flop that uses an STT magnetic tunnel junction as the nonvolatile device. The paper titled "Configurable Logic Operations Using Hybrid CRS-CMOS Cells" by Wang *et al*. investigates the use of the complementary memristive switch CRS-CMOS cell for the realization of several logic operations including IMPLY, AND, and OR. The paper titled "Design and Synthesis of Self-Healing Memristive Circuits for Timing Resilient Processor Design" by Kong *et al.* leverages memristive technology (such as RRAM) to perform self-healing against design variation in modern chips.

Two papers deal with security aspects. The paper titled "CSRO-Based Reconfigurable True Random Number Generator Using RRAM" by Govindaraj *et al.* explores memristive technology and features such as cycle-to-cycle variations and random telegraph noise for the true random number generator design. The paper titled "Memristors for Secret Sharing-Based Lightweight Authentication" by Arafin and Qu investigates the nature of memristive devices and how they can be used for secure and lightweight authentication.

Eight papers deal with aspects related to architectures and/or accelerators for specific applications. The paper titled "Code Acceleration Using Memristor-Based Approximate Matrix Multiplier: Application to Convolutional Neural Networks" by Nourazar *et al.* investigates the feasibility of building a memristor-based approximate accelerator to be used in cooperation with the general-purpose 86× processor. The paper titled "Networked Power-Gated MRAMs for Memory-Based Computing" by Diguet *et al.* proposes an architecture which is based on the network-on-chip to interconnect MRAM-based clusters, processing elements, and managers. The paper titled "Accelerating k-Medians Clustering Using a Novel 4T-4R RRAM Cell" by Rupesh *et al.* discusses an RRAM-based memory-centric hardware accelerator for *in situ* k-medians clustering based on bit-serial median rank order filters. The paper titled "Via-Switch FPGA: Highly Dense Mixed-Grained Reconfigurable Architecture With Overlay Via-Switch Crossbars" by Ochi *et al.* explores the use of memristive crossbar (on BEoL layers) to provide a programmable interconnection for a highly dense reconfigurable architecture. The paper

Digital Object Identifier 10.1109/TVLSI.2018.2878679

titled "Exploiting Memristors for Compressive Sampling of Sensory Signals" by Qian *et al.* explores the nondeterminism of memristive devices for compressive sensing applications allowing ultra efficient signal acquisition with much fewer measurements. The paper titled "Memristor-Based Hardware Accelerator for Image Compression" by Halawani *et al.* analyses and demonstrates the area, speed, and energy efficiency of a memristive crossbar for implementing the lossy Haar 2-D discrete wavelet transform image compression algorithm. The paper titled "High-Throughput Pattern Matching With CMOL FPGA Circuits: Case for Logic-in-Memory Computing" by Madhavan *et al.* addresses the speedup of pattern matching tasks and multidimensional associative searches by programing the memristive devices in the crossbar to perform logic or interconnect functions. The paper titled "Stateful Memristor-Based Search Architecture" by Halawani *et al.* proposes a memristor-based stateful search engine architecture for image matching and pattern inspection.

Five papers address aspects related to neuromorphic/deep learning system implementation using memristive devices. The paper titled "ReRAM-Based Processing-in-Memory Architecture for Recurrent Neural Network Acceleration" by Long *et al.* presents a recurrent neural network accelerator design with RRAM-based processing-in-memory architecture. The paper titled "A Hardware Architecture for Columnar Organized Memory Based on CMOS Neuron and Memristor Crossbar Arrays" by Shamsi *et al.* proposes a hardware architecture for columnar organized memory (brain-inspired associative memory with large capacity and robust retrieval) based on low-power neuron and crossbar memristor array. The paper titled "A 4-Transistors/1-Resistor Hybrid Synapse Based on Resistive Switching Memory (RRAM) Capable of Spike-Rate-Dependent Plasticity (SRDP)" by Milo *et al.* presents an RRAM-based spike-rate-dependent plasticity synapse with a 4-transistors/1-resistor structure. The paper titled "Neuromorphic Vision Hybrid RRAM-CMOS Architecture" by Eshraghian, Jr., *et al.* proposes a low-power silicon-based retinal network, which can generate four types of ganglion cell output signals. The paper titled "SRMC: A Multibit Memristor Crossbar for Self-Renewing Image Mask" by Shang *et al.* proposes a self-renewing computing-in-memory unit, which executes the mask algorithm for deep learning.

One paper covers the automation aspect. The paper titled "On Synthesizing Memristor-Based Logic Circuits With Minimal Operational Pulses" by Wang *et al.* proposes a synthesis algorithm to deal with the fan-out problems in memristor-based logic circuit design using implication logic.

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APPENDIX
RELATED WORK

1) J. L. Hennessy *et al.*, *Computer Architecture: A Quantitative Approach*. Amsterdam, The Netherlands: Elsevier, 2011.
2) S. Hamdioui *et al.*, "Memristor for computing: Myth or reality?" in *Proc. DATE*, 2017, pp. 722–731.
3) "Beyond COMS," International Roadmap for Devices and Systems, 2017.
4) H. A. D. Nguyen, J. Yu, L. Xie, M. Taouil, S. Hamdioui, and D. Fey, "Memristive devices for computing: Beyond CMOS and beyond von Neumann," in *Proc. VLSI-SoC*, 2017, pp. 1–10.
5) P.-E. Gaillardon *et al.*, "The programmable logic-in-memory (PLiM) computer," in *Proc. Design Autom. Test Eur. Conf. Exhib. (DATE)*, Mar. 2016, pp. 427–432.
6) S. Hamdioui *et al.*, "Memristor based computation-in-memory architecture for data-intensive applications," in *Proc. DATE*, 2015, pp. 1718–1725.
7) G. Indiveri and S.-C. Liu, "Memory and information processing in neuromorphic systems," *Proc. IEEE*, vol. 103, no. 8, pp. 1379–1397, Aug. 2015.
8) S. Li, C. Xu, Q. Zou, J. Zhao, Y. Lu, and Y. Xie, "Pinatubo: A processing-in-memory architecture for bulk bitwise operations in emerging non-volatile memories," in *Proc. IEEE DAC*, Jun. 2016, p. 173.

Said Hamdioui (S'99–M'02–SM'11) received the M.S.E.E. and Ph.D. degrees (Hons.) from the Delft University of Technology (TU Delft), Delft, The Netherlands, in 1997 and 2001, respectively.

He was with Intel Corporation, Santa Clara, CA, USA, with Philips Semiconductors R&D, Crolles, France, and also with Philips/NXP Semiconductors, Nijmegen, The Netherlands. He joined TU Delft as a Professor, where he is currently Chair Professor of Dependable and Emerging Computer Technologies and the Head of the Computer Engineering Laboratory. He has published one book and contributed to other two, and has coauthored over 180 conference and journal papers. He holds two patents. His current research interests include dependable CMOS nanocomputing (including reliability, testability, and hardware security) and emerging technologies and computing paradigms (including 3-D stacked ICs, memristors for logic and storage, and in-memory-computing for big-data applications).

Dr. Hamdioui was a recipient of many international and national awards, including the Automation Association Outstanding Dissertation Award in 2003, the 2015 HiPEAC Technology Transfer Award, and the Best Paper Award at ICCD 2015 and IVLSI 2016.

Pierre-Emmanuel Gaillardon (S'10–M'11–SM'16) received the Diplôme d'ingénieur from CPE-Lyon, Villeurbanne, France, in 2008, the M.Sc. degree in electrical engineering from INSA Lyon, Villeurbanne, in 2008, and the Ph.D. degree in electrical engineering from CEA-LETI, Grenoble, France, and the University of Lyon, Lyon, France, in 2011.

He was a Research Assistant with CEA-LETI. He was a Research Associate with the Swiss Federal Institute of Technology (EPFL), Zürich, Switzerland, and a Visiting Research Associate with Stanford University, Stanford, CA, USA. He is currently an Assistant Professor with the Electrical and Computer Engineering Department and an Adjunct Assistant Professor with the School of Computing, The University of Utah, Salt Lake City, UT, USA, where he leads the Laboratory for NanoIntegrated Systems.

Dr. Gaillardon was a recipient of the C-Innov 2011 Best Thesis Award, the Nanoarch 2012 Best Paper Award, the BSF 2017 Prof. Pazy Memorial Research Award, the 2018 NSF CAREER Award, and the 2018 IEEE CEDA Pederson Award. He has been serving as a TPC Member for many conferences, including DATE from 2015 to 2019, DAC from 2016 to 2018, and Nanoarch from 2012 to 2018, and is a reviewer for several journals and funding agencies. He is an Associate Editor for the IEEE TRANSACTIONS ON NANOTECHNOLOGY and he served as a Topic Co-Chair of *Emerging Technologies for Future Memories* for DATE from 2017 to 2019.

Dietmar Fey received the Diploma degree in computer science and the Ph.D. degree, with a focus on an investigation about using optics in computer architectures, from Friedrich-Alexander-Universität Erlangen–Nürnberg (FAU), Germany, in 1987 and 1992, respectively.

From 1994 to 1999, he was with Friedrich-Schiller-University Jena, Jena, Germany, where he made his habilitation. From 1999 to 2001, he was a Lecturer with the University of Siegen, Siegen, Germany. He became a Professor of Computer Engineering with the Friedrich-Schiller-University Jena. Since 2009, he has been the Chair of Computer Architecture with FAU. He was involved in several national and international research projects and initiatives on parallel and embedded computing. He has published over 130 conference papers, 3 books, and about 100 papers in journals and reports. His current research interests include parallel computer architectures, parallel programing environments, parallel embedded systems, and memristive computing.

Dr. Fey is a member of HiPEAC (European Network of Excellence on High Performance and Embedded Architecture and Compilation), a contributor of the HiPEAC roadmap, an author of the Eurolab4HPC report "Disruptive Technologies for years 2020–2030," and a member of the EU Cost Action 1401 "Memristors Devices, Models, Circuits, Systems and Applications."

Tajana Šimunić Rosing (S'90–M'97–SM'14–F'18) received the master's degree in engineering management and the Ph.D. degree in electrical engineering at Stanford University, Stanford, CA, USA, in 1993 and 2001, respectively.

She was a Senior Design Engineer with Altera Corporation, San Jose, CA, USA. From 1998 to 2005, she was a Full-Time Research Scientist with HP Labs, Palo Alto, CA, USA, and also led research efforts at Stanford University. She is currently a Professor, a holder of the Fratamico Endowed Chair, and the Director of System Energy Efficiency Lab with the Computer Science and Engineering Department, University of California at San Diego, San Diego, CA, USA. She is leading a number of projects, including efforts funded by DARPA/SRC JUMP CRISP program, with a focus on the design of accelerators for analysis of big data, SRC funded project on Internet of Things system reliability and maintainability, and NSF funded project on design and calibration of air-quality sensors and others. Her current research interests include energy-efficient computing, and cyber-physical and distributed systems.

Dr. Rosing has served on a number of technical paper committees. She was an Associate Editor of the IEEE TRANSACTIONS ON MOBILE COMPUTING and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS.