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23.3 A 51A Hybrid Magnetic Current Sensor with a Dual Differential DC Servo Loop and 43mA$_{rms}$ Resolution in a 5MHz Bandwidth

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Magnetic current sensors are widely used in applications where galvanic isolation and wide bandwidth (BW) are desired, such as in switched-mode power supplies and motor drivers. By using Hall plates for low frequencies and pick-up coils for high frequencies, hybrid magnetic sensors can achieve high resolution (tens of mA) over a wide frequency range (up to 15MHz) [1-3]. However, previous designs exhibit either poor gain flatness over frequency or limited energy efficiency. This work presents a hybrid magnetic current sensor that achieves ±1.1% gain flatness, which is 3× better than prior art [1-3]. Its energy efficiency is also 11× better than the state-of-the-art [1,4,5].

As shown in Fig. 23.3.1, the differentiating characteristic of coils and the all-pass characteristic of Hall plates can be smoothly combined by a 1st-order low-pass filter (LPF), which defines the crossover frequency f_x [1,2]. The sensor's resolution is then mainly limited by the integrated thermal noise of the coil and Hall sensors from DC to f_x, and can be maximized by optimizing f_x.

A simplified schematic of the coil and Hall paths is shown in Fig. 23.3.2. The coil path is built around two amplifiers A_1 and A_2 that implement a two-stage LPF with a corner frequency of f_x [1]. The input stage reads out the coil current and implements a pole f_{p1}=140kHz ($1/2\pi R_1C_1$) that limits its high-frequency output swing. This is followed by an output stage, which implements an LPF with a corner frequency of f_x ($=1/2\pi R_4C_3$) and a zero at f_{z2} ($=1/2\pi R_3C_3$) that cancels the pole at f_{p1}. To achieve a gain flatness of 1%, a similar pole/zero mismatch can be tolerated, which can be achieved by proper layout.

Since the coil path is DC-coupled, the offsets of A_1 and A_2 will also be amplified. To prevent this, the coil path should have a high-pass characteristic, but with a corner frequency f_{HP} much lower than f_x to maintain gain flatness. In [2], this required the use of external capacitors (10µF), while in [1], the use of on-chip DC-blocking capacitors (260pF) resulted in a relatively high f_{HP} (1.25kHz), which limited the gain flatness around f_x (10kHz). In this work, a dual differential DC servo-loop (D3SL) is proposed to emulate even larger on-chip capacitors, while occupying much less area. This allows both f_x (2kHz) and f_{HP} (15Hz) to be optimized for noise and gain flatness, respectively.

The proposed D3SL senses the DC voltage across R_2 and drives it to zero by regulating the output of the input stage. This effectively removes R_2 from the circuit, and as a result, the sensor's output-referred offset is mainly limited by the offset of A_2 and the residual offset of the Hall sensors. Exploiting the differential nature of the signal path, the voltage across R_2 is sensed by two resistors $R_{s1,2}$ (=10MΩ), integrated on C_{int} (=20pF), and then used to regulate the output of A_1 via feedback resistor R_{fb} (=1.6MΩ). The integrator is built around a two-stage amplifier A_{DSL}, whose high gain (~120dB) reduces the offset contribution of A_1 to the µV-level. A_{DSL} is chopped to mitigate its own offset, which would otherwise appear across R_2. The DSL integrator establishes f_{HP} (~15Hz), which causes a worst-case dip of 1% in the sensor's gain around f_x. To achieve the same gain flatness, an impractically large (100nF) blocking capacitor would have been required.

The temperature dependence of the coil current is determined by the large temperature coefficient (TC =0.34%/K) of the metal coil resistance R_{Coil}. As shown in Fig. 23.3.3, at frequencies above f_x, the gain of the coil path is determined by $R_{1,2,3}$. Most of the coil's TC can then be cancelled by implementing $R_{1,3}$ with silicided n-poly resistors (TC =0.29%/K) [1]. In this work, the residual TC is cancelled by realizing R_2 as a series combination of non-silicided p-poly (TC =-0.02%/K) and n-poly (TC =-0.15%/K) resistors.

As in [1], the Hall voltages output by two spinning quadruple Hall plates are first upmodulated to twice the spinning frequency f_{sp}, and then amplified by two capacitively-coupled amplifiers (CCAs). Both CCAs use switched resistors (>3GΩ) to provide DC feedback. Deadband switches after the 1st stage mitigate the extra offset caused by spinning-induced transients in the Hall-plate outputs. The amplified Hall signal is then demodulated and applied to the output stage via an LPF, whose pole ($f_{LPF}=1/2\pi(R_{LPF1}||R_{LPF2})C_{LPF}$) cancels the output stage zero f_{z2}. Since f_{z2} is 70× higher than f_x, the mismatch between f_{LPF} and f_{z2} has a negligible impact on gain flatness.

Due to the n-well's anisotropic resistance, the output of the spinning Hall plates will contain systematic ripple. In [2], this is split into three components, which are suppressed by three ripple-reduction loops (RRLs) in parallel. In this work, we note that the ripple can be split into two quadrature square-waves at f_{sp} and a square-wave at $2f_{sp}$. However, the latter represents the residual offset of spinning, as it cannot be distinguished from the upmodulated Hall voltage. Two RRLs are thus enough to suppress the systematic ripple.

As shown in Fig. 23.3.2, the two RRLs can be efficiently combined in a single multiplexed RRL (MRLL) built around A_5. This sequentially suppresses the quadrature ripple components, the offset of A_5, which limits the amplitude of the residual ripple, and the offset of A_4, which causes extra ripple at $2f_{sp}$. Each quadrature component is chopper demodulated and then integrated via R_{s3} (=10MΩ) and C_{fsp} (=5pF) to generate a correction signal that is upmodulated and fed back to A_4 via an auxiliary input stage. The offset of A_4 is suppressed similarly but with the chopper disabled. For a good tradeoff between residual offset and the low-pass filtering of residual spinning ripple, f_{sp} = 25kHz was chosen.

In [1], the large negative TC of the sensitivity of an n-well Hall plate (about -0.4%/K) is partially compensated by using a PTAT bias current (0.33%/K). Due to the large positive TC of the n-well resistance (0.37%/K), however, the voltage across the Hall plate will rise rapidly with temperature, limiting the maximum bias current for a given supply voltage, and thus the Hall plate's resolution. In this work, partial compensation is achieved by giving the DC gain of the output stage a positive TC (0.13%/K), by implementing R_{LPF} and R_4 with non-silicided n-poly (-0.15%/K) and non-silicided p-poly (-0.02%/K) resistors, respectively. The residual Hall plate TC is compensated by a tunable sub-PTAT bias generator, in which a PTAT voltage ΔV_{GS} is forced across a fixed non-silicided n-poly R_{c1} resistor in parallel with a tunable silicided n-poly resistor R_{c2}.

The chip was fabricated in a standard 0.18µm CMOS process (Fig. 23.3.7, top) and occupies 3.9mm^2. As in [1], it is mounted on an S-shaped low-resistance (250µΩ) current rail (Fig. 23.3.7, bottom), whose slots concentrate the magnetic field seen by two coil/Hall sensor pairs. The die thickness is 200µm, resulting in a current sensitivity of 283µT/A. It draws 7.1mA from a 1.8V supply, of which 4.4mA is used to bias the Hall plates.

To obtain a flat frequency response at room temperature, the gains of the Hall and coil paths are matched by trimming the bias current of the Hall plates via an 8-bit current DAC [1]. As shown in Fig. 23.3.4 (top right), the gain variation around f_x is less than ±1.1% (4 samples), which is mainly limited by the MRRL notches at f_{sp} and $2f_{sp}$. Figure 23.3.4 (top left) shows the sensor's overall frequency response. Its -3dB bandwidth is around 5MHz, even though eddy currents induced in the current rail reduce its gain above 200kHz. Confirmed by FEM simulations, the spread above 200kHz is due to the manual assembly process, which causes some variation in the position of the die above the current rail, and thus in the magnitude of the eddy currents.

The sensor's noise spectral density and the accumulated noise are shown in Fig. 23.3.4 (bottom left). In a 5MHz BW, the sensor achieves an accumulated input-referred noise of 43mA$_{rms}$. High frequency noise and spinning ripple are suppressed by the sensor's low-pass characteristic. The residual ripple at f_{sp} only causes a 0.3mA step in the total accumulated noise. The MRRL suppresses the dominant components of the spinning ripple (at f_{sp} and $3f_{sp}$) by more than 24dB (Fig. 23.3.4, bottom right), resulting in an input-referred ripple of 5mA$_{rms}$ (1.5µT$_{rms}$) which is about 5× less than that reported in [2] and is well below the sensor's total integrated noise.

As shown in Fig. 23.3.5 (top left), without the D3SL, the offset of the sensor (coil+Hall) is about 600µT (1σ) (5 samples). This drops to about 73µT (1σ) when the D3SL is enabled. To measure the gain drift of the Hall and coil paths over temperature, fixed currents (1A$_{p-p}$) are applied at 200Hz and 80kHz. The resulting normalized sensitivities are shown in Fig. 23.3.5 (top right). The proposed temperature compensation schemes reduce the gain variation of the coil path to ±0.9%, while that of the Hall path is ±2.7% (with a fixed TC trim setting).

As shown in Fig. 23.3.5 (bottom left), the maximum input current (-1dB compression point) of the Hall path is 55A, which is limited by the self-heating of the current rail. By injecting a test current (at 120kHz) into the coil path, the high-frequency dynamic range can be extrapolated, which is 72A$_p$ (51A$_{rms}$). The sensor's response to 1A$_{p-p}$ square-wave signal is shown in Fig. 23.3.5 (bottom right). The slight lack of amplitude flatness is due to the residual gain mismatch of the Hall and coil paths.

In Fig. 23.3.6, the performance of the current sensor is summarized and compared with the state-of-the-art. Compared to prior hybrid sensors, its resolution (1.5×), gain error (1.6×), and dynamic range (+9.5dB) are significantly improved. Compared to other CMOS magnetic current sensors, it achieves the lowest FoM (×11).

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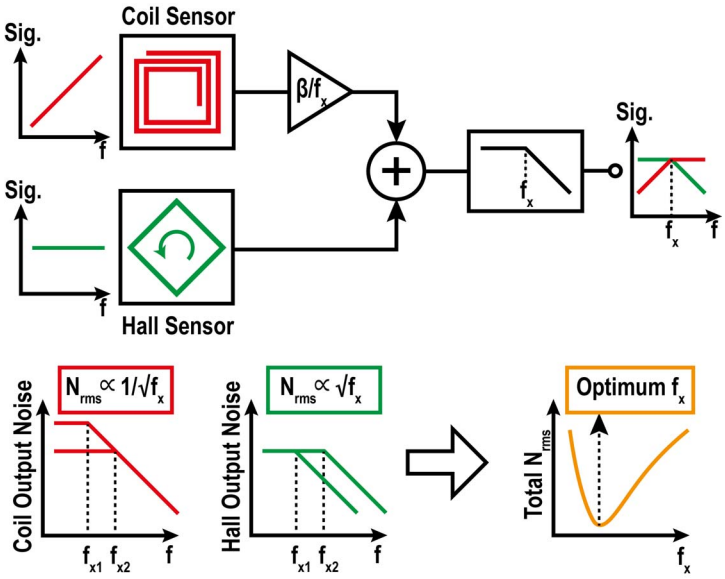

Figure 23.3.1: Simplified system block diagram + Optimum crossover frequency.

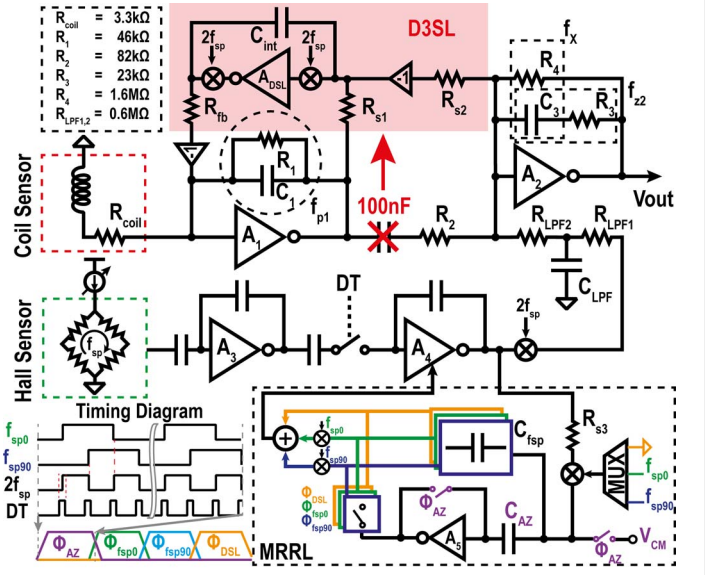

Figure 23.3.2: Simplified single-ended circuit diagram of the fully differential hybrid current sensor.

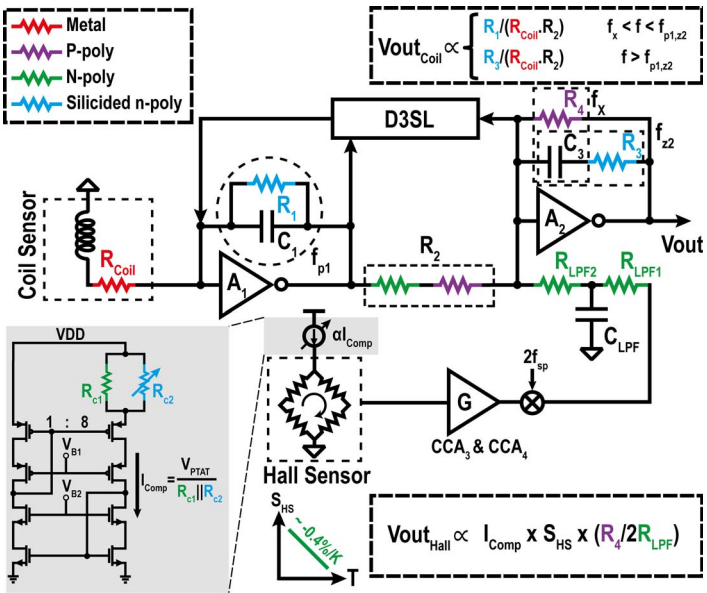

Figure 23.3.3: Temperature compensation in the coil path and Hall path.

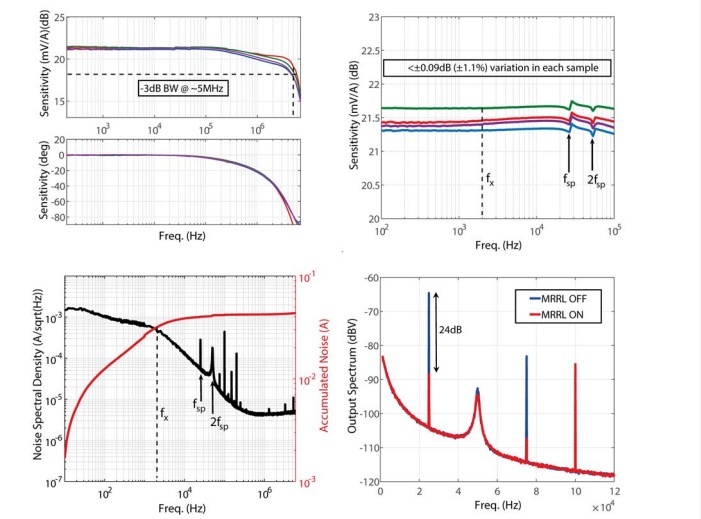

Figure 23.3.4: Sensitivity vs. frequency magnitude and phase (top left). Zoomed-in sensitivity vs. frequency around the crossover frequency (top right).Noise spectral density and accumulated noise referred to current rail (bottom left) Output spectrum w/ MRRL on/off (bottom right).

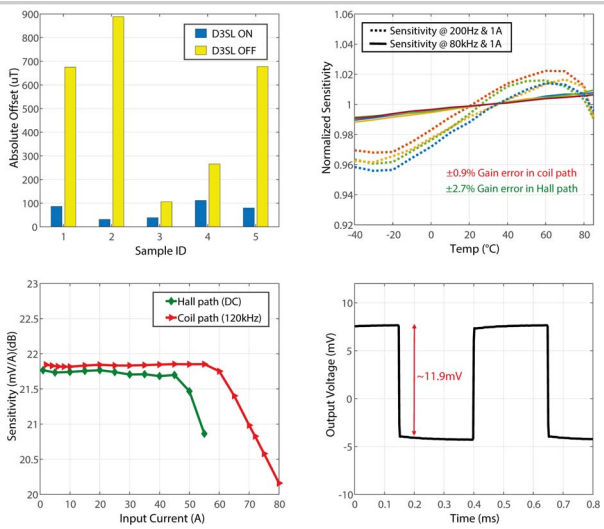

Figure 23.3.5: Sensor absolute offset (coil+ Hall) referred to current rail w/ D3SL on/off (top left). Sensitivity vs. temperature (top right). Sensitivity vs. input range for DC and extrapolated AC(rms) currents (bottom left). Transient response for a 1A$_{p\text{-}p}$ square-wave @ f_x=2kHz (1024× averaging) (bottom right).

	This Work	ISSCC'21 [1]	JSSC'19 [4]	APEC'19 [3]	JSSC'22 [5]
Sensor Type	**Coil + Hall**	Coil + Hall	Hall	Rogowski Coil + Hall	IFG
Technology [µm]	**0.18**	0.18	0.35	0.18	0.25
Supply [V]	**1.8**	1.8/3.3	3.3	1.8	1.8/5
Area [mm^2]	**3.9**	4.6	N/A	2.74	4+3.6
Resolution	**43 mA**	64 mA	480 mA	710 mA	11 mA[c]
Range	**DC: ±55 A AC: ±51 A**[a]	±25 A	±300 A	±60 A	±53 A[c]
Dynamic Range (DR) [dB]	**61.5**	52	56	39	74
BW [MHz]	**5**	1.8	1.7	15.3	0.125
Power Consumption [mW]	**12.8**	19.5	13.2	63.5	100[d]+13
Gain flatness	**±1.1%**	±12%	N/A	±3.7%	N/A
Gain Error	**±2.7%**	±4.5%	±4%	N/A	N/A
Temperature Range	**-40 to 85 °C**	-40 to 85 °C	-40 to 150 °C	N/A	N/A
Residual Ripple [µT]	**1.5**	74	N/A	N/A	N/A
Residual Offset [µT]	**73**	75	262	N/A	N/A
FoM[b] [fW/Hz]	**0.45**	17.7	5	145	8.5
DR + 10log(BW/Power)	**147**	131	137	122	135

[a]Extrapolated [b]FoM = Power/(BW x (Range/Resolution)^2) [c]Conversion rate = 45µT/A [d]Full-range power

Figure 23.3.6: Performance summary and comparison with state-of-the-art CMOS magnetic current sensors.

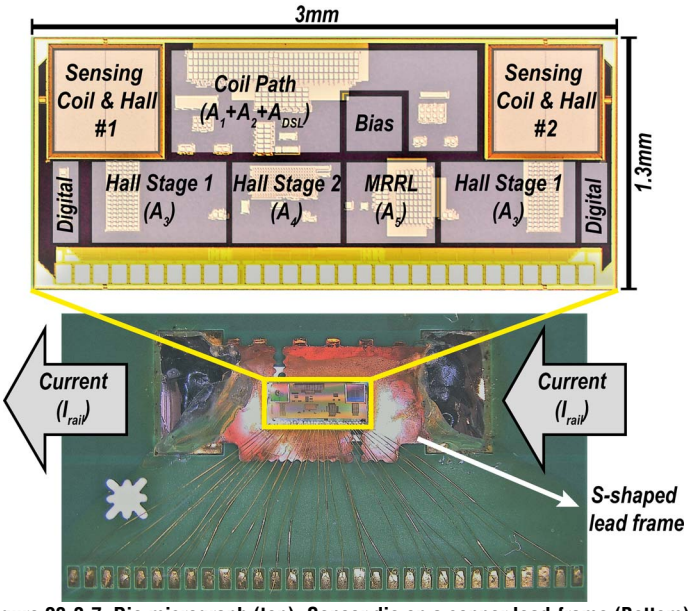

Figure 23.3.7: Die micrograph (top), Sensor die on a copper lead-frame (Bottom).

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