A High-Precision Capacitive Sensor System for Displacement Measurements

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To my beloved parents and Chi

致我亲爱的父母和刘驰

Contents

Chapter 1

Introduction

1.1 Motivation

Capacitive sensors are applied for measurement of a wide range of physical parameters (e. g. displacement/vibration, humidity, and acceleration), due to their simple structure, low-cost and high performance. Their operating principle is based on modulation of the electric field of the sensor by a variation of the physical parameter of interest. In the ideal case capacitive sensors do not consume or generate electrical energy, which makes them practically noise-free.

In many high precision industrial machines, capacitive sensors are used for accurate displacement/position measurements of critical elements. Even very small displacement of such critical elements can greatly influence the achievable performance of the overall system [3]. Hence, there is a need for fast and accurate displacement/position measurement in the sub-micrometer range with sub-nanometer precision [1-3].

A good example of such applications can be found in a lithography machine, as shown in Fig. 1-1. To maintain the imaging quality, the unwanted small displacement of a lens column has to be determined by a displacement sensor in real time. Then, this information is used to maintain the relative position between the lens column and the wafer stage. This application becomes even more challenging with the down scaling of the CMOS technology, which

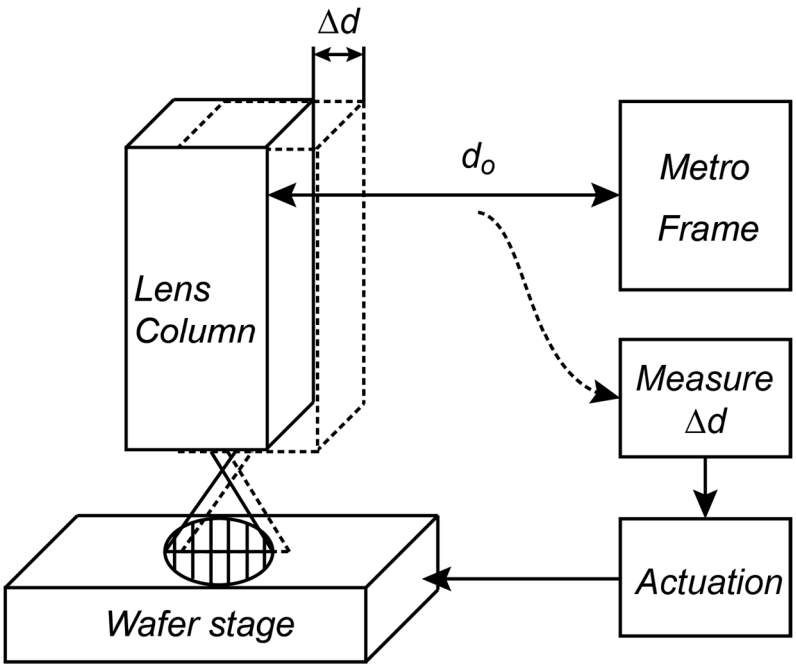

Figure. 1-1. A lithography machine in which the wafer stage is dynamically aligned with the lens columns by measuring its small displacement/vibration.

requires the measurement accuracy of the displacement sensor to scale in the same aggressive way.

Displacement measurement with sub-nanometer resolution is quite challenging for the designers of both the sensor and the interface electronics. The capacitive sensor has to provide very high sensitivity, determined by the mechanical structure of the sensor head. However, the conventional capacitive sensor heads suffer from a number of important non-idealities (e.g. electrode surface roughness, tilt, and mounting tolerance). The non-idealities of the sensor head need to be compensated by the interface electronics, which puts a large pressure on the performance of the interface electronics.

Power limitations pose another challenge to the designers of capacitive sensors in high-performance systems. To achieve high-resolution, it is required that the interface circuit is located very close to the sensor head, so that only the digital representation of the displacement information transfers through the noisy industrial environment. To this end, the overall sensor system has to be kept low-power to avoid a self-heating from deteriorating the performance of the sensor. This requirement leads to a quite big challenge for a high-resolution sensor interface. This becomes even worse when the sensor system is used in real-time applications, which require fast conversion.

To achieve good accuracy, the conventional capacitive sensor systems need to be calibrated periodically so as to eliminate the cross-sensitivity to the environment (e.g. temperature and humidity) and the drift of both the sensor head and the interface electronics. However, in inaccessible industrial environments, performing a sensor calibration is technically very difficult, costly and means an interruption of the production process. Therefore, the capacitive displacement sensor must provide accurate and stable measurements over a long period of time, while remaining insensitive to the variations of the ambient environment.

After performing a broad literature survey on the state-of-the-art capacitive sensors, it is concluded that there is no existing solution which demonstrates all above-mentioned properties (e.g. high resolution, low power and high precision). Hence, to fully exploit the advantages of capacitive sensors and to utilize them in high-precision applications, an in-depth investigation of their limitations and a dedicated research on new advanced system-level and circuit-level solutions, is essential.

1.2 Main Question and Challenges

A capacitive displacement-sensor system consists of a capacitive sensor and a capacitance-to-digital converter (CDC). The capacitive sensor converts the displacement into a capacitance change which is then digitized by the CDC.

The main question of this thesis is: how to measure capacitance with high resolution, short measurement time in a power efficient way, without frequent re-calibration. To answer this question, three main challenges need to be addressed:

1). Large standoff distance due to mounting tolerances:

The biggest challenge to realize a high-performance capacitive displacement sensor for nanometer displacements is the large standoff distance between the sensor plates. Due to mechanical limitations such as: the mounting tolerances of the sensor plates, the standoff distance d_o has to be maintained much larger than the maximum displacement Δd_{max} to be measured. This is needed to avoid a collision of the sensor plates during mounting and transportation. The large standoff distance, however, brings two negative impacts on the overall sensor performance: *reduced sensitivity* of the sensor and *increased dynamic range* (DR) requirement for the CDC. As will be described in Chapter 2, due to the large initial standoff distance of the sensor the required DR can be as high as 22-bit, while the actual range of interest is only around 12-bit. The details will be discussed in Chapter 2.

2) Power efficiency:

In many applications, the capacitive displacement sensor is used for real-time measurements and in control loops. One example is depicted in Fig. 1-1, where a control loop stabilizes the relative position of critical elements. In these applications a short conversion time is required to accurately track the position of the target and to avoid instability of the control system.

Besides, the capacitive sensor head, including its interface circuits (the CDC), has to be integrated in a small package. Therefore, as already mentioned, the power dissipation of the CDC has to be limited to avoid an excessive self-heating which might deteriorate the performance of the overall system due to the deformation of the sensing element and the thermal drift of the interface electronics.

Generally, the DR of a capacitive sensor interface is proportional to the product of its conversion time and the power consumption, meaning that a larger DR requires larger product of the two. Fig. 1-2 shows a qualitative plot about their relation. The red triangle indicates the practical relation between DR, power consumption and the conversion time of a conventional capacitive sensor system. The targeted applications, however, require a higher DR and a shorter conversion time, while maintaining a tight power consumption, which leads to the grey triangle in the same plot. The gap between these two triangles is what has to be filled up by this thesis work. As will be shown in the state-of-the-art survey in the following chapter, there is no existing solution which satisfies all the requirements.

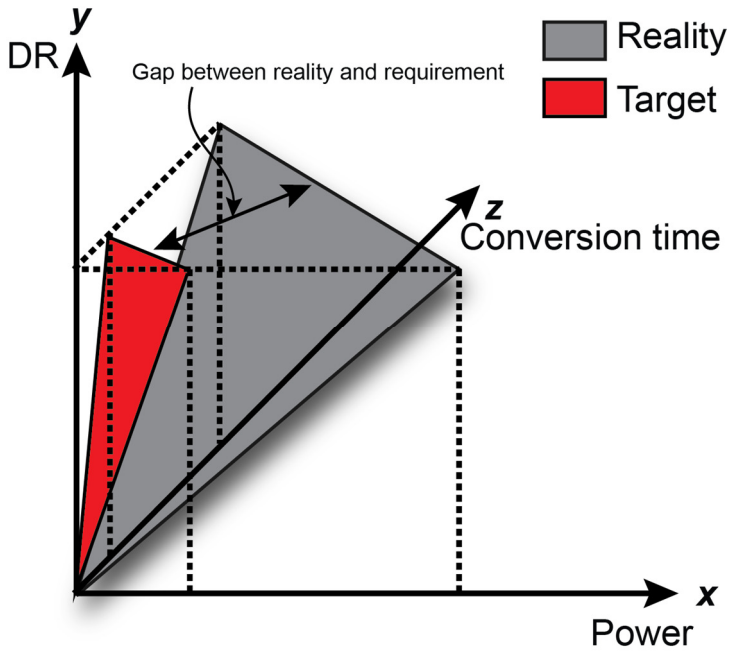

Figure. 1-2. Qualitative diagram of the relations between DR, power consumption and the conversion time. (the red triangular is the practical situation while the grey one is the requirement for the target applications, thus the gap in between is what have to be filled by this work)

3). Precision and stability:

The capacitive sensor system, as discussed earlier, will be applied in complex and high-precision machines in which the sensor is not easily accessible. As a consequence, the measurement precision has to be maintained for a long period of time, even if the environmental conditions (e.g. temperature) change, without the need for frequent calibration of the sensor system. Such a requirement, as will be further addressed in the following chapters, is not considered in most of the state-of-the-art capacitive sensor designs. Adding the requirement for precision, however, dramatically increases the design complexity of both the sensor head and the interface electronics.

1.3 Research methodology

To answer the research question and to create a capacitive sensor system which satisfies all the requirements, the following procedures have been followed:

1) A survey of the reported state-of-the-art solutions:

First, the state-of-the-art solutions of high-performance capacitive sensors are studied and analysed so as to evaluate their advantages and limitations for use in the targeted applications. The study is split into two parts: (i) investigation of the possible methods to overcome the non-idealities of the sensor head, with special attention to the mounting tolerances; (ii) investigation of the capacitance measurement approaches which deliver high resolution and precision.

2) Identify the problems and address them in a specific way:

Based on the analysis of the challenges, the performance of the system is split into different functions. Next, the errors and the power budgets of the functions are carefully defined. This helps to identify the problems and reduce the complexity of the overall investigation.

3) Solve each of the challenges by proposing and implementing proper techniques and solutions.

After defining the performance requirements at function level, a solution is proposed for each function. Next, possible design techniques and architectures are investigated. Finally, the validity of the proposed solutions is demonstrated by the experimental results with a developed and realized demonstrator.

1.4 Organization of the thesis

Following the research methodology, the thesis is organized as follows (Fig. 1-3):

Chapter 2 provides a detailed survey of the state-of-the-art capacitive sensor systems, for both the sensor and the interface electronics. The results of the survey provide solid understanding of the limitations of the existing solutions and help to define the challenges of the system. Based on that, the design challenges are split into two parts: the sensor head and the precision CDC.

Chapter 3 presents the details of the thermal stepper system, which helps to reduce the mounting tolerance of the sensor by smartly driving one of the sensor plate towards the other. Different control schemes as well as their trade-offs are discussed in detail. Finally, an optimal control system is proposed. A prototype is presented in which the control algorithm is implemented which shows better performance in terms of controllability, speed and power consumption.

Chapter 4 performs the system-level investigation and analysis of a precision capacitance-to-digital converter (CDC). Specifically, the error and power budgets are carefully tackled so as to achieve high resolution and precision in a power-efficient manner.

The detailed precision circuit techniques and implementation is discussed in Chapter 5. The proposed CDC is implemented and fabricated. The measurement strategy and results are shown and discussed in Chapter 6. Following the discussions, Chapter 7 concludes the thesis and provides recommendations for future works.

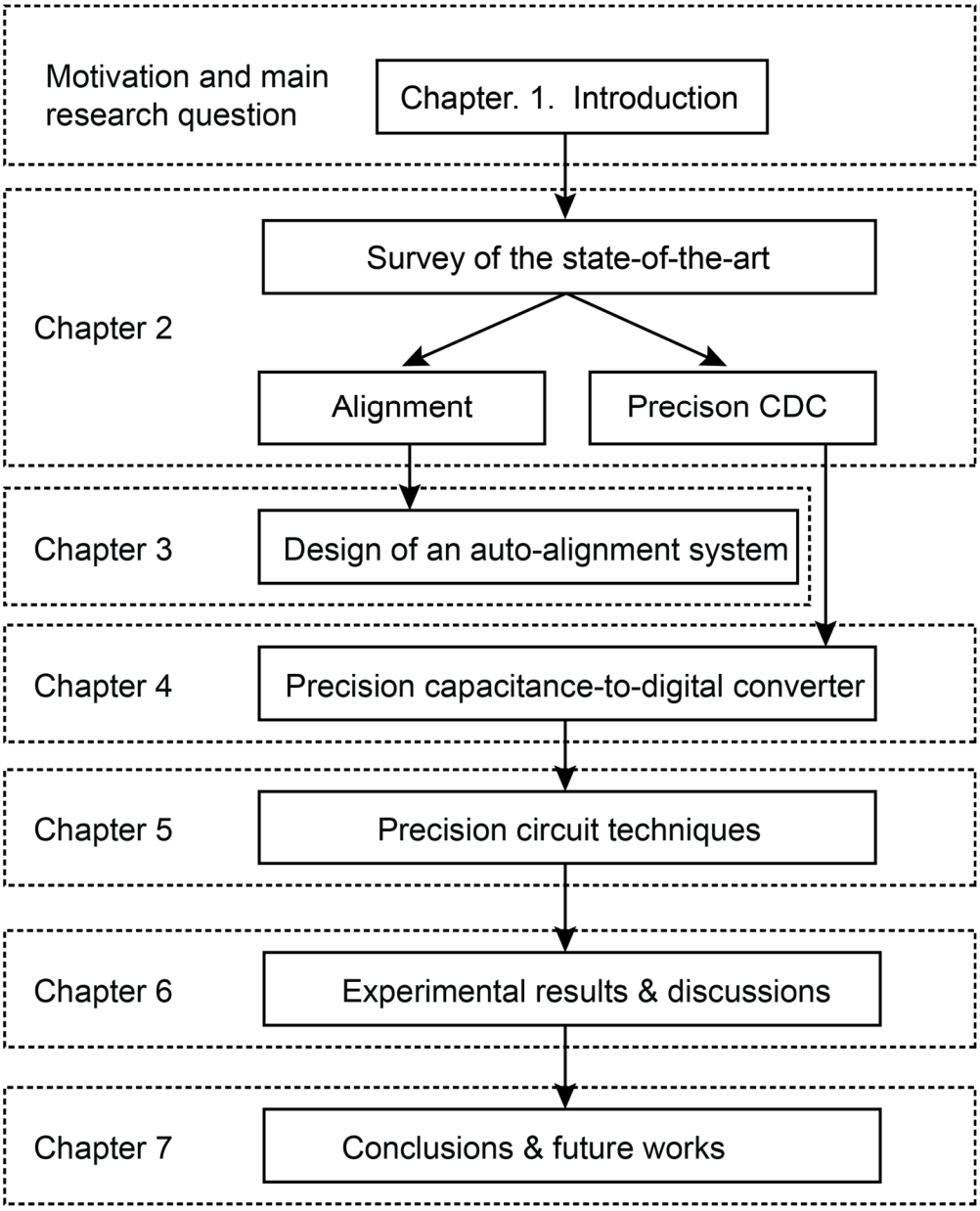

Fig. 1-3. Organization chart of the thesis

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Chapter 2

Background Overview

This chapter provides an overview and in-depth discussion of the state-of-the-art capacitive sensor systems. Specifically, some important aspects such as resolution, conversion time and power-efficiency are addressed. The advantages and limitations of existing works are discussed. The investigation is divided into three parts: 1) the capacitive sensor head; 2) capacitive sensor interface; 3) precision references for capacitance measurement. The corresponding state-of-the-art works are analysed accordingly.

2.1 Capacitive sensors

This section focuses on the investigation and performance analysis of a parallel-plate capacitive sensor head. It starts with a brief explanation of the operating principle of a capacitive sensor. Then, the important aspects of capacitive sensor are addressed. The problems and limiting factors of such capacitive sensor in high-performance applications are discussed further.

2.1.1 Operating principle of capacitive sensors

As shown in Fig. 2-1, a capacitive displacement sensor system consists of a capacitive sensor head and a capacitance-to-digital converter (CDC). The capacitive sensor converters the displacement into a capacitance change which is then digitized by the CDC.

The operating principle of a capacitive sensor is based on modulating the electric field of the sensor by a physical parameter of interest. The most sensitive way to measure small displacement is to use a parallel capacitive sensor with one of the plates being the target, while the other plate senses the displacement of the target, as shown in Fig. 2-1. The capacitance between two parallel plate is calculated as:

$$C_o = \frac{\varepsilon_o \varepsilon_r A}{d_o} \tag{2-1}$$

Where ε_o is the dielectric constant of vacuum, ε_r is the relative permittivity of the environment, A is the area of the parallel plates and d_o is the standoff distance between them. In the case of small displacement $\pm\Delta d$ (the displacement is much smaller than the standoff distance d_o), the capacitance value can be presented as:

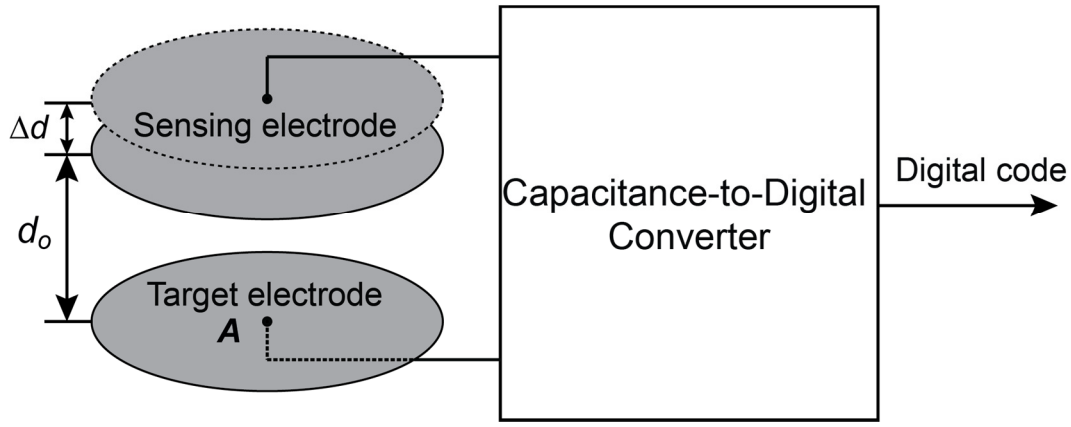


Fig. 2-1. A parallel-plate capacitive displacement sensor

$$C_x = \frac{\varepsilon_o \varepsilon_r A}{d_o \pm \Delta d_x} = C_o \pm \Delta C_x \approx C_o \mp \frac{\varepsilon_o \varepsilon_r A}{d_o^2} \cdot \Delta d_x \tag{2-2}$$

Where $\frac{\varepsilon_o \varepsilon_r A}{d_o^2}$ [F/m] is the sensitivity of the sensor. From Eq. (2-2) it is clear that the sensitivity of the sensor is inversely proportional to the square of the standoff distance d_o.

2.1.2 Alignment of the capacitive sensors

The biggest limitation of a high-performance capacitive sensor is the alignment accuracy, which reduces the sensitivity of the sensor and poses large dynamic range (DR) requirement for the succeeding capacitance to digital converter.

In practice, the standoff distance of the sensor head is usually in the range 100 μm to 500 μm [1] due to mounting and machining tolerances. According to Eq (2-2), large standoff d_o leads to *small sensitivity* of the sensor and thus poses *a strict noise requirement* on the interfacing electronics to reach the required measurement resolution.

Next to the *reduced sensitivity*, the large standoff distance also leads to *large dynamic range* requirement for the CDC. The required dynamic range (*DR*) of the CDC can be estimated as the ratio between the standoff and the minimum displacement Δd_{min} that needs to be detected:

$$DR = \frac{d_o}{\Delta d_{min}} \tag{2-3}$$

Taking the practical standoff distance (~100 μm to 500 μm) and the required measurement resolution (~ 20 pm), the required DR can be as high as 22- bit. The real dynamic range $DR_{real,}$ however, is the ratio between the maximum displacement Δd_{max} (~10 nm) and the minimum displacement Δd_{min}:

$$DR_{real} = \frac{\Delta d_{max}}{\Delta d_{min}} \tag{2-4}$$

Eventually, the required DR is only around 10-bit. Since $d_o >> \Delta d_{max}$, the system requires much higher dynamic range than it is practically needed, which means a big *waste of power*.

To improve the performance of capacitive sensors, it is desirable to improve the alignment accuracy of the sensor head, or in another word, reduce the standoff distance d_o.

Traditionally, there are three possible methods to improve the alignment accuracy:

1) Improve the fabrication quality

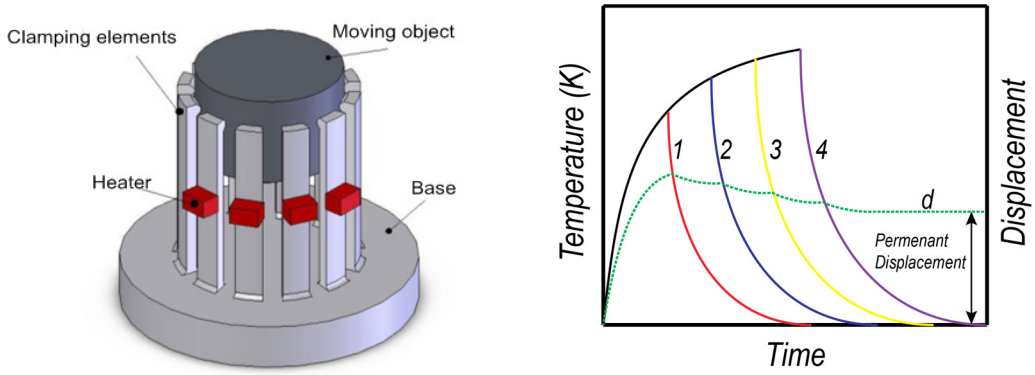
One way to improve the alignment accuracy is by machining all relevant parts with small tolerances, which significantly increase the cost of the total system. In addition to the increased cost, manufacturing parts with micrometer accuracy is not a solution for sensor systems that have to be transported in a completely assembled state, since it might experience much larger vibration which eventually destroy the sensor.

2) Perform manual alignment after sensor assembling

A more practical method to achieve good alignment accuracy and avoid collision during transportation is to perform extra manual alignment after sensor assembling. This can be done by using dedicated alignment device, such as micrometer screws. However, manual alignment also means high cost. Especially when there are a number of sensors to be aligned, this method would lead to huge inefficiency of both time and cost.

3) Incorporate self-alignment mechanism into the sensor-head

In order to reduce the cost and duration of accurate positioning, and to avoid the problem of transportation, a self-alignment mechanism can be integrated into the sensors. Then, after being assembled, the sensor can do the alignment automatically to the required level of accuracy. Examples of such positioning/alignment systems include piezoelectric actuators, electrostatic comb drives or thermal actuators. These devices can work in inaccessible environment and provide good positioning accuracy. However, they have to be operated continuously in closed-loop to maintain the position of the object being aligned. As a result, the power consumption and heat dissipation are increased, which affect the stability of the position of the aligned object. In addition, such system is relatively complex and expensive, which in turn reduces the advantages of using low-cost sensors.



(a) (b)

Fig. 2-2. (a) The thermal stepper system; (b) The corresponding qualitative temperature profile as well as the displacement of the object being aligned

2.1.3 Thermally-actuated auto-alignment system

In order to reduce the cost and duration of accurate positioning, and to avoid the problem of transportation, an auto-alignment system based on thermal actuation, called “thermal stepper” was proposed [2]. This system has several advantages compared to ordinary alignment systems: i) it is simple, cheap and reliable; ii) its alignment can be precise; iii) due to the proposed special control sequence, in contrast to conventional thermally actuated systems, the control system can be shut down after alignment, but the position will be maintained stably.

The diagram of the system is shown in Fig. 2-2 (a). Position adjustment of the sensor plate with the thermal stepper system is based on thermal actuation of the elements clamping the object. In its most simple form, four clamping elements are needed. Fig. 2-2 (b) shows the temperature profile of the four elements (1, 2, 3 and 4) and the displacement (d) profile during the operation.

The stepping action of the actuator system is created by applying heat in a special order. In the first phase all elements are heated and the moving object moves based on the thermal expansion of the clamping elements. After the initial heating, the elements are cooled down one after the other. The cooling down procedure causes the element to contract and thus shorten. Since only one element cools down at a time, the moving object is held in place by the other elements that are still heated, while the contracting element will slip relative to the surface of the moving object. After a complete step, the control system can be switched off and the new position of the electrode can be maintained stably by the clamping structure. By repeating the same control sequence, the object under alignment will be stepped to the desired position.

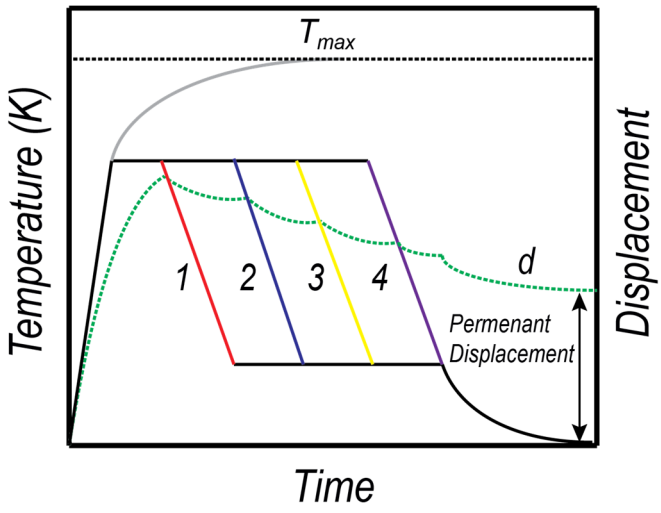


Fig. 2-3. Temperature and displacement profiles of a thermal stepper under closed-loop control (temperature of different thermal elements 1, 2, 3, 4 are marked as red, blue, yellow and purple, respectively. Displacement of the object is marked as green)

2.1.4 Control of the thermal stepper

The open-loop heating and passive cooling in Fig. 2-2 shows exponential thermal behavior. This behavior causes a very slow approaching of the elements to their final temperature. Waiting for all the elements to reach their steady-state temperature would make the system very slow; therefore the next step in the thermal cycle already starts when the temperature of some elements is still increasing or decreasing. As a result, there might be more than one element slipping at one time. Because of this, the system is very unpredictable [1, 3, 4].

To improve the predictability and the alignment speed of thermal stepper, a closed-loop control scheme can be implemented [4]. The typical temperature profile of a thermal stepper under closed-loop control is shown in Fig. 2-3. By means of closed-loop control, the temperature step T_{step} can be accurately set to any value between the initial and the maximum temperature T_{max}, which is defined by the input heating power and the property of thermal element. It can be guaranteed that every element reaches a defined temperature. This implies that every element also has a defined change in length.

As shown in Fig. 2-3, the control can be used to prevent an element from cooling down to its initial temperature. This control enables the system to cool down relatively fast, as cooling is limited to the first steep part of the exponential curve. As soon as the next element starts cooling down, the temperature of its predecessor can be fixed. This prevents two or more elements from contracting at the same time. As more elements are supporting the object, cooling only one element at time reduces the retraction of the object and thus increases the effective step size. Increased step size and decreased cycle time enable a faster movement of the system.

2.1.5 Discussion

This section discusses the basic operating principle and limitations of a parallel-plated-based capacitive displacement sensor. The performance of such sensor is greatly limited by its alignment quality. The mis-alignment leads to large standoff distance between the sensor plates. The large standoff distance significantly reduces the sensitivity of the sensor, while poses large dynamic range requirements on the succeeding interface circuits. Traditionally, the alignment accuracy can be improved by either improving the fabrication quality or performing extra alignment after sensor assembling. However, such solutions lead to high-cost as well as long working time.

By incorporating a low-cost self-alignment device into the sensor head, the alignment accuracy can be performed automatically after sensor assembling. To this end, a thermally-actuated alignment device, called "thermal stepper" has been introduced. In order to control the thermal stepper in an efficient way, a proper control system which optimizes the speed, repeatability, power dissipation and the number of connection wires is required. The details of the thermal stepper control is discussed in Chapter 3.

In the next section, the interface circuit which converts the capacitance to electrical signal will be addressed, including the possible structures and references used for the conversion. Based on the discussion, optimal selection of circuit architecture and references are discussed.

2.2 Capacitance measurement approaches

The previous section discussed the operating principle, existing problem and possible solutions of a parallel-plate capacitive sensor. In this section, the optimal interface circuit which converts the capacitance to electrical domain is discussed.

In the past decades, many principles have been investigated to measure capacitance. Regarding to the references used, two types of interfacing approaches can be distinguished:

(1) The unknown capacitor is compared with one, or a series of reference capacitors. The CDCs based on this approach give a digital representation (M) of the unknown capacitance C_x as a function of the reference capacitor C_{ref},

$$M = \mathrm{f}(C_x, C_{ref}) \tag{2-5}$$

(2) The unknown capacitor is compared with a combination of references, e.g. resistor, time, current, voltage, etc. The combination of different references generate an equivalent reference "capacitor" C_{ref}. Then this equivalent capacitor is compared with the unknown capacitor C_x by

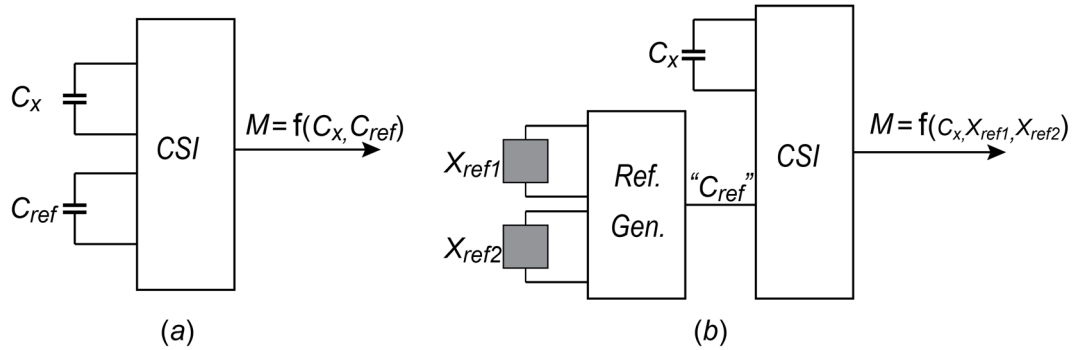


Figure. 2-4. Block diagrams of the conventional capacitance measurement approaches: (a) compare the unknown capacitance with a reference capacitance; (b) compare the unknown capacitance with a combination of references.

a CDC, as shown in Fig. 2-4(b). This way the measured capacitance C_x is a function of all the references that are used to generate the equivalent capacitance:

$$M = \mathrm{f}(C_x, X_{ref1}, X_{ref2}) \tag{2-6}$$

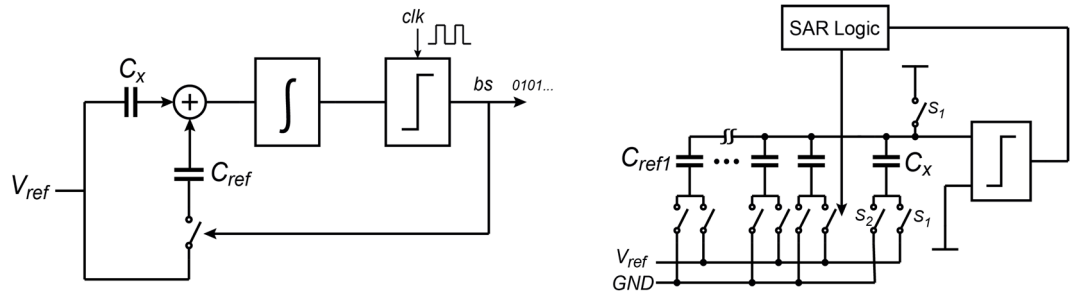
2.2.1 Comparison with Reference Capacitor

The most straightforward way of measuring a capacitance is comparing it with a reference capacitance. The CDCs based on comparison of the unknown capacitance with a reference capacitance can be either a *direct conversion* or an *indirect conversion* type.

1) Direct capacitance-to-digital conversion

When a CDC digitizes the signal by directly incorporating the unknown capacitor C_x and reference capacitor C_{ref} in an ADC block (Fig. 2-5(a)), it is referred as a *direct converted* CDC. Examples of such works include switched-capacitor (SC) Delta-Sigma based CDCs [5-9] (Fig. 2-5(a)) and successive approximation (SAR) based CDCs [10-12] (Fig. 2-5(b)) in which both capacitors are directly included in the ADC block by taking advantage of the charge-balancing/charge-redistribution nature of such ADCs. By applying the same reference voltage to both capacitors, the comparison is done at charge domain and the exact value of V_{ref} does not affect the comparison result. The output digital code is a representation of the ratio between the unknown capacitance C_x and the reference capacitance C_{ref}.

The Delta-Sigma modulator based CDC (shown in Fig. 2-5(a)) is based on charge-balancing: the charge that is supplied by the unknown capacitor C_x is balanced by the



(a) (b)

Fig. 2-5. CDCs based on direct comparison with reference capacitor: (a) Delta-Sigma modulator based CDC; (b) Successive-Approximation (SAR) based CDC.

charge which is supplied by the reference capacitor C_{ref}. At each clock cycle, a charge that is proportional to C_x is integrated by the integrator. The change of the integrator is monitored by a comparator, which controls the reference capacitor C_{ref} to supply a compensation charge (opposite sign) and produces a digital bitstream. By operating the loop for enough cycles *N*, the accumulated charge of the integrator is approximately zero, meaning that the charge from C_x is balanced by the charge from C_{ref}. This can be expressed as:

$$N \cdot V_{ref} \cdot C_x = N_1 \cdot V_{ref} \cdot C_{ref} \tag{2-7}$$

Where N_1 represents the number of '1's of the comparator output bitstream. The above equation can be rewritten as:

$$\frac{C_x}{C_{ref}} = \frac{N_1}{N} \tag{2-8}$$

This shows that the fraction of ones ('1') in the bitstream represents the ratio of C_x and C_{ref}. Hence known the value of C_{ref}, the capacitance C_x can be obtained by simply counting the number of ones in the output digital bitstream.

The SAR-based CDC (shown in Fig. 2-5(b)) works in two steps. The first step is the "sampling" step: the input of the comparator is shorted to ground (GND), and C_x is tied to the reference voltage V_{ref} while the reference capacitor array is connected to ground. Then, the charge stored on capacitors can be derived as:

$$Q_x = V_{ref} C_x \tag{2-9}$$

$$Q_{ref,tot} = 0 \tag{2-10}$$

Where Q_x is the charge stored in the unknown capacitor C_x, $Q_{ref,tot}$ is the charge stored in the reference capacitor array. During the sampling phase, the charge in the reference capacitor array $Q_{ref,tot}$ is set to zero.

The second step is the "conversion" step. The switch connected to the input of comparator is turned off. Then, a SAR logic selects one capacitor from the reference capacitor array at each clock cycle and compare it with the unknown capacitor. The selection and comparison is successively performed from the largest capacitor (MSB) to the smallest one (LSB). At the first cycle, the selected capacitor ($C_{ref,MSB}$) is switched to the same reference voltage. Thus due to the charge conservation, the voltage at the input of the comparator becomes:

$$V_x = V_{ref} \frac{C_{ref,MSB} - C_x}{C_{ref,MSB} + C_x} \tag{2-11}$$

Depending on the sign of V_x, the corresponding digital bit (MSB) is determined as '1' (when $V_x < 0$) or '0'(when $V_x > 0$). If MSB is '1', the MSB capacitor keeps the connection to V_{ref} for the remaining conversion cycles. If MSB is '0', the MSB capacitors is again connected to ground for the remaining conversion cycles. Then, in the next clock cycle, the next lower bit capacitor is selected and the same operation is performed. The conversion continuous until the least-significant bit (LSB) is defined [11]. In the end, the input voltage of the comparator can be estimated as:

$$V_x = V_{ref} \frac{\sum_{n=1}^{N} D_n C_{ref,n} - C_x}{\sum_{n=1}^{N} D_n C_{ref,n} + C_x} \tag{2-12}$$

Where D_n indicates the digital codes of the nth bit and $C_{ref,n}$ is the capacitance of nth bit. Ideally, the voltage V_x is approximately zero when the conversion finishes, meaning that the sum of the non-zero bits capacitors equals to the unknown capacitor C_x. Thus, the capacitance can be calculated as:

$$C_x = \sum_{n=1}^{N} D_n C_{ref,n} \tag{2-13}$$

2) Indirect capacitance-to-digital conversion

In many cases, the unknown capacitor is first converted to another unit (e.g. voltage, frequency, etc). Then it is digitized by a conventional analog-to-digital converter (ADC) or time-to-digital converter (TDC), as shown in Fig. 2-6. Although extra components are introduced during the conversion, the final result is still a function of C_{ref} only, due to the ratio-metric measurement. This type of CDC is referred as an indirect-compared CDC. With an indirect-compared CDC, the front-end circuit and the ADC can be optimized according to the practical requirements, which result in superior power efficiency [11].

Fig. 2-6 shows two most commonly used structures. The first one is based on a capacitance-to-voltage converter (CVC) followed by a conventional analog-to-digital converter (ADC) (shown

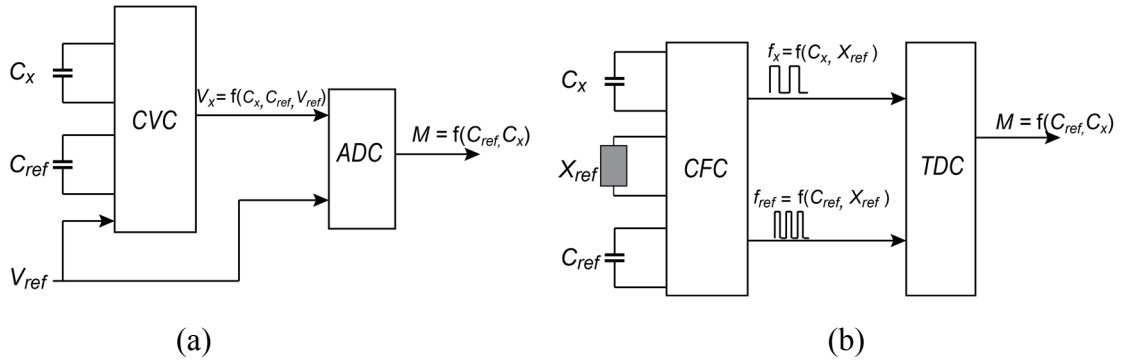


Fig. 2-6. CDCs based on indirect comparison with reference capacitor: (a) Capacitance-to-voltage converter followed by ADC; (b) Capacitance-to-frequency converter followed by TDC.

in Fig. 2-6(a)). In such CDCs, the unknown capacitance is first converted to a voltage signal by a CVC. The most commonly used CVCs are classified into two categories: switched-capacitor (SC) CVCs [13, 14] and continuous-time (CT) [15-19] CVCs with synchronous demodulation. Both techniques required an extra reference capacitor Cref and voltage V_{ref} to perform the capacitance-to-voltage (C-V) conversion. The output voltage of a CVC is a function of the unknown capacitance C_x, the reference capacitance C_{ref} and the reference voltage V_{ref}, as shown:

$$V_x = \mathrm{f}(C_x, C_{ref}, V_{ref}) \tag{2-14}$$

After the capacitance-to-voltage (C-V) conversion, the voltage signal is digitized by a conventional ADC [15-17, 20, 21], which use the same reference voltage as the CVC. Depending on the practical requirements, suitable ADC structures can be selected for optimal performance. The final result is a digital representation of the unknown capacitor as a function of the reference capacitor C_{ref}:

$$M = \mathrm{f}(C_x, C_{ref}) \tag{2-15}$$

The second type of an *indirect-compared* CDC is based on a capacitance-to-frequency converter (CFC) which converts both the unknown capacitance C_x and the reference capacitance C_{ref} into frequency/time signals (shown in Fig. 2-6(b)):

$$f_x = \mathrm{f}(C_x, X_{ref}) \tag{2-16}$$

$$f_{ref} = \mathrm{f}(C_{ref}, X_{ref}) \tag{2-17}$$

The conversion requires an extra reference component X_{ref}, which can be either resistor or inductor. In most of the CMOS compatible designs, resistor is used for the conversion [15, 20, 21]. After the capacitance-to-frequency (C-F) conversion, these two frequency signals are compared in a time-to-digital converter (TDC), which generates a digital representation of the unknown capacitance as a function of only the reference capacitance, as shown in Fig. 2-6(b). Because both the capacitors use the same reference for C-F conversion, the final result is not dependent on the extra reference used. The advantage of such solution is that the analog frontend doesn't have to be close to the TDC, because it produces semi-digital signals which

can be transferred in a relatively noisy environment without degrading the performance [21-23]. The TDC is usually implemented as a simple counter in a microcontroller [21, 23, 24].

2.2.2 Comparison with combination of references

As introduced earlier, a second category of capacitance measurement approaches is based on comparing unknown capacitance with a series of references whose combination generate an equivalent "capacitance". Finally, the measured result is a function of the references employed, as shown in Eq. (2-6).

1) Combination of frequency and resistive references ($C_{ref} = \frac{1}{f_{ref} R_{ref}}$)

The combination of a time reference and a resistor reference generates an equivalent capacitor whose value is $C_{ref} = \frac{1}{f_{ref} R_{ref}}$. There are two methods to measure a capacitance by comparing it with this equivalent capacitor. As shown in Fig. 2-7(a), the first method is based on an amplitude-modulated circuit. With a resistor reference and an AC excitation source, the modulator circuit (normally an active RC integrator [23, 25, 26]) generates a modulated signal whose amplitude is a function of the excitation frequency f_{ref}, the amplitude of the excitation signal V_{ref}, the unknown capacitor C_x and the resistor reference R_{ref} [27], written as:

$$\widetilde{V_x} = \mathrm{f}(C_x, R_{ref}, f_{ref}, |V_{ref}|) \tag{2-18}$$

This signal, together with the excitation signal, is feed into a demodulation circuit and then an ADC. The digital output of the ADC represents the unknown capacitor C_x as a function of the resistor and the time references, or in another word, the equivalent capacitance generated by the combination of the two:

$$M = \mathrm{f}(C_x, f_{ref}, R_{ref}) \tag{2-19}$$

Another method of comparing capacitance with resistor and time references is based on oscillator circuit, which generates a time-domain signal (frequency, pulse-width or phase shift) that is proportional to the unknown capacitance C_x, expressing as:

$$f_x = \mathrm{f}(f_{ref}, R_{ref}) \tag{2-20}$$

The most common way to realize an RC-oscillator is in the form of a relaxation oscillator [27]. The output signal of the oscillator can be either period/frequency [27] or pulse-width [28-30], depending on the implementation of the oscillator. The RC relaxation oscillator can be implemented by only a few digital logics which is compact and low power [31]. However, it

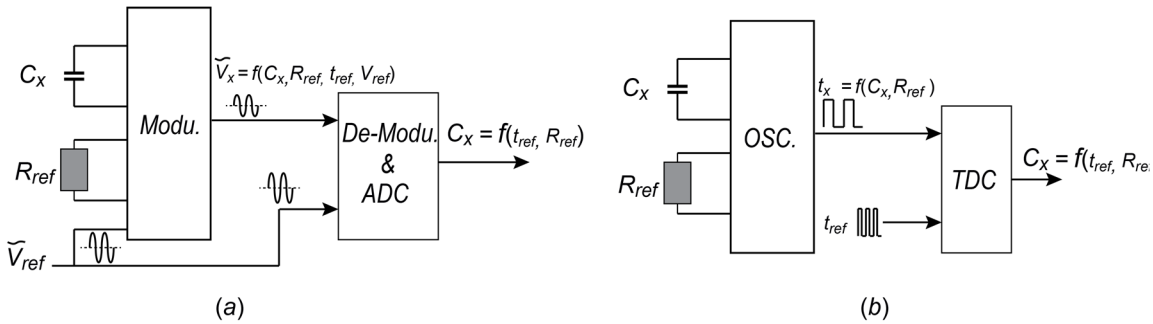


Fig. 2-7. CDCs based on comparison with combination of resistor and time/frequency references: (a) based on amplitude modulation; (b) based on oscillator circuit followed by a TDC

suffers from parasitic associated with both the sensor and the references, e.g. the oscillation frequency is highly depends on the shunting capacitance and resistance. Although different shielding techniques have been proposed to reduce the parasitic effect [32], it shows stability-accuracy trade-off [33]. Therefore, such implementation is usually applied in applications where the precision requirement is relaxed but the power budget and the volume is strictly limited. To boost the performance of the circuit, the oscillator usually employs active components, e.g. integrator, whose virtual ground suppress the effect of parasitic [26, 34, 35].

The output time-domain signal (e.g. period, pulsewidth, etc) of the oscillator is compared with a reference frequency/time signal by a TDC, which, in most cases can be implemented by a simple counter [36]. Eventually, the output of the TDC provides digital information of the capacitance as a function of the combination of the time and resistor references, as shown in Eq. (2-20). Because of the semi-digital feature of the oscillator output, the converted signal can be transmitted through noisy environment and interfaced by simple digital circuitry.

2) Combination of frequency, voltage and current references ($C_{ref} = \frac{I_{ref}}{f_{ref} V_{ref}}$)

The resistive reference shown in Fig. 2-7 can be replaced by a combination of voltage and current references, whose ratio equivalents to a resistance. Design examples based on this combination includes relaxation-oscillator-based interface [28, 33, 34, 37] or capacitance-controlled-oscillator (CCO) based circuit [38, 39]. As shown in Fig. 2-8(a), the relaxation-oscillator-based design usually employs charge-balancing principle. A switched current source I_{ref} replaces the resistor in an RC relaxation oscillator. The switching of this current source is controlled by the output of the oscillator. The charging by the reference voltage V_{ref} results in a voltage jump which is detected by the relaxation oscillator. Once the voltage is across a threshold, the oscillator controls the current reference to discharge the capacitor until the threshold is crossed again. This charging and dis-charging operation generates a time-domain signal (normally a period-modulated signal) at the output of the relaxation oscillator, which is a function of the unknown capacitance, reference voltage and the reference current, as shown:

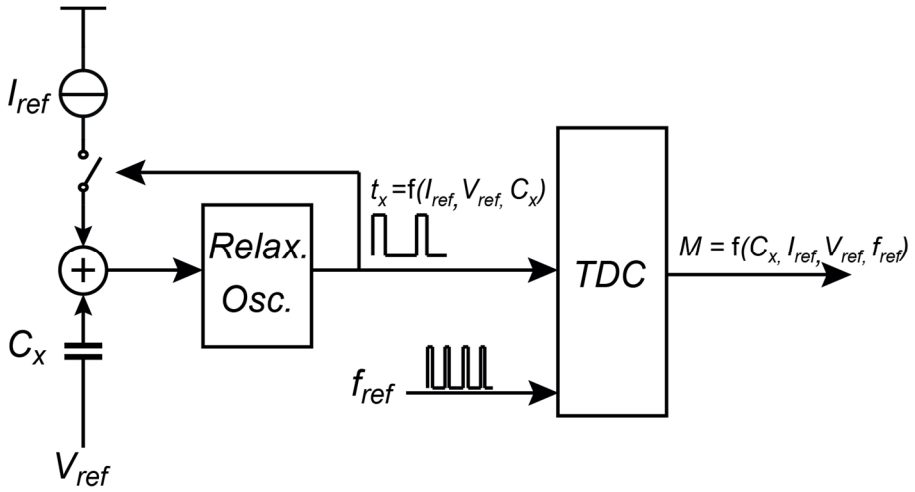
$$f_x = \mathrm{f}(I_{ref}, V_{ref}, C_x) \tag{2-21}$$

A TDC followed by the relaxation oscillator digitizes this signal by comparing it with a reference frequency source f_{ref}, which results in a capacitance measurement result depends on the combination of a current reference, a voltage reference and a time reference :

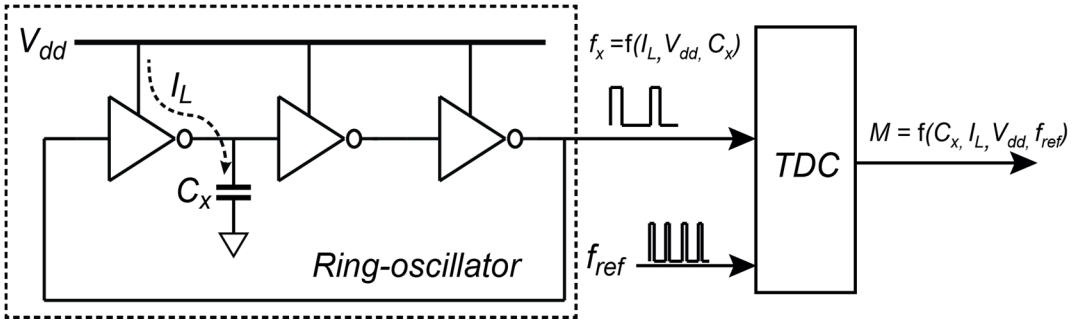
$$M = \mathrm{f}(C_x, I_{ref}, V_{ref}, f_{ref}) \tag{2-22}$$

In practice, the relaxation oscillator can be implemented in different ways, depending on the required performance. In [28, 34, 37], the relaxation oscillator is built around a comparator and a few digital logics, which provides very low power and compact solutions. However, for better immunity for the parasitic and higher resolution, active integrator is usually added to the charge-balancing frontend [21]. The active integrator usually implemented as a Gm-C integrator. Since both paths (charging and discharging) share the same integrator, the extra capacitance in the integrator doesn't play any role in the final measurement results.

For very low-voltage and low-power applications, the CDCs can be designed around a ring-oscillator [38, 39] followed by a TDC, as shown in Fig. 2-8(b). By incorporating the unknown capacitance into the ring-oscillator loop as a load capacitance for charge integration with precisely controlled current source, the ring-oscillator produces a period/frequency output



(a) Relaxation-oscillator-based interface



(b) Ring-oscillator-based interface

Fig. 2-8. CDCs based on comparison with the combination of a current reference, a voltage reference and a time reference.

signal whose frequency is determined by the combination of the supply voltage V_{dd}, the load current of the ring-oscillator I_L and the unknown capacitance C_x:

$$f_x = \mathrm{f}\left(I_{L,} V_{dd}, C_x\right) \tag{2-23}$$

The TDC after the ring-oscillator provides digital output of the measured capacitance as:

$$M = \mathrm{f}(C_x, I_L, V_{dd}, t_{ref}) \tag{2-24}$$

Unfortunately, the high sensitivity to parasitic and process variation limit such solution to relatively low-precision applications.

3) Combination of frequency and inductive references ($C_{ref} = \frac{f_{ref}}{L_{ref}}$)

It is also possible to build a reference capacitor using the combination of an inductive reference L_{ref} and the frequency reference f_{ref}. The most common method to do so is via an LC-oscillator [33, 40-42], which generates an output frequency signal that is proportional to the capacitance C_x and the reference inductance L_{ref}. The frequency signal produced by the LC oscillator can range from several hundred kHz to a few GHz , because it is insensitive to the loss component around C_x. This feature facilitates the measurement of capacitances with high loss materials [33].

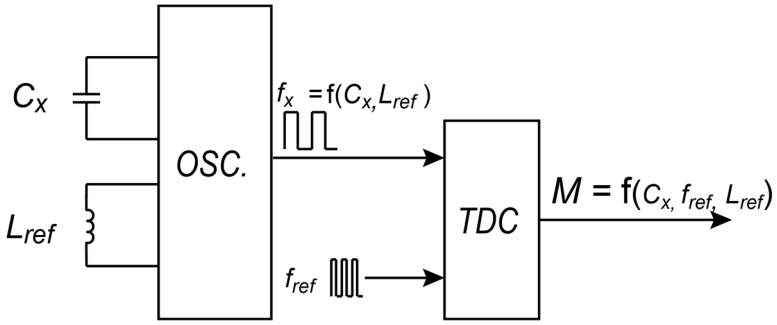
To digitize the output of the LC oscillator, a counter-based TDC is implemented in [42], which counts the period of the oscillation signal and provide a digital information of the oscillation frequency, as shown in Fig. 2-9 (a). While, for better accuracy and power-efficiency, [40, 41] implement a phase-lock-loop (PLL) frequency synthesizer, which tracks the frequency shift of the LC oscillator and converts it into a voltage change that can be digitized using an on-chip ADC. As a result, the digital output is a representation of the fluctuation of the capacitance.

The block diagram of such solution is shown in Fig. 2-9(b). First ignore the control voltage V_c, the voltage-controlled LC-oscillator generates a frequency signal that is proportional to the reference inductance L_{ref} and the unknown capacitance C_x:

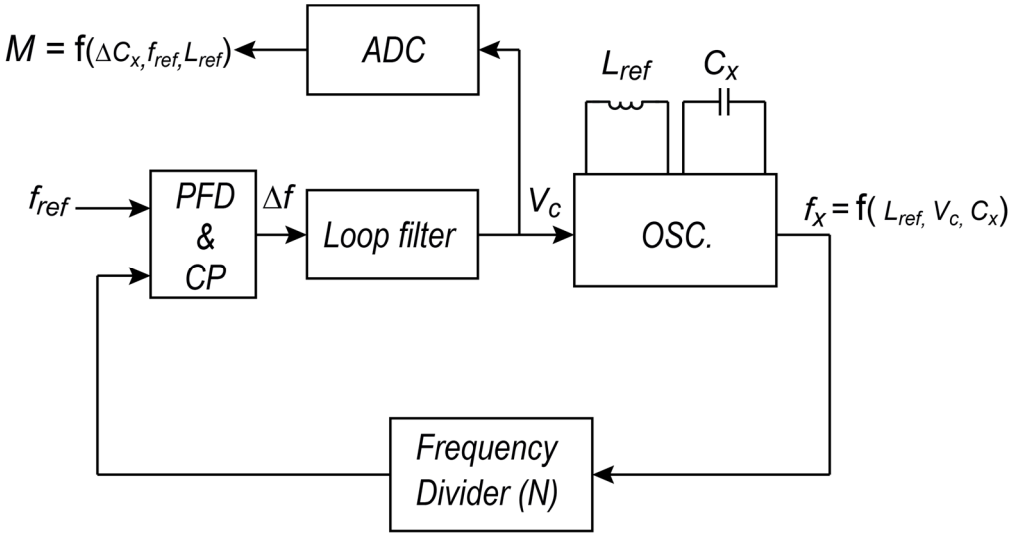
$$f_x = \frac{1}{L_{ref} C_x} \tag{2-25}$$

This frequency signal feed into a phase and frequency detector (PFD) after scaling by a frequency divider. The PFD applies a reference clock signal f_{ref}, and produces an output that is the difference between f_x and f_{ref}. After that, the frequency difference generates a change of the control voltage V_c via a charge-pump (CP) circuit. Then, the control voltage tunes the oscillation frequency of the LC-oscillator by controlling the varactors in the oscillator [40]. In the end, the synthesizer loop adjusts the control voltage Vc so that the oscillation frequency of the LC-oscillator is locked to the reference frequency:

$$f_x = N \cdot f_{ref} \tag{2-26}$$



(a) LC-oscillator digitized by a TDC



(b) LC-Oscillator included in a PLL frequency synthesizer

Fig. 2-9. CDCs based on comparison with the combination of a frequency/time reference and an inductance reference

In this case, the control voltage V_c is a function of the unknown capacitance C_x. Digitizing the control voltage by a traditional ADC gives the information about C_x, as a function of the inductance reference and the frequency reference.

The solution with LC-oscillator is favorable in chemical and bio-material applications, as many chemical properties show large sensitivity at RF/Microwave frequencies [40, 41]. The capability of an LC-oscillator to cover high oscillation frequencies makes it an ideal solution for such applications. In industrial applications, where the physical changes such as displacement and acceleration have to be detected, going for very high frequency results in a waste of energy.

2.2.3 Comparison and discussion

In Fig. 2-10, the performance of the capacitance-to-digital converters discussed in the previous section are summarized and plotted as a function of their effective-number-of-bit (ENOB) and the conversion time. The conversion principle include two groups. The first group, including

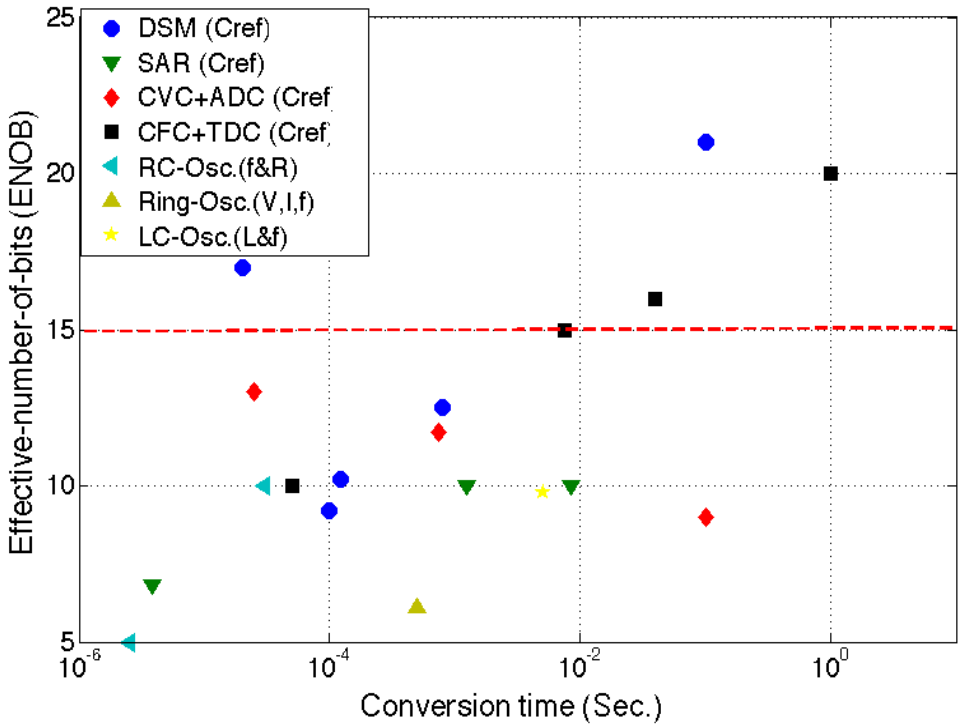


Fig. 2-10. Survey of the performances of state-of-the-art capacitance-to-digital converters

direct and indirect comparison type, consist of direct delta-sigma modulator (DSM) [5-9], direct successive approximation (SAR) [10-12], capacitance-to-voltage converter (CVC) followed by ADC [15-17], capacitance-to-digital converter (CFC) followed by TDC [21, 23, 24]. All of them are based on comparison of the unknown capacitor with a known reference capacitor. The second group is based on the comparison with a combination of different references, which generate an equivalent reference capacitor. The combinations include: combination of time and resistor references [31, 43], combination of voltage, current and time references [38], combination of inductor and time references [40].

From the plot, delta-sigma based designs cover wide application range from medium resolution (~ 10-bit) to high resolution (21-bit). At the medium resolution range, designs based on this principle show medium conversion speed compare to that of the other principles. At high resolution range, it shows clear speed advantage compare to its CFC-based counterpart.

The SAR CDCs are mainly used for low to medium resolution (< 10-bit) applications, due to their intrinsic matching issue. Such structure also reports medium conversion speed in this range.

The indirect-comparison type CDC, as discussed in the previous section, includes two groups of structures: capacitance-to-voltage converter (CVC) followed by ADC and capacitance-to-frequency converter (CFC) followed by TDC. The former one is usually designed for medium resolution applications, since the C-V conversion introduces extra noise. The CFC structure, however, can be extended to high-resolution applications, because the semi-digital property of such converters, which provide better immunity to noise and interferences.

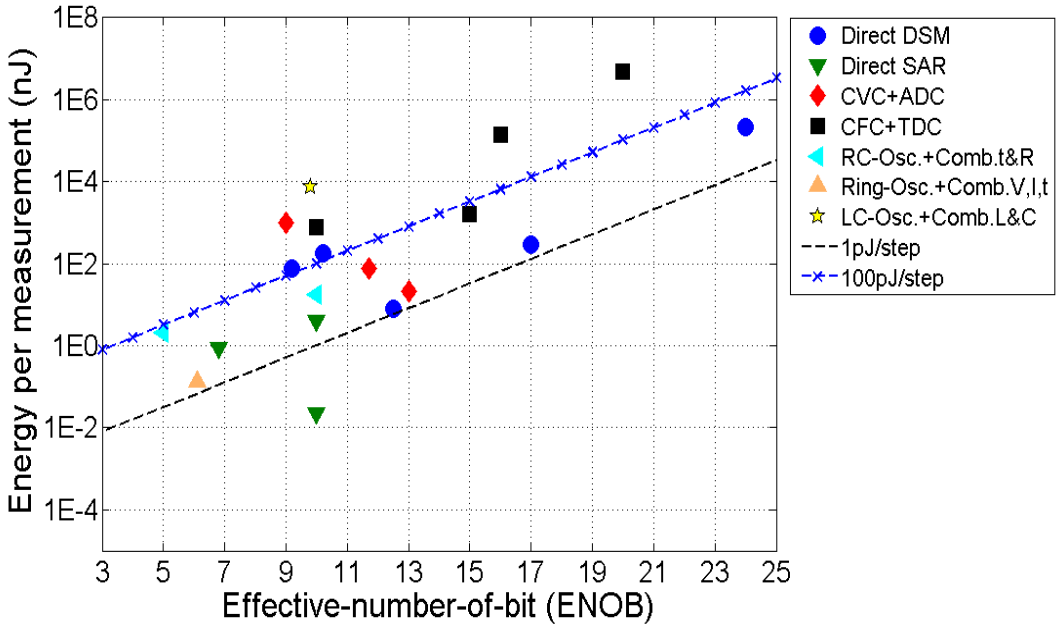


Fig. 2-11. Survey of the energy efficiency of state-of-the-art capacitance-to-digital converters

The works based on comparison with combination of different references are all located in low to medium resolution range (< 10-bit), as the existing works are mainly based on oscillator circuits which are very sensitive to parasitic influence. Moreover, their performances are further limited by the succeeding TDC.

Fig. 2-11 shows the energy consumption of the above discussed designs as a function of their ENOBs. For a reference purpose, two lines corresponding to Figure-of-Merits (FoMs) of 1 pJ/step and 100 pJ/step are also shown. The designs which sit closer to the reference FoMs are regarded as more power efficient.

It is clear that the direct delta-sigma based CDCs achieve good power-efficiency compare to its counterparts at all the resolution range, especially at high resolution range. The CFC-based converters, although reported high resolution, are more power hungry. The CVC-based CDCs can also achieve good power-efficiency, because optimal power budget can be made for the CVC and ADC separately. The best FoM belongs to SAR-based CDCs, while all the designs are in low to medium resolution region. It is also noticeable that most of the oscillator-based designs are power efficient, because of their simple structures. The only exception is the LC-oscillator based circuit, thus it is only used in specific applications as discussed earlier.

As a conclusion, both of the delta-sigma based CDC and the CFC-based CDC could achieve the required resolution, while the delta-sigma CDC wins in terms of power efficiency.

2.2.4 Conclusion

This section provides an overview of possible methods of measuring and digitizing an unknown capacitance. The capacitance measurement is based on comparing the unknown capacitance

with a known reference. The reference can be either a reference capacitor or a combination of other references (e.g. resistor, voltage, frequency, etc), which generates an equivalent reference capacitor. Circuit structures which utilize those references are investigated and compared in terms of their resolution, conversion time and power efficiency. The results provide good basic for selecting optimal interface circuit according to practical requirements.

In the next section, the performances of varies references that can be used for capacitance measurement will be discussed in detail. Specifically, more focus will be on the important features such as stability and accuracy.

2.3 Precision references

In previous section, the possible methods and combinations of references for measuring a capacitance are discussed in detail. This section focuses on an investigation of these references in terms of their qualities, such as stability, aging, tolerance and accuracy, which are important for precision capacitance measurement.

From the discussion above, it is clear that capacitance measurement is based on comparing the unknown capacitance with a reference capacitance or an equivalent reference capacitance that is built from the combination of other references, e. g. resistor, voltage, frequency, etc. The ultimate precision of the measurement, is thus determined by the quality of the references used. Of course, the circuit that performs the comparison also limits the achievable performance of the measurement. In this section, various references will be discussed in terms of their precision, stability, volume and price, which are the most important specifications for industrial high-precision industrial applications. After that, the interface circuits using these reference will be briefly addressed so that the limitation of the specific circuit is analyzed. Finally, the best possible references with good quality while facilitate the use of high precision circuitry is chosen for the design.

As discussed in the previous section, there are many ways to construct a reference capacitor for the measurement of an unknown capacitor. The most straightforward way is to directly use a reference capacitor whose capacitance is accurately known. Besides, it is also possible to build an equivalent capacitor using different combinations of references, as shown in the Section. 2.2. Those references include: resistor, time/frequency, inductor, voltage and current. In this section, the properties of those references are discussed in detail, with focus on the precision and stability. In the end, a discussion about the optimal selection of references and interfacing structure which leads to the required performance is made.

2.3.1 Capacitive reference

Capacitors can be divided into discrete and integrated types, each of them contains many sub-categories. The different discrete capacitors got their names from the dielectric material used,

which, to the most extent determines the quality of the capacitor. The most-commonly used discrete capacitors include ceramic, film, airgap and vacuum type of capacitors. Among each of these groups, further classifications are made according to the mixtures of their dielectric material and their performances. For instance, a ceramic type of capacitor is further classified to three classes based on their ceramic mixtures and performances [44]. Film capacitor is further divided according to their film materials which result in different properties for different applications [45].

As discussed earlier in Chapter 1, the most critical requirements for the target application is precision and stability, hence in this section only those classes who provide best precision and stability are discussed. Table. 2-1 lists the typical specifications of different discrete capacitors available in the market.

Table. 2-1. Benchmark of possible capacitance references

Type of capacitor	**Temperature coefficient (ppm/^{O}C)**		**Tolerance (%)**	**Volume**	**Aging**
	Typical	**Tolerance**			
Ceramic (NP0) [46]	0	± 30	> 2	Small [5]	< 0.1 %/life time[1]
Film (PP) [45]	± 40	N/A	> 2	Small [5]	1000 ppm/2 years [2]
Air gap [47]	30	N/A	0.1	Large [5]	< 300 ppm/year
Capacitance standard [48]	2	± 2	±0.005	Large [5]	< 20 ppm/year
PIP capacitor [3]	30	N/A	> 0.1 [4]	Integrated	N/A
MIM capacitor [3]	30	N/A	>0.1 [4]	Integrated	N/A
Lampard capacitor [49]	18	N/A	N/A	Medium [5]	N/A

[1] The NP0 capacitors do not experience ferroelectric aging. But environmental influences such as higher temperature, high humidity and mechanical stress can, over a longer period of time, lead to a small irreversible decline in capacitance, sometimes also called aging[44].

[2] Film capacitors may lose capacitance due to self-healing processes or gain it due to humidity influences. Typical changes over 2 years at 40 °C is ±1 % for PP film capacitors [45].

[3] The integrated capacitor here refers to AMS 0.35µm CMOS process. But the specifications with other process do not differ too much

[4] The precision of the integrated capacitors is highly depends on their matching. As a rule of thumb, 0.1% matching is almost the best one can achieve with careful layout and large enough capacitors.

[5] Small volume means the reference can be soldered on a small PCB. Medium volume can be also adapt to the PCB, but occupies relatively large area. The large volume refers to those who are much larger compared to the available space.

For ceramic capacitor, the NP0 type capacitor reports the highest temperature stability, which is around 0 ppm/^{O}C with a tolerance of ± 30 ppm/^{O}C in the military temperature range [44]. Among different types of film capacitors, the polypropylene (PP) film capacitor achieves the best temperature coefficient of ± 40 ppm/^{O}C [45]. But both types of the capacitors cannot achieve better than 2 % tolerance from sample to sample. The best available air-gap capacitor reference reports around 30 ppm/^{O}C temperature coefficient, 0.1 % precision and < 300 ppm/year drift. However, it is bulky and expensive [47]. Similarly, the GenRad 1404 series primary capacitance standard [48] shows very good thermal stability (2 ppm/^{O}C± 2 ppm/^{O}C drift) , excellent precision (± 5 ppm) and below 20 ppm /year drift. But it is again huge in size and costly .

The integrated capacitors are named after their specific constructions. For instance, the MIM capacitor is referred as a capacitor that is built on a sandwich structure of Metal, Insulator (SiO_2) and Metal, while the PIP capacitor is based on a Polysilicon-Insulator (SiO_2) -Polysilicon structure. The difference on the construction of the capacitors result in different properties of the capacitors. Both types of the capacitors report nearly 30 ppm/^{O}C temperature coefficient [50].

In [51], Thompson and Lampard show that if we have a cross-section of a conducting line-symmetric cylindrical shell which is divided into four parts, the cross-capacitance between two opposing cylinders depends only on the length of the cylinder and the permittivity of the dielectric. This type of capacitors are usually referred as the *Thompson and Lampard cross-capacitors*, which is usually used as stable and accurate capacitance standard [52]. In [49], a PCB realization of the similar structure shows 18 ppm/^{O}C drift of the cross-capacitance.

2.3.2 Resistive reference

The value of resistor does not only depend on the geometry of the resistor, but also its material properties. This gives the opportunity to make high precision resistors by properly designing the resistive pattern and selecting suitable material. In general, there are two main technologies for the design of high precision resistor. One is based on bulk metal foil, while the other one is based on thin film.

Resistors based on bulk metal foils are often used in ultra-precision applications. Its ultra-high stability is achieved by a sandwich construction of metal foil glued on a ceramic substrate. When the complete structure heats up, the foil is mechanically compressed by the substrate, which compensates for the positive temperature coefficient (TCR) of the foil [53]. Recent released products report sub-ppm/K temperature drift and below 0.01 % tolerance, which demonstrate superior performance compare to other types of resistors [54]. However, the stability under changing humidity or mechanical stress is not nearly as good, which requires careful (hermetic) packaging.

Thin film is another popular technology for precision resistors, which starts with a lithographic NiCr pattern and then uses a high temperature treatment to get low TCR. Moreover, a multi-

step digital trimming is performed to get the required accuracy. Comparing with the metal foil resistor, thin film shows somewhat lower stability and worse precision. However, it can be used to make precision resistor with much lower price and make high stability miniature chips or large resistance products, both are unpractical with metal foil resistors [53].

Another important specification is the long-term stability, which indicates the drift of capacitance with time. For many inaccessible industrial applications, replacing or calibrating the sensor system frequently is not very practical. Hence the long-term stability has to be considered.

Table 2-2 is a benchmark of the recently released resistor references where the above important parameters are taken into account.

Table. 2-2 Benchmark of possible precision resistor references

	Type	**R-range (MΩ)**	**Max. TCR (ppm/^{O}C)**	**Tolerance (%)**	**Long-term[1] drift**
VPG Z201[54]	Metal foil	< 0.1	0.8	0.005	50 ppm/2000 hours
VPG VHA412Z [55]	Metal foil	< 0.1	2	0.001	2 ppm/6 years
Alpha MP/MQ [56]	Metal foil	< 0.03	5	0.05	5 ppm/10000 hours
Vishay PLT [57]	Thin film	< 2	5	0.01	10 ppm/year
Vishay UMA0204[58]	Thin film	0.11 to 0.332	5	0.02	50 ppm/8000 hours[2]
VPG TCB [59]	Thin film	0.11 to 1	2	0.02	20 ppm/10000 hours

[1] *The long-term drift is specified at 25^{O}C without power loading of the resistor unless explicitly mentioned*

[2] *The drift is tested at 70^{O}C with maximum power load*

2.3.3 Frequency reference

Based on the mechanism of the frequency signal generation, frequency/time reference can be classified into many types, including crystal oscillator, silicon MEMS based oscillator, LC oscillator, RC oscillator, ring oscillator, and recently developed mobility-based [50] or thermal-diffusivity-based oscillators [60].

The most commonly used frequency/time reference is the quartz crystal oscillator which dominants the frequency reference market for decades [60]. It makes use of the mechanical resonance of piezoelectric material to create very precise and stable reference

signal. The commercial available crystal covers frequency range from a few tens of kilo-hertz to tens of mega-hertz while providing various levels of accuracy and stability. For instance, a temperature-compensated crystal oscillator (TCXO) provides accuracy in the 0.1 ppm to 5 ppm range [60] while having a temperature coefficient of sub-ppm/^{O}C over large temperature range [61].

The RC oscillator can be designed as either linear oscillator or non-linear oscillator. The linear oscillator generates sinusoidal output signal with a frequency selection feedback network (in this case, the RC network) and an active device to maintain the loop gain at unity. The oscillation frequency is determined by the RC product. Its precision is limited by the variations of the absolute values of the RC product and their drift due to environment change. Normally, such oscillators work in a frequency range from hundreds of kHz to a few MHz with intermediate precision (~1 % after the temperature compensation [60]) A nonlinear oscillator, on the contrary, is usually implemented using non-linear devices, such as comparator and Schmitt trigger [50]. Such oscillator produces a digital square-wave output signal, whose frequency is proportional to the RC time constant. The reported nonlinear RC oscillators can range from hundreds of kHz to a few tens of MHz. However, due to its sensitivity to the non-idealities of the non-linear devices, such oscillator also reports relatively low precision [60].

A ring oscillator is usually implemented as a circular chain of an even number of cascaded inverters (Fig. 2-12). Due to the small propagation delay of the digital inverter element, the ring oscillator can achieve very high oscillation frequency. The frequency is defined by the supply voltage, output current and the load capacitance of individual inverters, as shown in Eq. (2-21). Despite its advantage of high oscillation frequency, the ring oscillator is very sensitive to process, voltage and temperature variations [50, 60]. Hence it requires many compensation schemes to achieve an intermediate precision [62].

The LC-oscillator is usually built around a cross-coupled oscillator, whose oscillation frequency is defined by the LC tank, as shown in Fig. 2-12(a). The active circuit compensates for the losses of the tank and sustains the oscillation. Normally it is implemented as a cross-coupled transistors (Fig. 2-12(b)) which generate a negative impedance equal to $-\frac{1}{g_m}$ (g_m is the equivalent trans-conductance of the cross-coupled transistors). As mentioned earlier, the LC-oscillator is especially popular in RF range of frequencies [33, 60]. For low frequency applications inductors are expensive and impractical, especially for low cost sensor systems. The precision of LC-oscillator is highly limited by the process and temperature dependency of the LC components, which becomes worse at high temperatures [63].

Recently, many new frequency references have been reported based on different concepts, which provide good performance with very low power consumption. One example is the mobility-based frequency reference, which is designed for wireless sensor networks [50]. It employs the charge mobility of a MOS transistor as a reference, which generates a current that

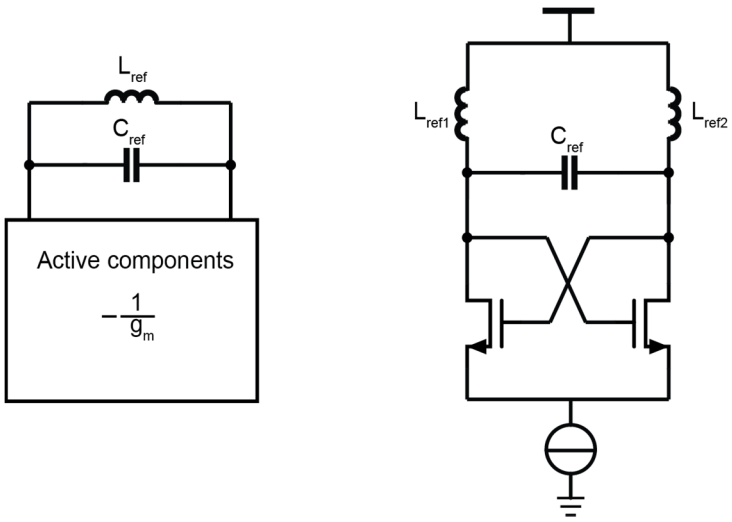


Fig. 2-12. (a) Block diagram of an LC-oscillator; (b) Simplified implementation of the LC-oscillator with cross-coupled transistors

is proportional to the charge mobility. This current, if included in a relaxation oscillator circuit, generates an oscillation signal with a frequency that is a function of the charge mobility. Since the mobility is less sensitive to process variations compare to the CMOS-based resistor or capacitor, it shows good accuracy as well as stability with temperature compensation [50].

Another newly developed approach is based on the thermal-diffusivity of silicon. In [60], an electro-thermal filter (ETF) is included into a frequency-lock loop. Thus the output frequency of a voltage-controlled-oscillator (VCO) is locked to the process-insensitive phase shift of the ETF. Again, with temperature compensation, the reference achieves 0.1 % inaccuracy and 11.2 ppm/^{O}C thermal drift [60, 64]. As a summary, Table. 2-3 lists a performance comparison of some state-of-the-art frequency references.

Table. 2-3. Benchmark of state-of-the-art frequency references

	Oscillation frequency (MHz)	**Temperature coefficient (ppm/^{O}C)**	**Inaccuracy (ppm)**
Quartz Crystal [1] [65]	10 to 60	0.05	N/A
RC Oscillator [66]	14	23	± 1900
LC Oscillator [67]	24	1.4 to 8.6	5 to 300
Ring Oscillator [62]	7.03	± 50.9	± 18400
Mobility-based Oscillator [50]	0.15	N/A	± 5000

	Oscillation frequency (MHz)	Temperature coefficient (ppm/^{O}C)	Inaccuracy (ppm)
Thermal-diffusivity-based Oscillator [64]	1.6	± 11.2	± 100

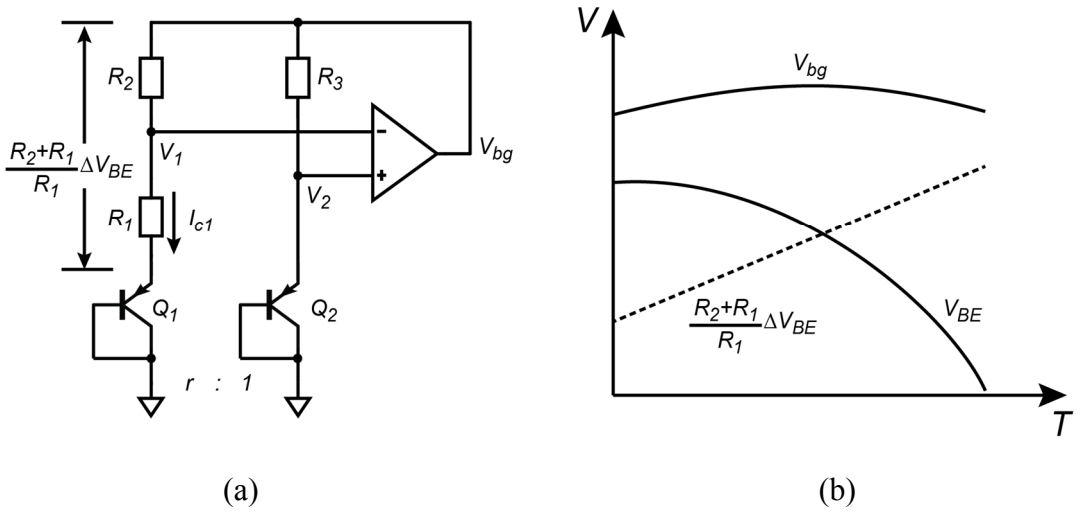
[1] Quartz crystal oscillator is the only one in the table which is not CMOS-compatible. But it can be very small with a surface-mounted (SMD) package.

2.3.4 Voltage reference

The integrated precision voltage references are mostly based on bandgap voltage reference of the semiconductor material. The basic idea of generating a bandgap voltage is to balance the negative temperature coefficient of a PN-junction with a positive temperature coefficient of the thermal voltage $\frac{kT}{q}$ [68]. To do so, a traditional method is to first generate a proportional-to-ambient-temperature (PTAT) voltage by biasing two BJT transistors at different current [69] or applying the same biasing current at different size transistors. A typical circuit diagram of bandgap reference is shown in Fig. 2-13 (a). Due to different transistor size, the base-emitter voltage difference between two transistors is roughly a PTAT type:

$$\Delta V_{BE} = V_{BE1} - V_{BE2} = \frac{kT}{q} \ln r \tag{2-27}$$

Where k is the Boltzman constant, T indicates the absolute temperature in Kelvin and q is the magnitude of charge of a single electron. The OTA guarantees that the voltage V_1 equals to V_2, which results in the following condition:



(a) (b)

Fig. 2-13. (a) Typical circuit diagram of bandgap reference; (b) Temperature behavior of the different voltages in the bandgap reference circuit

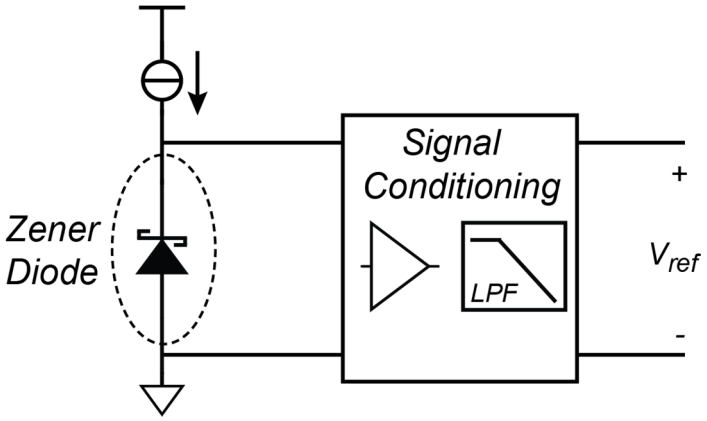


Fig. 2-14. Typical block diagram of a Zener-diode-based voltage reference

$$I_{C1} \cdot R_1 = V_{BE2} - V_{BE1} = \frac{kT}{q} \ln r \tag{2-28}$$

According to the equation, the current across R_2 and R_1 is then a PTAT current, thus the voltage across these two resistors is an amplified version of the PTAT voltage, which can be estimated as:

$$V_c = \frac{kT}{q} \frac{R_1}{R_2} \ln r \tag{2-29}$$

This PTAT voltage, together the base-emitter voltage of transistor Q1 whose temperature coefficient is negative, generate a voltage V_{bg} which is much less sensitive to temperature and is mainly determined by the bandgap energy of silicon [69]. The corresponding temperature behaviors of these voltages are shown in Fig. 2-13(b).

To overcome the nonidealities of the bandgap reference circuits, many advanced techniques are applied: trimmings are commonly used to reduce the V_{BE} spread and the PTAT errors of the bandgap voltage [70]. For the nonlinear temperature dependency of bandgap voltage, many curvature techniques are introduced [70, 71]. Moreover, the error contributed by the active devices are suppressed by applying advanced precision techniques such as auto-zeroing [72] and chopping [70]. The state-of-the-art bandgap voltage reference design in open literature reports a temperature coefficients in the range of 4 ppm/^{O}C to 15 ppm/^{O}C, while the inaccuracy after applying trimmings can reach as low as 0.1 % [70, 72, 73]. The commercial product ADR4520 which is designed specifically for high-precision application shows 2 ppm/^{O}C temperature coefficient in the military temperature range and 0.02 % inaccuracy [74], however, consuming much more power.

Another attractive voltage reference is based on a Zener diode. A Zener diode has well predictable reverse voltage which is very stable over temperature and time, due to the construction of the Zener element. For good noise and stability, Zener voltage reference is usually based on a buried-Zener diode. The conventional Zener diode offers a fairly low thermal drift of around 1 ppm/^{O}C to 2 ppm/^{O}C [75] and it can be further improved by applying

compensation techniques. Fig. 2-14 shows a block diagram of the typical Zener-diode-based voltage reference. The reverse voltage of a Zener diode is transmitted via an anlog signal conditioning chain, which provides filtering and buffering of the signal. Although providing superior precision performance, Zener voltage reference normally requires large reverse bias voltage (> 6 V) for its operation, which limits the use of such reference in low-voltage applications.

Besides the bandgap and Zener reference, [76] presents a very high precision voltage reference which is based on the floating-gate circuit with stored-charge technique. A dual floating-gate differential scheme is implemented in the design, which takes advantage for the slight voltage-dependent temperature behavior of poly capacitors so as to compensate their temperature coefficient by properly adjusting the corresponding bias voltages. In the end, it reports below 1 ppm/^{O}C temperature coefficient and 10 ppm drift in 1000 hours, while consuming only nano-Ampere current. Moreover, it also shows an initial accuracy of 0.01 %.

As a summary, Table. 2-4 is a performance comparison of the possible voltage references based on the above concepts.

Table. 2-4. Performance summary of possible precision voltage references

	Bandgap [70-74]	**Zener [77]**	**Floating-gate [76]**
Temperature coefficient (ppm/^{O}C)	2 to 15	0.05	1
Long-term drift (ppm/1000 hours)	25	1	10
Initial inaccuracy (ppm)	20	1.7	10

2.3.5 Current reference

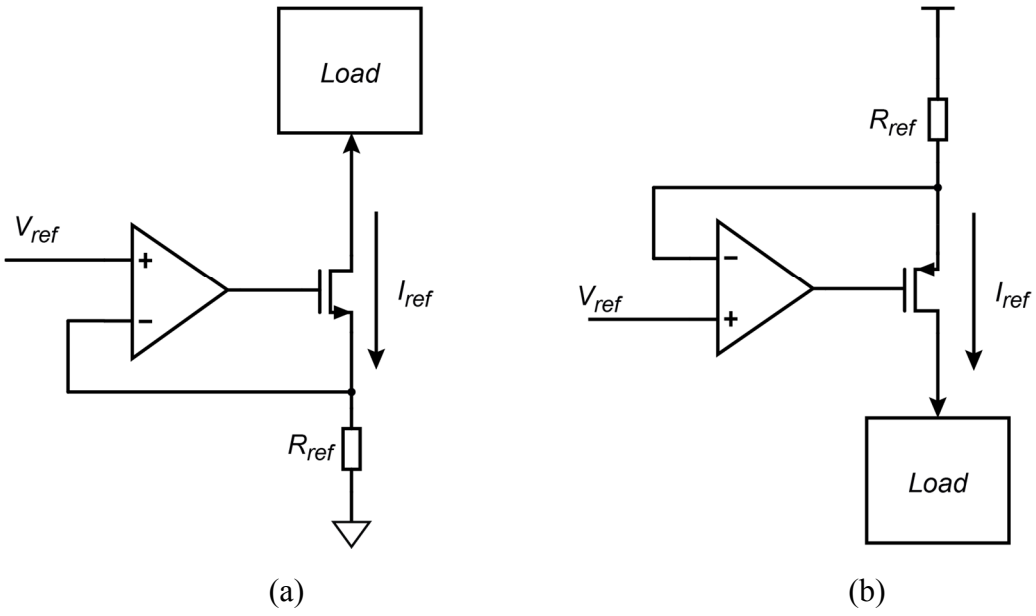
In general, a current reference is derived from a voltage reference by means of a voltage-to-digital (V-I) converter. An ideal current reference is independent of the properties of the load device, such as its impedance and voltage. Therefore, in practice current references are usually implemented with active devices which provide important properties such as high output impedance and constant current irrespective of the load devices.

A most common implementation is based on a regulated voltage-to-current (V-I) converter, as shown in Fig. 2-15. The regulation effect of the OTA provides a stable and accurate voltage across the reference resistor, which in turn, generates a constant current. Moreover, due to the high output impedance provided by the regulated transistor, the variation of the load voltage doesn't pose large effect on the current, provide that the voltage headroom across the regulated transistor is large enough to keep the regulated transistor in saturation region. The V-I converter can be configured as either sinking or sourcing type, as shown in the figure. The reference current is then calculated as:

$$I_{ref} = \frac{V_{ref}}{R_{ref}} \tag{2-30}$$

It is clear that the precision of such current reference is limited by many factors, including the quality of the resistor, the reference voltage and the OTA. Specifically, for fully CMOS realization, the onchip resistor is the dominating factor, which reports hundreds of ppm drift for each degree of temperature change. Therefore, temperature compensation techniques have to be applied in order to achieve good stability. In [78], a low temperature coefficient resistor is designed by compensating the negative temperature coefficient (TC) of an onchip resistor with a positive TC of a MOS resistor. Thus, the current source achieves a temperature stability of 132 ppm/^{O}C.

Another popular implementation of current reference is based on a self-biased CMOS currents source, which use a resistor as the current-defining element. The core schematic of such current source is shown in Fig. 2-16. All the transistors in the circuit are biased in saturation region. Therefore, using the conventional I-V relationship of MOS transistor, the current level can be derived as [68]:



(a) (b)

Fig. 2-15. Circuit diagram of (a) Sinking V-I converter; (b) Sourcing V-I converter

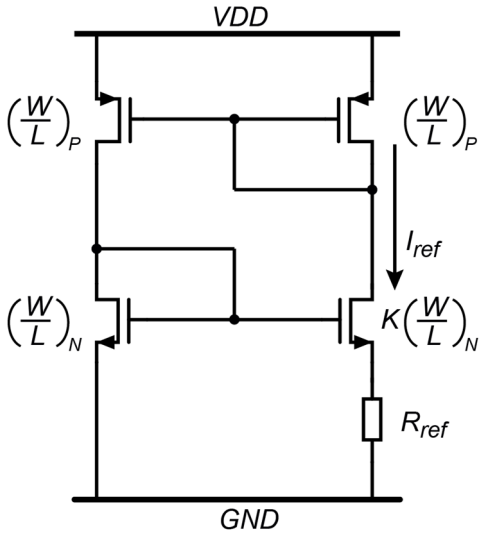


Fig. 2-16. Basic circuit diagram of a self-biased CMOS current reference

$$I_{ref} = \frac{2}{\mu_n C_{ox}(W/L)_N} \frac{1}{R_S^2}\left(1-\frac{1}{\sqrt{K}}\right)^2 \tag{2-31}$$

Where μ_n is the electron mobility and C_{ox} is the dioxide capacitance. In reality, there are two terms which are process and temperature dependent: the mobility of electrons μ_n and the onchip resistor R_s. The process-dependency limits the achievable precision while the temperature dependency prevent from getting good thermal stability of the generated current reference.

The temperature dependency is usually compensated by introducing extra elements which have opposite temperature coefficients. In [79], a PTAT voltage source is implemented in the V-I converter which compensates the negative temperature coefficient of the V-I converter in first-order. To gain better compensation for the curvature of the temperature dependency, higher-order compensation techniques are also introduced. In [80], a second-order compensation is achieved by implementing a MOS inverse Widlar mirror whose current ratio is temperature dependent. Then, by properly set its design parameters, the temperature dependency of the current mirror compensates the opposite temperature coefficient of the current source. Another high-order compensation technique is shown in [81]. The overall reference current is a combination of three currents: the current generated by the V-I converter which has negative temperature coefficient, a PTAT current and a current with high-order temperature dependency [81]. Therefore, by properly sizing the currents, their temperature dependencies are compensated to higher orders, which gives much better performance in terms of the thermal stability.

For the precision which is related to the process dependency of the circuit parameters, however, cannot be compensated by circuit techniques. Thus extra trimming is usually applied to get better initial accuracy. Table. 2-5 provides a summary of the performances of state-of-the-art current references.

Table. 2-5. Performance summary of state-of-the-art current references

	Regulated converter (onchip references) [78]	**Regulated converter (offchip references) [82]**	**Self-biased [79-81]**
Temperature coefficient (ppm/^{O}C)	132	Depends on the offchip references	0.7 to 50
Initial inaccuracy (%)	< 0.02	Depends on the offchip references	N/A [1]

2.3.6 Conclusion

This section presents a performance overview of references that can be used for capacitance measurement. The different types of references are explained in terms of their construction, material and performances. Their key performances such as stability, accuracy and tolerance are discussed in detail. The results provide good basic of selecting suitable references according to the practical requirements.

Based on the investigations in section 2.2 and 2.3, a discussion about optimal choice of the references and interface architecture will be addressed in the next section.

2.4 Discussion and conclusion

An interface circuit together with proper reference(s) are required for measuring capacitance. In the previous sections, possible interface circuit architectures and references for capacitance measurement are investigate. Their advantages and disadvantages are analyzed, which provides information about their suitability in different applications.

Based on the analysis, this section discusses the optimal combination of references and interface structure which could perform high resolution and high precision capacitance measurement in an energy-efficient way.

2.4.1 Selection of optimal combination of references

The ultimate achievable performance of a CDC is determined by the references employed in the comparison circuit. Hence, the references have to be selected such that they don't limit the performance. As discussed in the previous sections, many references can be employed in a CDC circuit, including capacitive reference or combinations of different references which generate equivalent capacitive reference.

As discussed in the above sections, the most straightforward way of implementing a CDC is to compare the unknown capacitor with a reference capacitor. Among all types of capacitors, the survey of section 2.3.1 shows that only the dedicated capacitor standard [48] could achieve below 10 ppm/^{O}C and small tolerance. However, such standard capacitor is bulky and expensive, which doesn't fit in the complex system where volume is strictly limited. The other types of capacitors could be small and low cost, however, none of them achieves the required precision. Therefore, using a capacitive reference in the precision CDC design is not feasible.

If a precision capacitive reference is not readily available, it is possible to generate an equivalent capacitor with proper combinations of different references, such as voltage, current, resistor, etc. The possible combinations that have been discussed in section. 2.3.

Discussions in the same section found that resistive and time references can be very precise and stable over temperature and time. Specifically, the metal foil resistor [54] and quartz crystal oscillator [64] provide superior performance which meet all the requirements of the target application. The voltage [74] and current references [81, 82], by proper design, can also achieve acceptable level of performances for the target application. The inductor-based reference, as states in section, it is only used in specific applications where high oscillation frequency is required [40, 41]. Hence it was not covered in this discussion.

As a conclusion, the combination of time and resistor references are preferred due to their high precision performance. The combination of voltage, current and time is also feasible for the target application, provided that they are properly designed and compensated.

2.4.2 Selection of optimal interfacing principle

Having the most precision references, however, doesn't necessarily guarantee that the CDC could achieve the required precision. Because the interfacing circuit which does the comparison of unknown capacitance with precision references also introduces extra errors, it is important to select an interfacing principle which could use precision references while introducing minimum extra errors.

As discussed earlier, the CDCs based on RC-oscillators or ring-oscillators are able to use combinations of references such as resistor, time and voltage, etc, which can be precise and stable. The ring-oscillator-based designs [38] compare the unknown capacitor with the combination of voltage, current and time references. But the existing works are all in low resolution and low precision applications due to their sensitivity to parasitic effect.

The precision of the above approaches are limited by their interfacing circuitry instead of the references used. Therefore, using precision references in this case doesn't help to improve the precision of the CDC. Moreover, the works based on these approaches are limited to low resolution applications, which are not suitable for the target application.

The high resolution applications, as shown in Fig. 2-11, are dominated by two types of CDCs: the direct delta-sigma modulator based CDC [8, 38, 83] and the CFC-based CDC [21, 23, 24,

84]. Both CDCs provide good immunity to parasitic via their active integrators, ratio-metric measurement natural [8, 23] and the applied auto-calibration techniques [21, 23]. Therefore, CDCs based on such principles can essentially provide good precision. However, the existing designs are all based on comparison with capacitive references. As discussed in section. 2.3.1, capacitive references can hardly provide the required precision with a reasonable size and cost.

In conclusion, the oscillator-based circuits facilitate the use of precision references. However, the interfacing circuits limit the achievable precision and resolution. A delta-sigma-based or CFC-based CDC may provide good performance while suffering from the low-precision capacitive references used. Therefore, to combine the advantages of precision circuitry and references, it is desirable to design the CDC with delta-sigma or CFC structure while employing other precision references rather than the capacitive one. A most straightforward method to do so is by means of the *charge-balancing* principle [69]: the charge generated by the unknown capacitor is balanced by the charge generated from the precision references. In the end, the capacitance can be expressed by a ratio of the references. The CDCs based on this principle are investigated further in the next section.

2.4.3 Conclusion

In this chapter, an investigation of high-performance capacitive sensor systems has been presented. The investigation is split into three parts: the sensor head, the interface circuit and the reference(s) used for the interface circuit.

Regarding to the sensor head, the biggest limiting factor is the mis-alignment. The big standoff distance of sensor plates due to bad alignment quality leads to a reduced sensitivity of the sensor and an increased demand for high dynamic range interface electronics. Both of the above problems result in high power consumption of the interface electronics. To solve the problem, a thermally-actuated alignment device has been proposed, which could align the sensor automatically after assembling. But to achieve good alignment speed and high repeatability, a good control system is required.

To interface a capacitive sensor, many possible circuit architectures have been developed in the past decades. Regarding to the references used, there are two types of interface structures identified: 1) the unknown capacitance is compared with a reference capacitance; 2) the unknown capacitance is compared with a combination of different references which generate an equivalent reference capacitance. State-of-the-art designs based on different references are investigated, in terms of their performances and power-efficiency. It is observed that the high-resolution applications are dominated by Delta-Sigma or CFC based interfaces.

Stability of the capacitive sensor is an important factor for high-precision applications, which, unfortunately has been ignored in most of the capacitive sensor designs. The ultimate stability of a capacitive sensor system is limited by the references used for capacitance measurement. For this reason, an investigation has been made for all the references which can be used for capacitance measurement. The investigation showed that the combination of resistive and

frequency references deliver good performance regarding to the stability, tolerance and absolute accuracy. Besides, this combination of references can be easily interfaced by a charge-balancing-based Delta-Sigma or CFC CDC, which reports high resolution in a power-efficient way.

Based on the investigation, Chapter 3 will focus on analyzing and optimizing the thermal stepper system so as to improve the alignment quality of the sensor head. [27]

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Chapter 3

Auto-alignment of Capacitive Sensor

In Chapter 2, it is stated that the performance of a high-precision capacitive sensor relies on accurate positioning of the sensor head. However, due to the relatively high mounting and manufacturing tolerances of industrial equipment, the desired sensor alignment is always a serious obstacle when using cheap, reliable and compact capacitive sensors. As a result, the misalignment reduces the sensitivity of the sensor while imposing large dynamic range requirement on the proceeding CDC.

To solve this problem, a thermally-actuated auto-alignment device has been proposed, which can effectively align the capacitive sensor after the sensor assembling. However, as indicated in Chapter 2, the preliminary open-loop controller experiences low control speed and unpredictable alignment accuracy. Hence, a better control scheme that delivers higher controllability and performance is desired.

This chapter investigates various control algorithms. The operating principle of the device is first described. Then, possible control algorithms are proposed and discussed. Based on that, optimal algorithm is selected, implemented and qualified.

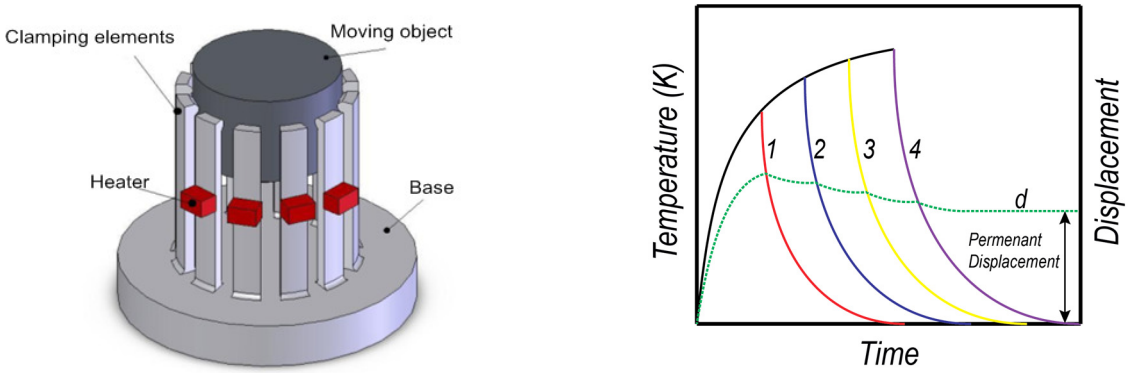
3.1. Open-loop control

The thermal stepper concept is based on thermal actuation. That is, the displacement is generated by means of heating or cooling of the thermal actuators. The actuators in this system are the clamping elements, as was shown in Fig. 3-1.

Because of the thermal expansion effect of materials, heating up the elements makes their length larger, thus moves the object upwards. On the contrary, cooling down the elements causes them to contract, and thus moves the object downwards. The relationship between the length of the elements and the temperature can be written as:

$$\Delta l = \Delta T \cdot \alpha \cdot l , \tag{3-1}$$

where ΔT is the temperature change of the elements (in K), α is the thermal expansion coefficient of the elements (in $\mu m \cdot m^{-1} \cdot K^{-1}$), and l is the initial length of the elements (in m). In the primary prototype design, aluminum is selected as the material, because of its good thermal expansion coefficient and low cost.



(a) (b)

Fig. 3-1. (a) The thermal stepper system; (b) The corresponding qualitative temperature profile as well as the displacement of the object being aligned

An open loop control system is simple and easy to implement, which only consists of a microcontroller and several power switches that switch on and off the heaters on the actuation elements. Therefore, it is small in size, and consumes very little power.

The simplest way of implementing an open-loop controller is to passively heat or cool the thermal elements for a pre-defined time and sequence. Fig. 3-1(b) shows a typical temperature profile of a four-element (1, 2, 3, and 4) thermal stepper system based on an open-loop control. Beside the temperature of the elements, the graph also shows the position of the moving object (d). The shape of the temperature profiles show exponential relation between the temperature and time. Assuming a first-order system, the relation can be expressed by the following equation [1, 2]:

$$\Delta T = PR_{th}\left(1 - e^{-\frac{t}{R_{th}C_{th}}}\right), \tag{3-2}$$

where P is the heating power (in *Watt*), R_{th} is the thermal resistance of the actuation elements (in *K/W*) and C_{th} is the thermal capacitance of the elements (in *J/K*).

From Eq. (3-2), it is clear that the maximum temperature change is determined by the heating power and the thermal resistance of the actuation elements, which can be written as:

$$\Delta T_{\max} = PR_{th} \ . \tag{3-3}$$

According to Eq. (3-1), Δl is proportional to the temperature change ΔT of the clamping elements. Therefore, to generate a specific Δl, it is possible to calculate the required temperature difference and heating power, using Eq. (3-1) and Eq. (3-3) respectively. In reality, however, the parameters such as α and R_{th}, are not accurate known. Therefore, with an open-loop control, it is very difficult to achieve accurate Δl. Moreover, the system shows poor rejection to the disturbances (e. g. ambient temperature variation).

Apart from the accuracy, we also consider the speed. The speed of the temperature change is determined by the thermal time constant of the elements, which is the product of the thermal resistance and the thermal capacitance of the actuation elements, as is written:

$$\tau = R_{th} \cdot C_{th} \tag{3-4}$$

As is shown in Fig. 3-1 (b), the maximum temperature is only reached after a long time, while the sequential cooling starts much earlier. This means that the elements start cooling down before $\Delta T_{\max}$ has been reached. As the elements start cooling one after the other, both $\Delta T_{\max}$ and the related step size becomes dependent on the order of cooling [3]. If we want to wait until the maximum temperature is reached before starting the sequential cooling, it will take a long time to perform one stepping action, which is also not desired.

After heating up, the cooling down procedure occurs exponentially with respect to time either. This means that the last phase of the process will be time-consuming. Besides, since the control system allows the next element to cool down after a few seconds, two or more elements may contract at the same time, which leads to unwanted slips of the moving object. As a result, the step size is smaller and inaccurate.

3.2 Closed-loop control

A closed-loop temperature control system can improve the performance of the thermal stepper. Since the temperature step T_{step} can be accurately set to any value between the initial and the maximum temperature, it can be guaranteed that every element reaches a defined temperature. This implies that every element also has a defined change in length.

As shown in Fig. 3-2, a closed-loop controller can be used to prevent an element from cooling down to its initial temperature. This control enables the system to cool down relatively fast, as cooling is limited to the first steep part of the exponential curve. As soon as the next element starts cooling down, the temperature of its predecessor is fixed. This prevents two or more elements from contracting at the same time. Moving only one element at time increases the effective step size. Increased step size and decreased cycle time enable a faster movement of the system. The complete system is only cooled down once the total number of the stepping actions is performed.

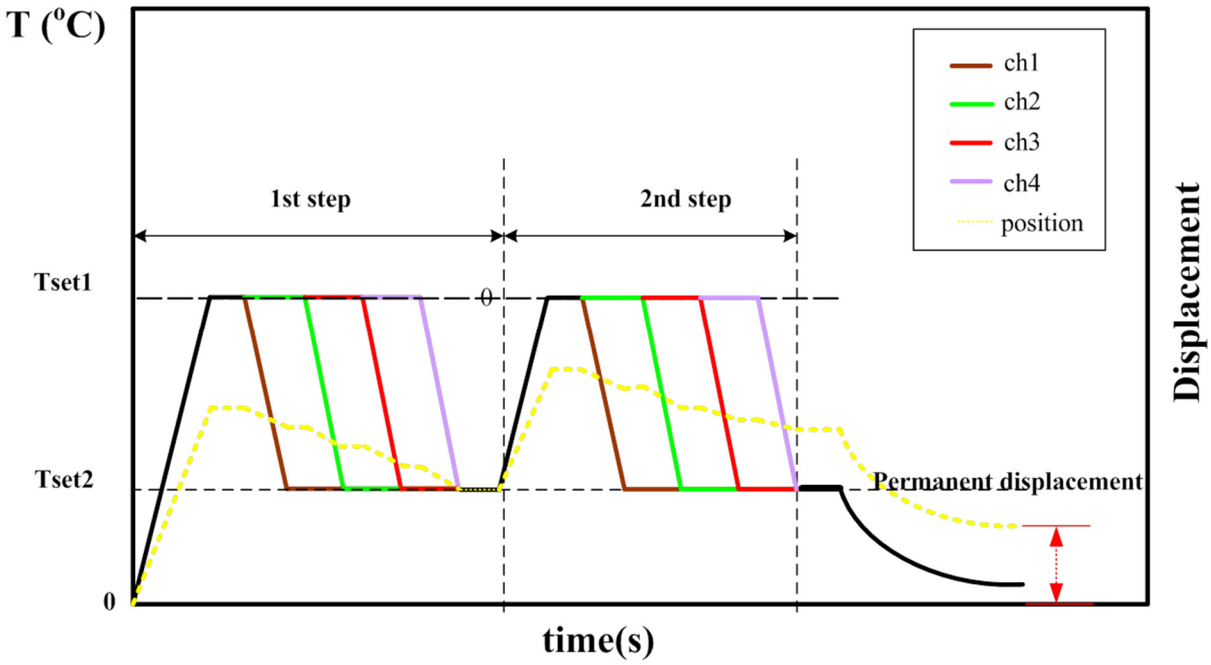


Fig. 3-2. Temperature and displacement profiles of a thermal stepper under closed-loop control

3.2.1. ON/OFF control

The most common and simple way of implementing a closed-loop controller is by means of an ON/OFF control. Such controller switches on and off the heating power depending on the measured temperature of the actuation elements. Hence, it is able to maintain the temperature of an actuation element at any predefined level.

A) Conventional ON/OFF control

Fig. 3-3 shows the block diagram of the ON/OFF type controller. The process temperature is measured and compared with a set-point. Then, an error signal is generated. Based on the sign of this error signal, the controller switches between maximum and minimum output level. In practical, some hysteresis is added into the controller, in order to prevent noise from switching the heater rapidly on and off when the temperature is near the desired value [1].

Fig. 3-4 shows the basic response of the ON/OFF controller. From the plot, the controlled temperature is varying around the set-point, because of the switching of the control signals. The value of such temperature ripples are related to many factors: the control power, sampling time, and the hysteresis. Thus to reduce the ripples, these factors have to be investigated and optimized.

In our design, large temperature ripples are not acceptable, because they may introduce unwanted displacements or tilts to the object. Therefore, many techniques have to be applied to limit the ripples to an acceptable level.

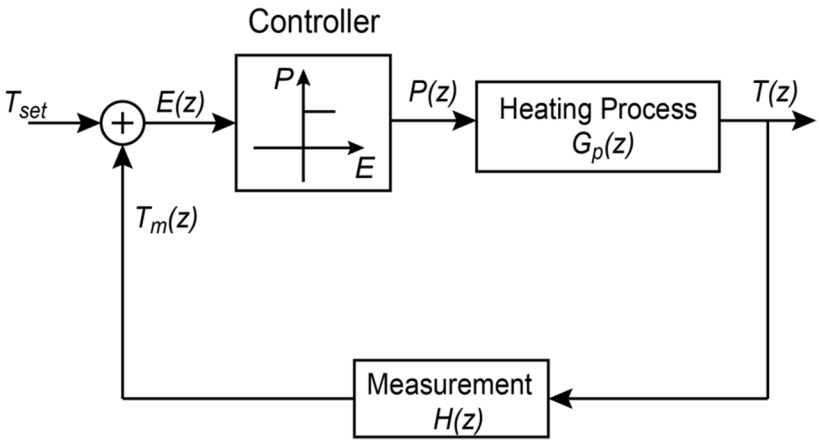


Fig. 3-3. Block diagram of the ON/OFF controller

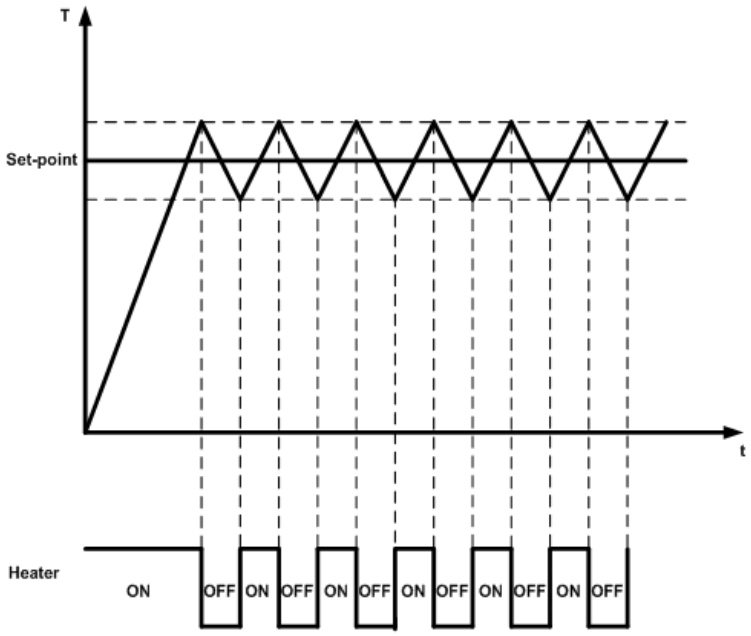


Fig. 3-4. Response of an ON/OFF controller

B) ON/OFF control with damping factor

In some practical implementations, a damping factor (or a differential term) is added to the error calculation of the controller. This is to stabilize the system in case of sudden change of the environment. For instance, in case the ambient temperature changes abruptly, the damping term will help the controller to react to the change quickly. In addition, the damping factor also help to reduce the temperature overshoot/ripples around the set-point and the overall system settling time, without increasing much of the design complexity.

The complete block diagram of the closed-loop control system is shown in Fig. 3-5. The *Gp(s)* represents the transfer function of the process under control. *T(s)* indicates the temperature of the process. The transfer function of the temperature measurement electronics is represented by *H(s)*.

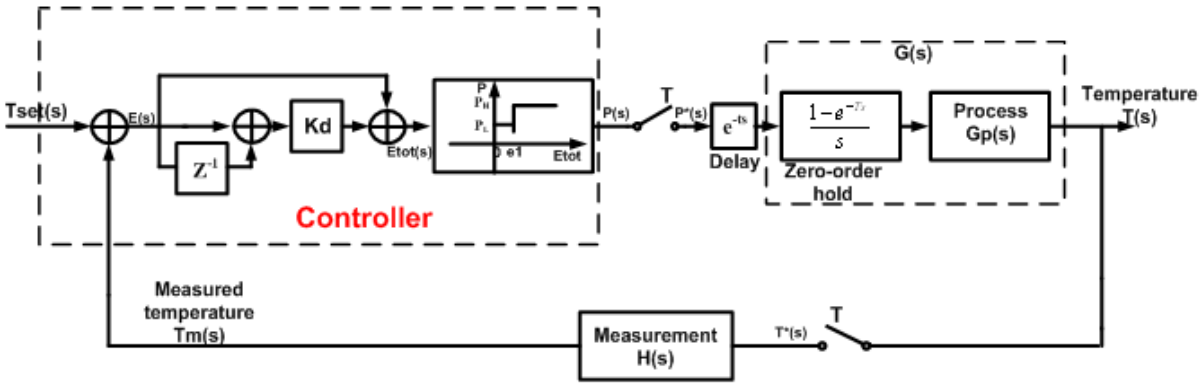


Fig. 3-5. Block diagram of a closed-loop control system based on a damped ON/OFF control

The temperatures are periodically measured, and the results (T_m) are compared with a set point temperature (T_{set}) to generate the error signals (e). The decision of the control signal is based on the error signal. Depending on the error signal, the microcontroller decides whether the element is heated or cooled down. With the extra differential term, the temperature ripples during the holding phase is reduced.

The effective error signal e_{eff} is calculated as:

$$e_{eff}(s) = K_p \cdot e(s) + K_d \cdot \frac{de}{dt} \tag{3-5}$$

3.2.2. Closed-loop PID control

The ON/OFF controller is simple and easy to implement. However, its performance is limited by the cycling behavior which is inherently associated with such type of controllers. Because of the cycling behavior, the temperatures during the holding phase always have some temperature ripples. Although it can be reduced by adding a damping factor in the controller as mentioned above, it is not completely removed. As explained earlier, the temperature ripples will cause local movements or tilts of the actuation elements. As a result, the performance of the thermal stepper is affected.

In order to stabilize the temperature at holding phase, a more advanced controller—PID controller can be implemented (Fig. 3-6). A PID controller looks at the current value of the error, the integral of the error over a time interval, and the current derivative of the error signal to determine how much control signal to apply [4]. In continuous time domain, such controller can be expressed as:

$$P_{out} = K_p \cdot e + K_i \cdot \int e \cdot dt + K_d \cdot \frac{de}{dt} \tag{3-6}$$

where K_p , K_i , K_d represent the proportional gain, the integral gain and the differential gain, respectively. P_{out} is the control power, and e is the error signal.

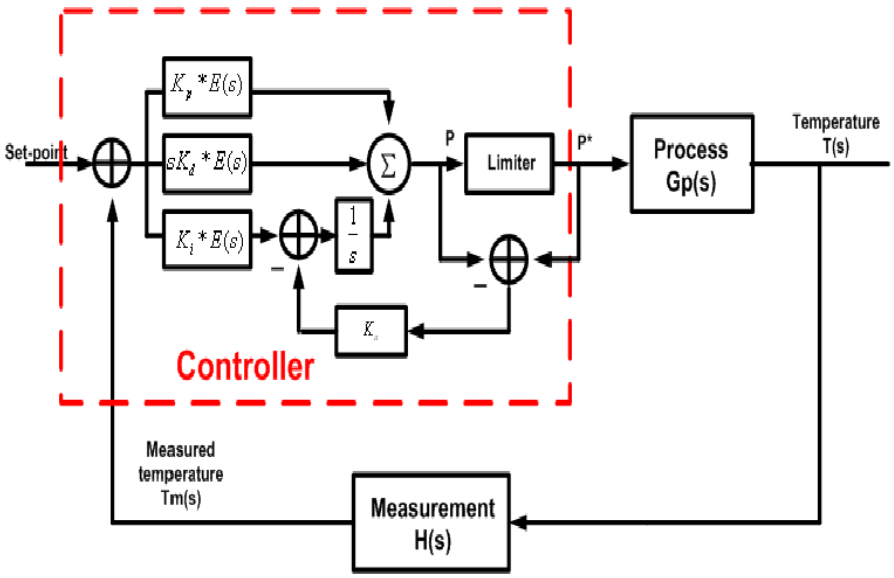


Fig. 3-6. Block diagram of the PID control based thermal stepper control system

Proportional term

The proportional term increases the speed of the temperature rise. With a fixed proportional gain, the control signal increase as the error increase. When the error becomes small, the control signal also becomes small. An important characteristic of the proportional term is that it produces a permanent residual error in the operating point of the controlled variable. This error is referred as the steady-state error. Increasing the proportional gain can reduce the temperature rise time, however, it also increase the overshoot above the set-point.

Integral term

The integral term calculates the accumulation of the previous errors. Thus even when the current error is zero, the integral term is non-zero. Finally, the steady-state error caused by the proportional term can be eliminated by the integral term.

However, in frequency domain, the integral term adds one pole, which reduces the phase margin of the closed-loop control system. Hence the stability of the system is reduced by adding an integral term. In time domain, the integral term may cause overshoots and oscillatory behavior. Large integral action decrease the rise time and increase the system settling time.

Derivative term

The derivative term acts as a damping factor, which stabilizes the system. Increasing the derivative action will decrease both the overshoot caused by the proportional or integral terms. Also, the derivative term reduces the system settling time especially in case of abrupt changes of the ambient temperature.

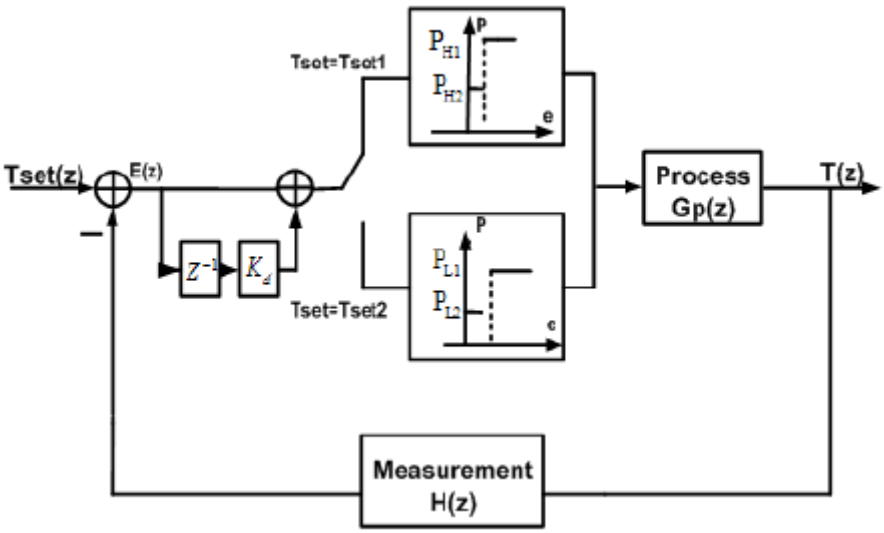


Fig. 3-7. Block diagram of the multi-level controller.

3.2.3. Multi-level control

The PID controller, as discussed, can effectively stabilize the temperature at the set-point. However, from circuit implementation perspective, a PID controller inclines the need of a digital-to-analog converter (DAC) in order to translate the calculated output to appropriate actuation power (see Eq. 3-6). This would increase the design complexity of the control system. More importantly, a DAC usually does not have enough driving ability to provide enough power to the actuators (or heaters). Because of this, a power amplifier is required for each of the actuators.

The problem with the power amplifier is that the same amount of current, which flows into the heaters, also flows through the output impedance of the amplifier. As a result, the amplifiers consume a large amount of power and generate considerable heat. As the complete control system is intended to be integrated into the sensor head, the generated heat raises the temperature of the sensor head and thus influences the performance of the system.

To minimize the design complexity, the self-heating effect and to combine the advantages of both control algorithms (simple ON/OFF and PID), a switch-mode multi-level controller is proposed. The block diagram is shown in Fig. 3-7. The multilevel controller is helpful for reducing the temperature ripple due to the multiple output power levels and the proportional control with damping factor. Moreover, as the controller is based on switch mode, the hardware and the software can be simplified. The elimination of the output power amplifiers increases the power efficiency and reduces the self-heating of the circuit.

As can be seen from Fig. 3-7, the calculation of the effective error (incl. damping term) is based on the same method as Eq. (3-6). After determining the effective error, the controller will apply proper heating power to the actuators (or thermal elements).

As mentioned in section 3.2.1, one of the purposes of applying closed-loop control is to avoid waiting for the exponential cooling behavior of the thermal elements. This is done by maintaining the temperature at a lower level (T_{set2}) by means of closed-loop control (see Fig. 3-2). Because of this, there are two temperature set-points, one of heating and one for cooling. For each set-point, two different levels of control power are available. The higher power level is used to increase the heating speed, with which each set-point can be reached fast. When the temperature of the element approaches the set-point, lower power level is used to maintain the temperature at the set-point with minimum ripples (variations around the set-point due to the switching on and off of the control power). The decision-making logic is shown in the following equation:

$$\begin{cases} P = P_{H1} & T_{set} = T_{set1} \,\&\, E_{tot} > E_1 \\ P = P_{H2} & T_{set} = T_{set1} \,\&\, 0 < E_{tot} < E_1 \\ P = P_{L1} & T_{set} = T_{set2} \,\&\, E_{tot} > E_1 \\ P = P_{L2} & T_{set} = T_{set2} \,\&\, 0 < E_{tot} < E_1 \\ P = 0 & E_{tot} < 0 \end{cases} \tag{3-7}$$

3.3 Circuit implementation

3.3.1. Temperature measurement circuit

To apply closed-loop control, the temperatures of the thermal actuation elements have to be measured. Then, based on the measured temperature and the target temperature (set-point), appropriate output power is applied depending on the control algorithm implemented. To measure the temperatures of the thermal actuation elements, thermistors are mounted on each of the thermal elements. These thermistors are well-calibrated in advance to ensure good matching (the tolerances of the thermistors are below 0.7% within the entire temperature range). The nominal resistance selected at 25 ^{o}C is 22 kΩ. This choice takes into consideration both the thermistor noise and self-heating effect.

The block diagram of the readout electronics is shown in Fig. 3-8. A typical Wheatstone bridge is implemented as the readout circuit of the thermistors [2]. To optimize the size of the electronics as well as the overall power estimation, the same readout circuit is used to interface all the thermistors of a thermal stepper device, meaning the measurement of the temperature is time-interleaved [5]. A low-noise instrumentation amplifier is used to provide enough gain for the signal. After the filtering, a 16-bit ADC digitizes the signal and sends the information to the microcontroller for processing. To reduce the systematic error of the measurement, system-level auto-zeroing is applied. To do so, the inputs of the instrumentation amplifier are periodically shorted to ground so that the system error (e.g. offset) is measured and recorded in the microcontroller. Afterwards, the error is compensated during the normal measurement.

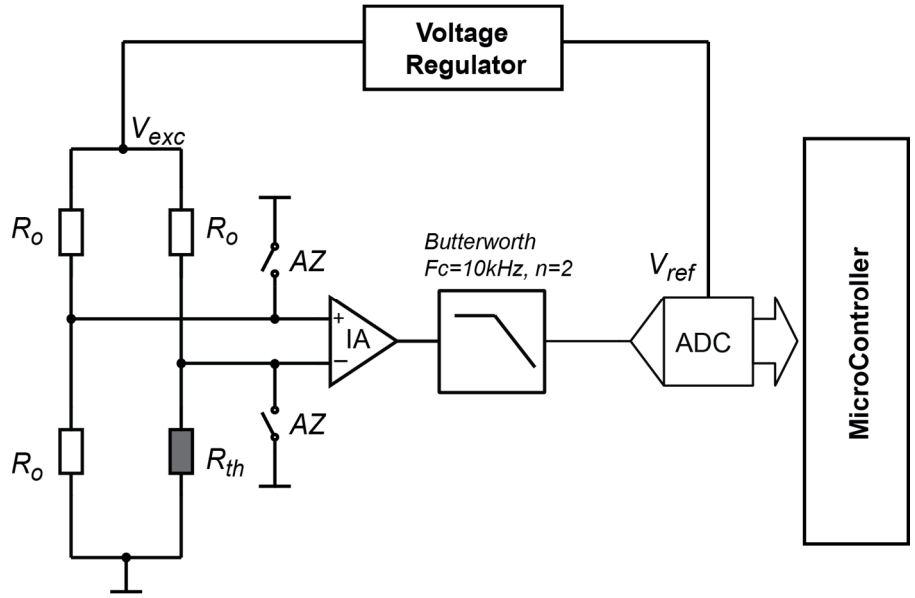


Fig. 3-8. Simplified schematic of the temperature measurement electronics to be used in a closed-loop controller

3.3.2. Control electronics

ON/OFF control:

The control electronics for a simple ON/OFF closed-loop controller consists of only two switches for each heater, which are controlled by opposite signals. On one side, both of the switches are connected to the heater. On the other, one switch connects to the power source while the other connects to ground. Based on the measured temperature (whether higher or lower than the set-point), the heater is connected to either the power source (ON state) or ground (OFF state). It is important to note that the switches have to be carefully selected such that it can sustain the current flow that is delivered to the heater without being destroyed. Otherwise, several techniques such as use parallel switches, or reduce maximum current though can be considered, as will be discussed shortly.

PID control:

Fig. 3-9 shows a simplified schematic of the PID controller electronics. A digital-to-analog converter (DAC) is used to convert the control signal to analog form. In order to save power, sample and hold (S/H) circuits are constructed so that only one DAC is required for multiple-channel control. After that, buffers, which have enough driving ability, are used to drive the heaters. The capacitance of the S/H circuit is determined by the system sampling frequency *fs* and the maximum acceptable drift caused by the input bias current of the power amplifier. First, the settling accuracy of the S/H circuit can be approximated by using the equation:

$$Accuracy = 1 - e^{-\frac{t}{RC}} \tag{3-8}$$

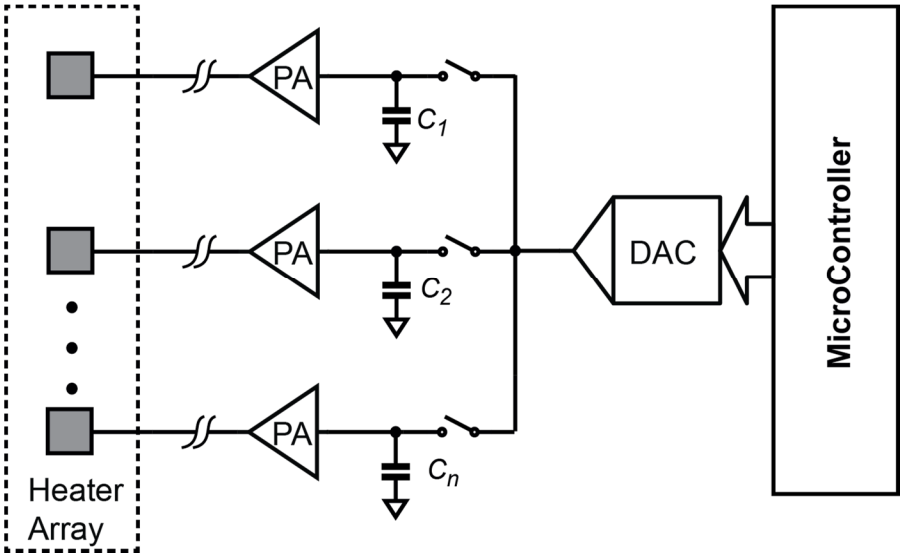


Fig. 3-9. Schematic of the closed-loop controller circuit based on PID control

where R (ohm) is the on-resistance of the sampling switch, and C (Fara) is the capacitance of the sampling capacitor ($C_1 \sim C_n$). To ensure the performance of the system, the S/H circuit has to be settled to the required accuracy before the next sampling. In this design, the settling accuracy is defined as 10 bits (0.1 %).

In addition to the settling time, the effect of the input bias current of the power amplifier has to be taken into account. Due to the input bias current of the amplifier, the control signal will slowly drift. This effect can be expressed by the following equation:

$$\Delta V = \frac{I_{bias}}{C}\Delta t \tag{3-9}$$

Where I_{bias} (A) is the bias current of the power amplifier, and ΔV is the drift of the control voltage.

Based on the above equations and requirements, the sampling frequency is 50 Hz and the sampling capacitance is 2.2 uF, so that the signal can settle to an accuracy of 10-bit. Moreover, power amplifiers with a low-bias current (50 pA) are used in the design in order to minimize the drift of the control signal.

Multi-level control:

The PID controller, as described in section 3.2.2, consumes a large power due to the fact that power amplifiers are required to deliver enough power to the heaters. Therefore, to deal with this problem, a switched-mode multi-level controller is proposed, which takes advantage of the low power feature of ON/OFF controller and the temperature stability feature of PID controller. A schematic of such controller is shown in Fig. 3-10.

To reduce the self-heating of the circuit, the power amplifiers are eliminated and the power source is located outside the system. The control power is delivered to the heaters only by several switches (Fig. 3-10). Thus, only the on-resistance of the switches will cause self-heating

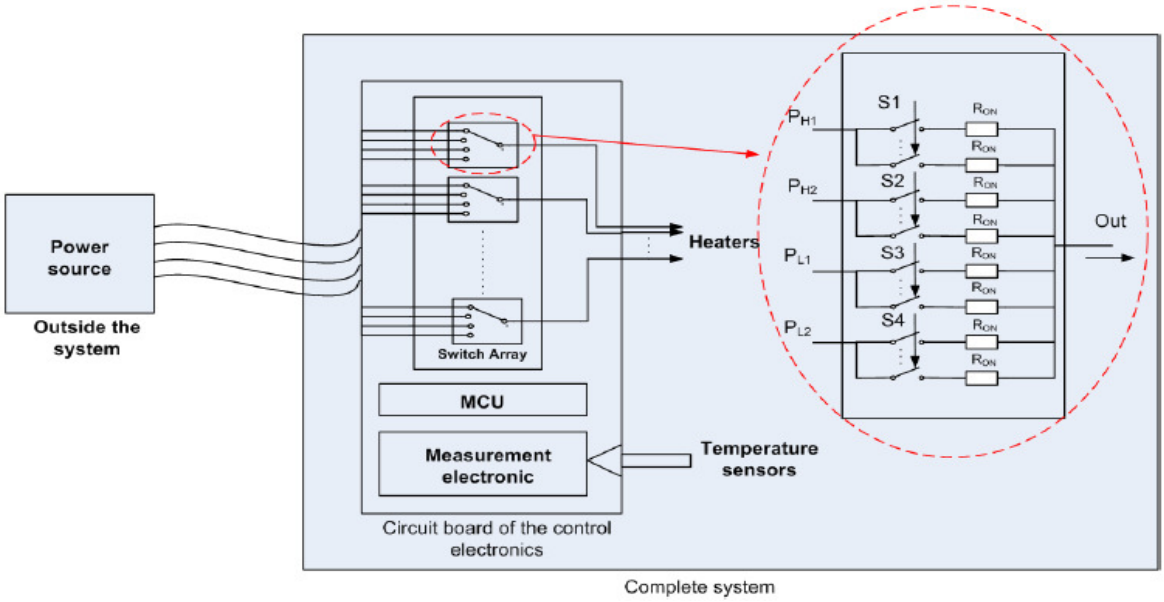


Fig. 3-10. Simplified schematic of the switch-mode multi-level controller

of the circuit. To further reduce self-heating of the control electronics, the supply current to the heaters is reduced. This is done by increasing the supply voltage and heater resistance at the same time so that the power delivered to the heaters are kept the same. In addition, several switches are connected in parallel to reduce the equivalent on-resistance, as shown in Fig. 3-10.

3.4 Experimental results

To validate the theoretical analysis, three different closed-loop controllers have been successfully implemented in printed circuit board level. Many experiments are performed to characterize their performances. The open-loop controller is out-of-scope in the validation, because of its poor immunity to external disturbances and low control predictability, which are not suitable for high-precision industry applications.

3.4.1. ON/OFF control

The control electronics was implemented in a printed circuit board, and the complete measurement setup was built, according to the functional blocks shown in Fig. 3-3. The image of the control electronics is shown in Fig. 3-11 (a). Moreover, Fig. 3-11(b) shows the image of the thermal stepper system.

Fig. 3-12 shows the measurement result of an upward stepping action. The top plot shows the temperatures of different thermal elements. From the curves, the rise and fall in temperature occur very fast because of the elimination of the exponential temperature profile, as discussed earlier. The bottom plot shows the position of the moving object.

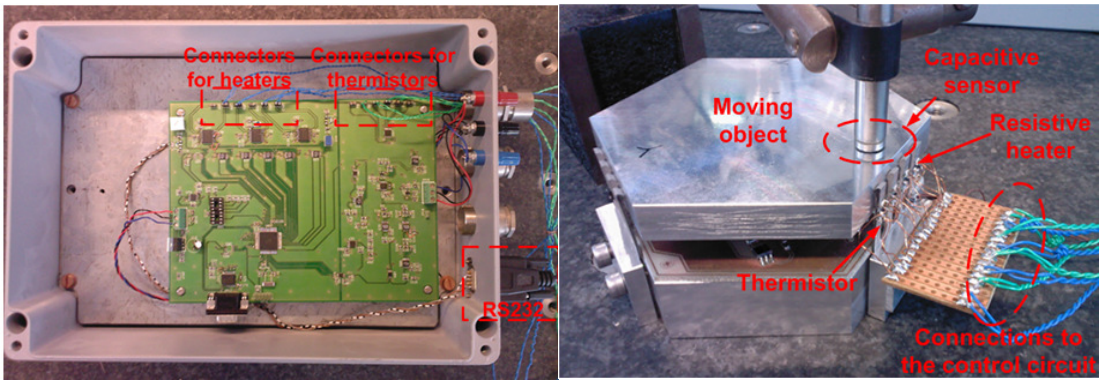


Fig. 3-11. (a) Image of the controller electronics board; (b) Image of the thermal stepper system with a commercial capacitive sensor to measure the displacement

In addition, the control power is removed at 230 sec, thus the temperatures of all the elements return to the initial temperature. However, the position of the object is maintained, which further proves the principle. Finally, the stepping speed is calculated as 1.2 μm/min. Moreover, the maximum tolerance of the step sizes is within 3 %, meaning a good repeatability of the alignment.

Apart from the upward stepping action, the downward stepping action is also performed. The measurement result of the action is shown in Fig. 3-12. The top plot shows the temperatures of four different thermal elements, and the bottom plot shows the position of the object. Also, after removing the control power, the position of the object remains. The stepping speed is calculated as 0.77 μm/min. The smaller step size in this measurement is due to the smaller temperature difference (4.5 ^{o}C) we made. Since the ratio between the final step and the initial step is almost constant, the larger the temperature difference is, the bigger the step size will be. However, the maximum temperature difference is limited by the output driving ability of the power amplifier and maximum available power supply.

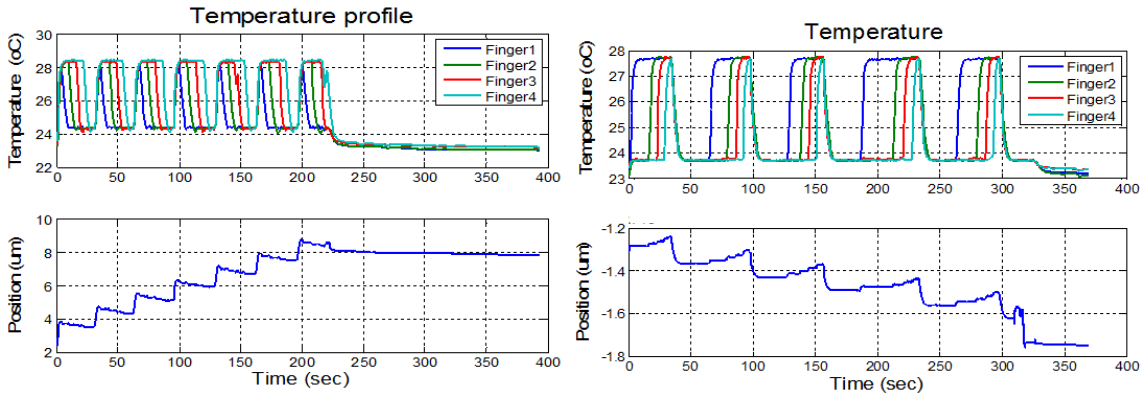


Fig. 3-12. Measurement results of (a) an upward stepping action; (b) a downward stepping action

The performances of the stepping actions are summarized in Table. 3-1.

Table. 3-1. Performances of the stepper system based on the 1st controller

	Upward	Downward
ΔT_{max} (°C)	5.5	4.5
Step size (µm)	0.8	0.64
Speed (µm/min)	1.2	0.77
Temperature coefficient of the step size (µm/K)	0.14	0.14
Maximum Tolerance of the step size (%)	3%	3%

3.4.3. PID control

To verify the effectiveness of PID controller, a test setup was built, as is shown in Fig. 3-13. The thermal stepper system is clamping a plate of the capacitive sensor. The flex-PCB, which contains the heaters and temperature sensors (thermistors), is glued onto the stepper system, and the connection wires extend from the bottom of the stepper. The capacitive sensor under alignment is used to measure the position of the plate (Fig. 3-14). The control electronics is implemented on a PCB board which controls the operation of the system, as shown in Fig. 3-14.

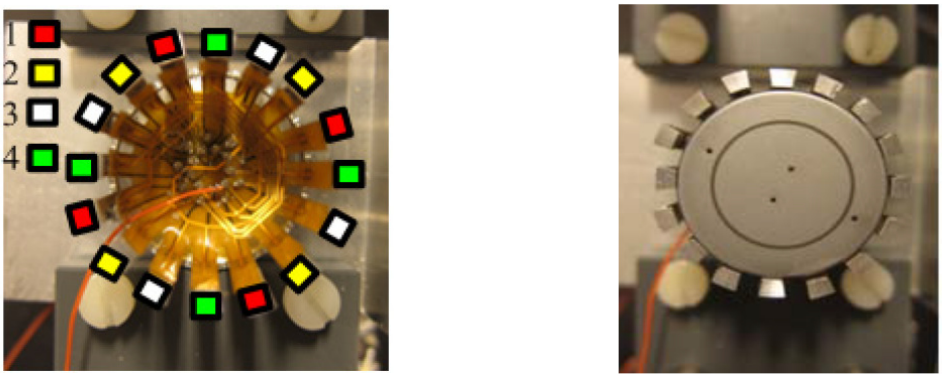


Fig. 3-13. a) Flex-PCB for easy connection (left); b) the thermal stepper device with flex-PCB mounted on the thermal elements (right)

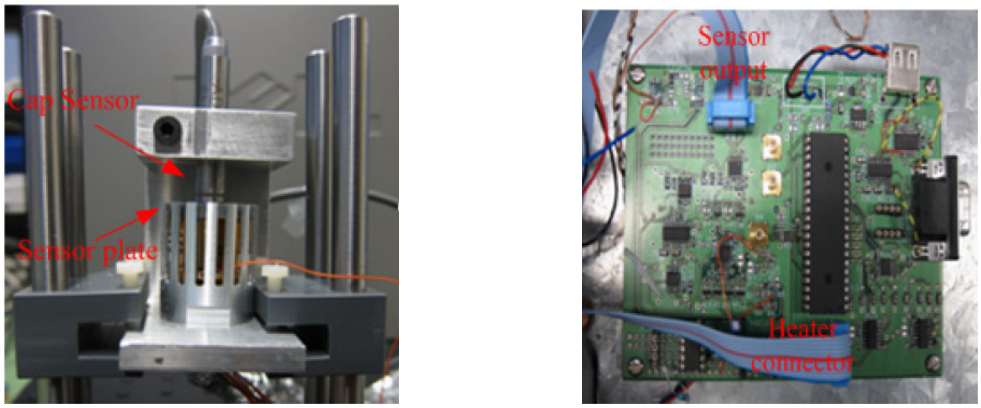


Fig. 3-14. Measurement set-up a) Thermal stepper system (left); b) Control electronics (right);

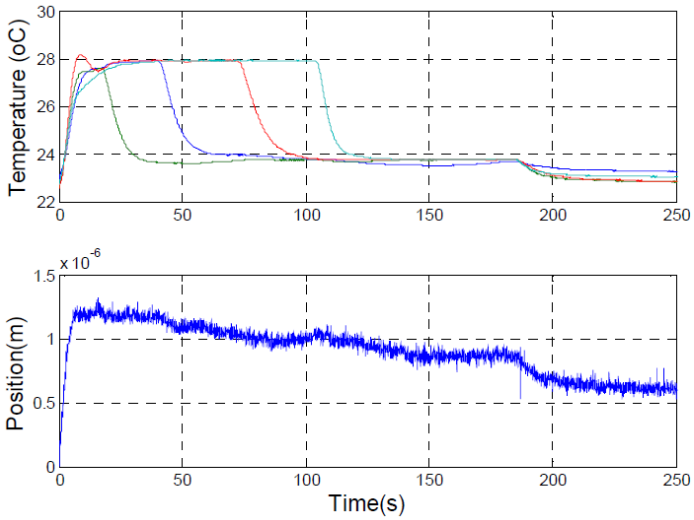


Fig. 3-15. Measured upward stepping action with the 2nd controller

With the setup, stepping actions are performed and the measurement result is shown in Fig. 3-15. The PID controller improves the temperature control performance during the holding phases by greatly reducing the temperature ripples, which validated the theoretical analysis. However, it is noticeable that with similar initial temperature difference the resulting step size (~ 0.62 μm) is smaller than that of the previous work. This is due to the fact that the thermal stepper device used in the measurement is smaller compare to that of the previous one. As a result, the elongation of the thermal elements is smaller with the same temperature difference, as described in Eq. (3-1).

3.4.4. Multi-level control

An optimized version of the controller based on the switch-mode multi-level control has also been built and tested. The maximum input voltage is increased to 10 V and the heater resistance is increased to 200 Ω. As a result, the maximum deliverable power (0.5 W) is assured at a lower current level (50 mA).

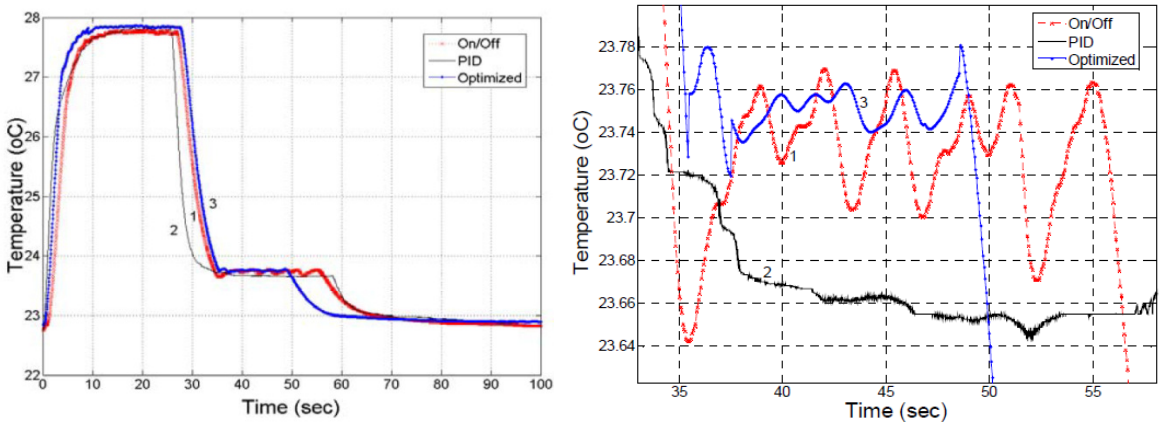


Fig. 3-16. Measurement results of three different controllers (a) during one stepping action; (b) Temperature ripples during the holding phase of the three different controllers.

As a comparison, the temperature measurement results of the different controllers during one stepping action are shown in Fig. 3-16 (a). In the figure, the three different curves marked by 1, 2 and 3, indicate the three different controllers: curve 1 is the PID controller, while curve 2 and 3 are the ON/OFF and the multi-level controllers, respectively. To further check the temperature ripples caused by the different types of controllers, the plot is zoomed-in from 30 sec to 60 sec, which is shown in Fig. 3-16 (b). As can be seen from the results, the optimized controller (multi-level controller) provides smaller temperature ripples compared to the simple ON/OFF controller. Comparing to the PID controller, the ripples are larger. However, the multi-level controller provides a large reduction in the power consumption of the control electronics due to the fact that power amplifiers are not used (section. 3.2.3).

3.4.5. Mechanical stability after alignment

After the alignment, the capacitive sensor has to measure displacement with high accuracy, and the system will not be calibrated again within certain short period of time. In that case, the alignment system should have good enough stability between two calibrations, so that the performance of the capacitive sensor is ensured.

Temperature stability is important for stability of the aluminum structure. In a controlled environment, slip between the clamping elements and measurement electrode has been pointed out as being the next biggest error source in the system. As slip effects are difficult to model correctly, additional experiments have been performed to ensure a stable behavior.

Clamping instability is suspected to occur mainly after an alignment step. The unwanted displacements reduce with time. A realistic result has been obtained by first performing alignment and then directly measuring the position of the electrode. If no displacements occur in this first time span, they are also not to be expected later.

A dedicated test setup has been built to perform the stability measurements. Fig. 3-17 (a) shows the main components. The thermal stepper device (1), which is made out of aluminum, is integrated into an aluminum block (2) which acts as a reference for the measurement and provides a thermal buffer. The relative distance measurement between electrode (3) on top of the reference block and the moving electrode (4) is only slightly affected by the thermal expansion effects in the clamping elements. As these effects cannot be cancelled out completely, the total setup is placed in an aluminum box (5) with 15 mm thick wall, and additionally isolated with 5 cm of isolating foam (6). The temperature stability of the reference block (2) is in the order of 1 mK during 1 hour measurement, without active thermal control. Fig. 3-17 (b) shows temperature at three different places during one hour measurement in which the stabilizing effect of the setup can be clearly seen.

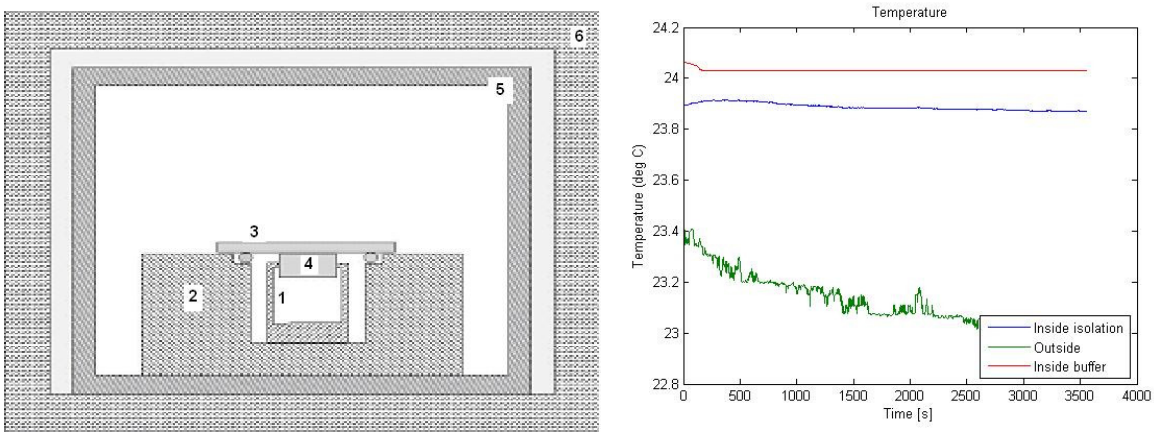


Fig. 3-17. a) set-up of the stability measurement; b) temperatures at different places of the set-up during the stability measurement

A Capacitive-to-Digital Converter [6] is used to measure the position of the electrodes with respect to each other. The system can measure capacitance with a resolution of 15 bits and with high stability. At a nominal distance of ~50 um, the position resolution is limited by the noise level to ~15 nm. This is not enough to prove sub-nanometer resolution. Therefore averaging is used to decrease the noise level and to increase the resolution [7]. The CDC samples at 2550 Hz and outputs the average of 255 samples at 10 Hz. A running average of 10 samples is used in the displacement graph to achieve a noise level of ~100 pm.

Fig. 3-18 (a) shows the measured electrode distance for 60 minutes, immediately after one alignment step. The first part shows a large displacement due to the heat induced by the thermal alignment. During the first 500 seconds the heat spreads evenly throughout the whole structure. After that this process is minimized, while the system very slowly loses heat to the surrounding environment. When we look at the curve from this point of time, as shown in Fig. 3-18 (b), we can observe a distance variation smaller than 1 nanometer during ~50 minutes. Careful inspection of the measurement result does not show any sudden jumps or displacements. The short-term drift (< 5 minutes) is below 100 pm during one hour measurement. Therefore we

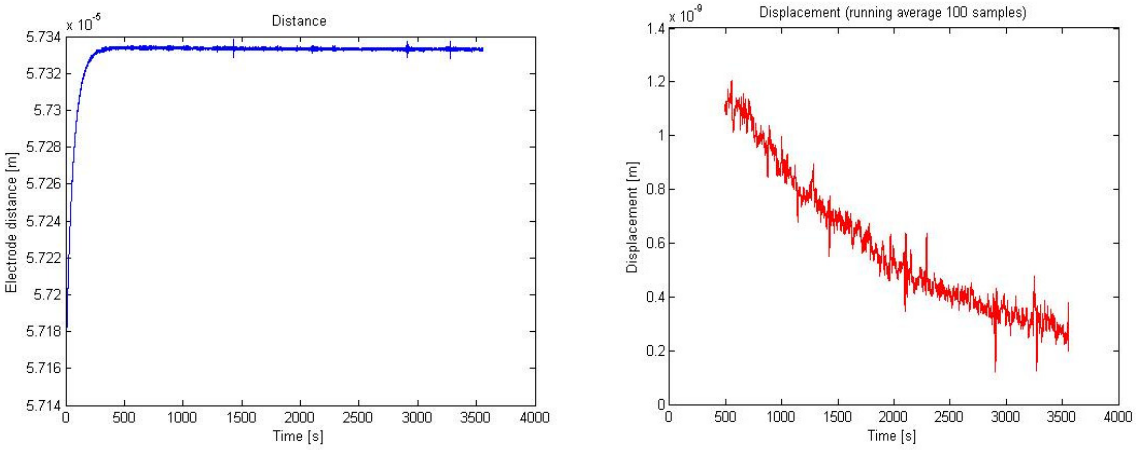


Fig. 3-18. a) long-term stability measurement results (60 min); b) zoom-in of (a) from 500 to 3500 seconds

can conclude that sthe clamping system is suitable for the positioning of sub nanometer resolution capacitive sensors.

3.5 Conclusion

Alignment is a key challenge when using cheap and compact absolute sensors, such as capacitive sensors, in high-precision measurements. The poor alignment accuracy usually causes large pressure on the interface electronics of the sensor, because of the increased requirement of the measurement dynamic range, sensitivity and power-efficiency, etc. To overcome the problem, a new alignment concept based on thermal actuation is proposed in this work. This system has several unique features compared to ordinary alignment systems: 1) it is simple, cheap and robust; 2) due to the proposed special control sequence, the control system can be shut down after alignment, but the aligned position will be maintained stably.

To control the thermal stepper system effectively and in a power-efficient manner, different control algorithms were investigated, including simple open-loop control and various alternatives of closed-loop controls. The pros and cons of different control algorithms were discussed in detail. To validate the investigation, three different controllers were implemented and tested with real thermal stepper device.

The experiments validated the thermal stepper concept: with the proposed special sequence of heating and cooling it is able to make movement of the object under test (in this case it is a sensor plate of a capacitive sensor). More importantly, after the movement, the controller can be shut down completely and the position of the object is maintained stably by the mechanical structure of the thermal stepper device.

Additionally, thought testing of different control algorithms it is proved that the ON/OFF controller is relatively easy to implement and also consumes less power, but it is at the cost of large temperature ripples during the maintaining phase of the temperature (section. 3.2.1). This may lead to unwanted slip or tilt of the object under alignment. A more advanced controller, the PID controller can solve the problem at the expense of more complicated electronics as well as higher power consumption (section. 3.2.2). The high power consumption leads to self-heating of the sensor, which my again cause unwanted movement. In the end, a switch-mode multi-level controller takes advantages of both the simple ON/OFF controller and the more complicated PID controller, leading to a balance on complexity and performance.

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Chapter 4

Precision Capacitance-to-Digital Converter

The investigation in Chapter 2 showed that the combination of a resistor and time provide a precise and stable equivalent capacitive reference. This chapter presents the system-level analysis and design of a precision capacitance-to-digital converter (CDC) based on a charge-balancing Delta-Sigma modulator. The CDC compares the unknown capacitance with a resistor/time reference.

4.1. Introduction

The Delta-sigma-based CDCs, as discussed in Chapter 2, provide high resolution in a power-efficient way, due to their unique oversampling and noise-shaping property [1-5]. The oversampling property spreads the quantization noise power in a wider frequency range, thus reducing the overall noise in the band of interest. Furthermore, the noise-shaping pushes the quantization noise to higher frequency, resulting in an even lower noise power in the signal band [1, 6-8]. The output is a stream of a digital code, namely the *bitstream*. The bitstream is fed into a digital decimation filter which filters the out-of-band noise and returns a digital representation of the measured capacitance.

Conventional Delta-sigma-based CDCs measure the unknown capacitance by comparing it with a well-known reference capacitance. As the measurement result is a function of the reference used, the ultimate achievable performance is limited by the quality of the reference capacitor. The investigation in Chapter 2 showed that it is difficult to find a capacitive reference that is precise and stable enough. Instead, a combination of resistive and time reference can provide high-precision equivalent reference capacitance. Hence, a Delta-sigma-based CDC, which uses the combination of resistive and time reference, is expected to add high precision to the other advantages of conventional Delta-sigma CDC.

4.2 Operating principle

Fig. 4-1 shows a simplified block diagram of the proposed CDC based on charge-balancing Delta-sigma modulation. The typical waveforms at critical nodes are shown in the same figure. Unlike conventional designs, this CDC utilizes precision resistive and time references. The reference resistance is first converted into current by a resistance-to-current converter (RIC) using a reference voltage V_{ref}. Then, the combination of this current and a crystal-based time reference generates an equivalent reference charge. The sensor capacitor is incorporated in a switched-capacitor circuit, which turns the sensor capacitance into a signal charge using the same reference voltage V_{ref}. After an initial reset of the integrator, the modulator balances the

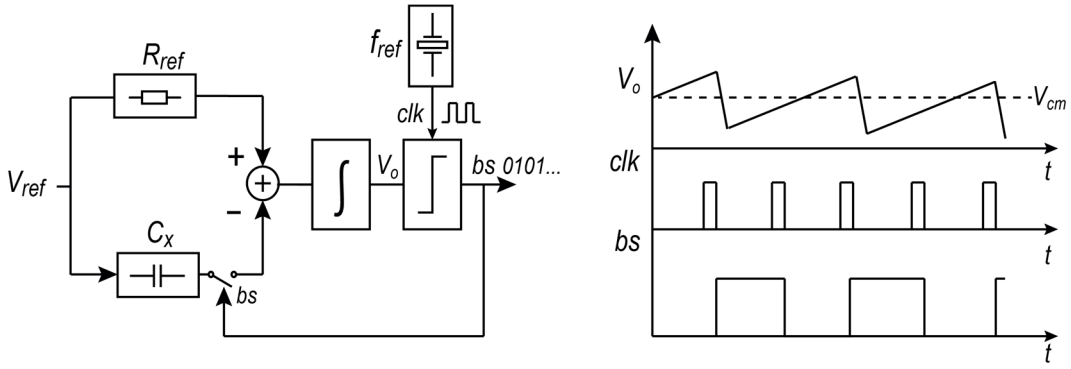


Fig. 4-1. A block diagram of the proposed precision CDC, based on a charge-balancing delta-sigma modulator with resistor/time reference, and typical waveforms at critical nodes.

signal charge against the charge supplied by the reference current. Since both: the signal charge and the reference charge, are proportional to V_{ref}, the output is insensitive to the exact value and the drift of V_{ref}, provided that the drift of V_{ref} is much slower than the conversion time.

This charge-balancing operation is synchronized to the crystal clock. Every clock cycle, a clocked comparator detects the polarity of integrator's output and thus generates a bit of the output bitstream *bs*. This bit determines whether the switched-capacitor circuit will provide a signal charge proportional to V_{ref} and C_x in the next clock cycle. The reference charge is integrated in every cycle, irrespective of *bs*. Thus, if the loop is operated for enough cycles, the accumulated charge in the integrator is approximately zero, meaning that the charge supplied by C_x is balanced by the reference charge (combination of V_{ref}, R_{ref} and t_{ref}). Suppose the loop operates for N cycles and the number of '1' s in the digital bit-stream is N_1, this charge balance can be expressed as:

$$N\frac{V_{ref}}{R_{ref}}t_{ref} = N_1 V_{ref} C_x \tag{4–1}$$

Where N is the total number of operating cycles and N_1 is the number of '1's in the digital bitstream. The average value of the bitstream can be written as:

$$\mu = \frac{N_1}{N} = \frac{t_{ref}}{C_x R_{ref}} \tag{4–2}$$

where t_{ref} is the clock period of the modulator. The bitstream, which is inversely proportional to C_x, can easily be processed in the digital domain, leading to a digital representation of C_x which depends only on precision resistive and time references:

$$C_x = \frac{t_{ref}}{\mu R_{ref}} \tag{4–3}$$

Ideally, if the conversion does not introduce an additional error, the precision of the measurement is purely dependent on the resistive and time references used. Therefore, if the resistive and time references provide high precision, the capacitance-to-digital conversion will

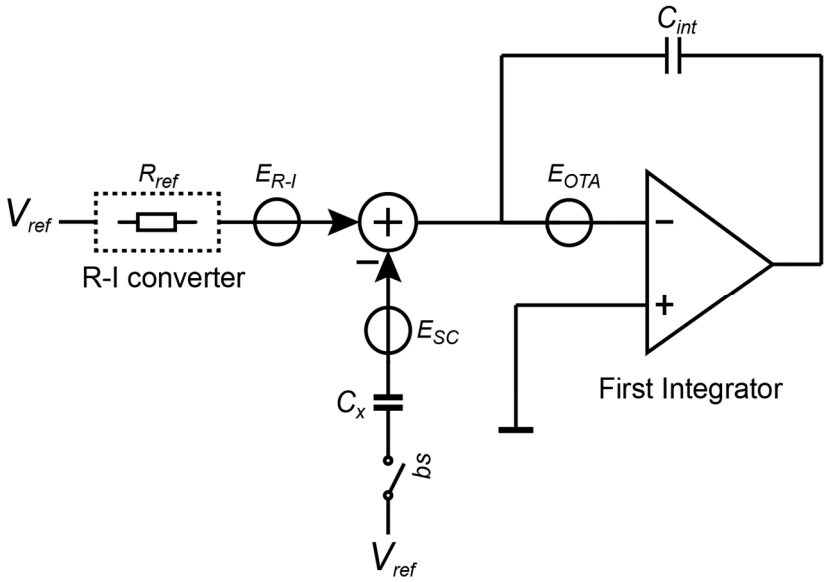


Fig. 4-2. Simplified circuit diagram of the first integrator of a Delta-Sigma CDC, including the three main error sources: E_{R-I}; E_{OTA} and E_{SC}.

also show high precision. Unfortunately, there are always extra errors associated with the conversion. In the next section, various error sources will be identified and discussed.

4.3 Error analysis

As explained in Chapter 2, having a precision reference doesn't necessarily mean that the CDC will provide a precision measurement. The comparison circuit also introduces extra errors, which degrade the performance of the overall system. Therefore, the error sources in the system have to be investigated and corresponding design techniques have to be proposed for their minimization/elimination.

In a higher-order (more than one loop filter) Delta-sigma modulator, the non-idealities of the latter stages are shaped by the preceding integrator(s) [1, 7, 8]. Thus given the fact that the Delta-sigma modulator is carefully designed, it is reasonable to assume that the first integrator dominates the error contribution. Three error sources are identified at the first stage (shown in Fig. 4-2): non-idealities of the: RIC E_{R-I}, the integrator E_{OTA}, and the switched-capacitor (SC) network E_{SC}.

4.3.1. R-I converter non-idealities (offset, offset drift, accuracy)

The R-I converter can either be implemented by directly applying a reference voltage to the reference resistor (passive RIC) or by means of an active RIC. In this work, the RIC is implemented as an active converter so as to prevent the non-idealities of the integrator to affect the quality of the reference current. The circuit diagram of the RIC is shown in Fig. 4-3. Ideally,

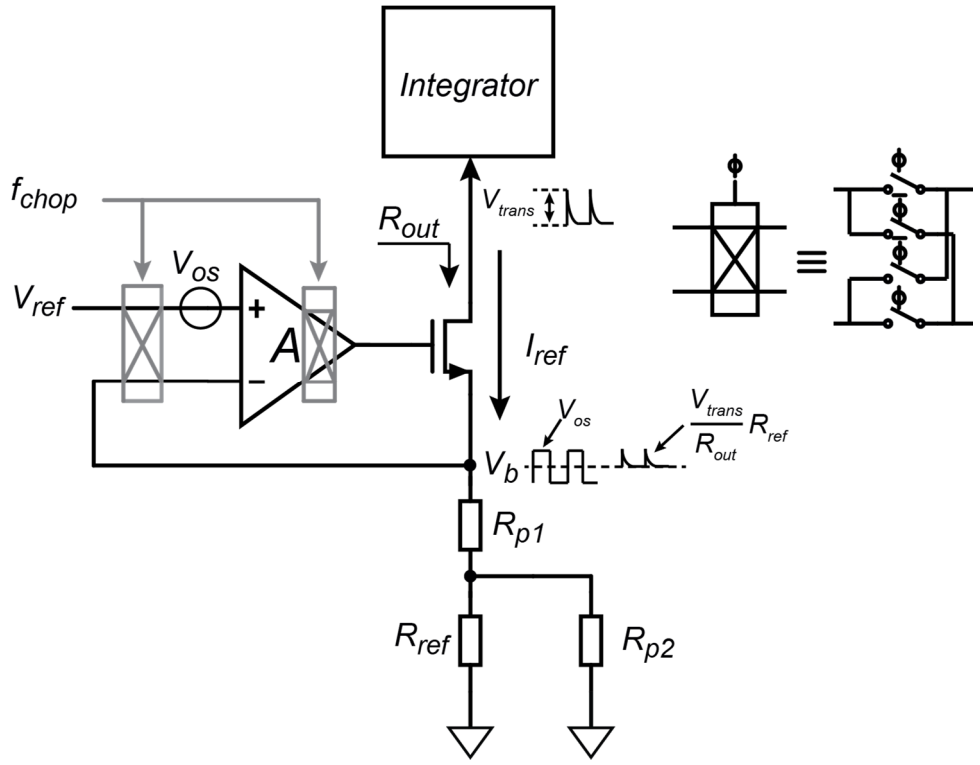


Fig. 4-3. Circuit diagram of the active R-I converter with identified error sources (chopping is applied to minimize the offset of the OTA)

if we assume that the open-loop gain of the OTA is infinite and all transistors are biased in the saturation region, the voltage V_b will be a perfect copy of the reference voltage V_{ref}, due to the negative feedback formed by the OTA and the NMOS transistor. As a result, the RIC generates a reference current which equals to:

$$I_{ref} = \frac{V_{ref}}{R_{ref}} \tag{4-4}$$

where R_{ref} is the off-chip precision reference resistance. Since the RIC is at the input of the CDC, its non-idealities have the same transfer function as the input signal which will not be suppressed by the loop filter. Therefore, those errors have to be minimized for the required performance. In an active RIC, as shown in Fig. 4-3, four error sources can be identified, which affect the precision of the reference current: the offset (V_{os}) of the active component (in this case the OTA); the finite gain (A) of the OTA; the parasitic resistances (R_{p1} & R_{p2}) associated with the PCB routing; and the finite output impedance (Z_{out}) of the RIC.

A. Offset voltage of the OTA:

The offset of the OTA is an additive error, which superimposes an error current on the reference current, as shown:

$$I_{ref}^{*} = \frac{V_{ref} + V_{os}}{R_{ref}} = I_{ref} + \frac{V_{os}}{R_{ref}} \tag{4–5}$$

The extra current error: $I_{error} = \frac{V_{os}}{R_{ref}}$, when injected in the delta-sigma modulator, produces an error in the output digital code. Combining Eq. (4-1) and Eq. (4-5), the measured capacitance can be derived as:

$$C_x^{*} = C_x \left(1 - \frac{V_{os}}{V_{ref} + V_{os}} \right) \tag{4–6}$$

The offset voltage of the OTA contributes to a gain error $C_x \frac{V_{os}}{V_{ref} + V_{os}}$ which degrades the measurement accuracy. Furthermore, due to the presence of the offset voltage V_{os}, the reference voltage V_{ref} is not completely compensated by the ratio-metric measurement any more. As a result, the thermal drift of both the reference voltage and the offset voltage contribute to the final thermal instability of the CDC.

Assume that the offset voltage has a temperature coefficient ∂ [ppm/^{O}C], thus with a temperature change of ΔT, the measured capacitance changes to:

$$C_x^{*}(\Delta T) = C_x \left(1 - \frac{V_{os} \cdot (1 + \partial \cdot \Delta T)}{V_{ref} + V_{os}(1 + \partial \cdot \Delta T)} \right) \tag{4–7}$$

Assuming that the offset voltage is significantly smaller than the reference voltage ($V_{os} << V_{ref}$), the thermal drift with respect to the initial capacitance is calculated as:

$$\frac{\Delta C_x(\Delta T)}{C_x^{*}} = \frac{C_x^{*}(\Delta T) - C_x^{*}}{C_x^{*}} \approx \frac{V_{os} \cdot \partial \cdot \Delta T}{V_{ref}} \tag{4–8}$$

Where $\frac{V_{os} \cdot \partial \cdot \Delta T}{V_{ref}}$ is the temperature drift induced by the OTA offset. Similarly, if the reference voltage V_{ref} has a temperature coefficient β, the extra temperature drift can be estimated as: $\frac{V_{os} \cdot \beta \cdot \Delta T}{V_{ref}}$.

It is clear that both drifts can be suppressed by minimizing the ratio of V_{os} and V_{ref}. The selection of V_{ref}, however, is bounded by the maximum acceptable reference resistor. Hence, the efforts need to be directed to reduce the absolute value of V_{os}.

The traditional methods of reducing the offset include auto-zeroing and chopping. While auto-zeroing interrupts the system operation, the chopping technique provides a continuous-time cancellation without disturbing the system operation. As explained earlier, the current source has to charge continuously the integrator. Hence, chopping is applied in the OTA (Fig. 4-3). The chopping ripples, when injecting to the delta-sigma loop, will be filtered by the low-pass

transfer characteristic of the system. So a dedicated filter is not required in this case. Besides chopping, the OTA has to be carefully designed and a layout with good matching has to be made, so that the initial offset voltage at its input is minimized. The detailed circuit implementation as well as the layout consideration of the RIC will be discussed in Chapter. 5.

B. Finite gain of the OTA:

The accuracy of the RIC depends on the perfect copy of the reference voltage over the resistor reference, indicating as V_b in Fig. 4-3. Ideally, if the OTA has an infinite open-loop gain, the voltage V_b will be a perfect replica of V_{ref}. Then, the generated reference current is determined by the ratio of V_{ref} and R_{ref}. In reality, due to the finite gain (A) of the OTA, V_b deviates from V_{ref}, as shown:

$$V_b = V_{ref} \cdot (1 - \frac{1}{1+A}) = V_{ref} - \frac{V_{ref}}{1+A} \tag{4–9}$$

As the reference voltage value is defined at system-level, the only way to minimize the error is to boost the gain of the OTA. Fortunately, there are many ways to do so, including gain-boosting and multi-stage design of the OTA. The details of the implementation will be further addressed in Chapter. 5. With a finite gain of the OTA, by replacing V_{ref} in Eq. (4-1) with V_b, as shown in Eq. (4-9), the measured capacitance is calculated as:

$$C_x^* = C_x\left(1+\frac{1}{A}\right) \tag{4–10}$$

If the finite gain of the OTA has a temperature coefficient γ, the error term $\frac{C_x}{A}$ also contributes to a thermal drift, which can be derived as:

$$\frac{\Delta C_x(\Delta T)}{C_x^*} = \frac{C_x^*(\Delta T) - C_x^*}{C_x^*} \approx \frac{\gamma \cdot \Delta T}{A} \tag{4–11}$$

Intuitively, this drift can be suppressed by providing enough gain for the OTA, which will be discussed in Chapter. 5.

C. Parasitic resistances:

Another source of error is the parasitic resistances associated with the PCB routing. As shown in Fig. 4-3, two types of parasitic resistances are identified: series resistance due to the PCB tracks to the pin of the chip (R_{p1}), parallel resistance due to the leakage path of the PCB board (R_{p2}). Both resistances alter the reference current, thus causing inaccuracy of the measurement.

Due to the presence of series parasitic capacitance R_{p1}, the measured capacitance is expressed by the following equation (supposing that $R_{p1} << R_{ref}$):

$$C_x^* \approx C_x(1+\frac{R_{p1}}{R_{ref}-R_{p1}}) \tag{4–12}$$

Where $C_x \frac{R_{p1}}{R_{ref}-R_{p1}}$ is the error term which needs to be minimized. Intuitively it can be done by maximizing the ration of R_{p1} and R_{ref}.

The parallel parasitic resistance R_{p2} contributes to another error term as shown:

$$C_x^* = C_x(1-\frac{R_{ref}}{R_{ref}+R_{p2}}) \tag{4–13}$$

Unlike the series parasitic resistance, it is desirable to maximize the parallel parasitic resistance to reduce the error. Hence, the reference resistance has to be selected such that it is significantly larger than the series parasitic resistance while much smaller than the parallel parasitic resistance. This requirement brings certain limitations in the real circuit implementation and the selection of the precision resistor, as will be addressed in Chapter. 5.

D. Finite output impedance of the R-I converter

As explained in Section. 4.2, the current source is continuously charging the integrator of the Delta-sigma modulator, while the switched-capacitor (SC) feedback periodically discharges the integrator when the comparator output is a digital '1'. Since the integrator has a finite speed, during the discharging phase of the SC feedback the virtual ground of the integrator shows transient behavior (Fig. 4-3).

Ideally, the output impedance of the RIC is large enough so that the variation of the virtual ground does not impose any effect on the generated current. However, when the variation is a dynamic signal, it is required that the output impedance of the RIC is large enough at the frequency of the dynamic signal and its harmonics. Assume that the RIC has a finite output impedance Z_{out} which is dependent on frequency, as shown in Fig. 4-3, the accumulated reference-charge error of each clock cycle when the digital output is '1' can be derived as:

$$Q_{error} = \frac{V_{trans}}{Z_{out}(f_{ref})}\int_0^{t_{ref}} e^{-\frac{t}{\tau}}dt = \tau\frac{V_{trans}}{Z_{out}(f_{ref})}\left(1-e^{-\frac{t_{ref}}{\tau}}\right) \tag{4-14}$$

where Q_{error} is the accumulated reference-charge error due to the transient signal at virtual ground and the finite output impedance of RIC. V_{trans} is the maximum voltage jump at the virtual ground, which is determined by the input reference voltage and the capacitive network (will be discussed in Section. 4.5), Z_{out} is the output impedance of the RIC at the reference clock frequency f_{ref}, τ is the time constant of the integrator assuming a first-order transfer function and t_{ref} is the reference clock period of the Delta-sigma modulator.

It is clear that the reference-charge error contributes to the inaccuracy of the final capacitance measurement result. By adding this error into the charge-balance equation (4-1), the expression becomes:

$$N\frac{V_{ref}}{R_{ref}}t_{ref} + N_1 Q_{error} = N_1 V_{ref} C_x \tag{4-15}$$

Substituting Eq.(4-14) in Eq. (4-15), the measured capacitance error can be calculated as:

$$C_{error} = \frac{Q_{error}}{V_{ref}} = \tau \frac{V_{trans}}{R_{out}(f_{ref})V_{ref}}\left(1 - e^{-\frac{t_{ref}}{\tau}}\right) \tag{4-16}$$

Normally, it is required that the clock period is much larger than the time constant of the integrator for complete signal settling, meaning that the exponential term is significantly small. Hence, the equation can be simplified as:

$$C_{error} \approx \tau \frac{V_{trans}}{R_{out}(f_{ref})V_{ref}} \tag{4-17}$$

Both the time constant of the integrator τ and the output impedance Z_{out} are strongly temperature dependent (since the bandwidth of the OTA is highly determined by the temperature). Therefore, this reference-charge error also contributes to the thermal instability of the measurement.

According to Eq. (4-17), there are many ways to reduce this error, including implementation of a fast OTA in the first integrator (thus small τ and small $\frac{V_{trans}}{V_{ref}}$) and fast OTA of the RIC (large R_{out} at high frequency). The detailed implementation of the OTAs will be discussed in Chapter. 5.

4.3.2. Integrator non-idealities (offset, offset drift, settling error, parasitic, finite gain)

The integrator(s) is one of the most important building blocks of the Delta-sigma modulator. The first integrator in a higher order Delta-sigma modulator dominates both the error contribution and the power consumption. Hence, its non-idealities have to be carefully addressed and their effect minimized according to the requirements.

Figure. 4-4 shows a simplified block diagram of the Delta-sigma-based CDC, with all the error sources of the first integrator. There are four main sources identified: the offset, the settling error and the finite gain of the integrator.

A. Offset and offset drift

To suppress the non-idealities of the virtual ground and the errors of the latter stages, the integrator is implemented as an active integrator. The OTA used to implement the integrator, however, contributes to offset V_{os}, as indicated in Fig. 4-5.

The offset can cause errors on both the resistive path and the SC path. As discussed earlier, the RIC is implemented as an active RIC with large output impedance. Hence, the offset of the

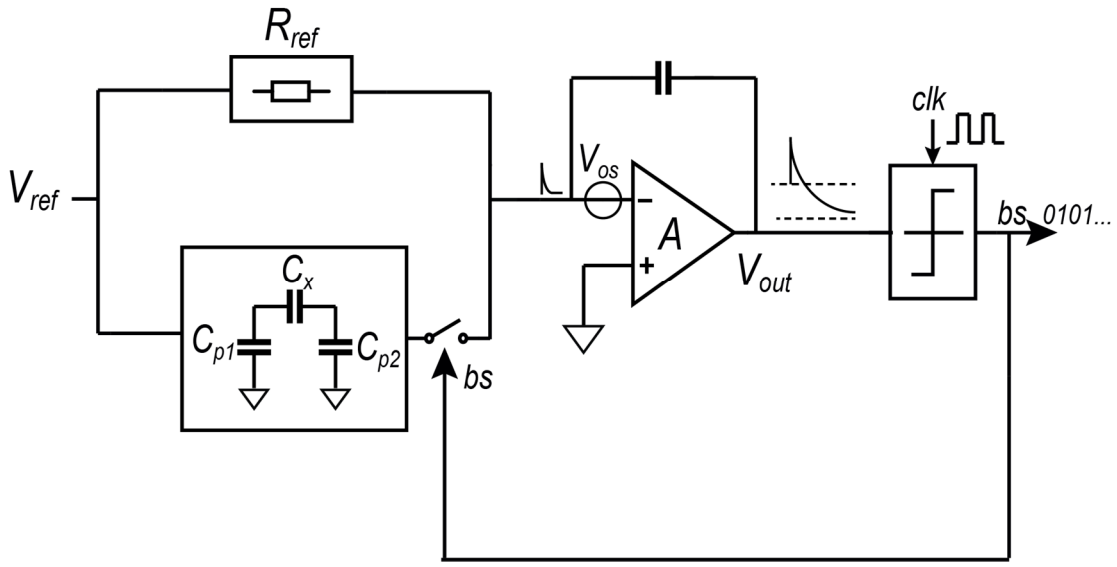


Fig. 4-4. Simplified circuit diagram of the Delta-sigma-based CDC with all the error sources of the first integrator

integrator can hardly cause error in this case. The SC feedback, however, is sensitive to the offset.

First, ignoring the parasitic capacitances, during the sampling phase, the sensor capacitor C_x samples a reference voltage V_{ref} with respect to the common mode voltage V_{cm}. The charge that is stored in the capacitor can be calculated as:

$$Q_x = \left(V_{ref} - V_{cm}\right) C_x \tag{4-18}$$

In the second phase (charge-transfer phase), $\phi_2 = 1$ and $\phi_1 = 0$, the charge that is still stored in C_x can be estimated as:

$$Q_x^{'} = \left(0 - V_{cm} - V_{os}\right) C_x \tag{4-19}$$

According to the charge-conservation law, the integrated charge can be derived by taking the difference of Eq. (4-18) and Eq. (4-19):

$$Q_{int} = Q_x - Q_x^{'} = \left(V_{ref} + V_{os}\right) C_x \tag{4-20}$$

Substituting Eq. (4-20) into Eq. (4-1), the charge-balancing equation becomes:

$$N_1 \left(V_{ref} + V_{os}\right) C_x = N \frac{V_{ref}}{R_{ref} t_{ref}} \tag{4-21}$$

By rewriting the equation, the sensor capacitance C_x can be expressed as:

$$C_x = \frac{N}{N_1} \frac{t_{ref}}{R_{ref}} \left(\frac{V_{ref}}{V_{ref} + V_{os}} \right) = C_x^* \left(\frac{V_{ref}}{V_{ref} + V_{os}} \right) \tag{4-22}$$

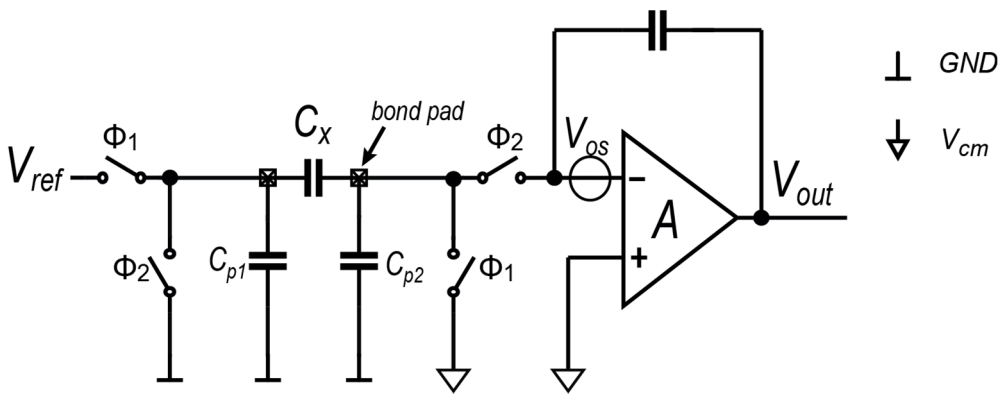


Fig. 4-5. A switched-capacitor (SC) integrator, with offset at the input of the OTA

Where C_x^* is the measured capacitance. From the equation, it is obvious that the offset voltage causes a deviation from the real sensor capacitance and the measured capacitance. Their relation can be written as:

$$C_x^* = C_x\left(1-\frac{V_{os}}{V_{ref}}\right) \tag{4-23}$$

From the above equation, the offset voltage of the integrator results in an offset capacitance in the final measurement result. Moreover, the offset drift due to temperature variation leads to a thermal drift of the measurement. To minimize this effect, it is desirable to minimize the offset voltage of the integrator. As will be discussed in Section. 4.3.3 and Section 4.3.4, system-level chopping and auto-zeroing are used to dynamically suppress the offset of the integrator down to an acceptable level. Besides, careful design as well as layout of the OTA is performed to reduce the initial offset voltage.

As shown in Fig. 4-5, the input capacitance seen by the integrator can be modelled as a sensor capacitance C_x with two parasitic capacitances C_{p1} and C_{p2}, on each side. The parasitic capacitances may have different origin: the sensor structure, the bond-pads, and the layout tracks. The parasitic capacitances cause errors in the measurement result, if the integrator is not ideal.

The parasitic capacitance C_{p1} on the drive side always sees a low impedance node during both the sampling and charge-transfer phases. Hence, its effect can be neglected. The parasitic capacitance on the sense side, however, is sensitive to the non-idealities of the integrator. If we assume that the only non-ideality of the OTA is the offset voltage, during the sampling phase ($\phi_1 = 1$ and $\phi_2 = 0$) the charge stored in C_{p2} is:

$$Q_{cp2} = V_{cm}C_{p2} \tag{4-24}$$

In the charge-transfer phase when the sensor has to transfer charge to the integrator ($\phi_1 = 0$ and $\phi_2 = 1$), the charge that is stored in C_{p2} changes to:

$$Q'_{cp2} = (V_{cm} + V_{os}) C_{p2} \tag{4-25}$$

As a consequence, for each clock cycle (one S/H action) the parasitic capacitance contributes to an error charge if the input offset voltage of the integrator is non-zero. The error charge can be calculated as:

$$Q_{e,int} = Q'_{cp2} - Q_{cp2} = V_{os} C_{p2} \tag{4-26}$$

Due to the error charge, the measured capacitance deviates from the real capacitance, as shown:

$$C_x^* = C_x + \frac{V_{os}}{V_{ref}} C_{p2} \tag{4-27}$$

It is obvious that the capacitance error is a function of the offset voltage and the parasitic capacitance. To reduce or eliminate this error, the most straightforward way is to either reduce the offset voltage or the parasitic capacitance or both. The parasitic capacitance, however, is caused by the layout tracks and the bond-pads. Hence, it is not completely under control. As a result, to reduce this error it is required to reduce the offset voltage of the integrator OTA. This is done by the auto-zeroing and system-level chopping, which will be discussed later.

B. Settling error

During the sampling phase Φ_1, the sensor capacitor C_x is sampled to a reference voltage V_{ref}. Then, in the charge transfer phase Φ_2, the resulting charge is transferred to the integrator. Due to the finite speed of the active integrator, the charge transfer is typically associated with exponential behavior. Fig. 4-6 shows the circuit diagram of the settling phase as well as the exponential waveform of the integrator output.

Assuming that the circuit is a single-pole system the transfer function can be expressed as:

$$H(s) = \frac{A_0}{1 + s\tau} \tag{4-28}$$

where $A_o = \frac{C_x}{C_{int}}$ is the closed-loop gain of the integrator. The time constant of the system can be written as:

$$\tau = \frac{C_{load}}{\beta g_m} \tag{4-29}$$

where $\beta = \frac{C_x + C_{int}}{C_{int}}$ is the feedback factor, g_m is the transconductance of the OTA, C_{load} is the overall load capacitance of the integrator, which can be described as:

$$C_{load} = \frac{C_{int} C_x}{C_{int} + C_x} + C_L \tag{4-30}$$

The time-domain response of the system is:

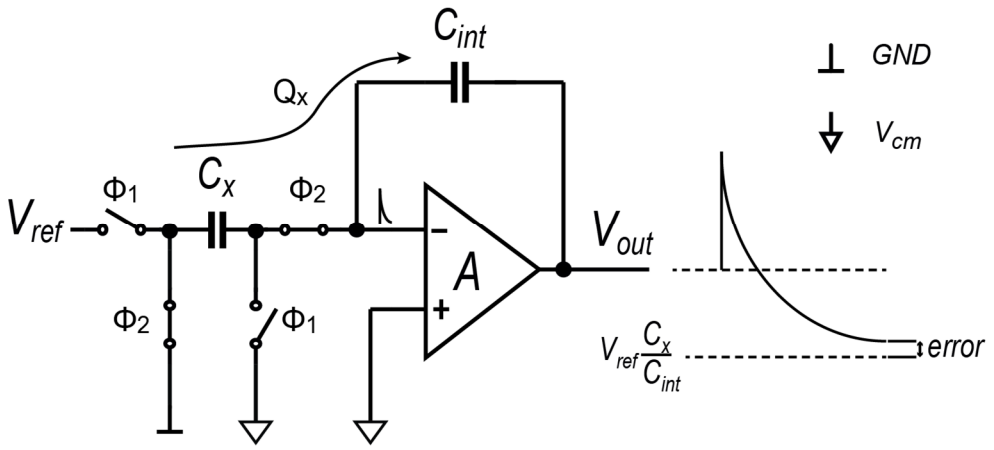


Fig. 4-6. Settling error of an SC integrator during the charge transfer phase

$$V_{out}(t) = \frac{C_x}{C_{int}} V_{ref} \left(1 - e^{-\frac{t}{\tau}} \right) \tag{4-31}$$

Hence, by substituting it to the charge-balancing equation Eq.(4-1), the measured capacitance can be derived:

$$C_x^* = C_x \left(1 - e^{-\frac{t}{\tau}} \right) \tag{4-32}$$

From Eq. (4-32), the measurement accuracy is determined by the exponential settling behavior. If n-bit settling accuracy is required, the following condition has to be met:

$$\tau \le \frac{t_{clk}}{2(n+1)\ln 2} \tag{4-33}$$

where t_{clk} is the clock period for each clock cycle of the Delta-sigma modulator. This condition reveals the minimum transconductance of the OTA used in the integrator for certain load condition and speed requirements. As will be discussed further in Section 4.5, the overall settling of the integrator is also limited by slewing when the driving ability of the OTA is finite. Hence, design margins has to be reserved for complete settling of the signal.

C. Finite gain

The OTA used in the integrator is non-ideal, meaning that its open-loop gain is finite. The finite gain of the OTA, if not well-considered, will cause errors as well as thermal drift in the measurement results. Referring to Fig. 4-7, if the gain of the OTA is finite, the negative input of the OTA (V_{vir}) is not a perfect replica of the positive input. As a consequence, the voltage at the virtual ground deviates from the common-mode voltage, depending on the gain of the OTA, as shown:

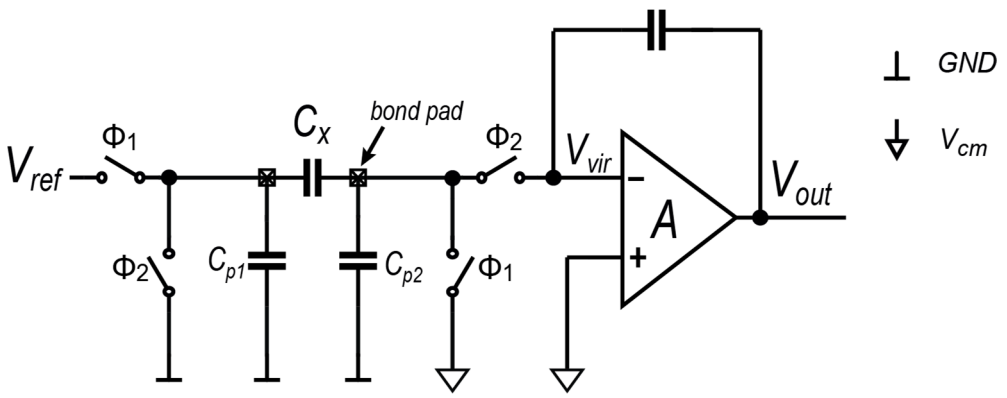


Fig. 4-7. Error of an SC integrator due to finite gain of the OTA

$$V_{vir} = V_{cm}\frac{A}{1+A} = V_{cm}\left(1-\frac{1}{1+A}\right) \tag{4-34}$$

where A indicates the open-loop gain of the OTA. The finite-gain induced error is very similar to that of the offset of the OTA. Hence, considering Eq. (4-23), Eq. (4-27) and Eq. (4-34), the measured capacitance in this case can be written as:

$$C_x^* = C_x\left(1-\frac{V_{cm}}{V_{ref}(1+A)}\right)+\frac{V_{cm}}{V_{ref}(1+A)}C_{p2} \tag{4-35}$$

The first term is due to the impact of the sensor capacitance as a result of the imperfect virtual ground. The second term is due to the impact of the parasitic capacitance on the sense side. Since the parasitic capacitance is not under control, the only way to minimize the error is to boost the gain of the OTA so that these errors become negligible. The gain-boosting of the OTA is discussed in Chapter. 5.

4.3.3. SC network non-idealities

Due to the parasitic capacitive feed-though and the redistribution of the channel charge at the clock-off edge, the MOS switch of the switched-capacitor (SC) feedback contributes to the charge-injection error [9, 10]. The charge-injection, as explained in [9], is a function of the voltages across the switch, the threshold voltage, dimension and oxide capacitance of the transistor that is used to realize the switch. The charge-injection can be described as:

$$Q_e = WLC_{ox}\left(V_{gs}-V_{th}\right) \tag{4-36}$$

where W and L are the dimensions of the transistor, C_{ox} is the oxide capacitance, V_{gs} is the gate-source voltage across the switch, V_{th} is the threshold voltage of the transistor. The injected charge error will split into two paths, as shown in Fig. 4-8. A portion of the charge will be injected to the input while the rest flows to the output, depending on the impedances seen by

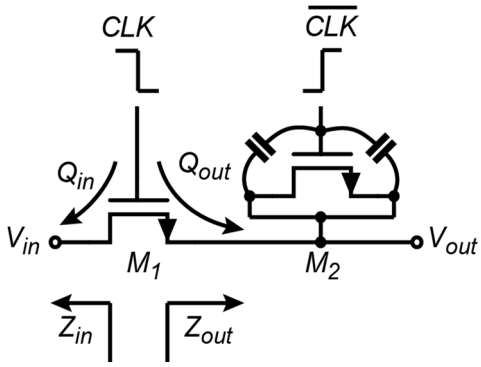


Fig. 4-8. Charge-injection error when the switch is off (a half-sized dummy switch is added to reduce the error)

the switch. Ideally, if the two impedances Z_{in} and Z_{out} are equal, the charge will equally split into the two paths, as shown:

$$Q_{in} = Q_{out} = \frac{Q_e}{2} \tag{4-37}$$

The threshold voltage, the dimension and oxide capacitance of the transistor are temperature dependent. Hence, the offset is also a function of temperature, resulting in an extra thermal drift of the measurement result, as shown in the following equation:

$$C_x^* = C_x + C_{os}(T) \tag{4-38}$$

Traditional solution to reduce the charge-injection error includes adding a half-sized dummy switch next to the critical switch [9], or performing two consecutive measurements with opposite polarities of the excitation signal [11].

The first method requires that the charge injection to both sides of the switch are equal [9]. This, however, can hardly be achieved. In the case of a SC integrator, the drive side of the switch is a reference voltage, meaning a good low-impedance node. The sense side is the virtual ground of the OTA. Hence, its' impedance is highly depends on the OTA. As a result, the two impedances Z_{in} and Z_{out} can hardly be identical. So the charge injection to the two sides of the switch is not equally split. In this case, adding half-sized dummy switch is not very effective.

The second method relays on that the charge-injections in two consecutive measurements are identical [11]. If this is the case, during the first measurement when the excitation voltage is positive, the measured capacitance can be written as:

$$C_{x1}^* = C_x + C_{os} \tag{4-39}$$

After that, in the second measurement, a negative excitation voltage is applied, so that the measured capacitance becomes:

$$C_{x2}^* = -C_x + C_{os} \tag{4-40}$$

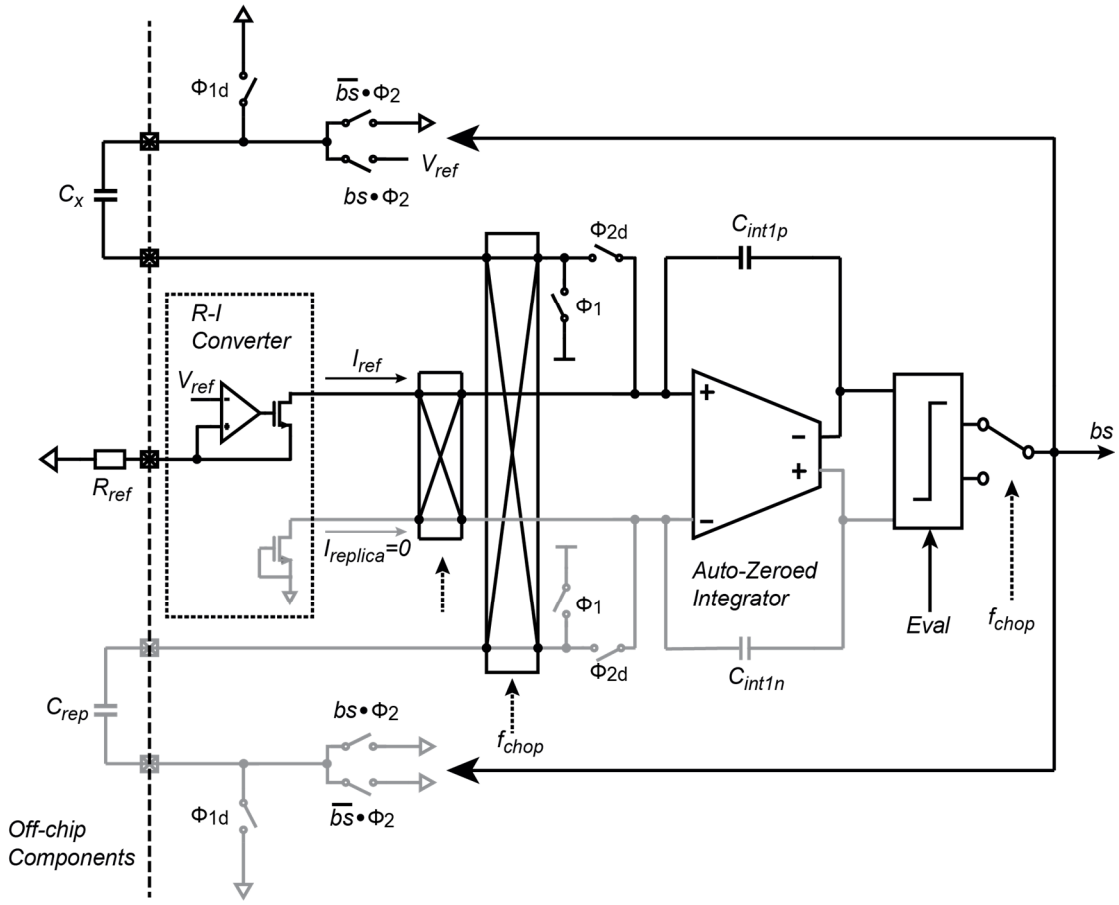


Fig. 4-9. The pseudo-differential implementation of the precision CDC with system-level chopper

If the charge-injection remains the same in the two measurements, the offset capacitances in the two measurements are identical. Hence, by taking the difference of the two measurements, the effect of the charge injection can be compensated:

$$C_x^* = \frac{C_{x1}^* - C_{x2}^*}{2} = C_x \tag{4-41}$$

Apart from the charge-injection error, this method can also be used to suppress the offset and the low-frequency error of the integrator, provided that the two consecutive measurements are fast enough. However, two measurements result in a doubled conversion time. Besides, it is hard to guarantee that the offset or charge-injection will be the same during the two measurements. Hence, the compensation effect is limited by the conversion speed and the variation of the errors.

Another effective way of dealing with the charge-injection error is to implement a differential structure. The charge-injection in a differential circuit becomes a common-mode error, which can be greatly suppressed by the high common-mode rejection ration (CMRR) of the circuit. As shown in Fig. 4-9, the CDC in this work has been implemented as a pseudo-differential circuit. To this end, a replica input network (shown in grey in Fig. 4-9) is added. The replica of

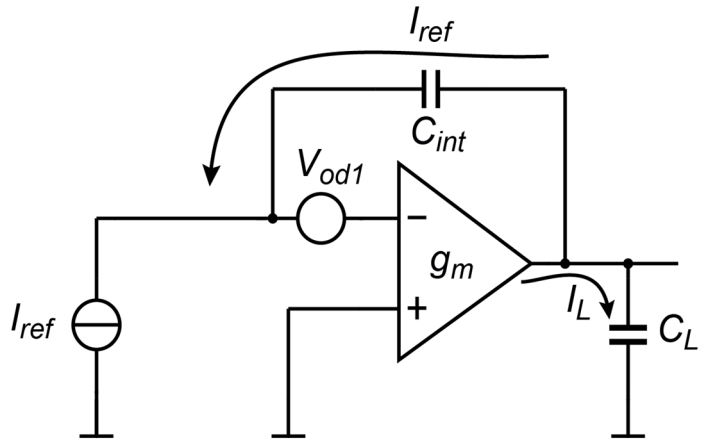


Fig. 4-10. The overdrive voltage at the input of the integrator due to continuous reference current.

the output stage of the current source balances the parasitic seen by the chopper without contributing any current. A SC network built around a capacitor C_{rep} that is nominally equal to C_x reduces differential charge-injection errors without contributing signal charge. To make sure that the charge-injection error is signal independent, a bottom-plate sampling is implemented by delaying the control clock of the critical switches [1, 9].

Unfortunately, even with differential circuit, it is still possible that the charge-injection mismatch in the two input paths can lead to a measurement error. The mismatch can be due to the mismatch of the switch transistors or the parasitic of the connection tracks [10]. To deal with the mismatches of the differential inputs, a system-level chopping is implemented by periodically swapping the two input paths as well as the output bitstream, as shown in Fig. 4-9. In this way, the mismatch error can be averaged out by the system-level chopping [4].

4.3.4. Continuous current induced error

As depicted in Section.4.2, the reference current source is continuously connected to the input of the integrator, while the unknown charge is supplied by a switched capacitor circuit that is controlled by the comparator. This is to avoid the switching of the current source so as to eliminate the timing-induced errors, such as clock jitter and finite switching speed of the switch from injecting extra error charge into the system [12-14].

However, as shown in Fig. 4-10, connecting the current source continuously to the integrator has an intrinsic problem. Since the same current with opposite sign has to be supplied by the OTA, it generates an overdrive voltage at the input of the integrator which is determined by the level of the reference current and the transconductance of the OTA. The magnitude of the overdrive voltage can be estimated as:

$$V_{od} = \frac{I_{ref}}{g_m}\left(1+\frac{C_L}{C_{int}}\right) \tag{4-42}$$

The first term $\frac{I_{ref}}{g_m}$ is due to the above-mentioned reason. The second term $\frac{I_{ref}}{g_m}\frac{C_L}{C_{int}}$ is due to the presence of a load capacitance. When a current is continuously charging the feedback capacitor C_{int}, the output voltage will change (ramp up or down). To make this change, the load capacitor also needs to be charged. The only way to charge the load capacitor is to draw current from the OTA. Therefore, the total current drawn from the OTA is no longer I_{ref}, but with an extra load current I_L. The ratio between I_{ref} and I_L is the ratio between C_{int} and C_L.

Since the overdrive voltage is always presents at the virtual ground of the integrator, it will be sampled by the SC feedback and thus contribute to the measurement error. The charge error Q_e for each sample-and-hold cycle can be calculated as:

$$Q_e = V_{od}C_x = \frac{I_{ref}C_x}{g_m}\left(1+\frac{C_L}{C_{int}}\right) \tag{4-43}$$

By substituting Eq. (4-43) into Eq. (4-1), the new charge-balancing equation can be derived as:

$$N_1(V_{ref}C_x + V_{od}C_x) = N\frac{V_{ref}}{R_{ref}f_{ref}} \tag{4-44}$$

By rewriting the above equation, the measured capacitance C_x^* can be represented as the sum of the sensor capacitance C_x and an error capacitance that is dependent on the overdrive voltage:

$$C_x^* = C_x + \frac{V_{od}}{V_{ref}}C_x \tag{4-45}$$

The overdrive voltage, as shown in Eq. (4-42) is a function of the transconductance of the OTA. Hence, it is strongly temperature dependent, leading to a temperature dependent error (thermal drift).

The overdrive voltage is determined by a constant reference current and the g_m of an OTA, thus it is an offset-like error. The drift of this error caused by the drift of g_m is very similar to an offset drift. Therefore, intuitively it is possible to suppress this error with classical offset-compensation techniques, such as chopping, auto-zeroing or correlated double sampling (CDS) [15].

Chopping is one of the most commonly applied solutions to reduce offset errors. The idea of chopping is to modulate the signal to high frequency before adding it to the offset error. Then, after the signal processing chain, e.g. amplification, the signal is demodulated back to the baseband while the offset remains modulated to high frequency. In this way, the offset can be distinguished from the signal and compensated by a low-pass filter [1, 10, 15]. However, this intrinsic overdrive error is not entirely the same as an offset error. It is associated with the signal, or in another word, is part of the signal. As sown in Fig. 4-11, when modulating the signal, the overdrive error is also modulated. Hence, chopping operating cannot separate this error from the signal.

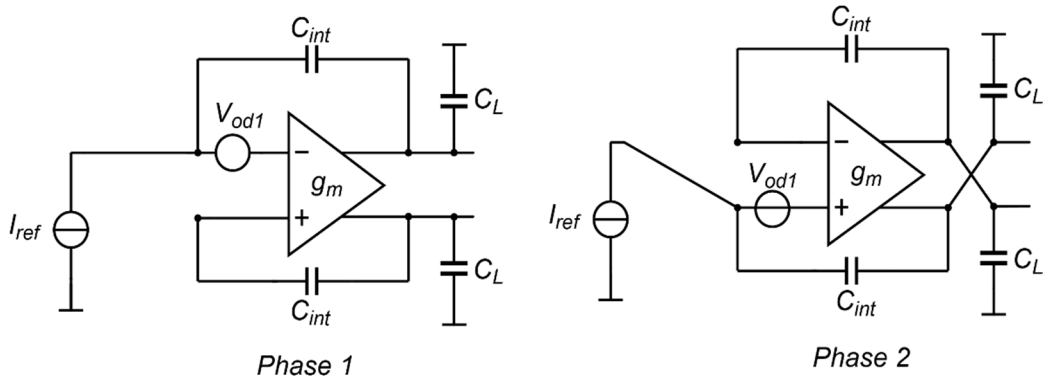
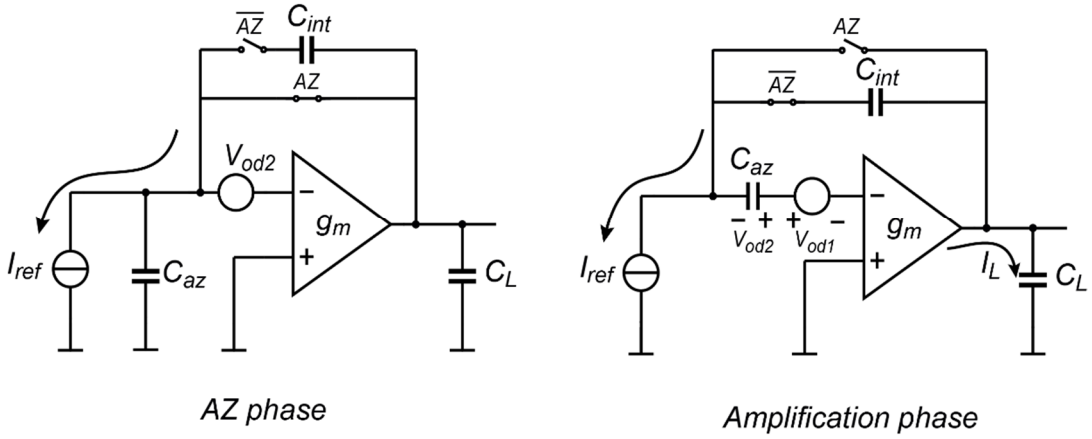


Fig. 4-11. Chopped integrator to compensate for the continuous-current-induced overdrive error



(a) (b)

Fig. 4-12. Auto-zeroed integrator to compensate for the continuous-current-induced overdrive error: a) auto-zeroing phase; b) amplification phase

Apart from chopping, another popular technique is auto-zeroing (AZ). A complete AZ cycle consists of two phases: the auto-zero phase in which the offset error is measured and stored; the compensating phase in which the signal passes the processing chain and the offset is subtracted from the signal [10, 15]. As shown in Fig. 4-12 (a), during the AZ phase, the integrator is configured as a unity-gain buffer and the overdrive voltage due to the continuous current is stored in an AZ capacitor C_{AZ}. After the AZ phase, the integrator resumes its normal operation (integration phase), in which the AZ capacitor is in series with the overdrive voltage so that the effect of the overdrive voltage is compensated. Ideally, if the compensation is perfect, the SC feedback will see a clean virtual ground. However, it is noticeable from Fig. 4-12 that the overdrive voltages in the AZ phase is not identical to that of the amplification phase.

During the AZ phase, as the integrator is configured as a unity-gain buffer, there is no load current to C_L. Hence, the overall current supplied by the OTA is I_{ref}, resulting an overdrive voltage as:

$$V_{od2} = \frac{I_{ref}}{g_m} \tag{4-46}$$

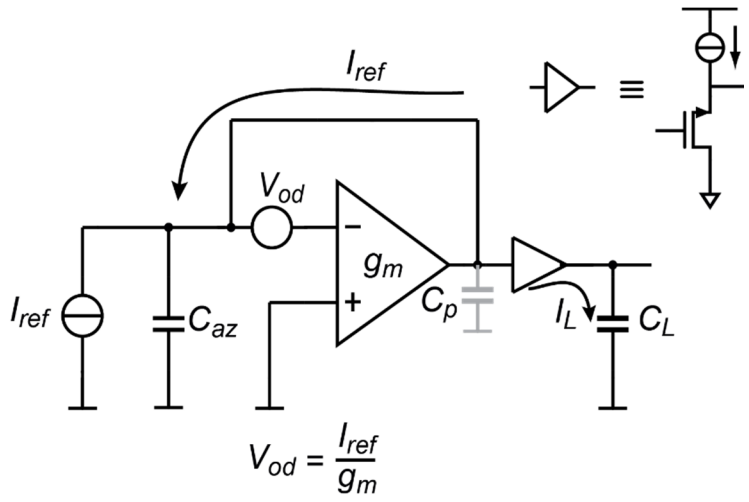


Fig. 4-13. Auto-zeroed integrator with output source follower to minimize the effect of load capacitor

During the amplification phase, however, the OTA has to supply an extra current I_L to the load capacitor. As a consequence, the overdrive voltage at the virtual ground is the same as Eq. (4-42). The difference between Eq. (4-42) and Eq. (4-46) leads to a residual overdrive error which amounts to:

$$V_{od,res} = \frac{I_{ref}}{g_m}\frac{C_L}{C_{int}} \tag{4-47}$$

It is clear that the residual offset is due to the different load conditions during the two phases. To eliminate this error, the most straightforward way is to create the same load condition in the AZ phase. This has to be done by adding a replica of the integration capacitor during the AZ phase, so that there will be the same level of load current. However, the matching between the integration capacitor and its replica determines the effectiveness of such solution. Moreover, such solution requires much more complicated clocks.

Another way of dealing with the problem is to minimize the load capacitance C_L. As shown in Fig. 4-13, this can be done by adding a simple source follower at the output of the integrator. In this case, the load current is provided by the source follower. The load capacitor of the integrator is only the parasitic capacitance seen at this node, which can be minimized by careful layout. The source followers at the output only need to drive relatively small capacitor, thus they don't add significant power to the system. In addition, their non-idealities, e.g. noise, mismatch, offset, are shaped by the integrator and thus become negligible.

Fig. 4-14 shows the complete implementation of the auto-zeroed frontend stage. During the AZ phase, the CDC is 'frozen' (the states of the integrators are preserved), and the offset voltage is stored in the AZ capacitors C_{AZ1} and C_{AZ2}. After the AZ, the modulator resumes its normal operation while the offset voltage is compensated by the voltage stored on the AZ capacitors. By properly sizing the source follower and careful layout, it is possible to make the residual offset negligible. Bottom-plate sampling is applied to make the charge-injection error signal independent.

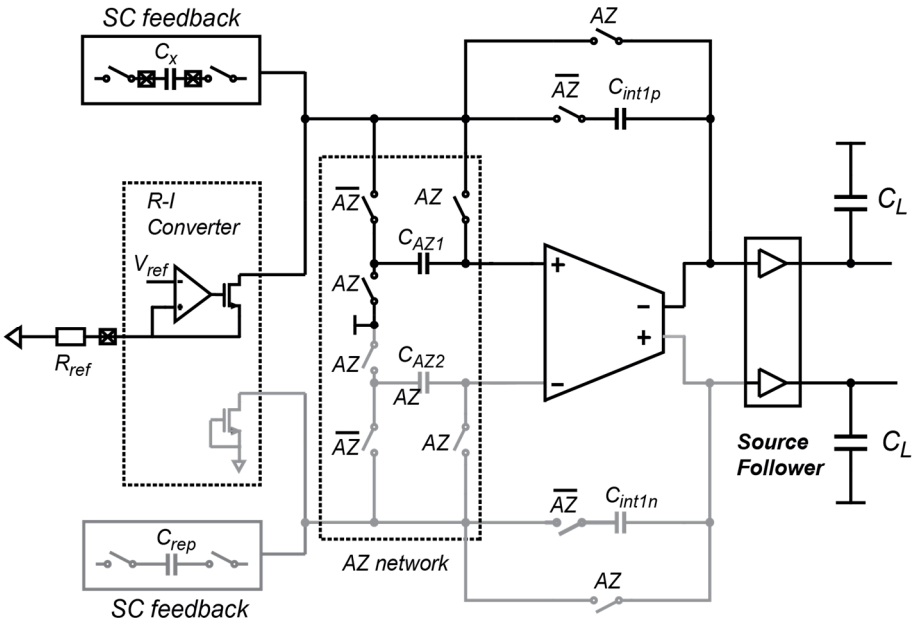


Fig. 4-14. Complete implementation of the auto-zeroed frontend stage with source follower to minimize the effect of the load capacitor

4.4 Noise analysis

In the previous section, the non-idealities of the proposed CDC have been analyzed in detail, followed by proposed solutions and techniques to minimize the errors. In this section, an in-depth noise analysis is presented, which defines the noise budget of each building block and the optimal structure of the Delta-sigma CDC.

In the analysis, it is assumed that the noise of the CDC is dominated by the noise at the input of the overall system, namely the frontend stage. Fig.4-15 shows a simplified circuit diagram of the frontend stage, with its noise paths indicated. Generally, there are three main noise paths: noise from the reference current source (path 1), noise from the SC network (path 2) and the input voltage noise of the OTA used to implement the integrator.

4.4.1 Noise due to the R-I converter

As mentioned earlier, an active RIC is preferred to convert the resistive reference to a current reference. The schematic of the RIC is shown in Fig. 4-16 (a). As the generated current is integrated by the integrator of the Delta-sigma modulator, the noise of the reference current source directly affects the noise performance of the CDC. As shown in Fig. 4-16 (a), two main noise sources are identified. One is the noise due to the OTA and the other is from the thermal noise of the resistive reference R_{ref}. The equivalent current noise density can be estimated as:

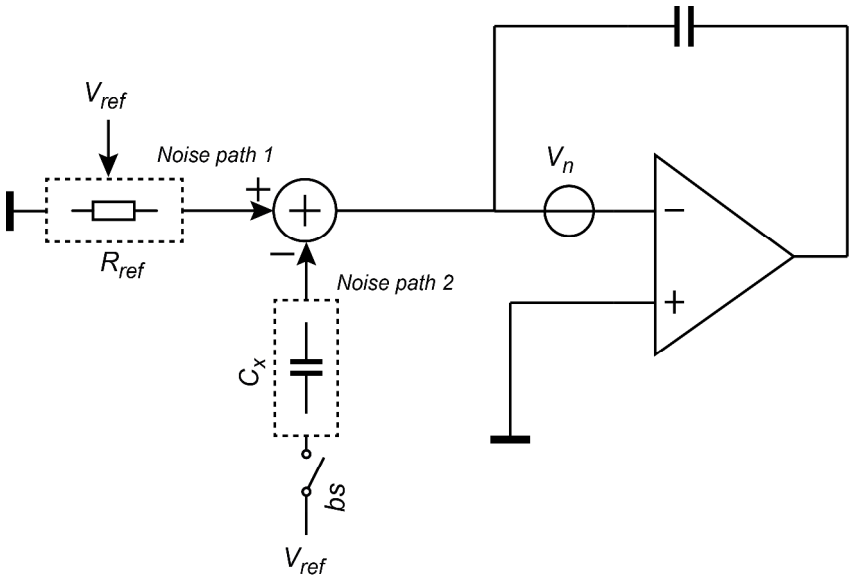


Fig. 4-15. A simplified circuit diagram of the frontend stage, including the main noise sources

$$I_{n,eq}^2 = \frac{4kT}{R_{ref}} + \frac{16kT}{3g_{m2}R_{ref}^2} \tag{4-48}$$

Where g_{m2} is the trans-conductance of the OTA in the RIC. The current noise is integrated by the integrator, whose transfer function is effectively a Sinc filter in the frequency domain [16], as shown:

$$H\left(f, t_{ref}\right) = t_{ref} \sin c\left(ft_{ref}\right) = t_{ref} \frac{\sin(\pi ft_{ref})}{\pi ft_{ref}} \tag{4-49}$$

Therefore, the noise power due to the current noise can be calculated as:

$$\overline{Q_{n2,Iref}^2} = t_{ref}^2 \int_0^\infty I_{n,eq}^2 \cdot H^2(f, t_{ref}) df = \left(\frac{4kT}{R_{ref}} + \frac{16kT}{3g_m R_{ref}^2} \right) \frac{t_{ref}}{2} \tag{4-50}$$

Additionally, the integrated current noise causes a voltage noise at the virtual ground of first integrator, which can be estimated as $V_{n,Iref} = I_{ref}/g_m$. This noise, fortunately, is much smaller compare to other noise source in most of the cases when a large g_m is implemented for the OTA. Hence it can be ignored. It is also important to mention that the resistance R_{ref} is selected based on the reference time period t_{ref} in order to guarantee the operation of the charge-balancing loop. E.g. larger t_{ref} would require larger R_{ref}, which in turn results in a smaller accumulated charge noise.

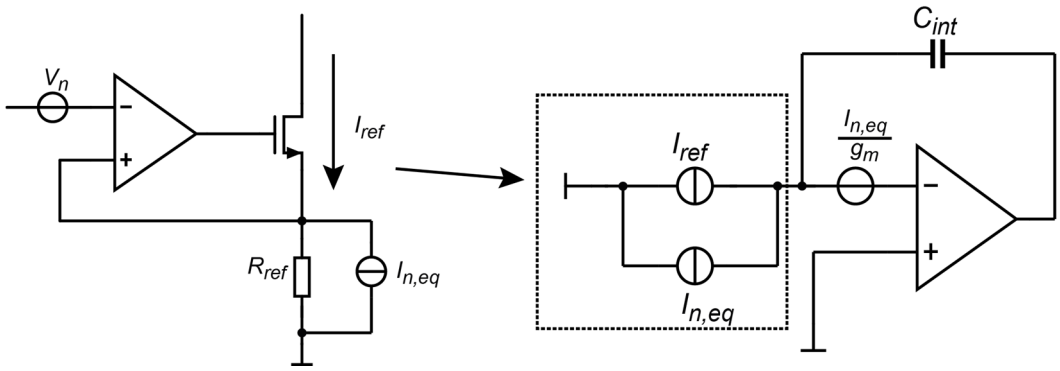


Fig. 4-16. (a) Schematic of the R-I converter, including its noise sources; (b) The frontend integrator of the proposed CDC, with the R-I converter connected at its input

4.4.2 Noise due to SC feedback

Due to the sample and hold operation of the switched capacitor (SC) integrator, the thermal noise of the switches and the operation trans-conductance amplifier (OTA) are sampled and integrated which affects the overall noise performance of the CDC. During the sampling phase, the noise of the switch on-resistance R_{on} is sampled on the capacitor C_x. Provided that the time constant $R_{on}C_x$ formed by the switched-capacitor circuit is much smaller than the sampling period, the resulting charge noise can be estimated as [17]:

$$\overline{Q_{n1}^2} = \int_0^\infty \frac{4kTR_{on,tot}}{1+\left(2\pi f R_{on,tot} C_x\right)^2} \cdot C_x^2 df = kTC_x \tag{4-51}$$

Where k is the Boltzmann constant and T is the absolute temperature in Kelvin. During the integration phase, both the switch noise and the OTA noise will be integrated. Assuming that the load capacitor is much smaller than the equivalent input capacitor, the integrator has a low-pass characteristic whose time constant is $(R_{on}+1/g_m)C_x$. Hence the charge noise due to the switch on-resistance can be calculated as:

$$\overline{Q_{n2}^2} = \int_0^\infty \frac{4kTR_{on,tot}}{1+\left(2\pi f (R_{on}+1/g_m) C_x\right)^2} \cdot C_x^2 df = kTC_x \cdot \frac{x}{1+x} \tag{4-52}$$

where $x = R_{on} \cdot g_m$ defines the relative contribution from the switches and the OTA noise to the total noise [17]. Similarly, the thermal noise of the OTA is integrated and filtered by the same transfer function. Assuming that the OTA noise is dominated by the input transistor pair, whose noise power can be estimated as $\frac{16}{3}\frac{kT}{g_m}$. Thus the integrated noise charge can be written as:

$$\overline{Q_{n3}^2} = kTC_x \cdot \frac{4/3}{1+x} \tag{4-53}$$

As explained in Section 4.4, the proposed CDC has a pseudo-differential structure, hence the noise due to the switch on-resistances have to be doubled, while the noise due to the OTA remains the same. The total noise charge is then calculated as:

$$\overline{Q_{n,S/H}^2} == \overline{Q_{n1}^2} + \overline{Q_{n2}^2} + \overline{Q_{n3}^2} = kTC_x \cdot (2 + \frac{2x}{1+x} + \frac{4/3}{1+x}) \tag{4-54}$$

4.4.3 Noise due to the auto-zeroing operation

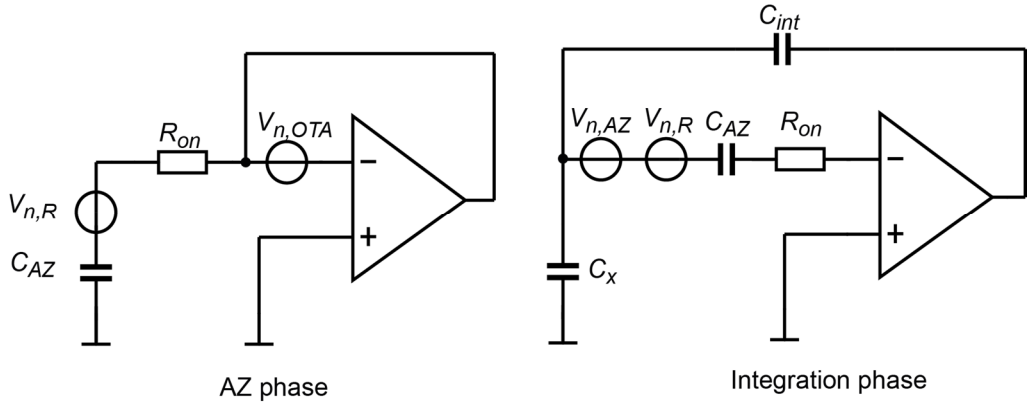
As discussed in Section. 4.4, the CDC performs periodical auto-zeroing (AZ) to cancel the overdrive voltage due to the continuous current integration. The AZ operation, unfortunately, introduces extra noise. Fig. 4-17 shows the noise model of the AZ operation. During the AZ phase (Fig. 4-17 (a)), the noise of both the switch on-resistance R_{on} and the OTA ($V_{n,OTA}$) are sampled on the AZ capacitor C_{AZ}. Similar to Eq. (4-51), Eq. (4-52) and Eq. (4-53), the noise voltage stored on C_{AZ} due to the AZ operation is derived as:

$$\overline{V_{n,AZ1}^2} = \int_0^\infty \frac{4kTR_{on} + \frac{16}{3}\frac{kT}{g_m}}{1 + \left(2\pi f (R_{on} + 1/g_m) C_{AZ}\right)^2} df = \frac{kT}{C_{AZ}} (\frac{x}{1+x} + \frac{4/3}{1+x}) \tag{4-55}$$

After the AZ, the CSI resumes its normal operation. The AZ capacitor is connected to the virtual ground of the OTA, as shown in Fig. 4-17 (b). During the integration phase, this voltage noise appears at the virtual ground and is sampled by the SC feedback. Hence, it leads to a noise charge which amounts to:

$$\overline{Q_{n,AZ1}^2} = \overline{V_{n,AZ}^2} C_x^2 = kT \frac{C_x^2}{C_{AZ}} (\frac{x}{1+x} + \frac{4/3}{1+x}) \tag{4-56}$$

The switches at the virtual ground for AZ operation contribute noise $V_{n,R}$ the same ways as the OTA noise (Fig. 4-17 (b)), thus its contribution can be derived as:



(a) (b)

Fig. 4-17. (a) Noise model during the AZ phase; (b) Noise model during the integration phase

$$\overline{Q_{n,AZswitch}^2} = kTC_x \times \frac{x}{1+x} \tag{4-57}$$

Again, due to the pseudo-differential natural, the total noise power has to be doubled, which amounts to:

$$\overline{Q_{\mathrm{n,AZ\_tot}}^2} = 2kTC_{\mathrm{AZ}} \cdot \left(\frac{\mathrm{C_x}}{\mathrm{C_{AZ}}}+1\right)^2 \cdot \left(\frac{\mathrm{x}}{1+\mathrm{x}}+\frac{4/3}{1+\mathrm{x}}\right) + 2kTC_{\mathrm{x}} \cdot \frac{\mathrm{x}}{1+\mathrm{x}} \tag{4-58}$$

4.4.4 System-level design of the Delta-sigma modulator

Based on the analysis above, the overall thermal noise of the CDC can be derived, assuming that all the noise sources are uncorrelated:

$$\overline{Q_{n,overall}^2} = \overline{Q_{n,S/H}^2} + \overline{Q_{n,AZ\_tot}^2} + \overline{Q_{n2,Iref}^2} \tag{4-59}$$

In an oversampled Delta-sigma CDC, the thermal noise is suppressed by the number of operating cycles *N*, thus the final thermal noise becomes:

$$\overline{Q_{n,final}^2} = \frac{\overline{Q_{n,overall}^2}}{N} \tag{4-60}$$

To determine the minimum number of cycles *N* needed to achieve the required resolution, it should be taken into account that the usable input range of the Delta-sigma drops when the order of the modulator increases. For 2nd order loop, the normalized input range (with respect to C_x) is around 0.75, while for 3rd order it shrinks to about 0.67. Thus for 2nd and 3rd order loops, the signal charges are $Q_{sig,2nd} = 0.75Q_{C_s}$ and $Q_{sig,3rd} = 0.67Q_{C_s}$, respectively. The signal-to-noise ratio (SNR) is calculated according to:

$$SNR = 20 \cdot \log_{10} \frac{\overline{Q_{sig}^2}\sqrt{N}}{\sqrt{\overline{Q_{n,S/H}^2} + \overline{Q_{n,AZ\_tot}^2} + \overline{Q_{n2,Iref}^2}}} \tag{4-61}$$

Fig. 4-18 shows a simulation result of the required number of operating cycles *N* to suppress the thermal noise (blue and green curves), as a function of the required effective-number-of-bit (ENOB). Due to the smaller available input range, 3rd-order loop requires slightly larger *N* for the same ENOB.

In addition to the thermal noise, the Delta-sigma modulator contributes to quantization noise. Behavior simulation of the modulator is performed in Matlab, where the input of the modulator is swept and the required number of cycles to bring down the quantization noise for specific resolution are plotted (red and black curves) as a function of the ENOB (Fig. 4-18). To make the design energy-efficient, it is suggested the thermal noise to slightly dominate the overall noise performance [18]. At the target ENOB>18-bit, 2nd-order loop just starts entering the thermal noise limited region. Hence 3rd-order loop is selected in this work for a more conservative design.

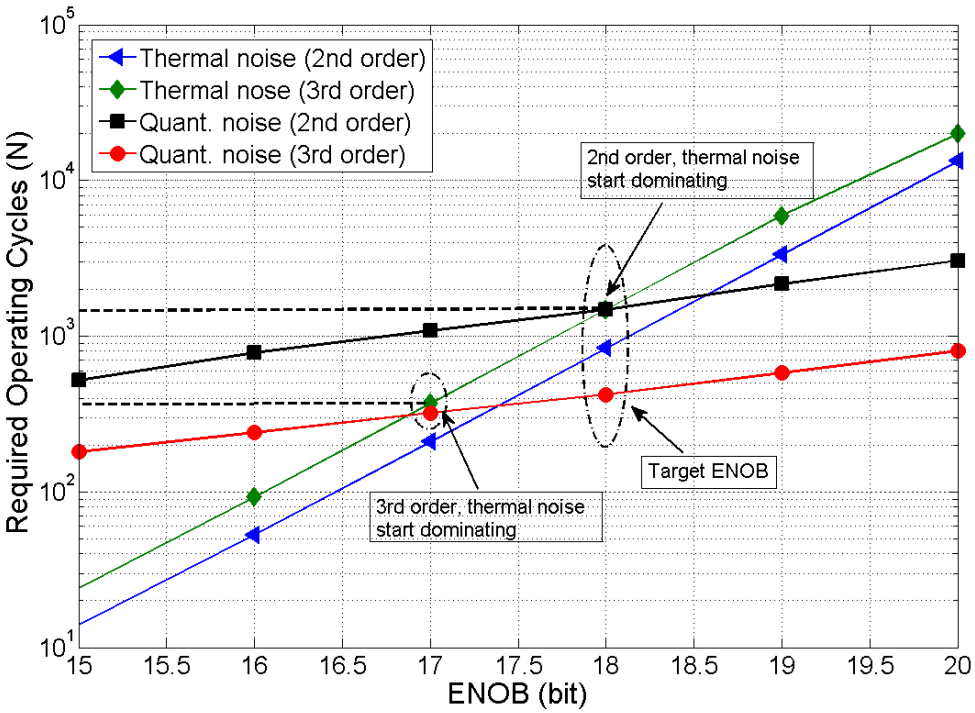


Fig. 4-18. The required number for operating cycles as a function of ENOB for both the quantization and thermal noise of the proposed CDC

Fig. 4-19 shows the block diagram of the proposed third-order incremental Delta-sigma-based CDC. A feed-forward loop-filter is used, since it decreases the output swing of the integrators, which improves the linearity of the modulator. Unlike the conventional implementation, a direct feed-forward path from the input to the comparator is omitted, since it would require a replica of the sensing capacitor [18] which adds extra thermal drift. The coefficients of the modulator

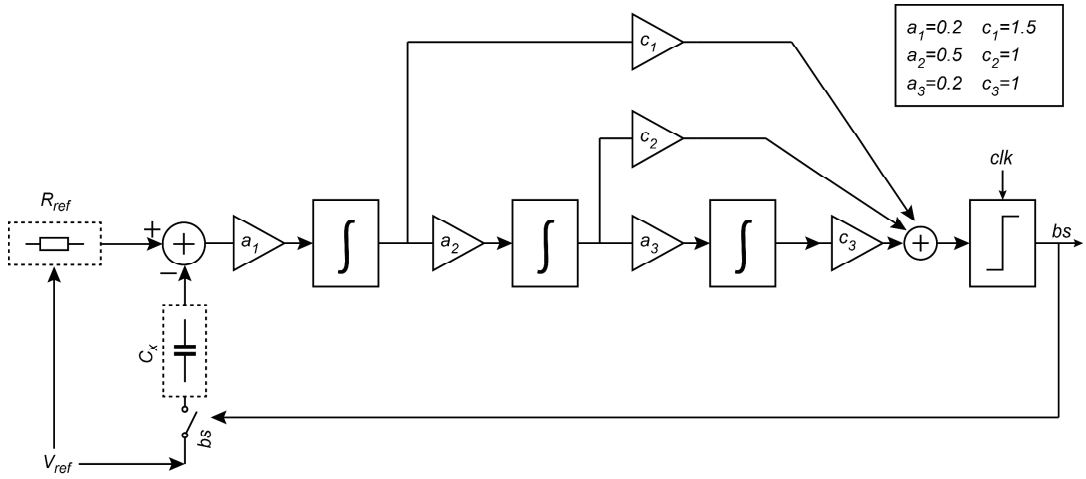


Fig. 4-19. Block diagram of the precision CDC based on a third-order Delta-sigma modulator

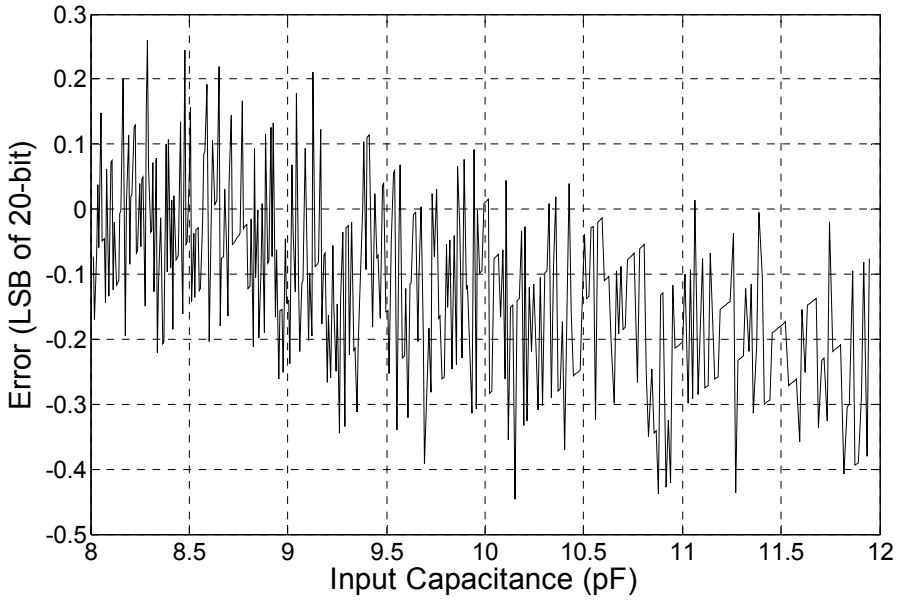


Fig. 4-20. Quantization error of a simulated third-order incremental converter with conversion cycles N=1000

were chosen so that the noise is optimized at DC with a usable input range of about $0.7C_{ref}$ [7, 8].

A behavior simulation of the third-order modulator shows that with an operating cycles N=1000, the quantization noise of the converter is within 20-bit resolution, as shown in Fig. 4-20. It can be concluded that a third-order modulator makes the design thermal-noise-limited, which is optimal for energy efficiency [4, 18].

The complete circuit diagram of the precision CDC is shown in Fig. 4-21. In this design, a pseudo-differential structure is implemented for better immunity to noise-coupling and charge-

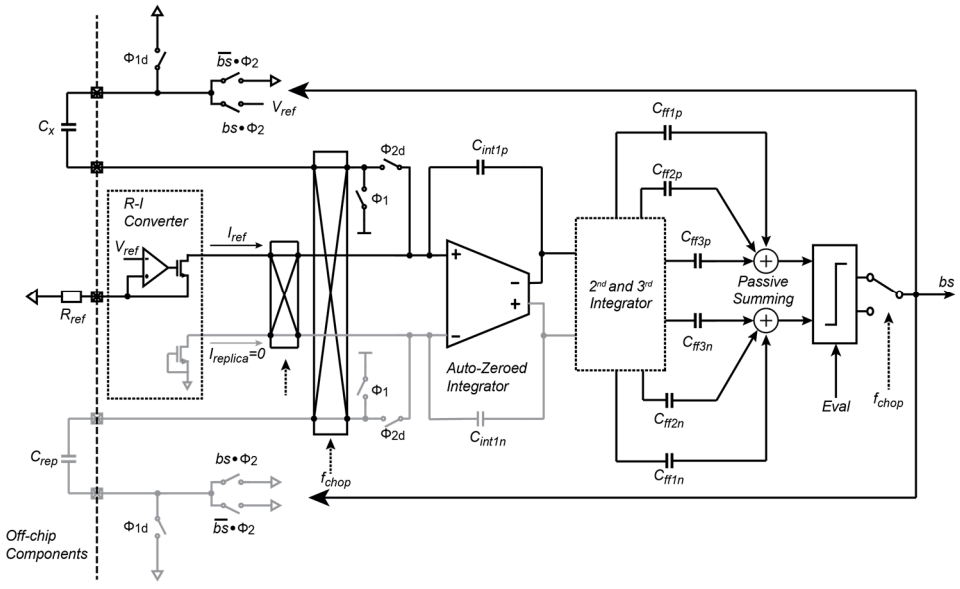


Fig. 4-21. Complete circuit diagram of the frontend and the Delta-sigma-based CDC

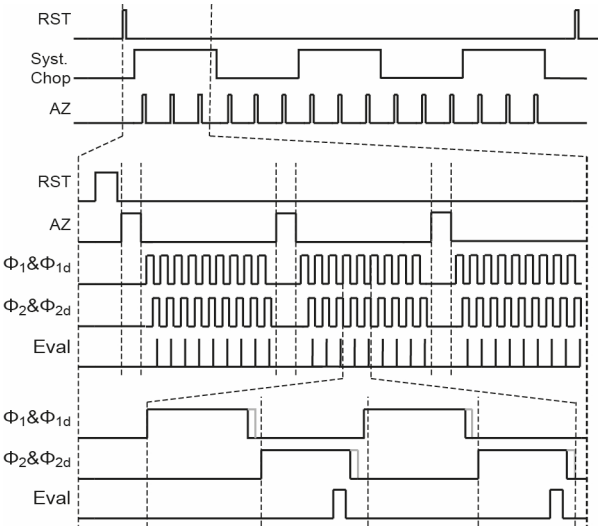


Fig. 4-22. Timing diagram of the precision CDC

injection error. To this end, the replica input as well as the feedback are implemented such that they do not contribute to the signal charge. But instead, they balance the circuit so that the coupled-noise and the switch charge-injection become common-mode error.

The second and third integrators are both implemented as conventional OTA-based switched-capacitor integrators. Since their noise and error will be shaped by the preceding integrator(s), their requirements are greatly relaxed. For simplicity, the detailed schematic is not shown. The summing of the feed-forward signals are done by passive summing of capacitor networks [1]. The comparator is implemented as a single-bit quantizer for good linearity and relaxed matching requirement [8]. As discussed earlier, system-level chopping is implemented by swapping the inputs and the output of the comparator accordingly so that the offset and mismatch-induced error of the system is further reduced.

Fig. 4-22 shows the timing diagram of the proposed CDC. Before each measurement, the integrators and the decimation filter are reset. After the initial reset, the RIC starts charging the integrator continuously, while the SC feedback balances the signal charge depends on the comparator output. Periodically, the modulator performs auto-zeroing to compensate for the offset and continuous current induced error (discussed in Section. 4.3.4). During the auto-zeroing (AZ) phase, the modulator states are 'frozen' by switching off the control clocks (Φ_1 and Φ_2). Apart from the AZ, as mentioned earlier, the system also performs system-level chopping (clock *syst.chop*). It is important to ensure that the system-level chopping clock is triggered by the AZ clock: because swapping the input signal also swaps the current-induced-overdrive (Section. 4.3.4), after each swapping the system performs AZ so as to store the correct information of the current-source-induced error.

4.5 Power consumption estimation and optimization

The previous section discussed the noise performance of the proposed CDC, followed by a system-level design and behavior simulation of the CDC. This section focuses on investigating and optimizing the energy consumption of the proposed CDC structure.

For a given capacitance measurement range, the energy consumption of a Delta-sigma-based CDC is mainly determined by the available measurement time and the required ENOB. The measured capacitance and the required ENOB lead to a minimum required operating cycles. The available measurement time and the required operating cycles define the settling time of the integrator and thus the supply current. Generally, in a Delta-sigma modulator, the non-idealities of the latter stages are shaped by the first integrator. Thus given the fact that the Delta-sigma modulator is carefully designed, it is reasonable to assume that the first integrator dominants the overall energy consumption.

As shown in Fig. 4-23, the SC path is controlled by a two-phase non-overlapping clock. During Φ_1, the sensor capacitor C_x is charged to a fixed voltage. Then in the second phase Φ_2, the charge is dumped to the integration capacitor, resulting in a voltage change at the output. This charge transfer is typically associated with a settling behaviour, which sets the speed requirement of the integrator and thus the supply current.

In most of the sensor applications, the reference voltage V_{ref} that charges the sensor capacitors is maximized in order to achieve good signal-to-noise performance at the input. In this case, the SC integrator works with large signal. Thus it experiences slew and linear settling phases. One exception is when a zoom-in capacitor is used [4, 19] so that only a small amount of charge is transferred to the integrator, hence there is no slewing in this case. But for this specific application where stability is of great interest, adding an extra zoom-in capacitor is not acceptable. Thus, the integrator will unavoidably slews due to the large amount of charge that is pumped into the integrator during the integration phase.

In this specific case, the total time for the signal settling contains two parts: slew time and linear settling time:

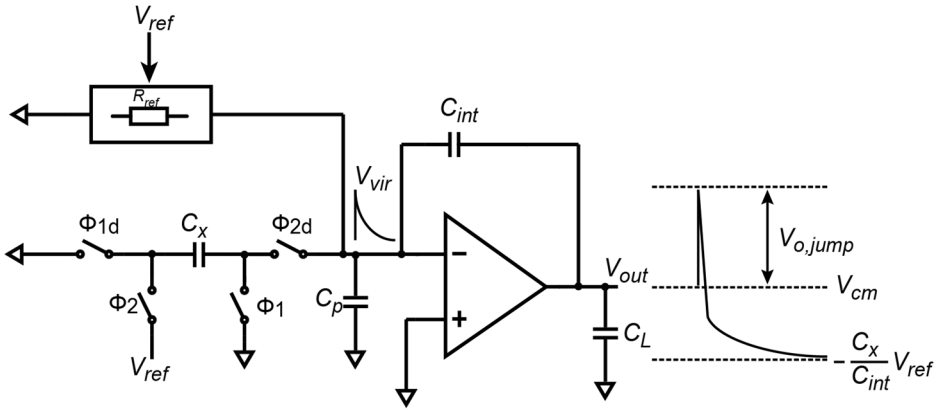


Fig. 4-23. The frontend integrator of the proposed CDC

$$t_{tot} = t_{SR} + t_{sett.} \tag{4–62}$$

The required slew-rate determines the minimum required output current of the integrator I_{out}, while the settling time translates to the required bias current for the input transistors I_{bias}, or in other words, the trans-conductance g_m.

Prior literatures estimate these two currents separately by assuming that these two processes are completely uncorrelated, and then allocate proper portion of the available time for each process. Finally, the dominant one will be taken as the supply current for the integrator implementation (assume a Class-A implementation of the OTA).

$$I_{\sup} = \max\{I_{out}, I_{bias}\} \tag{4–63}$$

However, this two processes are correlated and the above method is not optimal to estimate the minimum required current. More importantly, under different resolution and speed requirement, the allocation of t_{sr} and t_{sett} has to be adjusted accordingly for optimal design.

4.5.1. Slew

Due to the finite speed of the OTA, at the very beginning of Φ_2, there is no charge-transfer to the integrator. Therefore, according to the charge conservation law, a sharp voltage jump generates at the virtual ground as well as the output of the integrator [20, 21], as shown in Fig. 4-23. The voltage jump at the virtual ground can be calculated using the charge conservation law:

$$V_{in} \cdot C_x = V_{vir}(0) \cdot \left(C_p + C_x + \frac{C_{\text{int}} \cdot C_L}{C_{\text{int}} + C_L} \right) \tag{4–64}$$

Hence the voltage jump at the beginning of the integration phase can be expressed as:

$$V_{vir}(0) = V_{ref} \cdot \frac{(C_{\text{int}} + C_L) \cdot C_x}{C_x \cdot C_{\text{int}} + C_L \cdot C_{\text{int}} + C_x \cdot C_L} \tag{4–65}$$

Assuming that the output current of the OTA is I_{out} and the corresponding transconductance is g_m, if $g_m * V_{vir}(0) > I_{out}$ the OTA slews at the beginning of the settling phase, until the moment when $g_m * V_{vir}(t_{SR}) = I_{out.}$ After that, the linear settling starts and the output settles exponentially [20].

At the transition time, the voltage at virtual ground equals to:

$$V_{vir}(t_{SR}) = \frac{I_{out}}{g_m} \tag{4–66}$$

Thus the time needed for slewing to this transition point is the slew time T_{SR}:

$$t_{SR} = \frac{\left(V_{vir}(0) - \frac{I_{out}}{g_m}\right) \cdot C_{tot}}{I_{out} \cdot \beta} \tag{4–67}$$

Where, C_{tot} is the total load capacitor seeing at the output node:

$$C_{tot} = \frac{C_{\text{int}} \cdot (C_x + C_p)}{C_{\text{int}} + C_x + C_p} + C_L \tag{4–68}$$

Thus, for a given slew time, the required output current I_{out} can be calculated:

$$I_{out} = \frac{V_{vir}(0) \cdot C_{tot}}{t_{SR} \cdot \beta + \frac{C_{tot}}{g_m}} \tag{4–69}$$

4.5.2. Linear settling

As discussed earlier, the integrator slews until the condition of Eq. (4-66) is satisfied. Then the integrator starts linear settling. If we assume that the integrator is a first-order system, whose transfer function can be expressed as:

$$H(s) = \frac{A_{close}}{1 + s\tau} \tag{4–70}$$

Where A_{close} is the closed-loop gain of the integrator. The time constant of the system is represented by τ. In time-domain, the virtual ground voltage, which represents the settling error, settles exponentially, as described:

$$V_{vir}(t) = \frac{I_{out}}{g_m} e^{-\beta\omega_{unity}(t-t_0)} \tag{4–71}$$

Where t-t_0 is the time for linear settling, which represented as T_{sett} in Eq. (4-62), and ω_{unity} is the unity gain frequency of the OTA, which is defined as:

$$\omega_{unity} = \frac{g_m}{C_{tot}} \tag{4–72}$$

To further simplify the analysis, we assume that the output current I_{out} equals the bias current I_{bias} of the input transistor, which is mostly the case in normal OTA designs.

For energy efficient design, the ratio $\frac{g_m}{I_{out}}$ is usually set to around 25, meaning that the input transistors are biased in the weak inversion region [5]. Thus the equation becomes:

$$V_{vir}(t) = \frac{1}{25} e^{-\beta\frac{g_m}{C_{tot}}t_{sett}} \tag{4–73}$$

Thus, in order to achieve N-bit settling accuracy, this error has to be smaller than $2^{-(N+1)}$ (1/2 LSB). The required g_m can be found as:

$$g_m = -\frac{(N+1)\cdot\log(2)\cdot C_x}{\beta\cdot t_{sett}\cdot\log\left(1/25\right)} \tag{4–74}$$

Again, if we assume that the $\frac{g_m}{I_{out}}$ ratio is 25, the required bias current I_{bias} for the input transistors can be estimated as:

$$I_{bias} = \frac{g_m}{25} = -\frac{1}{25}\frac{(N+1)\cdot\log(2)\cdot C_x}{\beta\cdot t_{sett}\cdot\log\left(1/25\right)} \tag{4–75}$$

From Eq. (4-69) and Eq. (4-75), it is clear that the requirement for the minimum bias current I_{bias} and the output current I_{out} is correlated. The results highly depend on the proper budget of slew and linear settling time, the input reference voltage, the required number of bits and the available measurement time.

4.5.3. Optimization of the power consumption

As discussed in Section. 4.4, once the required ENOB and the measurement time is known, the required number of operating cycles and thus the available settling time t_{tot} for each cycle can be determined. Then, the corresponding requirements for slew and linear settling time directly determine the required supply current.

An example is shown in Fig. 4-24, where the required ENOB is 20-bit and the measurement time is 10ms. Based on these requirements and the noise analysis in Section. 4.4, the required operating cycles N can be estimated as 20000 (Fig. 4_18). Followed by that, the overall available time for the signal settling can be derived by taking the ratio of measurement time and the required operating cycle:

$$t_{tot} = t_{SR} + t_{sett.} = \frac{t_{conv.}}{N} \tag{4-76}$$

The required currents are then calculated using Eq. (4-69) and Eq. (4-75) at different budgets of the slew and linear settling time. The results are plotted as a function of different t_{SR}.

It is clear that, if the budget for slew is too tight while for the settling is too relaxed (small t_{SR}), the requirement for I_{out} dominants. On the contrary, if the budget for linear settling is too tight (large t_{SR}), the requirement for I_{bias} dominants. Therefore, for optimal design, the point where the requirement for I_{out} and I_{bias} equals is the optimal point for power consumption, as shown in the plot.

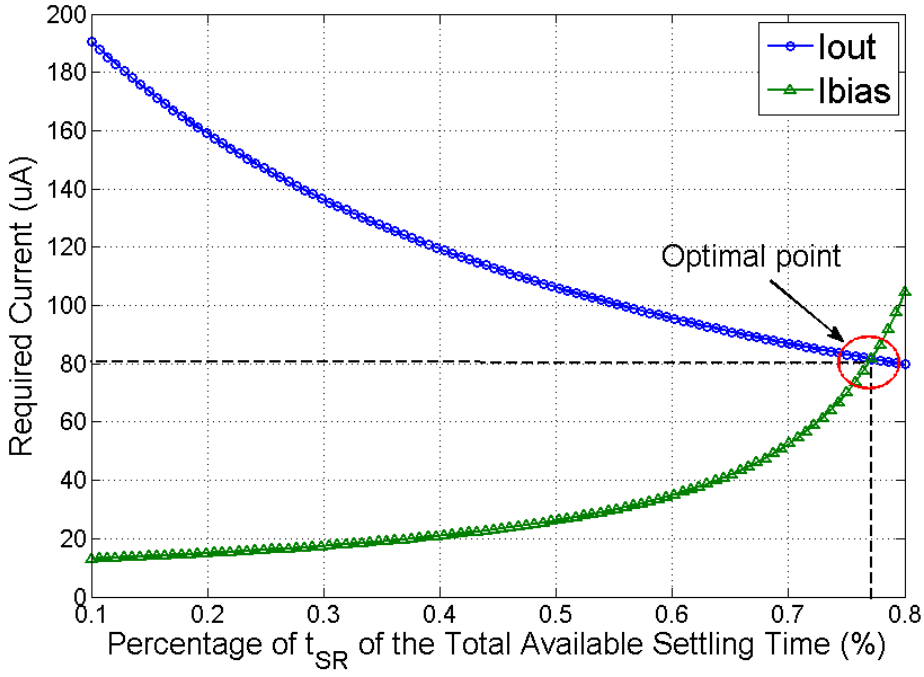


Fig. 4-24. The required supply current as a function of the slew time budget. (the simulation is done by assuming that the required ENOB is 20-bit and the total available conversion time is 10 ms)

PS: In the analysis, only 90% of the total available time is assigned for the settling. The remaining 10% is reserved for the comparator operation. (E.g. when t_{sr}=10%, t_{sett}=80%) The required number of cycles are simulated in a Matlab-based model as shown in Section. 4.4. The input range for 2nd-order modulator is defined as 0.2~0.8 (normalized to the feedback signal), while for 3rd order it is defined as 0.3~0.7.

To extend the analysis to a wider range, simulation is made for different combinations of conversion time and ENOB. In the simulation, the optimal point at each ENOB and measurement time combination is first calculated according to the method shown above. Then, the required total supply current is obtained based on the optimal points.

The energy consumption for each measurement is calculated and plotted as a function of the required ENOB, as shown in Fig. 4-25. When ENOB is below 17-bit, the required number of cycles is limited by the quantization noise of the modulator. But the thermal noise becomes dominant when ENOB requirement is above 17-bits. Thus the curves in Fig. 4-25 show different slopes in these two regions. If a slew-free case is considered, another curve can be calculated and plotted, which shows more than an order of magnitude improvement in energy consumption (Fig. 4-25). These curves are regarded as the references for optimal CDC design. The designs that are closer to the referencing curves are regarded as more optimal in terms of the energy-efficiency.

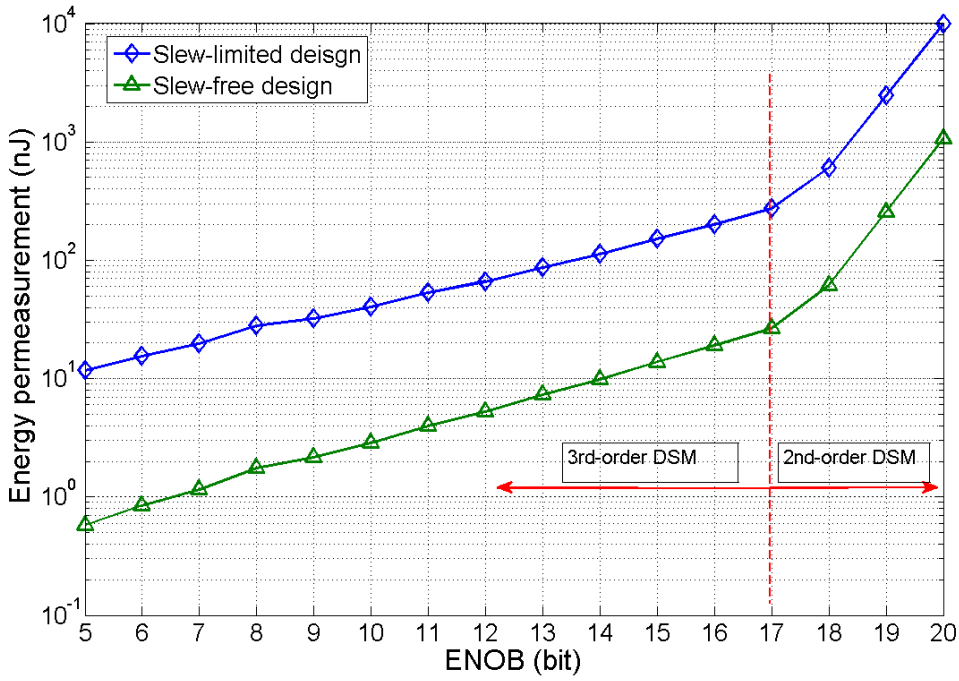


Fig. 4-25. Simulated energy consumption of an RC-comparison based CDC with and without slewing.

Note: in the analysis, the power consumption of the current source is not taken into account, because one could claim that the system could also work with a simple resistor connected directly to the input. Hence, the result is a fundamental limit of the proposed structure.

4.6. Conclusion

This chapter presents a system-level analysis of a precision CDC. The proposed CDC compares the unknown capacitance with a combination of time and resistive references to achieve accurate performance of the capacitance-to-digital conversion. It is based on a charge-balancing Delta-sigma modulator, in which the charge supplied by the sensor capacitor is balanced by a reference charge. The reference charge is generated by the high precision resistive and time references, which is expect to be precise and stable. The final conversion result is a function of the precision time and resistive references used.

Comparing an unknown capacitance to the combination of time and resistive references, however, is not as straightforward as comparing with a capacitive reference. Therefore, the nonidealities of the proposed CDC have been carefully identified and investigated. Based on that, appropriate error budgets can be allocated according to the practical requirements.

In addition to the non-idealities, this chapter performs an in-depth noise analysis of the proposed CDC. First, the dominant noise sources are identified. After that, each of the noise sources is analyzed carefully to understand their impact on the overall measurement result. The result of the analysis provides an optimal criteria for selecting the order of the Delta-sigma modulator,

defining the required operating cycles and allocating the noise budgets of each individual building blocks. Based on the analysis, a third-order loop filter with feed-forward compensation is chosen for this work. A behavior simulation is performed to validate the analysis and the proposed CDC structure.

Energy-efficiency is another important concern of the CDC design. In a properly designed Delta-sigma modulator, most of the power is consumed at the frontend stage. The power consumption of the frontend stage is usually determined by its speed requirement. The optimization is done by defining the budgets for slewing and linear settling of the frontend integrator such that none of them dominates the power requirement. Based on this criteria, the analysis is extended to a wide range of ENOB and conversion time. The result provides good reference for optimal CDC design.

The next chapter will focus on the precision circuit implementation of the proposed CDC. Based on the system-level analysis, proper error & noise budgets will be allocated for each of the building blocks. The corresponding circuit structures will be proposed, implemented and simulated.

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Chapter 5

Precision Circuit Implementation

In Chapter 4, a precision capacitance-to-digital converter based on comparing capacitance with a combination of resistive and time references is proposed. Besides, various non-idealities of the system that may affect the measurement performance are analyzed. To reduce the non-idealities, corresponding circuit techniques are discussed.

This chapter presents an implementation example of the proposed precision capacitance-to-digital converter in Chapter 4. The design considerations and circuit techniques introduced in the previous chapter are employed in the design to demonstrate their effectiveness. The implementation details of each of the building blocks are discussed. In addition, layout considerations improving the performance are briefly addressed.

5.1. Introduction

In Chapter 4, it was shown that a precision capacitance-to-digital converter (CDC) requires both high quality reference(s) and a high performance interface circuit. Based on the investigation of various possible references, the combination of resistive and time references is selected to build the equivalent capacitive reference for the measurement, because they provides high accuracy for reasonable size and price. Besides, this combination can be easily interfaced by many CDC interface circuits.

Regarding the interface circuit, a comprehensive survey and analysis of state-of-the-art CDC designs has been performed. The result shows that in the middle- to high-resolution range (15-bit to 20-bit), Delta-sigma-based interface circuits demonstrate superior performance with less power consumption, compared to other solutions. In addition, a charge-balancing Delta-sigma CDC provides an easy implementation of resistive and time references. Therefore, a charge-balancing Delta-sigma interface, which compares the unknown capacitance with a combination of resistive and time references, has been proposed.

The performance of the CDC is determined by both the reference(s) and the interface circuit. Therefore, the interface circuit has to be carefully designed, by minimizing every possible error sources that may degrade the precision of the overall measurement. In this chapter, the circuit implementation of all building blocks of the precision CDC is presented. Based on the error analysis of chapter 4, an appropriate error budget is allocated for each of the building blocks. To reach the desired level of performance, many precision circuit techniques are implemented. Specifically, the following blocks are discussed: the resistance-to-current converter (RIC), the active integrators, the comparator and the associated digital circuits. Next to the circuit implementation, the layout quality also affects the achievable precision of the system. Therefore, layout considerations of critical blocks are also shown.

5.2 Precision resistance-to-current converter (RIC) implementation

In measurements, the errors of the employed reference(s) cannot be suppressed by the comparison circuit. The references define the ultimate accuracy which can be achieved. The resistance-to-current converter (RIC) belongs to the reference part of the CDC. That is why its performance directly affects the measurement result. Therefore, the RIC has to be designed such that its error is within the required limits.

Fig. 5-1 shows a simplified circuit diagram of the precision RIC. It is implemented as an active RIC with large output impedance to suppress the effect of the integrator virtual ground wobbliness on the value of the reference current.

The negative feedback, formed by the amplifiers A_1, A_2 and transistor M_1, forces the voltage across the reference resistor to be equal to V_{ref}. Hence, the generated current can be calculated as:

$$I_{ref} = \frac{V_{ref}}{R_{ref}} \tag{5-1}$$

The accuracy of the current is mainly determined by the OTA, which consists of A_1 and A_2. Considering the finite gain of the amplifiers and its offset voltage, the generated current can be re-written as:

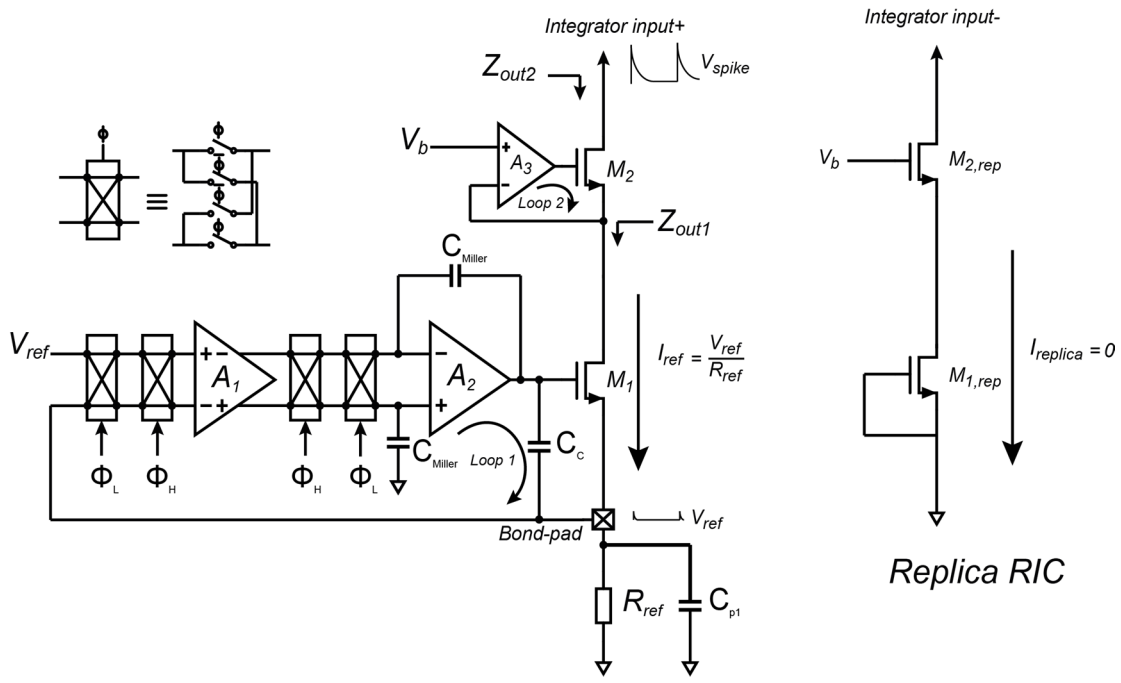

Fig. 5-1. Schematic of the precision RIC

$$I_{ref} = \frac{V_{ref}\left(\frac{A}{1+A}\right) + V_{os}}{R_{ref}} \tag{5-2}$$

where $A=A_1A_2$ and V_{os} represents the input referred offset voltage of the amplifier. To ensure a precise copy of the reference voltage V_{ref} over the reference resistor, a two-stage Miller-compensated amplifier (A_1 and A_2) with more than 120 dB total DC gain is implemented. The first stage A_1 is implemented as a fully-differential telescopic OTA. To achieve a sufficiently low offset and 1/f noise corner frequency, A1 is chopped by two nested-chopper pairs, operated at 50 kHz and 1 kHz [1, 2]. The choice of the 50 kHz chopping frequency is determined by the 1/f noise corner frequency of the OTA, which is around 30 kHz. To achieve good suppression of the 1/f noise, it is required that the chopping frequency is much higher compare to the original 1/f noise corner frequency [3, 4]. The low frequency chopper is introduced to suppress the charge-injection mismatch of the high frequency chopper switches. Hence, its frequency is selected to be 50 times lower than the high frequency chopper [2, 5, 6].

The decimation filter after the Delta-sigma modulator filters out the chopping ripples. The second stage A_2 is a single-ended implementation, which converts the differential signal into a single-ended output. The offset of the second stage is suppressed by the large gain of the first stage amplifier, thus it becomes insignificant.

In Section 4.3.3, we have proposed a pseudo-differential implementation of the CDC. To make the CDC circuit fully symmetrical so as to suppress the charge-injection mismatch, a replica RIC is implemented, as shown in Fig. 5-1. The replica RIC maintains the same output structure as the reference RIC, in order to generate the same parasitic for balancing the circuit. However, it does not generate current, meaning that the replica current $I_{replica} = 0$.

The RIC, as discussed in Chapter 4, is continuously connected to the integrator input, including the moments when the switched-capacitor (SC) feedback balances the charge stored in the integrator. Due to the finite speed of the integrator, the SC action causes voltage spikes V_{spike} (shown in Fig. 5-1) at the virtual ground of the integrator. These voltage spikes will alter the average value of the reference current beyond the acceptable error, if the output impedance of the RIC is not sufficiently high.

The voltage spikes due to the SC feedback represent a dynamic signal, whose frequency is determined by the system clock (200 kHz). As a consequence, it is required that the current source has enough output impedance up to 200 kHz and its harmonics, so as to minimize the effect of the transient behavior of the voltage at the input of the first integrator.

Referring to the simplified diagram in Fig. 5-2, and assuming that the external reference resistor R_{ref} is associated with a parasitic capacitance C_p, the reference impedance can be written as:

$$Z_{ref} = R_{ref} \,//\, \frac{1}{sC_p} = \frac{R_{ref}}{1+sC_pR_{ref}} \tag{5-3}$$

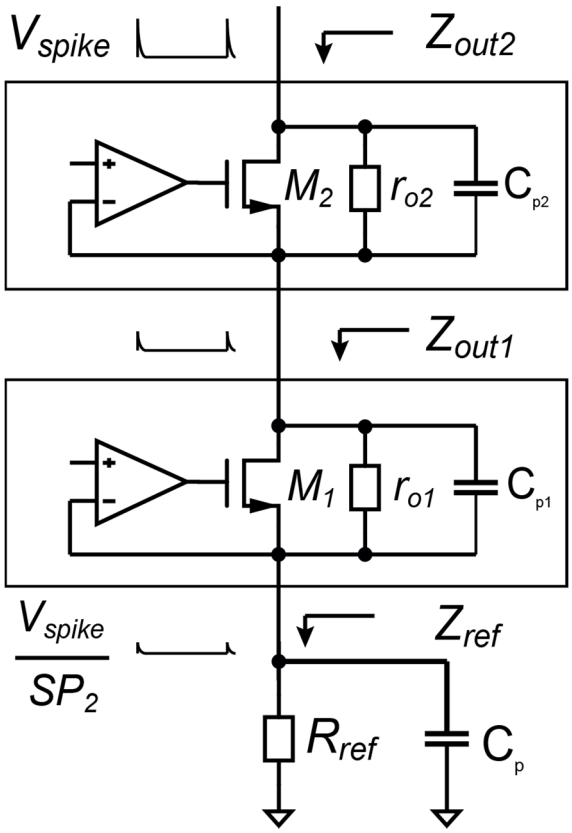

Fig. 5-2. Simplified circuit diagram of the precision RIC for estimating the output impedance

The frequency response of the Z_{ref} is shown in Fig. 5-3 (purple curve). In order to boost the impedance and to decouple the reference current from the virtual ground imperfections, a regulated cascade is implemented, which consists of A_1, A_2 and transistor M_1. Assuming that the output impedance of the transistor M_1 is a result of a resistance r_{o1} and a parallel parasitic capacitance C_{p1}, its value can be expressed by:

$$Z_{o1} = r_{o1} // C_{p1} = \frac{r_{o1}}{1 + sC_{p1}r_{o1}} \tag{5-4}$$

The impedance Z_{out1} looking at the drain of M1, and taking into account that it is in a negative closed loop, is [7]:

$$Z_{out1} = \left[\left(1 + A_1 A_2\right) g_{m1} Z_{o1} + 1 \right] Z_{ref} \tag{5-5}$$

The boosted output impedance has been plotted in Fig. 5-2 (green curve). Compared with the original impedance Z_{ref}, it is clear that the regulated loop (*loop 1*) provides a significant increase of the output impedance for a larger frequency range. With the boosted impedance, the imperfections of the virtual ground voltage is suppressed, which leads to a reduced error in the reference current I_{ref}. If we define the suppression ratio of the virtual ground imperfection as:

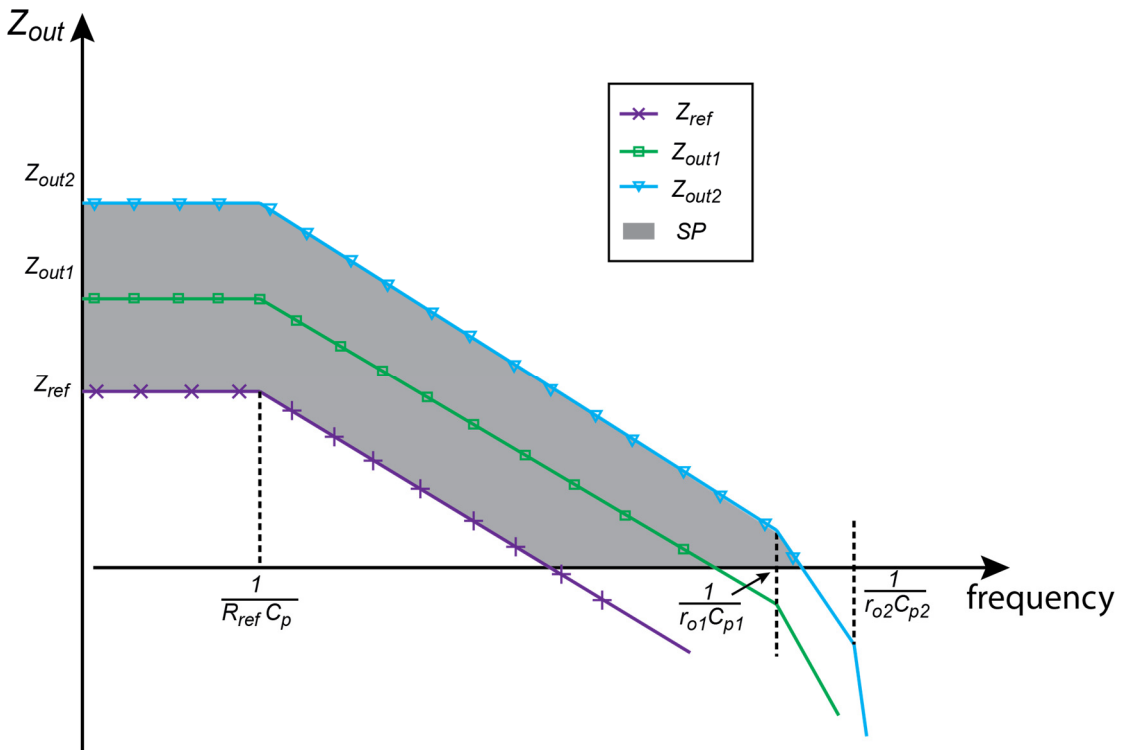

Fig. 5-3. Frequency response of the output impedances of the precision RIC and the suppression ratio (SP) of virtual ground non-idealities

$$SP = \frac{Z_{out}}{Z_{ref}} \tag{5-6}$$

With a regulated cascade M1, the suppression ratio can be derived as:

$$SP_1 = \left(1 + A_1 A_2\right) g_{m1} \frac{r_{o1}}{1 + sC_{p1} r_{o1}} + 1 \tag{5-7}$$

To further improve the output impedance, a second regulated cascade transistor M_2 is added. As a consequence, the output impedance seen from the virtual ground changes to:

$$Z_{out2} = \left[\left(1 + A_3\right) g_{m2} Z_{o2} + 1\right] Z_{out1} \tag{5-8}$$

The suppression ratio (grey area) of the virtual ground variation has been illustrated in Fig. 5-3. Similarly to Eq. (5-5), this ratio can be estimated as:

$$SP_2 = \frac{Z_{out2}}{Z_{ref}} = \frac{\left[\left(1 + A_3\right) g_{m2} Z_{o2} + 1\right] Z_{out1}}{Z_{ref}} \tag{5-9}$$

By substituting Eq. (5-5) and Eq. (5-8) into Eq. (5-9), the expression of the suppression ratio can be written as:

$$SP_2 \approx \left(1 + A_1 A_2\right)\left(1 + A_3\right) g_{m1} g_{m2} \frac{r_{o1}}{1 + sC_{p1} r_{o1}} \frac{r_{o2}}{1 + sC_{p2} r_{o2}} \tag{5-10}$$

The circuit-level simulation of the implemented RIC shows 35 GΩ output impedance at 200 kHz, which leads to more than 100 dB suppression of the virtual ground variation at this frequency. When the cascoded loop (*loop 2*) is not added, the output impedance drops down to 4 GΩ.

5.3 Frontend integrator implementation

As discussed in Chapter. 4, the first integrator is the frontend stage of the Delta-sigma modulator, and as such is the main contributor to measurement errors, as well as noise. The non-idealities of the following stages are attenuated by the gain of the frontend stage, thus become negligible. Therefore, the implementation of the frontend integrator is of most concern.

5.3.1. The main operational transconductance amplifier (OTA) of the integrator

The integrators are built around operational transconductance amplifiers (OTA). As discussed in Section 4.3.3, although the CDC is designed for a single-ended sensor, a pseudo-differential topology is implemented to increase its immunity to charge-injection errors of the SC network. For this purpose, a fully-differential OTA with input common-mode regulation is designed [8-10], as shown in Fig. 5-4. The OTA is implemented as a gain-boosted folded-casccde amplifier. The input pair is built by PMOS transistors to guarantee a low white noise and a low *1/f* noise corner. The input and output common modes are both designed to be $\frac{V_{dd}}{2}$.

The schematics of the boost amplifiers GB_p and GB_n are shown in Fig. 5-5 and Fig. 5-6, respectively. Two extra transistors (M_3 and M_4 in both figures), whose gates are connected to the desired common-mode input voltage are added to the input. As shown in Fig. 5-4, the inputs and outputs of the boost amplifiers, together with the cascade transistors of the main amplifier, form negative feedback loops. Therefore, the input common-mode voltages of the boost amplifiers are regulated to the desired voltage levels. The top boost amplifier GB_p regulates the drain voltage of M_{15} and M_{16} to $V_{cm,p}$ and the bottom boost amplifier GB_n fixes the drain voltage of M_9 and M_{10} to $V_{cm,n}$, ensuring a very high output impedance of the main amplifier [7, 8, 10]. The capacitors $C_{1,n}$, $C_{2,n}$, $C_{1,p}$, and $C_{2,p}$ are added to stabilize the gain-boosting loop [8]. These capacitances are relatively small (100 fF each), meaning that the boost amplifiers only have to drive small capacitive load. Hence, the current consumption of the boost amplifiers is only 12 µA.

As discussed in Section 4.3.2, the DC gain and settling behavior of this OTA are important for the overall performance of the CDC. Therefore, the OTA is designed for complete settling (settling error less than ½ LSB). The simulated bandwidth is above 7 MHz at 12 pF capacitive load across PVT (process, voltage and temperature variations). To ensure that the leakage of

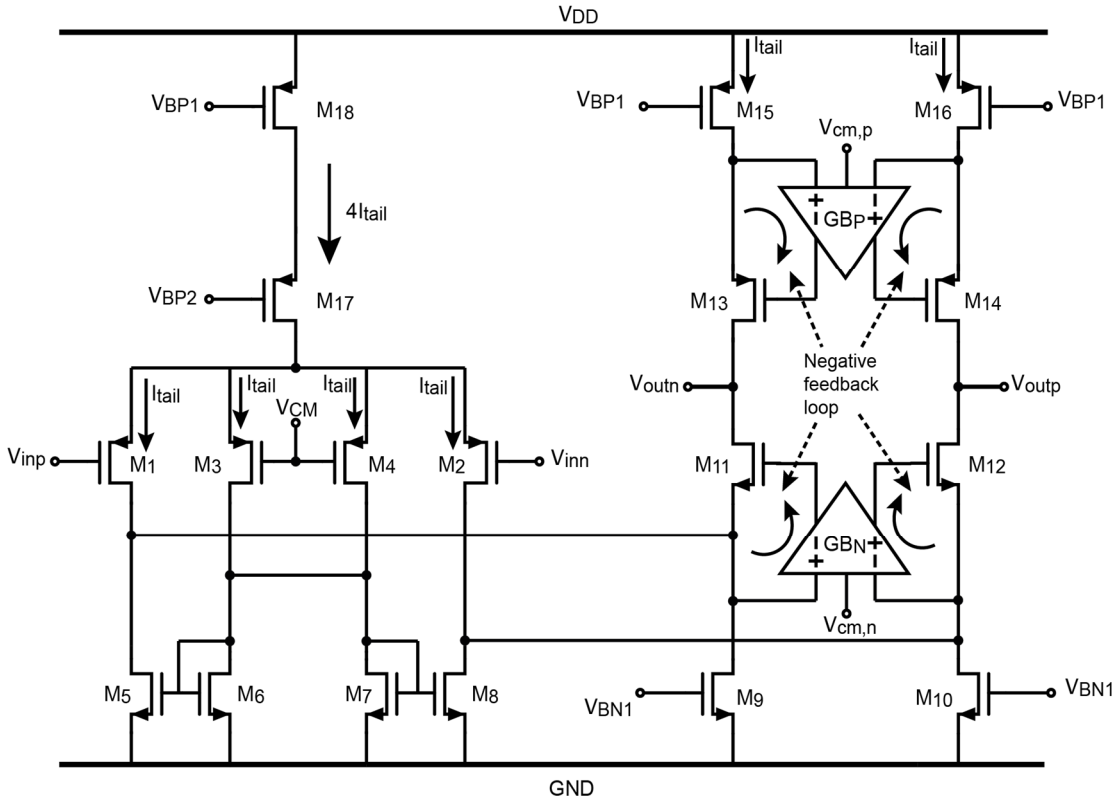

Fig. 5-4. Schematic of the first integrator OTA with input common-mode feedback and gain-boosting

the first integrator is negligible and provides enough suppression for the errors of the latter stages, the OTA is gain-boosted to get a DC gain above 140 dB under all operating conditions and process corners.

An input common-mode feedback (CMFB) of the main amplifier is realized by adding two extra transistors (M_3 and M_4) at the input, whose gates are connected to the desired common-mode level V_{cm}. During the reset phase when the OTA is connected as a unity gain buffer, the common-mode regulation effect can be represented by Fig, 5-7 (a). Due to the negative feedback loop formed by M_1 & M_2, and the output stage, the input and output common-mode voltages are regulated to V_{cm}.

To make better use of the current through transistors M3 and M4, their current is copied to the output by a current mirror (M6 and M7), as shown in Fig. 5-7 (b). By doing this, the bandwidth of the CMFB is doubled [9]. The imperfections of the OTA, such as offset and *1/f* noise,which affect the CDC precision, are taken care by the system-level auto-zeroing, as discussed in Section 4.3.3. In total, the OTA consumes 102 μA from 3.3 V single supply.

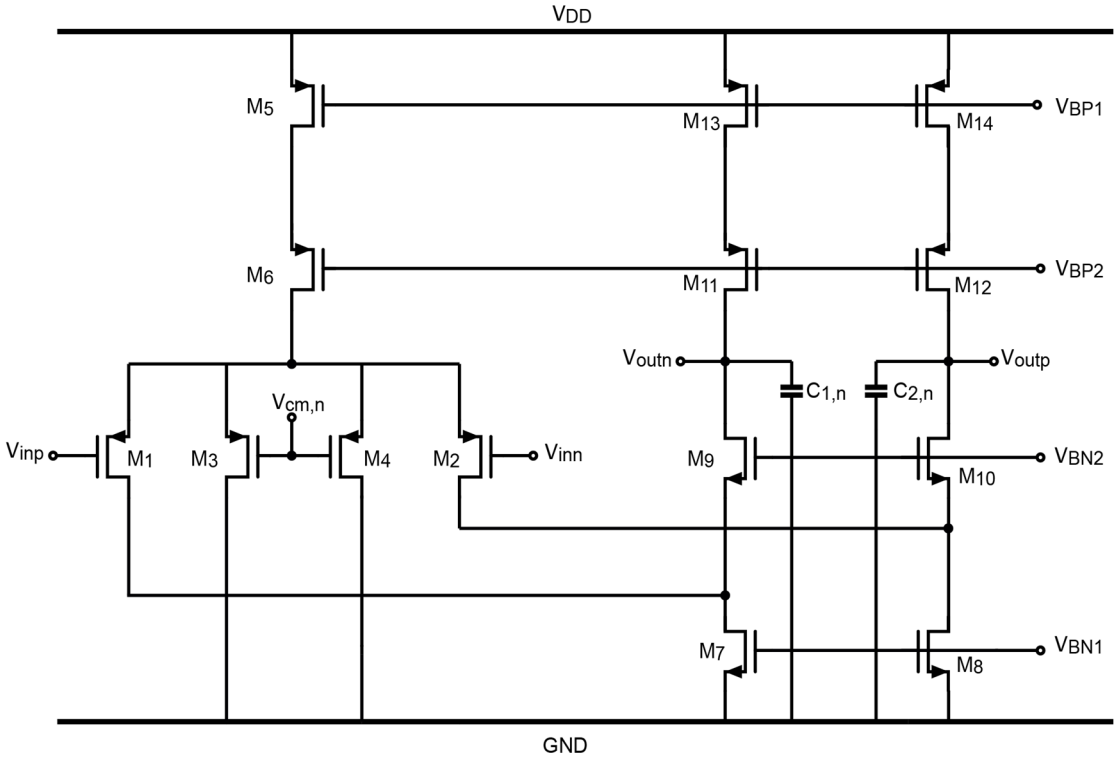

Fig. 5-5. Schematic of the gain boosting OTA GB_p

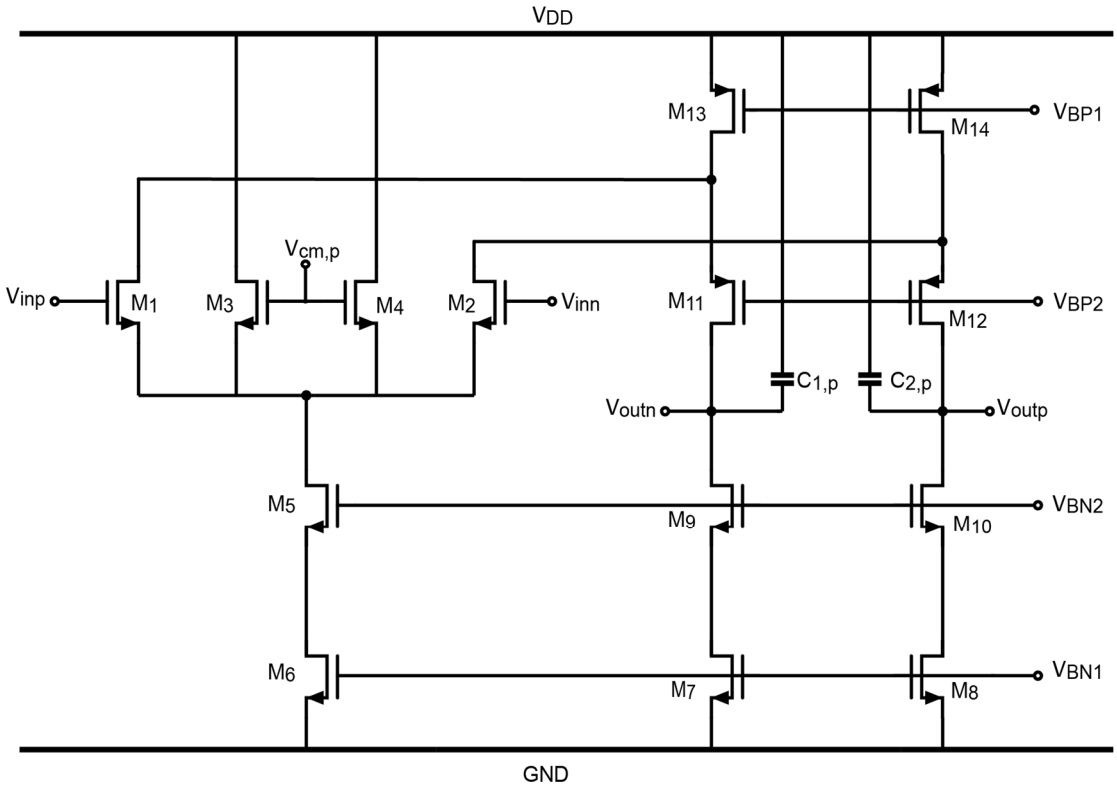

Fig. 5-6. Schematic of the gain boosting OTA GB_p

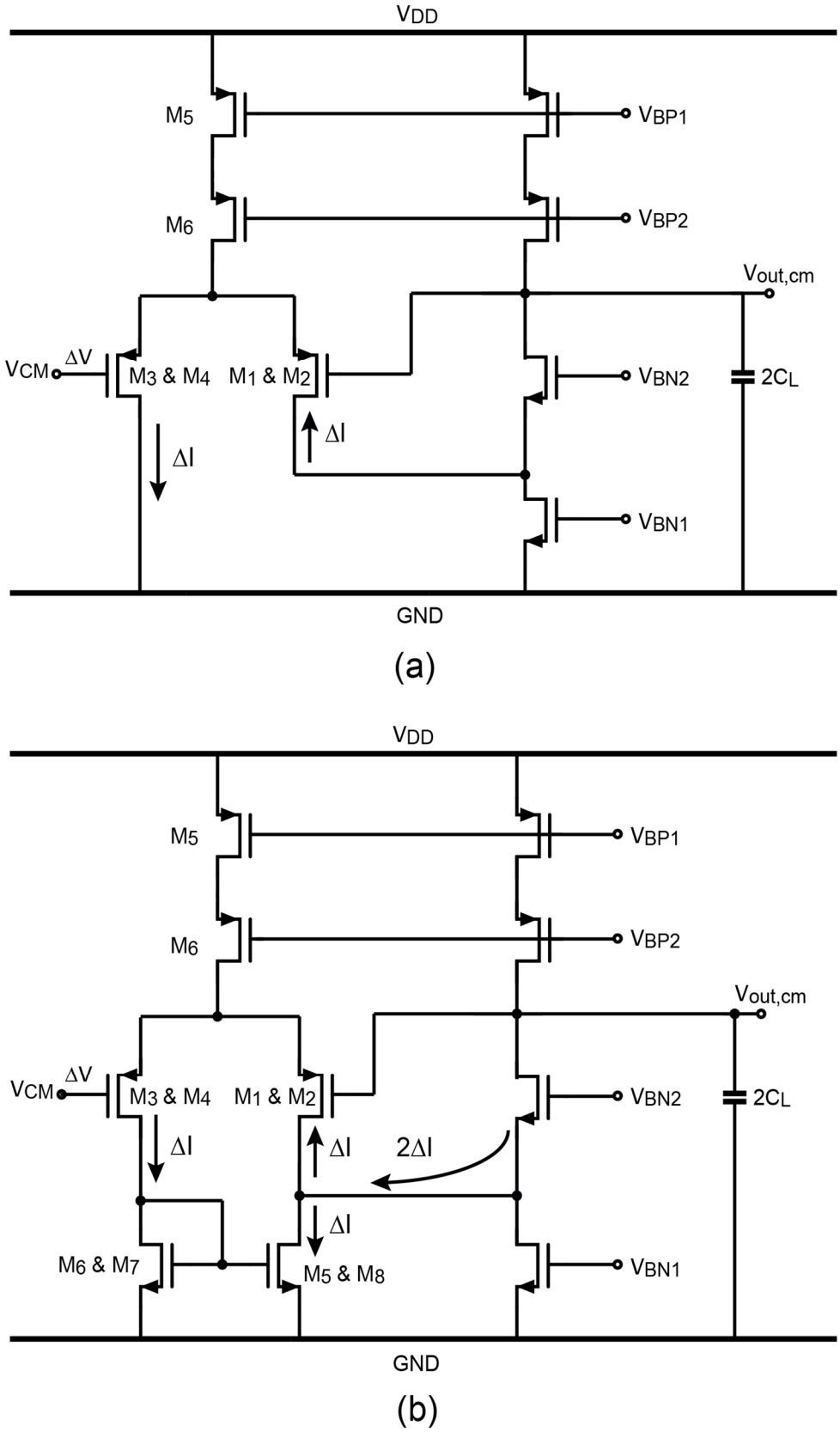

Fig. 5-7. (a) Input common-mode regulation during reset phase; (b) Bandwidth doubler of the input common-mode feedback

5.3.2. The slew-rate enhancement (SRE) circuit

As mentioned in Chapter 4, large reference voltage is used for the sampling capacitor to maximize the achievable SNR. In this case, the integrator works in large signal mode. As a consequence, the integrator slews at the beginning of the integration phase. The slewing increases the speed requirement of the amplifier, with which the integrator is built, for the required accuracy. To make the design energy-efficient, a slew-rate enhancement (SRE) circuit is added [11, 12], which provides extra output current during the slewing phase and returns to idle mode in the linear settling phase. The circuit diagram is shown in Fig. 5-8, while the schematic of the SRE is shown in Fig. 5-9.

The current sources are designed such that $I_2 > I_1$ (Fig. 5-9). In the normal operation when there is no slew, the top current sources enter deep triode region, which pulls voltage V_A and V_C close to the supply voltage. As a result, the output stages are turned off, which doesn't consume static power or generate error [12]. Whenever the OTA experiences slewing, the inputs of the SRE circuit see the same voltage spike as the main OTA. As shown in Fig. 5-9, if V_{inn} sees a positive voltage spike, V_A is pulled down, which turns on the output stage and thus supplies extra current to the output stage of the main OTA. In this way it boosts the slew rate of the main OTA. When the slew settles, the output stage of the SRE circuit is again turned off. The added currents I_2 and I_1 are insignificant compared to the main OTA (less than 5% of the main OTA), since this amplifier only has to drive a PMOS transistor so as to turn on the output stage. Besides, the SRE circuit only turns on at the beginning of the transient behavior. Therefore its error/noise does not contribute to the final measurement result.

Fig. 5-10 depicts the transient behavior of the virtual ground voltage and the output current of the integrator during the charge integration. Due to the finite speed of the integrator, the virtual ground sees a large spike at the beginning of the integration phase. Because of this large voltage spike, the integrator starts slewing. Without adding SRE, the integrator supplies a maximum current I_{max}, so that the voltage jump is slowly recovered until the voltage reaches a level that

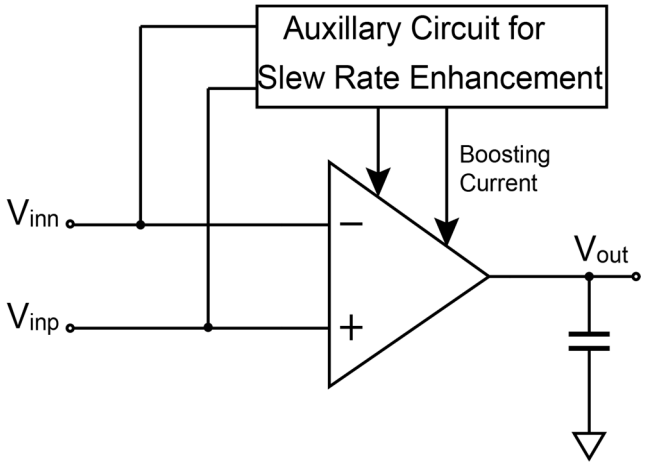

Fig. 5-8. Circuit diagram of the main OTA with slew rate enhancement (SRE) circuit

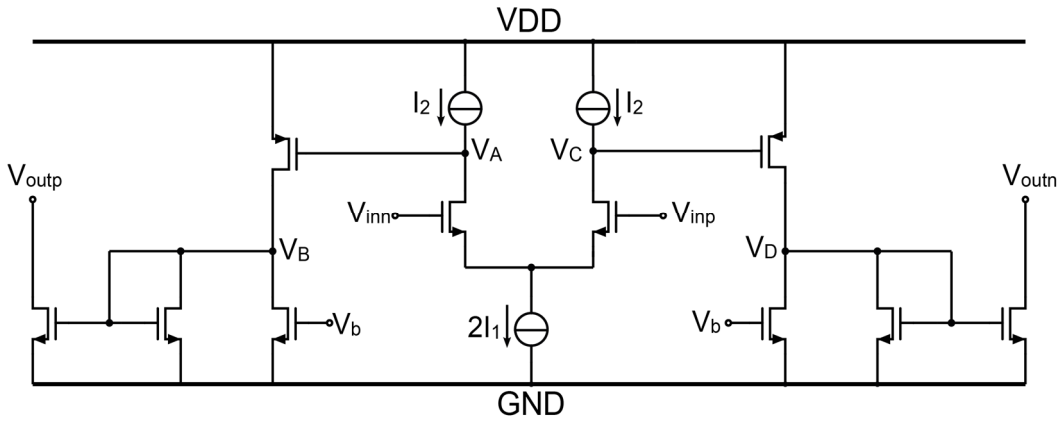

Fig. 5-9. Schematic of the auxiliary amplifier for slew-rate enhancement

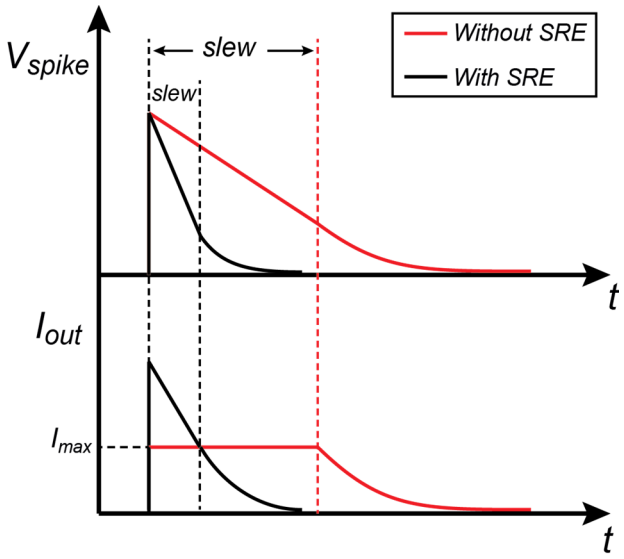

Fig. 5-10. Transient behavior of the integrator virtual ground during the integration phase

the integrator starts the linear settling. With SRE, however, the process is much faster. When a large spike is generated, the SRE circuit starts supplying extra output current to the integrator, which greatly increases the slew-rate of the integrator and reduces the slew time. After entering the linear settling phase, the integrator behaves in the same way as it should without the SRE circuit.

Design considerations:

1) Input offset of the OTAs

Due to the offset of the SRE circuit and the main OTA, the SRE circuit may turn on during the normal operation. Therefore, the design has to make sure that the SRE circuit is active only during large variation of the virtual ground voltage.

A most straightforward way is to tune the ratio between I_2 and I_1, because this ratio determines the minimum differential voltage at which the SRE circuit is activated. This voltage can be estimated as[12]:

$$V_a = (\frac{I_2}{I_1} - 1)\sqrt{\frac{I_1}{k}} \quad , \tag{5-11}$$

where k is the conductance parameter of the transistors (process dependent). Therefore, in the design, this voltage has to be much larger than the input referred offset of the main OTA and the SRE circuit. In general, the input offset of the amplifier without applying any offset cancellation technique can be in the range of ~ 10 mV [5]. Thus, in the design, Va is designed to be larger than 30 mV. Based on circuit-level simulations, this is achieved done by setting the ratio of I_2/I_1 to 1.4.

2) Mismatch of the current sources

The mismatch of the current sources would change the ratio between I_2 and I_1, which also affect the SRE circuit. Large ratio of I_2 and I_1 would cause the SRE circuit to be inactive even when slew happens. Contrariwise, small ratio may activate the SRE circuit when not needed.

Generally, it is conservative to assume 10 % mismatch of the current sources due to layout. In the design, it has to be made sure that even with 10 % mismatch of the current sources, the circuit still works fine.

Based on Eq. (5-11), the ratio is set to 1.4 to ensure that the SRE is insensitive to the input offsets of the OTAs. If we assume 10 % mismatch of the current sources, it results in worst-case I_2/I_1 ratio of 1.14 or 1.71.

To ensure that the SRE circuit works in all conditions, it is designed to be tunable. To this end, several sub-branches of the current sources are added, which are controlled by the shift register

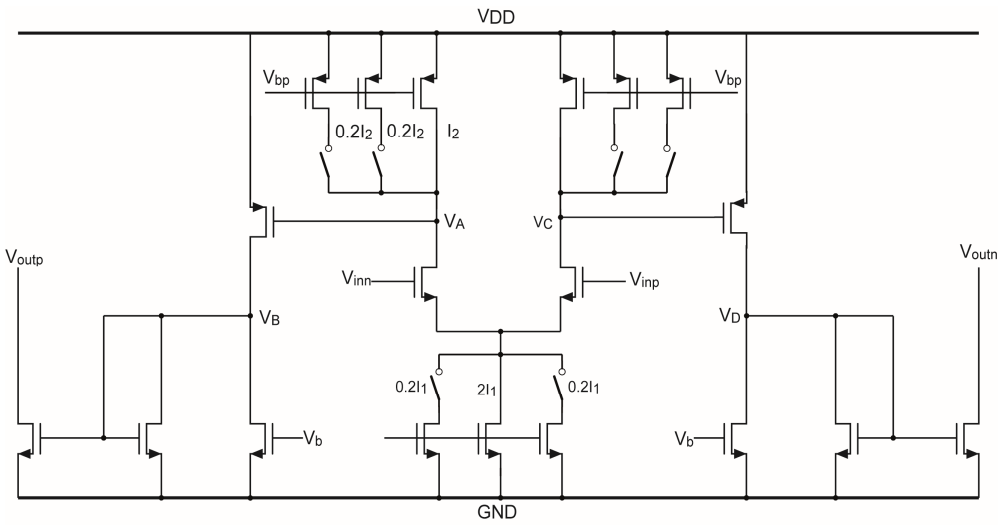

Fig. 5-11. Schematic of the SRE circuit with tuning possibility (the state-control switches are controlled by a shift register)

signal. During the real measurement, it is possible to tune the current ratio so that the SRE circuit works in right condition, as shown in Fig. 5-11.

5.3.3 Auto-zeroed frontend integrator

The final implementation of the frontend integrator is shown in Fig. 5-12. To reduce the charge-injection error, a pseudo-differential structure is implemented by providing a replica path, which does not contribute to the signal. A second current source is built (not shown in Fig. 5-12), which does not generate current but is a replica of the output stage of RIC (see section 5.3.1). The SC feedback is also replicated. But in the replica side, the capacitor always samples zero (ground) voltage instead of the reference voltage, hence it only contributes charge-injection instead of extra signal. An SRE circuit is added to improve the slew-rate of the integrator in a power-efficient way. As discussed in Chapter. 4, an auto-zeroing is employed to compensate for the continuous-current induced error. In addition, source followers are introduced between the outputs of the integrator and the load capacitors. This is to completely compensate for the load current induced overdrive error (Chapter. 4).

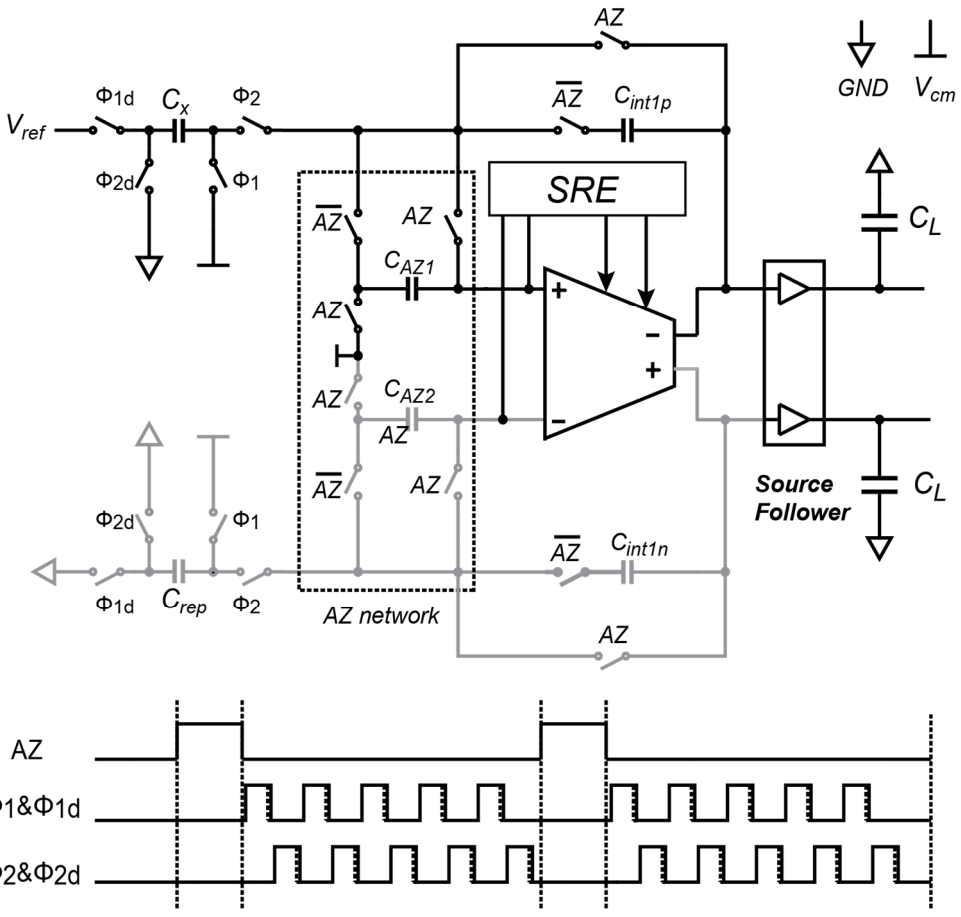

Fig. 5-12. Auto-zeroed frontend integrator with slew-rate enhancement and the corresponding timing diagram

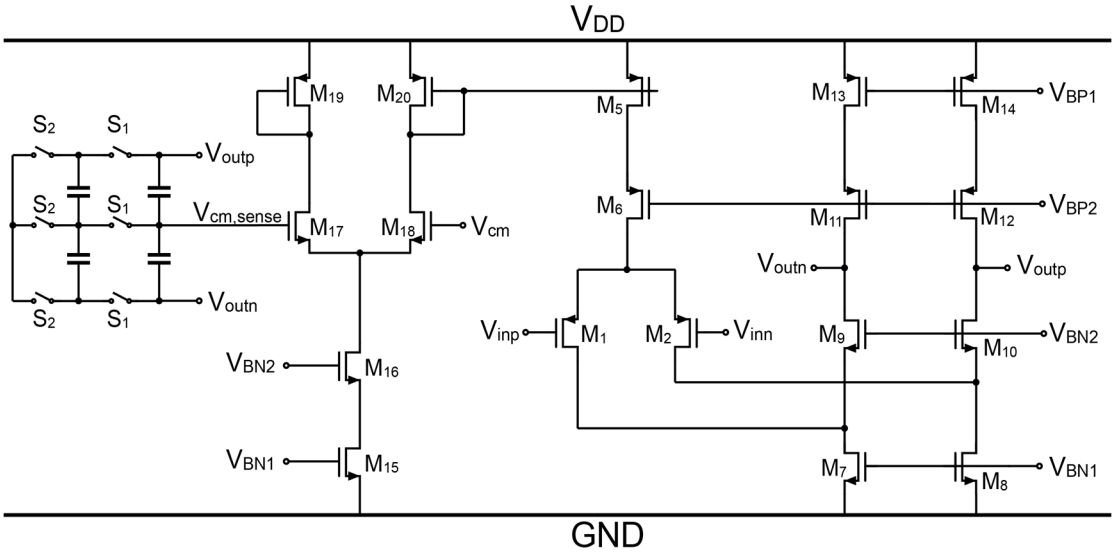

Fig. 5-13. Schematic of the second and the third integrator.

The timing diagram of the frontend integrator is also shown in Fig. 5-12. During the AZ phase, the CDC is 'frozen' (the states of the integrators are preserved) by switching off both Φ_1 and Φ_2 clocks. At the same time, the offset voltage, as well as the continuous-current-induced overdrive, are stored in the AZ capacitors C_{AZ1} and C_{AZ2}. After the AZ, the integrator resumes its normal operation. The AZ capacitors are connected between the inputs of the OTA and the sampling capacitors, hence the overdrive voltage and the offset are compensated for during the normal operation. To make the charge-injection error of the switches signal-independent, bottom-plate sampling is applied by slightly delay the switching of critical switches [2, 7].

5.4 The second the third integrators

As discussed earlier, the errors of the second and the third integrator are shaped by the first integrator, thus the requirements for these stages are relaxed. For this reason, the sampling capacitors of these stages can be greatly reduced, which leads to a reduced power dissipation. As a rule of thumb, the sampling capacitor is designed to be 4 times smaller than the sampling capacitor of the first stage [13, 14]. In principle, the third stage can be further shrink, because its error is shaped by the first and the second stages. However, for simplicity, in this work these two stages are implemented to be the same.

Figure. 5-13 depicts the schematic of the integrator. To generate the same common-mode voltage for both the input and the output, a fully differential folded-cascode OTA is implemented. To control the common-mode voltage, a common-mode feedback circuit is designed. As shown in the figure, a switched-capacitor (SC) network is built to sense the output common-mode voltage of the OTA [15, 16]. The sensed common-mode voltage $V_{cm,sense}$ is then compared with the desired common-mode voltage V_{cm} by an auxiliary OTA. The auxiliary OTA controls the tail current source of the main OTA. Hence, if there is any unbalance between

$V_{cm,\ sense}$ and V_{cm}, the auxiliary OTA adjusts the tail current of the main OTA such that the common-mode voltage of the main OTA equals the desired V_{cm}. For instance, if $V_{cm,sense}$ is larger than V_{cm}, the auxiliary OTA output increases, which lowers the tail current of the OTA. As a consequence, the output common-mode voltage of the main OTA is reduced until it is identical to V_{cm}.

The integrator is designed to drive a 2.5 pF capacitive load with a unity gain bandwidth of 5 MHz. The DC gain of the integrator is above 80 dB at all working conditions. The overall current consumption of the integrator is 20 μA from a 3.3 V single supply.

5.5 Comparator implementation

The error of the comparator, especially the in-band error, is greatly suppressed by the operation of the delta-sigma modulator, thus the performance of the comparator is also not critical [17] [18]. In this work, the comparator is designed with two stages: a simple pre-amplifier and a latch structure [2], as shown in Fig. 5-14.

The pre-amplifier has a gain of 10 X, which amplifiers the signal without degrade too much of the bandwidth [17]. The analog latch is a positive feedback, which latches to either supply or ground when it sees a difference in the input differential signal. The latch is controlled by an evaluation switch (Eval). When a comparison is not allowed, the switch resets the latch to an initial condition. Doing this keeps the latch in a pre-defined condition, which helps to improve the latching speed. When a comparison signal is received, the evaluation switch is off, which enables the latch to react on the differential signal that needs to be compared. The reaction time of the comparator is designed to be within 100 ns across PVT (process, voltage and temperature variation). The comparator draws 10 μA from 3.3V supply. After the analog latch, a Flip-Flop is added to lock the result before next comparison result is generated.

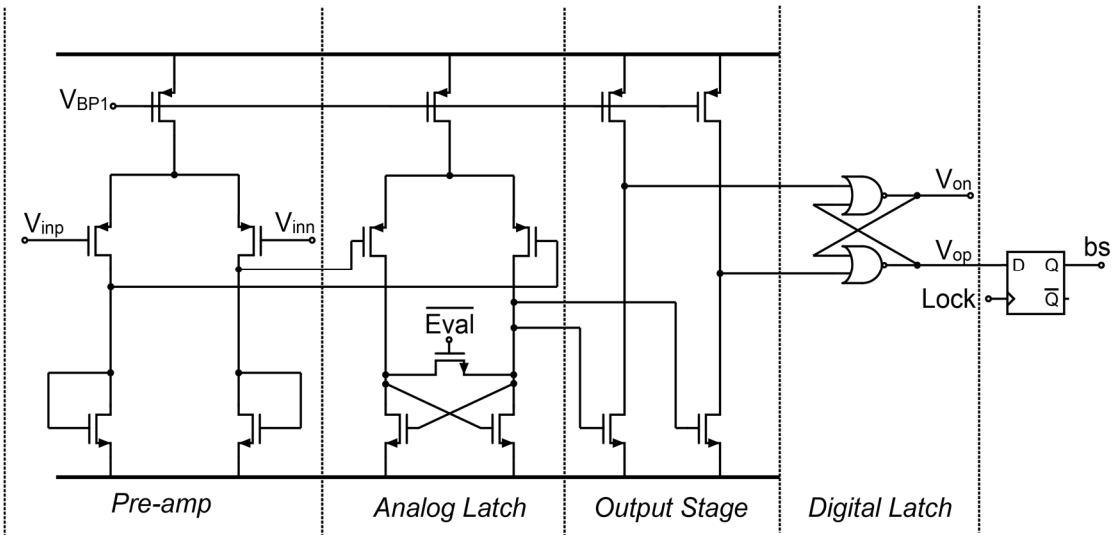

Fig. 5-14. Schematic of the comparator

5.6 Timing and decimation filter

To generate the four non-overlapping clocks (section 4.4.4) for the Delta-sigma operation, an onchip clock generator is implemented [19][Ref. Libin Yao]. The schematic of the onchip clock generator is shown in Fig. 5-15. Based on an external master clock (clk), two non-overlapping clocks are generated. To realize the bottom-plate sampling in order to eliminate the signal dependent charge-injection, two delayed clock ϕ_{1d} and ϕ_{2d} are also generated.

In this design, the possibility of using off-chip clocks are still preserved for safety. Hence, a digital multiplexer is added after each clock signal. By selecting the multiplexer inputs, it is possible to switch to off-chip clocks. In the final design, however, this is not needed. The clock signals are connected to corresponding switches via inverter chains which provide enough driving ability. For better noise performance, the last inverter (the one which directly drives the analog switches) is supplied by the analog voltage source, which is less noisy.

To reconstruct the signal and suppress the out-of-band noise of the Delta-sigma modulator, a digital decimation filter is required. For an incremental Delta-sigma modulator operating for N cycles, the decimation filter is a finite impulse response filter with a window size of N. The choice of decimation filter topology has a big impact on the achievable resolution.

The most straightforward way to realize a decimation filter for an incremental Delta-sigma modulator is to construct a digital filter with matched impulse response as the analog loop filter

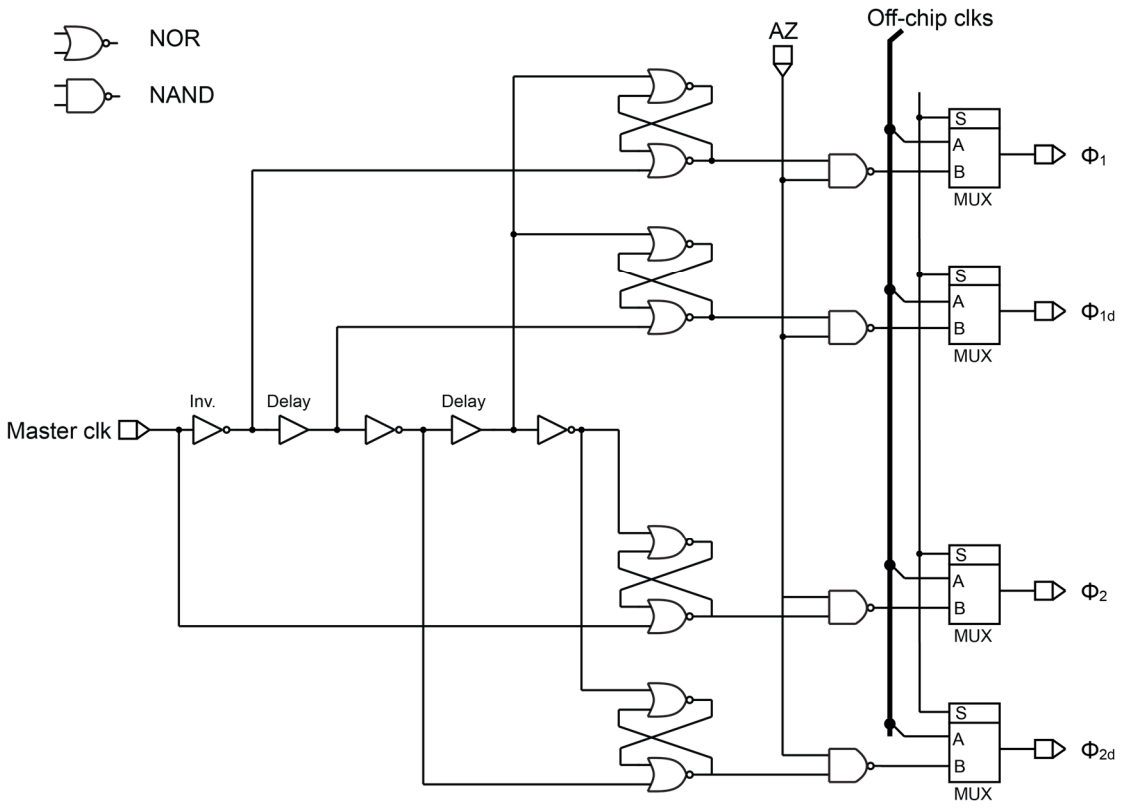

Fig. 5-15. Schematic of the onchip clock generator for generating the four non-overlapping clocks

[18]. This topology is also known as cascade of integrators (CoI). Since CoI filter matches with the analog loop filter, it provides high rejection of the out-of-band quantization noise. In addition, the implementation of CoI filter is relatively simple, as it only requires a few digital counters and accumulators. However, the CoI filter has a poor rejection for periodical noise, such as the dynamic noise caused by chopping operations and 50 Hz mains noise. Hence, for a thermal noise limited design with chopping, CoI filter is not an optimal solution as a decimation filter.

In this work, to achieve good suppression of the dynamic noise, a Sinc filter is implemented to decimate the output digital bitstream of the Delta-sigma modulator. The Sinc filter provides notches in its frequency response, which is ideal for suppressing the chopping ripples. By selecting the chopping frequency to be integer numbers of the system clock frequency, we can position the chopping ripple and its harmonics in the notches of the Sinc filter [2]. As a rule of thumb, the optimal order of the Sinc filter should be one order higher than the Delta-sigma loop [20]. Hence, in this work a $Sinc^4$ filter is implemented. For simplicity and flexibility, the filter is implemented off-chip in a FPGA. But it can be easily implemented onchip.

5.7 Layout considerations

In the previous sections, the implementation of precision building blocks is introduced. Besides the precision circuit techniques, the layout of the critical blocks also plays an important role in the ultimate achievable performance. In this section, the layout considerations and examples of these critical blocks are addressed. Besides, the overall layout floor plan is discussed.

5.7.1 Layout of the input pair

The input pair is the main contributor of a measurement error. For instance, the mismatch of the two transistors in an input pair causes an offset error [4, 5], which results in inaccuracy as well as thermal drift of the capacitance measurement (section. 4.3.2). Although many precision techniques (auto-zeroing and chopping) are implemented at system level to compensate for the offset, it is still required that the initial offset is small enough. Hence, the layout of the input pair has to be carefully conducted so as to minimize the mismatch and thus the initial offset.

A simplified diagram of the layout is shown in Fig. 5-16. The two input transistors (M1 and M2) of Fig. 5-16 are represented by *A* and *B*, while *C* stands for the transistors (M3 and M4) that form the input common-mode regulation circuit. To ensure good matching of the input pair, each of the input transistors is split into 8 unit pieces, and a common-central scheme is applied [21]. By doing this, it is guarantee that the two input transistors are well-matched no matter which direction the doping gradient is.

The transistors of the input common-mode feedback circuit (marked by *C*) are placed around the input pair. The mismatch between transistors *C* and the input pair (*A* and *B*) causes a common-mode voltage error, which does not affect the final measurement result. So their

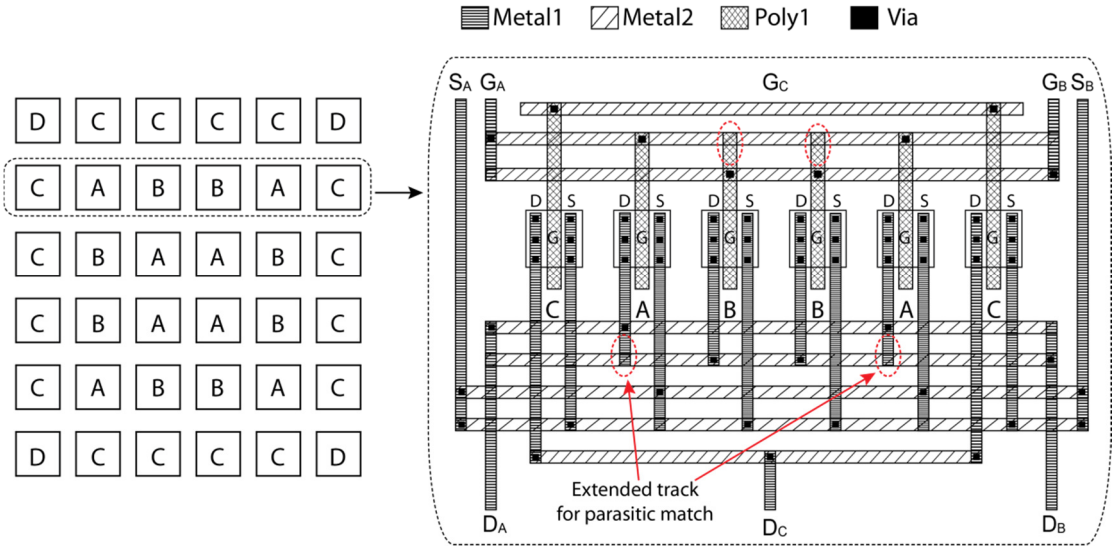

Fig. 5-16. Layout example of the critical input pairs to achieve good matching

matching with the input pair is less critical. Placing them around the input pair also ensures that all the transistors *A* and *B* see the same surrounding environment, which further improves the matching quality. Dummy transistors *D* are also added to provide the same surroundings for the common-mode feedback transistors *C*.

Figure. 5-16 also shows a layout example of one of the rows. The transistors are close to each other with the minimum allowed distance that is defined by the technology. To ensure that the parasitic due to connection wires are the same for transistors that need to be matched, a careful layout is made. The vertical connections are all made by metal 1, while the horizontal ones are made by metal 2. Besides, it is guaranteed that the connection metals for both transistors are identical in length and width. As is shown in the figure (red circles), some of the connection metals are extended more than it is actually needed. This is to match the parasitic capacitances of different transistors. For example, the drain (*D*) connections (metal 1) of transistors *A* are extended to overlap with the metal 2 drain connection of transistors B. In this way, the coupled parasitic of A and B are the same, which also improves the matching of the two transistors.

5.7.2 Layout of critical choppers

In the CDC, there are many choppers involved to achieve good precision. In section 5.2, it was shown that a nested-chopper is implemented in the RIC to reduce the offset error of the RIC. Besides, to suppress the charge-injection error of the SC feedback of the pseudo-differential CDC, a system-level chopper is implemented (section 4.3.3). The charge-injection and clock feed-through of the chopper switches may still cause residual offset error [5, 10] if the chopper layout is not carefully performed. For instance, if the chopper switches are not well-matched, the charge-injection error of the switches are no longer common-mode error. Hence, it will affect the precision of the final measurement. Besides, the imbalance of parasitic capacitors at the differential inputs of the first integrator causes offset error even if the switches are perfectly

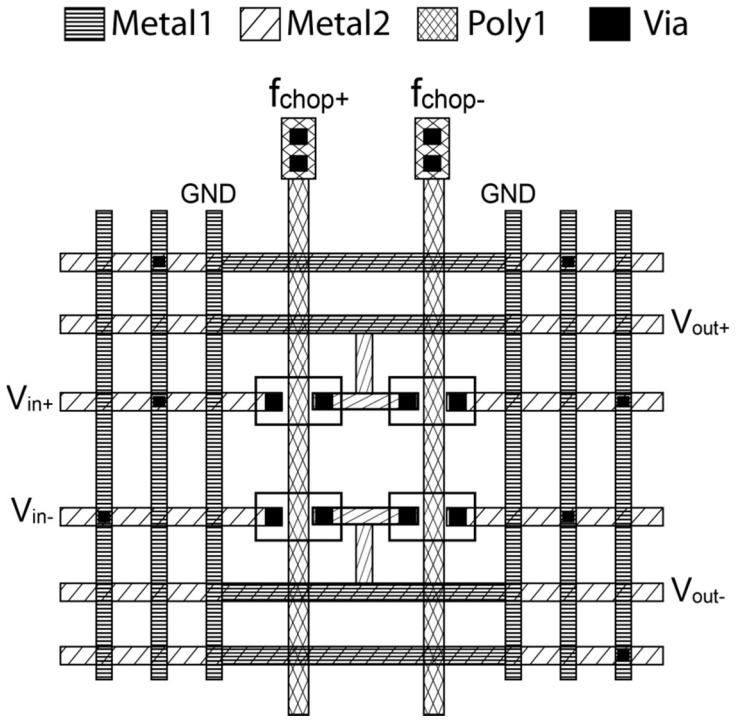

Fig. 5-17. Layout example of the chopper switches

matched. Therefore, a careful layout of the chopper is required to minimize both the mismatch of the switches and the parasitic capacitances.

Figure. 5-17 illustrates the chopper layout. To mitigate the afore-mentioned mismatch sources, the following methods are taken during the layout: first, the transistors are placed as close as possible to each other to minimize the mismatches [5]; second, a common central layout is made, which balances the parasitic of all the signal lines; third, the clock lines are carefully shielded by an on-chip coaxial cable [5, 10] to minimize the clock feed-through.

5.7.3 Floor plan of the overall chip

The floor plan of the chip is designed as follow (Fig. 5-18): the reference current source and the first integrator are made as symmetrical as possible. The integrator capacitors are arranged in a symmetrical way during the layout to achieve good matching. Since the 2nd and 3rd stage are less critical to the overall performance, the requirement for symmetry is relaxed. The biasing block is in the center of the chip. To avoid interference between digital and analog circuitry, the digital blocks and switches are far away from the most sensitive analog circuit (1st stage).

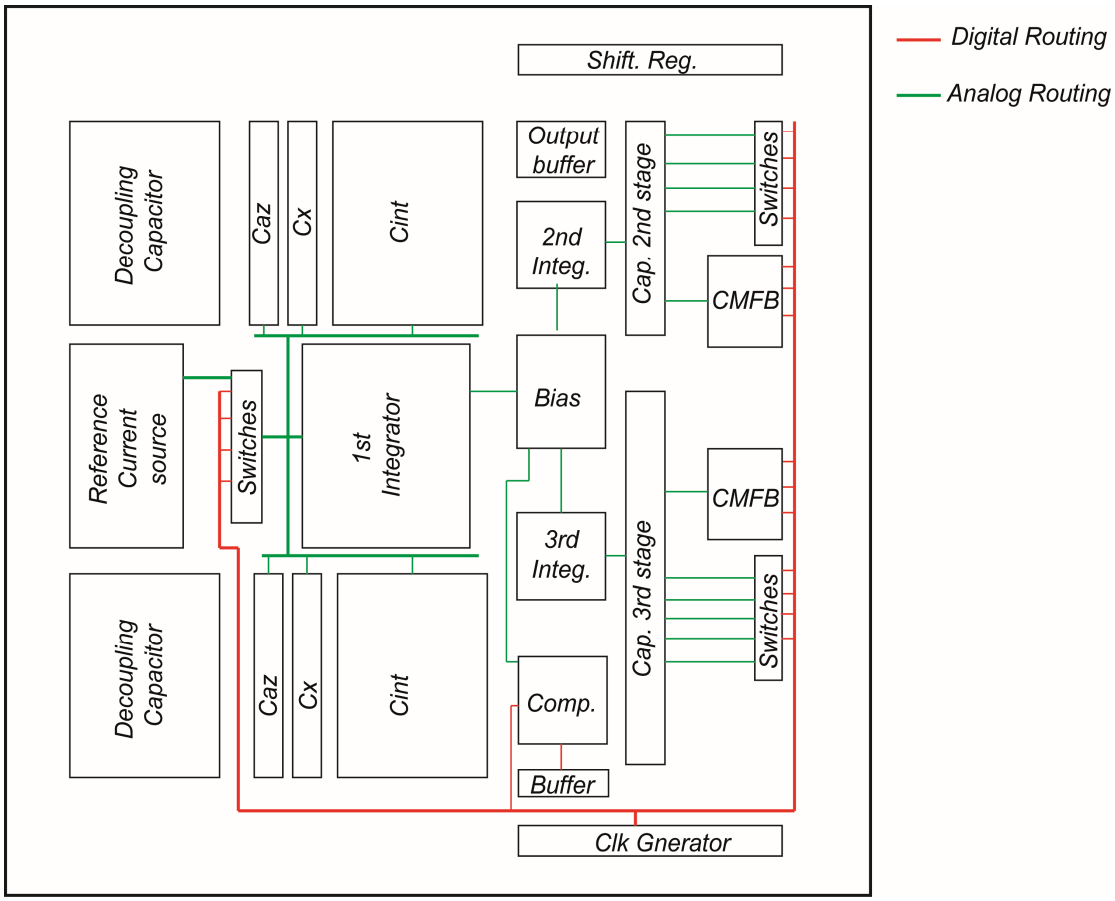

Fig. 5-18. Layout floor plan of the precision CDC

5.8 Conclusion

This chapter presents the circuit implementation of the proposed precision CDC, which compares the unknown capacitance with a combination of a resistive and time reference. With a high precision resistive reference and a crystal-stabilized time reference, an equivalent precision reference capacitance is generated. But the interface circuit, which does the comparison of the sensor capacitance and the references, also contributes to the measurement error. Hence, the building blocks of the interface circuit have to be carefully designed so that their error contribution is made negligible. In the proposed Delta-sigma based CDC, the main building blocks include: integrator, comparator, resistance-to-current converter (RIC), and some digital circuits (clock generator, decimation filter).

Based on the system-level analysis of chapter. 4, the error budgets as well as the specifications (gain, bandwidth, etc) of each individual building block are defined. Then, proper circuit topology is selected and implemented. To ensure that the error contribution of the individual blocks is within the error budgets, various precision circuit techniques, such as chopping and auto-zeroing, are implemented. Finally, the layouts of the critical components that are important for the CDC performance have been shown.

In the next chapter, the measurement strategy and the results of the qualification tests of the implemented CDC chip will be presented. Following that, a discussion of the measurement results compared to the theoretical analysis, will be provided.

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Chapter 6

Experimental Results and Discussions

This chapter describes the test strategy, the experimental test setup and the performance of the fabricated precision CDC, based on the design proposed in Chapter 5. The tested performance includes: noise, thermal and long-term stability, absolute accuracy, linearity and transfer characteristic. The experimental results confirm the effectiveness of the applied design approach, as well as the validity of the analysis. Finally, the performance of the new CDC is compared with the reported state-of-the-art CDCs.

6.1. Introduction

The integrated CDC was implemented and fabricated using the Austria-Microsystems (AMS) 0.35 µm 4P3M CMOS process. Fig. 6-1 shows a microphotograph of the fabricated CDC chip. It occupies an area of 6 mm^2, including the pad ring. In total, the chip consumes 230 µA current from a 3.3 V single supply. To validate the concept and the analysis, the performance of the fabricated chip is experimentally qualified.

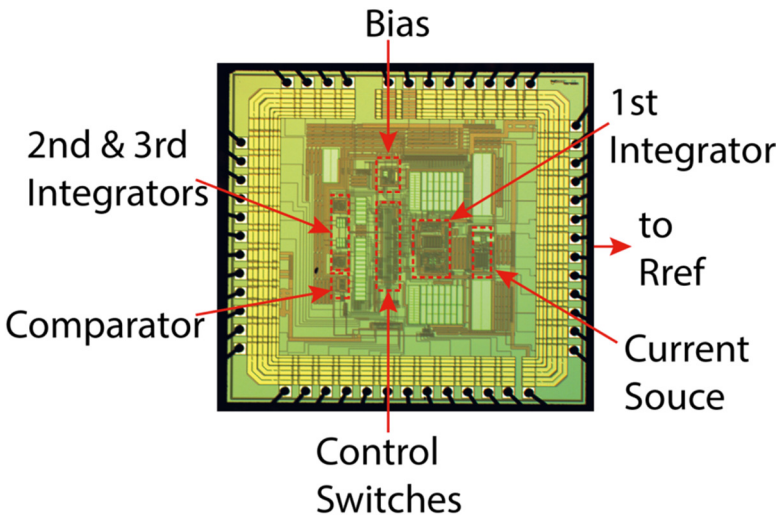

Fig. 6-1. Chip microphotograph of the precision CDC

The designed CDC is projected to demonstrate many advanced features, including high resolution, high stability (especially thermal stability) and accuracy. Next to the design challenges, the expected high performance poses serious challenges to the qualification tests, as well. Potential measurement imperfections may dominate the final results and in this way can compromise the performance of the CDC. To prevent this, all possible errors during the measurements have to be carefully considered. In this chapter, first, the measured parameters are defined and appropriate measurement strategies are proposed, which take into account all major error sources and proper solutions to minimize their impact on the measurement results

(Section. 6.2). Next, based on the defined strategies, a measurement setup is created. Depending on the requirements of the specific measurement (e.g. noise, stability, etc.), the measurement setup is adjusted accordingly. The performance of the CDC is qualified and the results are analyzed. Finally, the measured performance is compared with the state-of-the-art designs, to be able to evaluate the effectiveness of the proposed concept and the design approaches (Section. 6.3).

6.2 Measurement strategy and design for testability

6.2.1 Performance parameters and measurement strategy

A). Resolution and dynamic range

The resolution is defined as the minimum detectable signal fluctuations. The derivation of the CDC resolution is based on the measurement of the input-referred RMS capacitance noise. It was determined by performing multiple conversions at a single input capacitance and calculating the sample-to-sample standard deviation of the decimated outputs relative to the nominal capacitance (section. 6.3.1).

The dynamic range (DR) is defined as the ratio between the largest and smallest measurable values of a changeable quantity. As such, the DR of the CDC is defined as follows [1]:

$$\mathrm{DR\ (bits)} = \left(20\log_{10}\frac{\Delta C_{\max}}{\sigma_{rms}} - 1.76 \right) / 6.02 \qquad (6\text{-}1)$$

Where $\Delta C_{\max}$ is the capacitance input range, σ_{rms} is the standard deviation of the measured capacitances.

B). Thermal stability

The most straight forward way to qualify the thermal stability of a CDC is to fix the temperature of the measured capacitor while changing the temperature of the CDC under test. Then, the nonconformity of the measured capacitance at different temperatures is a measure of the thermal drift of the CDC. Such approach would require that the measured capacitor to be far away from the CDC so that its temperature can be fixed irrespective to the temperature of the CDC [2, 3].

However, in this work, the precision CDC is intended to be integrated in the sensor head, meaning that the CDC is not designed to handle large cable capacitance (~ 100 pF/meter) to connect to a remote capacitor. Hence, if long cables are used, the noise performance will degrade as the cable capacitance increases the noise gain of the first integrator. Moreover, it might cause instability, as the OTA is not designed to handle large input capacitance.

As explained in section 4.3.3, the CDC is designed as a pseudo-differential structure to reduce the charge-injection errors of the switches. For this reason, it is required that the parasitic

capacitances at the differential inputs are well-balanced so as to reduce the charge-injection mismatch [4]. Having a long cable to connect to a sensor capacitor would cause significant unbalance of the CDC inputs, leading to performance degradation. In principle, it is possible to balance it by providing the same cable capacitance to the replica input. However, matching two large cable capacitances (a few hundreds pF) is still very difficult and furthermore does not solve the increased noise gain issue.

Taking the above situations under consideration, two methods to reliably measure the thermal stability of a CDC is proposed:

Method I: Capacitor without known temperature characteristic

Since the temperature characteristic of the capacitor is not known, the capacitance is measured by both the CDC and the external precision equipment at different temperatures. In this way, the thermal behaviour of the capacitor is measured by the external precision equipment, while the combined effect of the thermal drift of the CDC and the capacitor is reflected in the measurement result of the CDC. If the external equipment is accurate and stable enough, it is possible to obtain the thermal drift of the CDC by comparing the two results [6].

To do so, both the CDC under test and the capacitor are positioned in the climate chamber with changing temperature. The precision equipment, on the contrary, is located outside the climate chamber where the temperature variation is much smaller. Under this conditions, employing a precision capacitor meter with low thermal drift (which can also tolerate longer cables) guarantees negligible effect of the slightly varying room temperature on the measured value of the capacitance. At each temperature point in the climate chamber, the capacitance is measured by both the CDC and the external equipment. With this method, it is important to ensure that the CDC and the external equipment measure the same capacitance. The solution to it will be discussed in section 6.3.2.

Method II: Capacitor with known temperature characteristic

The measurement can be completed with capacitors with pre-qualified temperature characteristic. In this case, the measurement result of the CDC is a combination of its own thermal drift and the temperature characteristic of the measured capacitor. Since the temperature behaviour of the capacitor is known, the thermal drift of the CDC can be obtained by removing the capacitor impacts from the measurement results.

However, this method also foresees challenges. First, the temperature characteristic of a capacitor may vary, meaning that the pre-qualified behaviour may not be exactly the same as the behaviour during the CDC measurement. Hence, the estimated CDC drift (by removing the pre-qualified capacitor impact from the CDC measurement result) may deviate from the actual value. Second, the parasitic associated with the pre-qualification system and the CDC measurement setup can be different, which will affect the accuracy of the measurement.

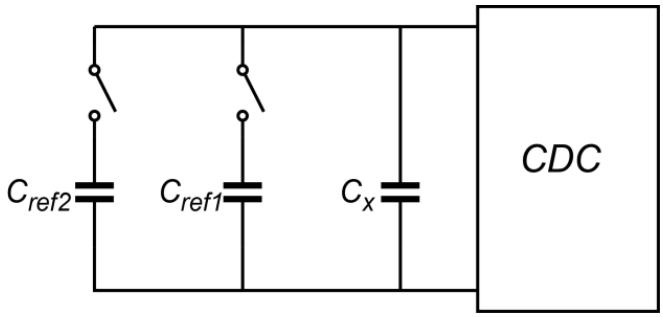

Fig. 6-2. Measurement setup for linearity test

C). Linearity

In principle, the linearity measurement is performed by sweeping the input signal across the measurement range, in which the Delta-sigma loop is stable, and recording the decimated outputs. Then, the nonlinearity can be obtained by calculating the point-to-point deviation between the measured results and the ideal linear curve.

In the case of CDC, however, the above method is difficult, because of the following reasons:

- It is difficult to have an accurate capacitor bank that generates a swept capacitance across the input range with pre-defined step size;
- The parasitic due to the capacitor connections degrade the linearity results;

Solution:

The integral non-linearity of the interface can be verified by the following approach: C_{ref1} and C_{ref2} are two extra small capacitors (on-board) other than the sensor capacitor C_x (Fig. 6-2). To test the linearity, four separate measurements are made, as shown in the following equations.

$$\mu_1 = \frac{C_x}{\Delta t / R_{ref}} \tag{6-2}$$

$$\mu_2 = \frac{C_x + C_{ref1}}{\Delta t / R_{ref}} \tag{6-3}$$

$$\mu_3 = \frac{C_x + C_{ref2}}{\Delta t / R_{ref}} \tag{6-4}$$

$$\mu_4 = \frac{C_x + C_{ref1} + C_{ref2}}{\Delta t / R_{ref}} \tag{6-5}$$

Ideally, we should have the following relation:

$$\mu_1 + \mu_4 = \mu_2 + \mu_3 \tag{6-6}$$

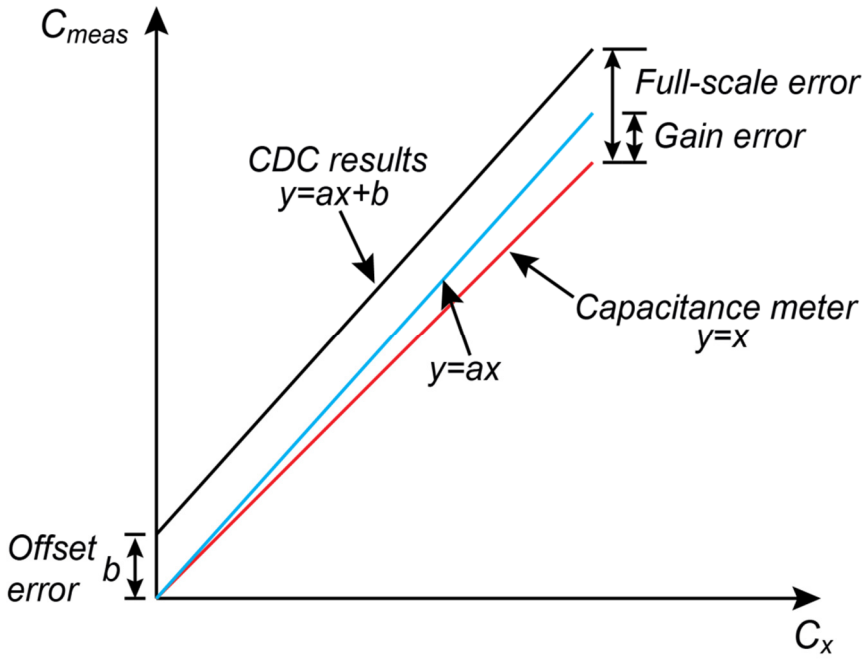

Fig. 6-3. Measurement error of a CDC with respect to the ideal linear transfer characteristic

In this case, the inaccuracy of C_{ref1} and C_{ref2} are not important, because they cancel each other in the equation. Only we have to make sure that during the separate tests, they do not drift due to environment variation, e.g. temperature or humidity. The integral non-linearity is defined as [7-9]:

$$\text{Nonlinearity}=(\mu_1+\mu_4)-(\mu_2+\mu_3) \tag{6-7}$$

Another advantage of this solution is that it is insensitive to parasitic capacitances that are associated with the measurement setup, e.g. the parasitic capacitances of the connection wires or the switches, provided that those parasitic capacitances do not change during the four consecutive measurements [7, 9]. This is because the parasitic effects will be included in the measurement of μ_1 to μ_4 and are compensated during the calculation of nonlinearity using Eq. (6-7). Hence, the measured nonlinearity does not depend on the parasitic effects and thus is more reliable.

D). Accuracy/precision

The measurement accuracy of the CDC can be qualified by comparing its measurement result with that of an accurate capacitance meter, e.g. a precision impedance analyser. To this end, both the CDC and the capacitance meter are used to measure the same capacitor. Then, their results are compared so that the deviation of the CDC measurement from that of the capacitance meter is the inaccuracy.

As shown in Fig. 6-3, the measurement is performed across the capacitance input range (3.5 pF to 17.5 pF), and both the offset error (additive error) and gain error (multiplicative error) of the

CDC are determined. By repeating the same measurements with different chips, it is also possible to qualify the chip-to-chip tolerance. Besides, using the results, the non-linearity of the CDC can also be determined in an alternative way to the one described in the previous section.

6.2.2 Design for testability

A test-friendly chip should be sufficiently tunable and observable. To increase the accessibility and adjustability of the sub-circuits, as well as to enable the chip to work in multiple operation modes, a set of design-for-testability (DFT) circuit techniques is included in the prototype design, which significantly improves the testability of the chip. An overview of these techniques is given in this section.

A). Configurable input capacitors

For testing flexibility, the CDC is designed such that it can either measure off-chip capacitor or on-chip capacitor. Figure 6-4 shows the schematic of the frontend stage, including the capacitors that can be selected. To balance the circuit, the replica side is designed to be exactly the same as the sensor side. The configuration to select between on-chip and off-chip capacitors are done by a shift register, which will be shown later.

To select between the capacitors, simple MOS switches are utilized. By controlling the signal S_1 and S_2, it is possible to switch between the off-chip and on-chip capacitors. The configuration is only done before the operation of the CDC, hence there is no switching during measurement. For this reason, those switches are relatively large to minimize the on-resistance for fast settling. The switches on the replica side are controlled by the same clocks as the sensor side. Hence, it is always ensured that the two paths are well-matched in terms of their parasitics, which helps to reduce the coupling noise and charge-injection errors.

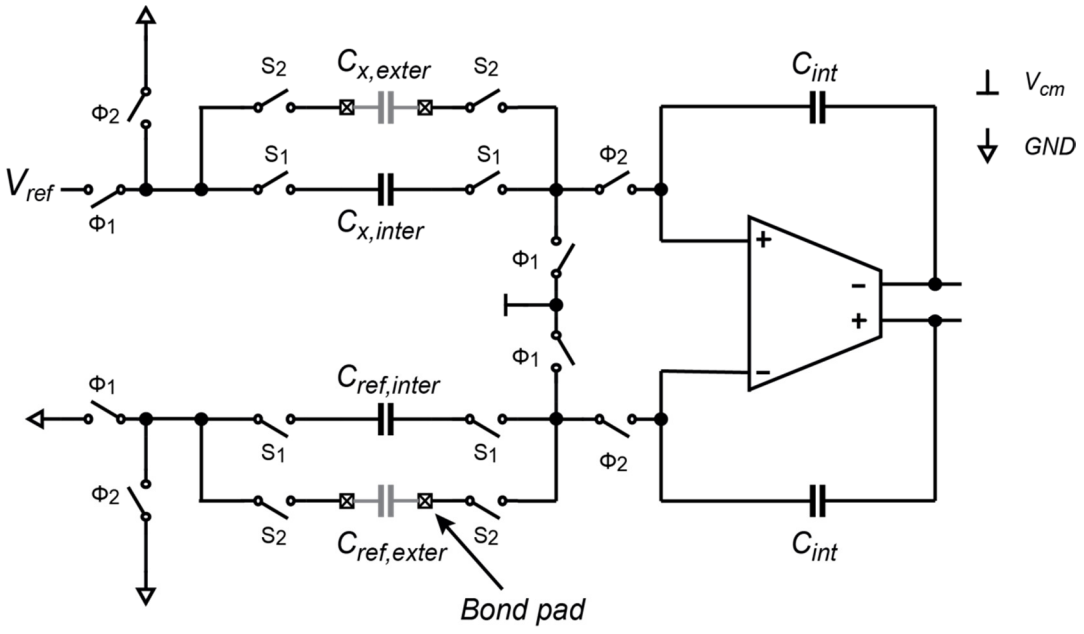

Fig. 6-4. Frontend stage of the precision CDC, with configurable sensor capacitors

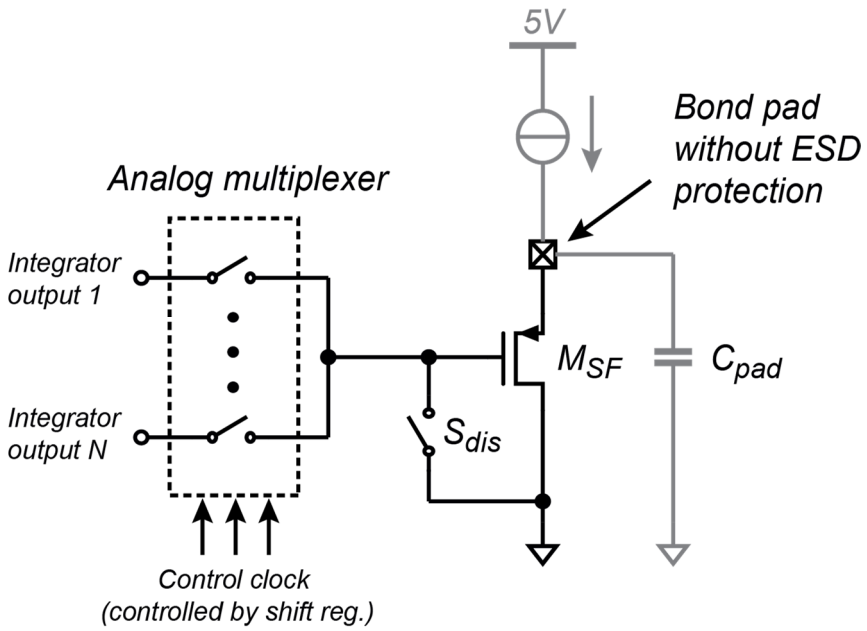

Fig. 6-5. Schematic of the output source follower for observing the waveforms of internal nodes

B). Output source follower

To facilitate observation of the voltage waveforms of the internal nodes without disturbing the normal circuit operation, such as the output nodes of the switched-capacitor integrators, on-chip analog output buffers are implemented. As illustrated in Figure 6-5, the core of such an analog output buffer is a PMOS source-follower (M_{SF}), which is driven by a constant current source from the test board. The source of M_{SF} is directly connected to a test I/O pad without ESD protection circuit (to prevent the clipping of the output due to limited voltage supply level of the chip). Therefore, the voltage waveform on the gate of M_{SF} can be reproduced at the test I/O pad with a shifted DC level, depending on the threshold voltage of the transistor (for the selected technology, the voltage shift is around 0.5 V ~0.7 V). Since there is no ESD protection circuit in the pad, the voltage level of the shifted waveform can be higher than the supply voltage of the chip. Regarding the heavy capacitive load on the I/O pad (C_{pad} can be as high as 10 pF), a large transconductance of M_{SF} (large area and aspect ratio) is required to ensure that the source-follower is fast enough to track the probed signal.

To increase the hardware efficiency, multiplexed switches are introduced so that each source-follower (and the associated test I/O pad) can be used for probing multiple internal nodes. These switches are controlled by the corresponding bits in the shift register. When analog probing is not needed, all multiplexed switches can be turned off, and the input of the source-follower is grounded by a NMOS switch (S_{dis}) to prevent undesired floating nodes (Fig. 6-5).

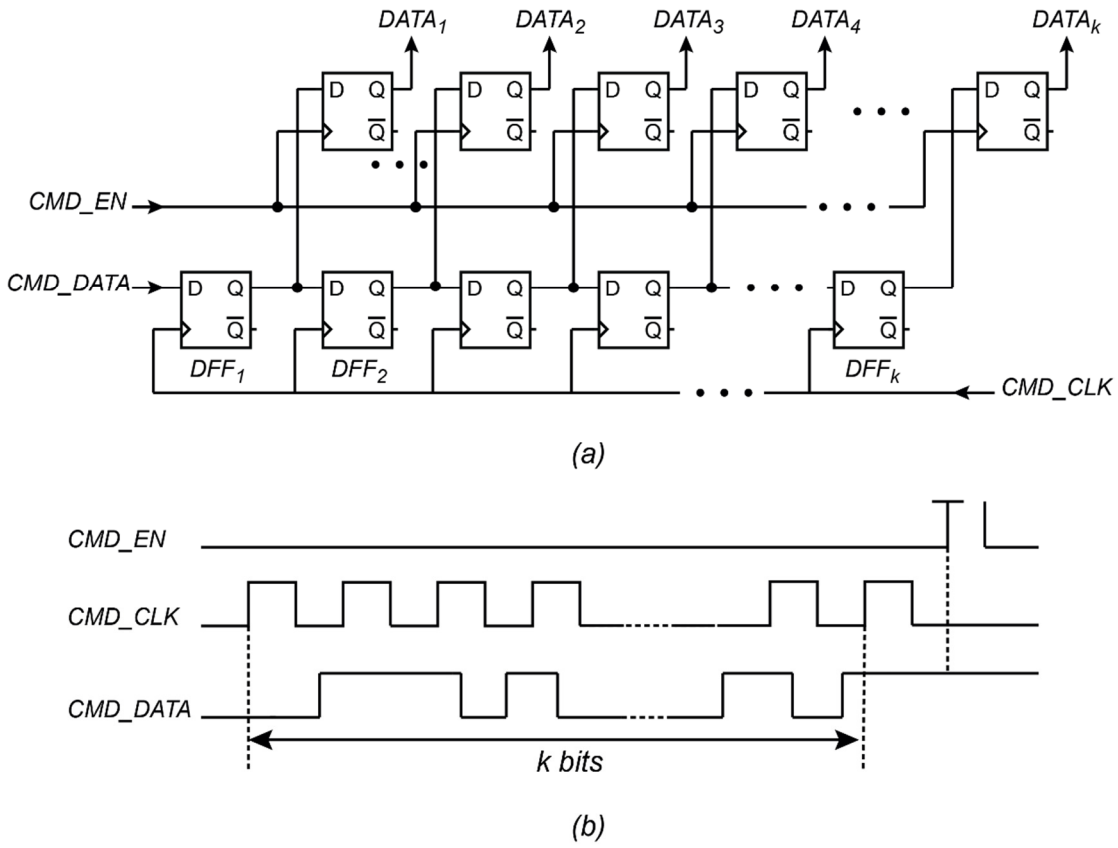

Fig. 6-6. (a) Schematic of the shift-register for configuring the CDC chip; (b) Timing of the shift-register during configuration

C). Shift register

A serial-in, parallel-out shift-register (Fig. 6-6 (a)) is used for the configuration of the prototype chip, which is built using standard D-flipflops (DFF). This is an efficient approach to configure the chip with multi-mode functionality, as only three extra digital I/O pins are needed: a command word serial input (*CMD_DATA*), a command word read-in clock (*CMD_CLK*) and a configuration enable trigger (*CMD_EN*). The length of the shift-register equals to that of the configuration command word.

Figure. 6-6 (b) shows the timing diagram of the proposed circuit. At each rising edge of the command clock (*CMD_CLK*), one bit of the serial configuration commands (*CMD_DATA*) is shifted into the DFF chain. When all the *k* bits commands have been shifted in, the enable trigger (*CMD_EN*) locks the data to a parallel row of DFFs. The outputs of these registers ($DATA_{1\_n}$) are then available for the configuration of the core circuits. After that, even if the *CMD_CLK* keeps operating, the configuration settings will not be altered. The command data can be either generated from an offchip FPGA or data acquisition device (DAQ).

In the prototype chip design, a 20-bit configuration word is defined. In reality, if the command clocks that drive the DFF chain are exactly the same for all the DFFs, it might happen that the previous command data, which is supposed to shift into next DFF, is refreshed by the new data. The situation becomes even worse when the DFFs are active after their preceding DFF, due to

the delay of the clocks. For instance, if DFF_1 is active before DFF_2, the command data that is supposed to shift to DFF_2 will be refreshed by the data of DFF_1. This problem can be eliminated by clever layout. As shown in Fig. 6-6 (a), the CMD_CLK enters the DFF chain from the right side while the CMD_DATA is from the left side. In this case, the parasitic resistance and capacitance of the metal tracks act as delay element, which cause small delay of the clocks between the DFFs. Therefore, it ensures that the DFFs are activated sequentially from right to the left, so that the data is shifted from one DFF to the next DFF without being overwritten by the new inputs.

6.3 Measurement results

In the previous section, the measurement strategies and the integrated additional features enabling the qualification tests have been presented. Here we first introduce the general measurement setup. Next, we present the specific modifications of the test setup needed for each measurement and the obtained measurement results.

6.3.1 Measurement setup

Figure. 6-7 shows an overview of the general measurement setup. The CDC chip together with the precision references and the sensor capacitor are mounted on a printed circuit board (PCB). For flexibility, the control clocks for the Delta-sigma modulation are provided by an FPGA. The generated digital bitstream (BS) is acquired by the FPGA and then transmitted to a National Instrument NI-6259 data acquisition board (DAQ), which communicates with the measurement PC via a USB cable. At the measurement PC, a graphical user interface is designed in Labview, which controls and visualizes the overall measurement. To adapt to different measurements that are targeting different specifications, this measurement setup is modified accordingly, as will be shown in Section 6.3.

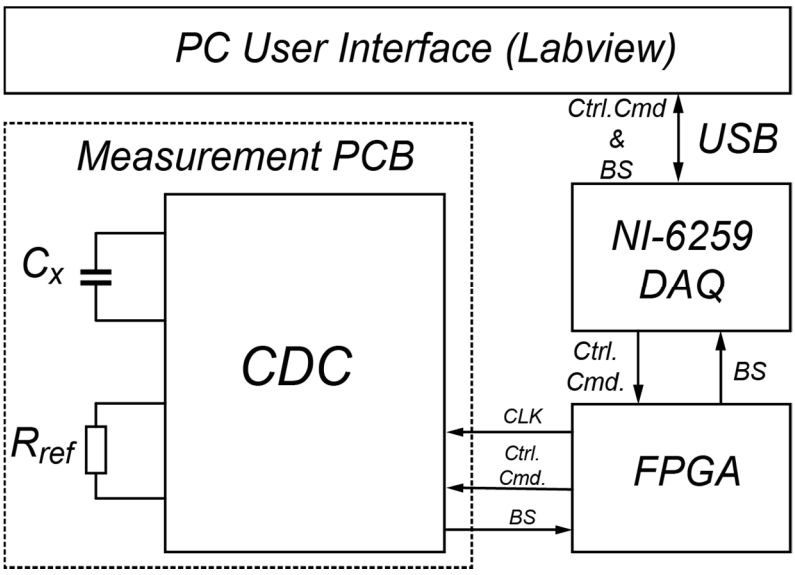

Fig. 6-7. Block diagram of the general measurement setup

Before starting the operation of the CDC, the user sets the control command in the user interface. Then, the control command is sent from the DAQ to the FPGA. The FPGA level-shifted the control command to 3.3-V logic and configures the on-chip shift register (section 6.2.4). After finishing the configuration, the FPGA starts generating control clocks for the CDC operation and acquiring the output digital bitstream of the CDC. The acquired digital bitstream is sent to the PC for real-time processing and storing. The user interface displays the real-time measurement results, including the measured capacitance, noise spectrum and ambient temperature. Besides, all the information is saved to text files for further data processing.

In the previous section, the measurement strategies and the additional features in the designed integrated circuit have been presented. To adapt the measurement setup to specific measurements, several modifications are required. This section focuses on specific measurements that are important for qualifying the CDC. Their measurement setups are first discussed. Then, the measurement results are shown and analyzed in detail.

6.3.2. Resolution

Figure. 6-8 shows a 65536-point FFT of the measured output digital bitstream, which clearly demonstrates a third-order noise shaping. To determine the resolution of the CDC, the standard deviation of the decimated output bitstream relative to the nominal capacitance is measured.

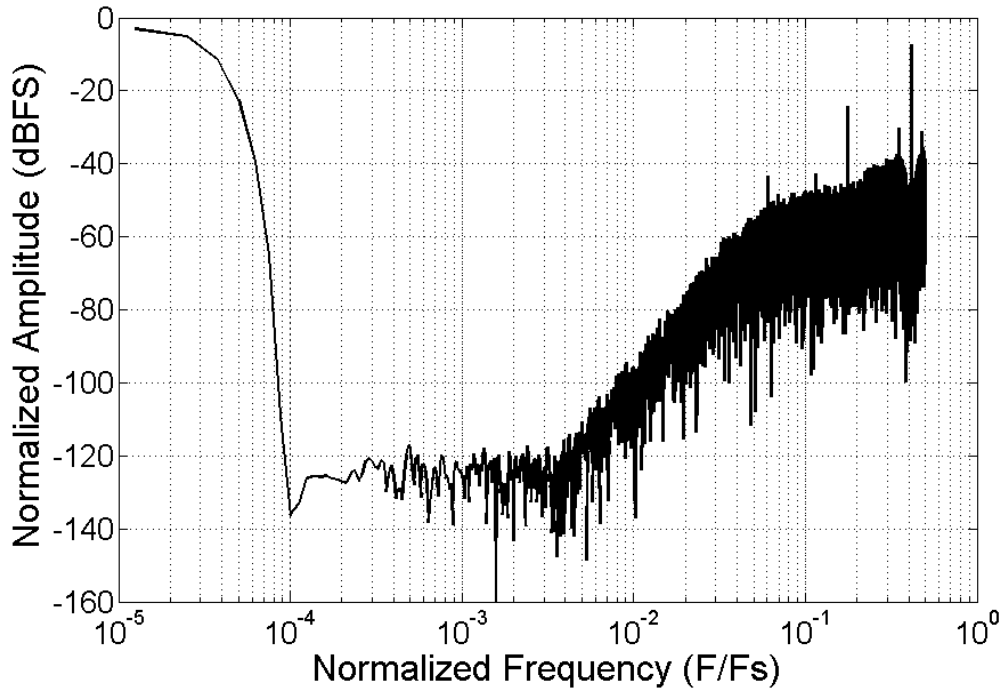

Fig. 6-8. Measured 65536-point FFT of the output digital bitstream with Kaiser window (frequency normalized to the average sampling frequency Fs=100 Hz)

Figure. 6-9 is a measured signal-to-noise ratio (SNR) as a function of the operating cycles. At low operating cycles, the quantization noise dominates the overall noise performance, thus with increased number of operating cycles the SNR increases fast (~12 dB improvement per doubling of the operating cycles [10]). After about 500 cycles, the thermal noise becomes the dominant noise source of the system, so the noise reduction follows the square-root law. E.g. ~ 3 dB improvement of the SNR for every doubling of the operating cycles.

At N=2000 (10 ms conversion time), the CDC achieves a dynamic range (DR) of around 18 bits, corresponding to an input-referred capacitance RMS noise of 42 aF with respect to an input range of 16 pF (6 pF to 22 pF). This is with good agreement with the theoretical analysis (Fig. 4-18). The small difference in the final resolution may be due to the fact that parasitic capacitance at the virtual ground would increase the noise gain which degrades the noise performance. Moreover, the noise of the reference voltages further degrades the performance. These factors are hard to estimate and were not included in the theoretical analysis of Chapter. 4.

It is worth mention that the CDC is heavily thermal noise dominated. In principle, a second-order Delta-sigma may better balance the quantization noise and the thermal noise, making the design more power-efficient [1]. However, adding one extra loop filter only increases the overall power consumption by less than 10 %. Therefore, for conservative consideration, this work implemented a third-order loop filter to guarantee that the quantization noise is insignificant.

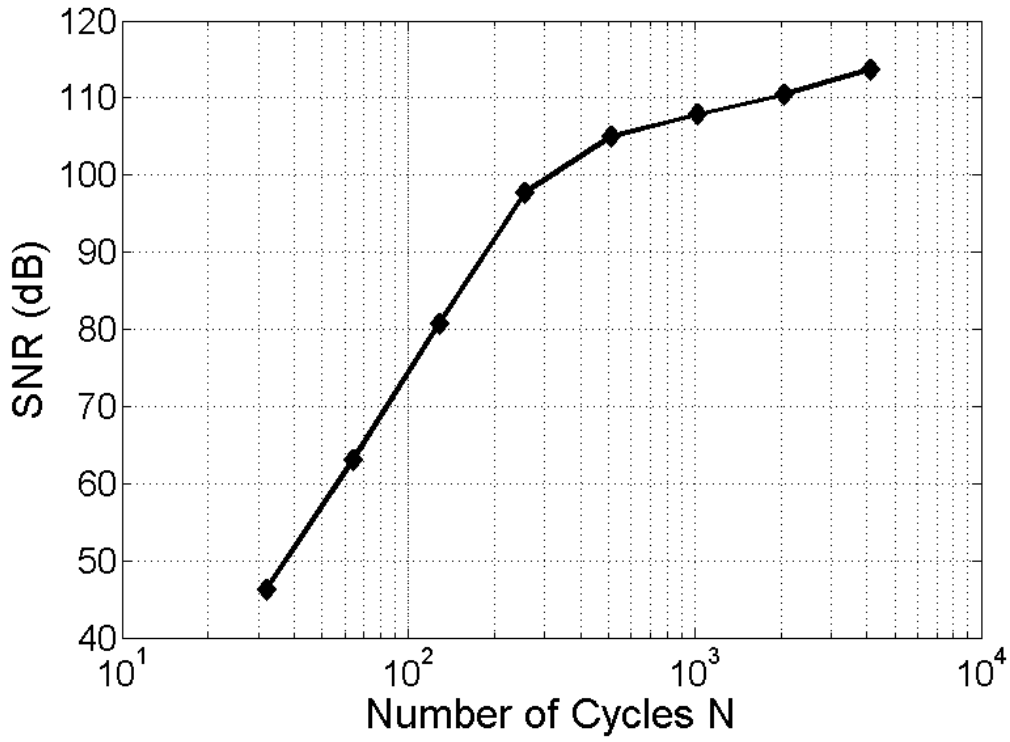

Fig. 6-9. Measured CDC resolution as a function of the number of operating cycles N

6.3.3. Stability

Stability (thermal and long-term) is the most important specification for the CDC. Hence, the qualification of the CDC stability is carefully performed, by taking care of all the impacts of the measurement setup. Since the design is targeting thermal drift below 10 ppm/^{O}C, any small error or instability of the measurement setup can compromise the measurement results. Therefore, it requires both a careful design of the measurement setup and a reliable execution of the measurement.

6.3.4. Thermal stability

To determine the thermal stability, two types of measurements are performed. One is based on measuring an on-chip capacitor at different temperatures and then comparing the results with documented temperature coefficient (TC) of the capacitor. The other is to measure an off-chip ceramic capacitor at different temperatures using both the CDC and an external precision capacitance meter.

6.3.4.1. Thermal stability measurement with off-chip C0G ceramic capacitor

As described in section 6.2.2, the thermal stability of the proposed CDC is qualified by measuring a capacitor with both the CDC and an external precision capacitance meter at each temperature points. In this way, the external capacitance meter measures the thermal characteristic of the capacitor. The results with the CDC contain the thermal characteristic of both the capacitor and the CDC itself. Hence, by comparing the results with the CDC and the precision capacitance meter, the thermal stability of the CDC can be extracted.

A measurement setup is proposed in Fig. 6-10, which is an updated version of the general measurement setup (Fig. 6-7). The CDC as well as the measured capacitor is located in a climate chamber in which the temperature is swept from 20 ^{O}C to 70 ^{O}C with a step size of 10^{O}C. The whole setup is in good thermal contact with an aluminum block, which stabilizes the temperature, as shown in Fig. 6-12. The temperature of the aluminum block is monitored by a commercial Pt-100 temperature sensor, which is interfaced by a Keithley 2000 digital multimeter.

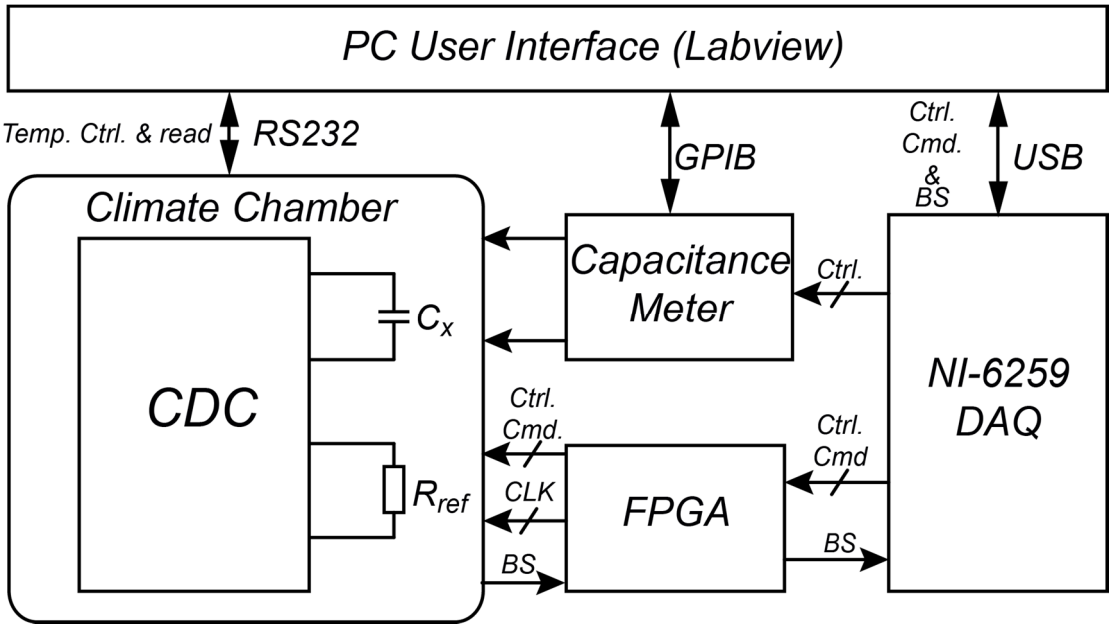

Fig. 6-10. Measurement setup for thermal stability test

First, the capacitance is measured by an Andeen-Hagerling A2700 high precision capacitance meter [11], which reports a TC of below 0.1 ppm/^{O}C and absolute accuracy better than 10 ppm. The capacitance meter is positioned outside the climate chamber. Since the room temperature during the measurement does not vary fast, the thermal drift of the precision capacitance meter is expected to be very small (< 1 ppm). In addition, the temperature of the climate chamber is swept with a step of 10 ^{O}C, meaning that the thermal drift of the CDC would be in the range of a few tens of ppm. As a consequence, the thermal drift due to the capacitance meter will be more than two orders of magnitude less than the CDC drift. Therefore, it is reasonable to assume that the contribution of the capacitance meter to the measured thermal drift is negligible. A photo of the real measurement setup is shown in Fig. 6-11.

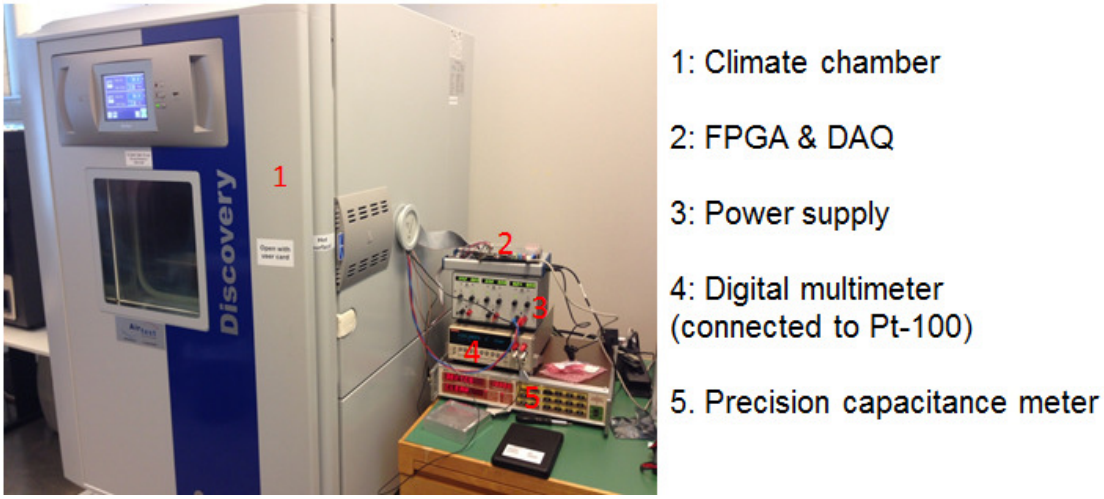

Fig. 6-11. The measurement setup for thermal stability test

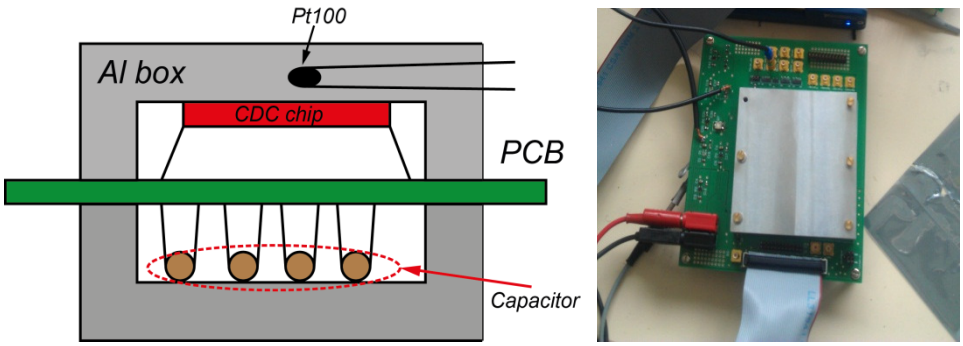

Fig. 6-12. Side view of the measurement board with Aluminum block as large thermal mass to stabilize the system temperature

In Fig. 6-12, it is shown that an Aluminum block surrounds the CDC with good thermal contact, which acts as a large thermal mass to stabilize the temperature variation of the system. The Pt-100 temperature sensor is in good thermal contact with the Aluminum block. Hence, it measures the real temperature of the CDC system. To reduce the error of the registered temperature value, sufficient time is allowed for thermal stabilization of the setup at each measurement point. At each stabilized temperature the capacitance of the capacitor is measured and recorded.

In the real measurement setup, however, the parasitic capacitance due to the connection wires (e.g. the connection between the capacitance meter and the PCB/capacitor) contribute to the measurement errors. Moreover, the parasitic is temperature-dependent, which leads to thermal drift of the measurement result. Such influence, if not well controlled, can easily compromise the measurement results.

To deal with the above-mentioned problem, a special design of the measurement setup and the measurement scheme is made. The schematic and timing diagram of the measurement setup is shown in Fig. 6-13.

The precision capacitance meter is connected to the measure PCB via a four-wire connection [12] to eliminate the impacts of the impedance of the connection wires on the final measurement result. To minimize the error contribution of the parasitic due to the PCB tracks, especially parasitic capacitances, an open-calibration is performed before each measurement of the capacitance meter with the help of a set of switches $S_1 \div S_4$, as shown in Fig. 6-13.

Before each measurement, the parasitic capacitance of the PCB tracks is measured during the open calibration mode. After that, the sensor capacitor C_x is measured by the capacitance meter. Then, the capacitance meter is switched off from the system and the CDC performs measurement of the same capacitor C_x. As explained earlier, the same procedure is performed at each temperature point across the range of interest (20 ^{O}C to 70 ^{O}C).

Figure. 6-14 shows the schematic of the measurement setup during open calibration, including all the parasitic elements. For simplicity, the four-wire connection is not included.

During this mode, the switches S_1 and S_4 are on, while S_2 and S_3 are off. Since the capacitance meter provides good suppression to parasitic capacitances that are coupled to ground, the effects of $C_{p7} \sim C_{p10}$ can be neglected. Since the switch S_4 is on, capacitances C_{p5} and C_{p6} are also coupled to ground, and their effect is suppressed by the low input impedance and high gain

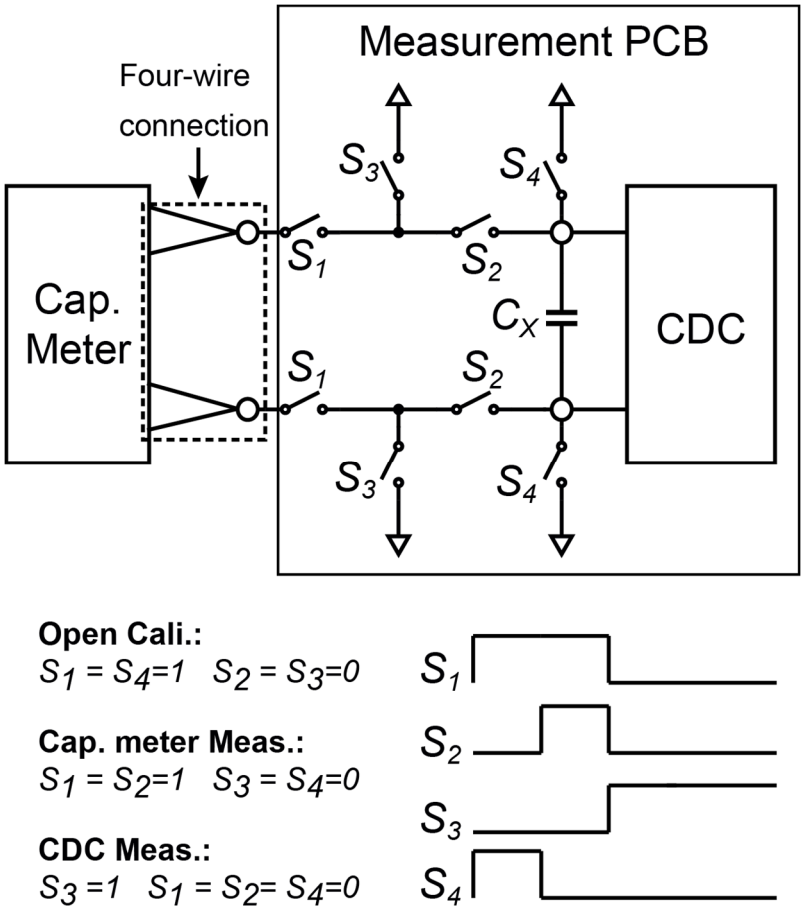

Fig. 6-13. Measurement setup for eliminating the effect of parasitic due to cabling

amplifier of the capacitance meter [11]. The other capacitances, e.g. C_{p3}, C_{p4}, are bypassed by switch S_4. Therefore, the capacitance meter measures only the parallel parasitic capacitance, which can be estimated as:

$$C_{m,open} = C_{p2} \tag{6-8}$$

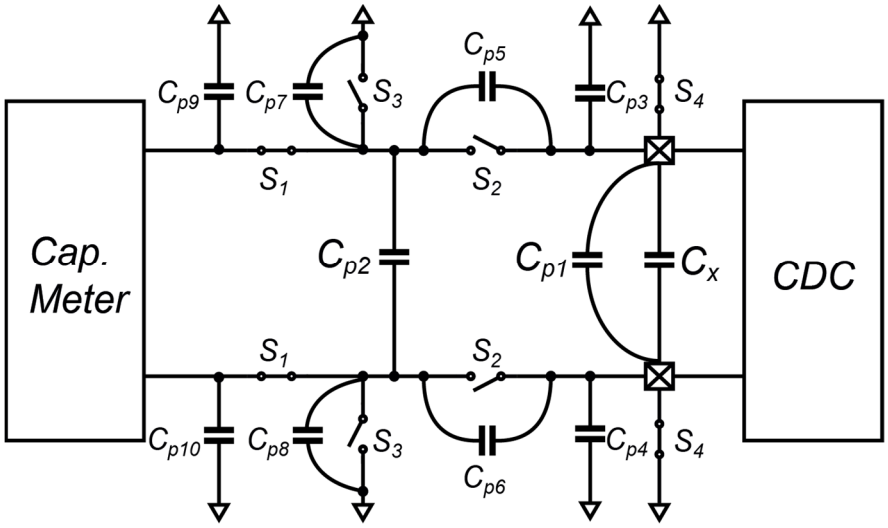

Fig. 6-14. Measurement setup during open calibration (S_1=S_4=1, S_2=S_3=0)

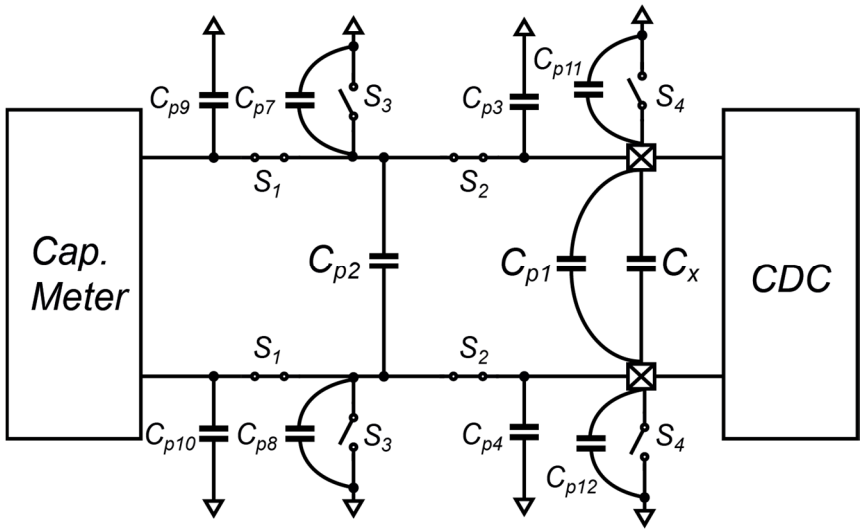

Fig. 6-15. Measurement setup during the capacitance meter measurement (S_1=S_2=1, S_3=S_4=0)

After the open calibration, the capacitance meter measures the sensor capacitor. In this mode, switch S_1 and S_2 are on, while S_3 and S_4 are off. Figure. 6-15 shows the schematic during this mode including the critical parasitic capacitances.

In this mode, the parasitic capacitances C_{p5} and C_{p6} across switch S_2 are bypassed. Hence, they are not shown in the figure. Again, since the capacitance meter is insensitive to parasitic capacitances that are coupled to ground, the capacitances C_{p3}, C_{p4}, $C_{p7} \sim C_{p12}$ are not presented in the measurement result. Hence, the capacitance meter in this mode measures the parallel combination of C_{p2}, C_{p1} and C_x, which can be written as:

$$C_{cm} = C_{p2} + C_{p1} + C_x \tag{6-9}$$

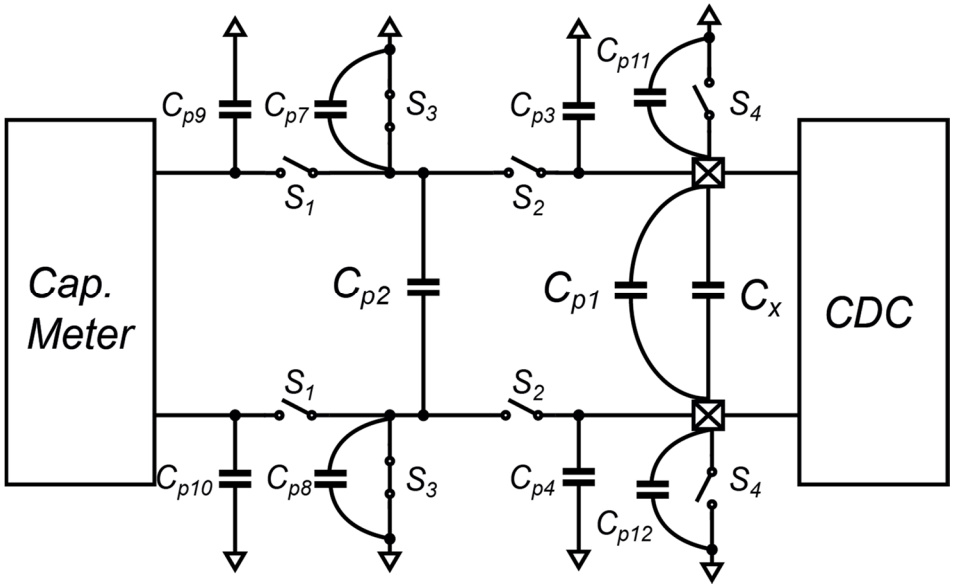

Fig. 6-16. Measurement setup during the normal operation of CDC (S_1=S_2=S_4=0, S_3=1)

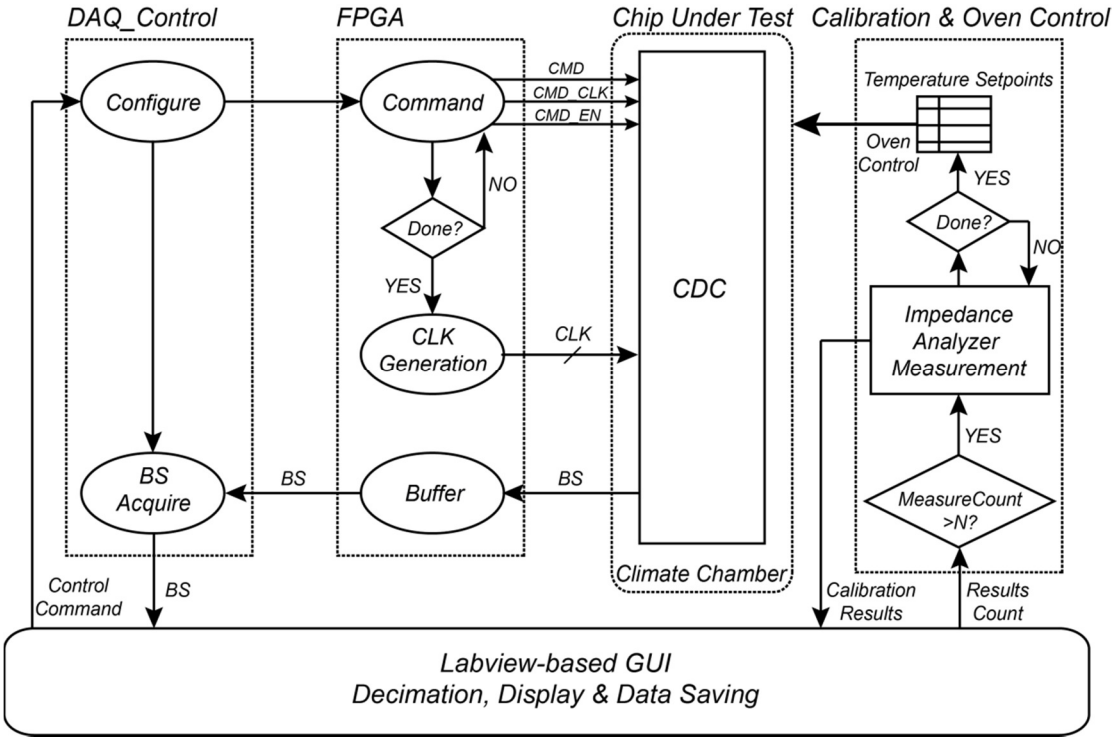

Fig. 6-17. Flaw chart of the thermal stability measurement

By subtracting the result of open calibration (Eq. (6-8)), the final measured capacitance is the parallel combination of C_{p1} and C_x, as shown:

$$C_{cm,final} = C_{cm} - C_{cm,open} = C_{p1} + C_x \tag{6-10}$$

During the CDC measurement mode, the setup is configured such that the capacitance meter is switched off from the system. Fig. 6-16 depicts the schematic in this mode, including the critical parasitic capacitances. In this mode, switches S_1, S_2 and S_4 are off, disconnecting the capacitance meter from C_x. Besides, switch S_3 is on, which bypasses the parasitic $C_{p7} \sim C_{p10}$ as well as C_{p2}.

If the CDC is well designed such that it provides low impedance excitation and ideal virtual ground, the parasitic capacitances C_{p3}, C_{p4}, C_{p11} and C_{p12} will not affect the measurement result. Hence, the CDC measures the parallel combination of C_{p1} and C_x:

$$C_{CDC} = C_{p1} + C_x \tag{6-11}$$

According to the above analysis, with the implemented measurement and calibration scheme, the CDC and the capacitance meter measure the same capacitance. Therefore, by comparing their measurement results, it is possible to determine the measurement error of the proposed CDC, as well as the thermal stability.

Figure 6-17 shows a flaw chart of the thermal stability measurement. Before starting the measurement, the DAQ sends a configuration command to the CDC, which configures the shift register of the chip (section. 6.2.3). Then, the Labview-based program controls the climate chamber to reach the pre-defined temperature set point. Meanwhile, the Pt-100 temperature sensor monitors the temperature of the climate chamber. When the temperature stabilizes at the

set-point, the FPGA starts generating control clocks for the Delta-sigma operation and receives back the digital bitstream of the CDC. After receiving the pre-defined number (N) of digital bitstream, the CDC stops its measurement. Then, the program controls the external capacitance meter to measure the same capacitor. For the measurement with capacitance meter, the above mentioned calibration scheme is implemented. Once the measurement of capacitance meter finishes, the program controls the climate chamber towards a new temperature set point and repeats the measurement at the new temperatures.

After repeating the above-mentioned measurement across the complete temperature range of interest, the results are processed to determine the thermal stability of the CDC. Fig. 6-18 shows the measurement result of four chips. As described earlier, the temperature is swept with a step size of 10 ^{O}C. Then, the thermal stability of the CDC is calculated by taking the difference of the measurement results across this range. Hence, the x-axis of Fig. 6-19 depicts the N^{th} temperature range of calculating the thermal stability (e.g. 1st: 10 ^{O}C to 20 ^{O}C, 2nd: 20 ^{O}C to 30 ^{O}C, etc.). From the plot, all of the chips show similar behavior, and all of them report thermal stability within ± 7.5 ppm/^{O}C from 20 ^{O}C to 70 ^{O}C.

The measured temperature characteristic, however, shows a strange trend: the temperature coefficient reduces with increasing temperature. This does not comply with the thermal characteristic of the references. The strange effect could either be due to the CDC itself or the connections to the outside world. Hence, to explore the strange effect in detail, another test is performed by measuring an on-chip capacitor. By doing this, the effect of the connections to the off-chip capacitors are eliminated, which gives a more insight view of the CDC.

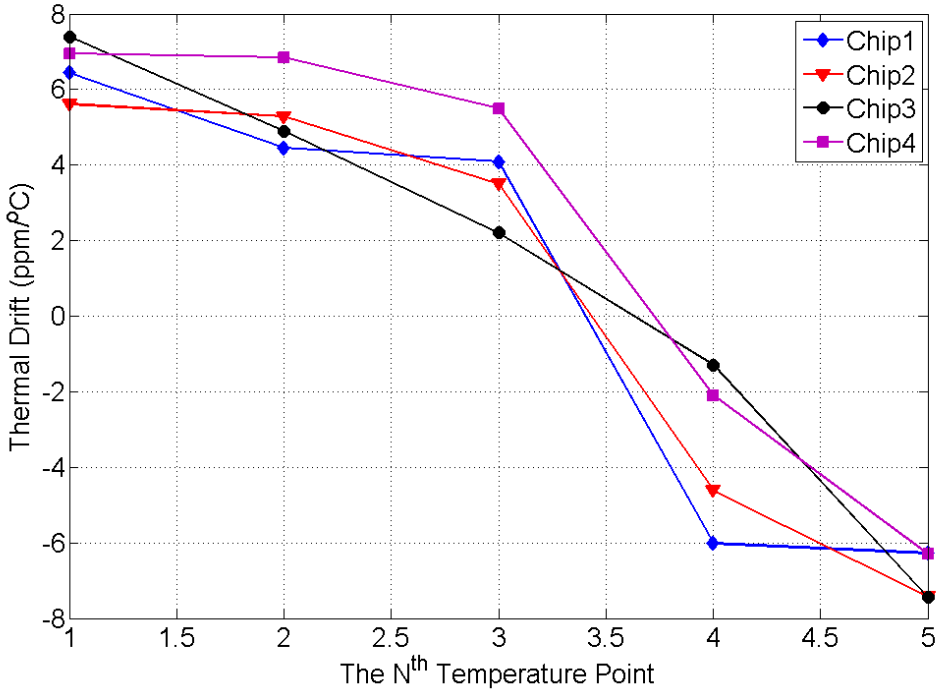

Fig. 6-18. Measured thermal stability of the CDC, using offchip ceramic capacitor

6.3.4.2. Thermal stability measurement with on-chip polysilicon-insulator-polysilicon (PIP) capacitor

Section 6.2.2 showed that the CDC could be configured to measure either an off-chip or on-chip capacitor. In this test, the CDC is configured to measure on-chip capacitor. Figure. 6-19 shows the measurement setup for this test. The CDC, as well as the precision references, are placed in a climate chamber which temperature is swept. The temperature of the system is still measured by the Pt-100 sensor, which is in good thermal contact with the Aluminum block, as shown in Fig. 6-12. At each stabilized temperature, the on-chip capacitance is measured by the CDC and the results are recorded.

The measurement results are plotted in Fig. 6-20. In this test, 10 chips are measured, and all of them show very similar behavior. The temperature drift for all the chips are around 24 ppm/^{O}C. However, in these results is incorporated the thermal drift of the measured on-chip PIP capacitor, which is specified to have a temperature coefficient of approximately 30 ppm/^{O}C [Ref. C35 datasheet]. Therefore, the thermal drift contributed by the CDC is around 6 ppm/^{O}C across the entire temperature range of interest. According to the specifications of the reference resistors and the crystal oscillator, the ultimate achievable thermal drift should be around 1~ 2 ppm/^{O}C. Therefore, it means that the CDC circuit contributes to extra thermal instabilities. This

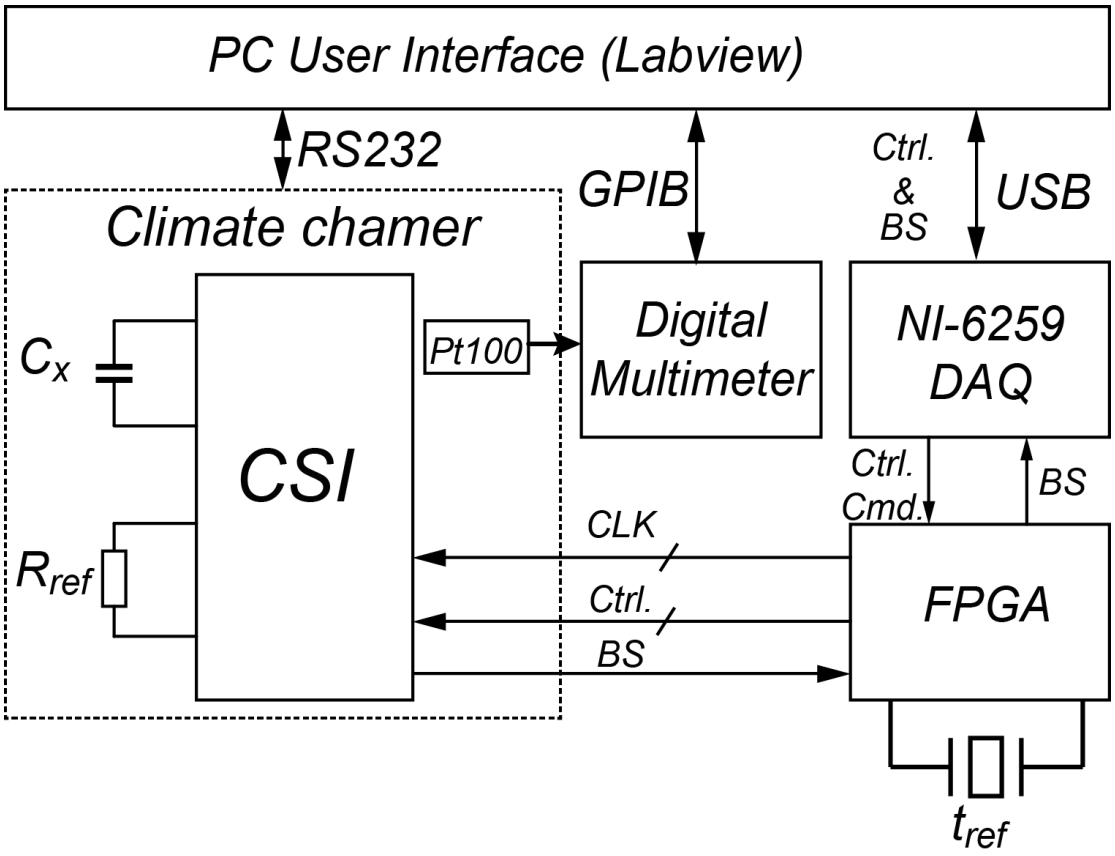

Fig. 6-19. Measurement setup for thermal stability test with onchip capacitor.

might be due to the incomplete compensation of the offset and the charge-injection errors. Besides, it could also be a result of the tolerance of the temperature coefficient of the PIP capacitor, which deviates from the pre-defined 30 ppm/^{O}C.

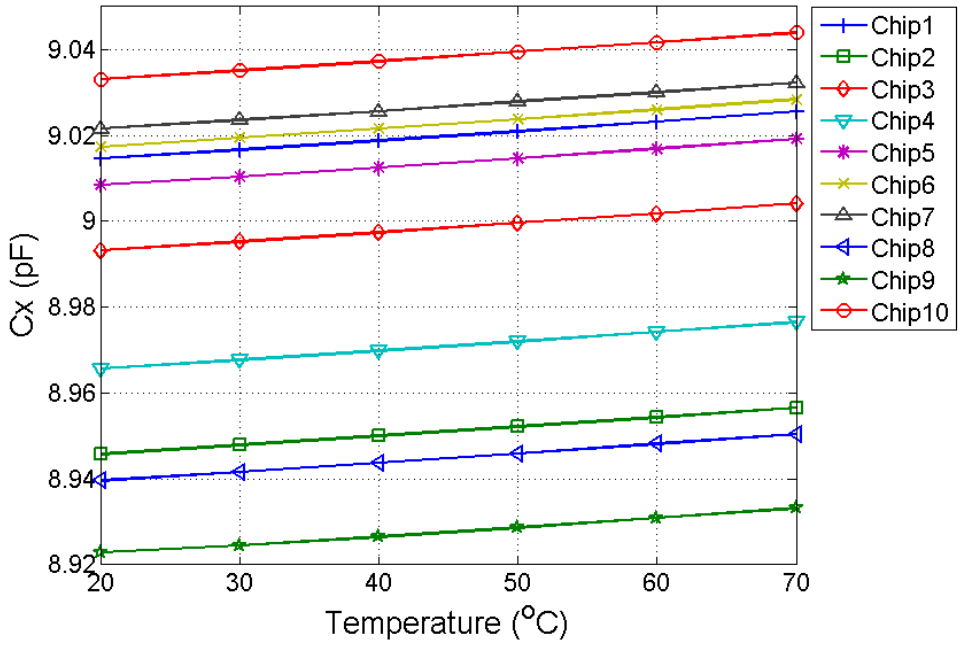

Fig. 6-20. Measured capacitance at different temperature (on-chip PIP capacitor)

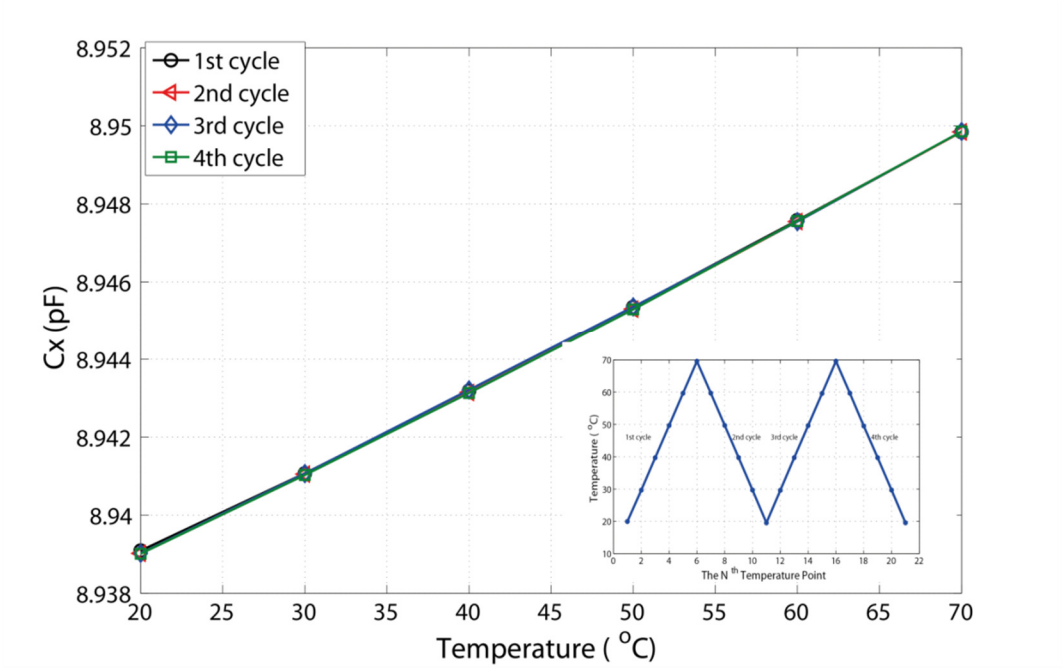

Fig. 6-21. System hysteresis and repeatability test results

To guarantee the reliability of the measurement results, the temperature was first swept upwards and then downwards, and the results at each point were recorded. As shown in Fig. 6-21, the results for the four temperature cycles are well repeatable, which proves that the system hysteresis does not have any impact on the measurement results.

As a conclusion, the temperature coefficient of the CDC is almost constant across the entire measured temperature range. The strange thermal characteristic in Fig. 6-18 is thus due to the connections to the off-chip capacitor.

B). Long-term stability measurement

To determine the long-term drift of the CDC, the setup shown in Fig. 6-9 was used. For the long-term stability measurement, the temperature and humidity of the climate chamber was kept constant. This is to eliminate the effect of environment on the final measurement results. Since the TC of the on-chip capacitor is in the order of 30 ppm/^{O}C, it is required that the temperature variation of the measurement setup should be smaller than 30 mK, so that the error contribution due to environment variation is less than 1 ppm. To guarantee this, big Aluminum block is used to stabilize the temperature of the setup. Besides, its temperature is monitored during the whole measurement. The humidity has smaller impact on the result, since an Aluminum block that prevents the air to flow into the CDC surrounds the setup. Yet during the measurement, the relative humidity is still controlled to be 50 % ± 1 %.

The measurement was performed for 116 hours. The output digital bitstream was first decimated by a Sinc^4 filter and then stored. Finally, an FFT transform was performed to the results and the noise spectrum is shown in Fig. 6-22. To verify the effectiveness of chopper, the same measurement was repeated without enabling the chopper. As can be seen from the figure, the chopper effectively reduces the *1/f* noise corner without altering the thermal noise level. The measured the *1/f* noise corner with all the choppers enabled is within 200 μHz, ensuring an hour-long stability. Fig. 6-23 shows the measured temperature and humidity of the measurement setup, as well as the capacitance. It is clear that the temperature variation during the measurement is within 0.05 ^{O}C. As the TC of the on-chip capacitor is around 30 ppm/^{O}C this temperature variation ensures that the temperature change does not degrade the performance of the CDC. From the figure, it is also clear that the measured capacitance does not have any relation with the temperature variation.

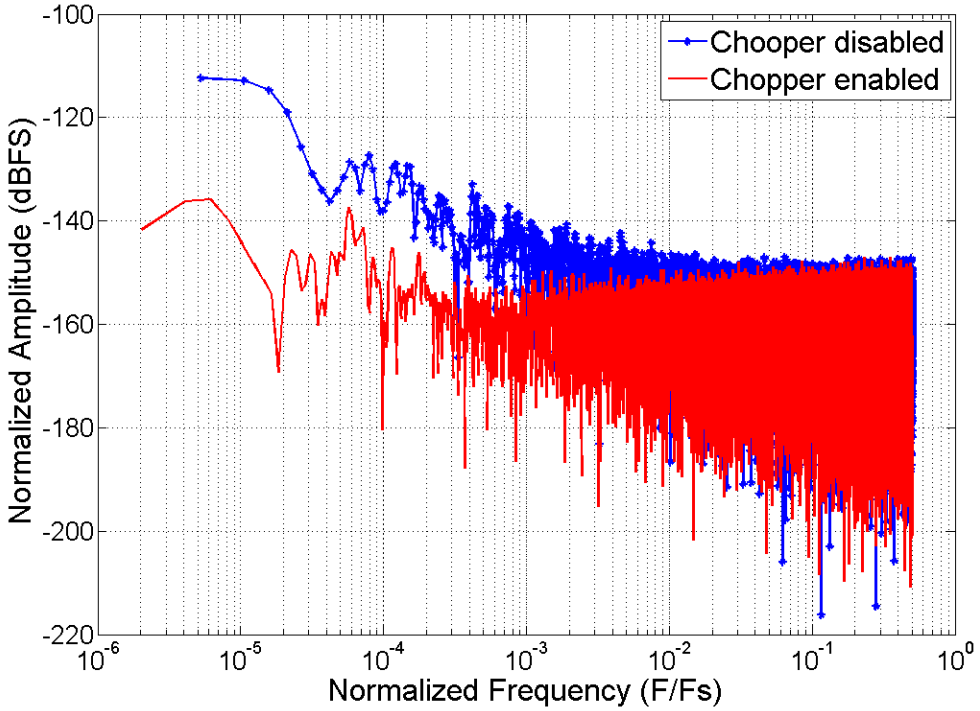

Fig. 6-22. Measured noise spectrum of the proposed CDC (results are decimated by Sinc^4 filter)

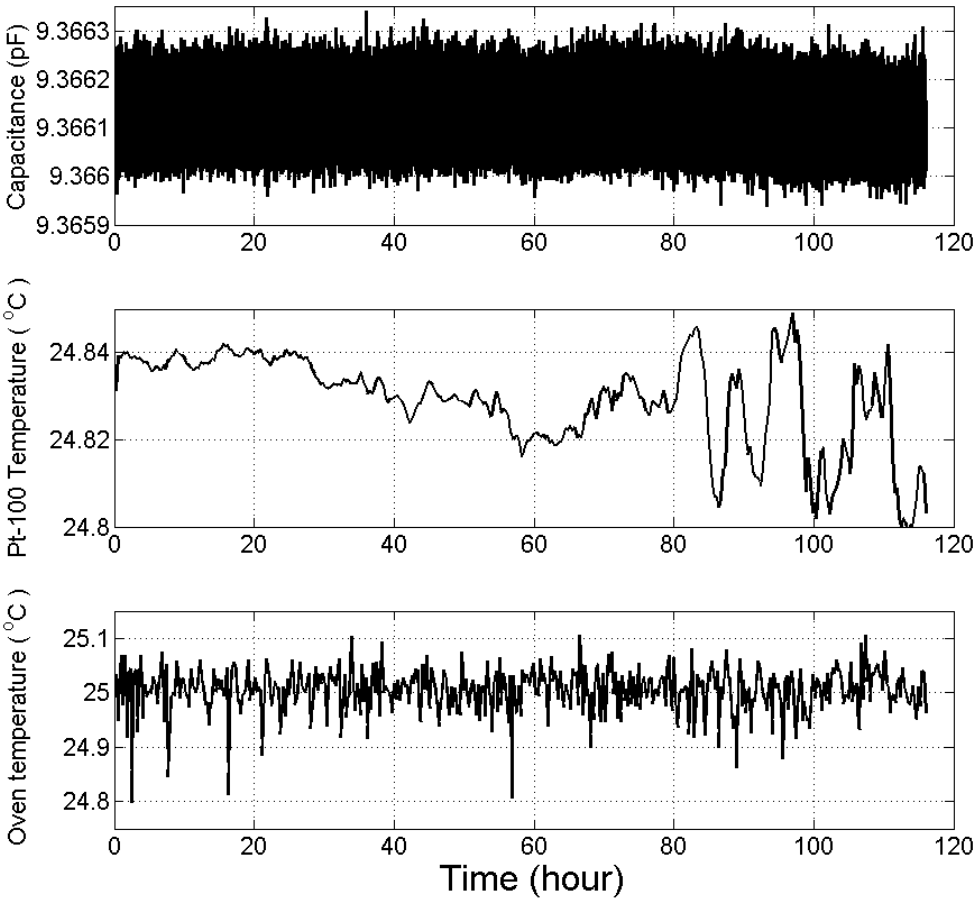

Fig. 6-23. Long term measurement of the capacitance and the temperature of the setup.

6.3.5. Transfer characteristic

The transfer characteristic of the CDC is measured by sweeping the input capacitance from 6 pF to 22 pF (stable input range of the Delta-sigma modulator). For referencing purpose, the same capacitances are measured by an external precision capacitance meter with 0.1 % absolute accuracy [11]. To ensure that the measurement of the capacitance meter is reliable and does not influence the CDC measurement, the same setup and method as for thermal stability measurement is applied (section 6.3.3), except for that the temperature of the measurement setup is fixed. The results of one chip are plotted in Fig. 6-24. As can be seen from the figure, the transfer curve of the CDC is very close to that of the precision capacitance meter. It is also observable that there is small deviation between the two curves, which seems as a combination of offset and gain error.

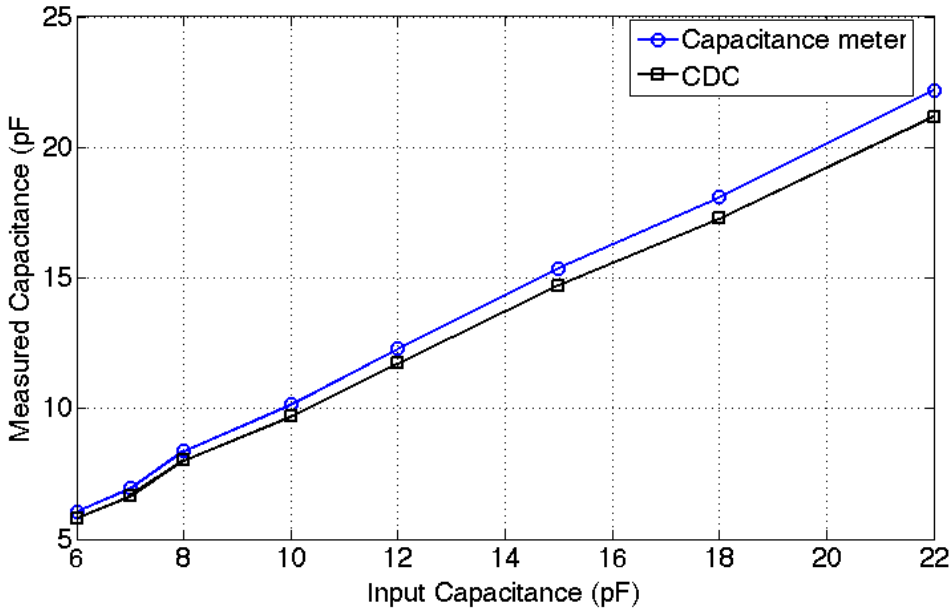

Fig. 6-24. Measured transfer curve of the CDC in comparison with that of an external precision capacitance meter

To further investigate the error, the measurement is repeated for 10 chips. To eliminate any possible errors due to the drift of the capacitance under test, the capacitance meter measurement is also repeated for 10 times, in correspondence to each of the chips. Then, the error between the CDC result and the result of the capacitance meter is calculated and plotted in Fig. 6-25, which provides a better insight of the error.

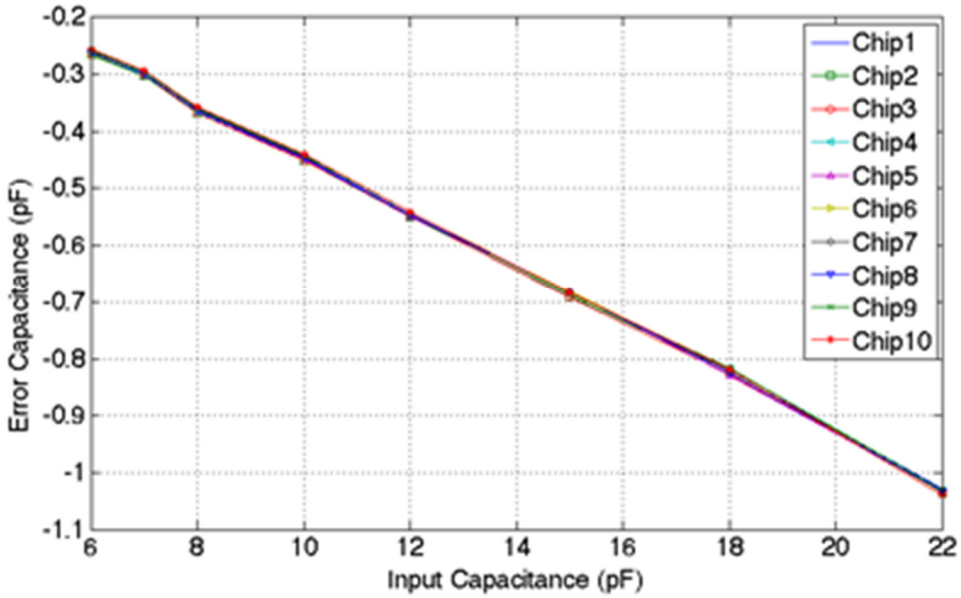

Fig. 6-25. Error capacitance of the CDC, when comparing to the external precision capacitance meter (10 chips are measured)

From Fig. 6-25 it is clear that all the chips show very similar behavior. Besides, all chips show an offset error as well as a gain error. This error may be due to the fact that the AZ clock is non-ideal, which gives an error of the overall conversion time. As described in Chapter. 4, the error of the conversion time leads to a gain error of the measurement result. Additionally, the parasitic resistances due to the connection wires to precision resistor give rise to both gain error and offset, as discussed in Chapter. 4. It is also possible that the capacitance meter is not ideal, which gives extra errors. As is shown in Fig. 6-25, the error is common to all the chips, meaning the above suspicions are reasonable. Therefore, by performing a simple 2-point calibration for one chip, it is expected that the error can be significantly reduced. Besides, as all chips show similar results, it is not necessary to calibrate all other chips but simply apply the calibration result of one chip to all others.

A two-point calibration is applied for only one chip (chip 2) at 6 pF and 22 pF, in order to compensate for the gain error and offset that are caused by the non-ideal transfer functions of both the capacitance meter and the CDC. After that, the calibrated parameters are used for all the other chips. The results show that all the chips have very similar behavior. This means that the CSI does not need extra calibration for each individual chip to achieve the same level of accuracy. In another word, the proposed CSI demonstrates low tolerance from sample to sample.

As shown in Fig. 6-26, the maximum inaccuracy is within ± 25 fF across the entire capacitance range (6 pF ~22 pF), which translates to an inaccuracy smaller than 0.2 %. This is due to the inaccuracy of the references used (e. g. R_{ref} has an inaccuracy of around 0.1 %) and the excess errors due to the CDC, such as residual offset and charge-injection, which are not completely compensated by the precision techniques applied. When comparing the results of all the chips,

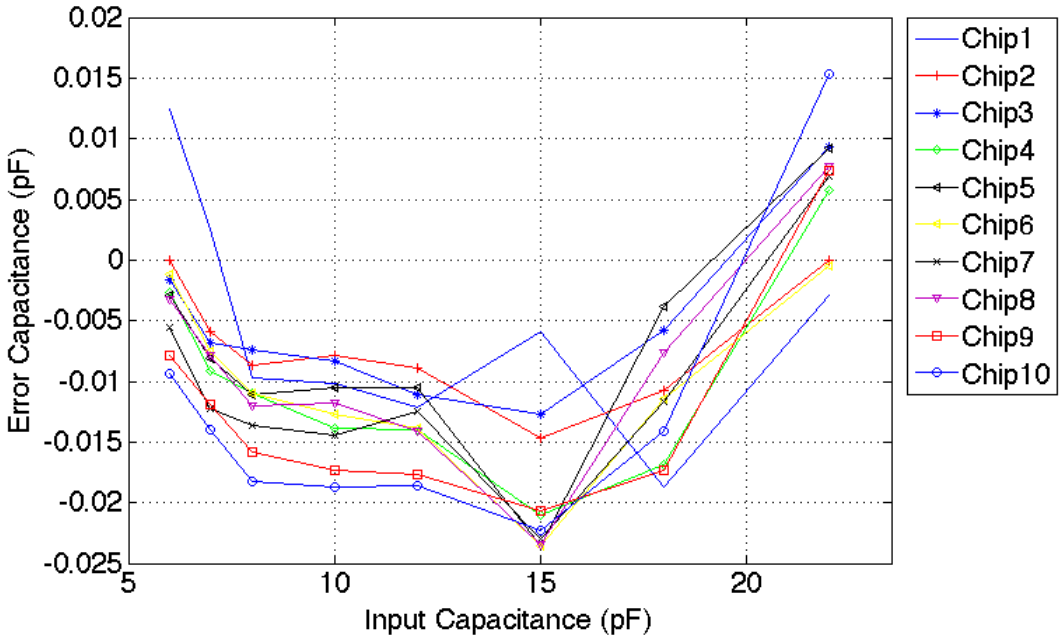

Fig. 6-26. Absolute error of the CDC measurement after a 2-point calibration of only one chip and apply the result to all other chips

the sample-to-sample tolerance is within 0.1 % without extra calibration of the individual chips. The small tolerance might be the result of the process variations or mismatches of different chips. It is also important to mention that all the chips are from the same wafer (no batch-to-batch variation).

6.5 Conclusion

In this chapter, the performance of the implemented CDC is investigated based on experiments. To perform the experiments in a reliable way, a series of measurement strategies are proposed, considering the expected performance and the limitation of the CDC. The measurement strategies then provide good basis for designing reliable measurement setup. To add more flexibility and testability to the CDC chip, a set of design for testability (DFT) blocks have been implemented.

The measured noise level shows good alignment with theoretical analysis, which proves the effectiveness of the noise analysis in Chapter. 4. The measured signal-to-noise (SNR) with different number of operating cycles shows that the design is thermal noise dominated, which is more power-efficient than quantization noise limited implementation. This also supports the choice of high-order Delta-sigma modulator. With an operating cycle of 2000 (10 ms conversion time), the CDC achieves a resolution of around 55 aF_{rms}. The CDC has a measurement range of about 16 pF (from 6 pF to 22 pF), which corresponds to more than 18 bits DR.

To qualify the thermal stability of the CDC, a special measurement setup has been designed considering all possible error sources that may compromise the performance of the CDC. Two types of measurement schemes are proposed and tested. With on-chip capacitor, the results show a temperature coefficient of around 6 ppm/^{O}C. With the off-chip capacitor, the result is within ± 7.5 ppm/^{O}C.

The long-term stability test shows that the 1/f noise corner of the CDC is below 200 μHz, ensuring an 18-bit? hour-long stability. Besides, the measurement clearly shows the effectiveness of the implemented choppers.

The transfer characteristic measurement shows an absolute accuracy within ± 25 fF across the entire measurement range (6 pF to 22 pF). By repeating the same measurement for all the chips, it shows a chip-to-chip tolerance smaller than 0.1 %. The inaccuracy is due to both offset error and gain error. After calibrating one chip with respect to the precision capacitance meter, all chips show accuracy within 10-bit. Comparing with the state-of-the-art CDC design, this work achieves a comparable figure-of-merit (FoM), but reporting the best stability as well as accuracy.

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Chapter 7

Conclusions and Recommendations

7.1. Merits of the proposed capacitive sensor interface

This thesis presents an investigation of capacitive sensor interface for high-precision and high-resolution displacement measurement, which resulted in significant improvement of performance with respect to: thermal-stability, absolute accuracy and power-efficiency. Besides, the research offers an optimal design approach for high-performance capacitive sensor interfaces. The high-performance is achieved by a charge-balancing Delta-sigma modulator utilizing a combination of high-precision resistive and frequency references. An in-depth error analysis, as well as noise analysis, is performed, which provides optimal criteria for the design. To deal with various error sources that may influence the precision of the measurement, various precision techniques, both at system-level and at circuit level, are applied. Figure 7-1 plots the figure-of-merit (FOM) of recent published state-of-the-art CDCs in terms of their energy consumption per single measurement, as a function of the effective number of bit (ENOB). The ENOB is defined as:

$$\text{ENOB (bits)} = \left(20\log_{10}\frac{\Delta C_{\max}}{2\sqrt{2}\sigma_{rms}} - 1.76 \right) / 6.02 \tag{7-1}$$

The FOM is calculated by using the well-accepted equation for Analog-to-Digital converters, as shown:

$$FOM = \frac{Pt_{conv}}{2^{ENOB}} \tag{7-2}$$

where P is the power consumption, t_{conv} is the conversion time for one measurement; ENOB is the effective number of bits. The FoM equation provides a quantitative evaluation of the required energy to digitize the input signal. The unit of the result is J/step. For referencing purpose, two FoM lines corresponding to 1 pJ/step and 100 pJ/step are also plotted. The proposed precision CDC, as shown in the plot, shows intermediate FoM compare to state-of-the-art designs.

Table 7-1 summarizes the performance of the CDC in comparison with state-of-the-art designs. As can be seen from the table, the proposed CDC achieves comparable FoM with most of the state-of-the-art designs. But it is worth to mention that besides the FoM, this CDC also demonstrates superior precision and accuracy, thanks to the precision references used and optimal design based on the in-depth error analysis.

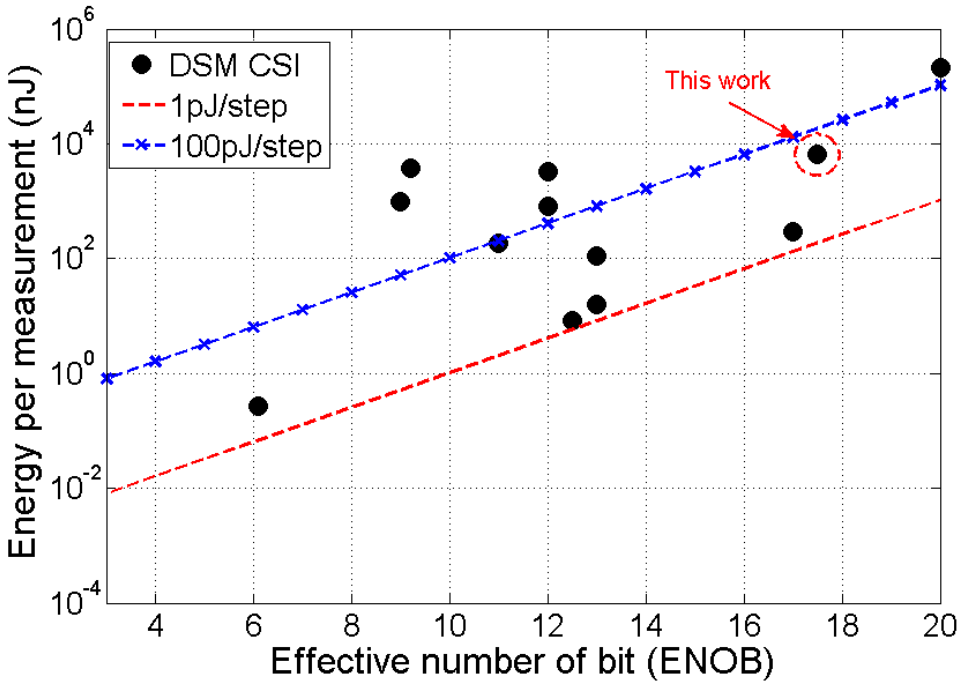

Figure. 7-1. Performance (Figure-of-Merit) comparison with state-of-the-art designs

Table. 7-1. Performance summary of the proposed CDC in comparison with state-of-the-art designs

	[1]	[2]	[3]	[4]	This work
Process	0.35µm CMOS	0.35µm CMOS	N/A	0.32 µm CMOS	0.35µm CMOS
Reference	Capacitive	Capacitive	Capacitive (Temperature stabilized)	Capacitive	Resistive & time
Sensor Capacitance (pF)	8 to 12	0.8 to 1.2	13 to 21	0 to 0.256	6 to 22
Conversion Time	20 µs	50 µs	20 ms	0.38 ms	10.5 ms
ENOB	13.5 b	8.8 b	18.2 b	6.8 b	16.7 b
Temperature Coefficient (ppm/^{O}C)	N/A	300	26	300	7.5
Absolute accuracy	N/A	N/A	0.05 %[1]	N/A	< 0.2 %[2]
Power	15 mW	15.8 mW	1.9 mW	84 µW	760 µW
FoM (pJ/step)	20.9	1765	125	283	74

[1] The accuracy is achieved by individual factory calibration and the accuracy is validated at 25 ^{O}C across the capacitance range of 13 pF to 21 pF. At different temperatures, additional compensation for gain drift over temperature is required and the exact performance is not available [3].

2 The accuracy is achieved by a two-point calibration for only one chip and then applies the result to all other chips across the range of 6 pF to 22 pF. The performance is also validated at 25 ^{O}C. However, since the tolerance of the thermal drift of the CDC is within 10 ppm at all temperatures (20 ^{O}C to 70 ^{O}C) according to Fig. 6-18, it is expected that similar accuracy can be achieved at different temperatures without the need of extra calibration.

7.2 Contributions of this research

The main contributions of this thesis are listed as follow:

- Reference components and capacitance measurement techniques providing the best long-term stability and low thermal drift are surveyed and investigated in this thesis. Due to the limited scientific information in this area it is essential to analyze the performance of existing components and solutions regarding their benefits and limitations. The outcome provides solid basis of selecting proper reference(s) and interfacing techniques for capacitance measurement. It is also found out that the combination of resistive and frequency references leads to an equivalent reference capacitance with superior precision (Chapter 2).
- It is observed that a multi-level passive controller embedded with a proportional-differential (PD) control algorithm provides a good balance among control accuracy, design complexity and power dissipation for controlling the temperature of a thermal actuator (Chapter 3).
- It is proved that by swapping the position of the measured (capacitance) and the references (resistor & time) at the input of a Delta-sigma modulator, it is possible to reduce the impact of clock non-idealities (e.g. jitter) while still being able to measure the same capacitance (Chapter 4).
- An in-depth error and noise analysis of the proposed CDC is conducted. This analysis provides a clear insight of the possible impact on the performance of the CDC of the various components and is a useful instruction for designing high-performance CDCs based on a similar structure (Chapter 4).
- The minimum required power for achieving specific noise and speed performance is derived. The derivation considers the impact of all possible components, including the bandwidth of the integrator, the capacitor network and the reference voltages. Hence, the proposed approach provides a more accurate estimation compare to the existing alternative methods. This results in more precise criteria for judging the performance of a CDC (Chapter 4).
- A solution is proposed for reducing the negative effect of the overdrive voltage at the input of an integrator caused by the continuous reference current. This intrinsic problem is solved by introducing an auto-zeroing of the integrator in a special way so that the state of the integrator is ‘frozen’ during the auto-zeroing and adding source followers at the output of the first integrator (Chapter 4).

- It is found that by "freezing" the states of the integrators, auto-zeroing (AZ) can be applied in a Delta-sigma modulator without influencing its performance. It is also proved that by combining multiple precision design techniques at both: system-level and circuit-level, it is possible to minimize the errors resulting from various non-idealities of the system (Chapter 4 and Chapter 5).
- In this thesis, a precision CDC qualification approach and process are researched by investigating potential impacts of the measurement setup/process and implementing proper solutions. Thanks to that a reliable measurement setup that provides reliable results is built (Chapter 6).

7.3 Recommendations for future works

7.3.1. Auxiliary circuit to compensate for the output common-mode drift of the first integrator as a result of input common-mode feedback

During the measurement of the proposed CDC it has been observed that the input common-mode feedback of the first integrator has an intrinsic problem that the output common-mode voltage will drift due to the charge-injection of the CMOS switches. Because of this, the CDC is not able to operate for longer time so as to further increase the resolution (as the output may saturate). As discussed in Chapter 6, this is also most likely the root-cause of the observed excess of thermal drift.

A possible solution to this intrinsic problem is to implement an auxiliary circuit that measures and compensates the output common-mode drift. The simplified schematic of the auxiliary circuit is shown in Fig. 7-2. Since the first integrator has an input common-mode regulation circuit (Chapter. 5), one side of the outputs will be the common-mode voltage while the other side is the output signal (Fig. 7-2). The output common-mode voltage V_{on} is compared with a reference common mode voltage V_{cm}. The difference between these two voltages can be used to drive an auxiliary SC network that pumps a negative charge to both inputs of the integrator so that the output common-mode drift is compensated. To this end, an auxiliary OTA is implemented (shown in the dashed rectangular), which compares the two voltages, amplifies the voltage difference and drives the SC network to compensate for the output common-mode drift. The SC network can be either driven by the same clocks of the Delta-sigma modulator (Φ_1 and Φ_2) or a slower clock that is scaled from Φ_1 and Φ_2, depending on the speed of the common-mode drift.

With the auxiliary OTA, the compensation capacitors can be much smaller compared to the sensor capacitors C_x, which does not impose extra load problem to the integrator. The accuracy of the control depends on the gain of the control loop that is formed by the auxiliary circuit and the integrator. The noise of the auxiliary OTA as well as the SC network is a common-mode

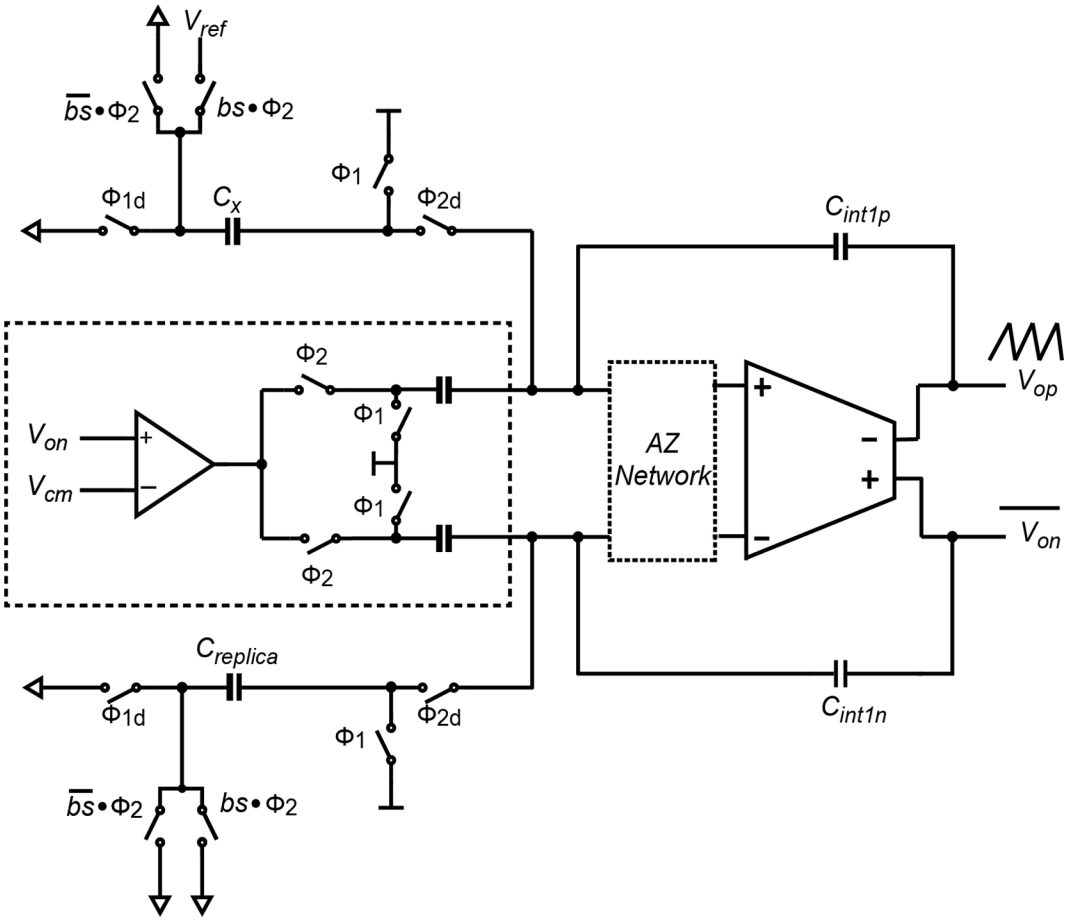

Fig. 7-2. Auxiliary switched-capacitor network to compensate for the output common-mode drift of the first integrator of the Delta-Sigma modulator.

error to the integrator. Hence, it will not degrade the noise performance of the integrator provided that the differential circuit is perfectly symmetrical. In practice, due to the mismatches of the differential inputs the performance of the integrator will degrade and thus design margins have to be reserved.

The mismatch of two differential compensation capacitors also creates measurement error (e.g. one compensation capacitor pumps more charge than the other). Therefore, system-level chopping can be applied to the auxiliary SC network to reduce the error, similar to that of the differential inputs.

7.3.2. Fast CDC for high-speed measurement

As described in Chapter. 6, the proposed CDC demonstrated good performance in terms of resolution, accuracy, thermal stability and power-efficiency. However, in some industrial applications, it is also required that the CDC can perform real-time measurement with low latency. For instance, to compensate for the small vibrations of a critical component, a control loop is usually built that measures the vibration and controls an actuator to compensate for the

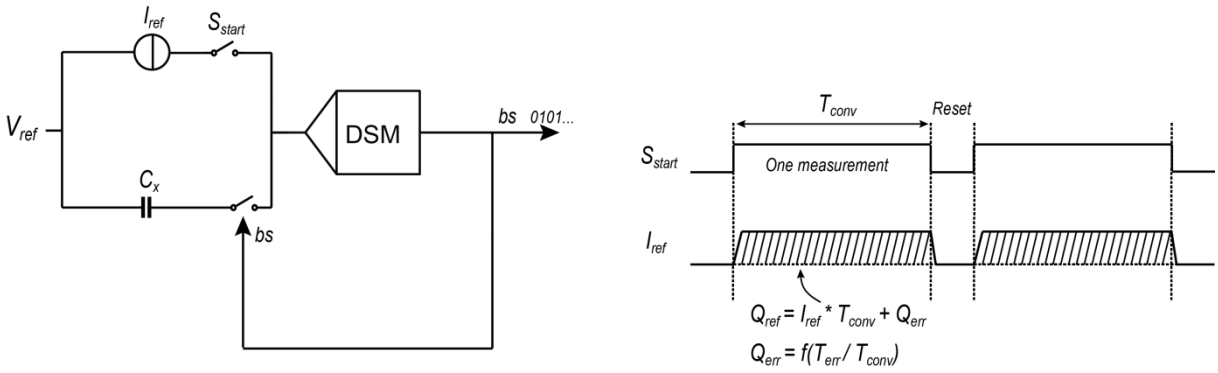

Fig. 7-3. Error due to the finite speed of the switch that turns on the current source

vibration. In such case, a fast measurement of the small vibration/displacement is vital to guarantee the stability of the control loop.

To achieve the same level of performance while greatly improving the measurement speed of the CDC, is challenging. Two major limitations are observed for the proposed CDC:

1). Finite speed of the switches that turns on/off the continuous reference current

As discussed, a continuous reference current is applied during the measurement, which in principle eliminates the impacts of the clock non-idealities. However, the reference current has to be turned off between two measurements (shown in Fig. 7-3). This is to avoid saturating the integrator when the measurement is not performed.

The accurate capacitance measurement of the proposed CDC relays on the accurate timing. Although the crystal oscillator can provide high accuracy and precision (Chapter. 2), the finite speed of the switches that switch on/off the continuous reference current may leads to uncertainties. Moreover, such uncertainty is highly temperature-dependent, which results in higher thermal drift. The maximum speed of the switch is determined by the process, which is not under control of the designer. With minimum size switch in 0.35 μm process, the simulation shows below 100 ns turn-on time of the switch. In principle, using better process (smaller feature size of the transistors) may result in fewer problems; however, smaller feature size of the transistors creates other problems such as lower output impedance thus lower achievable gain of the OTA and higher 1/f noise.

With relatively longer measurement (e.g. a few mili-seconds), this effect is insignificant. However, if a high-speed measurement is desired (e.g. below 100 μs), the impacts of the finite speed of switches can be significant.

2). Finite speed of the resistance-to-current converter (RIC)

Even if the switches can be turned on/off quickly, the finite speed of the RIC results in an extra error. When the RIC is connected to the integrator via switches, it requires some time to settle to a stable level of the reference current. The settling time depends on the bandwidth of the

RIC, which is definitely smaller than that of the minimum size switches. Therefore, it results in deteriorated performance as discussed above, especially when a fast measurement is needed.

Because of the above-mentioned challenges, further research is needed. One possible method is to carefully analyze the error and implement smart clocking schemes that compensate the turn-on error by the turn-off error. Besides, Self-calibration techniques can be incorporated.

Solution I:

A possible solution is to incorporate a fast but less precise CDC for the real-time measurement. With a capacitive-reference-based CDC it is possible to increase the speed, since it is a pure passive network and the impacts of switches are insignificant. Besides, zoom-in can be applied to achieve the same level of measurement resolution in a high speed [1]. In parallel to the fast CDC, a slow but precise CDC based on the proposed topology can be implemented, which periodically calibrates the capacitive-reference of the fast CDC (Fig. 7-4). If continuous measurement is required, two reference capacitors C_{ref} can be implemented so that while one of the C_{ref} is in calibration the other one can be used to maintain the real-time measurement.

However, there are still some challenges for implementing this approach. For instance, such solution would require more complex switch network as well as switching scheme, both of them may create extra errors due to charge-injection, parasitic or mismatches. Therefore, an in-depth error analysis and investigation will be required and possibly some extra precision techniques have to be incorporated.

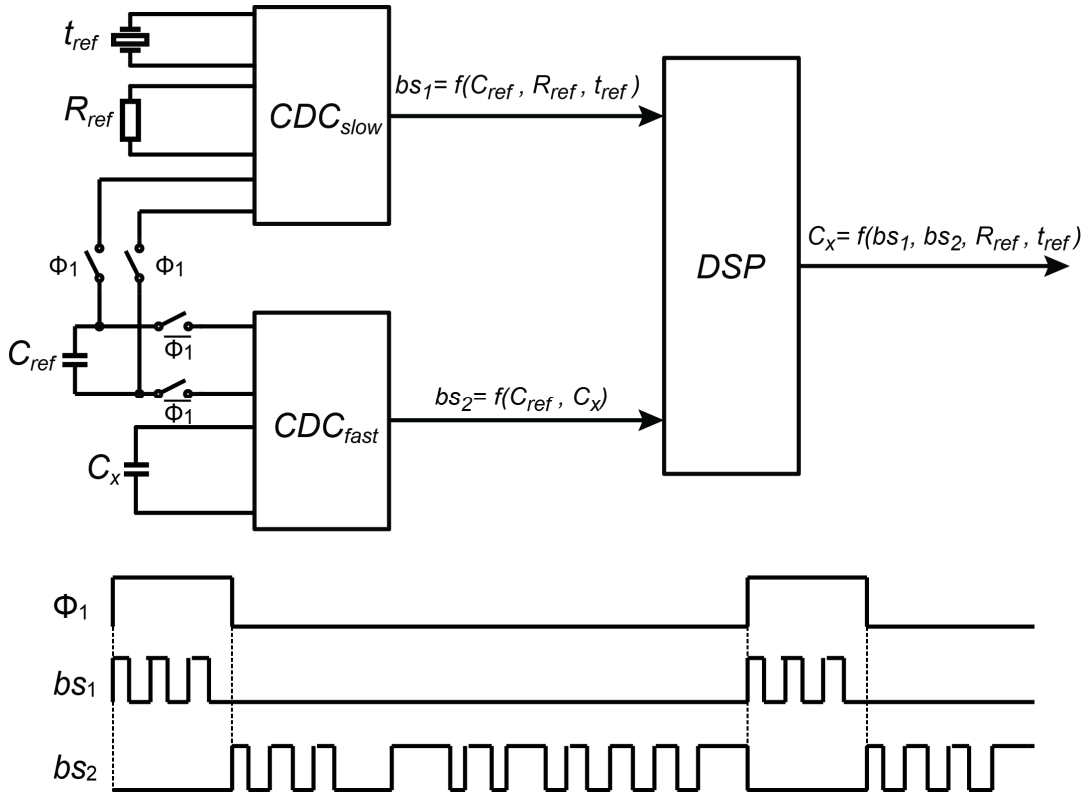

Fig. 7-4. Possible solution I: fast CDC for real-time measurement and slow CDC for calibrating the reference capacitance

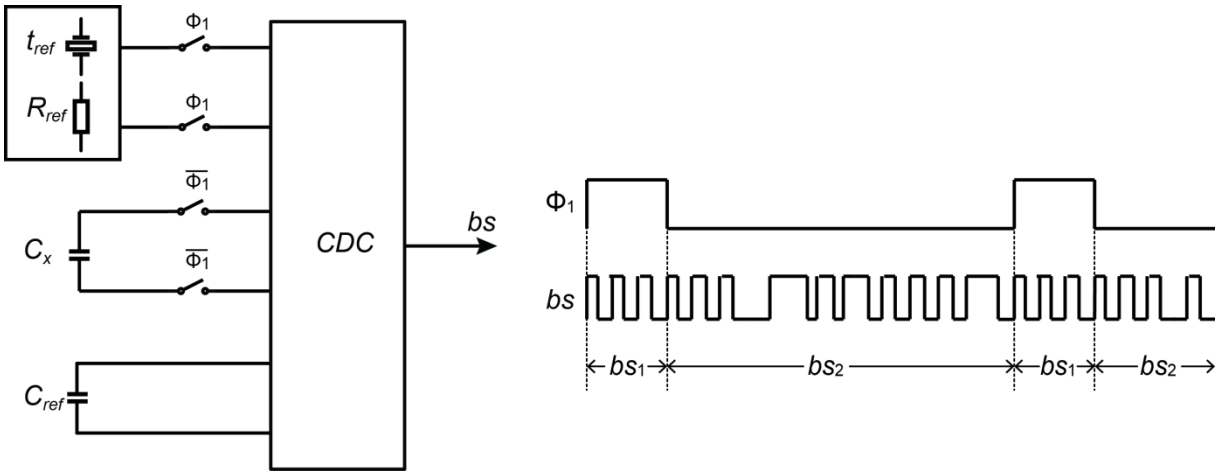

Fig. 7-5. Possible solution II: Time-interleaved CDC with two-phase measurement (Phase 1: calibration of reference capacitance. Phase 2: real-time measurement).

Solution II:

An alternative way is to use the same Delta-sigma modulator for both operations (fast measurement and slow calibration), as shown in Fig. 7-5. In the fast measurement mode, the CDC is configured as a capacitive-referenced CDC, operating in a high speed. In the calibration mode, combination of resistive and time references is used and the CDC is driven by a slower system clock. In this way the sensor capacitor and all the references will always see the same parasitic effects, because they always connect to the same Delta-sigma modulator.

The challenges of this approach are: 1) Lower power-efficiency, because the same modulator has to be adapted to two different operation modes; 2) For the fast CDC large switches are required, but large switches lead to larger charge-injection error for the calibration mode, which may degrade the achievable accuracy and precision.; 3) Continuous measurement is not possible, as the calibration will interrupt the real-time measurement. Therefore, this solution also requires in-depth error analysis and careful design for the required performance.

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Summary

This thesis presents the theory, design and qualification of a precision capacitive sensor system for displacement measurement that require high resolution, high precision and simultaneously, low power consumption. The challenge to achieve the required performance has been taken care at both mechanical domain (sensor head) and electronic domain (interface circuit). To overcome the design challenges, several precision techniques and new concepts have been proposed both at system level and circuit level. Finally, the performance of the proposed system has been qualified. The implemented prototype achieves a medium Figure-of-merit (FoM) related to power efficiency, compared to the state-of-the-art capacitive sensor interface design, while demonstrating a superior thermal stability as well as absolute accuracy.

Chapter 1

Chapter 1 presents the background, motivation and challenges of the research project. It starts with a discussion about the significance of high-precision and low-power capacitive sensors in the displacement/position measurements of high-precision industrial systems. The design of such sensor system usually faces many challenges due to the imperfection of the sensor head as well as the strict precision requirements at a limited power budget of the interface electronics. In order to overcome the challenges, a research methodology to split the challenges into mechanical and electrical domain is proposed.

Chapter 2

Chapter 2 presents a thorough investigation and discussion of high-performance capacitive sensor systems in terms of the sensor head, the interfacing principle and the reference(s) used for the interface circuit.

Capacitive sensors which are used for displacement measurements are generally fitted with parallel flat-plate electrodes. The performance of such sensor is greatly limited by its alignment quality. The miss-alignment leads to large standoff distance (between the sensor plates), which significantly reduces the sensitivity of the sensor, while poses large dynamic range requirements on the succeeding interface circuits. To solve the problem, the use of a thermally-actuated alignment device has been chosen which is capable of aligning the sensor automatically after assembly. To achieve a good alignment speed and high repeatability, an advanced control system is proposed.

To interface a capacitive sensor, many possible circuit architectures have been developed in the past decades. Regarding to the references used, they can be grouped into two types: 1) the unknown capacitance is compared with a reference capacitance; 2) the unknown capacitance is compared with a combination of different references which represent an equivalent reference capacitance. The exact method of comparing the unknown capacitance with the reference(s) can be based on oscillatory circuit (RC/LC oscillators), or Delta-Sigma modulator, or capacitance-to-voltage conversion circuit followed by standard Analog-to-Digital converters

(ADC). Based on an in-depth investigation of state-of-the-art designs it is observed that the high-resolution applications are dominated by interfaces that are based on Delta-Sigma or CFC (capacitance-to-frequency converter) principles. Among these works, capacitive reference is the most used reference component.

For high-precision applications, stability of the capacitance measurement is an important factor, which, unfortunately has been ignored in most of the capacitive sensor designs. The ultimate stability of a capacitive sensor system is limited by the references used for capacitance measurement. For this reason, reference(s) with superior accuracy and stability should be used for such application. But at the same time, the preferred reference(s) must be 'interface-able' by the capacitive sensor interface circuit. A study of all possible references showed that the combination of resistive and frequency references deliver good performance regarding to the stability and absolute accuracy. Besides, this combination of references can be easily interfaced by a charge-balancing Delta-Sigma or CFC-based capacitive sensor interfaces, which are reported to have high resolution in a power-efficient way.

Chapter 3

Chapter 3 presents an auto-alignment mechanism and its control electronics. Alignment is a key challenge when using capacitive sensors in high-precision measurements. The poor alignment accuracy usually poses large pressure on the interface electronics of the sensor, because of the increased requirement of the measurement dynamic range, sensitivity and power-efficiency. To overcome the problem, a new alignment concept based on thermal actuation is proposed in this work. This system has several unique features compared to ordinary alignment systems: 1) it is simple, cheap and robust; 2) due to the proposed special control sequence, the control system can be shut down after alignment, but the aligned position will be maintained stably.

To control the thermal stepper system effectively and in a power-efficient manner, different control algorithms were investigated, including simple open-loop control and various alternatives of closed-loop controls. The pros and cons of different control algorithms were discussed in detail. To validate the investigation, three different controllers were implemented and tested with real thermal stepper device. The measurement proves the validity of the thermal stepper mechanism. Additionally, through the analysis and measurements, a switch-mode multi-level controller is proposed, which takes advantages of both the simple ON/OFF controller and the more complicated PID controller, leading to a balance on complexity and performance.

Chapter 4

Chapter 4 proposes a Delta-Sigma based precision capacitance-to-digital converter (CDC) that compares the unknown capacitance with a combination of time and resistive references to achieve accurate performance of the capacitance-to-digital conversion. Comparing an unknown capacitance to the combination of time and resistive references, however, is not as straightforward as using a capacitive reference. The extra conversion step (converting the non-capacitive references into equivalent capacitance) can introduce additional error that might

deteriorate the overall performance. Therefore, this chapter performs a detailed analysis of the non-idealities that are associated in the proposed CDC.

Based on the analysis, appropriate error budgets have been allocated to each of the building blocks. Next, precision techniques at system level are proposed to minimize the error. For instance, although the capacitor to be measured is single-ended, the CDC employs a fully-differential topology to reduce the charge-injection error of the switched-capacitor (SC) network. Furthermore, system-level chopping is applied so that the mismatch error of the differential inputs is reduced.

Chapter 4 also provides an in-depth noise analysis of the CDC. The outcome of the analysis enables the definition of optimal criteria for selecting the order of the Delta-sigma modulator, defining the required operating cycles and allocating noise budgets to each individual building blocks. In this work, a third-order loop filter with feed-forward compensation is chosen for good balance of thermal noise and quantization noise, which leads to good energy efficiency.

Chapter 5

Chapter 5 describes the detailed circuit implementation of the proposed CDC. With a high precision resistive reference and a crystal-stabilized time reference, an equivalent precision reference capacitance is generated. The proposed CDC thus compares the unknown capacitance with this precision reference capacitance. Ideally, the comparison, or measurement precision is determined by the precision reference capacitance. In practice, the CDC, which does the comparison, introduces additional error. Hence, the building blocks of the CDC have been carefully designed such that their error contribution is made negligible. The building blocks in the proposed CDC include: (OTA-based) integrators, comparator, resistance-to-current converter (RIC), switched-capacitance network, and necessary digital circuitry that generates control clocks and decimate the digital bitstream of the Delta-Sigma modulator.

Based on the system-level analysis of Chapter 4, the error budgets, as well as the specifications (gain, bandwidth, etc) of each individual building block, have been defined. Then, a proper circuit topology has been selected and implemented. To ensure that the error contribution of the individual blocks is within the error budgets, various precision circuit techniques, such as chopping and auto-zeroing, have been implemented at both block level and system level.

Finally, the layouts challenges of the critical components that are important for the CDC performance are carefully addressed. Specifically, layout quality of the first integrator, the RIC, choppers and input switched-capacitor networks directly affect the level of offset and offset drift. Therefore, symmetric layout techniques have been implemented to guarantee the best matching performance of these critical components.

Chapter 6

Chapter 6 discusses the qualification process and setups created for qualification of the precision CDC. To perform the experiments in a reliable way, different measurement strategies are proposed, considering the expected performance and the limitation of the CDC. A number

of qualification tests have been performed, which validated the performance of the designed CDC. The measurements include: noise, thermal stability, long-term stability, transfer characteristic and absolute accuracy.

The measured noise level shows good alignment with the theoretical analysis, which proves the effectiveness of the noise analysis in Chapter. 4. With an operating cycle of 2000 (10.5 ms conversion time), the CDC achieves a resolution of around 55 aF_{rms} within a measurement range of 16 pF (from 6 pF to 22 pF), corresponding to more than 18 bits dynamic range. The thermal stability measurement shows that the thermal drift of the CDC is within 10 ppm/^{O}C for both on-chip and off-chip capacitance measurements. Additionally, the long-term stability test shows that the 1/f noise corner of the CDC is below 200 μHz, ensuring an hour-long stability. Besides, the measurement clearly shows the effectiveness of the implemented choppers. Finally, the transfer characteristic measurement shows an absolute accuracy within ± 25 fF across the entire measurement range (6 pF to 22 pF). By repeating the same measurement for all the chips, it shows a chip-to-chip tolerance smaller than 0.1 %. Comparing with the state-of-the-art CDC design, this work achieves a comparable figure-of-merit (FoM) of 30 pJ/step, but reporting the best stability as well as absolute accuracy.

Samenvatting

Dit proefschrift presenteert theorie, ontwerp en kwalificatie van een precisiesysteem voor het meten van verplaatsing met capacitieve sensoren. Vereisten voor het systeem zijn: hoge resolutie, hoge precisie en tegelijkertijd ook lage vermogensconsumptie. Om aan deze uitdagende eisen te kunnen voldoen is zorg besteed, uitgevoerd in zowel het mechanische domein (sensorkop) als het elektronische domein (interface schakeling). Verschillende precisietechnieken en nieuwe concepten zijn voorgesteld, op zowel systeem- als schakelingniveau. Uiteindelijk is het gedrag van het systeem ook gekwalificeerd. Vergeleken met andere eigentijdse ontwerpen, wordt met het gemaakte prototype enerzijds een gemiddeld cijfer van verdienste (Figure-of-Merit (FoM)) behaald voor wat betreft vermogensefficiëntie, terwijl anderzijds dit prototype uitblinkt door een superieure thermische stabiliteit en absolute nauwkeurigheid.

Hoofdstuk 1

Hoofdstuk 1 beschrijft de achtergronden en de motivatie van het onderzoeksproject: In veel precisie industriële toepassingen is het wenselijk om gebruik van compacte goedkope capacitieve sensorsystemen van precisiemetingen van verplaatsing en positie. Deze sensorsystemen moeten voorzien zijn van een digitale uitgang die geschikt is voor directe koppeling met digitale signaalprocesoren. Echter het bereiken van het gewenste gedrag vormt een grote uitdaging voor het ontwerp van zowel de sensor als de bijbehorende elektronica. Dit komt door enerzijds imperfecties van de sensorkop en anderzijds door gestelde hoge eisen en beperkt vermogensbudget. Daarom is het van wezenlijk belang om de problemen op te lossen op zowel systeemniveau als deelniveau en voor zowel het mechanische als het elektronische deel.

Hoofdstuk 2

Hoofdstuk 2 presenteert een diepgaand onderzoek en bespreking van capacitieve sensorsystemen met hoge precisie. In detail wordt aandacht geschonken aan de sensorkop, het interfaceprincipe, en referenties die worden gebruikt voor de interfaceschakeling.

Capacitieve sensoren die worden gebruikt voor verplaatsingsmetingen zijn veelal uitgerust met parallelle vlakke-plaat elektroden. Het kwaliteit van zulke sensoren hangt nauw samen met de kwaliteit van uitlijning.

Een minder goede uitlijning maakt het nodig om de ruststand tussen de elektroden voldoende groot te maken, hetgeen de gevoeligheid van de sensor aanzienlijk beperkt en bovendien een groter dynamisch bereik van de interfaceschakelingen vereist. Om dit probleem op te lossen is gekozen voor warmte-gedreven uitlijning, die automatisch wordt uitgevoerd na de assemblage van de sensoronderdelen. Teneinde een hoge uitlijnsnelheid en goede herhaalbaarheid te verkrijgen wordt een geavanceerd systeem voorgesteld.

Voor het koppelen van capacitieve sensoren aan elektronische schakelingen zijn de laatste tientallen jaren vele schakelingarchitecturen ontwikkeld. Voor wat betreft gebruikte referenties kunnen we een tweetal groepen onderscheiden: 1) De onbekende capaciteit wordt vergeleken met een referentiecapaciteit; 2) De onbekende capaciteit wordt vergeleken met een combinatie van verschillende referenties die een equivalente referentiecapaciteit representeren. De methode om de onbekende capaciteit te vergelijken met de referenties kan gebaseerd zijn op het gebruik van een oscillatorschakeling (RC/LC oscillatoren), een Delta-Sigma modulator, of een circuit voor Capaciteit-naar-Spanningomzetting gevolgd door een standaard Analoog-Digital Omzetter (ADC). Diepgaand onderzoek van hedendaagse ontwerpen laat zien dat voor toepassingen met hoge resolutie vooral interfaces worden gebruikt die gebaseerd zijn op Delta-Sigma of Capaciteit-naar-Frequentieomzettings- (CFC) principes. Voor wat betreft de toegepaste referentie blijkt een capacitieve referentie het meest gebruikt te zijn.

Voor precisietoepassingen is stabiliteit van de capaciteitsmeting een belangrijke factor, hetgeen helaas bij de meeste ontwerpen van capacitieve sensorsystemen onvoldoende aandacht krijgt. De ultieme stabiliteit van een capacitief sensorsysteem is beperkt door de toegepaste referenties. Om die reden dienen de toegepaste referenties een superieure nauwkeurigheid en stabiliteit te hebben. Tegelijkertijd dienen dergelijke referenties echter geschikt te zijn om gekoppeld te worden met de interfaceschakeling. Een studie van mogelijke referenties laat zien dat de combinatie van een weerstands- met een frequentiereferentie een goed gedrag vertoont ten aanzien van stabiliteit en absolute nauwkeurigheid. Deze combinatie van referenties blijkt bovendien goed koppelbaar te zijn met interfaces gebaseerd op ladingsbalans Delta-Sigma of CFC principes, waarvan bekend is dat ze een hoge resolutie hebben en een hoge vermogensefficiëntie.

Hoofdstuk 3

Hoofdstuk 3 presenteert een auto-uitrichtmechanisme en de bijbehorende regelelektronica. Uitrichting vormt een sleutelprobleem voor het gebruik van capacitieve sensoren voor precisiemetingen. Gewoonlijk vormt slechte nauwkeurigheid van uitrichting een lastig probleem voor de interface-elektronica van een positie-sensor, omdat er dan zwaardere eisen worden gesteld aan het benodigde dynamische meetbereik, gevoeligheid en vermogens efficiëntie. Om dit probleem op te lossen wordt in dit werk een nieuw concept geïntroduceerd dat gebaseerd is op thermische aandrijving. In vergelijking met gewone uitrichtsystemen heeft dit systeem verschillende unieke voordelen: 1) Het is simpel, goedkoop en robuust; 2) door de voorgestelde speciale volgorde van regeling, kan het systeem na het uitrichten worden uitgeschakeld, terwijl de uitgericht positie op een stabiele manier blijft bestaan.

Om het thermische stappersysteem op effectieve en vermogensefficiënte wijze te kunnen regelen, zijn verschillende algoritmes onderzocht, inclusief eenvoudige open-lus regeling, en verschillende varianten van gesloten-lus regeling. De voor-en nadelen van de verschillende regelalgoritmen worden tot in detail besproken. Ter validatie van het onderzoeksresultaat, zijn drie verschillende regelsystemen uitgevoerd en getest met een echte thermische stapper. De meetresultaten bevestigen de goede werking van het thermisch stapper-mechanisme. Gebruikmakend van analyse en metingen, wordt in aanvulling hierop een geschakelde multi-

level regelaar voorgesteld, die het voordeel heeft van zowel een eenvoudige AAN/UIT regelaar als dat van een meer gecompliceerde PID regelaar, wat een goede balans geeft tussen eenvoud en prestatie.

Hoofdstuk 4

In hoofdstuk 4 wordt een Capaciteit-Digitaalomzetter (CDC) voorgesteld die gebaseerd is op Delta-Sigmamodulatie en waarin een onbekende capaciteit wordt vergeleken met een combinatie van een tijd- en weerstandreferentie, teneinde een hoge nauwkeurigheid te bereiken. In vergelijking met het gebruik van een capaciteitsreferentie lijkt vergelijking van een onbekende capaciteit met tijd- en weerstandreferenties minder voor de hand liggend. De extra conversiestap (de conversie van een niet-capacitieve referentie naar een equivalente capaciteit) kan extra fouten veroorzaken die de prestaties van het geheel kunnen verslechteren. Daarom geeft dit hoofdstuk een gedetailleerde analyse van alle niet-idealiteiten die verband houden met de voorgestelde CDC.

Gebaseerd op de analyse worden geschikte foutbudgetten toegewezen aan elk van de bouwstenen. Vervolgens worden precisietechnieken voorgesteld om de fouten te minimaliseren. Bijvoorbeeld: hoewel de te meten capaciteit enkelzijdig is, is de topologie van de CDC volledig differentieel. Hierdoor worden fouten die zijn veroorzaakt door ladingsinjectie van het switched-capacitornetwerk gereduceerd. Verder wordt chopping uitgevoerd op systeemniveau, waardoor mismatchfouten worden verminderd.

Hoofdstuk 4 verschaft ook een diepteanalyse van de ruisaspecten van de CDC. De uitkomsten van deze analyse maken het mogelijk om: optimale criteria voor de selectie van de orde van de Delta-sigma modulator aan te geven, om het benodigde aantal bewerkingscycli te bepalen, en om ruisbudgetten toe te wijzen aan de verschillende bouwstenen. In dit werk wordt gekozen voor een derde-orde lusfilter met feedforward compensatie. Vanwege de goede balans tussen thermische en kwantisatie-ruis, leidt dit tot een goede energie-efficiëntie.

Hoofdstuk 5

Hoofdstuk 5 beschrijft de details van de uitgevoerde schakeling voor de CDC. Met een precisie weerstandsreferentie en een kristal-gestabiliseerde tijdreferentie wordt een equivalente capaciteit opgewekt. De voorgestelde CDC vergelijkt op deze manier de onbekende capaciteit met een (equivalente) precisie-referentiecapaciteit. In het ideale geval wordt de precisie van de vergelijking of meting bepaald door de precisie-referentiecapaciteit. In de praktijk blijkt de CDC die de vergelijking uitvoert een extra fout te veroorzaken. Vandaar dat de bouwstenen van de CDC met zorg zijn ontworpen, zodat hun foutbijdragen verwaarloosbaar zijn. De bouwblokken van de voorgestelde CDC omvatten: OTA-gebaseerde integratoren, een comparator, een Weerstand-Stroomomzetter, een switched-capacitor netwerk, en digitale schakelingen die nodig zijn voor het opwekken van kloksignalen en decimering van de digitale bitstream van de Delta-Sigmamodulator.

Gebaseerd op de analyse op systeemniveau van hoofdstuk 4, zijn foutbudgetten en de specificaties (versterkingsfactor, bandbreedte, enz.) van ieder bouwblok vastgesteld.

Vervolgens is een geschikte schakelingtopologie uitgezocht en uitgevoerd. Om er zeker van te zijn dat de foutbijdrage van ieder van de blokken binnen het vastgestelde budget is, zijn er verschillende precisie schakelingtechnieken, zoals chopping en auto-zeroing, toegepast op zowel blok- als systeemniveau.

Voor zover van belang voor de CDC prestaties, zijn ook uitdagingen op het gebied van layout van kritische componenten zorgvuldig aangepakt. Met name de layout kwaliteit van de eerste integrator, de RIC, choppers, en switched-capacitor netwerken aan de ingang hebben rechtstreeks invloed op het niveau van offset en offset drift. Daarom zijn technieken voor een symmetrische layout gebruikt, teneinde goede gelijkheid van kritische componenten te kunnen garanderen.

Hoofdstuk 6

Hoofdstuk 6 bespreekt het kwalificatieproces en de opstellingen die zijn gemaakt voor kwalificatie van de precisie-CDC. Om de experimenten op een betrouwbare manier te kunnen uitvoeren worden verschillende strategieën voorgesteld, waarbij wordt gelet op te verwachten kwaliteit en mogelijke beperkingen van de CDC. De uitgevoerde kwalificatietesten bevestigen de kwaliteiten van de CDC. De metingen betreffen: ruis, thermische stabiliteit, lange-duurstabiliteit, de overdrachtskarakteristiek, en de absolute nauwkeurigheid.

Het gemeten ruisniveau laat goede overeenkomst zien met de uitkomst van de theoretische analyse, hetgeen tevens de doeltreffendheid van de analyse in hoofdstuk 4 bevestigt. Met een werkbereik van 2000 (10.5 ms conversietijd), bereikt de CDC een resolutie van ongeveer 55 aF_{rms} binnen een meetbereik van 16 pF (van 6 pF tot 22 pF), hetgeen correspondeert met een dynamisch bereik van meer dan 18 bits. Metingen van de thermische stabiliteit laten zien dat de thermische drift van de CDC minder is dan 10 ppm/^{o}C voor zowel on-chip als off-chip capaciteitsmetingen. Verder laten testen van de lange-termijnstabiliteit zien dat de 1/f ruishoek van de CDC minder dan 200 μHz bedraagt, hetgeen een urenlange stabiliteit verzekert. Ook tonen de metingen aan, dat de uitgevoerde choppers doeltreffend werken. Tenslotte laat de meting van de overdrachtskarakteristiek zien dat de absolute nauwkeurigheid beter is dan ± 25 fF over het gehele meetbereik (6 pF tot 22 pF). Herhaling van dezelfde metingen voor alle chips laat zien dan de tolerantie van chip-tot-chip beter is dan 0.1%. In vergelijking met andere eigentijdse CDC ontwerpen, behaalt onze CDC een vergelijkbaar cijfer van verdienste (FOM) ter grootte van 30 pJ/stap, maar tegelijkertijd ook de beste stabiliteit en absolute nauwkeurigheid.

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Publications

Journal Publication:

1. **R. Yang**, O. van de Ven, Sha Xia, S. Nihtianov, "Autonomous Self-Aligning and Self-Calibrating Capacitive Sensor System for Displacement Measurement in Inaccessible Industrial Environments", Submitted to *Transaction Industrial Electronics*.

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About the Author

Ruimin Yang was born in Yuxi, Yunnan Province, China, in 1985. He received the B.Sc. degree in Electronic Science and Technology from Southeast University, Nanjing, China, in 2007. After that, he started the M.Sc. study in microelectronics at Delft University of Technology, Delft, The Netherlands, in September 2007. He received his M.Sc. degree from TU Delft in October 2009 and continued to pursue his Ph.D degree in Elecctronic Instrumentation Laboratory. The subject of his research is high-precision and low-power capacitive sensor system for industrial applications.

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