Series Operation of Switched-mode Power Supplies for LED Lighting

Master of Science Thesis

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July, 2015

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This thesis work has been carried out in the group of Advanced Development Europe, Philips Lighting in the period of October 2014 to June 2015, and submitted as partial fulfillment of the degree of:

Master of Science in Electrical Engineering

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Abstract

Solid-state LED lighting, as the fourth-generation lighting technology, has drawn great popularity due to its long lifetime, high luminous efficacy, high energy efficiency and sustainability. Technical advancement and rapid cost-down in LED technology bring entirely new possibilities in lighting applications and stimulate a significant transition from conventional lighting in the global lighting market.

Considering huge amount of conventional lighting fixtures in current use, a complete modification for LED lighting at system level can be costly, complex and time-consuming. Efforts are therefore made to develop retrofit LED lamps that can directly fit into the existing lighting systems with electrical compatibility. However, a typical multi-lamp luminaire for 2ft linear fluorescent lamps usually contains one or several branches where two lamps are connected in series to a common electro-magnetic ballast of that branch. The unique wiring scheme forms an input-series system and inevitably causes stability problems with conventional LED drivers, which are usually based on closed-loop switched-mode power supplies. Besides, operation conditions are flexible for 2ft retrofit LED tubes: they are randomly installed in either the two-lamp or one-lamp branch in the luminaire and can be connected with or without electro-magnetic ballast, which accordingly addresses additional design requirements.

This thesis work aims at developing an electro-magnetic ballast compatible LED driver for 2ft LED retrofit tube applications. A modulated peak current controlled self-oscillating buck-boost converter is proposed to achieve a positive dynamic input resistance, thereby realizing stable series operation. The validation can be generalized to other input-series systems. On the basis of proposed approach, a complete designing process of the LED driver, which is electrically compatible with the existing fluorescent lighting fixture, is presented. Key points of designing to fulfill all application requirements (include automatic mode selection) are discussed in detail. Two prototypes provide experimental results to verify the effectiveness of the proposed design.

Acknowledgement

First and foremost, I would like to express my deepest gratitude to my supervisors, Dr. Haimin Tao, who helped me without reservation throughout the past year and gave professional guidance on my thesis work, and Dr. Jelena Popovic, whose comments and suggestions were highly appreciated in formalizing the thesis. This thesis couldn't have been finished without their help and efforts.

My sincere thanks also go to Christiaan van Dijk, Patrick Zijlstra, Yi Wang and all other colleagues in Philips Lighting, who were always open to questions and discussions, and to Dik Pardijs, who decided to 'employ' me and generously gave me the opportunity to be in this cheerful team.

I greatly appreciate Delft Energy Initiative for their kindness in granting *Delft Excellence Scholarship* throughout my master's study.

Cheers to these coolest years ever in my life! I had great fun to have you guys around, Mingyao, Si, Di and Shining. My heartfelt thanks to my friends Rui and Zhenglin, with whom I shared the best years. It is too good to be true that we are still there for each other across the distance of oceans and continents. I would like to thank my boyfriend, Chongwen, for sharing every bitter or sweet moment with me, as he always does. He makes every day count.

This thesis is dedicated to my parents, who are the lifelong inspiration deep inside my heart.

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List of Abbreviations

LED: Light-emitting Diode

HID: High-intensity Discharge

SMPS: Switched-mode Power Supply

CRI: Color Rendering Index

EM: Electro-magnetic

ISOP: Input-series Output-parallel

EMI: Electromagnetic Interference

IVS: Input Voltage Sharing

OCS: Output Current Sharing

PFC: Power Factor Correction

SCM: Sensor-less Current Mode

RCC: Ringing Choke Converter (Self-oscillating Converter)

CCM: Continuous Conduction Mode

DCM: Discontinuous Conduction Mode

BCM: Boundary Conduction Mode

BJT: Bipolar Junction Transistor

Chapter 1 Introduction

1.1 LED Lighting Development

Since the late 18th century when electric light sources were first introduced and commercialized, there have been several milestones in lighting technology development.

Invented in early 19th century, incandescent light bulb is regarded as the first-generation electric light sources. An incandescent light bulb produces light when a wire filament is heated to glow by means of electrical current. However, 90% or even more power consumption of a typical incandescent bulb is converted into heat instead of visible light, which makes it less energy-efficient. Therefore, it is gradually phasing out and being replaced by other light sources such as compact fluorescent lamps.

A fluorescent lamp, the second generation of electric light source, basically consists of a tube filled with low-pressure gas, electromagnetic or electronic ballast and a starter. A basic diagram is shown in Figure 1-1. With the help of starter, the ballast generates a voltage over the terminals when AC voltage is applied, which is high enough to start up the lamp. After ignition, the ballast limits the current to an adequate level.

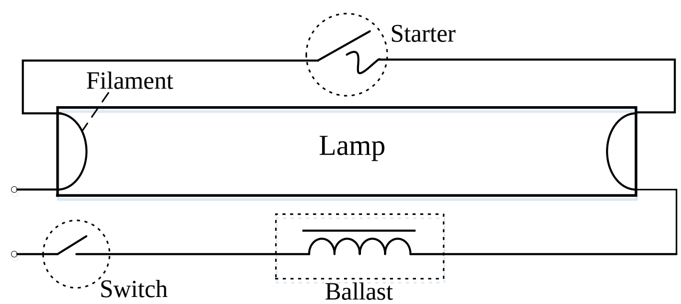


Figure 1-1 A fluorescent lamp diagram

The third generation light source, high-intensity discharge (HID) lamp, produces light by forming an electric arc between tungsten electrodes. HID lamps are favorable in applications that require high light intensity over large areas, such as warehouses, stadiums and public areas.

As the fourth-generation light sources, solid-state LEDs compete with the conventional light sources and show merits in long lifetime, high luminous efficacy, energy efficiency and sustainability. The earliest visible LED is demonstrated in 1962 [1], which is made of $GaAsP$ and emits red light. After that, more III-V compound semiconductors are used to fabricate LEDs capable of emitting various colors [2]. From 1990s, a new generation of high power, high-brightness blue, green and yellow LEDs on either $InGaN$ or $InGaN/AlGaN$ were reported in [3] and [4]. High-brightness blue LEDs become the core of today's white LED technology for general lighting purpose.

LED lamps utilize the LEDs as the light emitting components and are assembled in similar shapes with the conventional lamps for various lighting fixtures. There have been LED lamps which are designed to be direct drop-in replacement for incandescent or fluorescent lamps for different lighting purposes, covering from LED bulbs, LED spotlights, LED strips to tube-LEDs in Figure 1-2.

(a) LED bulb

(b) LED spotlight

(c) LED strip

(d) Tube-LED

Figure 1-2 LED lighting products by *Philips*

In general, an LED lamp consists of an LED array as the light emitting component and an LED driver to regulate DC current through the LEDs. The power rating of a single LED is usually limited and therefore multiple LEDs are arranged in an array for sufficient power output. Electrically, those LEDs can be connected in series or parallel depending on applications. Since most LEDs cannot emit light in every direction, the spatial arrangement should also be considered for light spread. An appropriate LED driver design is essential to convert the AC current to a constant DC current to drive off-line LEDs. The driver can be a linear power source or a switched-mode power supply (SMPS) as long as it provides a constant DC current. Figure 1-3 demonstrates a typical disassembled linear LED lamp with LED array and a driver board.

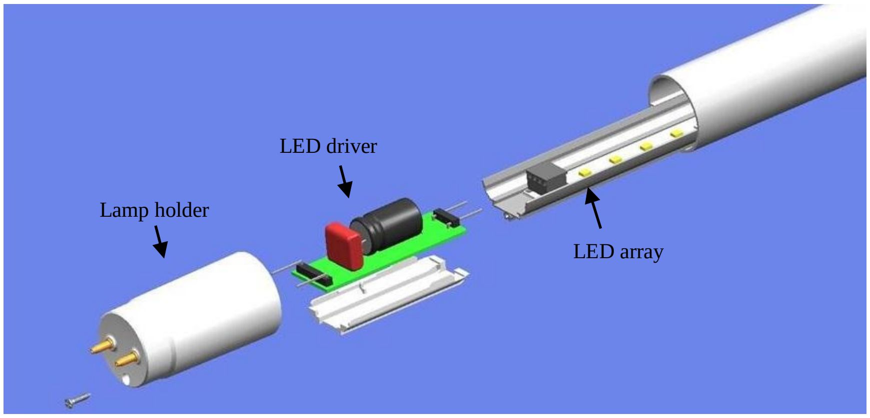


Figure 1-3 Disassembled LED tube with driver circuit board

LED manufacturers are steadily pushing up the luminous efficacy in recent years to compete with conventional light sources. For a fluorescent lamp, the luminous efficacy ranges from several lumens per watt (lm/W) to approximately 100lm/W depending on applications. In 2006, the milestone figure of 100lm/W for white LEDs was achieved at a forward current of 20mA [5]. Later in 2009, LED manufacturer *Cree* developed 186lm/W power LED at 350mA [6]. In 2011, *Osram* demonstrated a 200lm/W red LED at 40mA with color rendering index (CRI)>98 [7]. The newly reported tetra-chromatic phosphor-coated white LEDs in 2014 achieved >311.2lm/W for CRI>90, and >280.7lm/W for CRI>98 [8].Figure 1-4 plots the roadmap of commercial “warm white” LED products (2700 to 4100K) in terms of luminous efficacy. A projection is made for LED lighting technology based on compiled data by US. Dep. Of Energy [9].

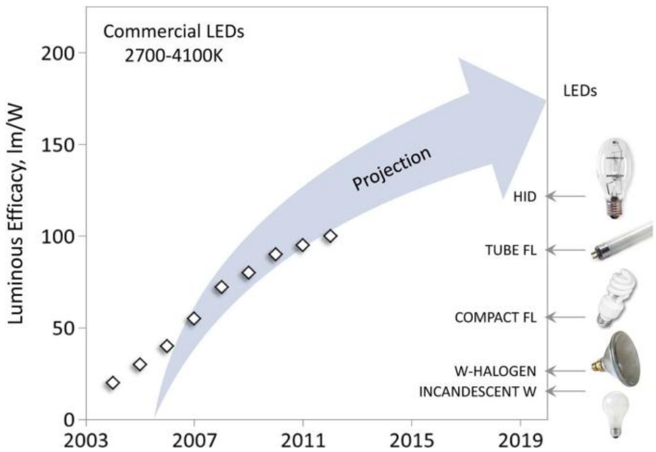


Figure 1-4 Luminous efficacy of different lighting technologies [9]

Among different light sources that are mentioned, fluorescent lamps have been the dominant light sources in various sectors of household, commercial and industrial lighting for their overall performance. However there are several drawbacks to mention. Fluorescent lamps are sensitive to power supply disturbances and consequently generate visible flickering when operated with an electro-magnetic ballast. Frequent switching will speed up its ageing process because each start cycle erodes the emission material on the cathode. This technology also suffers from dimming difficulties, non-ideal spectral power distribution and harmonic issues [10]. Besides, fluorescent lamps usually contain mercury, which is not environmentally friendly.

At the same time, technical advancement in LED technology brings entirely new possibilities in lighting applications. LED lighting is becoming affordable and thus gradually stimulates a transition from conventional lighting to LED lighting. In 2013, the *McKinsey*'s lighting market report [11] predicts the global LED's market share will increase to 60% of the overall lighting market by 2020.

All the facts above facilitate the transition from fluorescent lighting to LED lighting. Considering the huge amount of fluorescent lighting fixtures in current use, a complete modification for LED lighting at system level can be costly, complex and also time-consuming. As a result, a lot of efforts are made to develop retrofit LED lamps that are compatible with the existing lighting system. For instance, reference [10] assesses the feasibility of retrofitting and emphasizes the impact on power system. A novel driving technique which enables LED lamps to operate with electronic ballast is proposed and verified with a 36W experimental prototype [12]. In commercialization, several manufactures such as *Philips* and *Osram*, have already launched their LED lamps in the market as a drop-in replacement for fluorescent lamps.

1.2 Research Background

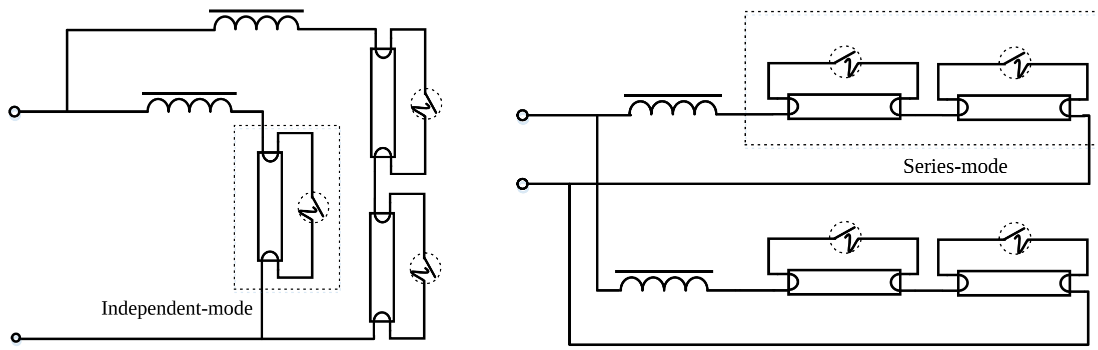
Nowadays linear fluorescent lamps, also referred as fluorescent tubes, of different standard lengths are still widely used in general lighting sector. Required by the basic operation principle, a ballast needs to be installed in series with the tube in a fluorescent lighting fixture. There are basically two kinds of ballast: electro-magnetic (EM) ballast and electronic ballast.

(a) Electro-magnetic ballast (b) Electronic ballast

Figure 1-5 Ballast for fluorescent lighting

Linear fluorescent lamps of 4ft and 5ft length usually work with an independent ballast and multiple lamps are paralleled. The same configuration is also valid for 2ft fluorescent lamps. However, it happens very often that two 2ft lamps are connected in series and work with a common ballast of that branch, forming an **input-series system**. This series connection is often adopted to reduce system cost, especially in multi-lamp luminaire.

Figure 1-6 below shows the popular three-lamp and four-lamp lighting fixtures for 2ft fluorescent tubes. Some branches in the luminaire have two lamps and a shared ballast while others have one lamp with an individual ballast. Hereafter, these two operation modes are referred to as **series-mode** and **independent-mode**, respectively.



(a) Three-lamp fixture

(b) Four-lamp fixture

Figure 1-6 Popular lighting fixtures for 2ft fluorescent lamps

LED lamps are expected to fit in the existing fluorescent lighting fixtures without or with little structure modification both physically and electrically. The LED tube lamps, as an alternative for fluorescent tubes, physically share the same dimensions and connections as fluorescent lamps. Therefore they can easily fit in such fixtures. Electrically, however, LED retrofit lamps will face the following issues.

(1) Stable series-mode operation

LED retrofit lamps based on conventional closed-loop design will run into trouble when two lamps are connected in series. In practice, this input-series system is considered stable if both lamps operate properly and deliver sufficient amount of light even after a disturbance occurs. Since most LED drivers are based on conventional closed-loop switched-mode power supplies, the series operation is technically challenging due to its negative dynamic input resistance. System instability is observed frequently in practice: it is very likely that only one lamp in the system will still work after a disturbance. Therefore, an appropriate driver design for LED retrofit lamps should realize stable series operation as a priority.

(2) EM ballast and direct mains compatibility

The retrofit lamp should be both electro-magnetic ballast compatible and direct mains compatible. As the earliest ballast to work with fluorescent lamps, EM ballast is still widely in use for its simple structure and long lifetime. It is desirable that the drivers are compatible with EM ballast when mounted in the existing luminaire. However, users may also require additional rewiring to remove or bypass the installed ballast. In this case, the driver will be connected to the mains directly.

(3) Automatic detection and mode-selection function

It is also worth mentioning that the LED retrofit lamp will be randomly installed in the luminaire and operate in either series mode or independent mode. It is thus required that the driver is capable of detecting different operating modes automatically and regulating the LED current to a same level regardless of the operation mode.

A retrofit LED lamp should be designed accordingly to fulfill these application requirements and thus can electrically fit into the existing fluorescent lighting systems.

1.3 Research Objectives

The unique application conditions of 2ft retrofit LED tube lamps put new design requirements on the LED driver, which will be investigated in this research work. The system to be investigated is simplified and described in Figure 1-7.

A complete system consists of an electro-magnetic ballast and two series connected LED drivers with individual LED load. However, the system configuration can be quite flexible since the components in dotted boxes, including the electro-magnetic ballast and a second driver, are both optional and can be removed. If the second driver is not present, the system has a single driver operating in independent mode. System input remains the same in any possible system configuration.

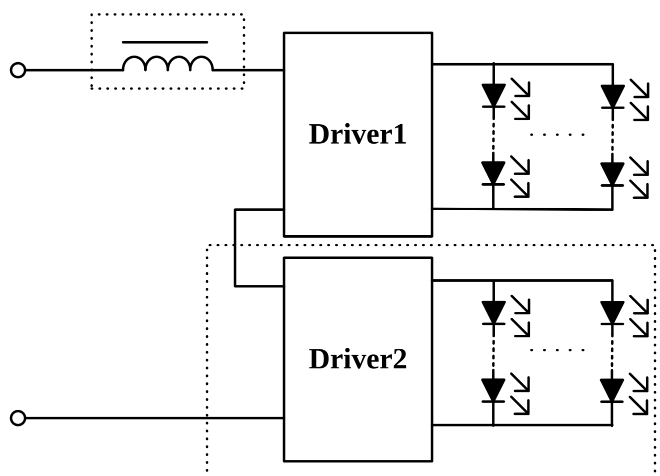


Figure 1-7 System schematic

The project aims at developing an electro-magnetic ballast compatible LED driver for 2ft LED retrofit tubes, which can operate in both independent and series mode with guaranteed stability. To achieve this goal, the following research sub-objectives are formulated.

(1) Investigate and evaluate suitable driver topology and control strategy for stable series operation

First of all, various possible circuit topologies and control strategies, including closed-loop and open-loop solutions, will be investigated and evaluated to realize stable series operation as a top concern. In presence of reasonable component tolerances, the system should still stably operate and result in acceptable system unbalance. The proposed approach has to be generally valid for an input-series system design. Prototypes implemented with the proposed control approach will be built to demonstrate its validity in principle.

(2) Design an EM ballast compatible LED driver for 2ft LED tubes and demonstrate functionality with prototypes

On basis of the outcome of (1), a complete driver will be designed for retrofit LED lighting applications. The prototypes will be electrically compatible with the existing lighting fixtures and meet all the application requirements stated in section 1.2, including EM ballast and mains compatibility, automatic mode detection and selection function. The design specifications are briefly summarized in Table 1-1.

Input voltage/V	$196 \leq V_{in,rms} \leq 264$, 50Hz
Driver output current/mA	72
Driver input power/W	7.5
Driver efficiency/%	>85
THD/%	<30

Table 1-1 Design specifications: 2ft retrofit LED driver

1.4 Thesis Outline

The thesis is organized in 6 chapters. The contents of each chapter are briefly outlined as follows.

Chapter 2 analyzes the stability of input-series system without specially designed control loop, and presents a literature review of related work on input-series output-parallel (ISOP) DC/DC modular converter and modular LED drivers with independent outputs. The control methods are studied and evaluated, on basis of which an open-loop approach is selected for further exploration.

Chapter 3 proposes a novel control strategy – modulated peak current control to realize stable series operation based on a boundary conduction mode buck-boost converter. The control equation and stability condition that are necessary for stable series operation are discussed in detail. In Chapter 4, the proposed approach is implemented with discrete component and validated in both simulations and experiments. System sensitivity to component tolerance is also checked upon requirements.

Chapter 5 presents the driver design procedure for 2ft LED tubes application based on the proposed control strategy. Used as a direct replacement, the driver is electrically compatible with the existing fluorescent lighting fixtures and meet all relevant requirements. The design is first verified with *LTSpice* simulations. Two prototypes are built accordingly to illustrate the functionality with experimental evidence. The experimental results in four distinct operation conditions are presented to evaluate driver performance.

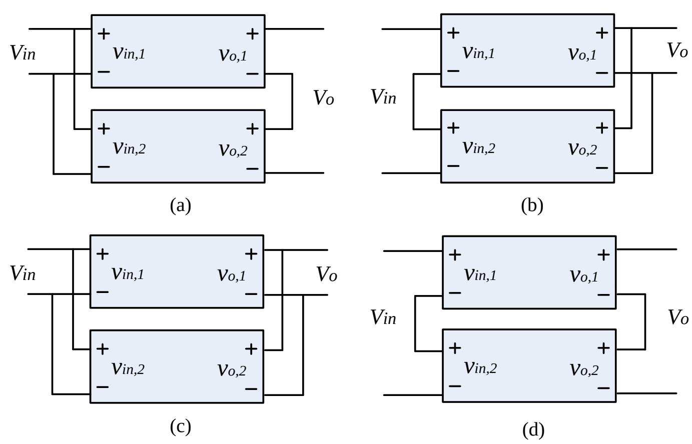
The last chapter gives a conclusion of the research work and recommendations on future work.

Chapter 2 Stability Analysis and Control Strategies Evaluation

This chapter first analyzes the stability of an input-series connected system based on different converter input characteristics. A conclusion for stability is reached as guidance for future design. It also presents the literature review on relevant control strategies that are employed by input-series output-parallel (ISOP) systems and modular LED drivers with independent outputs. Finally, different control strategies are evaluated for current application.

2.1 Input-Series System

The input-series concept is already widely discussed in modular DC/DC converter design, in which low voltage, low power DC/DC building blocks are connected in series or parallel to reduce either current or voltage stress on the converters [13].



(a) Input parallel and output series (b) Input series and output parallel
(c) Input parallel and output parallel (d) Input series and output series

Figure 2-1 Four possible connections of DC/DC modular converter

Of the four major combinations, the input-series output-parallel (ISOP) converter shares several critical features with the series connected two-lamp system in the present project. First of all, the inputs of two or more modular converters are connected in series. Secondly, for full modularization, each converter has its own power stage and controller and should be capable of stand-alone operation [14]. Since the output current needs to be shared equally among the modules, each converter is still regulated to be a constant power sink.

The modular concept is also implemented in LED drivers, with reference to the discussion of ISOP systems [15]. A modular LED driver is suitable for applications with a great amount of LEDs. In this case, a typical solution places the LEDs in a series-parallel connection but requires extra efforts on current sharing among the strings. A much easier way is to connect all LEDs in series with guaranteed equal forward current, especially when operating at a high input voltage. However, it can be risky in that one LED failure will cause the overall system to fail. The modular LED driver, as an alternative, separates the load into smaller groups with individual driving circuit. Thus, the failing module can be bypassed to avoid broader influence.

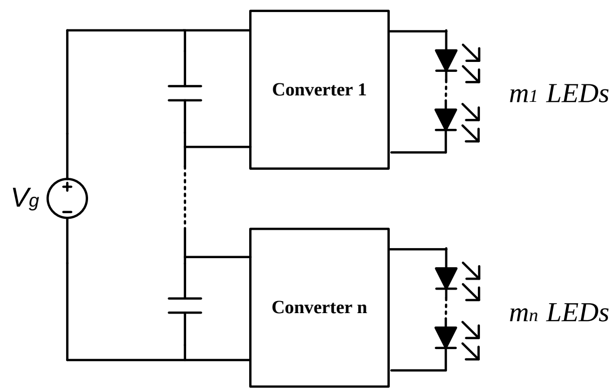


Figure 2-2 An LED application based on series-input converter modules

The system shown in Figure 2-2 is a series-input converter modules based LED application [15]. It also consists of several converters connected in series at the input. Instead of connecting in parallel at the output, however, each converter drives an independent LED string that makes a significant difference from the regular ISOP system.

In this chapter, control strategies that are already validated in ISOP systems and modular LED drivers will be reviewed and summarized in order to provide design references.

2.2 Stability of an Input-Series System

When two regular switched-mode power supplies are connected in series at the input, both of them are loading the power supply simultaneously and will impose inevitable impact on each other. Without any precaution taken, the system may suffer from stability problems. The stability issue in an input-series system with independent outputs is addressed in this section.

An input-series connected system is considered stable if input voltage is always shared by two constituent modules with a constant ratio and no voltage runaway phenomenon happens after a disturbance occurs.

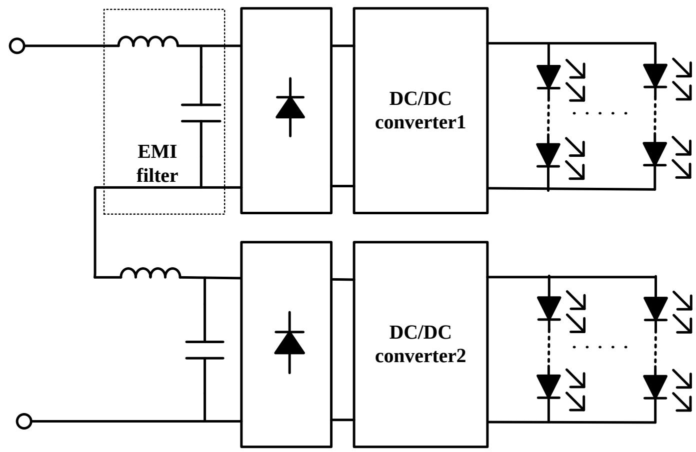


Figure 2-3 Input-series system schematic

The schematic of the input-series system is re-drawn from Figure 1-7 with details, each driver including an input EMI filter, a rectifier bridge and a DC/DC converter. The EM ballast is temporarily removed from the circuit. The input EMI filter is chosen to be an LC filter for analysis simplicity.

2.2.1 Input Voltage Sharing

The concept of **input voltage sharing** (IVS) has been extensively addressed as prerequisite of stability in an ISOP system. In duality, the concept of **output current sharing** (OCS) is also discussed in ISOP system.

To ensure proper operation of an ISOP system, all the constituent modules should work in equilibrium; that is both input voltage and output current are evenly shared among the modules. In steady state, two sets of parameters in all modules are naturally made equal by the connection: converter input currents and the output voltages. Besides, the average current through input capacitor remains zero. Assume the converters are lossless.

$$V_{in,i}\, I_{in,i} = V_{o,i} I_{o,i} \quad i = 1,2\ \ldots \qquad \text{Eq. 2- 1}$$

Mathematically, when either IVS or OCS is achieved with control efforts, the other condition will be automatically ensured by power conservation. However, the following example illustrates that it is critical to achieve IVS instead of OCS in practical implementation.

The simulation waveform in Figure 2-4 shows the divergence of input voltages in an input-series connected system with only dedicated output current sharing control. After a perturbation to $V_{in,1}$ at $t = 1ms$, the input voltages $V_{in,1}$ and $V_{in,2}$ gradually diverge from each other even though the output currents are still regulated to be the same. Converter 1 keeps taking over more voltage and may end up in destruction due to over-voltage. After a finite period of time, $V_{in,2}$ will be too low to maintain the output current for converter 2.

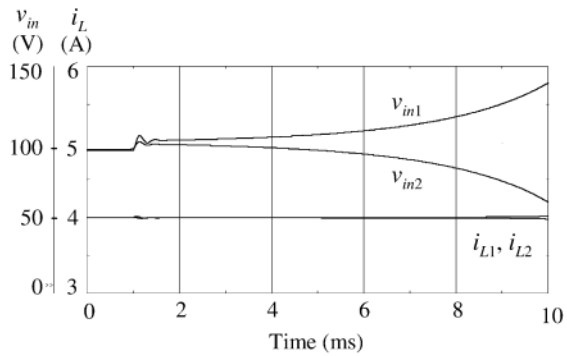


Figure 2-4 Divergence of input voltage: constant power load [13]

The reason is briefly explained: if OCS is guaranteed, all the converter modules behave as constant power sink. The inherent negative dynamic input resistance feature leads to a positive feedback process when a small perturbation is imposed at the converter input. A runaway effect will finally break the system equilibrium. A more detailed explanation will be present in section 2.2.3.

The simulation clearly shows that controlling at the output side is useless in practice. Although the output current is shared among the modules, the input voltages still drift away from each other. When IVS is realized, on the contrary, each converter behaves as a constant power source to the same load, resulting in a stable system. Therefore, any control strategy aiming at IVS will be stable.

It is also critical to achieve IVS in modular LED drivers. While the outputs of an ISOP system are paralleled to have naturally equal voltage, a modular LED driver has several independent outputs that drive floating LED strings. Considering a reasonable tolerance in LED forward voltage, the individual output power P_i will differ from each other. Thus, the primary control objective should be the proportionally distribution of line voltage [15]. That is,

$$\frac{V_{in,i}}{V_{in,j}} = \frac{P_i}{P_j}, i,j = 1,2 \dots \dots N \qquad \text{Eq. 2- 2}$$

When the output currents are regulated to be equal (for the same current-rating LED load), the equation to be satisfied becomes,

$$\frac{V_{in,i}}{V_{in,j}} = \frac{V_{o,i}}{V_{o,j}}, i,j = 1,2 \dots \dots N \qquad \text{Eq. 2- 3}$$

To conclude, a proper input voltage sharing is always required for stable operation of an input-series connected system.

2.2.2 Input Characteristics

At system level, the drivers are acting as two series-connected loads and the detailed circuit implementation will become invisible to the power supply. Their input characteristics, instead, are of greater concern for stability analysis.

Various control methods have been proposed to regulate a single switched-mode power supply in order to achieve the required circuit functions. For example, current feedback control is usually adopted in LED drivers to maintain a constant driving current for LED load, while in case of a voltage supply, the output voltage is tightly regulated via voltage mode control instead. Some power factor correction (PFC) converters are controlled with a constant on-time, therefore obtaining a good power factor.

In general, the controlling part of a switched-mode power supply can be implemented either in an open-loop or a closed-loop. The open-loop approach applies a pre-programmed control signal of the nominal operating conditions to the circuit. The converter has a simple structure but is vulnerable to external disturbance and component tolerances. Closed-loop control has better performance when the output is tightly regulated, since the real-time circuit information is incorporated to generate the control signals.

As load to the power supply, all switched-mode power supplies can be basically classified into three categories depending on their input characteristics, each category represented by a constant resistance, a constant current or a constant power load. A constant voltage behavior is not realistic under voltage source input, and therefore not included.

The following figure shows the representative input I-V curves of different load categories, excluding where input voltage is too low or too high to maintain regular operation. It should be noted that those non-ideal intervals are not considered in following discussion.

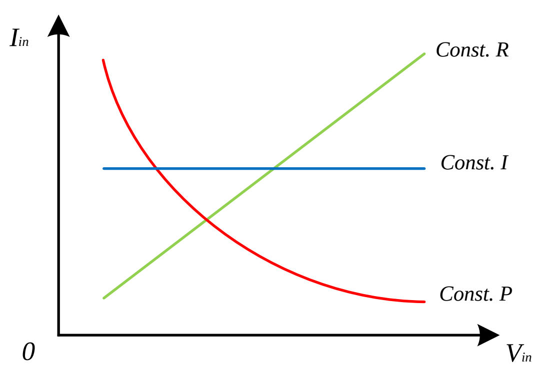


Figure 2-5 Switched-mode power supply input I-V curves

Dynamic input resistance (also called differential resistance or AC resistance) is the ratio of a small change in input voltage to the corresponding change in input current at any operating point. Mathematically it is the derivate of input voltage with regard to input current.

$$r_{in} = \frac{dV_{in}}{dI_{in}} \quad \text{Eq. 2- 4}$$

In an I-V curve shown in Figure 2-5, the inverse slope intuitively characterizes its dynamic input resistance at that operating point. A constant current load is characterized with a flat input I-V curve and has an infinite dynamic input resistance. The constant resistance category, in a broad sense, will include any curve that has a positive slope over the full operation range, which means that r_{in} is always a (finite) positive value. Similarly, the constant power category will also include curves with a negative slope and hence a (finite) negative r_{in}.

The following table summarizes the categories in terms of I-V curve slope and the value of r_{in}.

Category	**I-V curve slope**	r_{in} **criterion**
Constant resistance	positive	$0 < r_{in} < +\infty$
Constant current	zero	$r_{in} = \infty$
Constant power	negative	$-\infty < r_{in} < 0$

Table 2-1 Input characteristics classification

2.2.3 Stability Analysis

The switched-mode power supplies are already modeled in three categories, namely a constant resistance, a constant current or a constant power load and therefore, the stability is checked upon the prerequisite that input voltage sharing is achieved in the corresponding input-series system when a disturbance is imposed and no voltage runaway happens.

The rectifier converts the AC voltage into one polarity, and has no effect on the switched-mode power supply input characteristics. A sinusoidal input voltage indicates that at every moment, a periodical disturbance is introduced which will challenge the system stability and bring the risk of voltage runaway. To simplify the analysis, the stability is checked at DC voltage input.

1. Constant resistance load

Given the nominal operating point, some converters adopt open-loop control schemes to reduce system cost and control complexity. For example, a buck-boost converter operating in discontinuous conduction mode behaves as a loss-free resistor [16]. The equivalent resistance is $R_{e,i}$ $(i = 1,2)$.

The currents at the input side in Figure 2-6 have the following relation. I_{in} is the system input current for all drivers. $I_{conv,i}$ is the current drawn by the i^{th} converter while $I_{c,i}$ is the current flowing through the corresponding input capacitor.

$$I_{conv,i} = I_{in} - I_{c,i} \quad i = 1,2 \qquad \text{Eq. 2- 5}$$

In steady state, the current through input capacitor $I_{c,i}$ will be zero and voltage over the capacitor remains constant.

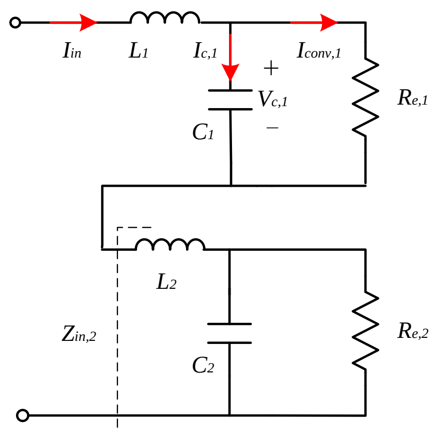


Figure 2-6 Input-series system: constant resistance load

When the input voltage of converter 1 (marked with $V_{c,1}$) increases due to a disturbance, the current flowing through the converter $I_{conv,1}$ will increase according to the input characteristic curve and thus discharge the input capacitor properly to a lower level. This mechanism ensures the system stability.

The input impedance of each driver under AC input equals,

$$Z_{in,i} = \frac{\omega^2 R_{e,i} L_i C_i + \omega L_i + R_{e,i}}{\omega R_{e,i} C_i + 1} \quad i = 1,2 \qquad \text{Eq. 2- 6}$$

According to the basic principles of circuit, connecting two impedances in series is stable. The input voltage will always be shared proportionally to the input impedance ratio even when perturbations are imposed. When two input impedances are equal, the input voltage will be evenly shared. If not, a balanced operating point will still be automatically reached by self-adjustment along the characteristic curves.

The conclusion is not limited to a constant resistance load. The converter dynamic input resistance does not necessarily to be a constant over the full range. The systems will be stable provided that both switched-mode power supplies always have positive dynamic input resistance.

2. Constant current load

An open-loop peak current controlled converter will possibly result in a constant current load characteristic. However, connecting two constant current load in series is unstable, as indicated in [14] and [17].

In Figure 2-7, the converter is represented with a current source that conducts the amount of current that the converter needs to consume.

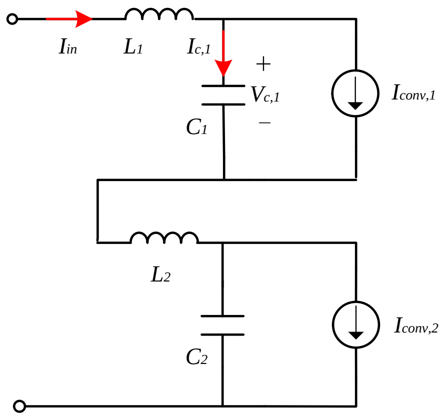


Figure 2-7 Input-series system: constant current load

It is easy to appreciate that the input voltage is evenly shared only if two current sources are identical at all time, which is almost impossible in practice. Otherwise, the system will run into instability. Assume at a time instant $t = t_0$, converter 1 starts to consume a larger current than $I_{conv,2}$ due to an external disturbance. Since the input current is equal to both, the current source $I_{conv,1}$ will have to draw current from the input capacitor marked with C_1. Thus the capacitor voltage can't be built up and the input of that converter is short circuited. In this case, the other driver will take over the full input voltage. The system will end up in voltage runaway.

3. Constant power load

Most of the conventional closed-loop switched-mode power supplies behave like a constant power load. A closed-loop control is needed where the output has to be controlled with required accuracy. It also increases the system robustness against external disturbance. Regardless of the specific control implementation, the converter will behave as a constant power sink once the output power is well regulated.

As shown in Figure 2-5, a constant power load has a negative dynamic input resistance, which will definitely cause stability problem [13], [14].

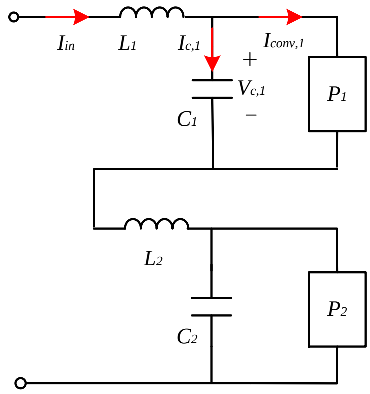


Figure 2-8 Input-series system: constant power load

Each converter behaves as a constant power sink that sinks P_i,

$$I_{conv,i}V_{c,i} = P_i \;\; i = 1,2 \qquad \text{Eq. 2- 7}$$

Assume the system is originally operating in steady state. Now consider the input voltage of converter 1 ($V_{c,1}$) rises slightly due to a disturbance. In response, the output regulator of converter 1 will decrease the duty ratio of gate signal in order to maintain the desired output. The average input current $I_{conv,1}$ is reduced as a consequence and the EMI capacitor is charged up, leading to further increase of the input voltage. The whole process is a positive feedback and as a result, a runaway phenomenon will occur. The voltage over converter 1 keeps increasing while eventually, the input voltage over converter 2 will finally drop to a level where it is no longer possible to provide the desired output.

Hence, two regular closed-loop controlled converters should not be connected in series when no extra care is taken. Once drifted away from the stabilizing state, the system can never reach a second equilibrium operating point. The conclusion can be generalized to any switched-mode power supply with a negative dynamic input resistance.

Stability analysis shows that stable input voltage sharing is guaranteed only if both switched-mode power supplies have positive dynamic input resistance. Hence, the sufficient condition for input-series system stability is that for the full operation range, the following equation is satisfied.

$$r_{in} = \frac{dV_{in}}{dI_{in}} > 0 \qquad \text{Eq. 2- 8}$$

Intuitively, the input curve should have a (finite) positive slope at any point within the operating range, which guarantees a disturbance in input voltage will result in a current change in the same polarity. The conclusion will be used to explore suitable circuit topology and control strategy for an input-series system.

2.3 State-of-art Control Strategies in Input-Series Systems

Guided by the conclusion in section 2.2, a majority of researches on ISOP systems and modular LED drivers are dedicated to achieve such characteristics by means of different control strategies. They are reviewed and summarized in this section.

2.3.1 Open-loop Control Strategies

Some converters operating in a specific mode inherently behave as loss-free resistors, while some other converters may need an additional internal loop to achieve that characteristic. In the latter case, however, it is still an open-loop solution since the output current is not regulated.

In commercial LED driver design, for instance, a boost-based ringing choke converter can be implemented with a fixed on-time control scheme. Similar to a PFC, the constant on-time creates a nearly sinusoidal input current waveform that follows the input voltage, which is rectified mains voltage. Hence, the equivalent input impedance becomes a pure resistance R_e, which only relies on the preset on-time t_{on}.

$$R_e = \frac{V_{in}}{I_{in}} = \frac{2L}{t_{on}} \qquad \text{Eq. 2- 9}$$

Another example is a fixed-frequency buck-boost converter operating in discontinuous conduction mode without additional control. The converter inherently behaves as a loss-free resistor and the input impedance is duty ratio D dependent. The effective resistance is derived from the averaged switch model [16], which is duty-ratio dependent. The duty ratio D will be set at the nominal value to realize a rated driving current for the load.

$$R_e = \frac{2L}{D^2 T_s} \qquad \text{Eq. 2- 10}$$

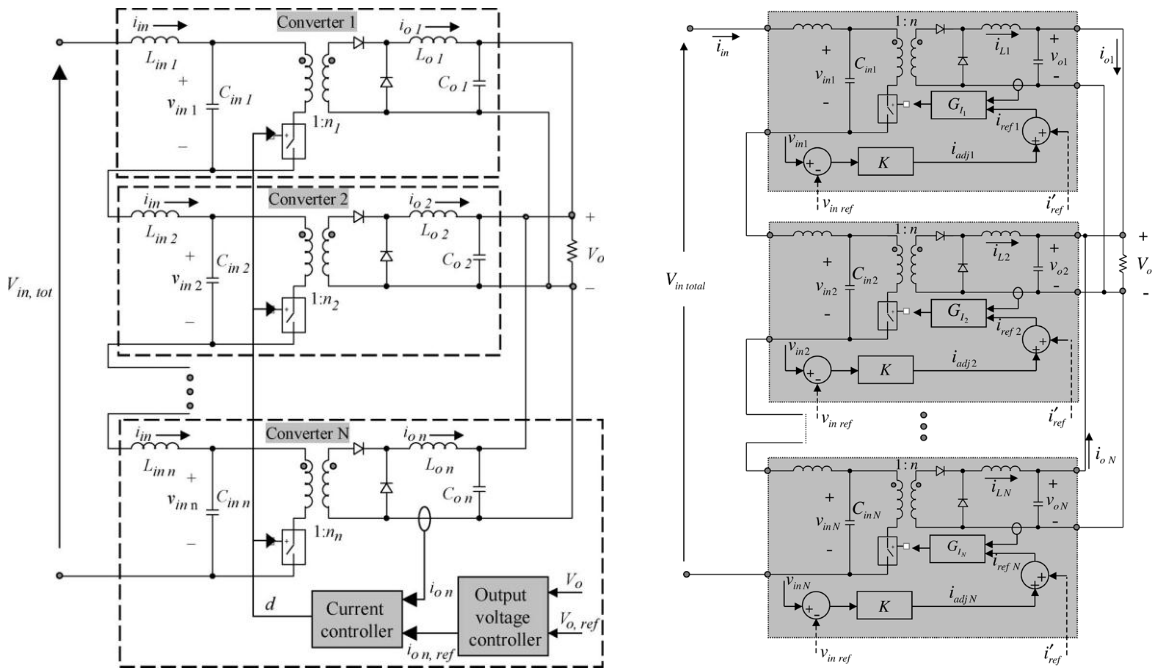
The open-loop approach has a simpler structure but will enable appropriate sharing of input voltage to some extent. The total input voltage is distributed according to the input impedance of each driver. Voltage runaway is not likely to happen although the voltage sharing might be uneven in case of significant component mismatch. One added value of this approach is the inherent power factor correction function.

2.3.2 Closed-loop Control Strategies

A closed-loop solution is more complicated but can achieve accurate input voltage sharing and output control. There are several closed-loop control strategies discussed in literatures for ISOP system and modular LED driver application.

1. Common-duty-ratio approach

A simple but stable control method described for ISOP system is a common-duty-ratio approach, discussed in [18] and [19]. In a system composed of converters with the same topology, one converter is chosen to be the master converter that employs a regular voltage or current mode control while all others are slave converters that follow a global duty ratio.



(a) Common-duty-ratio approach (b) Three-loop approach

Figure 2-9 Two closed-loop control strategies [13][18]

Figure 2-9(a) shows a basic block diagram of the common-duty-ratio controlled ISOP system with forward converters, proposed in [18]. The master converter N is regulated by a standard current mode control and generates a duty ratio accordingly. The duty ratio information is made common to all slave converters by means of communication. Although all slave converters do not have individual control stage, they execute a closed-loop generated duty ratio.

Consider a system with two constituent forward converters. In steady state, the average voltages across the output inductor $(L_{o,1}, L_{o,2})$ and the average currents through the input capacitors $(C_{in,1}, C_{in,2})$ are all zero. The transformer turns ratio is denoted with n_1, n_2 and effective duty ratio in small signal model is denoted with $D_{eff,1}, D_{eff,2}$.

$$V_{in,1} n_1 D_{eff,1} = V_o = V_{in,2} n_2 D_{eff,2} \qquad \text{Eq. 2- 11}$$

$$I_{o,1} n_1 D_{eff,1} = I_{in} = V_{o,2} n_2 D_{eff,2} \qquad \text{Eq. 2- 12}$$

Therefore, when a common duty ratio is applied.

$$D_{eff,1} = D_{eff,2} \quad \text{Eq. 2- 13}$$

$$\frac{V_{in,1}}{V_{in,2}} = \frac{I_{o,1}}{I_{o,2}} = \frac{n_2}{n_1} \quad \text{Eq. 2- 14}$$

When all the converters are identical, the input voltage will be equally divided among them. In presence of component mismatch, though the input voltage may not be evenly shared, the runaway effect can still be avoided. The common-duty-ratio approach has a self-correcting mechanism. The converter with a higher turn ratio temporarily produces a higher secondary voltage and thus a higher inductor current. However, it also leads to higher input current which discharge the input capacitor and decreases the input voltage. This self-correcting mechanism will ensure the system stability.

The same approach is also proposed to LED modular drivers [15], [20]. When the common duty ratio serves all the converters, the output currents are all equal and the input voltage is distributed proportionally to the output voltage, satisfying Eq. 2-3. Hence, this method is valid even when each driver module is driving arbitrary number of LEDs.

2. Three-loop control approach

In practical situation where component tolerance cannot be strictly avoided, an input voltage control loop is still required to precisely distribute the input voltage among the converter modules. Reference [13] presents a three-loop current mode control scheme which consists of an input voltage loop, an output voltage loop and an inner current loop for any buck-derived DC/DC converter and reference [21] details the step-by-step design process. The block diagram is shown in Figure 2-9(b).

The basic idea of three-loop control is that the individual input voltage loop and the common output voltage loop will collaborate to influence the inner current loop, illustrated in Figure 2-10. An output voltage loop generates a common current reference fed to all converters. Within each individual controller, the initial current reference is adjusted by the dynamic input voltage error of that converter. The inner current loop senses the real-time inductor current and regulates it to the modified current reference by varying the duty cycle.

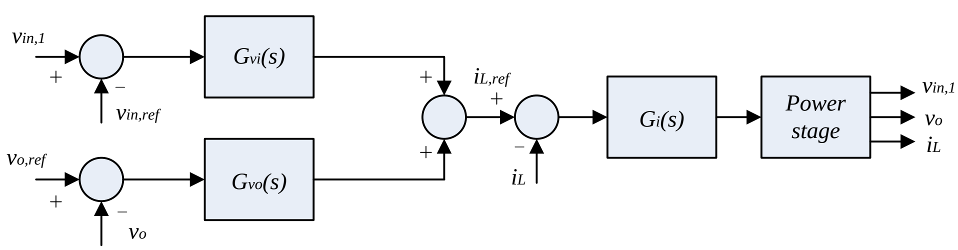


Figure 2-10 Three-loop control approach

In order to regulate the input voltage directly, a proper input voltage reference needs to be chosen. One option is the active input voltage reference recommended in [13], which is the average of the voltages across input capacitors. It should be noted that the average value is not necessary equal to the source voltage divided by N considering the resonance of input LC filter. Therefore, communication between the converters is also necessary to set the input voltage reference dynamically.

$$v_{in,ref} = \frac{\sum_{i=1}^{N} v_{c,i}}{N} \quad \text{Eq. 2- 15}$$

One advantage of such reference is the minimized interference between input voltage loop and output voltage loop and resulting improved transient behaviors. The total correction elements from input voltage loop add up to zero and thus decouple the design of output voltage controller from the input voltage loop.

$$\sum_{i=1}^{N} i_{adj,i} = 0 \quad i = 1,2 \ldots N \quad \text{Eq. 2- 16}$$

An incremental negative resistance model [22] is used for stability analysis. The power stage is modeled as a negative resistance. In parallel with the negative resistance, a controlled current source representing the adjustment signal $i_{adj,1}$ from input voltage loop is placed. Thus, the total converter input current is separated into the current through the negative resistance and the correction current through the input voltage loop. The basic idea is that, by adding the adjustment signal, the stability condition is satisfied.

As commented by [23], the input voltage loop has to be carefully designed. Note that the converter should be necessarily controlled in such a way that equivalent input impedance is positive to stabilize the system, based on the previous discussion. That is, the total input current will increase in case of elevated input voltage and discharge the input capacitor to a reasonable level. Therefore, a minimum stabilizing gain is derived from the converter model.

The same principle is also applicable for voltage mode control. Instead of adjusting the inductor current reference, the input voltage loop directly generates a correction component to the final control signal. Reference [24] presents a uniform voltage distribution control which also includes an input voltage loop.

3. Other approaches

Sensor-less current mode (SCM) control is another alternative solution to achieve stable operation of ISOP systems [25], [26]. The output voltage error, together with the real-time system input voltage is fed to the SCM controller to compute correspondent switching waveforms.

Reference [27] presents a charge control with input voltage feed-forward scheme used in a high-speed train power system, which ensures IVS in both steady state and transients. In order to equally distribute the line voltage, the average input current of each converter is adjusted by the real-time input voltage difference. Thus, IVS is guaranteed for all operating conditions, including the transients. It should be noted that such control scheme is only valid for two-converter system.

2.4 Evaluation of Different Control Strategies

In the previous section, the state-of-art control strategies that are employed in input-series systems are reviewed. The control strategies are classified into two categories, namely open-loop strategy and closed-loop strategy.

The open-loop strategy aims at making the driver inherently a resistor by means of adopting a specific operation mode or adding an auxiliary control. The closed-loop strategy maintains the conventional closed-loop control but requires additional input voltage sharing control to avoid voltage runaway. Whatever category the control strategy belongs to, the key idea of all efforts is common to all: achieve stable input voltage sharing by actively tuning the input characteristics.

The table below summarizes the general pros and cons of different control approaches in terms of input voltage sharing accuracy, system complexity and cost, output regulation and other necessary implementation requirements.

Control strategy	**Pros**	**Cons**
Open-loop	- Simple structure; - Lower cost; - Close-to-unity power factor;	- Limited IVS accuracy due to component tolerance; - Output current not regulated, line regulation problem;
Closed-loop with additional IVS control	- High IVS accuracy, barely affected by component tolerance; - Output current actively controlled, good line regulation;	- More complicated structure; - Higher cost; - Communication needed;

Table 2-1 Comparison of different approaches

Despite of its complexity and higher cost, a closed-loop approach has many benefits. Input voltage sharing can be achieved with high accuracy and is barely affected by component tolerance in the constituent converters. Line regulation performance is also believed to be satisfying since output current is actively regulated despite of input voltage variation.

However, there is practical limitation to implement a closed-loop control in current application. It is shown in the literature view that communication is always required to share information. In common-duty-ratio approach, a global duty ratio information needs to be shared among all constituent converters. The input voltage loop reference in three-loop control approach is also set in a global view. Although communication can be implemented with various methods, including isolated analog or digital communications and direct gate drive coupling, it is difficult to realize in current application. As required by the application condition, no additional wiring or re-wiring for communication bus is permitted in the lighting fixture.

An open-loop approach makes good compromise in system simplicity and performance. The open-loop solution has an intrinsic drawback on line regulation performance that leads to output variation in case of input disturbance. However, there are other benefits to mention. It has a simpler structure and the overall system cost will be reduced consequently, which is preferable for a consumer product. The inherent resistive characteristic helps to achieve a close-to-unity power factor. The light intensity difference due to component mismatch will not be visually significant if the output current unbalance is limited to a reasonable range. Therefore, an open-loop based solution will be further explored in the following investigation.

2.5 Conclusion

In this chapter, stability of an input-series system with independent outputs is studied and analyzed on basis of three different input characteristic categories. A conclusion on system stability is drawn that the DC/DC converter has a positive dynamic input resistance over the operating range.

The state-of-art control strategies implemented in current input-series systems are reviewed to provide design reference. The control strategies are classified into open-loop or closed-loop approach and are evaluated in key aspects for current application. A practical limitation for closed-loop control is the complex realization of communication, while the open-loop approach makes good compromise in system simplicity and overall performance. Therefore, an open-loop based solution is chosen to be further explored.

Chapter 3 Modulated Peak Current Controlled Buck-boost Converter

A modulated peak current controlled buck-boost driver, which realizes stable series operation, is proposed in this chapter. The converter operates in boundary conduction mode in a self-oscillating manner. It is regarded as an open-loop solution because the output current is not tightly regulated with a feedback loop. The basic control strategy and operation principle will be discussed in detail.

3.1 Self-Oscillating Buck-boost Converter

A self-oscillating buck-boost converter is selected in consideration of both application conditions and system cost.

The system input is a sinusoidal voltage. When there is no bulk capacitor after the rectifier, the driver input will be a rectified sinusoidal voltage. At the output, the LED string voltage is nearly a constant voltage, which is not very sensitive to output current. Only non-isolated DC/DC converter topologies are considered as it is a low-power application. In this case, a buck converter can only operate when the input voltage exceeds the output voltage and results in blanking time around the zero-crossing points. Similarly, a boost converter is not suitable either since the LED voltage is lower than the input voltage for most of the time. Considering the voltage conversion ratio, hence, a buck-boost topology is chosen to guarantee full-range operation.

The converter will operate in self-oscillating mode. Self-oscillating converters, which are usually referred to as ringing choke converters (RCC), have been popular for years in cost-sensitive consumer appliances. They are widely used in low-power applications, such as mobile charger and LED drivers, for the relatively simple structure and low cost. To implement a self-oscillating converter, only a few discrete components are required to provide the driving signals instead of a commercial controller.

3.1.1 Buck-boost Converter

As the name suggests, the output voltage V_o of a buck-boost converter can be either higher or lower than input voltage V_{in}. By controlling the transistor duty ratio D , output voltage can be regulated in between zero and an infinite value. The following figure shows the buck-boost topology. Note that the converter has a negative output with respect to the input polarity. The basic operation principles of a buck-boost converter are explained as follows [28], [29].

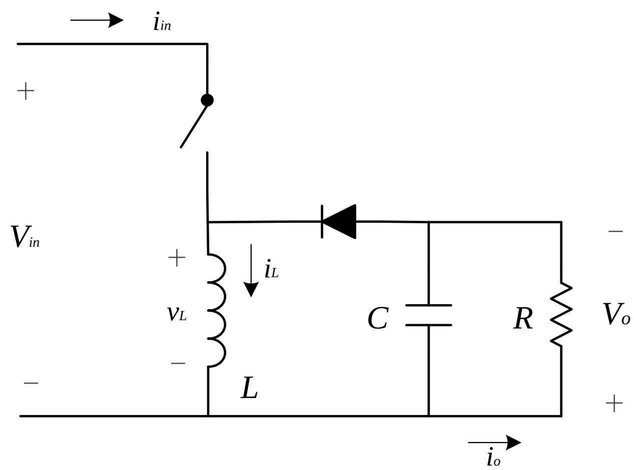


Figure 3-1 Buck-boost converter

If neglecting the voltage drop over the switch, the inductor is being charged by the input voltage during the transistor on-time t_{on}. Inductor current i_L rises linearly with a slope of V_{in}/L and input energy is first stored in the coil.

$$I_{L,pk} = \frac{V_{in}}{L} t_{on} + I_{L,valley} \qquad \text{Eq. 3- 1}$$

The valley current $I_{L,valley}$ can be a positive value for continuous conduction mode (CCM) or zero for discontinuous conduction mode (DCM) and boundary conduction mode (BCM). At this moment, the free-wheeling diode is reverse biased and thus isolates the output from input. Meanwhile, output current is supplied by the energy stored in the output capacitor from the previous cycle.

At the instant $t_{on} = DT_s$, the transistor is switched off by the control signal. The voltage over the inductor reverses its polarity and hence inductor current starts to drop with a constant slope V_o/L. Freewheeling diode now conducts and transfers the energy from the coil to the load during the off-time $t_{off} = (1 - D)T_s$.

$$I_{L,valley} = I_{L,pk} - \frac{V_o}{L} t_{off} \qquad \text{Eq. 3- 2}$$

According to the inductor current waveforms, a buck-boost converter can operate in CCM, DCM or BCM.

1. CCM operation

In continuous conduction mode, the inductor current doesn't reach zero at all time. The following waveforms show the operation in CCM.

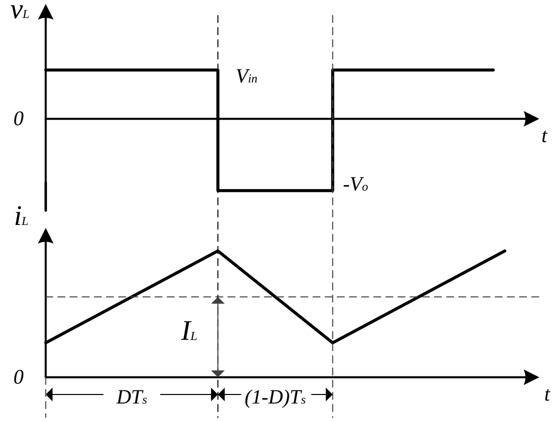


Figure 3-2 Buck-boost converter: CCM waveforms

Knowing the inductor voltage over one cycle has to be zero in steady state in a switching period T_s,

$$V_{in}DT_s + (-V_o)(1-D)T_s = 0 \qquad \text{Eq. 3- 3}$$

The voltage conversion ratio is thus,

$$\frac{V_o}{V_{in}} = \frac{D}{1-D} \qquad \text{Eq. 3- 4}$$

2. DCM operation

If the inductor is fully discharged before the next switching cycle starts, the converter enters discontinuous conduction mode. Apart from the on- and off-state in CCM, a third state is reached, where the switch is opened and the diode is blocked. The inductor current remains zero during the third state and the output current is supplied by the output capacitor.

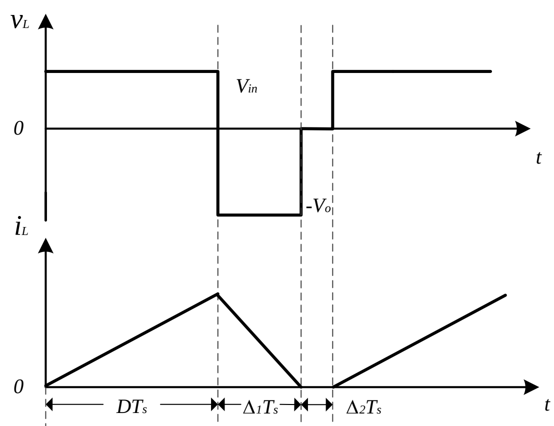


Figure 3-3 Buck-boost converter: DCM waveforms

$I_{o,max}$ is the maximum output current for DCM operation.

$$I_{o,max} = \frac{V_o T_s}{2L} \qquad \text{Eq. 3- 5}$$

3. BCM operation

In between CCM and DCM, there is a boundary operating mode. The inductor current goes to zero at the end of the off-interval and a new cycle starts right at that moment.

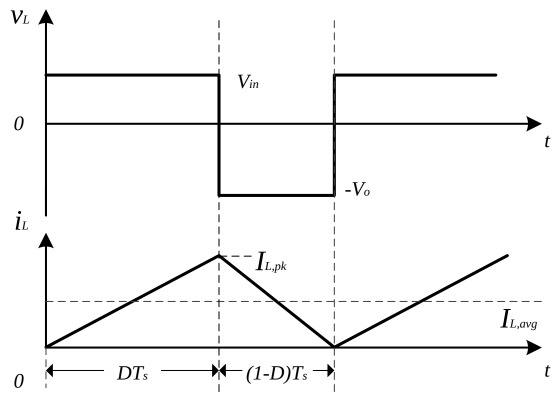


Figure 3-4 Buck-boost converter: BCM waveforms

One important property of BCM is the average inductor current is exactly half of the peak current value. The relation between input and inductor currents can be derived from the waveforms as well.

$$I_{L,avg} = \frac{1}{2} I_{L,pk} = \frac{V_{in} D T_S}{2L} \quad \text{Eq. 3- 6}$$

$$I_{in} = D I_{L,avg} \quad \text{Eq. 3- 7}$$

A boundary output current for BCM is derived as,

$$I_{oB} = \frac{V_O T_S}{2L} (1-D)^2 \quad \text{Eq. 3- 8}$$

A self-oscillating converter always operate in boundary conduction mode and the properties indicated by Eq.3-6 and 3-7 can be utilized therefore.

3.1.2 Self-oscillating Converter

A self-oscillating converter (also known as RCC converter) basically consists of four additional passive components and one auxiliary winding. The switching signals come from the oscillation of the passive components. Theoretically, the same principles can be applied to any converter such as buck, boost or buck-boost topologies.

The operation principles of a basic RCC circuit will be discussed based on buck-boost topology without any additional control. Figure 3-5 shows the schematic.

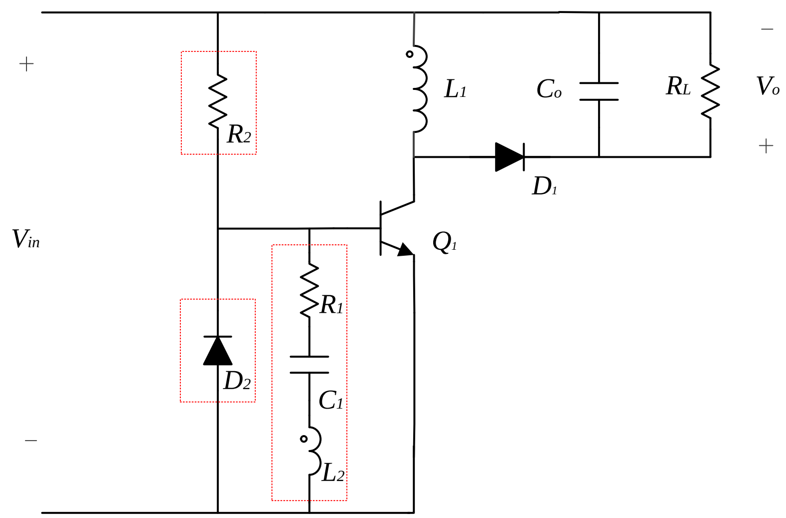


Figure 3-5 Self-oscillating buck-boost converter

For the ease of control implementation, the buck-boost topology is inverted to have a grounded switch. The power switch is an NPN bipolar transistor. In the schematic above, the components in red dashed boxes constitute a basic self-oscillating configuration. Their functions are briefly stated:

R_1: Base-current limiting resistor

C_1: Oscillating capacitor

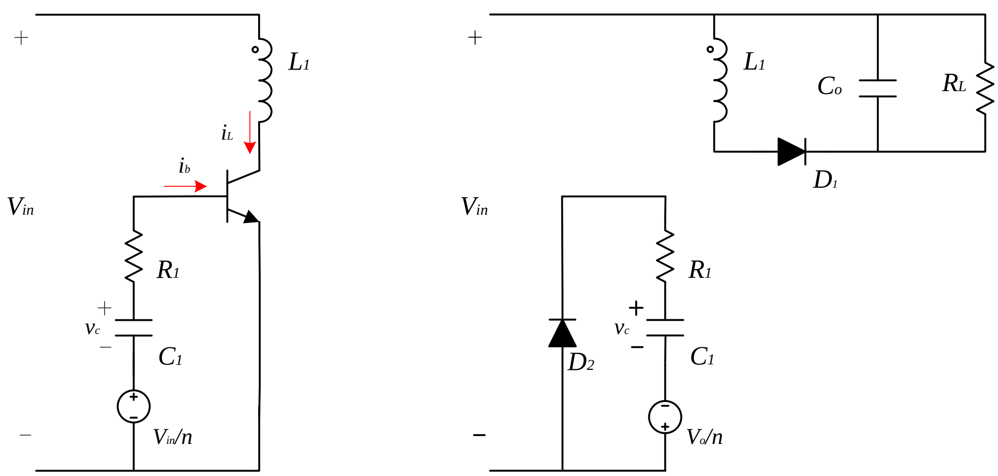
R_2: Start-up resistor

D_2: Free-wheeling diode

L_2: Auxiliary winding (coupled to L_1)

The on- and off-state equivalent circuits are illustrated below in Figure 3-6. The auxiliary winding L_2 is coupled to the main inductor L_1 and is replaced by a voltage source in the equivalent circuit. The operation principles of a self-oscillating converter are briefly discussed in [30] based on the on- and off-state equivalent circuits.

When the circuit is powered on, a small start-up current will flow to Q_1 base via the start-up resistor R_2 and partially turns Q_1 on. The inductor L_1 is excited and gets a positive voltage which equals $V_{in} - V_{ce}$. At this time, a positive voltage with the same polarity appears over the auxiliary winding L_2, which equals $\frac{V_{in}-V_{ce}}{n}$ (n: turns ratio). Transistor Q_1 is forward biased by the auxiliary winding and the base current increases. As the device is more on, the collector-emitter voltage V_{ce} will drop and the auxiliary winding gets gradually higher voltage. The positive feedback process will fully turn on the transistor soon.



(a) On-time (b) Off-time

Figure 3-6 RCC equivalent circuits

In the following calculations, the on-state voltage drop over the transistor is ignored. Assume the initial states of capacitor voltage and inductor current are,

$$v_c(0) = V_{C0} \quad \text{Eq. 3- 9}$$

$$i_L(0) = 0 \quad \text{Eq. 3- 10}$$

The inductor current, which is equal to the collector current, increases linearly. The capacitor C_1 is being charged by the auxiliary winding.

$$i_L(t) = \frac{V_{in}}{L} \times t \quad \text{Eq. 3- 11}$$

$$v_c(t) = V_{C0} \times e^{-\frac{t}{\tau}} - \left(\frac{V_{in}}{n} - V_{BE}\right) \times \left(1 - e^{-\frac{t}{\tau}}\right), \ \tau = R_1 C_1 \quad \text{Eq. 3- 12}$$

As the capacitor C_1 is being charged, the voltage over the base resistor will decrease and reduces the base current as a result.

$$i_b(t) = -C_1 \frac{dv_c(t)}{dt} = \frac{1}{R_1}\left(\frac{V_{in}}{n} - V_{BE} + V_{C0}\right) e^{-\frac{t}{\tau}} \quad \text{Eq. 3- 13}$$

After a while, the circuit will reach a critical point at time instant $t = \mathrm{t}_1$.

$$i_L(t_1) = i_c(t_1) = \beta i_b(t_1) \quad \text{Eq. 3- 14}$$

Based on I-V curve of a BJT, the transistor will shift back to the active region. However, due to the storage time of a bipolar transistor t_s, the transistor will still remain on for a while and delay the switch-off action.

During the transistor storage time, the base current keeps decreasing and collector-emitter voltage builds up. The voltages on both windings will decrease. The positive feedback process again leads to the turn-off of the transistor. The auxiliary winding gets a reversed voltage and draws current from Q_1 base to keep it off deeply.

The initial status of the off-period has to take storage time into account. Substituting $t = t_1 + t_s$ into Eq. 3-11 and 3-12,

$$i_L(t_1 + t_s) = \frac{V_{in}}{L} \times (t_1 + t_s) = I_1 \qquad \text{Eq. 3- 15}$$

$$v_c(t_1 + t_s) = V_{C0} \times e^{-\frac{t_1+t_s}{\tau}} - \left(\frac{V_{in}}{n} - V_{BE}\right) \times \left(1 - e^{-\frac{t_1+t_s}{\tau}}\right) = V_{C1} \qquad \text{Eq. 3- 16}$$

During off-time, the inductor current now decreases with a constant slope.

$$i_L(t) = I_1 - \frac{V_o}{L} \times (t - t_1 - t_s) \qquad \text{Eq. 3- 17}$$

A reversed polarity voltage appears over the auxiliary winding and now the diode D_2 serves as a freewheeling diode. The voltage over C_1 follows Eq. 3-18. The voltage drop over the freewheeling diode is denoted with V_F.

$$v_c(t) = V_{C1} \times e^{-\frac{t-t_1-t_s}{\tau}} + \left(\frac{V_o}{n} - V_F\right) \times \left(1 - e^{-\frac{t-t_1-t_s}{\tau}}\right) \qquad \text{Eq. 3- 18}$$

At the end a cycle, the inductor current will reach zero and capacitor voltage goes back to V_{C0} in steady-state. During the off-time, the energy storage in the primary winding will be transferred to the load. When all the energy is released, every winding will go back to the starting state. The resonance of inductor and parasitic capacitance after inductor current goes to zero helps to start the next cycle. The voltage on secondary winding swing from $-V_o/n$ to V_o/n in a pendulum way and turns on the transistor again.

Figure 3-7 shows the operating waveforms of a self-oscillating converter. The voltage over auxiliary winding is denoted with v_s.

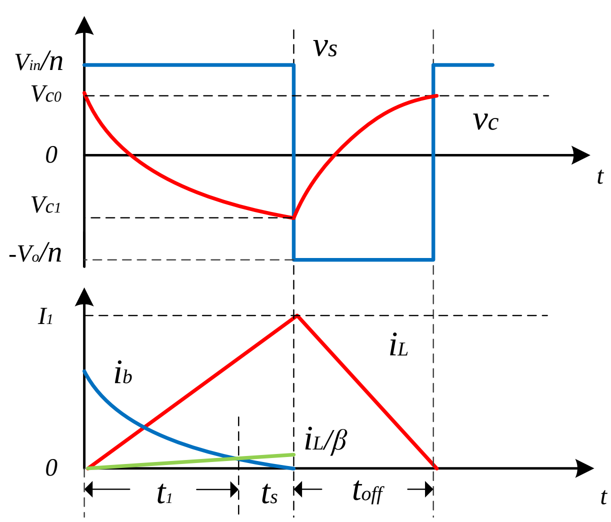


Figure 3-7 Self-oscillating converter waveforms

In summary, a self-oscillating buck-boost converter operates in boundary conduction mode with a variable frequency. The transistor is forced to turn off when the oscillation reaches a critical point and is turned on again when the inductor current goes down to zero. However, it is also possible to implement peak current or constant on-time control, which actively turns off the transistor before that critical point. One example is to replace the Si diode with a zener diode to set the inductor peak current, in cases where the output is not tightly regulated [31]. A current sense resistor R_s in series with the transistor emitter will be necessary to sense the inductor peak current. It is also applicable to implement constant on-time control with discrete components, utilizing the RC constant.

3.2 Modulated Peak Current Control

An important property of a BCM buck-boost converter is that the average input current can be expressed in terms of input voltage, output voltage and inductor peak current. This unique feature gives a chance to adjust the input characteristics as desired by setting an appropriate $I_{L,pk}$. A novel control concept, which is named modulated peak current control, is proposed for stable series operation.

3.2.1 Control Equation and Stability Condition

In order to mathematically generate the equations that describe a BCM buck-boost converter, following assumptions are made.

1. Converter operation is ideal: the power switch is turned on or off immediately at critical points without any delay.
2. The on-state voltage drop over freewheeling diode and power switch is ignored.

The basic relation between input and inductor currents for a BCM buck-boost converter is already derived from the basic operation waveforms and is valid at any certain DC operating point. Substituting Eq. 3-6 into 3-7, the average input voltage becomes,

$$I_{in} = \frac{D}{2} \times I_{L,pk} \qquad \text{Eq. 3- 19}$$

Duty ratio D can be written from Eq. 3-4.

$$D = \frac{V_o}{(V_o + V_{in})} \qquad \text{Eq. 3- 20}$$

Combining Eq. 3-19 and 3-20,

$$I_{in} = \frac{V_o}{2(V_o + V_{in})} \times I_{L,pk} \qquad \text{Eq. 3- 21}$$

The average input current I_{in} at that operating point is thus expressed as a function of input voltage V_{in}, output voltage V_o and inductor peak current $I_{L,pk}$. The output voltage V_o is assumed to be a constant, as the LED load voltage is not significantly affected by the output current. Control efforts that dedicated to control the peak inductor current can not only effectively regulate the converter output power but also shape the input characteristic.

It is mentioned previously that a constant peak current control can be easily implemented in the self-oscillating converter by replacing the free-wheeling diode D_2 with a zener diode and adding a current sense resistor R_s. Zener diode will clamp the inductor peak current to a constant value set by the following equation.

$$V_z = I_{L,pk}R_s + V_{BE} \qquad \text{Eq. 3- 22}$$

However, the input characteristic of the driver links to instability risks. Suppose a constant peak current reference $I_{L,pk}$ is applied. It is clear from Eq. 3-21 that the input current will drop as a result of higher input voltage, indicating a negative dynamic input resistance. Thus, a constant peak current control is not suitable for series operation.

Instead of a static current reference, a modulated peak current control block sets the inductor peak current reference dynamically, depending on the real-time input voltage. The **control equation** is written as,

$$\boldsymbol{I_{L,pk} = aV_{in} + b \quad a, b > 0} \qquad \textbf{Eq. 3- 23}$$

The equation that governs the input characteristics now becomes,

$$I_{in} = \frac{V_o}{2(V_o+V_{in})} \times (aV_{in} + b) \qquad \text{Eq. 3- 24}$$

which needs to fulfill the stability condition derived in chapter 2. It is noted that the variable V_{in} now appears in the numerator and therefore it would be possible to make I_{in} a monotonous increasing function of V_{in} for stability considerations. Mathematically, the derivative of I_{in} with respect to V_{in} needs to be positive over the input voltage range,

$$\frac{dI_{in}}{dV_{in}} = \frac{aV_o^2 - bV_o}{2(V_o+V_{in})^2} > 0 \qquad \text{Eq. 3- 25}$$

The stability condition equation is concluded as,

$$\boldsymbol{aV_o - b > 0} \qquad \textbf{Eq. 3- 26}$$

Consider an AC input voltage. Assume the rectifier bridge is ideal. The voltage after the rectifier bridge is therefore a rectified sinusoid.

$$v_{in}(t) = V_{pk}\,|\sin(2\pi ft)| \qquad \text{Eq. 3- 27}$$

V_{pk} is the peak input voltage that equals to $\sqrt{2}$ times the RMS value and f represents the line frequency.

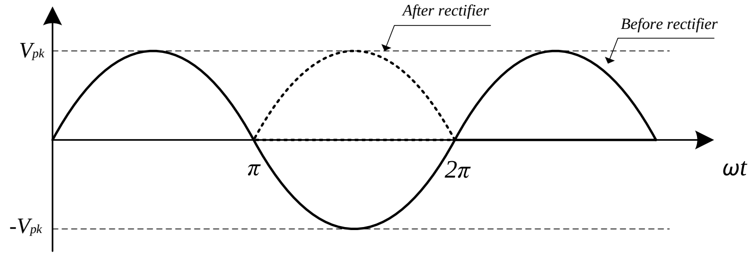


Figure 3-8 Input voltage waveforms

The phase angle is $\theta = 2\pi f t$ and all quantities that vary with instantaneous input voltage will be expressed as a function of θ.

$$v_{in}(\theta) = V_{pk}\,|\sin(\theta)| \qquad \text{Eq. 3- 28}$$

The current waveforms of a modulated peak current controlled buck-boost over half line cycle are drawn to illustrate the basic operation principles. The inductor peak current reference $i_{L,pk}(\theta)$ has a DC component as the constant offset and an AC component, which is proportional to dynamic input voltage value.

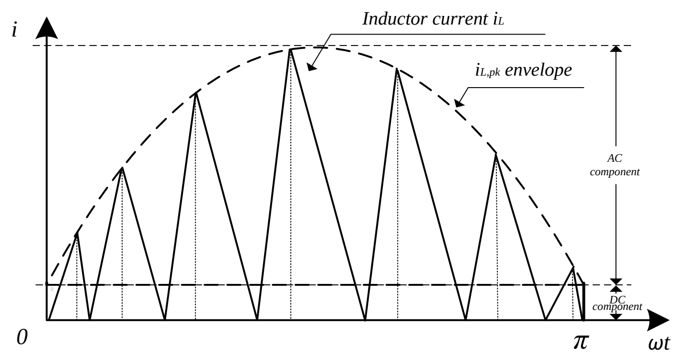


Figure 3-9 Modulated peak current control: current waveforms

The coefficients a and b must satisfy the equation above to guarantee a positive dynamic input resistance over the operating range. On the other hand, the coefficient pair should also be able to deliver a required output current to LED load. When the input voltage is a rectified sinusoid described by Eq. 3-28, the average diode current $i_D(\theta)$ equals,

$$i_D(\theta) = \big(1 - D(\theta)\big) \times \frac{i_{L,pk}(\theta)}{2} = \frac{V_o}{2(V_o + v_{in}(\theta))} \times (a v_{in}(\theta) + b) \qquad \text{Eq. 3- 29}$$

In steady state, the average current through the output capacitor will be zero. The average value of $i_D(\theta)$ over half mains cycle is thus equal to the output LED current I_o.

$$\frac{1}{\pi}\int_0^{\pi} i_D(\theta)d\theta = I_o \qquad \text{Eq. 3- 30}$$

So far, the converter operation is assumed to be ideal: the power switch is switched off immediately once the inductor current reaches the current reference. However, the storage time of a bipolar transistor will cause a delay in turning off the switch in practice. Storage time is defined as the delay interval from the removal of positive base drive current to the beginning of collector current decay [32]. It does not necessarily imply an increase of switching loss but will definitely limit the highest switching frequency of the converter. If turn-off is delayed, the actual peak current could exceed the reference value by an excessive current Δ_{i_L} and brings control inaccuracy.

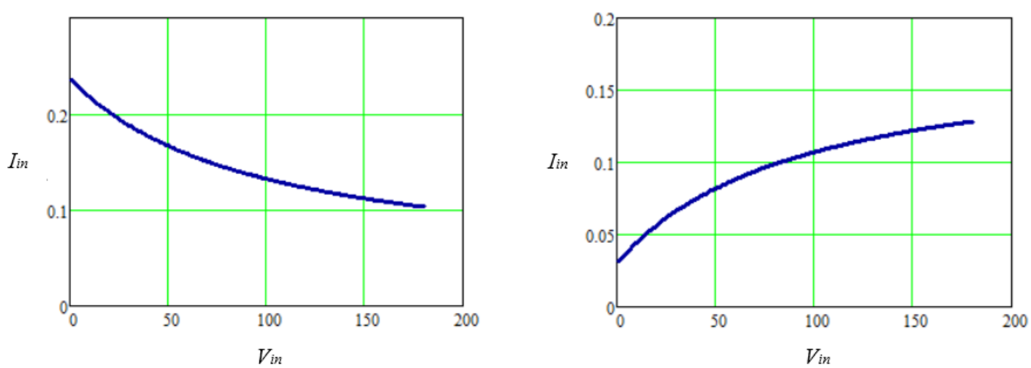
It is by far quite difficult to model the storage time effect with electrical parameters since it is affected by multiple factors including temperature, voltage and current. For simplicity, the storage time effect is modeled with a constant delay time Δt for analysis, which represents the interval from the generation of turn-off control signal to the completion of turn-off process. Assume that during Δt inductor current still rises with a constant slope.

$$\Delta_{i_L} = \frac{V_{in}}{L}\Delta t \qquad \text{Eq. 3- 31}$$

The control equation can be adjusted accordingly.

$$I_{L,pk} = aV_{in} + b + \Delta_{i_L} \qquad \text{Eq. 3- 32}$$

Figure 3-10 shows the input curves of a buck-boost converter under constant peak current control and modulated peak current control, respectively. The output current of each converter is regulated to the same level when operating with half-mains input by setting an adequate current reference. The characteristics are plotted with reasonable assumptions on L and Δt.



(a) Constant I_{pk} control (b) Modulated I_{pk} control

Figure 3-10 Input characteristic under different control strategies

It is easy to perceive that the input curves should pass through the origin and during a short start-up interval input current will rise with input voltage as the power goes up. The curves plotted in Figure 3-10 are based on ideal mathematical calculation, in which non-ideal intervals are not implied. It is still acceptable since during start-up both current and voltage are relatively low. And above all, the characteristic in steady-state is of greater concern to the overall system stability.

As predicted by Eq. 3-24 (setting $a = 0$), the input current of constant peak current control tends to go down at higher input voltage. The converter now has a similar characteristic as a constant power load. Previous analysis already shows that the negative dynamic input resistance is detrimental to the stability of an input-series system.

On the contrary, the modulated peak current control strategy results in positive dynamic input resistance by relating the peak inductor current to real-time input voltage. Compared to the constant peak current control, the input characteristics of modulated peak current control is more close to a resistor, which is desirable for series operation.

3.2.2 Circuit Implementation

A control strategy on inductor peak current is derived in section 3.2.1 in order to achieve stable operation of the input-series system. The inductor current reference governed by Eq. 3-23 has a dynamic AC part that varies with real-time input voltage and a static DC offset that remains constant. The control strategy can be implemented in different ways, either with discrete components or a controller IC.

A basic implementation of modulated peak current controller is presented in Figure 3-11. Five major function blocks are denoted in the schematic, namely rectifier, EMI filter, power stage, self-oscillating block and modulated-peak-current controller.

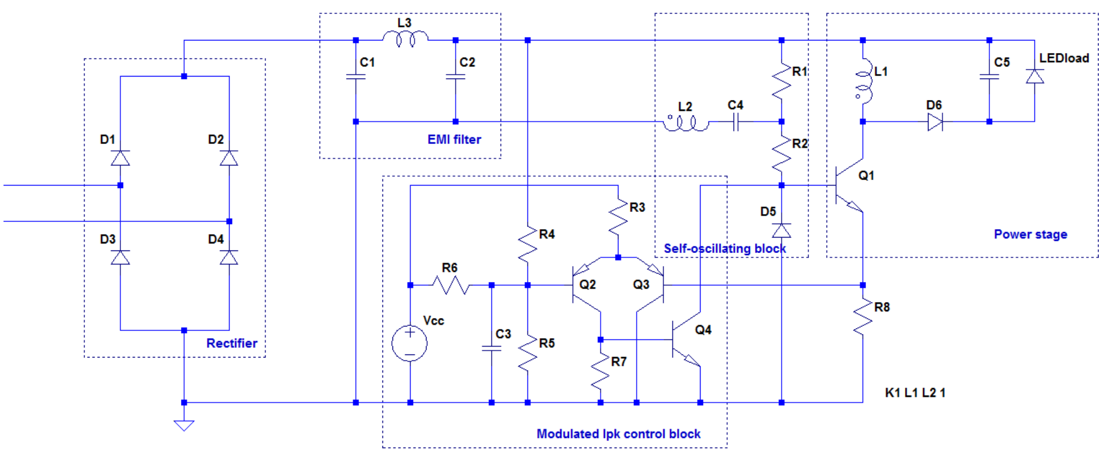


Figure 3-11 Modulated I_{pk} controlled buck-boost converter

The system input is an alternating voltage. Before connected to the DC/DC converter, the AC voltage is first rectified by a rectifier bridge. An EMI filter forms a low-pass filter to filter out the high frequency noise. To enable full range operation, the power stage is chosen as a buck-boost converter with additional passive components and an auxiliary winding to facilitate the self-oscillating. The passive components are arranged exactly the same as discussed in section 3.1. Instead of being naturally turned off by oscillation signals, the transistor is actively turned off at a certain current level. A current sense resistor R_8 is added to sample the inductor current. The modulated-peak-current controller mainly consists of a comparator to control the inductor peak current.

The core control function is achieved by a comparator consisting of two PNP transistors Q_2 and Q_3 with common emitter, shown in Figure 3-12. The bases of Q_2 and Q_3 are used as the inputs of the comparator. The peak inductor current reference is connected to Q_2 base as v_{ref}, while the real-time inductor current information is fed to Q_3 base as a voltage signal v_{sense}.

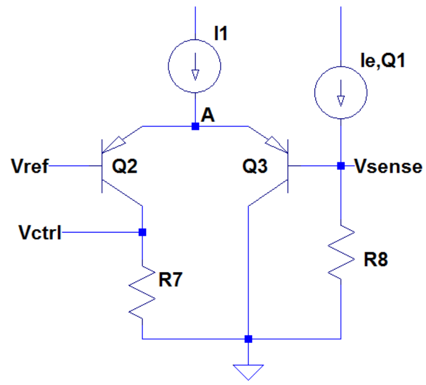


Figure 3-12 Comparator schematic

The emitter current i_{e,Q_1} (equal to inductor current i_L plus a small amount of base current of Q_1 when the switch is closed) is sensed by the sense resistor R_8 and translated into a proportional voltage v_{sense}.

$$v_{sense} = i_{e,Q_1} R_8 \qquad \text{Eq. 3- 33}$$

The peak current reference is also indicated with a reference voltage v_{ref}.

$$v_{ref} = (av_{in} + b)R_8 \qquad \text{Eq. 3- 34}$$

The reference voltage is acquired by a three-resistor network in Figure 3-11, setting the static and dynamic components respectively. Resistors R_4 and R_5 form a voltage divider connected to the bus voltage while R_5 and R_6 forms another one connected to a power supply V_{cc}. A small capacitor C_3 is placed at Q_2 base to filter out the high-frequency ripple from the bus voltage. Based on the principle of superposition, the reference voltage is calculated as,

$$v_{ref} = \frac{\frac{1}{\frac{1}{R_5}+\frac{1}{R_4}}}{R_6+\frac{1}{\frac{1}{R_5}+\frac{1}{R_4}}} \times V_{cc} + \frac{\frac{1}{\frac{1}{R_5}+\frac{1}{R_6}}}{R_4+\frac{1}{\frac{1}{R_5}+\frac{1}{R_6}}} \times v_{in} \qquad \text{Eq. 3- 35}$$

In most cases, $R_5 \ll R_6$ and $R_5 \ll R_4$ are valid for low-power application. Hence Eq. 3-35 is simplified to be,

$$v_{ref} \approx \frac{R_5}{R_6+R_5} \times V_{cc} + \frac{R_5}{R_4+R_5} \times v_{in} \qquad \text{Eq. 3- 36}$$

The power supply V_{cc} on one hand provides the static current reference via a voltage diver, and on the other hand powers up the comparator. Together with a resistor R_3, it serve as a current source to the comparator. In the schematic shown in Figure 3-12, it is replaced by a current source I_1.

The operating principles are explained as follows. Originally, the voltage over sense resistor (v_{sense}) is zero and thus transistor Q_3 base has a zero input, while the voltage at transistor Q_2 base (v_{ref}) has a positive value. Transistor Q_3 consequently conducts the total amount of current I_1. The common-emitter point A is clamped at a lower potential that keeps transistor Q_2 off.

$$v_A = v_{sense} + (-V_{BE,Q_3}) \quad \text{Eq. 3- 37}$$

During the transistor on-interval, v_A increases as the inductor current goes up until the voltage is sufficient to turn on Q_2. At the critical instant when v_{sense} reaches v_{ref}, Q_2 will conduct a portion of I_1. The control signal v_{ctrl}, which is the voltage over R_7, rises and turns on Q_4 as a result. The base of main transistor Q_1 is pulled down to ground via Q_4 and is thus being turned off. After that, v_{sense} decreases to zero again awaiting the next cycle.

It is worth mentioning that that two PNP transistors Q_2 and Q_3 form the comparator in a differential manner. If the property of one transistor is changed dramatically by temperature and the other one is not, the comparator will be very imprecise. Fortunately, these two transistors are placed so close to each other or even packed in the same package that they will most likely suffer the same temperature change. When they are affected simultaneously, the comparator will still function well.

3.2.3 EM Ballast Compatibility

The electro-magnetic ballast used in line-frequency fluorescent lighting is mostly an inductive ballast. The main function of the ballast is to facilitate lamp start-up process and limit the current flowing through the lamp afterwards. As required by application, the driver under development should be compatible with various electro-magnetic ballasts.

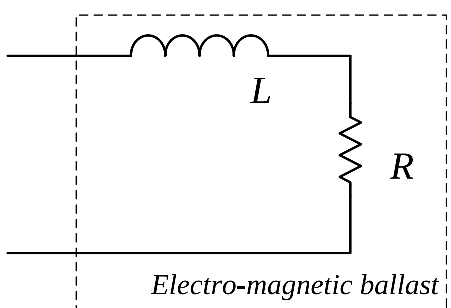


Figure 3-13 Electrical representation: electro-magnetic ballast

An electro-magnetic ballast is in general an inductor with a series resistance. It will not in principle influence the fundamental operation of the driver, which is based on a switched-mode power supply. However, some interactions should be taken into consideration.

First of all, an electro-magnetic ballast may cause driver input voltage distortion. The inductance value of an electro-magnetic ballast is in the order of several *Henries*. Shortly after power-on, oscillations may be observed due to the resonance of the EM ballast and the driver EMI filter at a frequency of several hundred *Hertz*. In steady-state, the time-varying current passing through the inductor will induce a voltage over the ballast, whose amplitude is proportional to the inductance value and rate of current change. A fast changing current can generate a voltage spike up to more than a hundred volts.

$$v_L = L\frac{di}{dt} \qquad \text{Eq. 3- 38}$$

This induced voltage is superposed on the power supply voltage, which may well impose excessive voltage stress at the converter and destroy the power switch as a result. If so, a safety margin and/or transient voltage suppression are thus essential for reliability. However, it is also possible that after superposition the peak voltage is reduced.

Secondly, the presence of a large inductor may further distort the current waveform due to the resonance frequency it forms with the EMI filter, and consequently increase the total harmonic distortion. In some cases, however, the large inductance helps to filter out some high-frequency component and therefore THD even becomes better.

Thirdly, power loss in its significant series resistance and the magnetic core may bring the overall efficiency down.

3.3 Control Equation Analysis

The control equation described by Eq. 3-23 has two coefficients a and b, which set the AC and DC components in the current reference, respectively. These two coefficients should meet the following requirements.

1. Ensure the basic condition for stability stated in Eq. 3-26.
2. Achieve nominal output current by utilizing Eq. 3-30.

Constrained by the second requirement, coefficients a and b are not independent variables but interrelated to each other. If coefficient a increases, b has to decrease in order to maintain the same output current. On top of this, however, many pairs of coefficients are possible to achieve the same output current while maintaining the positive dynamic input resistance. It hence gives a lot of freedom to compromise on different technical objectives of the specific application by choosing an appropriate pair of coefficients. The effect of coefficients a, b will be analyzed theoretically and investigated by *Matlab* simulation. The performance will be evaluated in terms of power balancing and power regulation as a guidance in coefficient setting.

3.3.1 Linearized Input Curve

An input curve of a modulated peak current controlled self-oscillating buck-boost converter has been plotted in Figure 3-10(b). It is a non-linear curve, whose slope decreases gradually as the input voltage increases. In order to simplify *Matlab* calculations, the input curves are first linearized upon power conservation.

To illustrate, Figure 3-14 shows both the original input curve and the linearized input curve.

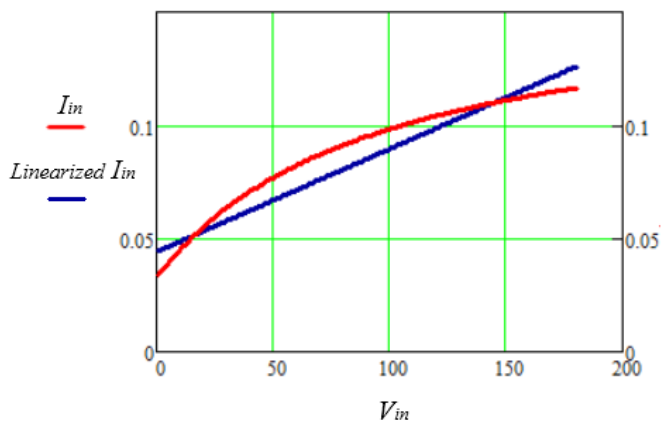


Figure 3-14 Linearization of input curve

In order to linearize the characteristic of a specific design, the following steps are taken. The linearized input curve is characterized with a constant dynamic on-resistance R_{dyn} and a current intercept I_{ofs}.

$$V_{in} = R_{dyn} \times (I_{in} - I_{ofs}) \qquad \text{Eq. 3- 39}$$

The input current I_{in} is thus represented as,

$$I_{in} = \frac{V_{in}}{R_{dyn}} + I_{ofs} \qquad \text{Eq. 3- 40}$$

Given the designed nominal power P_{nom} and R_{dyn}, the current offset I_{ofs} can be calculated accordingly. In ideal situation, the input voltage is assumed to be exactly half of the nominal input voltage (230V). By integrating the instantaneous power over half mains cycle, the driver should be capable of delivering the nominal power P_{nom} specified for this design.

$$P_{nom} = \frac{1}{\pi}\int_0^{\pi} \frac{230\sqrt{2}}{2}\sin(\theta)\,\left(\frac{\frac{230\sqrt{2}}{2}\sin(\theta)}{R_{dyn}} + I_{ofs}\right)d\theta \qquad \text{Eq. 3- 41}$$

Substituting Eq. 3-40 into equation 3-41, the solution to I_{ofs} is,

$$I_{ofs} = \frac{\pi P_{nom}}{230\sqrt{2}} - \frac{230\sqrt{2}\pi}{8R_{dyn}} \quad \text{Eq. 3- 42}$$

Hence, the input characteristic is linearized as follows.

$$I_{in} = \frac{V_{in}}{R_{dyn}} + \frac{\pi P_{nom}}{230\sqrt{2}} - \frac{230\sqrt{2}\pi}{8R_{dyn}} \quad \text{Eq. 3- 43}$$

Although it seems not realistic to have current offset at zero input in reality, it is still acceptable since the magnitudes of voltage and current are so small that it counts for very little in the overall power. However, I_{ofs} shouldn't be a negative value anyway. It means there is a lower boundary for the dynamic on-resistance R_{dyn} which equals,

$$R_{dyn,min} = \frac{230^2}{4\,P_{nom}} \quad \text{Eq. 3- 44}$$

Matlab can then calculate the operating points when two drivers are connected in series, given the input characteristic in the form of Eq. 3-40.

$$I_{in,1} = \frac{V_{in,1}}{R_{dyn,1}} + I_{ofs,1} \quad \text{Eq. 3- 45}$$

$$I_{in,2} = \frac{V_{in,2}}{R_{dyn,2}} + I_{ofs,2} \quad \text{Eq. 3- 46}$$

When they are connected in series to a sinusoidal input voltage, two relations are naturally established at any time.

$$I_{in,sys}(\theta) = I_{in,1}(\theta) = I_{in,2}(\theta) \quad \text{Eq. 3- 47}$$

$$V_{in,sys}(\theta) = \sqrt{2}V_{mns}\sin\theta = V_{in,1}(\theta) + V_{in,2}(\theta) \quad \text{Eq. 3- 48}$$

Since 50Hz is a relatively low-frequency input, it is thus reasonable to assume the system characteristics change dynamically with negligible delay. Together with Eq. 3-45 and 3-46, system input current can be calculated.

$$I_{in,sys}(\theta) = \frac{I_{ofs,1}R_{dyn,1} + I_{ofs,2}R_{dyn,2} + \sqrt{2}V_{mns}\sin\theta}{R_{dyn,1} + R_{dyn,2}} \quad \text{Eq. 3- 49}$$

Their operating points are therefore determined mathematically. The average power is again the integral of instantaneous power through the mains cycle.

$$P_{in,i} = \frac{1}{\pi}\int_0^{\pi} V_{in,i}(\theta)\, I_{in,i}(\theta)d\theta \quad i = 1,2 \quad \text{Eq. 3- 50}$$

3.3.2 Simulation Results: Effect of a, b

With the help of *Matlab*, the impact of different input characteristics are investigated in a statistical way. *Matlab* programs compare the system performance at different R_{dyn} and aim to give some hints on how to properly select the coefficients a and b.

System performance is evaluated in terms of power. There are two reasons: 1) in an input-series system, input currents are naturally made equal and hence power balancing implies how well the input voltage sharing is achieved. 2) The calculations are all based on input curves and have no information linked to the output end. Therefore, it is much easier to compare the power delivered by the converter.

In a specific design, the nominal value of R_{dyn}, P_{nom} and V_{mns} should be given as constant. The typical values of R_{dyn} and P_{nom} represent the intrinsic characteristics of a driver design. Due to component tolerance, however, all drivers of that design will not be identical and their own $R_{dyn,i}$ and $P_{nom,i}$ will differ from each other on a reasonable spread. The RMS value of nominal input voltage is fixed at $V_{mns} = 230V$ but the real input voltage $V_{mns,i}$ can vary within $\pm 15\%$.

Thus, in total, three random variables are considered: $R_{dyn} = \{ R_{dyn,1}, R_{dyn,2}, R_{dyn,3}, \dots \}$ and $P_{nom} = \{ P_{nom,1}, P_{nom,2}, P_{nom,3}, \dots \}$ representing individual converter intrinsic properties; $V_{mns} = \{V_{mns,1}, V_{mns,2}, V_{mns,3}, \dots \}$ representing the real operation condition.

If the sample size is sufficiently large, a random variable X will tend to follow a normal distribution.

$$X \sim N(\mu, \sigma^2) \qquad \text{Eq. 3- 51}$$

Its probability density function $f(x)$ is written as,

$$f(x) = \frac{1}{\sigma\sqrt{2\pi}} e^{-\frac{(x-\mu)^2}{2\sigma^2}} \qquad \text{Eq. 3- 52}$$

where μ is the mathematical expectation and σ is the standard deviation. Theory of mathematical statistics shows if a random variable X follows normal distribution, the chance that it falls into $(\mu - 3\sigma, \mu + 3\sigma)$ will be 0.9974. Figure 3-15 plots the probability density function.

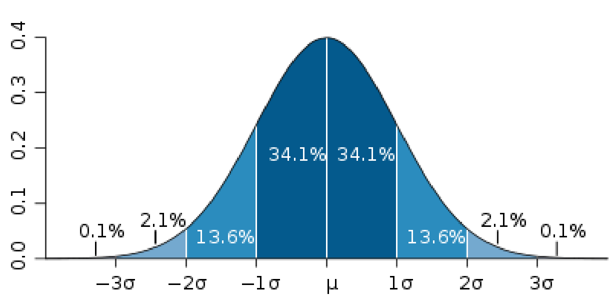


Figure 3-15 Normal distribution: probability density function $f(x)$ [33]

For each random variable, a normal distribution based on $\pm 3\sigma$ principle is generated by *Matlab* program. Any variable that ranges out of $(\mu - 3\sigma, \mu + 3\sigma)$ is excluded automatically by the program since such extreme situation will rarely happen and is no longer considered. It doesn't matter what is the exact value of σ, as long as it is a consistent standard in evaluation.

1) Power balance (IVS): R_{dyn} and P_{nom}

When two constituent converters have identical input characteristics, the input voltage (and thus input power) will be well balanced. However, the characteristics mismatch cannot be avoided due to discrete component tolerances, the overall contribution of which is reflected on the value of R_{dyn} and P_{nom} as intrinsic property of the converter.

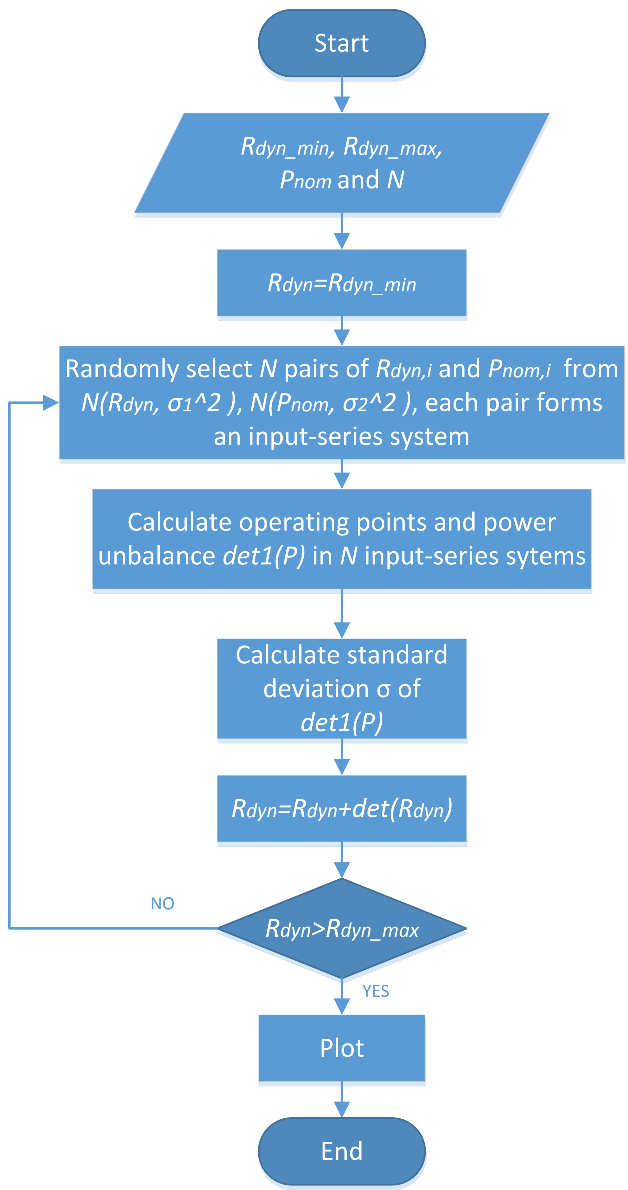


Figure 3-16 *Matlab* calculation flow chart

A flowchart in Figure 3-16 helps to explain the detailed procedure. R_{dyn}, whose reciprocal indicates the slope of the input curve, is regarded as the single independent variable and will step from R_{dyn_min} to R_{dyn_max} with a fixed step $det(R_{dyn})$. At each R_{dyn}, a statistical calculation is carried out to analyze the power balancing performance.

A *Matlab* program will generate N pairs of $R_{dyn,i}$ and $P_{nom,i}$ values from their normal distributions and as a result, N input-series systems for statistical purpose are formed. In each input-series system, their operation points can be calculated mathematically according to Eq. 3-47 to 3-50. The power balancing performance of two converters will be statistically analyzed. The power unbalance $\Delta_1 P$ is defined as,

$$\Delta_1 P = \frac{2(P_1 - P_2)}{P_1 + P_2} \times 100\% \qquad \text{Eq. 3- 53}$$

The following figure shows the *Matlab* plot of $\sigma(\Delta_1 P)$ as a function of dynamic resistance R_{dyn}.

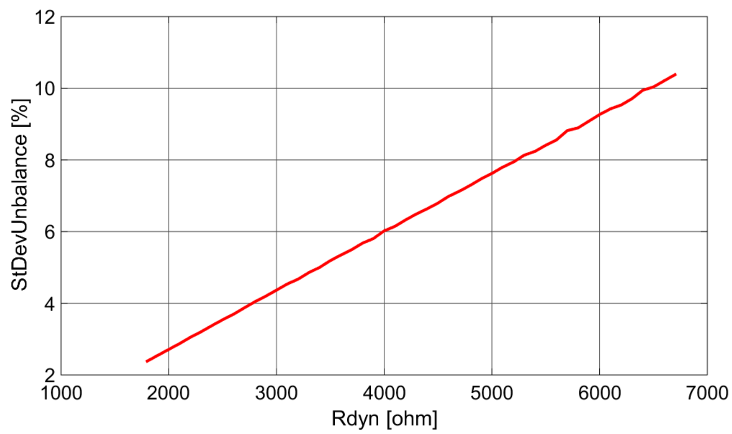


Figure 3-17 *Matlab* simulation: power unbalance

It is observed that as R_{dyn} increases, the power unbalance $\Delta_1 P$ is more scattered with a larger standard deviation from statistical point of view.

2) Power regulation: V_{mns}

Another external factor that will influence the converter power is the input voltage. In practice, a $\pm 15\%$ tolerance on input voltage is always realistic. However, the power in an open-loop converter is not regulated and vulnerable to input voltage variation.

$$v_{in,sys}(\theta) = \sqrt{2} V_{mns} \sin\theta \qquad \text{Eq. 3- 54}$$

The flowchart in Figure 3-16 can be modified to study the power regulation performance at different R_{dyn}. Here instead, a normal distribution is assumed on input V_{mns} while converters remain identical to each other.

Power regulation performance is evaluated on another criteria $\Delta_2 P$ defined as,

$$\Delta_2 P = \frac{(P-P_{nom})}{P_{nom}} \times 100\% \qquad \text{Eq. 3- 55}$$

Again, *Matlab* simulation results are plotted showing $\sigma(\Delta_2 P)$ as a function of dynamic resistance R_{dyn}.

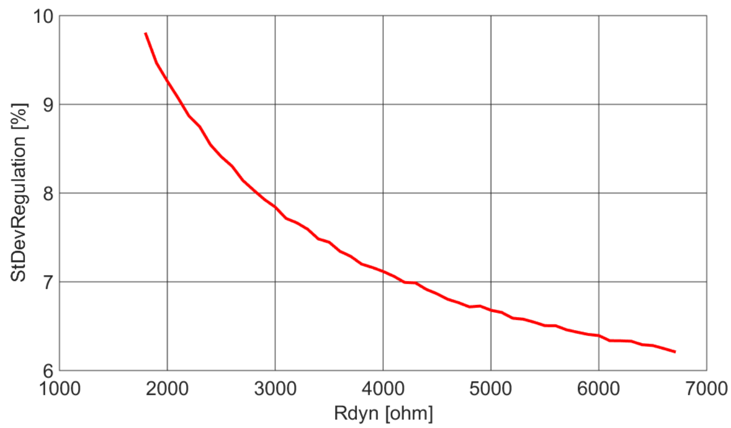


Figure 3-18 *Matlab* simulation: power regulation

It can be concluded from Figure 3-18, the power is less influenced by input voltage when R_{dyn} is at a larger value.

3.3.3 Explanation

Matlab simulation results show the opposite trends on how power balancing and power regulation change with R_{dyn}. Previously it is mentioned that two coefficients are mutually dependent: if coefficient a increases, b has to decrease in order to maintain the same output.

There are basic correlations between coefficients a, b and the shape of input curves. A flatter curve, as a result of smaller a and larger b will be favorable in order to better maintain a constant power. On the contrary, a steeper curve resulting from larger a and smaller b is preferable to minimize the power unbalance between two converters. Explanations are followed below.

1. Power balance

The input characteristics become flatter as a result of smaller a and an increase in power unbalance is observed for the same tolerance. To explain, the converter will have more flexibility in moving along the curve and adapting to the mismatch if the input characteristic has a steeper slope. On the contrary, the operating point is bounded to a smaller region which gives little possibility for adjustment. Therefore, a larger coefficient a is preferable in consideration of minimum power unbalance and output current unbalance.

2. Power regulation

A larger coefficient b greatly influences power regulation performance and then line regulation performance if the output voltage only varies gradually. Line regulation is defined as the capability to maintain a constant output current/voltage in response to input changes [34]. Mathematically, it is defined as,

$$\%Line\ regulation = \frac{(I_o - I_{o,nom})}{I_{o,nom}} \times 100\% \qquad \text{Eq. 3- 56}$$

Line regulation is always an issue for most open-loop power supplies since the controller is not regulating the output at all. In the proposed control scheme, for instance, the peak current reference is preset to obtain the nominal output current at nominal input voltage. The AC component in the current reference comes from the input voltage and is proportional to the input voltage at any time. It increases when the input voltage increases, which will be finally translated into a higher current and a higher power. However, the DC component will remain constant no matter how the input voltage changes.

3. Total harmonic distortion

Total harmonic distortion mainly comes from the interaction with EMI filter, non-ideal operations near zero-crossing points and most importantly, the basic operation of that topology.

An application note [35] presents a theoretical analysis on total harmonic distortion of a high PF flyback PFC converter. The flyback PFC converter is implemented with a constant ON-time control strategy and has a sinusoidal peak current envelope for secondary current as well. However, as illustrated in Figure 3-19, the primary current is triangular-shaped and it only flows during the on-time.

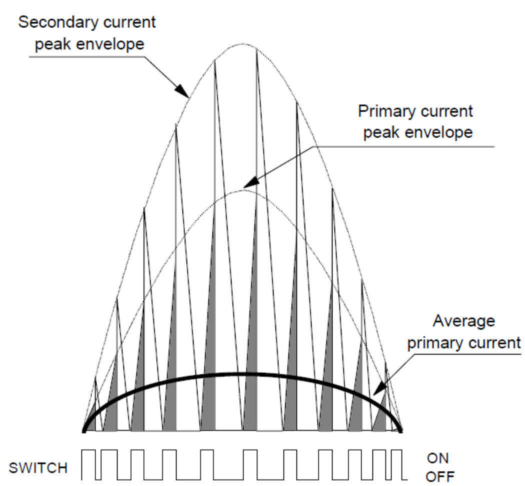


Figure 3-19 High PF flyback current waveforms [35]

The average primary current is the average value of each shaded triangle over the high-frequency switching cycle.

$$I_{in}(\theta) = \frac{I_{L,pk}|\sin\theta|}{2(1+K_v|\sin\theta|)} \quad \text{Eq. 3- 57}$$

K_v is the ratio between the peak input voltage V_{pk} and the reflected voltage of the flyback converter (or V_o for buck-boost converter).

$$K_v = \frac{V_{pk}}{V_o} \quad \text{Eq. 3- 58}$$

The line current before the rectifier bridge is plotted for different K_v. The EMI filter filters out the high-frequency ripple so only low-frequency component can be seen by the mains.

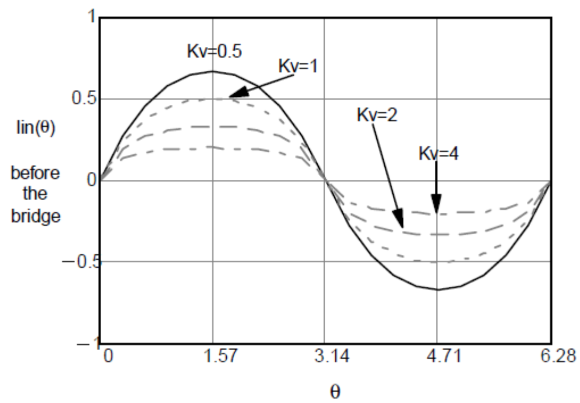


Figure 3-20 High PF fly-back PFC line current [35]

The line current will be sinusoidal for $K_v = 0$ which requires an infinite output voltage and it is not realistic. The current waveform starts to distort from a sinusoidal shape when K_v increases. Thus, flyback topology (or buck-boost topology) does not permit a non-distorted input current, unlike boost topology.

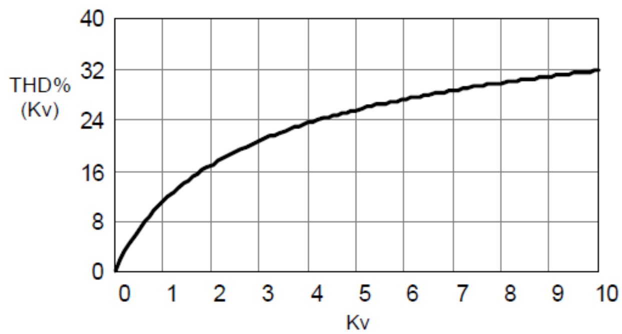


Figure 3-21 THD% as a function of K_v [35]

In addition, current distortion is partly due to the non-ideal operation near zero-crossings and it can be more or less impacted by setting different coefficients. A larger coefficient b sets a higher DC offset in current reference. Therefore, at zero-crossing points where the AC component is zero, a higher DC offset will distort the current from sinusoid.

However, THD cannot be calculated in *Matlab* with the simplified input curve but will be further explored with *LTSpice* simulation and prototype experiments.

3.4 Summary

In this chapter, a modulated peak current controlled buck-boost self-oscillating converter is proposed to realize stable operation of an input-series system. It is considered as an open-loop based solution since converter output current is not regulated via a feedback loop.

The proposed control strategy follows a simple control equation, which sets the inductor current reference with two coefficients a and b. Stability condition is derived mathematically and should be fulfilled as priority. A basic circuit implementation based on discrete components is also presented and explained.

The control equation is also analyzed in detail. Two coefficients a and b determine the dynamic AC part that varies with real-time input voltage and the static DC offset that remains constant in current reference, respectively. Many pairs of coefficients are available to achieve the same output while maintaining the stability condition satisfied. Their effect on circuit performance is investigated with *Matlab* simulation to provide some design hints.

Chapter 4 Principle Verification: Modulated Peak Current Control

In this section, the control method for stable input-series operation will be examined with both simulation software *LTSpice* and prototypes. The converters are built with discrete components on basis of the schematic shown in section 3.2.2. As an open-loop solution, the effect of component tolerances is also studied.

4.1 EM-ballast and LED Load Modeling

Two electro-magnetic ballasts, for independent and series modes respectively, are specified as reference ballasts for design and verification phase. LED load arrangement is also already defined for this application. The electro-magnetic ballasts and LED load are first modeled with electrical parameters, which will be applied in simulation.

1. LED load

The LED load specified for this application consists of 64 low-power LEDs. They are arranged in two parallel strings, each of which has 32 LEDs in series.

To represent the load behaviors in simulation, the LED load is characterized by the forward voltage V_F and its dynamic on-resistance R_{dyn_LED}, which are two general parameters for LEDs.

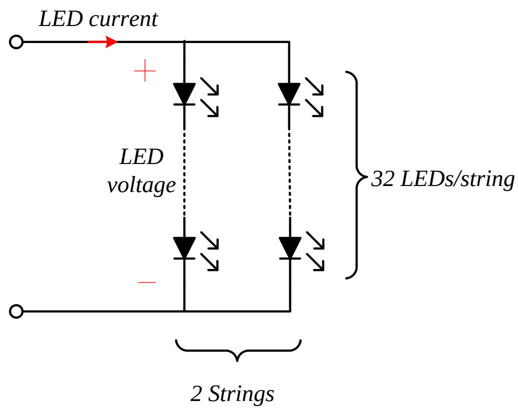


Figure 4-1 LED load arrangement

To obtain the load characteristics, two LED loads that will be used in the test are connected to a current source, separately. As the current increases from 45mA to 95mA, LED voltage is measured with a voltage-meter at every 10mA. LED current and voltage are measured at two ports of the load. Below are the measured LED load I-V curves.

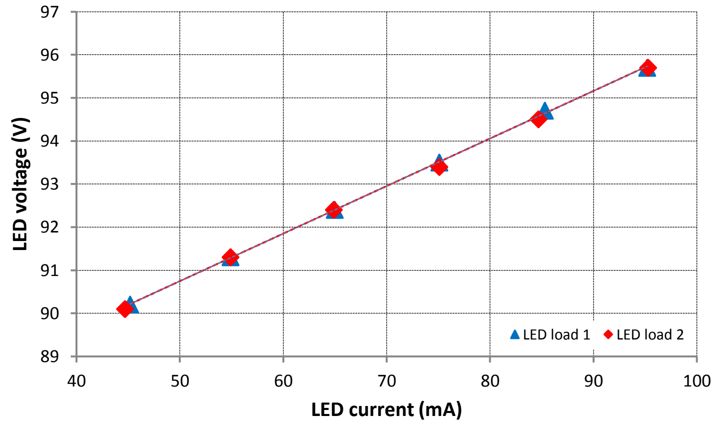


Figure 4-2 Measured LED load characteristic

The resulting I-V curves are then fitted into linear equations, which are quite close to each other with a fitting coefficient $R^2 > 0.999$. Taking an average, the LED load is described in the form of Eq. 4-1.

$$V_{LED} = R_{dyn} I_{LED} + V_F \qquad \text{Eq. 4- 1}$$

It should be noted that mismatch in between two LED strings are not considered.

2. Electro-magnetic ballast

Each ballast is rated with a specific power and should be used with lamps at the same power level. Depending on the manufacturers, the electro-magnetic ballast for 2ft fluorescent lamps vary from one to another in electrical parameters. To facilitate the design procedure, there are two reference ballasts that are used for series- or independent-mode. An inductive ballast can be represented with an inductance and a series resistance. The modeling procedure of the reference ballast for two-lamp mode is presented.

Modeling is carried out in accordance with the operating conditions: V_{mns} and f.

$$V_{mns} = 230V \qquad \text{Eq. 4- 2}$$

$$f = 50Hz \qquad \text{Eq. 4- 3}$$

The ballast is directly connected to an AC voltage source described by Eq. 4-2 and 4-3. The resulting RMS current I can be measured.

Neglecting the AC resistance R_{ac}, the impedance can be calculated.

$$Z = \frac{V_{mns}}{I} = \sqrt{R^2 + (2\pi f L)^2} \qquad \text{Eq. 4- 4}$$

The resistance can be measured with a multi-meter. The inductance is therefore calculated,

$$L = \frac{\sqrt{(\frac{V_{mns}}{I})^2 - R^2}}{2\pi f} \quad \text{Eq. 4- 5}$$

In a similar way, the reference ballast for one-lamp independent operation is also modeled. These electrical models of reference electro-magnetic ballast will be used in simulation later on.

Reference EM ballast	Operation mode	L/H	R/Ω
TRIDONIC EC36 LC502K	Series	1.4	40
MST BTA	Independent	1.7	41

Table 4-1 Reference EM ballast electrical models

4.2 Simulation Results

LTSpice is a simulation tool for electrical circuit analysis and is used to verify the proposed circuit for stable-series operation.

In *LTSpice*, several input-series systems are built for evaluation based on the schematic in Figure 3-11. Four different control options (correspond to different coefficient pairs) are selected for a same output current at 72mA, which are numbered from #1 to #4. Control option #1 has a pure AC current reference while #2 and #3 have a portion of DC offset in their reference settings. Control option #4 represents the regular peak current control, whose inductor current reference is a pure DC value.

The coefficient settings for each control option are summarized in the following table.

Control Option	Coefficient a	Coefficient b
#1	0.0025	0
#2	0.0020	0.0601
#3	0.0015	0.1121
#4	0	0.3052

Table 4-2 Coefficients for #1-4 control options

Four control options are all capable to deliver the desired output current working independently at half nominal input voltage. Their input I-V curves are plotted based on mathematical calculations. A reasonable assumption on delay time is also incorporated in calculation.

As the DC offset in current reference increases, the I-V curves tend to be flatter. Especially, the DC offset in control option #3 is so significant that part of the input characteristic is close to a flat line, which approaches the boundary for stability. Control option #4, the regular peak current control, has a negative dynamic input resistance.

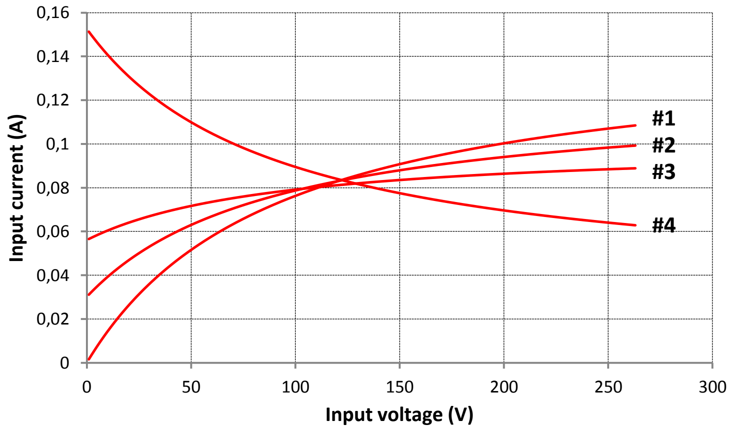


Figure 4-3 Input curves: different I_{pk} control options

4.2.1 Input-series System Verification

In each input-series system, two identical converters of the same control option are connected in series to nominal input voltage. These systems are simulated in *LTSpice* to verify the basic operating principle and stability. All simulations are without ballast unless mentioned otherwise.

1. System stability

A sinusoidal input voltage is applied to the system and it implies a periodical disturbance that is introduced. System stability can be concluded if input voltage is always shared by two constituent modules with a constant ratio and no voltage runaway phenomenon takes place. Simulation results for all four input-series systems are summarized in the following table.

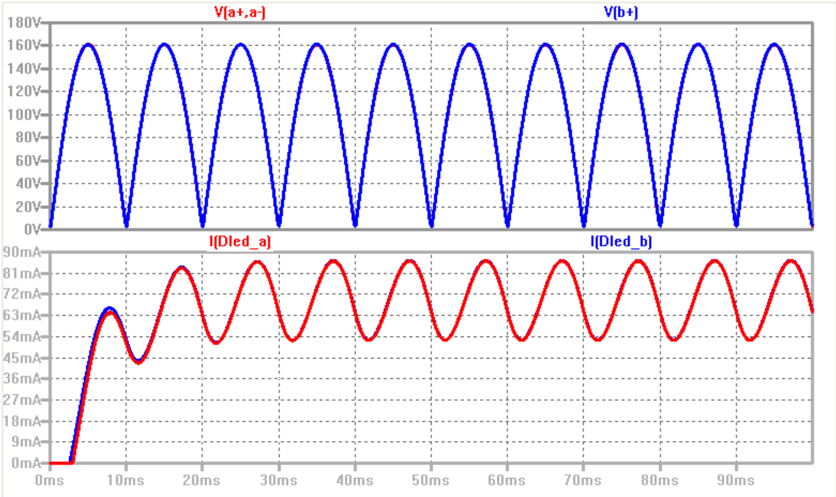
Input-series System Control option	**Stability (Yes: ✓, No: ✗)**	**Simulation Output Current /mA**	
		Lamp1	**Lamp2**
#1	✓	70.30	70.30
#2	✓	70.87	70.87
#3	✓	70.28	70.28
#4	✗	--	--

Table 4-3 Simulation results: stability verification

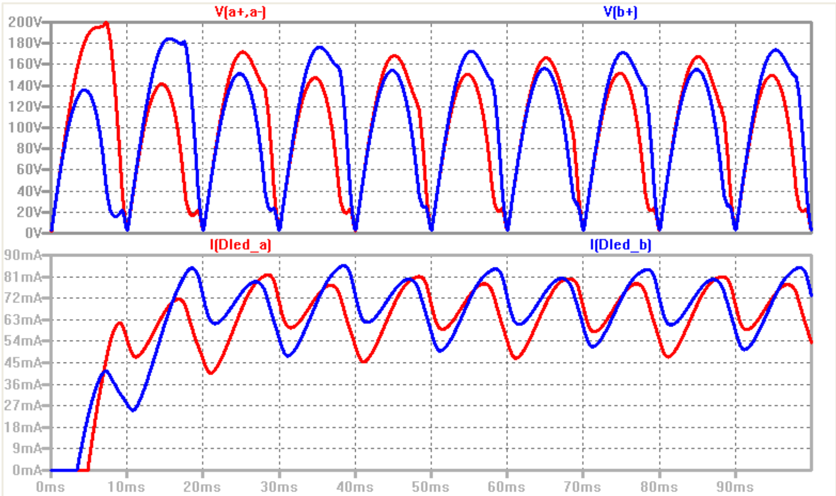
Simulations show that all input-series systems except #4 are stable from IVS point of view. In addition, the output current is also well controlled. The input-series system based on control option #4 is not stable since the input voltage tends to drift to one driver, indicating risks of voltage runway.

The input voltage sharing performance of a stable and an instable system is compared in Figure 4-4. The input nodes of two identical converters (downstream the rectifier bridge) are denoted with a_+,

a_-, $b_+$and b_- while the negative node b_- is taken as the ground reference of the system. Their corresponding input voltages and output currents are plotted, respectively.



(a) A stable system: control option #2



(b) An instable system: control option #4

Figure 4-4 Simulation results: IVS and output current waveforms

Figure 4-4(a) is the waveform of a stable system (based on control option #2). The total input voltage is evenly shared, each converter taking exactly half mains input voltage. The overlapping output current waveforms also tell that the output currents are well balanced. Therefore, the system is stable and two constituent converters are well in balance in terms of input voltage sharing. The same is true for control option #1 and #3. Figure 4-4(b) shows the waveform of an instable system (based on control option #4). The input voltage is distributed with a quite arbitrary ratio.

The simulation results can already be foreseen from the input curves plotted in Figure 4-3. By setting appropriate coefficient pairs, the input current I_{in} of control option #1, #2 and #3 is all made monotonous increasing function of V_{in}, which is critical for system stability. The input current of control option #4, on the contrary, is a monotonous decreasing functions of V_{in}. As discussed before, the negative dynamic input resistance is detrimental to system stability in input-series-connected system. It is observed in simulation that voltage runway phenomenon or sometimes extremely uneven voltage sharing occurs.

2. Operation waveforms

Circuit operation details are available in *LTSpice* simulation for validation of control implementation. All the waveforms are captured from the input-series system based on control option #2.

The fundamental operation principles are also verified in detail. The modulated-peak-current controller is implemented in such a way that the power switch is turned off once the peak inductor current reaches the reference. The output current is therefore controllable by actively setting the current reference at a proper value.

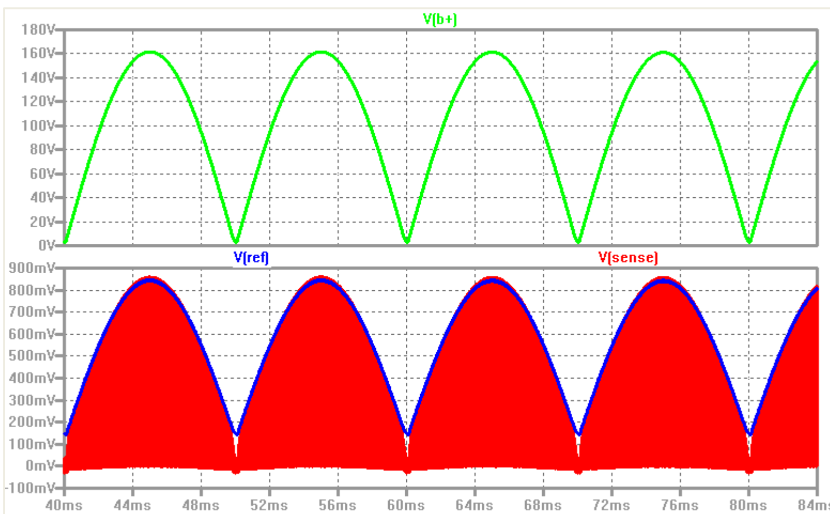


Figure 4-5 Simulation waveforms: driver input voltage and comparator signals

Figure 4-5 plots the rectified driver input voltage ($v_{b_+,GND}$) and two comparator input signals. Inductor peak current reference, which is already translated to a corresponding voltage, is denoted with v_{ref} while the sensed voltage is denoted with v_{sense}. v_{ref} is a smooth rectified sinusoidal voltage with a constant DC offset, whose AC component follows the shape of input voltage. The comparator is functioning well since v_{sense} waveform is enveloped by v_{ref}.

After zoom-in, Figure 4-6 shows detailed switching waveforms of the main power transistor. Inductor current (i_L), transistor collector-emitter voltage (v_{CE}) and transistor base current (i_b) are plotted on the same timeline. Two major findings that are observed in Figure 4-5 and Figure 4-6 are further explained as follows.

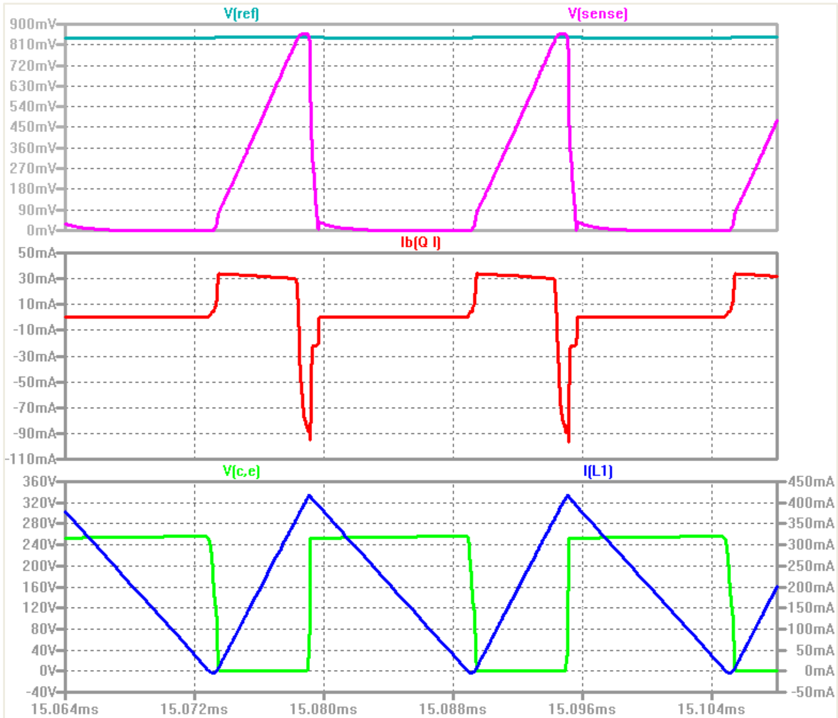


Figure 4-6 Simulation results: power transistor switching waveforms

First of all, the power transistor Q_1 cannot be switched off immediately at the critical instant when $v_{sense} = v_{ref}$. Turn-off process is delayed by the storage time effect of the bipolar transistor since the stored charge needs to be extracted to fully turn off the transistor. Meanwhile, the bipolar transistor is still conducting current and as a result, the inductor current will exceed the reference by a Δi_L . This explains the excessive voltage over the sense resistor.

The storage-time effect becomes more significant near the peak input voltage. When zooming into the switching waveforms near the crest, the delay time can be clearly observed. At the critical time instant when the sensed current reaches the reference current, the controller starts to switch off the transistor and the base current injected into the transistor drops sharply. While the transistor is being switched off, the inductor current continues rising linearly for a time interval Δt. After that, the transistor is fully off. The collector-emitter voltage builds up and inductor current starts to decrease. In Figure 4-6, a delay time of $\Delta t = 858.9ns$ is measured.

Secondly, self-oscillating converters are not able to keep good oscillations near zero-crossing points of the input voltage. The auxiliary winding does not get sufficient energy to maintain the oscillations. The transistor naturally turns off before it reaches the required peak current as shown in Figure 4-5. It is also expected that the non-ideal operation of the self-oscillating converters at those spots will result in a current distortion.

3. EM ballast compatibility

Compatibility with the reference ballast is also proven in *LTSpice*. The ballast electrical model is previously derived and applied in simulation. The following figure shows the input voltage sharing with the EM ballast.

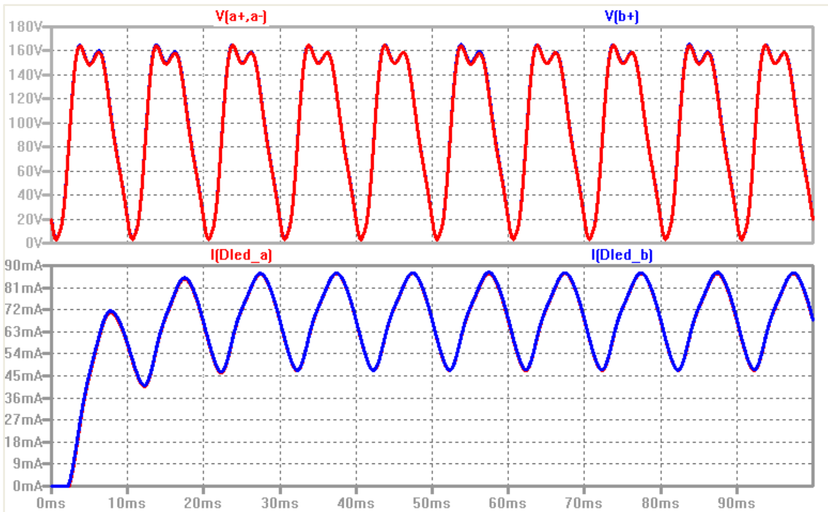


Figure 4-7 Simulation results: IVS and output current waveforms (with EM ballast)

The input voltage is much more distorted, as shown in Figure 4-7. Especially near the crest, a double-voltage-peak is observed due to the inductor induced voltage. However, the superposed peak value is not increased. The output current is also more distorted compared to the simulation without EM ballast.

In steady state, the system is still doing well in input voltage sharing even in presence of the EM ballast in series.

4. Line regulation and THD

Based on ±15% tolerance on mains voltage, the output current is measured at every 5% change of input voltage. The resulting curves on line regulation performance are plotted in the following Figure 4-8.

The output currents show linear dependency on the input voltage for all the three systems. Control option #1 has a pure AC current reference and thus the line regulation performance is the worst. A 15% higher input voltage leads to 23% increase of output current. The second system ends up with 20% higher output current while the output current of the third system increase by 17%. A conclusion is also drawn from both theoretical analysis and simulations that a larger coefficient *b* in the control equation will help to improve line (power) regulation performance.

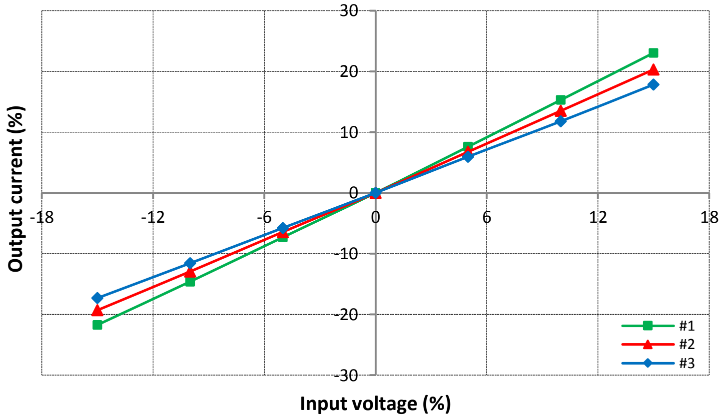


Figure 4-8 Simulation result: line regulation performance

Total harmonic distortion (THD) can also be impacted by setting different coefficients. It is discovered in simulation that a higher DC offset will contribute to a higher THD since the current distortion is partly due to the non-idea operation near the zero-crossings. At those points, the AC component equals to zero and a higher DC offset will further distort the current from a pure sinusoid. The *Fourier* analysis on input current shows that the control option with higher DC reference has a higher THD and a lower power factor.

Control Option	THD/%	Power Factor
#1	11.91	0.976
#2	20.55	0.962
#3	29.02	0.943

Table 4-4 Simulation results: THD and power factor

Therefore, two coefficients will impact the system performance in different ways. They should be tuned to satisfy the design targets and compromise between various technical objectives.

4.2.2 Sensitivity to Component Tolerance

It is preferable to have a balanced input-series system, which means each constituent converter delivers comparable amount of output power/current. Output current is especially important in a lighting system since LED current is directly linked to its light output. Therefore, a key parameter to be studied is the output current unbalance in such a system.

Output current unbalance (in percentage) between the two drivers is defined by the following equation. The signs of unbalance indicates the relative current magnitudes.

$$\%Output\ current\ unbalance\ \Delta I_o = \frac{2(I_{o1}-I_{o2})}{I_{o1}+I_{o2}} \times 100\% \qquad \text{Eq. 4- 6}$$

In reality, all components have certain tolerances on their technical specifications. For instance, the tolerance of a resistor indicates how much it can deviate from the nominal resistance value measured under standard conditions. The same goes for a capacitor, an inductor or a zener diode. The deviation may result from the manufacturing process, temperature change, or different application conditions. Two inductor values may be different since the air-gap length may not be very accurately controlled in the manufacturing process.

The component tolerance is commonly specified in percentage, by which the value can vary, in either direction from the nominal value. Typical tolerances for resistor are 1%, 2%, 5%, 10% and 20%. From statistics perspective, nearly all component values will fall into the tolerance band. The larger the tolerance is, the more it can vary from the stated value. In applications where accuracy is strictly required, it is also possible to use high-precision components with even smaller tolerance but higher cost at the same time.

The tolerances have an impact on system balance in this open-loop input-series system. In case of component mismatch, the input characteristics are no longer identical and will have an impact on input voltage sharing. The following simulation will focus on how sensitive the system is to component tolerances.

The tolerances studied are inductor value L (including L_1 and L_2), LED forward voltage V_{LED}, power supply voltage V_{cc}, and current sense resistor R_s (R_8 in Figure 3-11). Based on general tolerance statistics, the circuit sensitivity to major component variations is studied. Since the system is symmetric, all adjustments are carried out on the same converter.

Simulations are carried out under the conditions that the constituent drivers: 1) have the same control option and are originally identical; 2) have certain tolerance on only one parameter each time. Control option #4 is excluded since the system it constitutes cannot operate stably.

Parameter	**Tolerance (%)**	**Ctrl Option #1**	**Ctrl Option #2**	**Ctrl Option #3**	**Ctrl Option #4**
Identical	0	0	0	0	N/A
$\boldsymbol{L}$	+10	-0.13	-0.19	-0.21	
	-10	+0.58	+0.69	+0.68	
$\boldsymbol{V_{LED}}$	+3	-5.04	-5.58	-7.14	
	-3	+5.18	+5.89	+7.21	
$\boldsymbol{V_{cc}}$	+5	+0.48	-1.41	-4.88	
	-5	-0.61	+1.13	+4.2	
$\boldsymbol{R_s}$	+1	+1.37	+1.87	+2.71	
	-1	-1.44	-2	-2.96	

Table 4-5 Simulation results: component-tolerance-caused ΔI_o(%)

The converter is peak current controlled and hence theoretically, the inductor value will not influence the output current. As long as the turns ratio is correct, the secondary winding is still getting sufficient voltage for self-oscillation. In simulation, a 10% tolerance on inductor value already represents a worst case. A very slight change (<1%) in output current unbalance is observed however. Most likely is that the current overshoot during storage time is dependent on inductor value. It can be concluded that the converter is not sensitive to inductor value at all, and thus in mass production it is possible to choose inductors with higher tolerance and lower costs.

Another important tolerance is the forward voltage of LED load. Among the simulation results, it is also the most significant factor. The LED load is already defined for this application and an average spread of 3% on LED voltage can be expected. The simulation results show that a $\pm3\%$ variation in the LED forward voltage will cause around $\pm5\%$ unbalance in the output currents. The driver with higher LED voltage is getting relatively lower current.

Normally the constant voltage V_{cc} is supplied by the auxiliary winding, which is coupled to the main inductor. It provides the DC offset via a voltage divider when necessary and also serves as the power supply for the comparator to function. When it is only used to power the comparator, a large series resistor makes it a current source and thus $\pm5\%$ voltage variation can hardly affect the output balance as in control option #3. The output current will be affected when V_{cc} is also setting the DC component in current reference. In that case (control option #2 and #3), the inductor peak current reference varies with V_{cc} and leads to mismatch in output current. A more significant influence is observed when a larger DC component is present.

Current sense resistor R_s is placed at the collector of main switch to sense the inductor current. The voltage over series resistor generates one input signal of the comparator to compare with the reference voltage. The precision of R_s will determine how well the real inductor current tracks the reference. In general, a 1% variation in sense resistor will bring 2~3% extra output unbalance. A high precision sense resistor is necessary in an open-loop regulated converter for control accuracy.

The simulation also confirms how the coefficient setting affects the circuit sensitivity to component mismatch. The input characteristics become flatter from control option #1 to #3 (as a result of smaller a) and an increase in output unbalance is observed for the same component tolerance. For instance, the output unbalance caused by LED forward voltage in control option #3 is almost 1.5 times than control option #1. *LTSpice* simulation results are well in consistence with the *Matlab* simulation results that are calculated on the simplified input characteristics.

4.3 Prototype Experiments

Two ‘driver prototypes are assembled on general PCB boards, the implementation of which is based on the second control option. The prototypes are first individually tested at half nominal input voltage as if in ideal input voltage sharing condition. Both drivers function well and deliver almost the same amount of output current (~73mA). The measured driver efficiency is (~88%) for both.

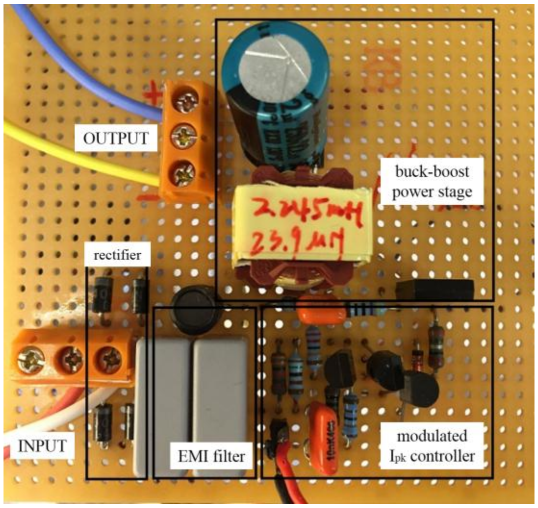


Figure 4-9 Prototype for principle verification

They are deemed as ‘identical’ since each component has the same stated value although the real values may differ due to component tolerance. Although a slight output current unbalance (~2.6%) is still present in the following input-series test, these two drivers are considered as ‘identical’ and serve as the reference origin through the entire experiment. All experimental results are without EM ballast unless mentioned otherwise.

4.3.1 Input-series System Performance

1. System stability

Two prototypes are connected in series and powered up at nominal input voltage. Measurements are repeated with and without EM ballast.

Parameters	Without EM ballast	With EM ballast
V_{in_rms} /V	230.1	230.1
I_{in_rms} /mA	69.5	68.2
P_{in}/W	15.4	15.2
PF	0.962	0.973
I_{thd1}/%	19.8	23.1
I_{o1} /mA	73.6	71.7
I_{o2}/mA	71.7	69.9
ΔI_o/%	+2.62	+2.54

Table 4-6 Input-series system measurement results

The series system shows stability over the full operating range. The input voltage waveforms are shown in Figure 4-10. The transient DC component that is observed in the waveform comes from the start-up of the power supply and it disappears after 4 to 5 mains cycles. The overlapping waveforms of channel 1 and 2 show that the system input voltage is evenly shared by the drivers during either start-up or steady state.

In an input-series connected system, a good input voltage sharing is also the prerequisite for a well-balanced power in LED loads from the perspective of power conservation.

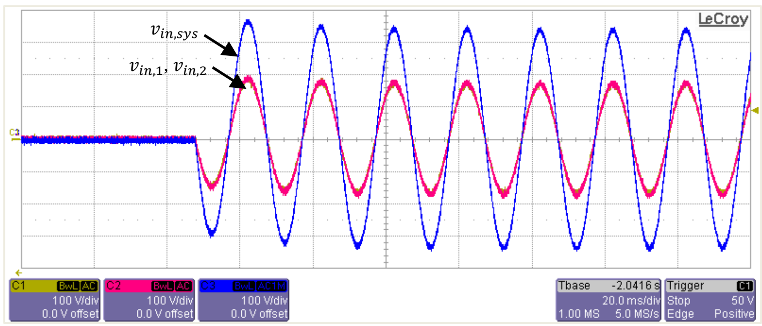


Figure 4-10 Input voltage sharing waveforms

Output current waveform is shown in Figure 4-11, which has 100Hz ripple. The measured peak-to-average current ripple is 26%.

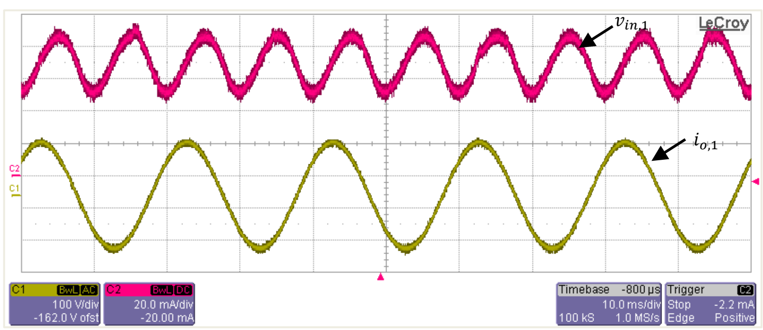
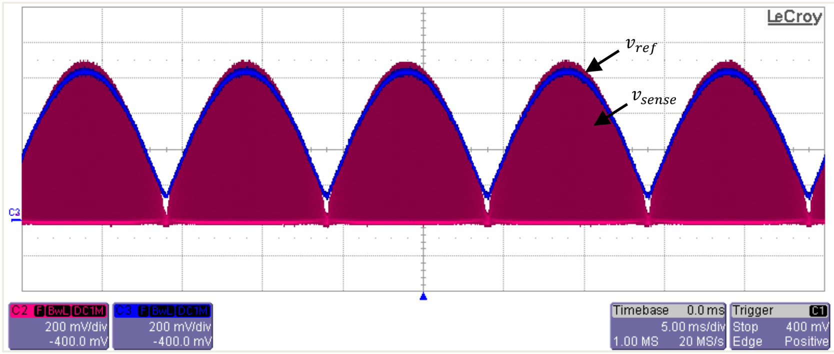


Figure 4-11 Input voltage and output current waveforms

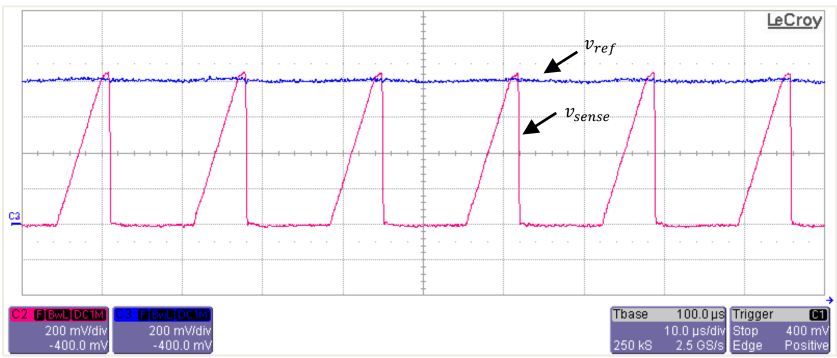
2. Operation waveforms

Figure 4-12 shows the waveforms of reference voltage v_{ref} and sense resistor voltage v_{sense}. The waveforms match up with simulations quite well. Over the mains cycle, the inductor peak current is controlled by the reference current. Besides, the same non-ideal phenomena that show up in simulation are also observed in experiments due to the insufficient energy of the auxiliary winding at those intervals. The blanking area is where the oscillations are not well maintained.

Figure 4-12(b) is the zoomed waveform around the crest. The slope of v_{sense} changes suddenly because transistor Q_4 is taking action to turn off Q_1 at that time. After a small time interval, the transistor is fully switched off. The sense resistor voltage falls to zero.



(a) Comparator inputs



(b) Zoomed-in waveforms

Figure 4-12 Comparator input signals

Figure 4-13 illustrates the switching waveforms of the power transistor Q_1. Once the controller starts to turn off the transistor, the base current will decrease dramatically as the charge stored in Q_1 is being extracted by transistor Q_4. Q_4 generates a negative peak in base current, which is helpful in accelerating the turn-off process.

The total delay time measured is $1\mu s$ in Figure 4-13, which allows excess current flowing through the inductor.

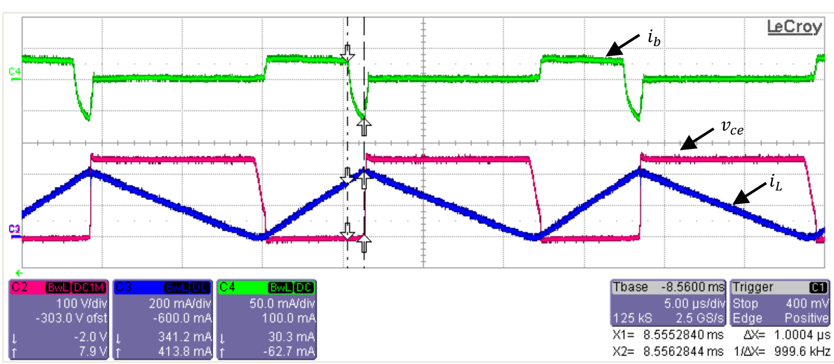


Figure 4-13 Switching waveforms: power transistor Q_1

3. EM ballast compatibility

The driver is also compatible with the reference electro-magnetic ballast specified for the design. The driver input voltage is distorted from a sinusoidal waveform due to the significant inductance of the ballast. Especially during the first mains cycle, oscillations are observed due to the interactions between EMI filter and the EM ballast as analyzed. However, the voltage sharing is still satisfying.

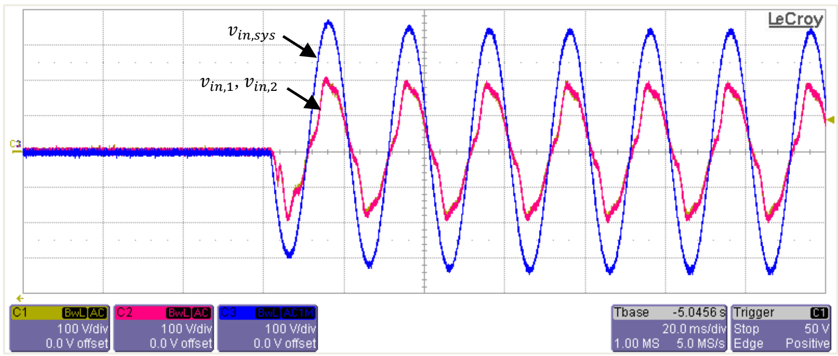


Figure 4-14 Input voltage sharing waveforms (with EM ballast)

4. Line regulation and THD

Line regulation performance is also measured with prototypes. A $\pm 15\%$ variation in input voltage is taken into consideration. All measurements are carried out in steady operation states. Line regulation is calculated with regard to the nominal output current measured at nominal input voltage.

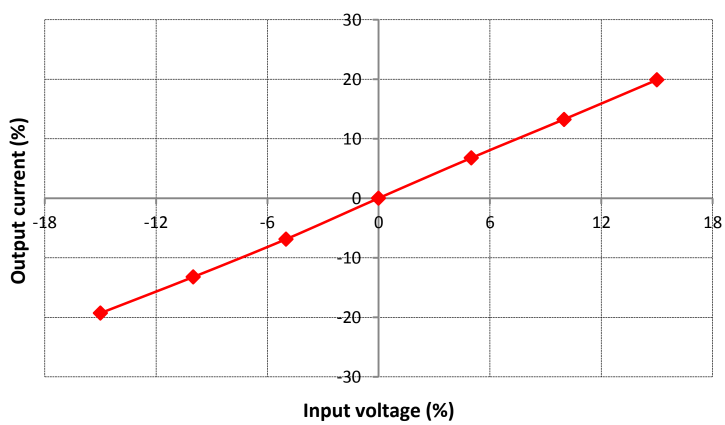


Figure 4-15 Prototypes: line regulation performance

It shows that output current is linearly dependent on the input voltage. When input voltage varies by $\pm 15\%$, output current will vary from the nominal output current by approximately $\pm 20\%$, which is also consistent with simulation results in Figure 4-8.

Since output current is not tightly regulated by a feedback loop, it is sensitive to input voltage variation. It is an intrinsic property of an open-loop converter if no extra modulation is performed to alleviate. However, the output current (directly linked to output light) of the two drivers will increase or decrease simultaneously and therefore the balance of the output currents will not be affected.

Total harmonic distortion measured without EM ballast is 19.8% and increases to 23.1% if measured with EM ballast. As expected, the current waveform is further distorted as an interaction with the dominating inductance in the ballast.

4.3.2 Circuit Sensitivity Test

The circuit sensitivity to component tolerance is investigated with the prototypes. The relevant parameters are changed accordingly to explore their influence on output current unbalance. The evaluated parameters includes inductance value L (L_1 and L_2 included), LED forward voltage V_{LED}, temperature T and transistor storage time t_s.

Inductance value L and LED forward voltage V_{LED} can be changed easily in simulation setting. Their effects have been explored in Chapter 4 with simulation tools. Temperature will mainly influence the properties of semiconductor devices like diode and transistors, which cannot be modeled accurately and comprehensively with electrical parameters. Transistor storage time t_s is also difficult to model in principle since it is determined by multiple factors. Hence, it is preferable to investigate their impact in experiments.

Instead of the fact how much the exact values deviate from the nominal value, it is greater concern to know how much they deviate from each other and how it will be translated to unbalance in output current. The unbalance of a parameter X is defined similarly to output current unbalance, which will be used as the independent variable in the following analysis.

$$\%Parameter\ unbalance\ \Delta X = \frac{2(X_1 - X_2)}{X_1 + X_2} \times 100\% \qquad \text{Eq. 4- 7}$$

1） Inductance value L

The tolerance of inductor value in production is mainly due to the air-gap length accuracy. Typical inductance tolerances are 5%, 10% and 20%.

Two inductors are built for the prototypes and inductance is changeable by expanding or shrinking the air-gap. Generally, $\pm 10\%$ is a practical tolerance on inductance. Seven different combinations that may occur are checked in experiments. The cases where both inductances are 10 percent higher or lower are excluded since they are in fact making no change at all. During every measurement, it is also ensured that the inductor is not saturated by monitoring the current waveforms.

The output currents in the following table are measured in mA. The percentage $\pm 10\%$ is for indication only. A more accurate ΔL is repetitively calculated for each combination with measured inductances.

Driver #1 Driver #2	+10%	0	-10%
+10%	N/A	73.5 71.6	73.6 71.6
0	73.6 71.7	73.6 71.7	73.7 71.5
-10%	73.7 71.6	73.5 71.7	N/A

Table 4-7 Sensitivity measurements: inductance value ΔL

The output current unbalance is calculated on the basis of experimental measurements and plotted with regard to inductance value unbalance. Simulations results are also plotted in the same figure for comparison.

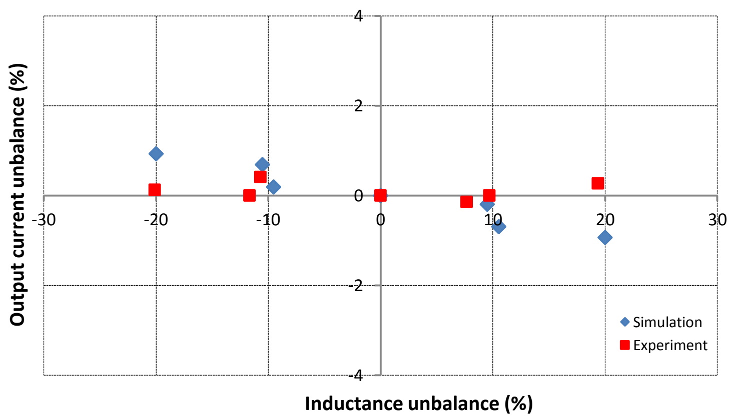


Figure 4-16 Sensitivity plot: inductance value ΔL

The simulation result is symmetric since all other components are strictly kept identical. The experimental results will involve more complicate interactions. Both results show that the driver is hardly affected by the inductor value, which matches the theoretical analysis very well. When both inductors remain unchanged, the original output current unbalance is +2.62%. Take this position as the new 'origin', all data points in the other six combinations fluctuates around the x-axis. Even the influence in the worst cases ($\Delta L = 20\%$) is very slight. It is an important attribute of this control strategy since it doesn't strictly require a precise inductance to guarantee balanced output current.

2） LED load voltage V_{LED}

It is shown in simulation results that the system is very sensitive to the unbalance in LED voltage. The unbalance in LED voltage will be doubled in output current unbalance. The LED load in this application is already specified and a tolerance of $\pm 3\%$ is given.

The LED voltage is changed by shorting or adding one LED in the string, which will bring approximately $\pm 3\%$ variation as needed. Similarly, the percentages in the following table is for indication only. The voltage over the LED string and the LED current are measured respectively. The output currents are measured in mA.

Driver #1 / **Driver #2**	**+3%**	**0**	**-3%**
+3%	N/A	75.3 68.8	78.0 67.3
0	70.7 73.5	73.6 71.7	76.2 70.3
-3%	69.2 72.1	72.0 74.5	N/A

Table 4-8 Sensitivity measurements: LED forward voltage ΔV_{LED}

The curve is again translated so that the origin represents both LED loads are not changed. The simulation results are plotted as well after they are re-calculated accordingly.

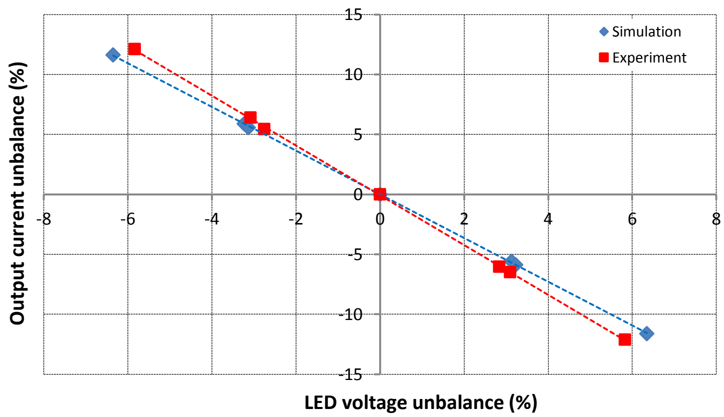


Figure 4-17 Sensitivity plot: LED forward voltage ΔV_{LED}

It is observed that the output current unbalance is linearly dependent on LED voltage unbalance. The curve is fitted into a linear function that has $R^2 > 0.999$.

$$\Delta I_o = -2.08 \Delta V_{LED} \qquad \text{Eq. 4- 8}$$

It is possible to reduce the standard deviation σ of LED voltage by arranging the LED load. If more LEDs are connected in series, less variation in LED voltage is acquired since the deviation on single LEDs will compensate each other. The current LED load has 32 LEDs in series and 2 strings in parallel. However, considering the system cost, it is already the best load arrangement. Otherwise an even higher voltage will be imposed on the transistor and a transistor at higher voltage rating is needed.

3） Transistor storage time t_s

The storage time of a transistor cannot be precisely modeled in simulation because it is determined by a lot of factors. Therefore the effect on output unbalance is mainly investigated in experiments. The definition of storage time is from 90% decrease of base current I_b until 90% decrease of collector current I_c, as shown in Figure 4-18. This definition is adopted by a majority of BJT manufactures in their specifications.

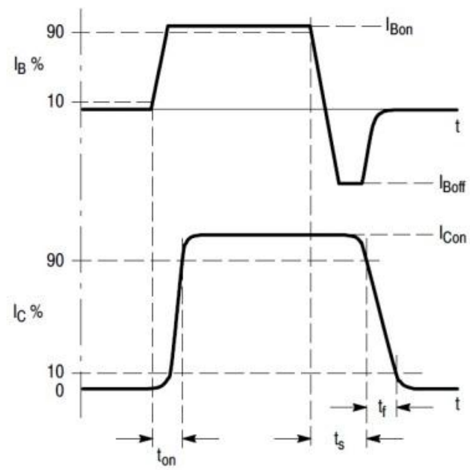


Figure 4-18 Storage time t_s definition

Four BJTs from same manufacturer with the same part number but different storage time are used to investigate the effect of storage time. The storage time of each BJT is measured in the same operating condition in driver #2, which is connected to half mains voltage assuming ideal series operation condition. The storage time is measured according to the definition in Figure 4-18 on the oscilloscope.

The stated storage time on datasheets and measured storage time are both listed in Table 4-9.

BJT	Measured Storage time /μs	Stated Storage time /μs
#1	1.065	1.5~2.0
#2	1.136	1.5~2.0
#3	1.230	2.0~2.5
#4	1.310	2.5~3.0

Table 4-9 Stated and measured storage time

In total, 12 combinations with four BJTs are tested with two prototypes. All measurements are all carried out in steady states and the corresponding output current unbalances are calculated.

Driver #1 Driver #2	BJT #1	BJT #2	BJT #3	BJT #4
BJT #1	N/A	73.5 71.5	73.1 73.0	72.7 73.9
BJT #2	74.4 70.5	N/A	74.0 72.7	73.7 73.7
BJT #3	76.0 70.2	75.9 71.0	N/A	75.3 73.3
BJT #4	77.0 69.9	76.9 70.6	76.5 72.0	N/A

Table 4-10 Sensitivity measurements: storage time Δt_s

The storage time unbalance is distributed in a symmetric way. A mid-point on that segment is thus taken as the new origin to exclude influence of other irrelevant factors. The adjusted curve is plotted in Figure 4-19 where storage time is the single variable.

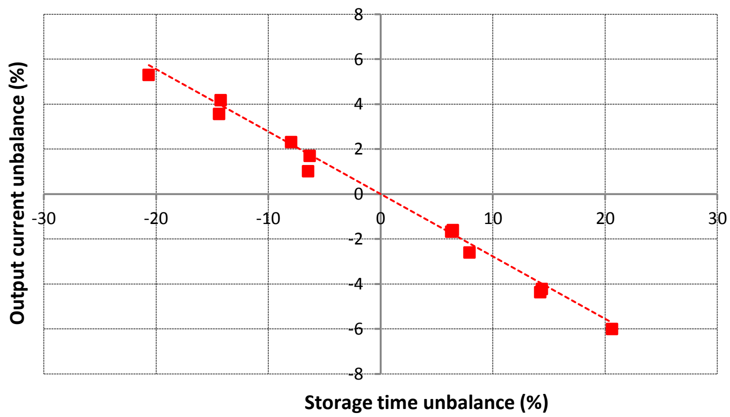


Figure 4-19 Sensitivity plot: storage time Δt_s

Storage time also appears to have a linear influence on the output current unbalance. Experimental results show that a 20% unbalance in transistor storage time will roughly lead to 6% current unbalance at the output. The correlation is fitted into a linear function with a fitting coefficient of $R^2 > 0.98$.

$$\Delta I = -0.28\Delta t_s \quad \text{Eq. 4- 9}$$

Normally, a datasheet only specifies a t_s range in a standard test condition. In a different operating condition, somehow, the range can be narrowed. The BJTs under test have a relatively wide stated range in storage time but result in not that much difference in measured value. For instance, BJT#1 and #4 are specified with a storage time of $1.5\sim2.0\mu s$ and $2.5\sim3.0\mu s$, respectively. However, the measured storage times only increase from $1.065\mu s$ to $1.310\mu s$ by 23%. In this sense, a practical distribution based on specific operation condition is more useful to evaluate circuit sensitivity but not yet available in most cases.

4） Ambient temperature T

Most semiconductor devices are sensitive to temperature change. The temperature dependence of bipolar transistors are is to multiple parameters that affect the semiconductor properties. There have been a lot of researches [36] [37] [38] demonstrating the temperature dependence of current gain β, base-emitter voltage V_{BE}, inverse current I_{CBO} and I_{CEO} and storage time t_s. *Ebers-Moll* equation that describes the transistor model is,

$$I_c = I_s(e^{\frac{qV_{BE}}{KT}}) \qquad \text{Eq. 4- 10}$$

I_s is the reverse saturation current. It seems from Eq. 4-10 that V_{BE} has a positive temperature coefficient. However, I_s is also temperature dependent. The overall temperature dependence of V_{BE} is around $-2.1mV/$℃ [39] [40].

I_{CBO} is due to the minority carriers and hence very much sensitive to temperature change. It increases dramatically as the temperature goes up. A rule of thumb is that I_{CBO} is doubled for every 10℃ increase in temperature [41]. I_{CEO} is also temperature dependent in that,

$$I_{CEO} = (1 + \beta_{DC})I_{CBO} \qquad \text{Eq. 4- 11}$$

Due to the increased number of electro-hole pairs at elevated temperature, β increases with temperature [41]. Transistor storage time is also influenced by temperature change.

There are in total four bipolar transistors in this configuration, including an NPN power transistor in the power stage, two PNP transistor in the comparator and one NPN transistor that helps to turn off the power transistor. The overall effect of temperature is examined with prototypes at the worst case. The highest ambient temperature to be checked is 50℃ as the worst condition in application. A lab-use oven is used to obtain the high ambient temperature. The internal ambient of the oven is heated up to the required temperature by hot air blower. However, the air convection may unexpectedly cool down the driver. Thus, the driver is placed in a plastic container sealed with tapes. A thermo-couple is positioned close to the driver in the same container to monitor the ambient temperature for accuracy.

To check the temperature dependence, one driver is put in higher temperature (50℃) while the other in room temperature (23.5℃). The output current is measured after a sufficiently long time until a thermal steady-state is observed. The experimental results are filled in the following table. The unit of current measurements shown is mA.

Driver #1 **Driver #2**	**50℃**	**23.5℃**
50℃	N/A	73.5 71.4
23.5℃	73.3 71.9	73. 4 71.7

Table 4-11 Sensitivity measurements: temperature ΔT

The overall effect turs out to be that the driver which is put in the high ambient temperature has a slightly decreased output current than its original value. The output unbalance for each configuration is calculated. The curve is corrected as well to exclude other co-existing factors.

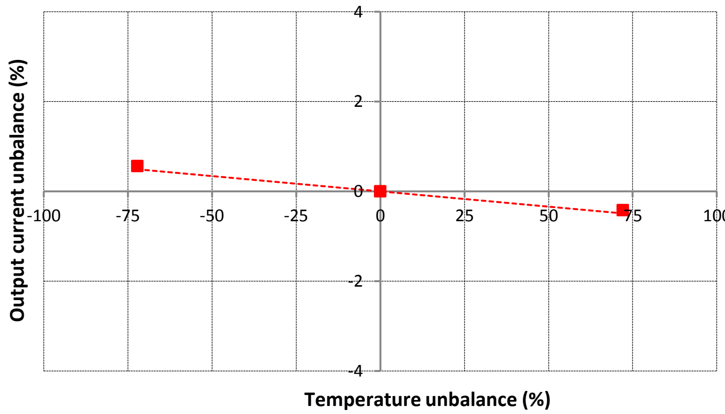


Figure 4-20　Sensitivity plot: temperature ΔT

The temperature change has very limited influence on the output current balance. On average, an extra 0.5% current unbalance is induced in the worst case. It proves that the circuit is hardly affected by temperature and has excellent thermal stability.

5） Summary

All curves are summarized in the following figure to compare their relative contribution to output current unbalance at the tested working point.

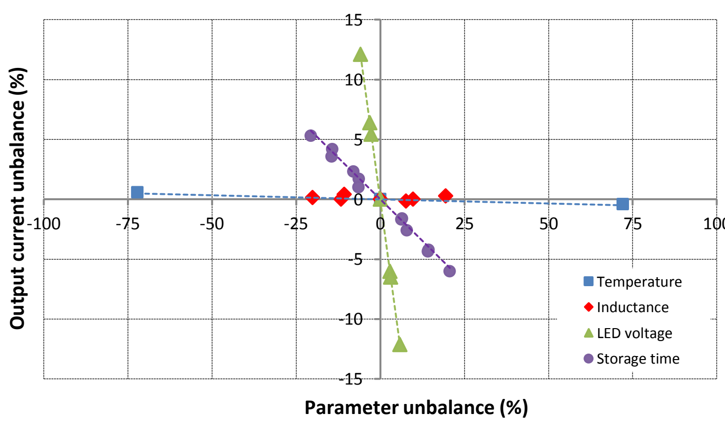


Figure 4-21　Summary plot: circuit sensitivity

Temperature divergence and inductor value spread have very limited impact, normally lower than 0.5%. These are considered as good attributes of the circuit. The circuit is more sensitive to transistor storage time t_s and LED voltage V_{LED}. To minimize the output current unbalance ΔI_o, it is preferable to use transistors with smaller t_s spread. It will also help by arranging the LED strings to decrease the spread of V_{LED} if possible.

4.4 Summary and Conclusion

In this chapter, the basic functionality of the proposed control strategy and its corresponding implementation is validated with both simulation tools and prototypes.

It was mentioned in last chapter that multiple pairs of coefficients are capable of delivering a certain output current while satisfying the stability condition. In order to investigate the effect of different a and b on system performance, four input-series systems based on different control options are built with discrete components in *LTSpice*. Simulation results show that the modulated peak current controlled buck-boost operate stably if the controller setting meets the stability condition.

Under each control option, circuit sensitivity to a practical component tolerance, including inductor value L, LED voltage V_{LED}, power supply V_{cc}, and current sense resistor R_s, is explored in simulation. The results show consistence with *Matlab* simulation that a steeper input curve is good for output balance but bad for line regulation and THD performance.

Two prototypes based on the second control option are built. Evaluation results proves the system stability and EM compatibility again. At given operation point, circuit sensitivity is also checked. As predicted by the control strategy fundamental, the system is hardly affected by inductor value. The unique implementation also excludes the effect of temperature change and system has satisfying thermal stability over the checked temperature range. Transistor storage time and LED voltage have more significant impact but are limited to <15% for practical component tolerances.

Chapter 5 Retrofit LED Driver Design

In this chapter, a driver design example is presented for 2ft LED tube application. The driver is electrically compatible with the existing fluorescent lighting fixtures and can be a drop-in replacement. The contents of this chapter include detailed design procedures, simulation verification and experimental results.

5.1 Specifications

The system input voltage has a nominal value of 230V, 50Hz and allows $\pm 15\%$ variation in amplitude. The LED array is already defined for this application, which comprises 2 parallel strings and 32 LEDs in series per string. Each driver has a nominal output current at 72mA, and a nominal input power of 7.5W. Two reference ballasts are provided for design phase use. The specifications listed below are all defined with reference EM ballast in the system unless mentioned otherwise.

The electrical specifications of the retrofit LED driver to be designed are defined as follows. All specifications listed below are defined with reference EM ballast in the system unless mentioned otherwise.

Input voltage /V	$196 \leq V_{in,rms} \leq 264$, 50Hz $V_{in,nom}$=230
Driver output current /mA	72
Driver input power/W	7.5
Driver efficiency /%	>85
THD /%	<30 (<20 independent-mode without EM ballast)

Table 5-1 Design specifications: 2ft retrofit LED driver

The driver should be electrically compatible with the mainstream fluorescent lighting fixtures. As comprehensively discussed in Chapter 1, the major functionality should include:

1. Stable series- and independent-mode operation
2. Mains and EM ballast compatibility
3. Detection and automatic operation-mode selection

Additionally, it is preferable that the output current unbalance is minimized. Within reasonable component tolerance on inductor value $L(\pm 10\%)$ and LED voltage $V_{LED}(\pm 3\%)$, the resulting output current unbalance (ΔI_o) should be within $\pm 15\%$ in series-mode operation.

5.2 Design Considerations

5.2.1 Operation Flow-chart

The application requires each driver should be capable of both series- and independent-mode operation depending on the specific luminaire configuration. The driver has to first detect the input voltage and decide which mode it should enter by itself.

The driver may apply different control schemes in those operation modes. As discussed in last section, when connected in series, the drivers will operate in open-loop to ensure stability. If a higher input voltage is detected, it needs to switch to one-lamp independent mode automatically. In this case, the driver may continue operating in open-loop or turn to closed-loop regulation for accurate output current.

The operation process is described in Figure 5-1 with a flowchart. Once the circuit is powered on, a default low-current mode for safe start-up is first entered. This default mode avoids potential over-current or over-voltage for safety reasons. It takes a while for detection signal to build up and during this period the default mode should always be active. After detection signal is fully established, the driver is able to decide which mode to go for depending on the criteria in the flowchart.

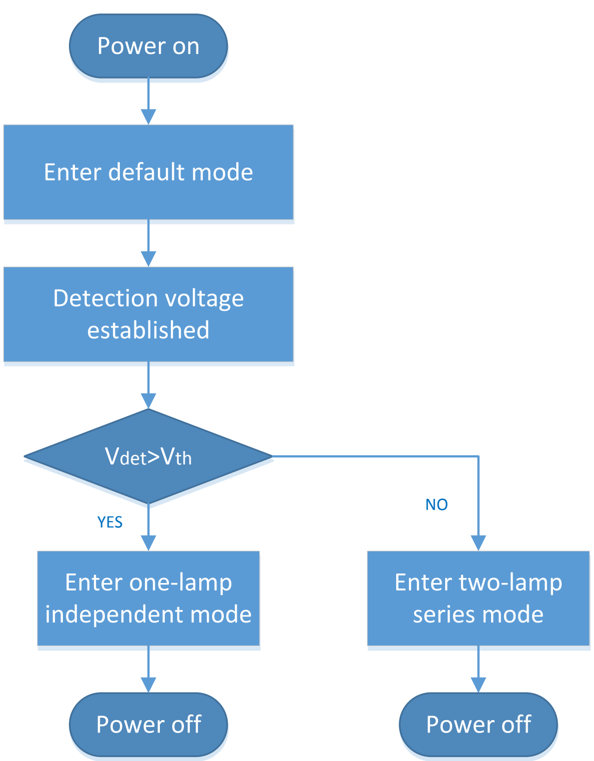


Figure 5-1 Flowchart: driver operation principle

Based on the flow chart, several add-on blocks are added to facilitate full functionality. They are introduced and explained in the following sections.

5.2.2 Control Option

Chapter 4 already gives three available control options and their performance analysis in terms of system stability, sensitivity to component tolerance, line regulation, and total harmonic distortion elaborately. Provided the design specifications, the driver under development will be implemented with the first control option, which has only AC component. Here are the considerations.

1. Total harmonic distortion

A general total harmonic distortion requirement for the driver is <30%. However, independent operation without EM ballast is one critical operation condition that requires THD <20%. The voltage conversion ratio K_v in independent mode is almost doubled than series-mode and will lead to a more distorted input current waveform, as illustrated in [35]. In series-mode, control option #2 is already approaching the THD limit and therefore will be no longer considered. Instead, it is feasible to achieve less distortion with control option #1.

2. Sensitivity to component tolerance

Sensitivity to component tolerance is another important consideration in driver design since it is preferably to have equal light output in the same luminaire. Although the resulting output current unbalance from major component spread (ΔL and ΔV_{LED}) is acceptable, there are some other minor mismatch. These minor effect are not studied extensively but are also contributing to the overall unbalance performance. A steeper input characteristic curve of control option #1 also helps to minimize the sensitivity to component tolerance.

3. Accuracy of internal power supply V_{CC}

An internal DC power supply V_{CC} has to be built with a zener diode or linear regulator. This internal power supply powers the comparator and provides the DC offset in current reference as well. In case that it sets part of the current reference, it needs to be a high precision power supply. By taking away the DC component, the V_{CC} voltage does not need to be that accurate.

In one-lamp independent mode, the driver will continue operating in open-loop for the ease of implementation. Another advantage is the consistent light output variation in one luminaire in case of input disturbance. Especially in a three-lamp luminaire where two lamps are in series and a third lamp is in parallel (shown in Figure 1-6(a)), it is preferably to have the same level of light variation.

5.3 Driver Design Procedure

A complete driver schematic is presented in Figure 5-2. There are six major function blocks that are denoted with dashed lines, including rectifier bridge, EMI filter, self-oscillating buck-boost converter, modulated peak current controller, internal power supply V_{cc} and detection and mode-selection block.

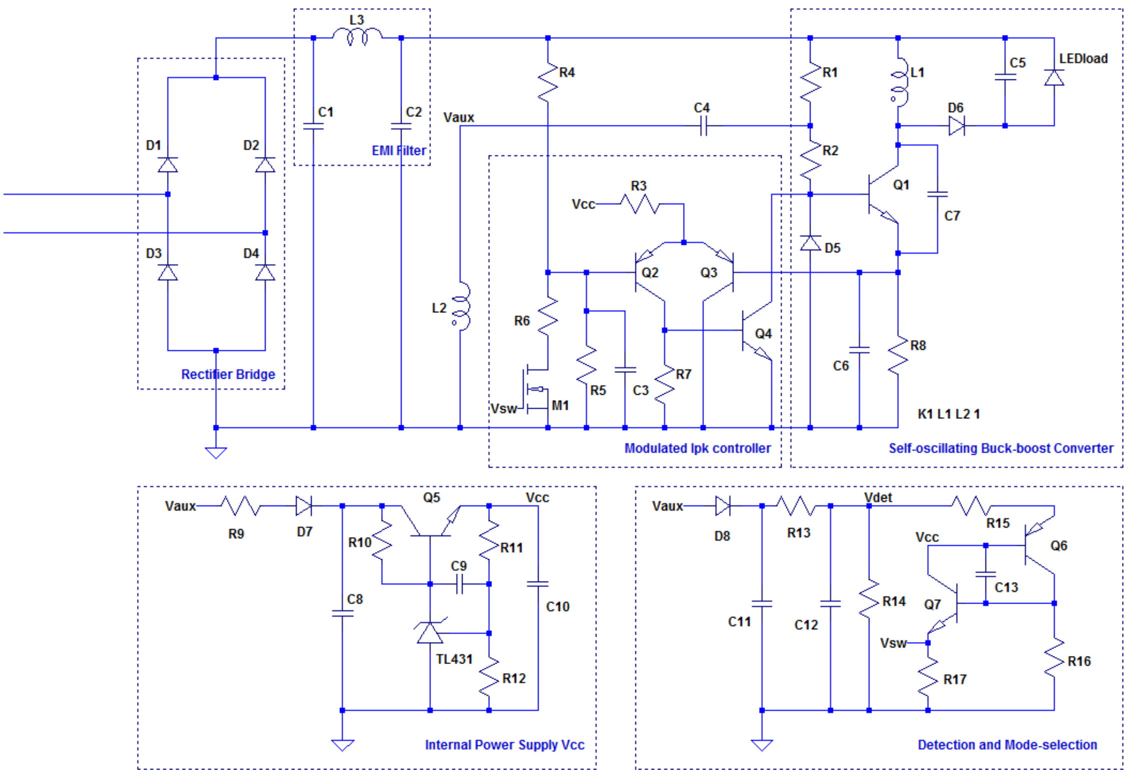


Figure 5-2 Complete driver schematic

The modulated peak current controller does not differ much from Figure 3-11 except that the DC component has been removed and a scaling-down branch for independent mode (R_6 and M_1) is paralleled at reference input node. Two additional blocks are introduced, as the name suggests, to set up an internal power supply and provide detection and mode-selection function. The detailed design procedures are followed.

5.3.1 Power Stage and Self-oscillating Components

The power stage design of a self-oscillating buck-boost converter is quite similar to a general buck-boost design. How the components are selected are discussed in detail. However, there is not much literature in designing a self-oscillating converter. To obtain better performance of the self-oscillating converter, there are some general guidelines in component selection. It should be noted that the designed values, especially in the self-oscillating part, are subject to adjustment in experiments.

1. Inductor

One good property of the proposed control scheme is that the output current is theoretically not affected by the inductance value at a certain working point. However, the operating frequency is controlled by the inductance value. In boundary conduction mode, the on and off time are easily calculated near a DC operating point.

$$t_{on} = \frac{I_{L,pk}L}{V_{in}} \qquad \text{Eq. 5- 1}$$

$$t_{off} = \frac{I_{L,pk}L}{V_o} \qquad \text{Eq. 5- 2}$$

The resulting operating frequency is,

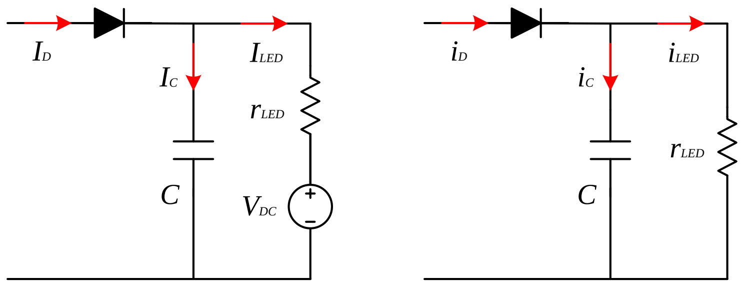
$$f_s = \frac{1}{t_{on}+t_{off}} = \frac{V_{in}V_o}{I_{L,pk}L(V_{in}+V_o)} \qquad \text{Eq. 5- 3}$$

Assume the peak inductor current is already set to satisfy the output current requirement. Thus, the inductance value is the dominant factor in controlling the operating frequency. The switching frequency of a self-oscillating converter is variable, which depends on the input voltage and the load, and hence the frequency selection is flexible. Depending on the specific demands, tens of kilohertz can be a moderate choice in reality. To avoid audible noise, the frequency shouldn't be lower than 25kHz. Compared with series-mode operation, an independent lamp gets full mains voltage and thus a lower peak current is needed for the same power demand. Both on and off time intervals in Eq. 5-1 and 5-2 will decrease and lead to a higher frequency.

When the control equation is already known, the inductance value can be changed freely to select a proper operating frequency. A 2.2mH inductor built on EF16 core (available in the lab) is chosen. The operating frequency near input voltage peak is around 50kHz and 70kHz for series- and independent-mode, respectively.

2. Output capacitor

The fluctuations in input voltage create unacceptably large current ripple at the output end and hence an output capacitor is placed in parallel with LED strings. An appropriately sized output capacitor will help to reduce ripples at line frequency. The intrinsic property of LED itself has an effect on the ripples as well. To analyze the effect, LED load is represented in its equivalent form with a DC voltage source and a dynamic resistance. By isolating the AC component from DC component, an AC signal circuit is obtained for ripple analysis [42].



(a) Equivalent circuit (b) AC signal circuit

Figure 5-3 Output current ripple

In buck-boost topology, the diode is forward biased when the switch is off. Assuming that the output current is the average value of diode current (and it should be in steady state), the instantaneous diode current can be estimated as follow with acceptable error.

$$I_D = I_o - I_o \cos(4\pi f_L t) \quad \text{Eq. 5- 4}$$

The line frequency is denoted as f_L, which is $50Hz$ here. The AC component in diode current is then,

$$i_D = -I_o \cos(4\pi f_L t) \quad \text{Eq. 5- 5}$$

If k_{ripple}(in %) of nominal output current is the peak-average current ripple in LED strings, the remaining current should go into the capacitor.

$$C = \frac{1}{4\pi f_L r_{LED}} \sqrt{(\frac{1}{k_{ripple}})^2 - 1} \quad \text{Eq. 5- 6}$$

In ac signal simulation, a capacitor at $68\mu F$ can readily keep the ripple to $\pm 30\%$ under the small-signal excitation i_D. An electrolyte capacitor is chosen.

3. Power transistor and power diode

In a buck-boost converter, the voltage stress on the transistor during its off time will be the sum of input and output voltage. The current through the switch is equal to the input current when the switch is conducting. As required, the transistor and diode selection needs to satisfy both working situations.

The highest voltage stress on the transistor appears in single-lamp mode where the driver gets full mains voltage. The diode gets exactly the same voltage stress during the transistor on-interval. The maximum voltage is,

$$V_{sw} = V_D = \sqrt{2} V_{in,max} + V_o \quad \text{Eq. 5- 7}$$

The maximum current is obtained in series operation mode in order to retain the same amount of power. The maximum current stress for both transistor and diode is the maximum inductor peak current,

$$I_{sw} = I_D = (I_{L,pk})_{max} \quad \text{Eq. 5- 8}$$

The voltage and current stresses put the fundamental requirements on the active components. However, there are more factors to be considered. If the β of the transistor is higher, the loss in start-up resistor can be reduced as noted in [31]. The β value is also expected to have a small variation to avoid extremely high peak current during start up and false oscillations in case of load change.

A fast recovery diode MUR160 ($600V, 1A$) and a high-voltage NPN power transistor 3DD4520 A6 ($800V(V_{CBO}), 450V(V_{CEO}), 4A$) are chosen. A small capacitor ($100pF$) is in parallel with the transistor in order to reduce turn-off losses.

4. Secondary (auxiliary) winding

The secondary winding design should be in such a way that the voltage over the secondary winding can maintain self-oscillation, either by providing sufficient gate signal voltage for a MOSFET or base current for a BJT. The primary winding gets the full input voltage when the switch is closed and a reverse output voltage when the switch is open. The positive voltage has a sinusoidal envelope.

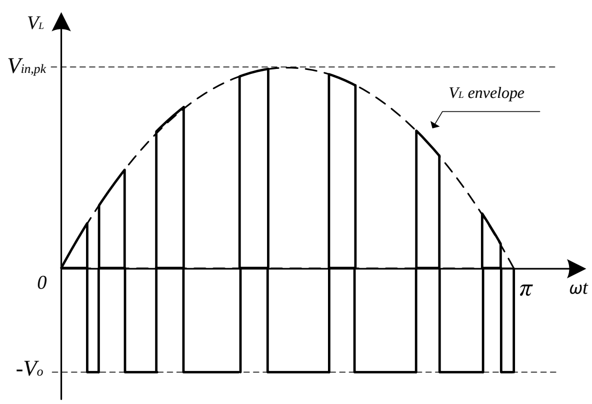


Figure 5-4 Primary winding voltage

The secondary voltage is preferably at around 10V as a rule of thumb in engineering to facilitate the oscillations and turn on the transistor. By setting the peak voltage at 16V, the transformer turn ratio is determined.

$$n = \frac{V_p}{V_s} = 10 \quad \text{Eq. 5- 9}$$

It can be expected that near zero crossings of input voltage, the energy in secondary winding may not be sufficient to turn on the transistor.

5. Base resistor and capacitor

One criterion for selecting the base resistor is that the base current is guaranteed to turn on the transistor at worst situation. The resistance can also be tuned to achieve minimized loss, especially in low-power applications [43]. During on-time, the capacitor is charging up according to time constant τ. If the transistor is turned off naturally by the oscillation, it is obvious that the on-time and operation frequency is tunable by changing the capacitor value. If transistor is actively switched off, however, the capacitor is no longer capable to do so.

One design idea is to keep zero voltage fluctuations across the capacitor C_4. The capacitor voltage will reverse its polarity during off-time. As soon as next cycle starts, the secondary winding voltage plus the capacitor voltage might generate a large current into the base. The inrush current inevitably causes more power dissipation in the base resistor R_2. A time constant five times larger than the switching periods is sufficient to maintain zero-voltage fluctuation.

$$R_2 C_4 = \frac{5}{f} \qquad \text{Eq. 5- 10}$$

Another benefit is that the base current is much easier to determine when the capacitor voltage fluctuates around zero. Neglecting the capacitor voltage, the base current is supplied by the auxiliary winding via a base resistor R_2.

$$i_b = \frac{\frac{v_{in}}{n} - V_{BE} - v_{sense}}{R_2} = \frac{i_c}{\beta} \qquad \text{Eq. 5- 11}$$

The peak collector current is proportional to the input voltage as the control equation promises. Taking a typical value $\beta = 15$,

$$R_2 = 338\Omega \qquad \text{Eq. 5- 12}$$

$$C_4 = 303nF \qquad \text{Eq. 5- 13}$$

The nearest standard values are chosen: 330Ω and $330nF$.

6. Start-up resistor and sense resistor

The start-up resistor provides the initial base current when the circuit is powered on. Since the collector current has to rise from zero, a small amount of kick-off current will be sufficient. However, the high input voltage is applied to it at all time. Therefore, the power loss on this resistor matters to the overall efficiency. Practically, the power dissipation should be less than 1% of the maximum output power [43]. In practice, a $1.5M\Omega$ start-up resistor makes good compromise in between the start-up time and power dissipation.

Similarly, the sense resistor which detects the collector current is also limited by the power dissipation requirement [44]. If 1% of total power is allowed to dissipate in the sense resistor, the required resistance is,

$$R_8 = \frac{P}{I^2} = 2.7\Omega \qquad \text{Eq. 5- 14}$$

A more conservative value is chosen as 2.2Ω.

5.3.2 Transistor Turn-off

The transistor storage time, especially in power transistor, will cause delay in switching actions. The delay limits the maximum operating frequency of the circuit and also affects the control accuracy. During the switch turn-off transients, the inductor current will continue rising to a value beyond the reference. The observable delay time is the time interval between the instants when base current and inductor current start to drop, respectively.

One method to reduce the effect is to use a *Baker Clamp*. A standard baker clamp circuit is implemented with three diodes near the base.

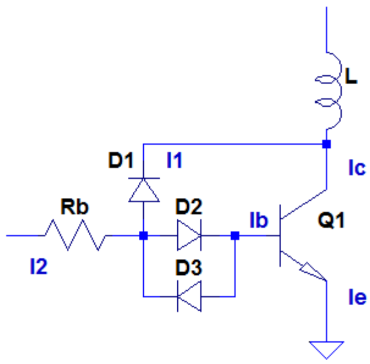


Figure 5-5 Baker clamp

The Baker clamp in Figure 5-5 introduces a current feedback to the transistor current and avoids saturation by decreasing the gain. The diode D_1, which is called the feedback diode, diverts part of i_2 to i_c and thus fastens the switch-off. The clamp diode D_2 is used to raise sufficient drive voltage. Another diode D_3 provides a path to extract the charge when the transistor is being turned off. Theoretically, a baker clamp can reduce the storage time by a factor of 5 to 10. However, it is not adopted in this design since a high voltage diode is needed.

Another factor that affects the turn-off transients is the sense resistor voltage. While the transistor Q_1 is being switched off, the emitter current decreases and the base voltage of Q_3 drops. If the reference voltage does not change, Q_2 will conduct less current and Q_4 will be supplied with lower base current simultaneously. As a result, less current will be extracted from Q_1 base and causes the delay in switching-off.

In order to switch off Q_1 faster, a small capacitor C_6 is paralleled to the sense resistor R_8. The capacitor gradually discharges and helps to slow down the voltage drop at v_{sense}. Therefore, the phenomena that delays the switching-off will be alleviated.

5.3.3 Internal Power Supply V_{cc}

The power supply V_{cc} in principle has two functions in the circuit. Firstly, it works as a static voltage source and sets the reference offset via a voltage divider (not valid in this design). Secondly, together with R_3 (which is significantly larger than the transistor on-resistance), it supplies the comparator in the form of a current source. The external power supply V_{cc} needs to be removed anyway in implementation. Figure 5-6 illustrates a power supply built with voltage regulator TL431.

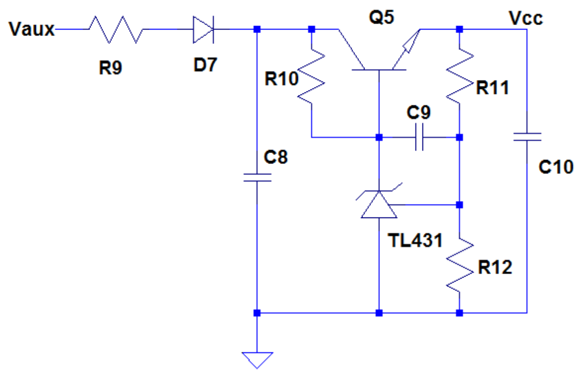


Figure 5-6 V_{cc} power supply

The auxiliary winding voltage will first charge the capacitor C_8 via a diode and a resistor. The resistor limits the maximum charging current to the electrolyte-capacitor. The voltage over the electrolyte-capacitor will fluctuate around the voltage of the auxiliary winding, which has a sinusoidal envelope. The voltage regulator is connected in its typical application and the output voltage V_{cc} is decided by R_{11} and R_{12} in Figure 5-6. TL431 has an internal voltage reference V_{REF}.

$$V_{cc} = (1 + \frac{R_{11}}{R_{12}})V_{REF} \qquad \text{Eq. 5- 15}$$

It is also possible to implement the power supply with a zener diode rated at the desired V_{cc} value and a resistor in series to guarantee sufficient current through the zener diode. A comparison was made to choose the better solution. Generally, TL431 has a tolerance of 0.5~2.0% on V_{REF} depending on the manufacturers and specific part number [45], while zener voltage are specified with 2~5% tolerances [46]. In addition, zener diode is more sensitive to temperature change. Another advantage of TL431 configuration is the electrolyte-capacitor can be smaller. In order to maintain a constant current through the zener, a larger electrolyte-capacitor is required to smooth the voltage. But it is not necessary in the TL431 configuration since the output is barely affected by that voltage. Based on these reasons, a TL431 is preferable to function as an internal power supply V_{cc}.

It is also worth mentioning that before V_{cc} voltage is established, the comparator is not able to control the inductor current. The current at which the transistor turns off is determined by the self-oscillation and it can be several times higher than the regular current. Therefore, the power supply voltage should be set up as soon as possible. A possible modification is to replace the diode with a zener diode. The diode in self-oscillating block conducts during transistor off-time since it is forward biased by the negative voltage in auxiliary winding. During transistor on-time, it withstands a reverse voltage until its breakdown voltage, which is described in Eq. 3-22. The use of a zener diode will clamp the high inductor inrush current to an accepted level.

5.3.4 Detection and Mode-selection

A detection block in design is necessary to decide in which mode the driver will operate and the corresponding functional circuit will be automatically enabled by the detection signal.

The key parameter for detection is the input voltage, which easily distinguishes different operation conditions. If the detection signal V_{det} exceeds a certain threshold, it is considered that the driver is individually connected to the mains. Otherwise, it is considered that the driver is connected in series with another driver.

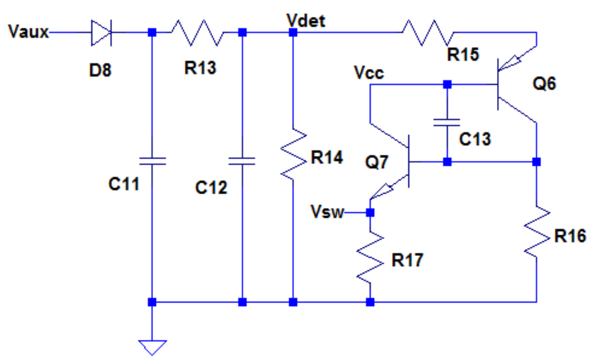


Figure 5-7 Detection signal generation

The detection signal V_{det} comes from auxiliary winding, the positive value of which is proportional to the input voltage. The positive voltage over auxiliary winding is rectified and therefore generates the detection signal, as shown in Figure 5-7. The detection signal is then compared to a threshold voltage V_{th}, which equals to $V_{cc} - V_{BE,Q_6}$. In case of high detection signal, two transistors $Q_6$and Q_7 will conduct. Therefore, the node denoted with V_{sw} is connected to power supply V_{cc} , which will turn on the low-voltage MOSFET M_1 and change the current reference value accordingly. Otherwise, the MOSFET is off and the voltage divider ratio is at higher level.

It is noted that the detection signal is established by charging up a capacitor and takes a while for V_{det} to reach the threshold voltage V_{th}. During the transients, however, the voltage divider is preferable at lower dividing ratio so that even in high input condition, the current will not overshoot. The default mode after power-on should have the MOSFET on and the voltage divider ratio at the minimum level. The capacitor C_{13} that connects two transistor base and resistor R_{16} are used to set the default mode.

Originally V_{sw} is at ground potential. When the power supply voltage V_{cc} is built up, it charges the capacitor C_{13} via a resistor R_{16}. The voltage over C_{13} rises with an RC charging curve.

$$v_c(t) = V_{cc}\left(1 - e^{-\frac{t}{\tau}}\right), \tau = R_{16}C_{13} \quad \text{Eq. 5- 16}$$

Meanwhile, the base voltage of Q_7 is lifted to a higher potential and turns on Q_7 temporarily. Now the node V_{sw} is brought to a high potential and turns on the low-voltage MOSFET M_1. Base potential of Q_7 follows,

$$v_{base}(t) = V_{cc} - v_c(t) \quad \text{Eq. 5- 17}$$

Afterwards, if the detection signal V_{det} doesn't exceed V_{cc}, capacitor voltage will be charged to V_{cc} and V_{sw} will drop to ground potential. As a result, a larger current reference is established for sufficient current. Otherwise if detection signal V_{det} exceeds V_{cc}, V_{sw} is kept at high voltage potential since transistor Q_7 continues conducting.

There are three points that needs attention for appropriate functioning.

Firstly, the power supply voltage V_{cc} should be built faster than detection signal V_{det} for proper functioning of detection circuit. It is also mentioned in the last chapter that the current is not controllable before V_{cc} powers up the comparator and causes current overshoot in LED load.

Secondly, time constant $\tau = R_{16}C_{13}$ for charging should be carefully selected to be longer than the time needed that V_{det} exceeds V_{cc} to avoid early mode transition.

Thirdly, the voltage divider in the filtering network should be designed in such a way that the input voltage boundaries are appropriately detected and distinguished. In series mode operation, it is very likely that one lamp will switch to a higher current reference ahead of the other due to start-up time mismatch. The voltage divider should also take care that the second lamp will not falsely stay in the default mode afterwards.

5.4 Simulation Results

LTSpice simulations mainly focus on the proper functioning of detection and mode selection circuit. Steady state operation that has been verified in Chapter 4 is not repeated hre in this section. Simulation waveforms are obtained for two distinct operation modes (without EM ballast).

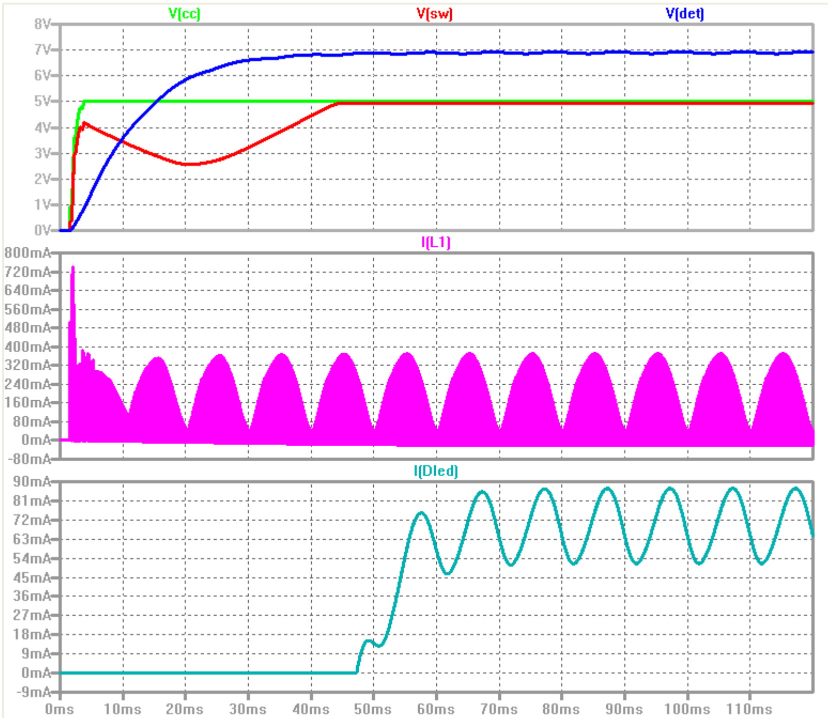


Figure 5-8 Independent-mode start-up simulation

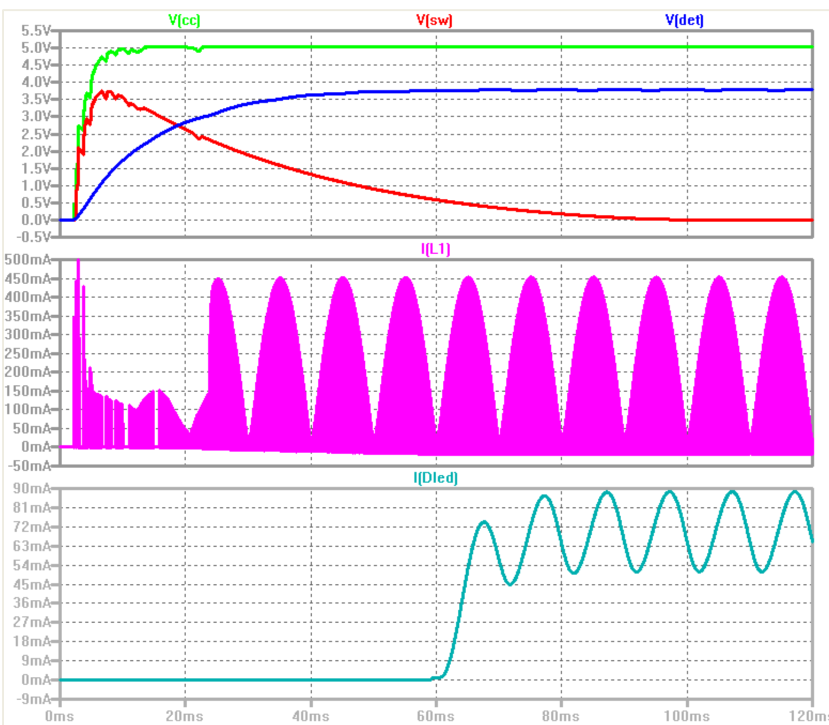


Figure 5-9 Series-mode start-up simulation

The detection and mode-selection block is functioning well according to the simulation waveforms. The built-up time of V_{cc} is shorter than V_{det} in both cases, which allows the detection circuit to compare the signals correctly. V_{sw}, the gate signal of M_1, rises together with V_{cc} and consequently the low-current default mode is always first entered after power-on. Shortly after V_{cc} is established, V_{sw} gradually decreases to zero unless interrupted by a high detection signal V_{det}. In Figure 5-8, a high detection signal is detected before V_{sw} drops to the gate threshold voltage of M_1 and the default mode is retained thereafter. On the contrary, in Figure 5-9, detection signal never exceeds the detection threshold voltage and will finally turn off M_1. A higher inductor current reference is adopted shortly in order to deliver sufficient power in series mode.

The inductor current seems discontinuous in the first tens of milliseconds and results in a zigzag trace of V_{cc}. The phenomenon is however not significantly observed in prototype experiments. The current overshoot before V_{cc} is fully built up is below 1A in both cases.

5.6 Prototype Experiments

Two prototypes are built on general-purpose PCB boards, equipped with all required functionality. Their performance will be evaluated with following experiments. Figure 5-10 shows one of the prototypes, each block indicated with dashed rectangular.

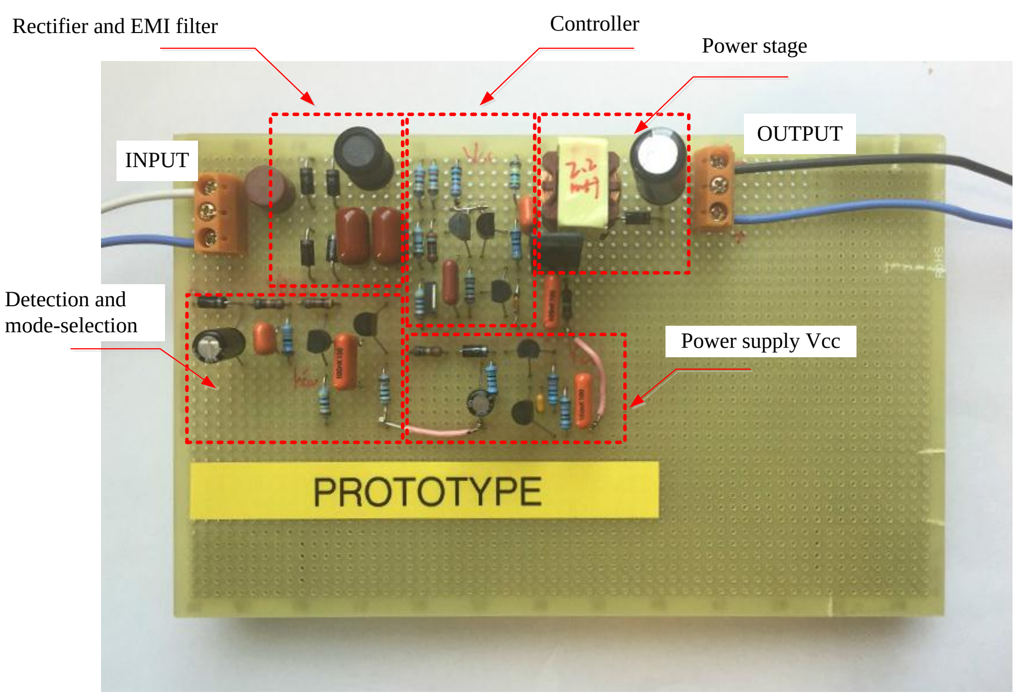


Figure 5-10 Driver prototype

In total, six EM ballasts from different manufactures are available for compatibility tests: two of them are 38/40W for series-mode while others are 18/20W for independent-mode. Among them, two ballasts from *Tridonic* (36W) and *MST* (18W) are the reference ballasts.

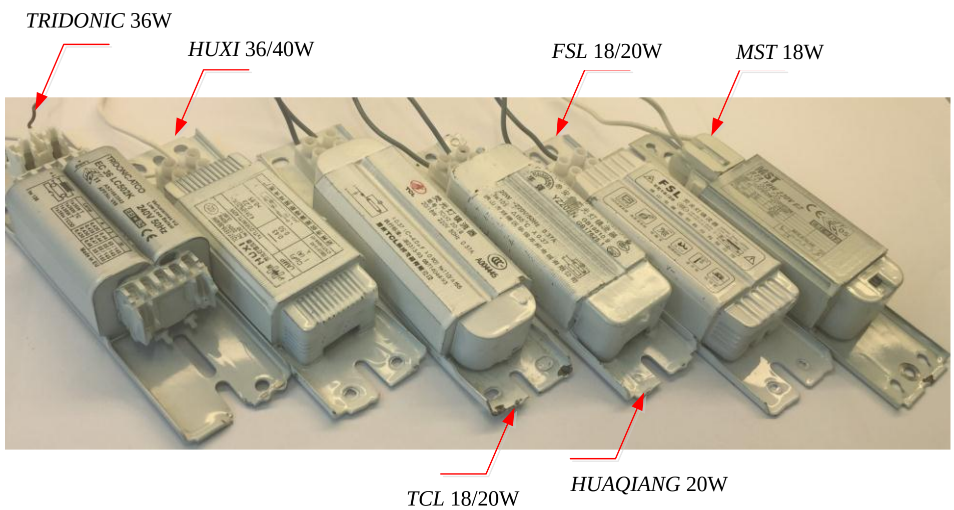


Figure 5-11 EM ballast cluster

Their specifications are listed in Table 5-2. Equivalent inductance *L* and resistance *R* come from experimental measurements. Apart from electrical parameters, two thermal parameters are also stated: tw (℃) is the highest operating temperature, which is limited by insulation of the windings and Δt (℃) is the temperature rise in normal operation.

Ballast type	**Power rating /W**	**Input voltage /V**	**Frequency /Hz**	**Tw/℃**	**Δt/℃**	**L/H**	**R/Ω**
TRIDONIC EC36 LC502K *	36	240	50	130	55	1.4	40
HUXI TOES8518	36/40	220	50	130	60	1.5	93
MST BTA *	18	230	50	130	50	1.7	41
TCL YZ201G	18/20	220	50	110	55	1.6	42
HUAQIANG YZ20ZN	20	220	50	105	55	1.7	109
FSL EB18/20	18/20	220	50	105	60	2.1	137

Table 5-2 EM ballast specifications and electrical models (* reference ballast)

Two LED loads for experiments have the same structure: 32 low-power LEDs in series in each string and 2 identical strings in parallel.

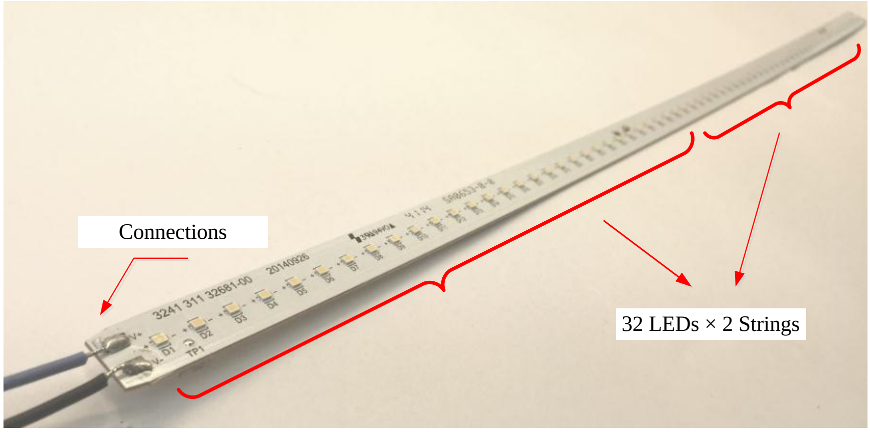


Figure 5-12 LED load

A *LeCroy* 350MHz oscilloscope, a *NF* programmable AC/DC power source, a *YOKOGAWA* precision power analyzer are used for experiments and measurements.

5.6.1 Steady-state Measurements

In steady-state, the prototypes will be evaluated in various aspects, including electrical specifications, compatibility with EM ballasts, line regulation performance and sensitivity to ΔL and ΔV_{LED}.

Prototypes are first measured to determine whether their performance meets the design specifications. All measurements are with reference ballasts specified for design phase. The data in the following table are read from a power analyzer.

Parameter	Specifications	Series-mode	Independent-mode	
		Lamp1 / Lamp2	Lamp1	Lamp2
Driver input power	7.5W (±10%)	7.4W/7.5W	7.9W	7.6W
Output current	72mA (±15%)	71.7mA /72.5mA	73.8mA	71.8mA
LED ripple current (peak to average)	<30%	24.2%	26.3%	26.3%
Driver efficiency	>85%	89.2%/89.1%	85.9%	85.8%
PF	>0.9	0.99	0.94	0.93
THD	<30%	9.1%	26.1%	27.6%
Current unbalance	<18%	-1.1%	N/A	N/A
Ballast loss	<1W	0.23W	0.15W	0.12W

Table 5-3 Electrical specifications and measurement results

The drivers under test meet all electrical specifications that are shown in Table 5-2. Due to open-loop regulation, the driver's output is sensitive to component spread. Therefore, two drivers have unequal output current although all components are stated with the same part number and value. Instead of simulation tryouts, it is a more common way to tune design parameters in experiments, preferably based on multiple prototypes.

Both drivers achieve a >85% efficiency in four operation modes, which is a satisfying result for low-power applications. Usually when input voltage increases, the efficiency of switched mode power supply will increase. However, in independent mode where input voltage is almost doubled, the efficiency is even 3% lower than series-mode. This is mainly due to the increasing power loss in the power transistor. The base current provided by the auxiliary winding is also doubled and it over-drives the transistor, which results in excessive loss at the base. It cannot be avoided by increasing the base resistor, otherwise in series-mode the base current will be insufficient.

Total harmonic distortion also increases significantly from series-mode to independent-mode. Partly it is due to the higher voltage ratio k_v which makes the input current flatter near the top and less like sinusoid. The application of EM ballast is also a reason. Compared to the EM ballast used in series-mode, the ballast for independent-mode is causing more distortion.

In all cases, the compatibility with reference EM ballasts is not a problem. Power losses in EM ballast are below 1W.

Line regulation performance is evaluated according to its definition: input voltage is changed within $\pm 15\%$ on purpose to measure the output current variation. Measurements are carried out at every 5% change in input voltage. Figure 5-13 plots the line regulation performance in different operating modes.

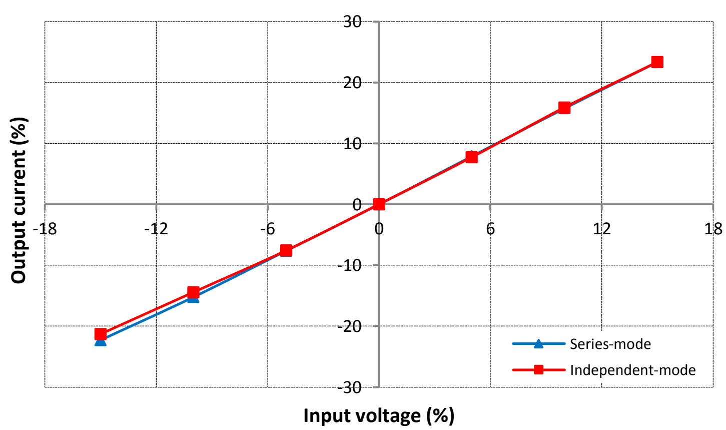


Figure 5-13 Line regulation performance

As predicted, line regulation performance is a bit worse than the previous two prototypes evaluated in principle verification (Chapter 4). Output current is more sensitive to input voltage variation since the current reference is totally proportional to input voltage. In all four operation modes, a

15% variation at the input leads to around 23% variation at the output. However, it is good for multi-lamp luminaire since all lamps have the same response to input variations.

Apart from reference ballast, there are several EM ballasts available for testing. The driver's performance on various EM ballasts are evaluated by the following table. Output current unbalance is in its absolute value.

Mode	**Ballast Type**	U_{rms1}/ V	I_{rms1}/ mA	PF	P_1/W	P_2/W	**Ballast loss/W**	$I_{thd,1}$/ %	I_o/mA	$\lvert I_o \rvert$ /%
Series mode	Direct mains	229.9	66.3	0.99	15.1	15.1	N/A	9.1	74.1/74.9	1.1
	TRIDONIC	**229.9**	**65.1**	**0.99**	**14.9**	**14.6**	**0.3**	**8.9**	**71.7/72.5**	**1.1**
	HUXI	229.9	62.9	0.99	14.3	13.6	0.7	7.6	67.3/67.9	0.9
Independent-mode	Direct mains	230.0	35.1	0.92	7.4	7.4	N/A	17.5	70.3	N/A
	MST	**229.9**	**36.0**	**0.93**	**7.7**	**7.5**	**0.2**	**27.9**	**72.3**	
	TCL	230.0	35.9	0.93	7.6	7.4	0.2	27.6	71.9	
	HUAQIANG	229.9	35.2	0.94	7.6	7.3	0.3	24.7	69.7	
	FSL	229.9	35.4	0.93	7.6	7.3	0.3	26.4	70.1	

Table 5-4 Performance on various EM ballasts

The drivers are compatible with all EM ballasts for tests. Ballasts losses are mainly in the range of 0.2~0.3W except 0.7W for *HUXI* ballast. Some ballasts, for instance *HUXI*, *HUAQIANG* and *FSL*, have a larger series resistance and lead to a lower output current compared with direct mains measurements. Other performances in PF, THD and output current unbalance do not show distinct differences with different EM ballasts.

Principle verification in Chapter 4 already shows that a modulated peak current controlled buck-boost converter in BCM is barely affected by inductor value. Hence circuit sensitivity to inductance tolerance is not repeatedly tested. The effect of LED voltage mismatch is investigated in the same procedure. LED voltage is changed by shorting or adding one LED in the strip to mimic $\pm 3\%$ variation. The corresponding output currents are listed in the following table.

Driver #1 **Driver #2**	**+3%**	**0**	**-3%**
+3%	N/A	74.3 70.4	76.6 69.1
0	70.0 74.8	72.6 73.2	75.1 71.9
-3%	68.6 77.3	71.3 75.8	N/A

Table 5-5 Sensitivity measurements: LED voltage ΔV_{LED}

By taking a new origin to exclude all other effects, the output current unbalance brought by LED voltage unbalance is plotted in Figure 5-14.

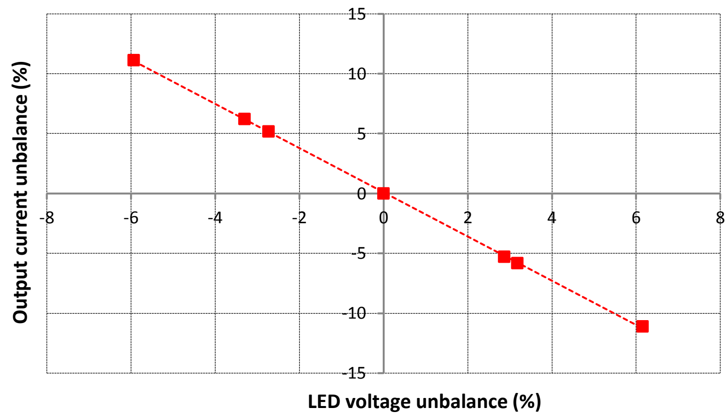


Figure 5-14 Sensitivity plot: LED voltage ΔV_{LED}

The correlation is fitted with a linear curve that has a fitting coefficient $R^2 > 0.99$.

$$\Delta I_o = -1.85\Delta V_{LED} \quad \text{Eq. 5- 18}$$

The removal of DC component in current reference results in a steeper input curve, which is beneficial to reduce circuit sensitivity. Comparing Eq. 5-18 with Eq. 4-8, the influence of LED voltage variation is further reduced. For a maximum ΔV_{LED} of 6%, 11% output current unbalance is observed in those two prototypes.

5.6.2 Transient and Steady-state Waveforms

There are three key points to be checked during start-up intervals: 1) whether the detection and mode selection block is functioning properly; 2) whether the possible current overshoot is to some extent avoided; 3) whether in series-mode the input voltage is still stably distributed.

To avoid current overshoot at the output, it is important to set an appropriate RC time constant to maintain the default mode during the whole start-up interval. If the capacitor C_{13} is charged up too rapidly, the converter may shift back to high-current mode before the detection voltage is fully established. The following waveforms shows the consequence of an inappropriate time constant setting.

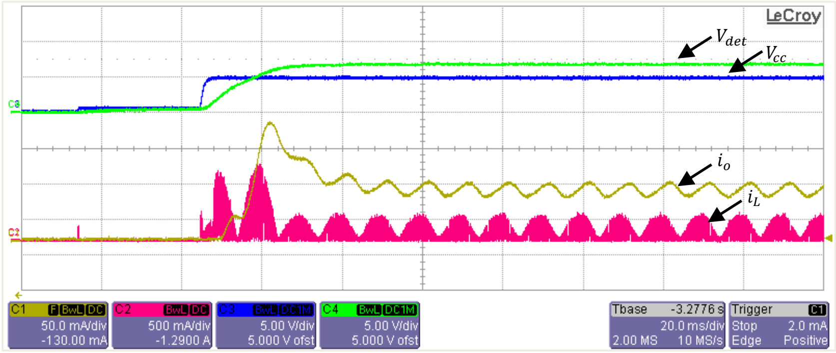
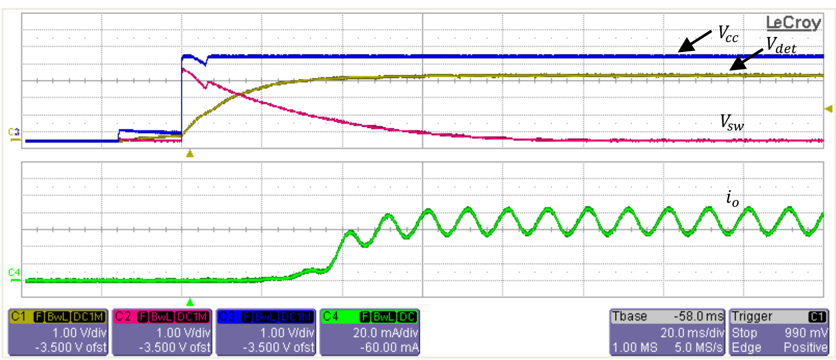


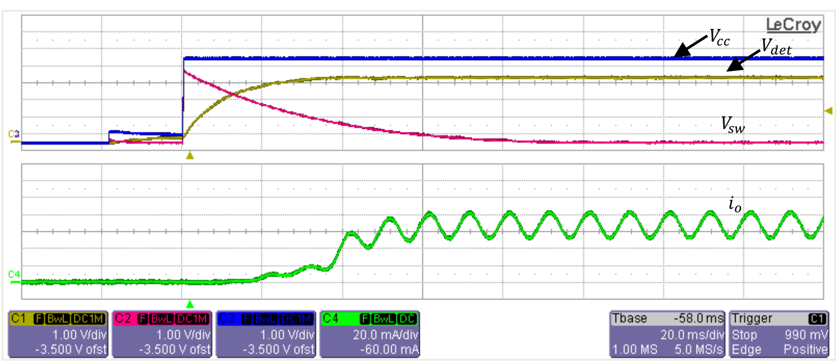
Figure 5-15 Example: inappropriate time constant

The time constant is too small to cover the whole start-up interval. During start-up, output current shows significant overshoot by approximately 100% of $I_{o,nom}$ as a result. The inductor current is first seized to low level (first half mains cycle) but shifts to high level afterwards. This excessive inductor current finally translates into output current overshoot. Therefore, it is necessary to tune the capacitor value to achieve a gradually increasing output current.

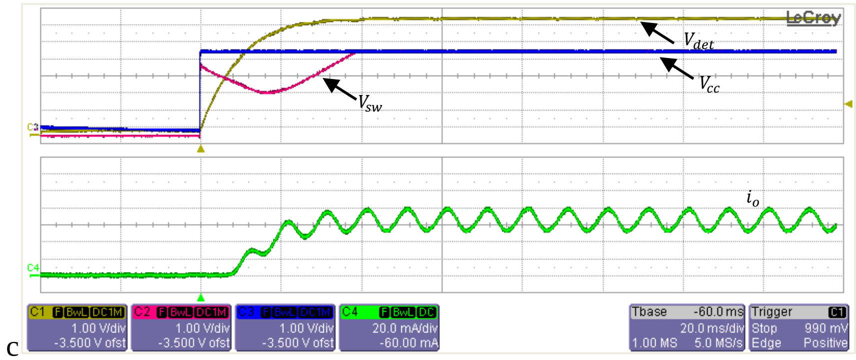
Start-up waveforms of the same prototype are captured in four different operation modes: series mode with EM ballast, series mode without EM ballast, independent mode with EM ballast and independent mode without EM ballast. The AC voltage source starts up at 90 degree to emulate the worst start-up case, which will most probably cause current overshoot.



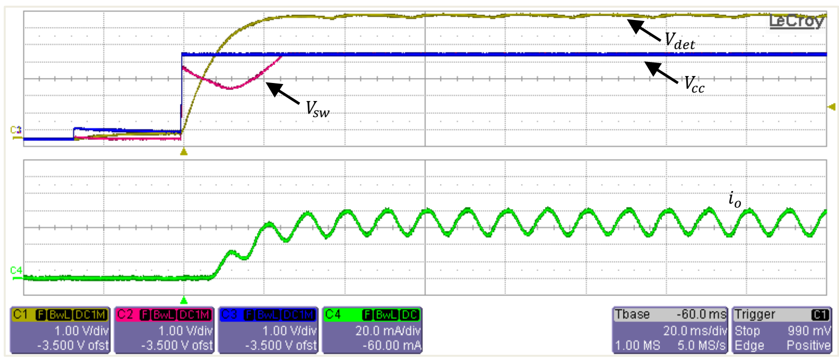
(a) Series-mode without EM ballast



(b) Series mode with EM ballast



(c) Independent mode without EM ballast



(d) Independent mode with EM ballast

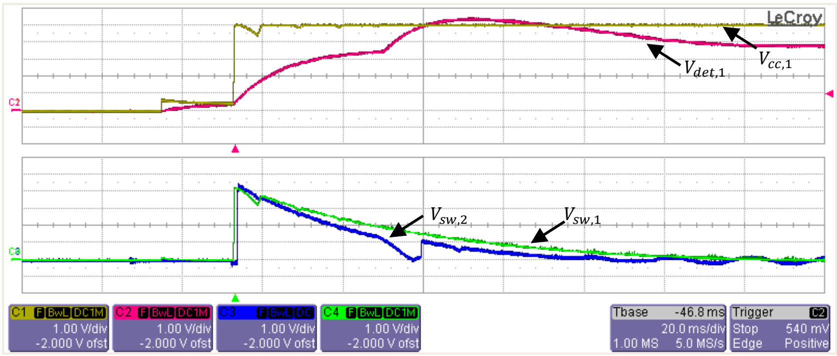
Figure 5-16 Detection waveforms in start-up interval

The detection and mode selection circuit is functioning well for all four situations in that they all enter the correct operation mode with a smoothly increasing output current. At the same time, the compatibility with two reference EM ballasts is not a problem.

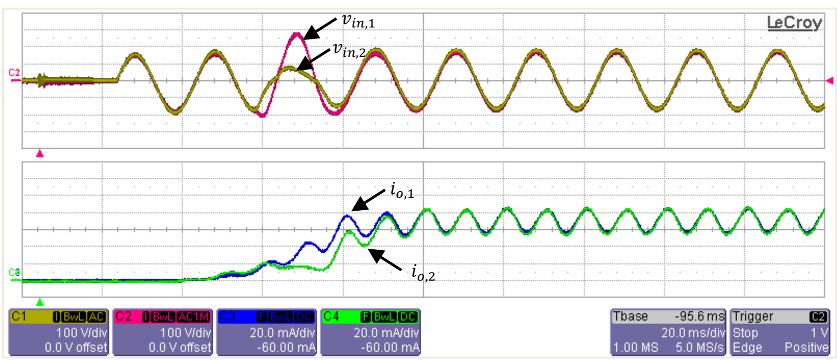
The small triangular spots observed in Figure 5-16(a) are due to the large voltage ripple over the input capacitor C_8 of TL431. The self-oscillating during start-up interval is not sufficient to maintain a nearly steady voltage at C_8 and hence the output of TL431 fluctuates. This phenomenon is observed in series mode only since auxiliary winding voltage is halved and the capacitor is charged up relatively slowly. In steady-state, however, TL431 gives stable V_{cc} voltage without visible fluctuation.

A mismatch in start-up time is mimicked by increasing C_{13} value, which slows down the transition from default mode into series mode. In prototype #1, the capacitor value C_{13} is increased from $100nF$ to $147nF$, which result in more out-of-sync V_{sw} signals. Figure 5-17(a) shows the experimental waveforms of detection signals.

Prototype #2 first enters series mode with a faster decreasing $V_{sw,2}$ and hence exhibits a smaller input impedance, while prototype #1 still stays in the default low-current mode with a larger input impedance. This explains the significant uneven sharing of input voltage during the third mains cycle in Figure 5-17(b). As a result of the voltage re-distribution during the transients, detection voltage of prototype #1 $V_{det,1}$ increases with a steeper slope but still does not exceed the threshold voltage. $V_{sw,2}$ also dramatically drops since the input voltage is too low to maintain a stable power supply voltage $V_{cc,2}$. Finally, prototype #1 also enters the series mode and stable input voltage sharing is observed after around 4 mains cycles.



(a) Detection signals

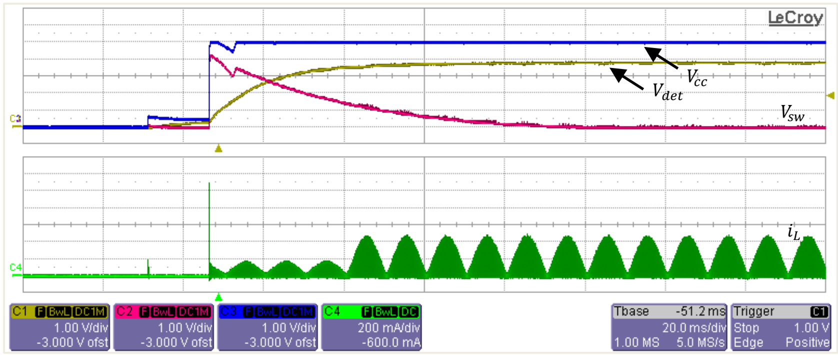


(b) Input voltages and output currents

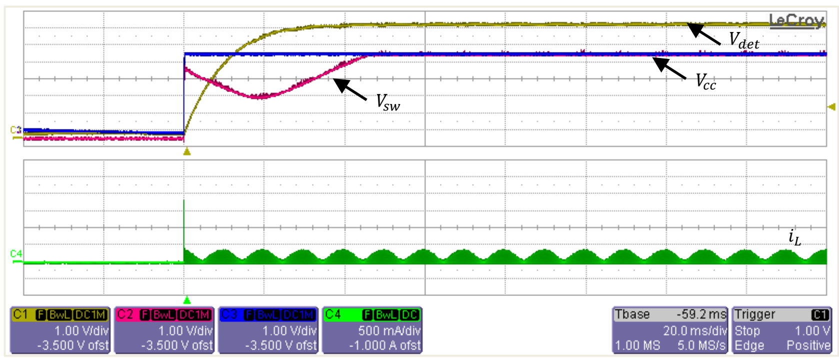
Figure 5-17 Detection performance with start-up time mismatch

In general, the start-up time of a self-oscillating converter will not vary obviously from one to another since the start-up resistor has limited tolerance. By changing the capacitor value to 150%, the experiment can readily emulate the worst case during start-up.

It is also mentioned that inductor current is not controllable before V_{cc} is built-up. Figure 5-18 shows the inductor current overshoot when D_5 is a general-purpose diode. Current overshoot is overserved during a limited start-up interval. A $I_{ovs} = 1.1A$ current overshoot is observed during V_{cc} built-up time of $t = 161.8us$ in series-mode. It is even more significant in independent mode due to the high input voltage. V_{cc} is established faster within $t = 116.2us$ but the current overshoot has an amplitude of $I_{ovs} = 1.8A$, which shall bring potential risks.



(a) Series mode without EM ballast



(b) Independent mode without EM ballast

Figure 5-18 Inductor current overshoot with general diode D_5

When the freewheeling diode D_5 is replaced by a zener diode, it is possible to limit that overshoot to an acceptable level. Figure 5-19 shows the result. The current overshoot in independent mode is reduced to approximately 1.2A.

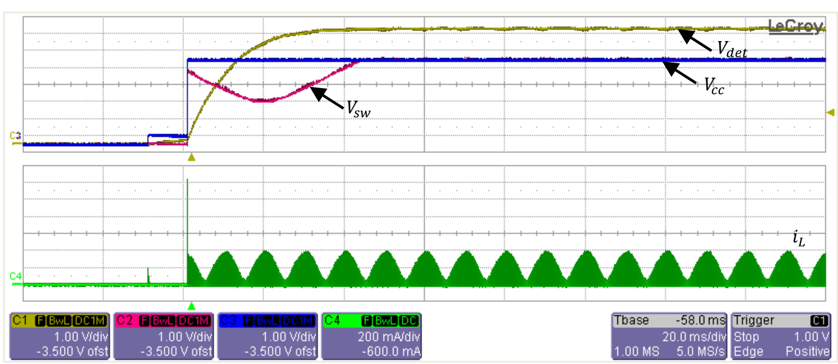
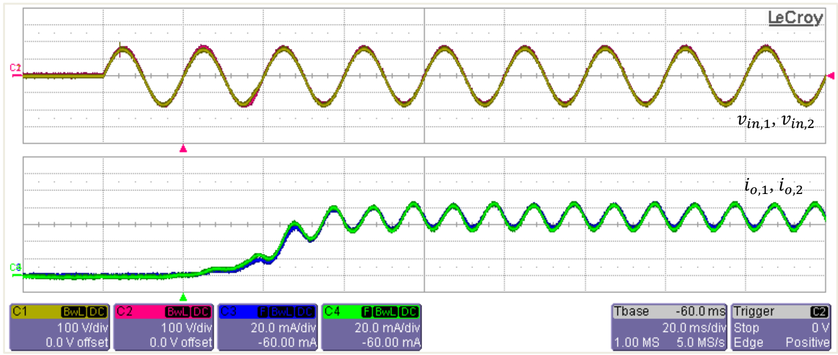
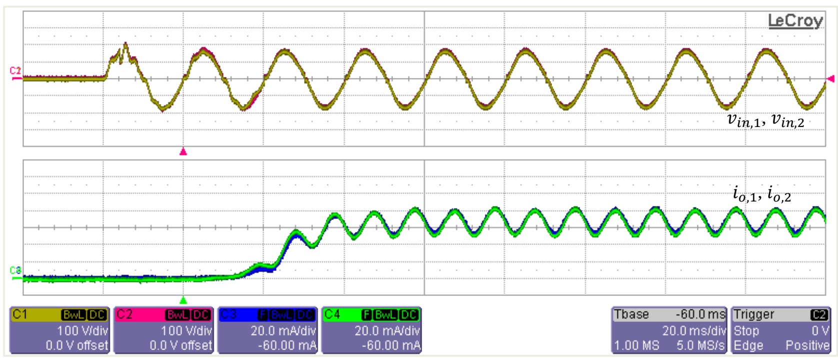


Figure 5-19 Inductor current overshoot after zener replacement

Input voltage sharing is always a concern in an input-series system as it is a prerequisite for system stability. It can be an issue during start-up if the mode-select action is non-simultaneous in two lamps. Figure 5-20 presents the input voltage sharing during start-up of the prototypes. A small DC component exists for a short while after the AC source is powered on but disappears after several mains cycles.



(a) Without EM ballast

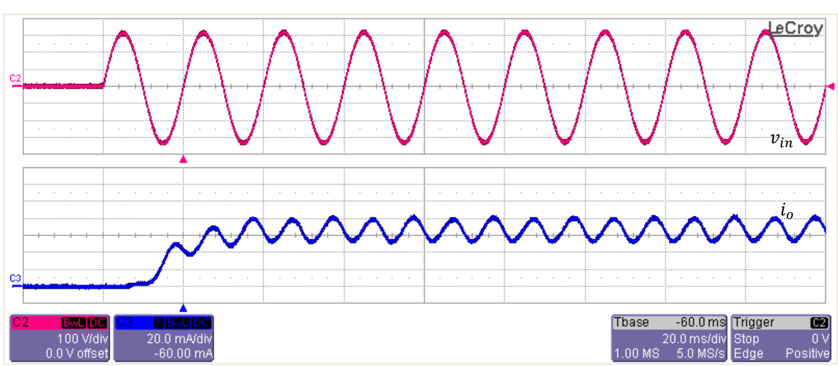


(b) With EM ballast

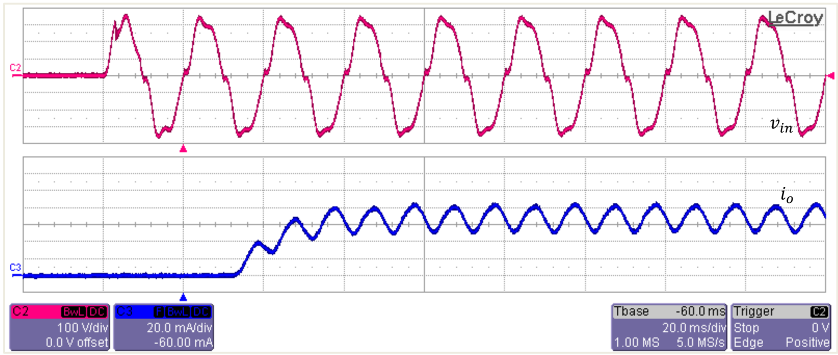
Figure 5-20 Series mode start-up waveforms

It can be concluded that the system is stable during start-up interval. The input voltage is nearly equally shared and output currents overlap with each other. A start-up time of $50\sim60ms$ is needed for this input-series system to stabilize its output current. When operating with EM ballast, the oscillations between EM ballast (L) and input EMI filter (C) are observed. After two mains cycles, the oscillations are dumped out.

The start-up input voltage and output voltage waveforms for independent mode are followed in Figure 5-21. Due to a higher input voltage, it takes around $20\sim30ms$ for output current to stabilize in this mode. A similar oscillation in between the EM ballast and EMI filter is observed.



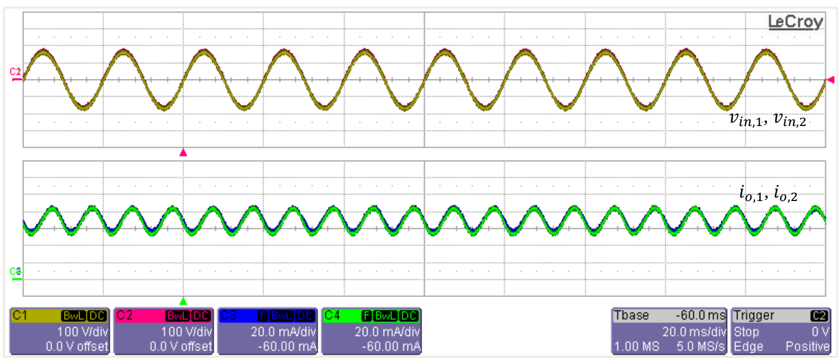
(a) Without EM ballast



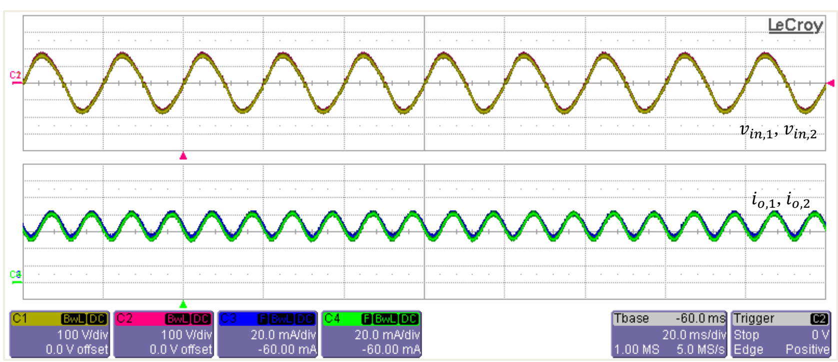
(b) With EM ballast

Figure 5-21 Independent mode start-up waveforms

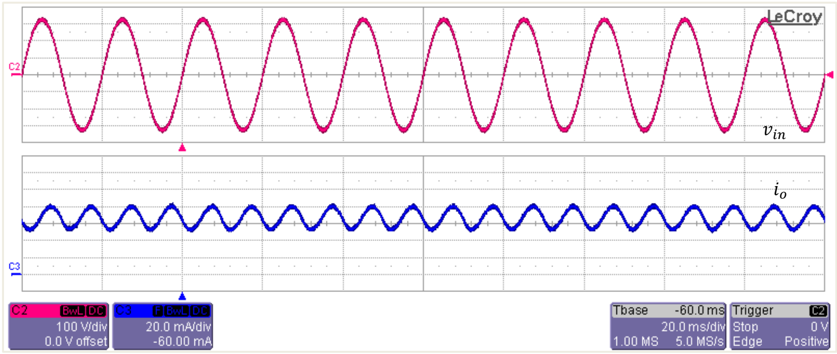
The steady-state operation waveforms are captured for four different operation modes accordingly. In series-mode steady state, two drivers are in balance in aspects of input voltage and output current, indicated by the following Figure 5-22(a) and (b). The input voltage and output current waveforms for independent mode are also shown.



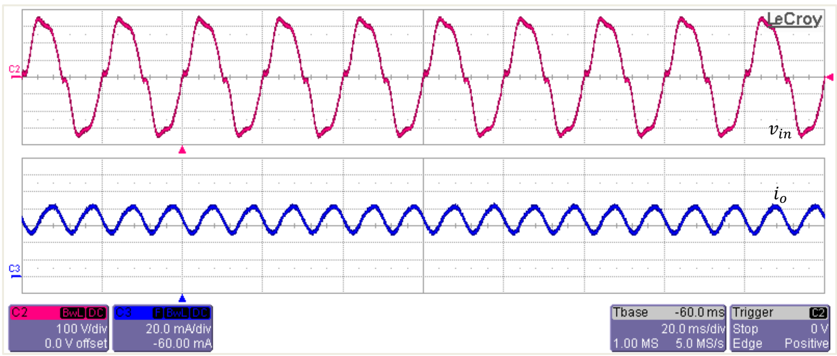
(a) Series mode without EM ballast



(b) Series mode with EM ballast



(c) Independent mode without EM ballast



(d) Independent mode with EM ballast

Figure 5-22 Steady-state operation waveforms

Input voltage is a little bit distorted near the zero-crossing points but the peak voltage is unchanged anyhow. Compared with series mode, the input voltage is more distorted with peak voltage value increased by $30V$. It hence imposes extra stress on the components that should be taken into consideration. Peak to average output current ripple in steady state are measured.

Operation mode	Peak-to-peak current ripple/mA	Peak-to-average current ripple/%
Series without EM ballast	34.4	23.8
Series with EM ballast	34.8	24.2
Independent without EM ballast	34.3	23.8
Independent with EM ballast	37.9	26.3

Table 5-6 Current ripple measurements

5.7 Summary

This chapter present a complete design-to-implement procedure of a retrofit LED driver, based on the proposed control strategy. The designed driver is electrically compatible with the existing fluorescent lighting fixtures as a drop-in replacement.

Emphasis is placed on the design of detection and mode-selection function to enable a self-adapting driver in different operating conditions, which depend on the luminaire. Once powered on, the driver detects the input voltage and automatically enables the corresponding control. Other design considerations include the low-current default mode setting during start-up transients, avoidance of inductor current overshoot and internal power supply built-up.

The performance of two driver prototypes are evaluated in various aspects. The steady state measurements meet all the electrical specifications at nominal input voltage with reference ballasts. Start-up and steady states operating waveforms also validate the design.

Chapter 6 Conclusion and Recommendations

6.1 Conclusions

This research work mainly investigates series operation of switched-mode power supply for 2ft LED retrofit lighting applications. The major contents are:

- **Propose a modulated peak current controlled self-oscillating buck-boost converter for stable series operation**

The stability criterion for an input-series system is first concluded with theoretical analysis according to simplified SMPS input characteristics: the input-series system will be stable if both constituent modules have (finite) positive dynamic input resistance.

The state-of-art control strategies that are already implemented in current input-series systems are evaluated and compared in both open-loop and closed-loop categories. A practical limitation for closed-loop solution is the communication requirement, which is not easily fulfilled in current application. On the basis of related work, a modulated peak current controlled self-oscillating buck-boost converter is proposed to realize stable series operation. It is an open-loop approach and the controller follows a simple control equation, which sets the peak inductor current reference with two coefficients a and b.

$$I_{L,pk} = aV_{in} + b \qquad a, b > 0$$

The sufficient stability condition is derived mathematically as,

$$aV_o - b > 0$$

The proposed approach is generally valid for an input-series system design and has several advantages: easy implementation with discrete components, close-to-zero sensitivity to inductor value and temperature, and the feasibility in adjusting driver characteristics with two coefficients a, b.

Principle verification is carried out with *LTSpice* simulations and two prototypes are built to validate the proposed control strategy. Input-series systems based on different control options are built and evaluated in terms of system stability and circuit sensitivity to component tolerances. In a stable input-series system, circuit sensitivity is further studied by means of measuring output current unbalance brought by various component tolerances, which is important to an open-loop solution.

- **Demonstrate with a complete driver design: LED driver for retrofit replacement**

A complete design-to-implement procedure of a 7.5W EM ballast compatible driver for retrofit LED lighting applications further illustrates the control principles with a detailed case study. The proposed driver is electrically compatible with existing fluorescent lighting fixtures as a drop-in replacement. Special design considerations are given to detection and mode-selection, default low-current mode for soft start-up (avoidance of current overshoot) and removal of external power supply.

Two experimental prototypes are built to validate the design. The steady state measurements meet all the electrical specifications, including output current, THD, efficiency and etc. Besides, all other functionalities are also achieved. These include stable series- and independent-mode operation, mains and EM ballast compatibility, detection and mode-selection function. In series mode, inductor value and LED voltage tolerance induced output current unbalance is limited to the required range.

To conclude, the research work delivers the expected outcomes and give answers to the corresponding research questions.

6.2 Recommendations and Future Works

The open-loop approach based on modulated peak current control makes good compromise in system simplicity and overall performance. However, an open-loop controlled switched mode power supply always has an intrinsic drawback on line regulation performance. The impact of input variation may be alleviated to some extend by means of complicated modulation but cannot be eliminated completely. This research work doesn't dive into the line regulation performance improvement but it is helpful to further investigate in future works.

Despite of its implementation complexity, a closed-loop based solution has many benefits that have been discussed. With a dedicated control loop, input voltage sharing can be achieved with high accuracy and output current balance won't be sensitive to component tolerances at all. Line regulation performance is also believed to be better. Currently the implementation of a closed-loop control is practically limited by the re-wiring requirement to enable communication function.

In future works, alternative communication options via power line maybe a method so that two lamps can pass on information from one to the other. For instance, a novel signal transmission method based on power line communication that seems feasible is proposed in [47]. It utilizes PWM carriers of different frequency to transfer 0 or 1 to the DC bus while keeping the converter power regulation not affected. In addition, the feasibility to construct an input-series system without communication also needs to be investigated, which will eventually decouple the system into modular concept. It is not only meaningful for retrofit LED drive design and most importantly, for input-series system design.

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