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DOI
10.1016/j.mssp.2019.03.008

Publication date
2019

Document Version
Final published version

Published in
Materials Science in Semiconductor Processing

Materials Science in Semiconductor Processing 97 (2019) 67–70

Contents lists available at ScienceDirect

Materials Science in Semiconductor Processing

journal homepage: www.elsevier.com/locate/mssp

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ARTICLE INFO

Keywords:
Thermal oxidation
Amorphous silicon passivation
Defect encapsulation
Silicon heterojunction solar cells

ABSTRACT

This work shows an alternative surface cleaning method for c-Si wafers to replace the standard chemical procedures as RCA or HNO_3 which involve hazardous chemicals or unstable processes. The method consists in a high-temperature oxidation treatment (HTO) performed in a classical tube furnace that incorporates organic and metal particles present on the c-Si surfaces in the growing SiO_2 layer. The result is as a reliable pre-treatment method for obtaining less defective c-Si surfaces ready for solar cell fabrication after SiO_2 removal. To test the surface passivation quality obtained with our alternative cleaning method, we grow amorphous silicon (a-Si:H) layers by plasma enhanced chemical vapor deposition on both sides of the c-Si wafer and systematically compare the effective carrier lifetime (τ_{eff}) and implied V_{OC} (iV_{oc}) to the wafer treated with the standard cleaning in our laboratory. We optimize HTO treatment time reaching τ_{eff} of ~6 ms and iV_{oc} of 721 mV for the best sample. We ascribe the improved passivation quality using HTO to two concurrent factors. Firstly, the encapsulation of defects into SiO_2 layer that is then etched prior a-Si:H deposition and secondly, to modification of the pyramids' morphology that facilitates the surface passivation. SEM pictures and reflection measurements support the latter hypothesis.

1. Introduction

In both semiconductor and photovoltaic industries, the cleaning of the crystalline silicon (c-Si) wafers to remove residues prior device fabrication is a crucial step. Therefore, wafers are dipped in chemical baths to remove organic and metallic impurities from the Si surfaces. The most commonly used procedure consists in a cycle of oxidation-etching steps in order to encapsulate all the surface contaminants into thin SiO_2 grown on the c-Si surface and etch them away using highly diluted hydrofluoric acid (HF) [1–4]. This method is fundamental to achieve high performance devices. Indeed, a contamination-free Si surface will reduce defect density at interface, giving higher passivation quality than a not-treated surface [5,6]. This thin oxidation is often done via RCA cleaning [7] or ozone-based treatment [8]. Alternatively, the use of so-called nitric acid oxidation cycle (NAOC) results in comparable lower surface recombination velocity [9]. Both mentioned cleaning methods involve hazardous chemical substances that make the treatment costly owing to the disposal of the chemical waste, safety and environmental risks. Therefore, alternative cleaning methods might be attractive to reduce costs and simplify the fabrication of devices, such as c-Si solar cells. Attempts to reduce number of steps in the cleaning procedure were made by Lu et. al. [10]. with promising values of saturation current density (J_0) below 10 fA/cm^2. Hydrogen plasma pre-treatment is eventually used to hydrogenate c-Si bulk [11]. Also, replacing the final HF etching step with hydrogen plasma etching was suggested by Mueller et. al. [12].

In this work, we propose a novel wafer cleaning method that consists in a single-step high temperature oxidation (HTO) followed by SiO_2 etching in diluted HF solution. This method can be evidently deployed also in batch mode. As a result of volume expansion process, the HTO process consumes c-Si surface such that organic/metallic contaminants are encapsulated into SiO_2 layer. Typically, ~50% of the total SiO_2 thickness is expanded into Si during thermal oxidation process [13]. Moreover, also impurity gettering is performed during this process. A similar approach has been developed in Ref. [14], with gettering and hydrogenation of the wafer through SiN_x layer and rapid thermal firing. We investigate the passivation quality of double-side textured wafers treated with HTO for variable treatment time by passivating the c-Si surfaces with a-Si:H layers growth via plasma enhanced chemical vapor deposition (PECVD). These a-Si:H layers provide both chemical and field-effect passivation. We compare the HTO-treated samples to a wafer treated with the standard wet-chemical oxidation NAOC method. The better passivation quality obtained with the optimized HTO treatment time is related also to morphology

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https://doi.org/10.1016/j.mssp.2019.03.008
Received 11 September 2018; Received in revised form 4 January 2019; Accepted 8 March 2019
Available online 15 March 2019
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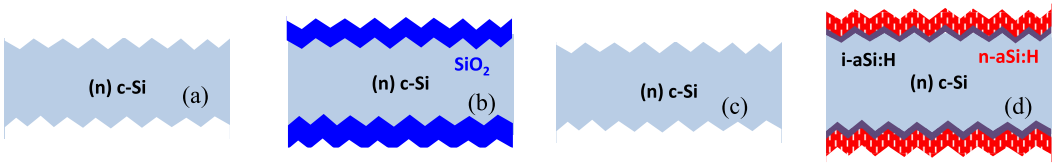

Fig. 1. Sample fabrication steps: (a) Chemical texturing of the wafer; (b) Thermal oxidation of double sided textured wafer; (c) Etching of SiO_2 in HF; (d) i/n a-Si:H stack PECVD deposition as a passivation layer.

modifications of the random pyramids that additionally facilitate the growth of high quality a-Si:H layer.

2. Experimental details

For symmetric samples fabrication, we use 4 inches n-type float zone (FZ) silicon wafers (c-Si) with polished < 100 > oriented surfaces, a resistivity of 2.5 Ω cm and initial thickness of 280 µm. The c-Si substrates are cleaned in a nitric acid (99% HNO_3) bath for 10 min at 20 °C, followed by a dip in 69.5% HNO_3 at 110 °C to remove organic residuals and metallic contaminations, respectively. Samples are then chemically textured in a solution containing TMAH, AlkaText® and H_2O to obtain random pyramids with < 111 > oriented facets on both sides of the wafer (Fig. 1 (a)).

Then, the wafers are subjected to HTO process in a tube furnace (Tempress Systems) at a temperature of 1050 °C in O_2 atmosphere. The treatment time is varied between 20 and 230 min that corresponds to a resulting SiO_2 film of from 40 to 200 nm-thick (Fig. 1 (b)). The temperature is reached with a ramp of 10 °C/min and the O_2 flow is set at 3 slm in a dry environment. After oxidation, we remove the SiO_2 layer by dipping the sample in 0.55% HF (step (c) in Fig. 1) with an etching rate of ~1 nm/m for the necessary time to make the silicon wafer surface hydrophobic. Instead, the reference wafer is treated with the so-called nitric acid oxidation cycle (NAOC) method, consisting in HNO_3 99%, subsequent HNO_3 69.5% and HF step, as described in Ref. [15], that we repeat three times [9]. Finally, the samples are loaded into the PECVD reactor where both sides of the c-Si substrate are covered by a stack of intrinsic and phosphorous doped a-Si:H layers with a thickness of 4.5 and 6 nm, respectively (step (d) in Fig. 1). Afterwards, the samples are annealed at 190 °C for 30 min to enhance passivation quality [16]. Quasi-steady-state photoconductance (QSSPC) lifetime measurements [17] are performed on the fabricated samples using a Sinton Instruments WCT-120 carrier lifetime setup. Effective lifetime (τ_{eff}), implied open-circuit voltage (iV_{OC}) and recombination current density (J_0) are extracted from the measured curves. Furthermore, the as-textured and the optimized HTO treated samples are further characterized by cross-sectional scanning electron microscopy (SEM XL50 Philips with acceleration voltage of 5 kV) and optical reflectance is carried out using a Pelkin Elmer Lambda UV-VIS near-infrared spectrophotometer.

3. Results and discussion

Fig. 2 shows the minority carrier lifetime against injection level for double-sided textured wafers passivated by i/n a-Si:H stack pre-treated with variable HTO time and compared to the reference pre-treated with NAOC. All the results shown here are after annealing at 190 °C for 30 min to improve chemical passivation [18]. The reference sample (black curve in Fig. 2) shows τ_{eff} of ~2 ms extracted at 10^{15} cm^{-3} injection level. By increasing the HTO time, the measured lifetime progressively increases as compared to the value of the reference. For the shorter HTO times tested (from 22 to 56 min), the passivation quality improvement is limited only to the low injection level. We observe a slight decrease in lifetime of around 200 µs at low injection level when 37 and 56 min HTO treatment are applied. This is most likely due to different pre-conditioning of the PECVD chamber since the samples

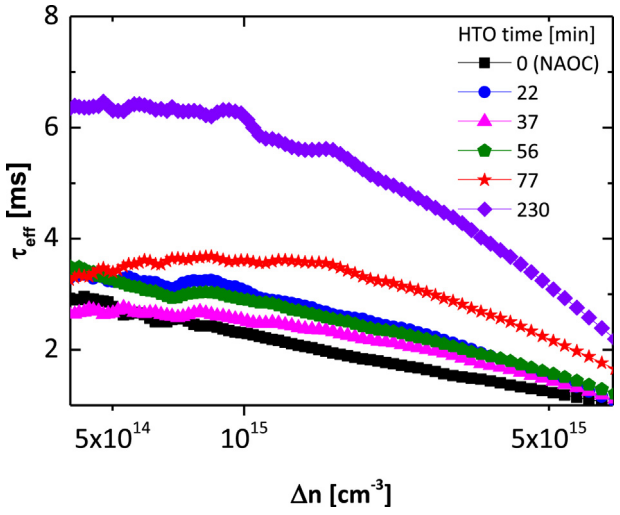

Fig. 2. Minority carrier lifetime versus carrier density of double sided textured wafers passivated by 4.5/6 nm-thick a-Si:H for a variable HTO treatment time. The curves are measured after a post-deposition annealing at 190 °C for 30 min. Reference samples cleaned with NAOC is also added for comparison.

have been processed in different time slots. It is remarkable how similar values of lifetime at high injection level are achieved in the NAOC and 37 and 56 min HTO cases. When a sample is oxidized for 77 min, corresponding to ~100 nm-thick SiO_2, lifetime improves significantly both in high and low injection level with τ_{eff} of ~4 ms which doubles the value measured for NAOC reference.

By increasing the HTO time to 230 min (~200 nm-thick SiO_2 layer) the entire curve shifts up with τ_{eff} of ~6 ms at 10^{15} cm^{-3} injection level.

Fig. 3 displays the implied V_{OC} and J_0 extracted from the curves in Fig. 2 as function of the HTO treatment time. We clearly note the effect described above with a progressive increase in iV_{OC} (i.e. surface

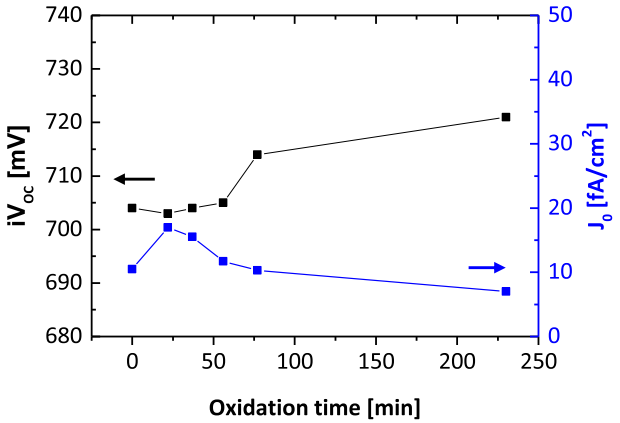

Fig. 3. Implied V_{OC} and saturation current density (J_0) of double-sided textured wafers passivated by 4.5/6-nm thick i/n a-Si:H with NAOC or thermal SiO_2 pre-treatment as function of the oxidation time.

chemical passivation) with increasing thickness of the SiO_2 layer. For the NAOC reference sample, iV_{OC} is 705 mV, while the highest iV_{OC} of 721 mV is measured for the sample treated with 230 min of HTO. The opposite trend is noted for J_0. For the NAOC reference, J_0 is 12 fA/cm^2, while for the sample pre-treated with 230 min of oxidation, J_0 decreases to 7 fA/cm^2.

We can conclude that the passivation quality of i/n a-Si:H stack is then affected by HTO treatment time and therefore by the grown SiO_2 thickness. We tentatively explain the improved surface passivation obtained with HTO by the encapsulation of surface contaminants present on the Si surface within thermal SiO_2, which partially expands into the Si bulk. All these surface contaminants are then etched away by removing the SiO_2 in HF solution. This results in a *clean* c-Si surface ready for passivation by a-Si:H stack. Increasing the HTO time, SiO_2 goes deeper into the Si bulk and more impurities are removed from Si surface [19]. An enriched chemical passivation is achieved by $J_0 < 10$ fA/cm^2. This indicates that more surface contaminants have been removed from the surface than in the NAOC case.

It is noteworthy to remark how the proposed HTO process is capable of improving performances in FZ wafers. By transferring this method to industrially-relevant Czochralski wafers (CZ), the encapsulation of surface impurities into SiO_2 and stabilization of bulk lifetime by the so-called *tabula rasa* treatment [20] can be achieved at the same time.

To further analyze the effect of HTO on the c-Si wafer surface, we rely on cross-sectional scanning electron microscopy (SEM). Fig. 4 (a) shows a SEM image of an as-textured wafer, while Fig. 4 (b) is the image taken after HTO treatment (230 min) and subsequent etching of SiO_2. The scale is slightly different due to different focus obtained to have optimal images. The reference textured wafer in Fig. 4 (a) has

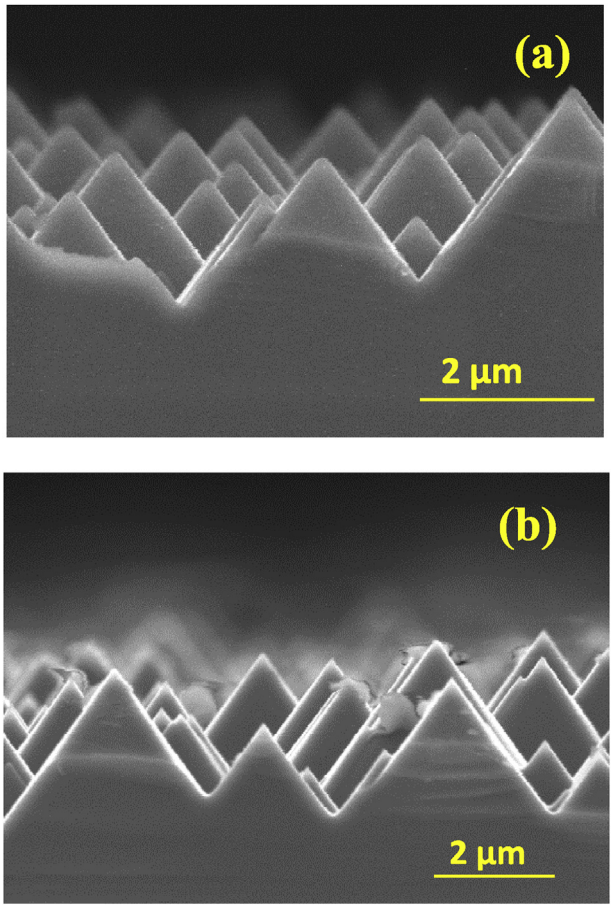

Fig. 4. Cross-sectional Scanning Electron Microscopy (SEM) of textured wafers (a) after texturing and (b) 230 min of HTO treatment. Both images are taken after etching the SiO_2 layer.

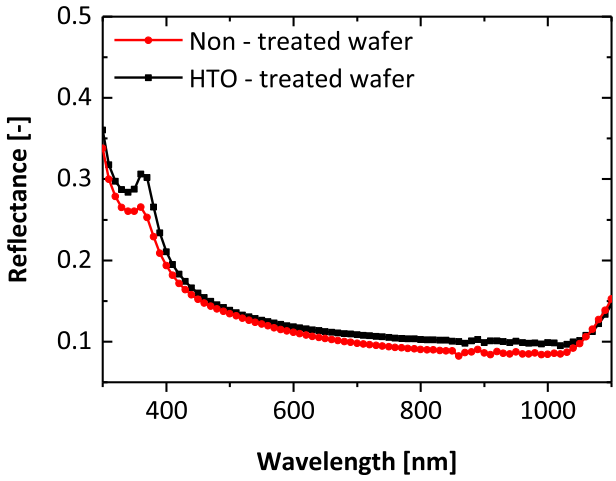

Fig. 5. Measured reflectance of reference (red line) and HTO-treated (black line) wafers.

steep valleys of the pyramids. On the other hand, the HTO-treated wafer has rounded valleys; therefore, the amount of defects is decreased. In general, the more the tip or the valley of a textured wafer is rounded, the less is the structural defect density associated to it [21]. Therefore, it is easier to obtain enriched chemical passivation. In particular, the more the valley is rounded, the more it is unlikely to have epitaxial growth of a-Si [22]. This concurs to the improved passivation properties. The images reveal residuals that are the results of a cut in 6-cm wide slab to fit the cross-sectional stage of SEM. The drawback of this procedure stays in the slightly reduced reflectivity due to not perfect light scattering and reduced optical path length in the c-Si wafer [23]. Fig. 5 shows the reflectance exhibited by the same wafers shown in Fig. 4. In the whole wavelength range, the reflectance is lower for the HTO-treated wafer. Therefore, light scattering is more efficient in the reference sample than the HTO-treated one. We can conclude that, although the pyramids' size is the same in both textured and HTO-treated cases, the pyramids' valleys are slightly more rounded in the HTO-treated case compared to as-textured wafer. This issue can be nevertheless overcome by using transparent conducting oxide layer or anti-reflective dielectrics, such as MgF_2 or SiO_x [24].

4. Conclusion

In conclusion, we investigate an alternative cleaning method suitable for textured c-Si wafers that does not involve the use of hazardous chemicals. This method consists in a high-temperature oxidation (HTO) treatment in a conventional furnace followed by an etching step HF solution prior further processing the substrate for device fabrication. To measure the passivation quality, the textured c-Si surfaces are covered with a-Si:H layers deposited by PECVD. Since the HTO encapsulates Si surface impurities, we perform a series of HTO treatment time to investigate the impact on chemical passivation. After HF etching, the wafers are immediately transferred to PECVD chamber to deposit 4.5/6 nm-thick i/n a-Si:H layer. These samples have been characterized using QSSPC method and compared to a sample equally passivated but pre-treated with 3 cycles of thin wet-oxidation and HF etching (NAOC). This analysis is carried out by passivating the textured wafer by 4.5/6 nm-thick i/n a-Si:H, but the conclusions drawn are the same for other a-Si:H layer thicknesses. We find out that increasing oxidation time, i.e. thermal SiO_2 thickness, both carrier lifetime and implied V_{OC} progressively improved and exceeded the values measured on the reference sample treated with NAOC. The best HTO treatment time is found at 230 min with τ_{eff} and iV_{OC} of 6 ms and 721 mV, respectively. Since the passivation layers stack is kept constant for all the samples fabricated, we can conclude that the improvement in chemical passivation are to

be ascribed to the removal of impurities from the c-Si surface and to the formation of rounded valleys after etching the thermally-grown SiO_2, as shown by cross-sectional SEM images. It is to remark that HTO process can be applicable also to planar wafers. The drawn conclusions are the same except for less defect density of the polished c-Si interface compared to textured one. This method could be further engineered and optimized for batch process compatible with mass production. Moreover, this method is also beneficial for industrial CZ wafers, since a *tabula rasa* could be performed at the same time with encapsulation of defects.

Acknowledgment

The authors would like to thank ADEM program for funding this research and Martijn Tijssen for his help with PECVD reactor.

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