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DOI
10.1109/TIM.2022.3160529

Publication date
2022

Document Version
Final published version

Published in
IEEE Transactions on Instrumentation and Measurement

Characterization Challenges of a Low Noise Charge Detection ROIC

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***Abstract*— This article presents the experimentally characterized performance of a low noise and wideband sensor readout integrated circuit (ROIC). The ROIC is designed to detect small amounts of charge generated by a silicon p-i-n detector as a result of particle detection, with very high time resolution and limited power consumption. The architecture of the ROIC permits the analog components of the particle readout to be designed with a reduced bandwidth by implementing the so-called intersymbol interference (ISI) cancellation technique, which improves the noise performance, while reducing the deterministic ISI-induced errors associated with the narrowband circuit; hence, a low error rate (ER) can be maintained. The readout is designed to detect 160 aC charge portions delivered randomly by the detector at a maximum of 4×10^8 events/s with a small average ER while consuming 2.85 mW. Detailed information about the ROIC designed in 65-nm CMOS technology, and the simulated performance, are already reported in a previous publication. This article aims to present the challenges related to the design of the test setup and the obtained experimental results with the first prototype of the ROIC, as well as to discuss the data acquisition process.**

***Index Terms*— Characterization, data acquisition, double-threshold technique, low noise, low power, readout front end, wideband.**

I. Introduction

THE experimental environment for qualifying high-performance sensor readout circuits requires advanced electronic instrumentation which complies with very challenging specifications in terms of noise, processing speed, time resolution, and power consumption [1]–[3]. The device under test (DUT) is a low noise and wideband readout integrated circuit (ROIC) operating based on an intersymbol interference (ISI) cancellation scheme to detect small amounts of charge generated by a silicon p-i-n detector as a result of particle detection, with a very high time resolution in the order of nanoseconds and limited power consumption. Detailed information about the ROIC designed in 65-nm CMOS technology, and the simulated performance, are already reported in a previous publication [4]. The ROIC, as illustrated in Fig. 1, has the following functional blocks: a trans-impedance amplifier (TIA), followed by a voltage amplifier, and a discriminator.

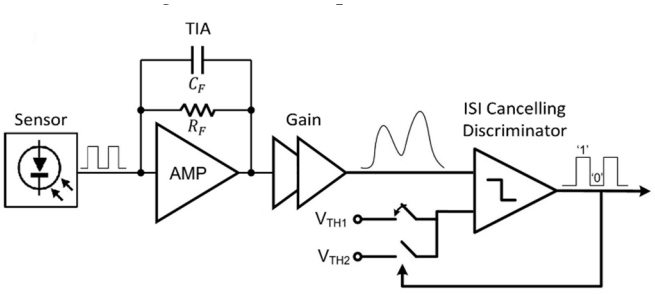

Fig. 1. Block diagram of the double-threshold technique.

In order to reach the required accuracy for event detection, the double-threshold charge detection technique is used in the discriminator. The main idea behind this technique is to relax the TIA and amplifier bandwidth requirement, with the aim to reduce both power consumption and the integrated noise while compensating for the induced pileup of the signals (called ISI) due to the limited bandwidth at the output by adding a small amount of architectural complexity [4]. In this way, a low detection error rate (ER) can be achieved with reduced signal bandwidth, despite the ISI in the case of two events, one occurring shortly after the other. In this regard, a double-threshold comparator (see Fig. 1) is used in the discriminator to detect input signals in the case of a pile-up, helping to reduce the ER. In addition, to reach a good time resolution for the landing event, a clock period of 2.5 ns is chosen, allowing an event rate up to 4×10^8 events/s [4].

Regarding the post-layout simulations, the proposed architecture can detect 160 aC charge portions (equivalent to 1000 e^-) arriving with a Poissonian distribution at a maximum rate of 4×10^8 events/s with average ERs of 23% in single-threshold and 2.2% in double-threshold mode within the optimal operation. The readout channel consumes 2.85 mW of power and occupies an 8000 μm^2 area [4]. A microphotograph of the chip, packaged in a QFN-32 package, is shown in Fig. 2.

This article presents the test setup designed to evaluate the performance of the first prototype of the proposed architecture, including the assessment of the efficacy of the double-threshold technique. We discuss the challenges related to the experimental qualification tests and data acquisition. The focus of the presented qualification tests is on the optimization of

Manuscript received December 21, 2021; revised February 16, 2022; accepted March 7, 2022. Date of publication March 17, 2022; date of current version March 31, 2022. This work was supported by the Dutch Top Consortium for Knowledge and Innovation (TKI) HTSM. The Associate Editor coordinating the review process was Ferran Reverter. *(Corresponding author: Alireza Mohammad Zaki.)*

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Digital Object Identifier 10.1109/TIM.2022.3160529

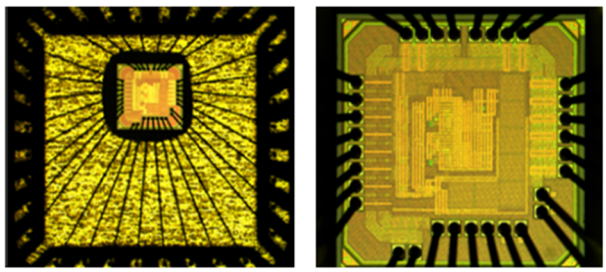

Fig. 2. Microphotograph of the chip.

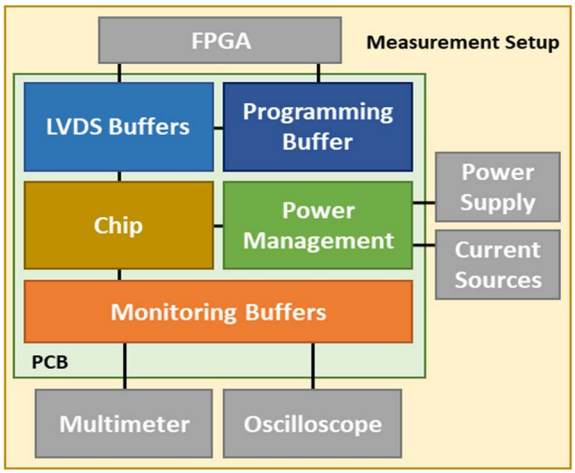

Fig. 3. Measurement setup and isolation buffers.

both threshold levels and estimation of the detection ER in single and double-threshold modes.

Section II introduces the measurement setup and the ROIC internal blocks. In Section III, challenges concerning the data acquisition process that can degrade the detection ER (e.g., noise, sampling, and threshold levels) are recalled and tackled by a set of chip debugging features. Section IV provides the experimental results for the evaluation of the data acquisition process, optimization of the threshold levels, and calculation of the detection ER in both single and double-threshold modes. The article ends with conclusions.

II. ROIC Measurement Setup

The measurement setup consists of a power supply and two current sources to bias the chip and generate the charge injected into the readout channels, a field-programmable gate array (FPGA) to program and test the readout channels, and an oscilloscope for signal monitoring. Test setup devices are connected to the chip through isolation buffers implemented on the printed circuit board (PCB) (see Fig. 3) and in the chip itself, to reduce the peripheral noise injection and to avoid loading effects.

Fig. 4 presents the internal block diagram of the ROIC with two parallel readout channels. There are some additional functional blocks for programming, readout channel testing, and input signal generation provided by a digital-to-analog

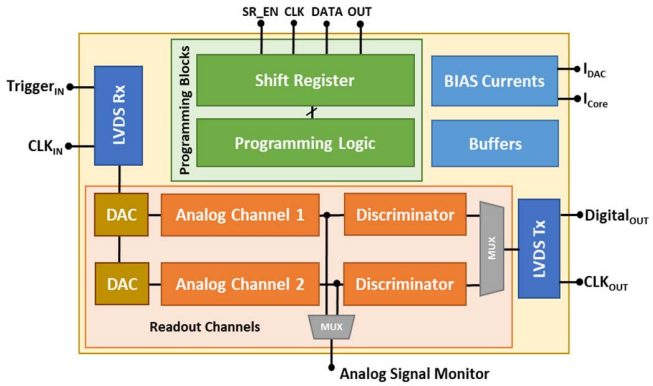

Fig. 4. Internal architecture of the chip.

converter (DAC). The programming blocks contain a 37-bit shift register (SR) to store the chip program, transmitted by an FPGA, and a set of switches (programming logic block) to apply the desired changes into the readout channels. The FPGA, through a high-speed low-voltage differential signaling (LVDS) interface, transmits a 400-MHz sampling clock to the comparator for signal discrimination and a trigger signal to the DAC for input signal generation. The readout channels reply to the FPGA through a single-bit digital line that rises to logical "1" once the injected charge is detected.

A. Chip Programming

Through chip programming, the internal parameters of the readout channels are set to test the chip functionality and evaluate the response efficiency under different working conditions. The FPGA and SR communicate through four wires, all isolated by an external integrated circuit (IC) labeled the programming buffer in Fig. 3. To program the SR, the FPGA must activate the programming mode of the chip by setting the pin SR_EN to logical "1," and in the next step, transmit a 1-MHz programming clock signal and a 37-bit data vector to the CLK and DATA pins, respectively. In contrast, to check the accuracy of the transmission and programming, the FPGA can read the data stored in the SR through the OUT pin. Through programming, the following parameters can be set: a model of the detector capacitance (C_D) implemented at the input of each readout channel, the values of the feedback components (C_F and R_F) of the TIA, the threshold voltage levels (V_{TH1} and V_{TH2}) of the discriminator, and the select pin of two multiplexers for monitoring and collecting the signals of the desired readout channel.

B. Readout Channel Testing

The goal of the qualification test is to verify whether the proposed architecture can amplify the detector signal, confine the noise, and translate it into processable digital data with a reasonable ER.

The analog part of the readout channel, comprising a TIA and two gain stages, would generate a voltage signal for any charge particle absorbed by the detector. As concluded

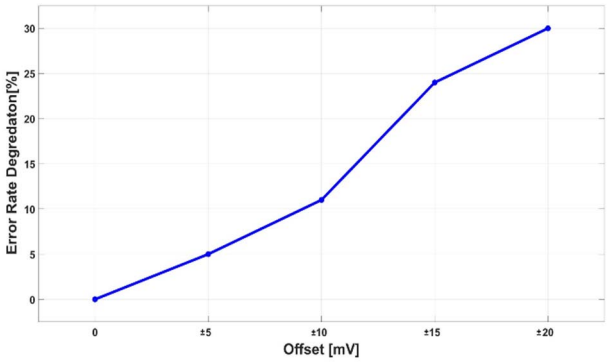

Fig. 5. Simulated ER degradation versus offset seen at the input of the comparator.

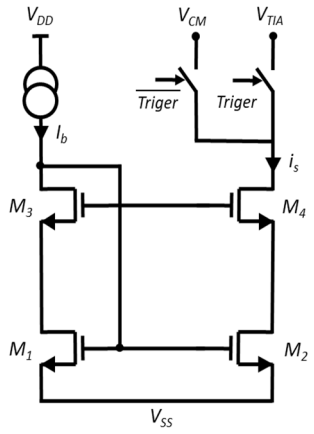

Fig. 6. Schematic of the current DAC.

in [4] and [5] through post-layout simulations, to minimize the detection ER, the TIA feedback resistance must be set to $R_F = 330$ KΩ, which in combination with a $C_F = 12$ fF results in an equivalent noise charge of ENC $= 174\ e^-$[rms] and a bandwidth of 81 MHz. This would correspond to a voltage signal with an average peak level of 340 mV and a noise power of 59.54 mV_{rms} at the end of the analog chain (i.e., after the second gain stage).

The analog voltage signal is then fed to a dynamic comparator that, in every clock cycle, sets the digital output to logical "1" once the voltage signal exceeds the threshold levels. The dynamic comparator makes the detection ER dependent on the comparator offset voltage and the sampling moment. In the case of offset voltage, Fig. 5 illustrates the relation with the detection ER. In the design phase, the transistors of the comparator were sized to limit the offset below 10 mV and, in turn, achieve a maximum detection ER degradation of 1% [4]. In the case of the sampling moment, the sampling clock and peak level of the analog voltage signal should be synchronized to cancel out its contribution to the detection ER. The synchronization process is discussed in detail in Section III.

In this set of experiments and throughout this work, in order to only focus on the operational accuracy of the readout channels, the detector is substituted by a digitally controlled current source (DAC) (see Fig. 6). Modeled as a current generator in parallel with a capacitance (C_D), the DAC must emulate the detector characteristics by generating a sequence of small and fast current pulses.

Here, the challenge is to emulate the signal generated by a physical detector with the DAC. In practice, the current pulse induced by the moving charge inside the detector toward its electrodes appears as a voltage pulse after the preamplifier. The shape of this voltage pulse is a function of the time constant of the preamplifier feedback network [6], [7]. If the time constant is small compared with the duration of the detector charge collection time, the current flowing through the feedback resistor is essentially equal to the instantaneous value of the current flowing into the detector. Thus, the measured voltage pulse has a shape nearly identical to the time dependence of the current produced within the detector plates; therefore, this pulse is called the current pulse. In contrast, if the time constant is larger than the detector charge collection time, the current is integrated into the feedback capacitor. Therefore, the charge stored in the feedback capacitor represents the charge pulse produced by the detector [7]. The integrated charge on the feedback capacitor will finally discharge through the feedback resistor, and the shape of the voltage signal after the preamplifier will become largely independent of the shape of the detector current pulse, leading to a voltage that can be represented as

$$V = \frac{Q}{C_F} e^{\frac{-t}{\tau_F}} \tag{1}$$

where Q is the total charge produced in the detector and $\tau_F = C_F R_F$. In the TIA, the time constant of the feedback network is $\tau_F = 3.9$ ns, which is larger than the detector charge collection time $t_c = 1.8$ ns. In this regard, the posterior case is realized, and the current signal of the detector can be emulated by square wave current pulses with the same equivalent charge. The generation of each current pulse corresponds to the charge generated by the detector during an event.

The concept of the DAC is a current mirror in which one branch is biased by a current source I_b, while the other one connects to a switch network which is controlled by a trigger signal applied by the FPGA through the LVDS interface. Two switches steer the current between the input of the readout channel and an arbitrary node where the current is dumped. In addition, the biasing current I_b is provided by an external current source, allowing calibration of the detector current. In terms of the square wave current pulses that are being generated, the charge of each pulse can be calculated by the following:

$$Q = t_c \times i_s \tag{2}$$

where t_c is the detector charge collection time and i_s is the amplitude of the pulse. Regarding the detector charge collection time of $t_c = 1.8$ ns, to generate a current pulse equivalent to a $160 - \text{aC}$ charge, the amplitude of the pulses is set to $i_s = 90$ nA. Hence, the FPGA must generate a train of trigger pulses with a pulsewidth of 1.8 ns, while the external biasing current source provides a current of $I_b = 90$ nA. Fig. 7 illustrates the simulated channel response to a current

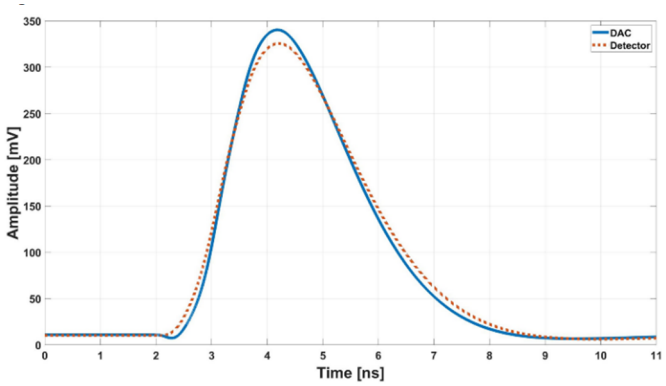

Fig. 7. Simulated channel response to the current signal generated by the DAC (blue solid line) and the detector (orange dashed line).

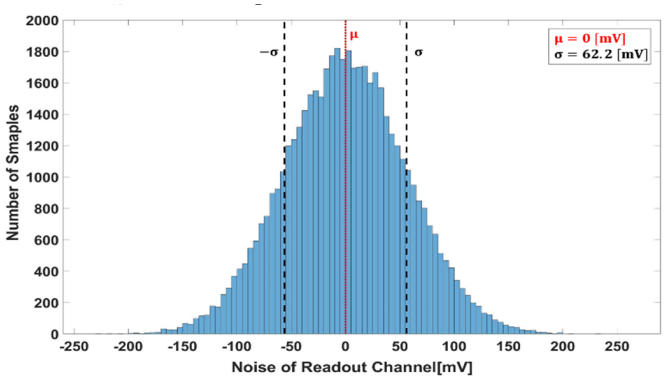

Fig. 8. Histogram of the noise at the end of the analog chain.

signal equivalent to a 160 aC charge generated by the detector and the DAC. The figure shows that the DAC can accurately emulate the detector signal.

III. Data Acquisition Challenges

The functional blocks implemented in the readout channel can degrade the performance of the ROIC if they are not properly calibrated. In this regard, their programmable parameters must be optimized and set based on experimental test results to minimize the ROIC detection ER. In this section, challenges concerning the data acquisition process are recalled.

A. Readout Channel Noise

Regarding the post-layout simulation, the ROIC has an ENC = 174 e^- [rms], which corresponds to noise power of $\sigma_n = 59.54$ mV_{rms} at the output of the analog blocks. The noise of the readout channels in the experimental tests is expected to be larger than the one evaluated by simulations, since the components, devices, and wires used in the test setup inject additional noise into the DUT.

The actual noise of the readout channels can be measured by monitoring the signal at a control pin connected to the output of the analog blocks while the readout channels are silent (i.e., the DAC is not triggered). The noise power can be calculated either by measuring the peak-to-peak fluctuations or drawing a histogram of the signal [7]. Due to the advanced oscilloscope (Keysight MSO9064A 600 MHz) used in this set of experiments, the noise power is measured by drawing a histogram of the voltage signals collected for 30 s to obtain a sufficient number of samples. In addition, to limit the environmental noise, a shielded active probe is used for signal monitoring. Fig. 8 illustrates a histogram of the noise measured at the end of the analog chain. Measurements reveal that the real noise power of the readout channel is $\sigma_{n_{real}} = 62.2$ mV_{rms}, which is equivalent to ENC = 179 e^- [rms].

B. Threshold Levels

The selection and optimization of the threshold levels V_{TH_1} and V_{TH_2} is critical for an effective detection scheme. The optimized threshold levels define the minimum ER in the detection of events. Although formulation exists for optimizing the threshold levels of a comparator for events arriving at fixed times, none exist for the events showing up randomly [8].

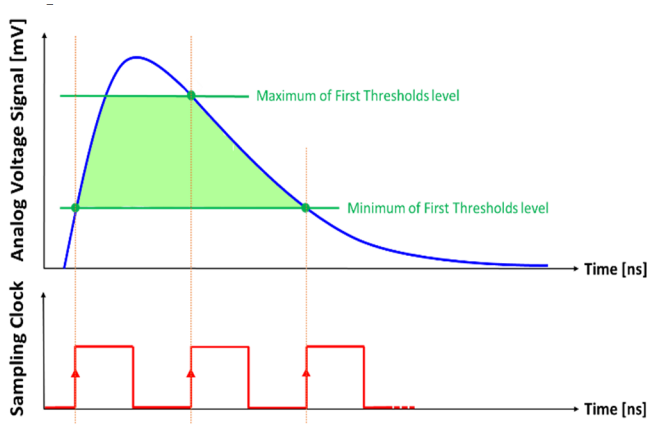

Fig. 9. Authorized region (shown in green) of the first threshold level concerning the sampling clock period.

There are several sources of error to be considered [5], [9], [10]; nevertheless, noise is the most significant contributor for both threshold levels. In some cases, the comparator may sample the voltage signal when it is near the threshold value, whereby noise determines the upper hand in making the decision. In addition, as the implemented comparator is a dynamic one, the shape and time width of the analog voltage signal must also be taken into account [11]. In the case of the first threshold level, to avoid losing the event, V_{TH_1} must be set at a level where the width of the analog voltage signal exceeds one clock cycle. However, the width of the voltage signal must not exceed two sampling clock periods so as not to sample the same event twice. Fig. 9 represents the authorized region of the first threshold level concerning the sampling clock period. The same approach is employed for the second threshold level V_{TH_2}; however, the amplitude of the voltage signal after the pileup must also be taken into account.

In general, for a high threshold level, the events arriving at such compromised times might be missed, giving rise to missed detections (i.e., false negatives). In contrast, if the threshold level is too low, noise can be detected as an event, giving rise to erroneous detections (i.e., false positives) [5].

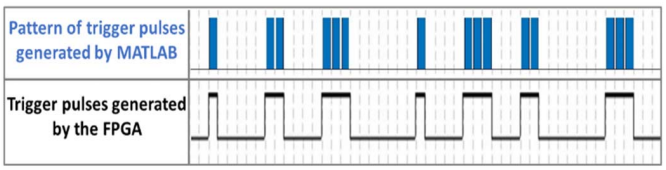

Fig. 10. Pattern of logical "0" and "1" with a Poissonian distribution and the corresponding trigger pulses generated by the FPGA.

By equating the rate of false positives and false negatives, the optimum value of both threshold levels can be selected in the authorized region through experimental tests, as discussed in Section IV.

C. Poissonian-Distributed Trigger Pulses

In the detector, the charge signals are generated randomly, while in the DAC they are generated as a function of trigger pulses provided by the FPGA; thus, the time resolution of the input charge signals is proportional to the frequency of the trigger pulses. The FPGA can generate a train of digital pulses with a maximum frequency of 400 MHz at the pin $\text{Trigger}_{\text{IN}}$ (see Fig. 4), which assigns a time slot of 2.5 ns to every event. In this case, to imitate the random arrival of events, the FPGA must send the trigger pulses at random time slots. In addition, a trimmable delay can be applied to the DAC trigger pulses through chip programming to defer the arrival of the charge signal at each slot; however, this delay is identical for all of the trigger pulses.

The events land on the detector with a Poissonian distribution [9], so trigger pulses must have the same behavior. In this regard, a pattern of logical "0" and "1" with a Poissonian distribution can be generated by MATLAB to be scanned by the FPGA to generate Poissonian-distributed triggers. This also simplifies the experimental tests as we can directly compare the pattern of the DAC trigger signal with the one generated by the comparator to evaluate the ROIC operation. Fig. 10 illustrates the pattern of logical "0" and "1" with a Poissonian distribution and the corresponding trigger pulses generated by the FPGA.

D. Sampling Synchronization

As mentioned above, the DAC can generate current pulses in random time slots rather than distributing them randomly along the time. Moreover, the applied delay is identical to all of the trigger pulses. Therefore, the DAC always generates pulses at a fixed moment during the slot, and an ideal operation is realized.

However, at the same time, the detection ER could be dominated by the sampling contribution. This is because of the fact that the comparator samples the analog voltage signal at points that might be lower than the peak, while the noise of the readout channel is constant. As a consequence, due to a lower sampling SNR, the number of missed detections rises; hence, an increment in the detection ER is observed. For instance, in the case of maximum event rate (one trigger per slot), the DAC generates equally spaced current pulses

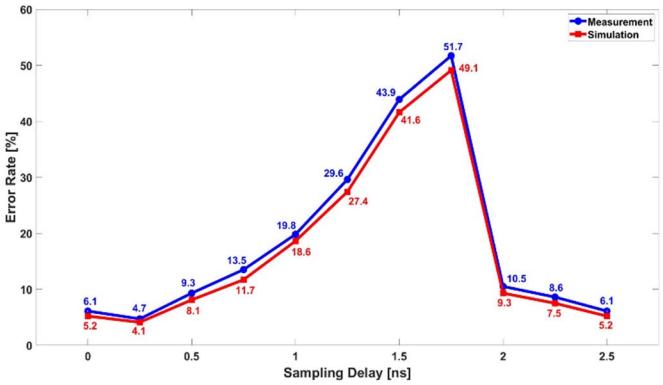

Fig. 11. Simulated (red) and measured (blue) ERs as a function of the sampling delay of the dynamic comparator for single-threshold mode with well-separated trigger pulses.

(every 2.5 ns). If the comparator samples the voltage signal at a point outside the peak, all subsequent pulses will also be sampled at the same point, and therefore, the ER will increase rapidly. Thus, the rising edge of the sampling clock must activate the comparator in a region where the voltage signal exceeds the threshold level or, in the best case, when the voltage signal is at the maximum point. Any lack of synchronicity between these two signals would correspond to a larger ER due to a lower sampling SNR.

Fig. 11 illustrates both simulated and measured ERs as a function of the sampling delay of the dynamic comparator (t_{delay}) for the single-threshold mode. In this experiment, a set of well-separated fixed pattern pulses triggers the DUT once the threshold level is optimized. As shown, sampling the voltage signal after a short t_{delay} leads to a lower ER than simultaneous triggering and sampling; however, a further increment in t_{delay} corresponds to a much larger ER. The delay corresponding to the minimum ER is denoted by the optimum t_{delay}, which is the propagation time of the DAC and the blocks existing in the analog channel.

Such a rise in the detection ER is induced by the dynamic comparator, which makes the ER a function of the arrival time of the events and sampling moment. As a solution to cancel out contribution of sampling moment from the detection ER, the dynamic comparator can be replaced with a continuous one that reacts in the same way for any arrival time of the events; however, the former is the one of interest due to the limited power budget [5], [12], [13].

In this article, to analyze the error associated with the random arrival of the events, the detection ER is measured for several values of t_{delay}, and the overall ER is estimated by averaging the measured values. In addition, in the anticipation of the performance of the continuous comparator in subsequent designs, the focus of this set of measurements is on the optimum t_{delay} that corresponds to the optimal operation.

The minimum ER is reached once the sampling moment of the comparator and the peak of the analog voltage signal are in synch [4]. In other words, when the rising edge of the sampling clock activates the comparator at the maximum point of the voltage signal, sampling occurs at the maximum SNR. Finding

TABLE I
MEASURED CHARACTERISTICS OF THE ANALOG VOLTAGE SIGNAL AS A FUNCTION OF R_F FOR $C_F = 12$ fF

R_F [$K\Omega$]	V_{Peak} [mV]	t_{delay} [ns]	SNR
150	256	0.19	3.82
210	299	0.29	4.67
270	328	0.36	5.11
330	348	0.41	5.6

the optimum t_{delay} which leads to the maximum sampling SNR requires several practical steps. The calibration and test features implemented on the chip can speed up this process. Since the output of the analog channel is accessed through an internal buffer (see Fig. 4), the optimum t_{delay} can be measured on an oscilloscope by subtracting the moments of time when the voltage signal reaches the peak level and the DAC trigger signal rise.

In the optimum t_{delay}, the DAC contribution is always constant, while the contribution of the analog channel mainly depends on the TIA feedback resistance R_F and the gain bandwidth (GBW) of the TIA core amplifier. Table I summarizes the measured peak voltage, the corresponding t_{delay}, and the SNR of the analog signal for several programmable values of the TIA feedback resistance R_F and minimum feedback capacitance $C_F = 12$ fF. As far as the results presented in Table I, the optimum t_{delay}, V_{Peak}, and SNR rise by increasing the feedback resistance R_F. In this regard, there is a particular optimum t_{delay} for any TIA feedback resistance that leads to sampling with the maximum SNR. Thanks to the trimmable delay that can be applied to the DAC current pulses through chip programming, the comparator sampling moment can be easily synced to the peak point of the analog voltage signal.

Regarding the analysis performed in [4], the feedback resistance is set to $R_F = 330$ KΩ, which results in an optimum $t_{\text{delay}} = 0.4$ ns. This optimum t_{delay} corresponds to a rise in the sampling clock once the voltage signal is at the maximum point, i.e., sampling with the maximum SNR; nonetheless, in the real application, this synchronization is not possible due to the random arrival of events. The detailed measurement results for the optimum t_{delay} and estimation of the overall ER for events with random arrival times are presented in the next section.

IV. EXPERIMENTAL RESULTS

The goal of the following sets of experimental tests is to verify the measurement test setup, evaluate the data acquisition process, optimize the threshold levels V_{TH_1} and V_{TH_2}, and calculate the detection ER in both single and double-threshold modes. For these purposes, the FPGA must trigger the readout channel by a pattern of logical "0" and "1" that precedes the 400-MHz sampling clock with a $t_{\text{delay}} = 0.4$ ns, collect the data generated by the chip, compare the pattern of trigger pulses and chip data, and calculate the detection ER.

Comparing the pattern of trigger pulses and chip data, the FPGA calculates the number of true, erroneous, and missed

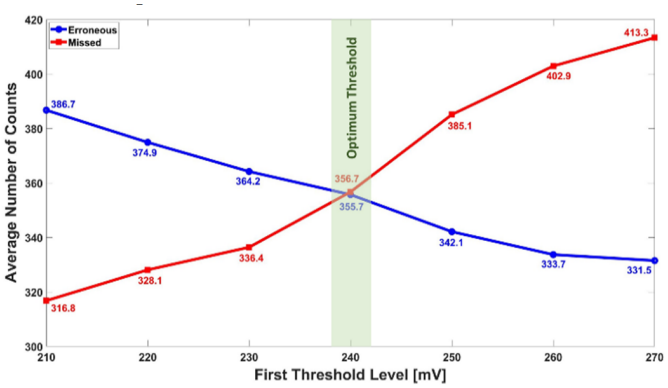

Fig. 12. Average number of erroneous (blue) and missed (red) counts as a function of the first threshold level.

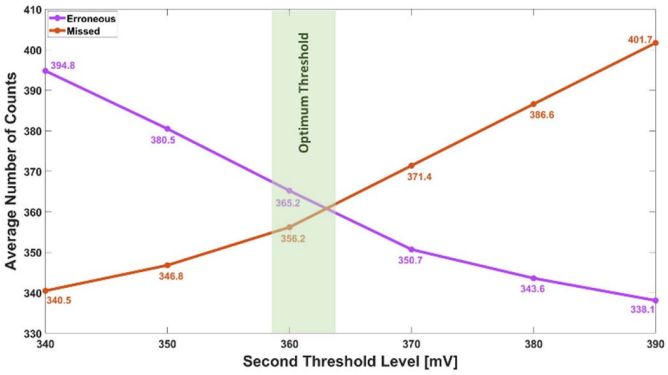

Fig. 13. Average number of erroneous (purple) and missed (orange) counts as a function of the second threshold level.

counts. The true counts correspond to the number of bits at which the pattern of the trigger pulses and chip data matches. In some cases, due to the noise of the readout channel, the comparator might generate another logical "1" in the following bits, referred to as erroneous counts, while the missed counts stand for the events missed by the comparator. In addition, the subtraction of erroneous and missed counts is referred to as false counts. The number of false counts is interesting when the number of events is counted for a specific time period without the need to record the exact time of their occurrence. In this case, the number of missed events is compensated by the number of erroneously counted events. In each experiment, the ER is calculated as the ratio of false counts to the total number of trigger pulses.

In this work, the optimized threshold corresponds to the level (in the authorized region) at which the number of erroneous and missed counts is equal. In this regard, they must be recorded, while the readout channel is triggered with a fixed pattern of trigger pulses. In the case of the first threshold level V_{TH_1}, the DUT is programed in single-threshold mode and triggered by 5000 well-separated pulses (event rate of 4 MHz) to avoid any possibility of a pileup. For the second threshold level V_{TH_2}, the DUT is programed in double-threshold mode and triggered 5000 times by two consecutive pulses with a frequency of 4 MHz. In addition, it is worth mentioning

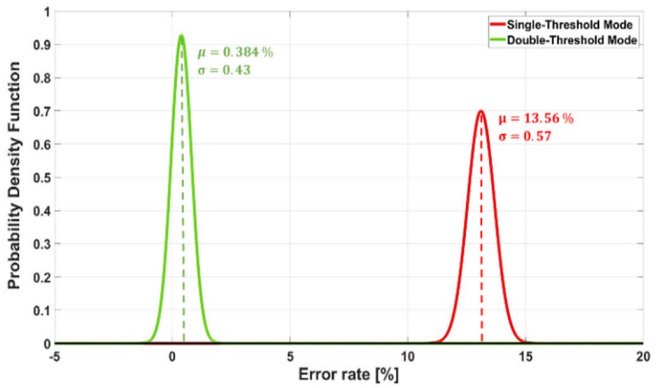

Fig. 14. Distribution of the detection ER for single-threshold mode (red) and double-threshold mode (green).

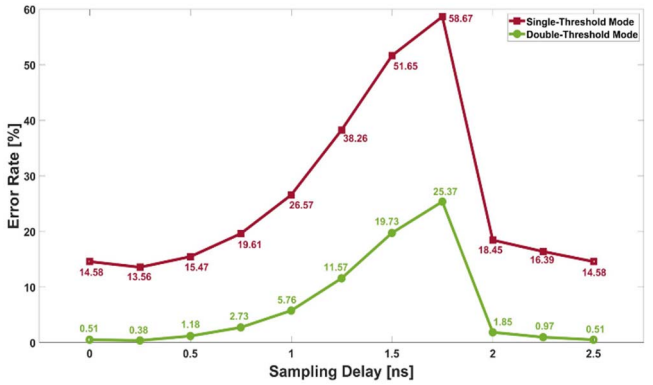

Fig. 15. Detection ER as a function of the sampling delay of the dynamic comparator for single-threshold mode (red) and double-threshold mode (green).

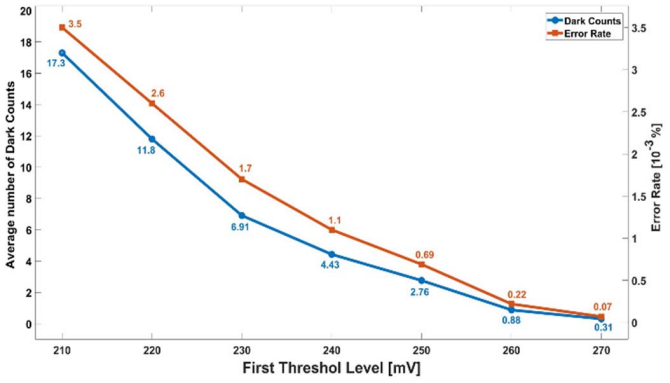

Fig. 16. Average number of dark counts (blue) and corresponding ERs (orange) as a function of the first threshold level.

that the experimental tests are repeated 100 times to estimate the variability of the results, increase the accuracy of the optimization, and generate consistent results.

Figs. 12 and 13 represent the average number of erroneous and missed counts as a function of the first and second threshold levels for the optimum t_{delay}, respectively. Regarding the results presented in the figures, the optimum values of the threshold levels are $V_{\text{TH}_1} = 240$ mV and $V_{\text{TH}_2} = 360$ mV as the average number of erroneous and missed counts are almost equal at these levels.

Once the optimized threshold levels are determined, the qualification tests can commence the performance assessment of the proposed architecture by estimating the detection ER. The readout channel is triggered by 5000 Poissonian-distributed trigger pules, and the experimental tests are repeated 100 times. Fig. 14 plots the distribution of the detection ER for both single and double-threshold modes at the optimum t_{delay}; on average, the ERs are 13.56% with $\sigma_{\text{Single}} = 0.57\%$ and 0.384% with $\sigma_{\text{Double}} = 0.43$, respectively. Therefore, the readout achieves a maximum ER of 15.27% in single-threshold mode, and 1.674% in double-threshold mode with the optimum t_{delay}.

The detection ERs represented so far correspond to the sampling of the voltage signal at the peak point, which indicates the optimal operation; however, in the real application, this condition is not feasible due to the random arrival of the events. To determine the performance of the DUT for events with random arrival times, the measurements can be repeated for other values of t_{delay} by optimizing the threshold levels and estimating the ER for each case. Then, the overall ER can be approximated as the average of all measured ERs. Fig. 15 presents the detection ER as a function of the sampling delay of the dynamic comparator for both single- and double-threshold modes. According to the measurement data, it can be concluded that, for Poissonian-distributed events with random arrival times, the DUT has an average ER of 26.16% in single-threshold mode and 6.41% in double-threshold mode.

In addition to event registration, the readout channels must remain silent once there is no charge generated by the detector. To test this aspect of operation, chip data are recorded for a certain amount of time, while the readout channel is not triggered. In this case, the pulses generated by the comparator, called dark counts, are recognized as an error. The test is repeated 100 times, as illustrated in Fig. 16, where the average number of dark counts and corresponding ER is a function of the first threshold level for a measurement time equivalent to 5000 slots. The order of the ERs for the dark counts is 10^{-3}%, which is rather small and negligible. In this regard, the designed readout interface can register the events hitting the detector surface at a quite negligible intrinsic ER.

TABLE II

AVERAGE NUMBER OF DARK COUNTS AND THE CORRESPONDING ER FOR DIFFERENT VALUES OF THE FIRST THRESHOLD LEVEL

V_{TH_1} $[mV]$	Dark Counts	ER $[10^{-3}\%]$
210	17.31	3.5
220	11.84	2.9
230	6.91	1.7
240	4.43	1.1
250	2.76	0.69
260	0.88	0.22
270	0.31	0.07

Table II summarizes the average number of dark counts and the corresponding ER for different values of the first threshold

level. The number of dark counts rises for smaller values of the first threshold level; however, in all cases, they are negligible, as their corresponding ERs are quite small.

V. Conclusion

The double-threshold technique is proposed as a solution to the conflicting requirements of a small input signal, large bandwidth, and low power capability of ROICs. The designed ROIC requires a qualified test setup with convincing and cogent properties for evaluating the ROIC characteristics. In this set of experiments, the data acquisition process is adequately characterized in terms of noise, sampling moments, and data collection to address a worthy and qualified experimental setup with optimized threshold levels.

The measured noise power of the readout channel is $\sigma_{n_{\text{real}}} = 62.2\ \text{mV}_{\text{rms}}$, which is equivalent to ENC $= 179\text{e}^-$ [rms]. The DUT operates in the most optimum way with threshold levels of $V_{\text{TH}_1} = 240$ mV and $V_{\text{TH}_2} = 360$ mV, and when the sampling clock is fed to the comparator with a time delay of $t_{\text{delay}} = 0.4$ ns in terms of the DAC trigger pulses. This setup corresponds to a maximum ER of 15.27% in single-threshold mode, and 1.674% in double-threshold mode for Poissonian-distributed trigger pulses. In terms of the randomness of arrival times of the Poissonian-distributed charge portions, at a maximum rate of 4×10^8 events/s, the average ER of the DUT is estimated to be 26.16% in single-threshold mode and 6.41% in double-threshold mode. In addition, at the selected threshold levels, the intrinsic false counts of the ROIC are negligible.

Finally, due to the challenges associated with generating current pulses in the DAC, the noise of the input charge is not considered in this set of experiments. Instead, it will be studied in an upgraded test environment where the DAC is substituted by a decent network that generates current pulses with tunable amplitude and random arrival times to imitate the actual detector precisely.

References

[1] R. Kleczek, P. Grybos, R. Szczygiel, and P. Maj, "Single photon-counting pixel readout chip operating up to 1.2 Gcps/mm^2 for digital X-ray imaging systems," *IEEE J. Solid-State Circuits*, vol. 53, no. 9, pp. 2651–2662, Sep. 2018, doi: 10.1109/JSSC.2018.2851234.

[2] M. Ciobanu *et al.*, "PADI, an ultrafast preamplifier–discriminator ASIC for time-of-flight measurements," *IEEE Trans. Nucl. Sci.*, vol. 61, no. 2, pp. 1015–1023, Apr. 2014, doi: 10.1109/TNS.2014.2305999.

[3] A. Sakic *et al.*, "High-efficiency silicon photodiode detector for sub-keV electron microscopy," *IEEE Trans. Electron Devices*, vol. 59, no. 10, pp. 2707–2714, Oct. 2012, doi: 10.1109/TED.2012.2207960.

[4] M. A. Disi, A. M. Zaki, Q. Fan, and S. Nihtianov, "High-count rate, low power and low noise single electron readout ASIC in 65 nm CMOS technology," in *Proc. 30th Int. Sci. Conf. Electron. (ET)*, Sep. 2021, pp. 1–5, doi: 10.1109/ET52713.2021.9580005.

[5] M. A. Disi, "Single electron readout circuit: SERCuit," M.S. thesis, Dept. Microelectron., TU Delft, Delft, The Netherlands, 2020.

[6] P. Grybos, P. Maj, and R. Szczygiel, "Comparison of two pole-zero cancellation circuits for fast charge sensitive amplifier in CMOS technology," in *Proc. 14th Int. Conf. Mixed Design Integr. Circuits Syst.*, Jun. 2007, pp. 243–246, doi: 10.1109/MIXDES.2007.4286158.

[7] M. Nakhostin, "Pulses from ionization detectors," in *Signal Processing for Radiation Detectors*. Hoboken, NJ, USA: Wiley, 2017, pp. 1–75.

[8] M. J. M. Pelgrom, "Sample and hold," in *Analog-to-Digital Conversion*, 3rd ed. New York, NY, USA: Springer, 2013, pp. 57–86.

[9] H. Spieler, "Signal processing," in *Semiconductor Detector Systems*. Oxford, U.K.: Oxford Univ. Press, 2005, pp. 134–189.

[10] E. Säckinger, "Advanced transimpedance amplifier design," in *Analysis and Design of Transimpedance Amplifiers for Optical Receivers*. Hoboken, NJ, USA: Wiley, 2018, pp. 343–372.

[11] S. D'Amico, G. Cocciolo, A. Spagnolo, M. De Matteis, and A. Baschirotto, "A 7.65-mW 5-bit 90-nm 1-Gs/s folded interpolated ADC without calibration," *IEEE Trans. Instrum. Meas.*, vol. 63, no. 2, pp. 295–303, Feb. 2014, doi: 10.1109/TIM.2013.2278998.

[12] L. Ratti, M. Manghisoni, V. Re, and G. Traversi, "Discriminators in 65 nm CMOS process for high granularity, high time resolution pixel detectors," in *Proc. IEEE Nucl. Sci. Symp. Med. Imag. Conf. (NSS/MIC)*, Nov. 2013, pp. 1–6, doi: 10.1109/NSSMIC.2013.6829777.

[13] R. Sangeetha, A. Vidhyashri, M. Reena, R. B. Sudharshan, S. Govindan, and J. Ajayan, "An overview of dynamic CMOS comparators," in *Proc. 5th Int. Conf. Adv. Comput. Commun. Syst. (ICACCS)*, Mar. 2019, pp. 1001–1004, doi: 10.1109/ICACCS.2019.8728470.

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