MSc thesis in Electrical Engineering

High-Dynamic-Range, Low-Power Digital-Input Direct-PWM Class-D Amplifier

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Abstract

Class-D amplifiers are quickly becoming the standard in many audio applications. Their highly efficient behavior and wide power range make these amplifiers more suitable than traditional Class A/AB audio amplifiers. Battery-powered devices are a particularly interesting sub-field due to their special demand for extended battery duration and higher efficiency. An output power lower than 2 W, along with good performances in terms of linearity and efficiency, is often required. Many stand-alone Class-D Amplifiers (CDA) have analog inputs, making them susceptible to interference that negatively impacts their behavior. This problem can be mitigated by employing an insensitive input digital interface. Many standard solutions often require complex architectures, which limit these systems' reliability. This work proposes a digital-input class-D amplifier with a multi-level output stage that, together with a relatively low (480 kHz) switching frequency, reduces idle power consumption while achieving good linearity. Based on a 180 nm BCD technology, it can drive a 16-Ω load showing pre-layout simulated performances: -111.3 dB THD+N, 115.6 DR, 91.4% peak efficiency, and 2.14 mW idle power consumption.

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1 Introduction

Class-D amplifiers are quickly becoming the standard in many audio applications.

Their highly efficient behavior and wide power range make this particular class of amplifiers optimal for use in smartphones, cars, and portable speakers, as well as television sets and theater systems. Mobile applications are particularly interesting due to the stringent demand for extended batteries, requiring high-efficiency amplifiers. Such applications often require an output power lower than 2 W and good performances in terms of linearity and efficiency [2].

Figure 1.1 shows the comparison between the efficiency for standard classes of audio amplifiers versus their normalized output power. Thanks to a switching output stage controlled by a pulse width modulated (PWM) signal, the output transistors are alternately turned on and off, switching the output voltage between the supply lines. Class D amplifiers are much more efficient than standard classes of amplifiers, in which the output transistors operate in the saturation region, requiring a constant bias current through them. Class-D amplifiers usually achieve more than 90% efficiency [1].

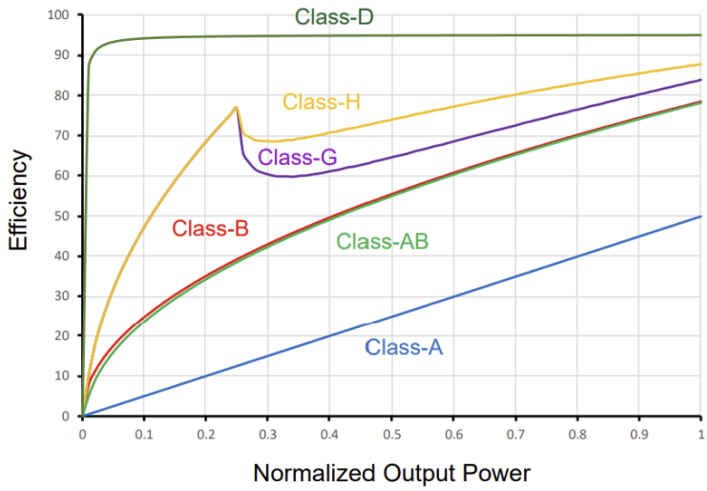

Figure 1.1: Efficiency of standard classes of audio amplifiers.

The switching behavior of class-D amplifiers makes their output a train pulse whose average is equal to the input signal [7]. The average of the output signal is usually obtained by employing a non-resistive low-pass filter to filter out the high-frequency content of the output node.

1.1 Class-D Amplifier Operation

Figure 1.2 shows a simplified analog input class-D amplifier connected in the common Bridge-Tied-Load (BTL) configuration [11].

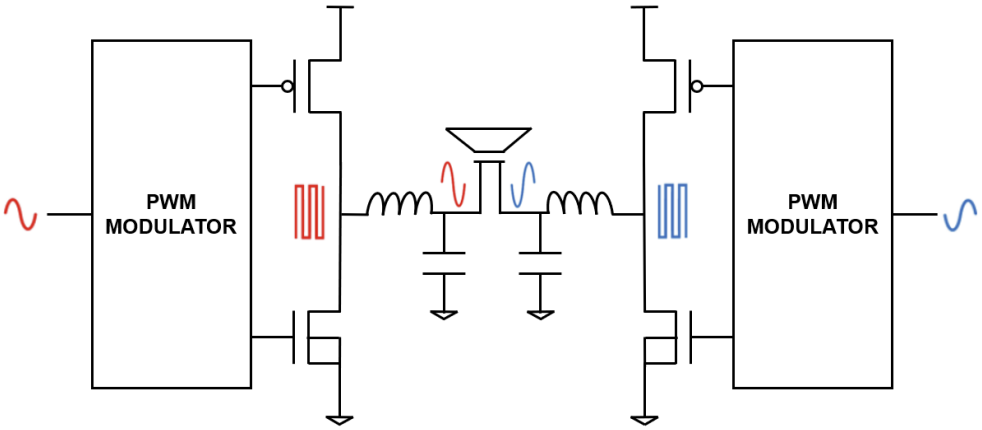

Figure 1.2: Simplified Class-D Amplifier.

In this configuration, one amplifier drives one side of a load, and another amplifier, with an inverted signal from the first amplifier, drives the other side of the load. This increases the swing and the power delivered to a load compared to a single-ended architecture.

Commonly, class-D amplifiers employ some PWM scheme, which in the analog domain can be easily generated by comparing the signal to a triangle wave reference. For the configuration above, typically, AD-PWM and BD-PWM can be used. AD-PWM generates two complementary output pulse trains, while the BD-PWM outputs are not the inverse of each other [11].

The BD scheme applied to the configuration shown above has a significant common-mode content in its output, but with respect to the AD-PWM scheme, it does not show odd Inter-Modulation (IM) distortion between the input signal and the carrier frequency [19]. The output stage of a class-D amplifier usually limits its linearity performances [1][2][3][8].

Class-D amplifiers are usually driven in closed-loop configurations to compensate for their non-ideal switching behavior, which strongly degrades their linearity, noise, and Power-Supply-Rejection-Ratio (PSRR) [1]. Regular closed-loop CDAs generally sense the power stage output and feed it back to compare with the audio input. Similar to the amplifier in Figure 1.2, many stand-alone Class-D Amplifiers (CDAs) have analog inputs, making them susceptible to interference that negatively impacts their behavior [16]. This problem can be solved by employing an insensitive digital interface.

1.2 Digital Input Class-D Amplifiers

Digital input CDAs have several advantages over their analog counterpart. Digital inputs adapt directly to modern digital driver interfaces and peripherals such as wireless headphones and speakers. Furthermore, digital inputs are insensible to external interference [2].

To make an efficient comparison between the digital input and the analog output, digital input CDAs need different architectures. In general, a data conversion around the signal chain has to be performed. Depending on the position of the main Digital-to-Analog Converter (DAC) around the partially or fully analog loop filter in the CDA, two architectures can be distinguished in the literature, shown in Figure 1.3 [5].

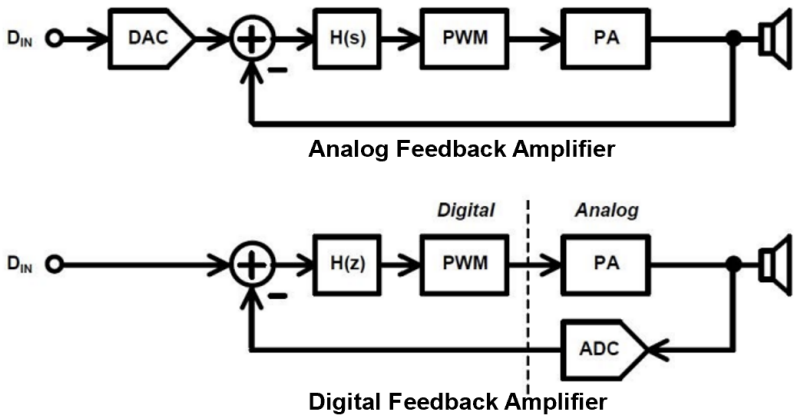

Figure 1.3: Block diagrams of general digital-input Class-D amplifiers [5].

The top figure shows a standard analog CDA controlled by an open-loop DAC in front of the loop filter. This architecture has the fundamental advantage of being less complex than the others. On the other hand, the input DAC quality limits the performances of the whole amplifier, becoming the bottleneck of the architecture [13][8][3].

The bottom figure shows a Digital Feedback Amplifier in which a hybrid digital loop replaces the traditionally fully analog loop filter with an ADC in the feedback path. This digital architecture is more reliable than a fully-analog one but also of increasing complexity. Furthermore, the feedback ADC needs to be fast enough to maintain the stability of the loop and still employ an accurate DAC in its internal feedback path [21][9][6].

Digital input class-D amplifiers based on a fully analog loop filter can be further classified into two categories based on the selection of the DAC architecture, as it is shown by the schematized CDA architectures of Figure 1.4.

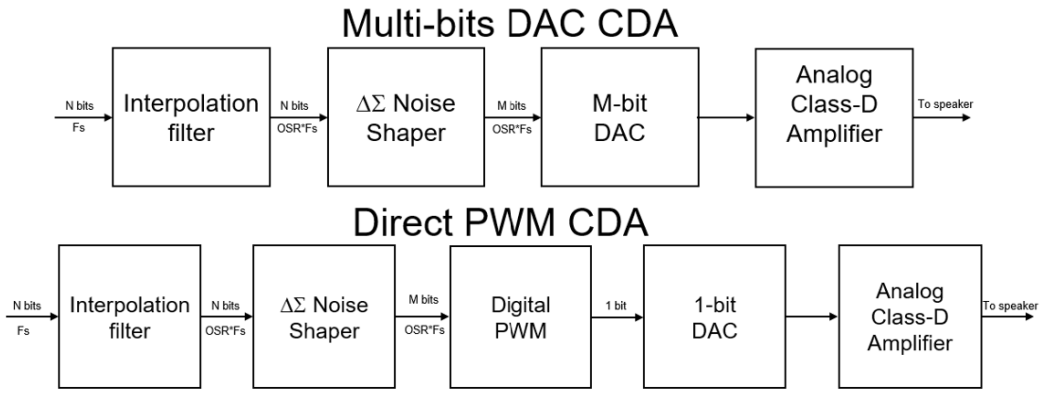

Figure 1.4: Multi-bits and Direct PWM class-D amplifiers [2][17].

The top figure employs a multi-bit oversampled DAC, while the bottom figure shows the direct PWM architecture. In this topology, the PWM is generated in the digital domain, and a single-bit DAC can be used to drive the analog loop filter. Lower bits DACs are intrinsically more linear and employ simpler architectures than Multi-bits. However, they are also much more sensitive to jitter, which causes a degradation of the class-D amplifier performances.

In this thesis work, a digital input class-D amplifier is proposed, based on the work of [23][12] and achieving similar to low-power CDAs state-of-the-art performances [17] while employing a less complex, more robust architecture.

The direct digital PWM architecture is chosen to be at the core of the proposed system. Several techniques are applied to the design of the DAC, which would otherwise limit the performance of the whole amplifier.

1.3 Thesis Objectives

Among the recently published Class-D Amplifiers targeting diverse output power ranges, this thesis focuses on the design of a digital-input CDA for low-power mobile audio applications[1].

Table 1.5 [17] list the performances of several class-D amplifiers published in the literature.

	Matamura ISSCC'21	Gaalaas ISSCC'05	Karmakar ISSCC'20	Dooper JSSC'12	Chien ISSCC'20	Cope ISSCC'18	Zhang JSSC'21
Process [nm]	40	600	180	140	500	180	180
Supply [V]	1.8	12	14.4	5	5	20	14.4
Load [Ω]	16	6	4	4	8	4	8
Max. Pout [W], @THD+N 1%	0.086	7*	24*	2.7	1.42	>20	>10
Max. Pout [W], @THD+N 10%	0.105	10	28	3.4	–	–	–
Minimum THD+N [%]	0.0022	0.0032*	0.00078	0.015	0.0009	0.0013	0.0004
SNR/DR [dB]*** (A-weighted)	113/113	102*/103	110*/109	103/103	106/-	116/116	109.7/111.2
PSRR @ 217Hz [dB]	94	65	–	85	99	<80	-
Efficiency η [%]	93	88	91	90	92	90	91
fsw [kHz]	175**	450*	2000	384	168	400	4200
Loop Filter's Order	5th	7th	3rd	2nd	2nd	5th	3
Modulation Scheme	ΔΣ (Digital in.)	ΔΣ (Analog in.)	ΔΣ-PWM (Analog in.)	PWM (Digital in.)	PWM (Analog in.)	PWM (Digital in.)	PWM (Analog in.)

Figure 1.5: Class-D amplifiers comparison [17][10][12][4][8][5][23].

Dynamic Range (DR) performances higher than 113 dB [17] were achieved for low-power audio applications CDAs. On the other hand, peak Total-Harmonic-Distortion+Noise (THD+N) performances as low as 0.0004 % (-107.8 dB) were achieved for relatively high-power CDAs (14 W) [23].

Low-power, digital-input Class-D amplifier [17] achieving -93.15 dB peak Total-Harmonic-Distortion+Noise (THD+N), 113 dB Dynamic Range (DR), 1.23 mW idle power consumption while driving a 16 Ω load is considered the design benchmark for this thesis work as it represents the closest to our application of interest.

This thesis aims to achieve similar or better than state-of-the-art digital-input low=power class-D amplifiers performances in terms of DR and THD+N while maintaining an as-low-as-possible complexity and low idle power consumption.

The table below shows the target specifications of this work.

Specification	Target
THD+N	< -110 dB
DR	> 115 dB
Maximum Efficiency	> 90%
Idle Power Consumption	As low as possible

Figure 1.6: Targeted specifications for the proposed class-D amplifier.

[1] Maximum output power equal to 82 mW, while loaded by a 16 Ω load.

1.4 Thesis Organization

This thesis is structured as follows.

Section 1 introduces the thesis work and presents the thesis objectives. Section 2 briefly describes the main CDA architectures found in the literature, introducing the Direct Digital PWM CDA at the center of the proposed architecture. It further explains the high-level design of the proposed system. Section 3 deals with implementing the high-level system architecture and explains the design methodologies and techniques employed to keep low power consumption. Finally, Section 4 presents the final performances achieved by this thesis work and proposes possible future works.

2 Architecture Overview

This chapter introduces the high-level design of the proposed digital-input CDA architecture. The system is explained step by step, from the direct Digital PWM topology to the final proposed architecture.

2.1 Direct Digital PWM Amplifiers

The high-level architecture of the employed Direct Digital PWM Amplifier (DDPA) is shown in Figure 2.1. The main idea behind this architecture is to use a regular closed-loop CDA at the end of the signal chain driven by a simple 1.5-bit DAC. The digital audio input is directly converted to a digital pulse width modulated signal in an open-loop fashion. This D-PWM code is then directly fed to a 1.5-bit digital-to-analog converter, which drives a regular analog CDA [13].

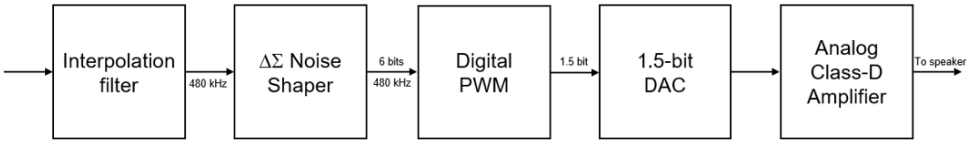

Figure 2.1: Direct Digital PWM Amplifier architecture.

The generation of the PWM signal driving the CDA is performed in the digital domain. In an analog PWM, the so-called natural sampling process generates a PWM signal by comparing an incoming analog signal to an analog triangular reference, as shown in Figure 2.2.

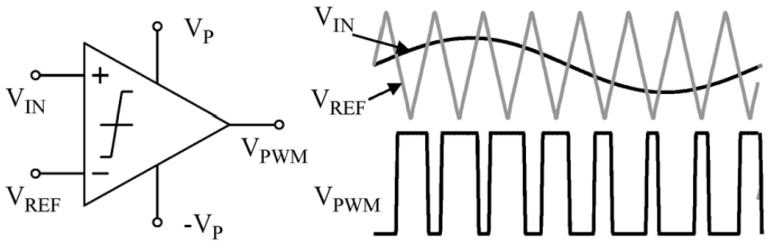

Figure 2.2: Natural sampling PWM generation [2].

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Although the generation of a natural PWM signal involves a highly non-linear comparator, the ideal frequency spectrum of this process only contains intermodulation (IM) products of the carrier and the input signal without having any harmonic of the input signal, as shown in Figure 2.3. Once the IM products are filtered out, the ideal spectrum looks distortion-less.

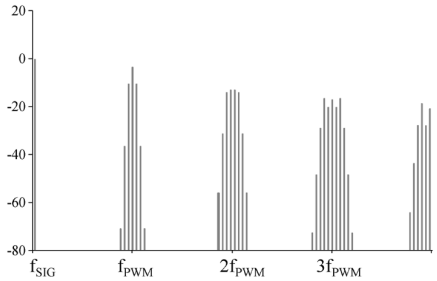

Figure 2.3: Natural sampling process: Frequency spectrum [2].

To understand the effect of a digital PWM modulation process in terms of linearity, we can separately consider the role of quantization and sampling of the digital triangular reference one at a time.

Figure 2.4 shows the effect of the quantized triangular reference in the spectrum. As it is shown, quantization results in additive white noise. Figure 2.5 shows the impact of the sampled triangular reference in the spectrum, which on the other hand, results in additional tones and, therefore, distortion.

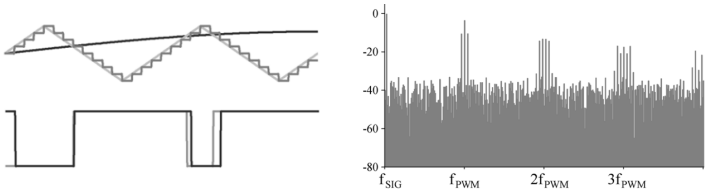

Figure 2.4: Noise caused by quantization in a D-PWM process [2].

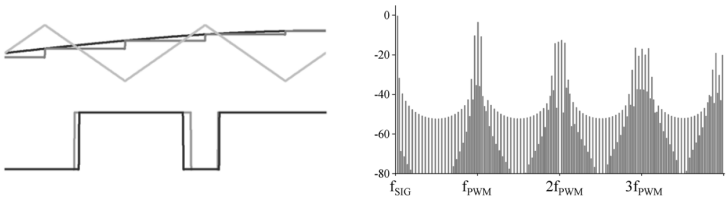

Figure 2.5: Distortion caused by sampling in a D-PWM process [2].

A digital PWM process is intrinsically prone to cause non-linearities. Furthermore, to reach a good Signal-to-Noise Ratio (SNR), the number of quantization levels needs to be relatively high (N $\geq$ 14 bit for SNR = 100 dB [19]), which leads to an unpractical high required sampling frequency.

If we consider an audio bandwidth up to 40 kHz, with a 14-bit resolution, the carrier frequency would need to be:

$$F_{SW} \geq 2 \cdot F_{IN} \cdot 2^N \simeq 2.85\ GHz \tag{2.1}$$

which is clearly unfeasible in standard CMOS processes.

Therefore, three different issues must be mitigated in the digital PWM process.

The distortion introduced by the sampling process can be reduced if the sampling frequency becomes so high to approximate a natural PWM. The white noise introduced by the quantization process can be shaped and filtered using a Delta-Sigma converter. Finally, to decrease the required sampling frequency, the number of bits of resolutions can be reduced by employing a digital truncator.

The blocks in front of the D-PWM shown in Figure 2.1 have the effect of compensating for the digital PWM process. The Interpolation filter up-samples the digital input signal approximating a natural sampling. A delta-sigma is then used to decrease the number of resolution bits and shape the quantization noise out of the audio bandwidth. Any SNDR and THD can therefore be obtained at the expense of a higher clock frequency [2].

Direct D-PWM amplifiers are therefore chosen as the core architecture of the proposed digital-input CDA. Their main advantage is their relatively low complexity in implementing a 1-bit DAC and the possibility to reuse standard analog Class-D amplifier loops. On the other hand, due to noise shaping, a large amount of out-of-band noise risks being pushed back into the audio bandwidth due to clock jitter. Therefore, a precise clock is needed to achieve high performance, as discussed in Section 2.3.2.

2.2 Multilevel Delta-Sigma Modulator

A multi-level, fully digital DSM achieves the noise shaping function needed to shape the noise introduced by the quantization process out of the audio bandwidth and increase the SQNR available for the blocks following in the signal chain. Figure 2.6 shows the error-feedback structure employed for the DSM. Rather than feeding back the MSB from the output as done traditionally in analog delta-sigma loops, here, the truncation error (represented by the discarded LSBs) is filtered and fed back to the input. The loop filter H_e is located in the feedback path and employs fully digital components.

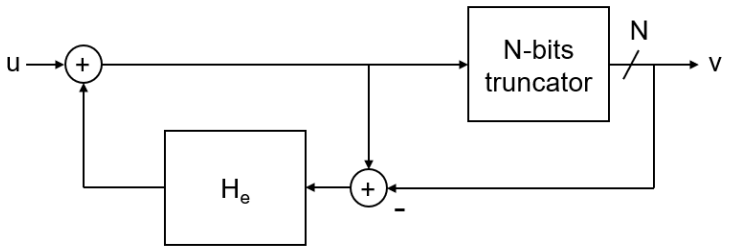

Figure 2.6: Delta-Sigma Error-feedback structure [20].

From a quick linear analysis, it is possible to obtain the output signal function of the input in the discrete z-domain:

$$V(z) = U(z) + [1 - H_e(z)]E(z) \tag{2.2}$$

Showing, therefore, a Signal Transfer Function (STF) equal to 1 and a Noise Transfer Function (NTF) equal to $[1 - H_e(z)]$. The NTF is designed to maintain enough SQNR for additional signal conditioning after the Delta-Sigma Modulator. A 63-levels, 6th-order DSM with an oversampling ratio of 12 and an out-of-band gain of 6 dB was finally chosen to achieve a maximum SQNR for a maximum stable input amplitude of 0.9 FS, equal to around 145 dB. The resulting NTF is shown below:

$$NTF(z) = \frac{-3.34z^5 + 11.42z^4 - 17.1z^3 + 13.61z^2 - 5.66z + 0.97}{z^6 - 2.57z^5 + 3.21z^4 - 2.34z^3 + 1.02z^2 - 0.25z + 0.03} \tag{2.3}$$

A high-order NTF with a relatively low oversampling ratio of 12 enables a low switching activity, reducing power consumption. For bandwidth in the audio range up to 20 kHz, the DSM switching frequency is equal to 480 kHz. The number of levels of the DSM is then designed based on the requirement for the peak SQNR.

2.3 Digital Pulse-Width-Modulator

The DSM output is directly transformed into a pulse-width modulated digital signal ready to be converted into the analog domain via a subsequent DAC and finally injected into the analog loop filter of the class-D amplifier, as shown in Figure 2.7. The relationship between the clock driving the D-PWM block and the DSM frequency is fixed by the number of levels of the DSM output, considering that every level corresponds univocally to a different duty cycle.

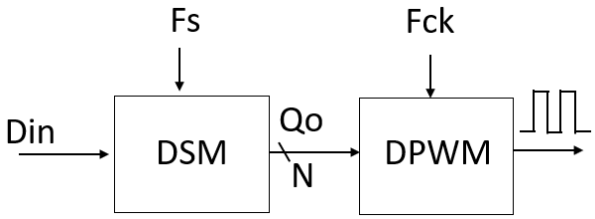

Figure 2.7: Fck-Fs DSM D-PWM relationship.

In general:

$$\frac{F_{ck}}{F_s} = n - 1 \quad for\ n = log_2 N \tag{2.4}$$

As discussed, the limited sampling frequency results in distortion, as the spectrum showing the output of a sample D-PWM block in Figure 2.8 demonstrates. Both even and odd-order harmonics appear in the spectrum, posing a fundamental SQNR limitation in the audio bandwidth. Even harmonics can be filtered out by applying a differential BD D-PWM scheme.

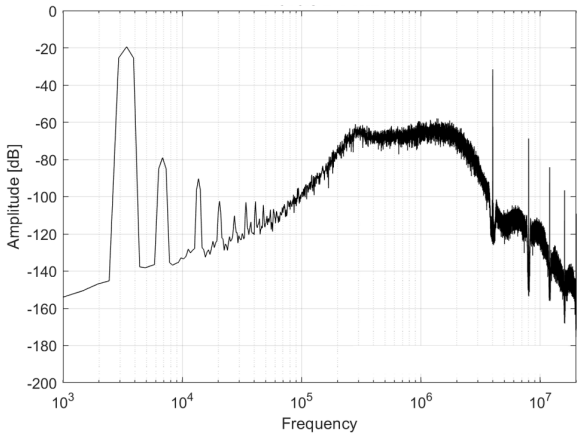

Figure 2.8: D-PWM Spectrum with harmonic distortion.

Figure 2.9 shows the spectrum at the output of a fully differential BD D-PWM block, the odd harmonic distortion introduced by the digital process is not filtered out and now dominates the linearity performances as the input amplitude increases, posing a fundamental limitation toward the achievement of a good peak SQNR.

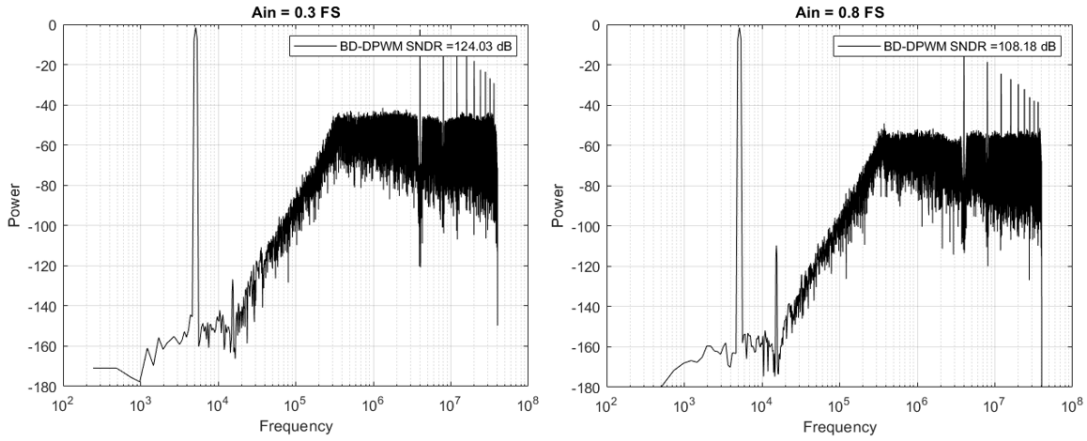

Figure 2.9: D-PWM distortion as the digital input amplitude increases.

2.3.1 Pre-Distortion Digital Filter

Since the principle of operation of the D-PWM is known, its intrinsic non-linearity can be removed entirely by applying to its transfer function the reciprocal of its error term. A specific pre-distortion digital filter can therefore be applied at the signal chain's input to compensate for the non-linearity introduced by the subsequent D-PWM operation. The following transfer function of the digital filter can be obtained $D_{out} = D_{in}(1 + f)$, where:

$$f = -\frac{1.5 \cdot S_{in}^2}{S_{ref}^2 - S_{in}^2} \tag{2.5}$$

Where S_{in} is the slope of the digital input and S_{ref}, is the slope of the reference PWM triangle wave.

Furthermore, by taking the Taylor expansion of the expression above, it is possible to arrive at a simplified equation that results in a less complex digital implementation:

$$f* = -1.5 \cdot \left(\frac{S_{in}}{S_{ref}}\right)^2 \tag{2.6}$$

Figure 2.10 shows the simulated spectrum at the output of the D-PWM block after the pre-distortion filter is applied at the input of the digital signal chain for input amplitudes of -80 dB FS and 0.8 FS. Maximum theoretical Dynamic range (DR) of 133.72 dB and peak Signal-to-quantization-noise ratio (SQNR) of 122.74 dB were simulated.

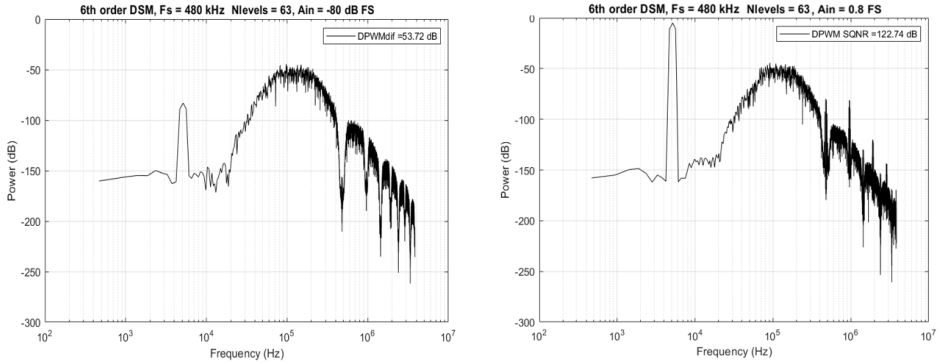

Figure 2.10: Simulated FFT at the output of the D-PWM block for -80 dB an 0.8 FS.

2.3.2 Jitter in Digital-input Class-D Amplifiers

A timing error due to the random deviations of the edges of the sampling clock with respect to an ideal clock source is referred to as jitter. A clock jitter degrades the performance of a discrete-time delta-sigma by corrupting the input even before it is processed by the converter[20]. In the frequency domain, jitter has the effect of down-modulating the out-of-band noise back into the audio bandwidth, reducing the maximum achievable SQNR. Employing multi-bit DACs helps reduce the sensitivity to clock jitter as the error is reduced with a smaller step size in the DAC output signal. On the other hand, multi-bit DACs are inherently more prone to non-linearity due to mismatch between the single elements of the DAC. For this reason[1], a 3-levels (1.5 bits) I-DAC is chosen, and therefore a low-jitter clock source is assumed. Figure 2.11 shows the simulated jitter performance at the output of the multi-level DSM, in black, and after the DPWM block, in red, for a maximum input amplitude of 0.9 FS. As shown, to achieve an SQNR of 126 dB, a clock source with an absolute jitter of 100 fs RMS or lower is required.

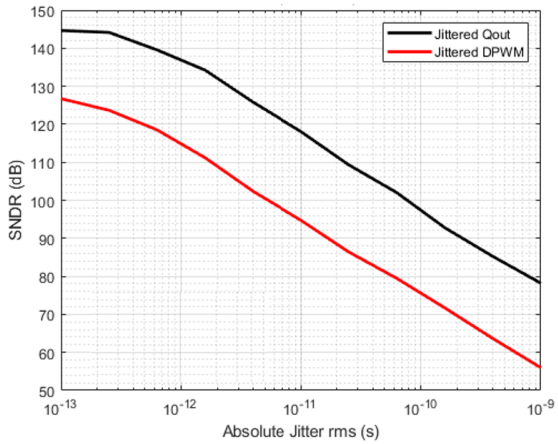

Figure 2.11: Jitter performance of the proposed digital Input CDA architecture.

[1] and for noise advantages as will be explained in Chapter 3

2.4 Analog Class-D Amplifier Loop

Figure 2.12 shows the complete system-level architecture of the proposed digital-input CDA. The digital code from the D-PWM is transformed into a 3-levels current using a 3-levels current steering DAC. This current is then injected into a fully differential third-order analog loop filter built around a non-traditional 3-levels power stage to compensate for its non-linearities as in [23]. The extra level introduced in the power stage minimizes switching activity in idle operation without needing extra flying capacitors, complex circuitry, or extra supplies, as will be explained in detail in Chapter 3. Furthermore, the output stage switches deferentially, providing a stable mid-rail common-mode level.

PWM re-modulation is necessary to avoid an otherwise self-oscillating operation of the analog loop. The multi-level PWM re-modulation scheme is implemented with two comparators by comparing an inverted and a non-inverted triangle wave to the loop filter output.

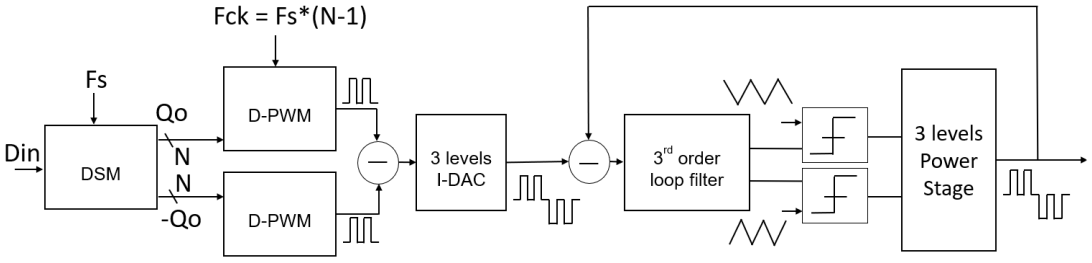

Figure 2.12: High-level architecture of the proposed digital input class-D amplifier.

A third-order loop filter in Figure 2.13 provides high loop gain and, thus, high linearity in the audio bandwidth. Two feedforward paths introduce two zeros in the loop gain to compensate for the three poles in the origin and make the loop stable. A local resonator is introduced between the output of the third integrator and the first one to introduce a pair of complex and conjugated poles and increase the loop gain in the audio bandwidth.

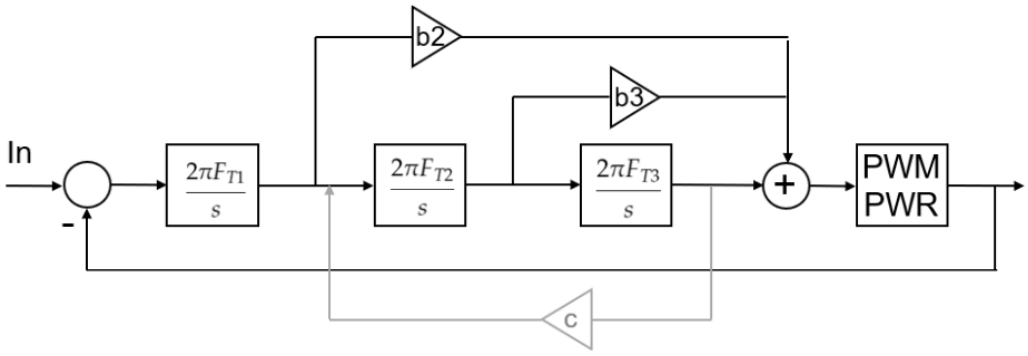

Figure 2.13: Feedforward analog loop filter with local feedback.

The loop-gain in the Laplace domain:

$$H(s) = 2\pi F_{T1} 2\pi F_{T2} 2\pi F_{T3} \left(\frac{b_2}{2\pi F_{T2} 2\pi F_{T3}} s^2 + \frac{2\pi F_{T2} b_3}{2\pi F_{T2} 2\pi F_{T3}} s + 1 \right) \cdot \frac{1}{s^3} \tag{2.7}$$

From which, the location of the compensating zeroes and the characteristics of the loop:

$$F_z = \sqrt{\frac{F_{T2} F_{T3}}{b_2}} \qquad \zeta = \frac{b_3}{2F_{T3}} \cdot F_z \qquad K = 2\pi F_{T1} 2\pi F_{T2} 2\pi F_{T3} \tag{2.8}$$

In order to maintain a low switching activity, a low-power triangle wave generator built around a simple RC integrator generates two 480 kHz triangle waves shifted by 180°. The differential switching rate of 960 kHz enables a 290 kHz loop bandwidth [2] based on stability conditions and a loop gain larger than 60 dB over the audio band. Figure 2.14 shows the simulated nominal loop gain amplitude and phase, showing a stable system with a phase margin of around 65.3°.

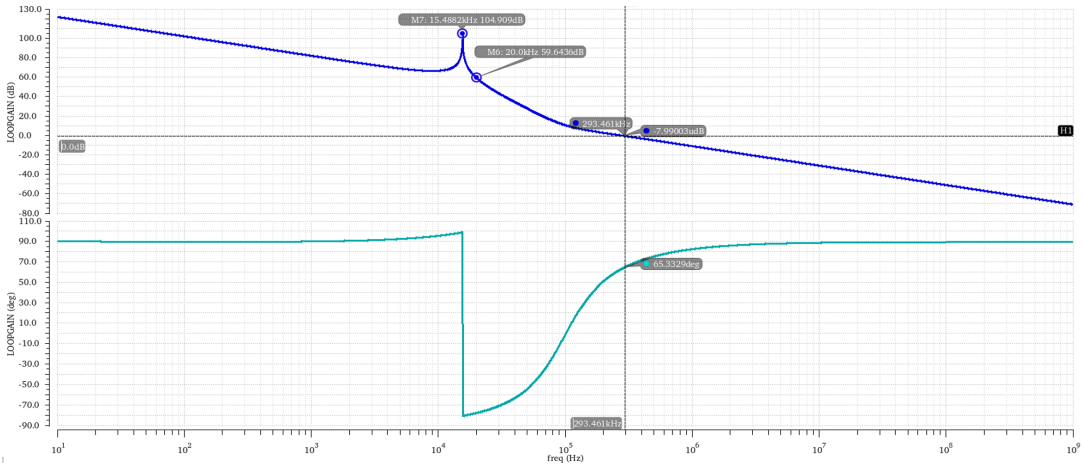

Figure 2.14: Loop Gain of the 3rd order CDA loop filter.

3 Circuit Design

The following chapter describes the circuit implementations of the architecture illustrated in Chapter 2. As the application requires a low-quiescent current, particular attention is placed on the design of the analog blocks from an idle-power consumption point of view. For this reason, several recently published techniques were implemented to achieve lower noise and lower power consumption without affecting their performances.

3.1 Analog Loop Overview

The D-PWM block is followed by a coarse DAC. Popular configurations used in Oversampled DACs are the current steering DAC (I-DAC) and resistor DAC (R-DAC) structures. I-DAC architectures using three-level elements have a fundamental advantage in terms of thermal noise and characteristics that make them suitable for low-power audio designs[18]. During the third phase of the I-DAC, which due to the PWM scheme, mostly occurs for low input amplitude, the DAC is disconnected from its output. This characteristic plays a fundamental role in the proposed architecture's DR performances. The noise contribution of the DAC, which is dominant for large signals, does not play a role in the determination of the DR, as for small signals, the DAC is mostly disconnected, and its equivalent output noise can be considered negligible with respect to the other noise sources[15].

Fig. 3.1 shows the block diagram of the analog part of the proposed architecture. The I-DAC directly drives the first stage of the analog loop filter. Traditionally, Class-D amplifiers have large output common-mode (CM) swing, requiring an I/V amplifier between the DAC and the first integrating stage to isolate the I-DAC from the voltage fluctuations due to the output CM variation. An alternative is to have a local fast CM stabilization circuit, but it would increase the complexity of the design and the power consumption as a result of that. In this design, a 3-levels, CM-stabilized output stage is employed, minimizing the noise and complexity of the system [17]. Furthermore, the additional level introduced at the output reduces the switching activity, reducing the total power consumption [23].

The selection of the loop feedback resistor R_{FB} is of fundamental importance as, together with the DAC and the loop filter, it is a dominant noise source. Furthermore, its value also dictates the current that the I-DAC needs to sink or source and therefore poses a basis for the expected power consumption of the system.

Assuming the noise coming from the DAC is negligible, the Dynamic Range of the proposed structure can be found by calculating the equivalent differential noise power density at the input of the loop filter:

$$P_{N,in,diff} = P_{N,LF,diff} + 8KTR \quad \left[V^2/Hz\right] \tag{3.1}$$

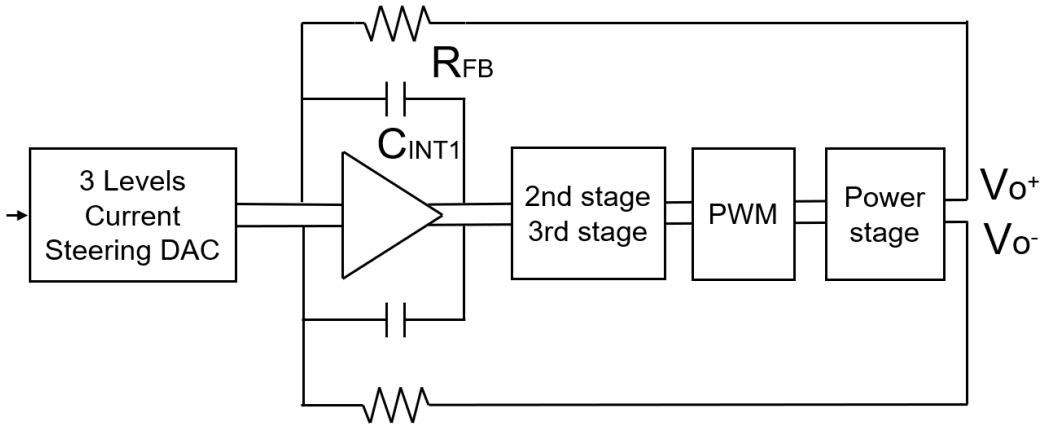

Figure 3.1: Block diagram of the analog portion of the proposed class-D amplifier.

Figure 3.2 shows the theoretical relationship between the dynamic range of the proposed architecture, the feedback current (imposed by the unit DAC current), and the value of the feedback resistor R_{FB} in the condition in which the noise generated by the first Operational Transconductance Amplifier (OTA) of the loop filter is designed to exhibit the same noise generated by the feedback resistors.

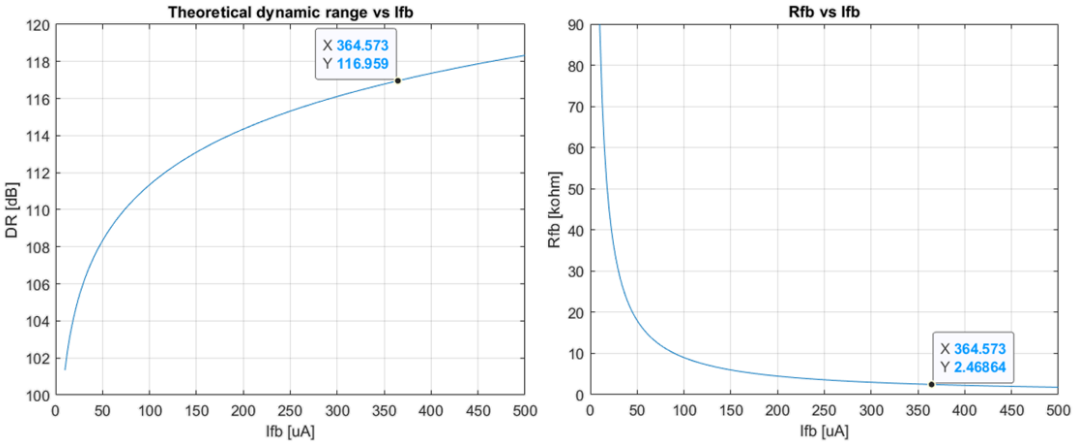

Figure 3.2: Relationship between R_{FB}, DR and the feedback current I_{FB}.

The resistor is chosen based on the requirement described in Chapter 1 equal to $R_{FB} = 2.4\ k\Omega$, which set a nominal $DR = 117\ dB$, and the current sank and sourced by the DAC equal to $I_{FB} = 375\ uA$.

3.2 Three Levels Current Steering DAC

The DAC must be able to maintain an SQNDR larger than 120 dB to keep enough margin for the following blocks in the signal chain. A low-noise biasing circuit was designed to achieve an SNR equal to 117 dB for large signals by employing a mirrored noise filter. The idle power consumption was reduced by implementing a dynamic operation of the DAC during the dump phase.

The basic operation of a differential 1.5 bits (3 levels) current steering DAC is shown in Figure 3.3. Its behavior can be studied considering three different phases.

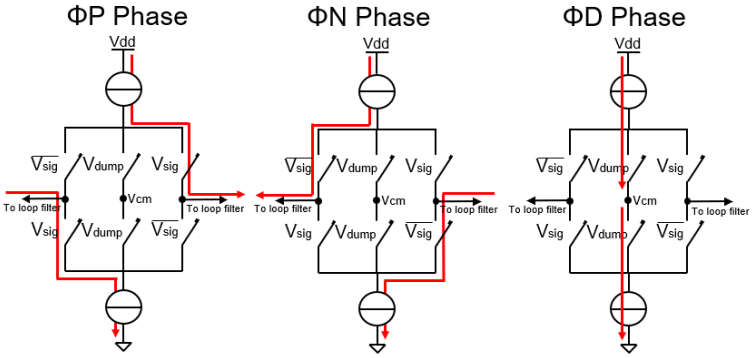

Figure 3.3: Basic operations of a three levels current steering DAC.

During the two signal phases, Φ_P and Φ_N , a set of two switches are activated either to source the current from the top current source and inject it inside the loop filter or to sink it from the loop filter towards the bottom current source. In these two phases, the equivalent output noise is defined by the noise generated by the current sources.

During a third dump phase, Φ_D, the switches closed during the signal phases remain open, and an additional couple of switches close to letting the current flow internally in the DAC, the central node V_{CM} is connected to a buffer to prevent the current from flowing directly from the power supply to ground. In this phase, the DAC presents a couple of high-impedance nodes at its output, and the noise generated by the DAC is virtually null.

The noise generated by the three-levels I-DAC is, therefore, code-dependent and ultimately depends on the duty cycle of the input D-PWM signal. On average, the DAC-generated noise is maximum when the input duty cycle is large (corresponding to a larger input amplitude and a shorter dump phase) and minimum when the input duty cycle is small (corresponding to a smaller input amplitude and a longer dump phase).

The current references of the DAC should be designed to minimize their noise contribution as they pose a fundamental limitation for the peak THD+N characteristics of the CDA due to the linear relationship between the code and the output noise as expressed in the equation below:

$$I_{n\_ref} = Code \cdot I_{n\_ref0} \tag{3.2}$$

where I_{n_ref0} represents the current noise contribution of a single DAC current source while I_{n_ref} represents the total noise.

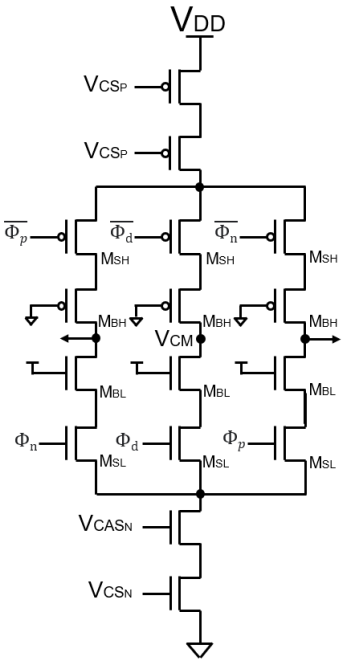

Figure 3.4: 3 levels I-DAC implementation.

Figure 3.4 shows the transistors implementation of the DAC. Cascoded current sources are employed to increase their output impedance and shield the current source transistor from voltage variations due to clock feed-through.

Additional always-ON transistors M_{BL} and M_{BH}, have been added to shield the output nodes from clock feed-through coming from the signal switches, resulting in signal-dependent glitches causing distortion [14].

Additional signal-dependent glitches are due to voltage variation across the cascaded current sources during a phase transition. A simplified schematic of the DAC only showing the signal switches is shown in Figure 3.5. If the driving signals are not appositely designed with an overlapping clock scheme, during a transition between two different phases, there could be a short period in which none of the switches are closed. In this situation, the parasitic capacitance C_X would discharge, and the current source would not have enough voltage headroom to be maintained in saturation, ultimately switching off. When the current source would switch on again, the initial charging of C_X would cause a current spike which would inject a high-frequency glitch into the loop filter resulting in distortion.

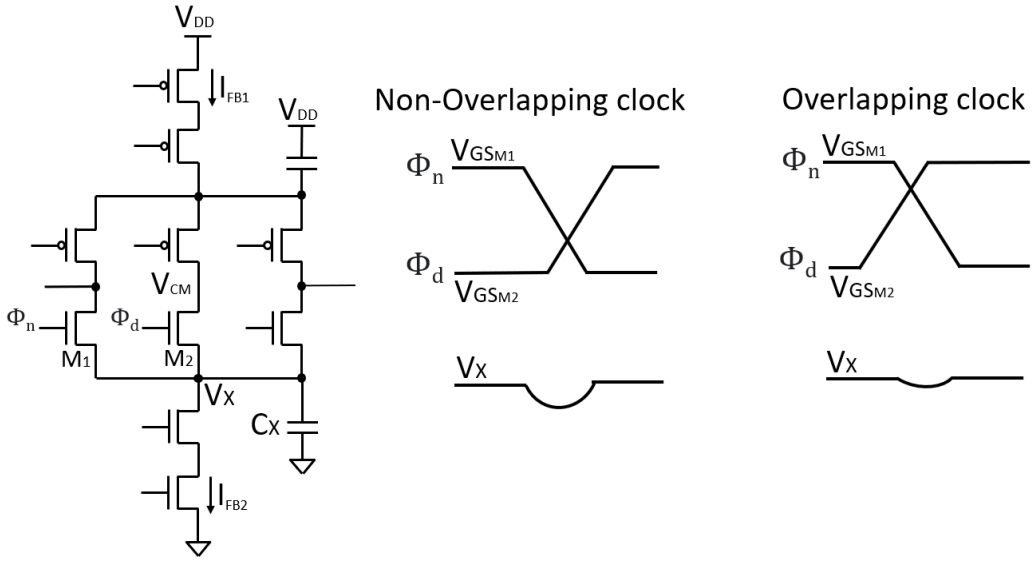

Figure 3.5: Glitches in the three levels current steering DAC.

Figure 3.6 shows the 3-transistors inverter used to generate the overlapping driving signals and a simulation of its transfer curve characteristic. This non-traditional inverter makes the selection of the trip point easier by adding a third central transistor working as a voltage-controlled resistor.

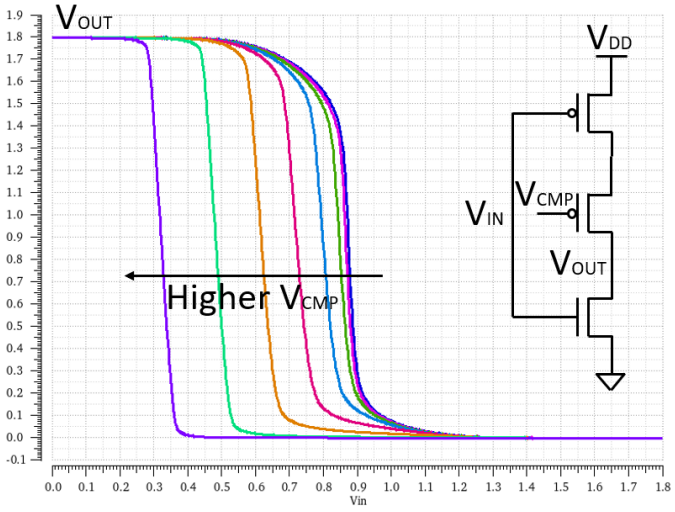

Figure 3.6: Characteristic transfer curve of a 3-transistors inverter.

3.2.1 Biasing Network

The noise of the DAC current sources limit the peak THD+N achievable by the CDA. The I-DAC biasing network is shown in Figure 3.7.

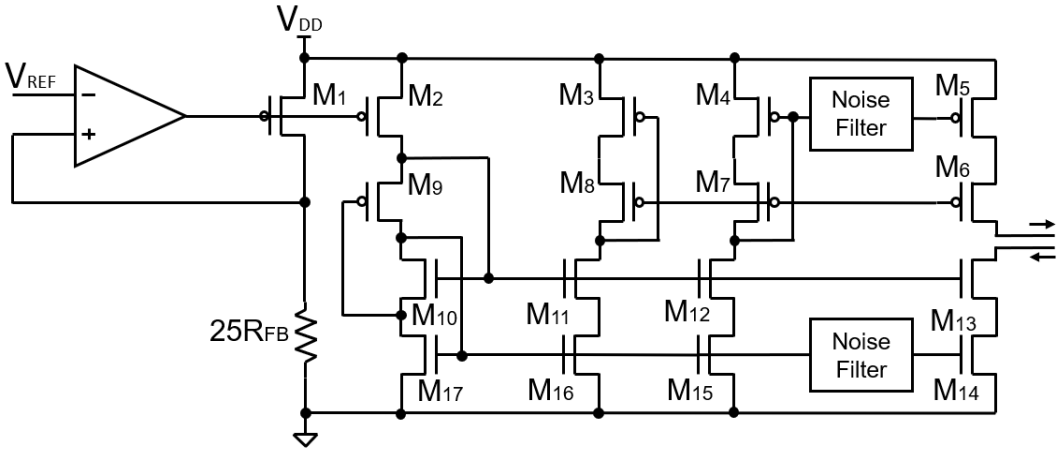

Figure 3.7: Input I-DAC biasing network.

The reference current is generated by applying a reference voltage over a resistor proportionally matched to the feedback resistor R_{FB}.

To minimize the power consumption of the biasing block, a reference current 25 times smaller than the feedback current, was chosen. This represents an advantage in idle power consumption but results in a more significant mirrored noise coming from the biasing network, which adds to the thermal noise generated by the current sources M_{14} and M_5.

An additional noise filter is implemented to decrease the equivalent noise bandwidth at the input of the current source transistors [15].

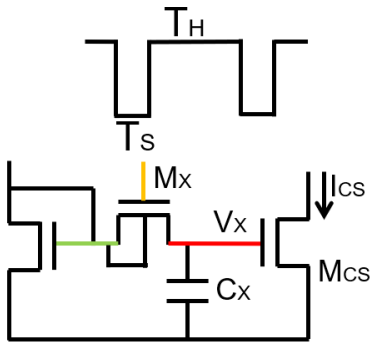

Figure 3.8: Noise filter implementation.

Figure 3.8 implements a low-bandwidth low-pass filter using an OFF transistor M_X as a high-value resistor. The transistor M_X is controlled by a long Hold square wave signal to compensate for the eventual gate leakage of M_{CS}, which would cause a shift to the gate voltage V_X and therefore change the value of the current I_{CS}

The filter reduces the equivalent noise bandwidth at the M_{CS} gate, making negligible the noise coming from the preceding biasing network. An additional noise source with an integrated power noise equal to KT/C is introduced due to the switching behavior of M_X. However, this additional noise source is unimportant due to the cyclo-stationary property of white noise, which makes the power noise negligible. The KT/C noise is indeed averaged based on the low-duty cycle of the controlling signal at the gate of M_X.

Figure 3.9 demonstrates the effect of the noise filter in the time domain by showing the V_X node before and after the additional filter.

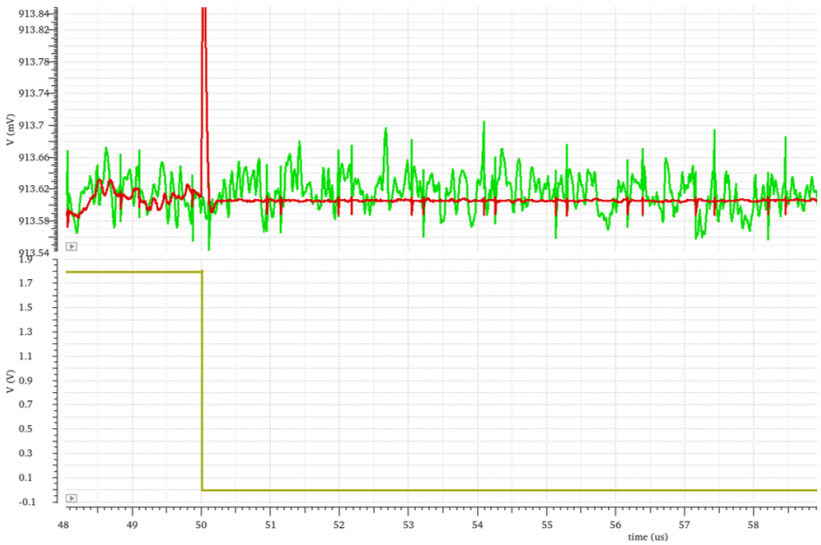

Figure 3.9: Time domain simulation of the circuit in Figure 3.8.

The design of the current source transistors M_{14}, M_5 follows a traditional procedure in which their operating point is set as much into strong inversion saturation, keeping enough voltage headroom to maintain the current sources in saturation.

3.2.2 Dynamic Dump-State

During the dump phase, the DAC is disconnected, and the current constantly flowing in the middle branch is not used for signal purposes. This wasted current, not negligible in value, adds up to the idle state power consumption. As explained in Section 3.2, the current sources cannot be entirely switched off without introducing a high-frequency glitch that would compromise the DAC linearity.

To obviate the need for a constant current through the DAC, the current sources can be switched on only for a certain amount of clock periods before the next signal state and switched off otherwise. Using this technique, the current sources would switch on for enough time before the signal state and be able to charge the parasitic capacitance avoiding the current glitch. The current sources would otherwise be entirely off, saving idle power consumption.

Since the driving signals are still in the digital domain, the time window needed to activate the current sources in the dump phase can be created by shifting the digital input signal by a fixed amount of clock periods.

The dynamic dump state mechanism is explained in Figure 3.10, in which the digital signal was shifted by one clock period for simplicity.

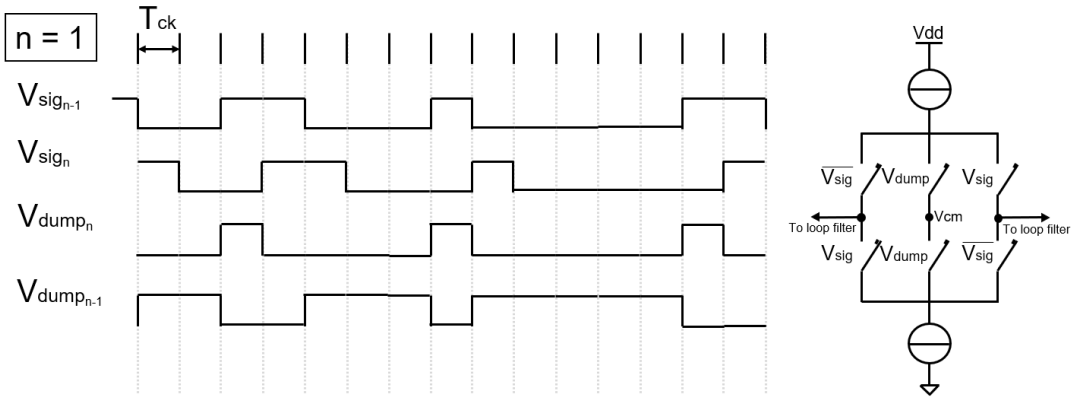

Figure 3.10: Dynamic dump-state time waveforms.

The waveforms $V_{sig_{N-1}}$ and $V_{dump_{N-1}}$ represent the signal and dump state before the dynamic technique is applied. It can be noticed that the signals are complementary, meaning that the current sources are always switched on. The signal state is then shifted by one clock period in V_{sig_N}.

V_{dump_N} can now be generated using some simple digital logic on V_{sig_N} and $V_{sig_{N-1}}$. Now the dump state is not a complementary version of the signal state anymore, and the current sources can be entirely switched off with the consequence of saving power consumption.

3.3 Analog Loop Filter

The current sourced by the I-DAC is directly injected inside the third-order loop filter built around the power stage to compensate for its non-linearities in the audio bandwidth. Figure 3.11 shows the single-ended, simplified implementation of the block diagram shown in Figure 2.13.

A targeted loop gain in the audio bandwidth larger than 60 dB was obtained by a third-order loop filter, designed to keep the stability conditions under corners, $F_{UG} < F_{PWM}/\pi = 306\,kHz$. Low power consumption is achieved by employing feedforwarded OTAs and using the assistant DAC technique in the design of the input OTA.

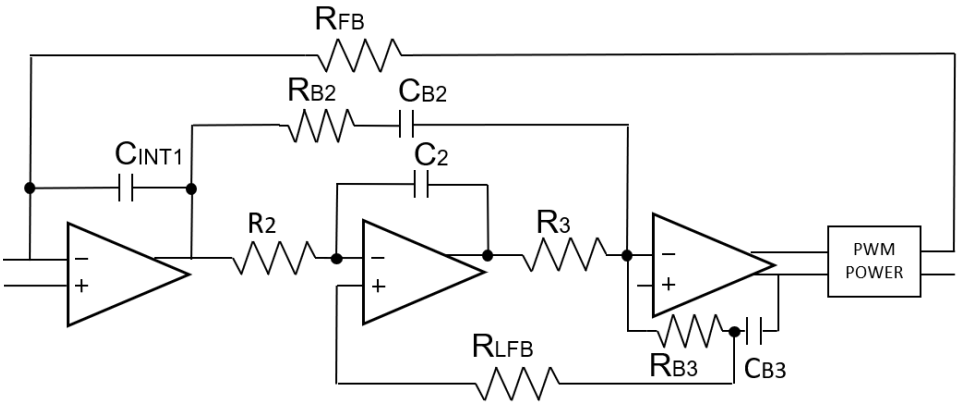

Figure 3.11: Simplified, single-ended version of the third-order loop filter.

The poles in the origin are implemented with RC integrators. The feedforward paths are implemented in a continuous time fashion by the ratio of the RC series between the R_{B2},C_{B2}, and R_{B3},C_{B3}. The local resonator is implemented with the resistor R_{LFB} between the output of the third integrating stage and the virtual ground of the second stage. 2 bits trimming is applied to all the capacitors to maintain a robust design under time-constant variations.

The feedforward architecture employed in the loop filter has a significant advantage in terms of noise with respect to a feedback structure. The location of the zeros: $F_z = \sqrt{(F_{T2}F_{T3})/(b_2)}$ does not depend on the unity gain frequency of the first integrator $F_{T1} = 1/(2\pi R_{FB}C_{INT1})$ that can therefore be set independently based on the stability condition and the noise considerations for R_{FB}. Since R_{FB} was set to a relatively low value to minimize its noise contribution, an independent Ft1 enables an additional degree of freedom in the choice of the integrating capacitance C_{INT1} and, therefore, the chip area.

As commonly happens, the first stage of the loop filter is the more demanding in terms of power consumption due to its stringent requirement in terms of thermal noise and linearity. In particular, the linearity conditions are exacerbated by the large swing switching signals from the power stage that the OTA has to process. Furthermore, the OTA would need to sink and source the relatively high amplitude current injected by the DAC, further increasing the OTA biasing currents and, therefore, its power consumption.

Two low-power techniques are applied to the loop-filter first OTA to reduce its power consumption. The first technique uses a so-called Assisting DAC [22], in charge of sinking and sourcing the major part of the current that would otherwise need to be supplied by the OTA. The second technique consists in using a two-stage feedforward compensated OTA [23]. With respect to a more traditional Miller-compensated Op-Amp, it does not need to continuously charge and discharge the Miller capacitor and therefore is intrinsically less power-hungry. The diagram of the proposed first integrating stage is shown in Figure 3.12.

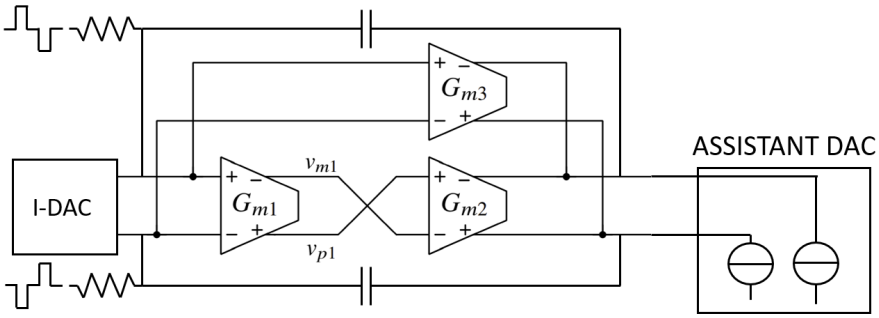

Figure 3.12: Diagram of the first OTA of the loop filter with the assistant DAC.

Ideally, the assisting DAC sinks and sources a copy of the current through the integrating capacitor C_{FB}, generated via the subtraction between the current through the feedback resistor R_{FB} and the current injected by the input I-DAC. This 3-level current can be supplied by a DAC similar to the input one, digitally controlled by the driving signals controlling the input I-DAC and the ones controlling the output power stage.

As shown in [22], particular attention must be paid to matching the current waveforms, as every current mismatch has to be supplied by the OTA, which can now not supply large currents.

Figure 3.13 shows a simulation of the current waveforms in the first integrating stage. The top pane in blue shows the current through the integrating capacitor C_{INT1}. The second pane, in red, shows the current flowing through the assisting DAC, while the current sunk by the OTA is in yellow. Although its absolute value is strongly reduced, it is not entirely null due to the extra current for which the OTA has to compensate.

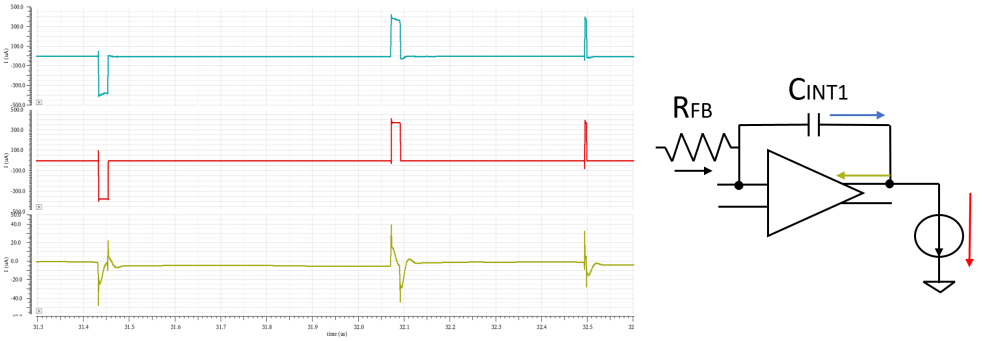

Figure 3.13: Time domain simulation of the currents in the first loop filter OTA.

Figure 3.14 shows the implementation of the feedforward OTA used as the main architecture to implement all the OTAs in the loop.

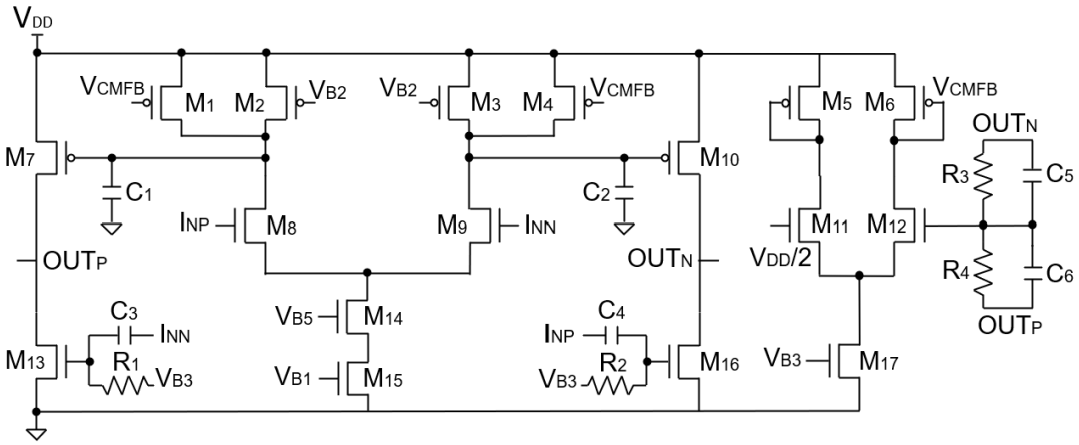

Figure 3.14: Two-stages feedforward compensated OTA.

The 2-stage feedforward compensated OTA is implemented by ac-coupling the inputs to M_{13} and M_{M16}. This allows for a higher gain-bandwidth frequency (and hence a more linear amplifier) without increasing the power consumption.

The noise levels of the OTA are fixed based on Section 3.1 by sizing the first stage of the OTA appositely. In particular, the cascoded tail current source formed by M_{14} and M_{15} is biased in strong inversion, and the input differential pair transistors M_8, M_9 are biased in weak inversion to reach the needed transconductance.

3.4 Triangle Wave Generator

The analog BD-PWM re-modulation inside the loop filter needs the generation of two triangle waves shifted 180° between each other. Since power efficiency is a central theme in this thesis work, a simple triangle waveform generator based on an RC integrator was chosen.

A targeted specification on the linearity of the output triangle waves, with amplitude 0.9 FS, resulted in a loop gain at the carrier frequency of 480 kHz, smaller than -26 dB, that was found by simulation. Feedforward compensated OTAs are used to keep low power consumption. A 2-bits capacitive trimming circuit maintains time-constant variations over corners.

The architecture employed is shown in Figure 3.15.

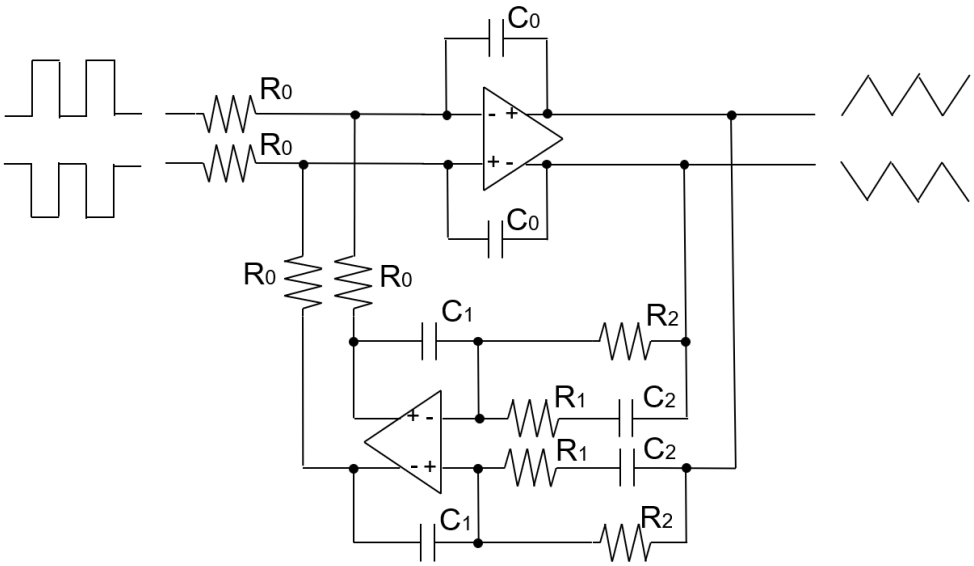

Figure 3.15: Implementation of the low-power triangle wave generator.

The two triangle waves are simply generated by integrating two complementary square waves via a fully differential RC integrator. A DC Servo-Loop is built around the top integrator to fix the DC operating point of the OTAs. The circuit has to be designed to achieve a linear behavior of the triangle waves so that it does not compromise the linearity of the loop filter during the PWM generation.

The loop-gain can be easily calculated as follows:

$$L(s) = \frac{1 + \frac{s}{C_2(R_2+R_1)}}{\left(\frac{s}{R_0C_0}\right)\left(\frac{s}{R_2C_1}\right)\left(1 + \frac{s}{R_1C_2}\right)} \tag{3.3}$$

An asymptotic representation of the loop gain is shown in Figure 3.16. F_{CK} represents the switching frequency of the triangle waves, equal to 480 kHz. The loop gain at this frequency sets the linearity of the triangle wave, as shown in the simulation in Figure 3.17, in which two triangle waves with different loop gains at F_{CK} are shown.

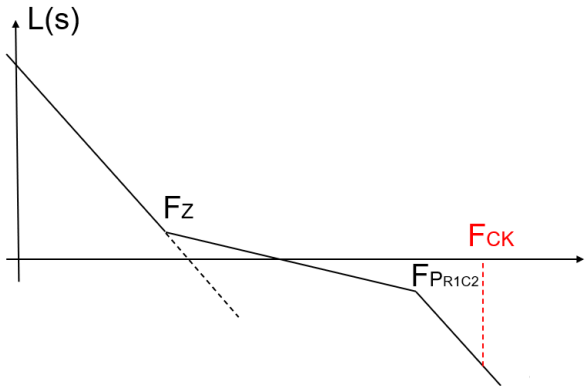

Figure 3.16: Asymptotic loop gain of the circuit in Figure 3.15

The simulation shows that the lower the gain, the more linear the output triangle wave. For this reason, the pole formed by R_1 and C_2 was added after the crossover frequency. On the other hand, the relative location between this pole and the zero F_Z is set to maintain the stability of the loop.

Finally, the pole in the origin formed by R_0 and C_0 generated by the forward path integrator controls the amplitude of the triangle waves.

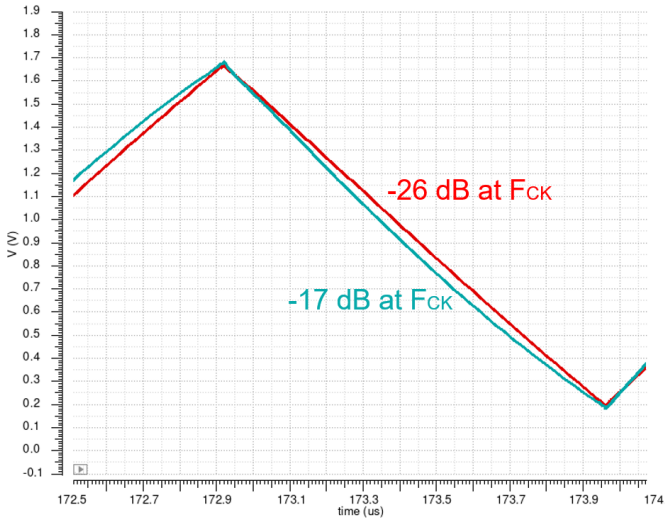

Figure 3.17: Effect of the loop gain at F_{CK} in the linearity of the triangle wave generator.

3.5 Power Stage

The non-traditional power stage, similar to [23], uses an additional set of switches to introduce an additional common-mode level. A simplified schematic portraying the power stage in the BTL configuration is shown in Figure 3.18.

During the common-mode phase, the transistors M_{C1} and M_{C2} turn on such that the V_{PWMA} and V_{PWMB} nodes are brought to the same voltage level, and the current through the load is null.

This scheme has two fundamental advantages. The 3-level power stage perfectly adapts to the operation of the 3-levels Current Steering DAC. The differential structure stabilizes the CM level so that the I-DAC can directly connect to the loop filter. Furthermore, the additional level in the power stage decreases the switching rate and consequently decreases power consumption.

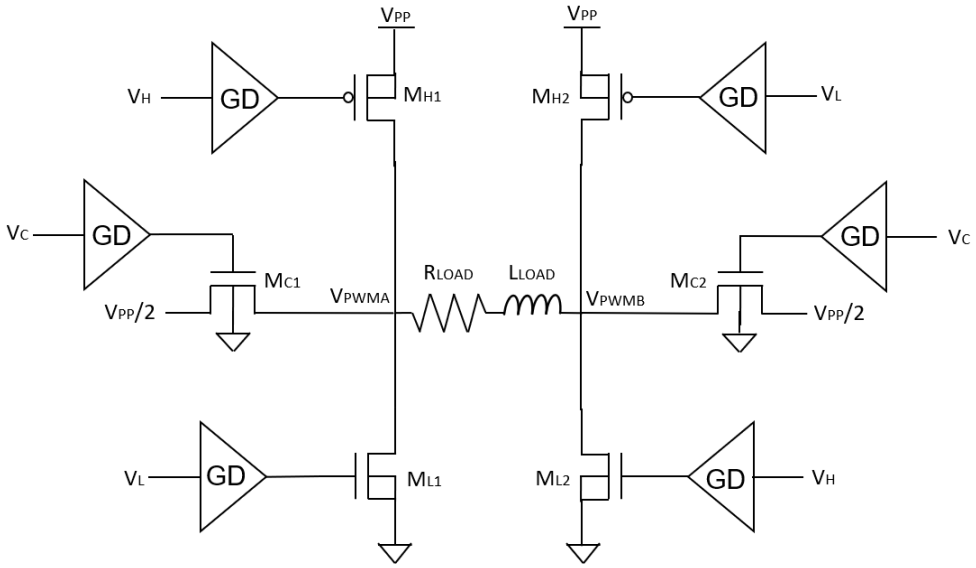

Figure 3.18: Proposed three levels power stage.

Since the final application of this thesis work is a low-power audio amplifier, it is desirable to use low-voltage transistors as output transistors.

Therefore, particular care must be placed in the power stage design as the phenomenon of ringing and body diode conduction can easily pull the output nodes V_{PWMA} and V_{PWMB} above and below the supply rails.

Figure 3.19 shows the phenomenon of ringing. On the left of the figure is depicted the top power stage transistor connected between the supply rail and the load. Since the connection to the power rail pin is usually made using bonding wires, modeled in the first instance as electrical components introducing a certain amount of inductance, the power stage transforms into a resonant circuit with a specific resonance frequency. When a fast transition happens in the power stage, the resonance circuit is excited, and ringing appears in the output transient.

The ringing effect can be reduced by slowing the transitions in the output power transistors. Naturally, this poses a fundamental trade-off with the switching losses.

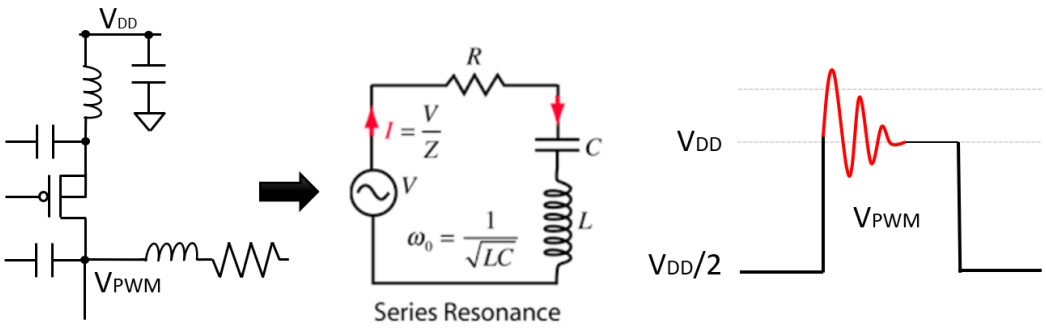

Figure 3.19: Ringing in class-D amplifier power stages.

The second source of overshoots is due to the conduction of the bulk diode, as depicted in Figure 3.20. The figure depicts the transition between the state in which the top transistor is turned on and the common mode state in which the middle transistor is activated. The driving signals of the power transistors are rendered in blue and yellow. If a period in which both transistors are off (dead time) exists, the current will continue to flow through the inductive load by turning on one of the body diodes of the output transistors.

The effect of body diode conduction can be removed entirely by imposing a crossover between the driving signals of the power transistors (dead time equal to zero or even a negative dead time). Naturally, this has effects on the shoot-through current, as for a certain period, transistors connected to different voltage potentials will be active at the same time, generating a current through them.

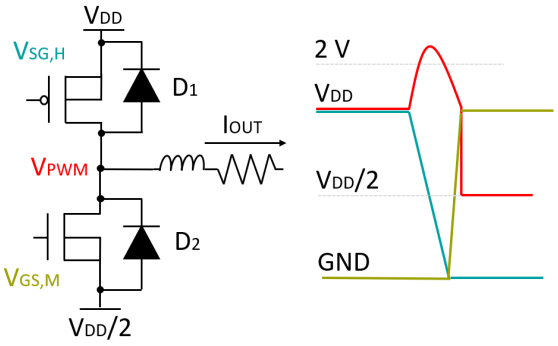

Figure 3.20: Dead-time in class-D amplifier power stages.

Figure 3.21 shows one side of the power stage and its PWM waveforms. The top figure draws attention to the transition between the middle and lower states. The output node V_{PWM} switches between $V_{PP}/2$ and GND; the source of the middle-level transistor is equal to the output node V_{PWM}. The V_{GS} of the middle transistor is, therefore, V_{DD} when the transistor needs to be switched on and zero when the transistor switches off, as the absolute values of V_{PP} and V_{DD} are the same.

The bottom figure draws attention to the transition between the higher and middle states. The output node V_{PWM} switches between V_{PP} and $V_{PP}/2$; the middle-level transistor's source is equal to the output node $V_{PP}/2$. In this second case, the V_{GS} of the middle transistor is, therefore, $V_{DD} - V_{PP}/2 = V_{PP}/2$ when the transistor needs to be switched on and $-V_{PP}/2$ when the transistor switches off. Since $V_{PP}/2 = 0.9\ V$ and $V_{TH} \simeq 0.7V$, the middle transistor is not fully turned on in this state transition, and a bootstrap circuit needs to be implemented in the middle state transistor.

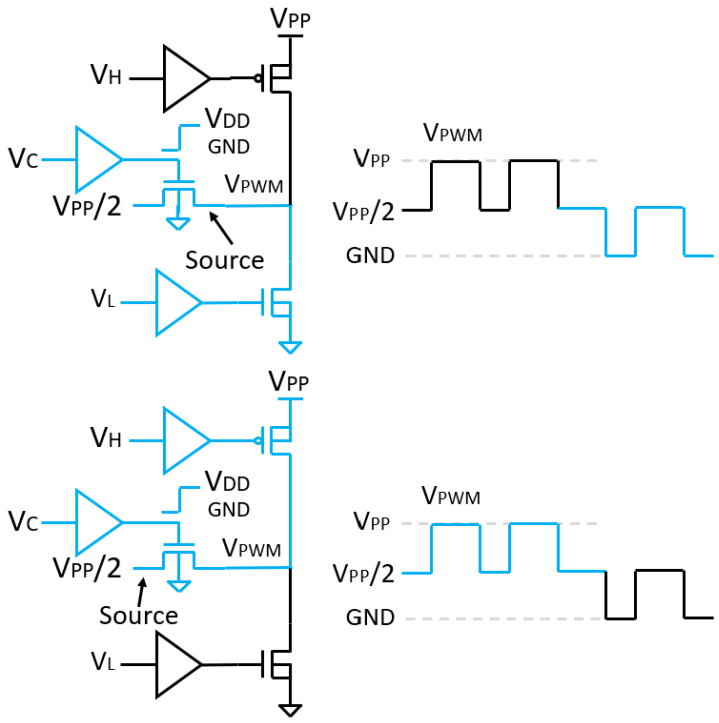

Figure 3.21: Operation of the three levels power stage.

3.5.1 Gate Drivers

Figure 3.22 shows a simplified version of the bootstrapped gate driver of the common-mode transistor, along with the waveforms explaining its behavior.

The driving signal V_C in the $0 - 1.8\ V$ domain is generated from the output of the PWM re-modulator to activate the common-mode transistor when pulled to a $1.8\ V$ and deactivate it when pulled to GND. Initially, V_C is $0\ V$, and the node V_{BOOT} is connected to $V_{DD} = 1.8\ V$through a Schottky diode, letting the capacitor C_{BOOT} charge to a voltage equal to around $1.8\ V$ (considering negligible for this simplified analysis, the voltage drop around the diode). In this scenario, the node $V_G = 0\ V$, and the common-mode transistor is switched off.

The driving signal V_C is then pulled to $1.8\ V$ since the charge through the capacitor cannot fully discharge, its voltage drop remains relatively constant, and the node V_{BOOT} raises to around $2.7\ V$. In this scenario, the node $V_G = 2.7\ V$ and the common-mode transistor is switched on.

By examining the V_{SGH} of M_1 and V_{GSL} of M_2, we can find that no level shifter is required. V_{GSL} assumes values between $-1.8\ V$ and 1.8 , while V_{SGH} assumes values between $0\ V$ and $2.7\ V$; therefore, M1 is the only transistor that needs to be 5 V rated, while all the others can be 2 V rated low-voltage transistors.

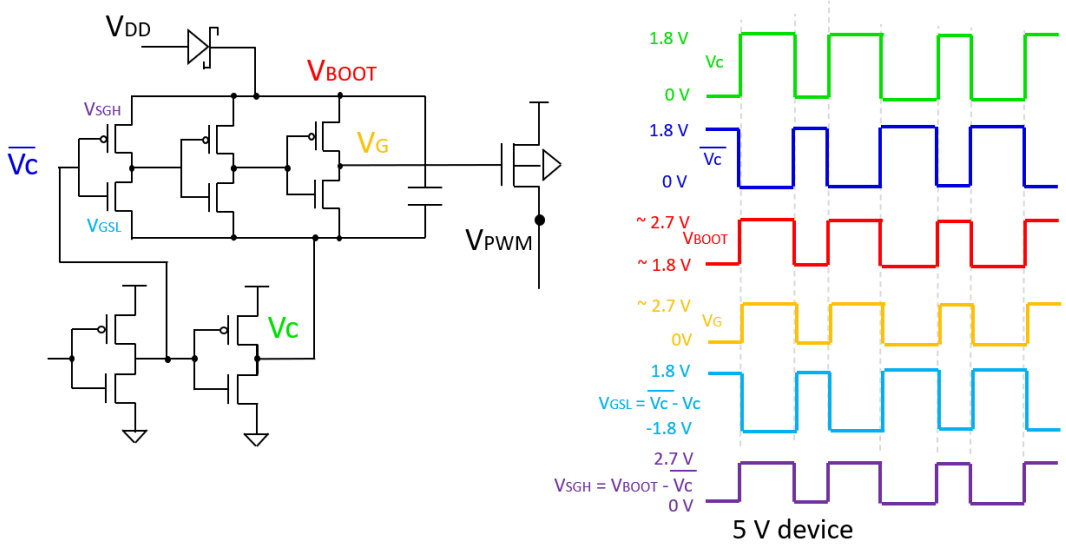

Figure 3.22: Proposed gate drivers for the power stage common mode transistor.

4 Simulation Results

Unless otherwise noted, all results presented in this chapter were simulated under the following conditions:

- The class-D amplifier is loaded by a 16 Ω resistor series with a 33 uH inductor.
- The output stage power supply $V_{PP} = 1.8\ V$.
- The analog loop power supply $V_{DD} = 1.8\ V$.
- The PWM re-modulation frequency inside the loop filter $F_{PWM} = 480kHz$.
- Bonding wires are modelled on every pin of the design, including a parasitic inductance of 2 nH. The bonding wire model is shown in Figure 4.1.

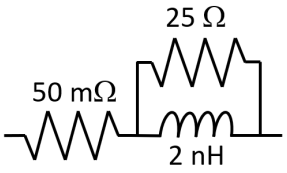

Figure 4.1: Bonding wire electrical model.

Figure 4.2 shows the current steering DAC driving signals over corners and input amplitude variations. As discussed in Chapter 3, an overlapping clock is implemented to avoid turning off the cascaded current sources.

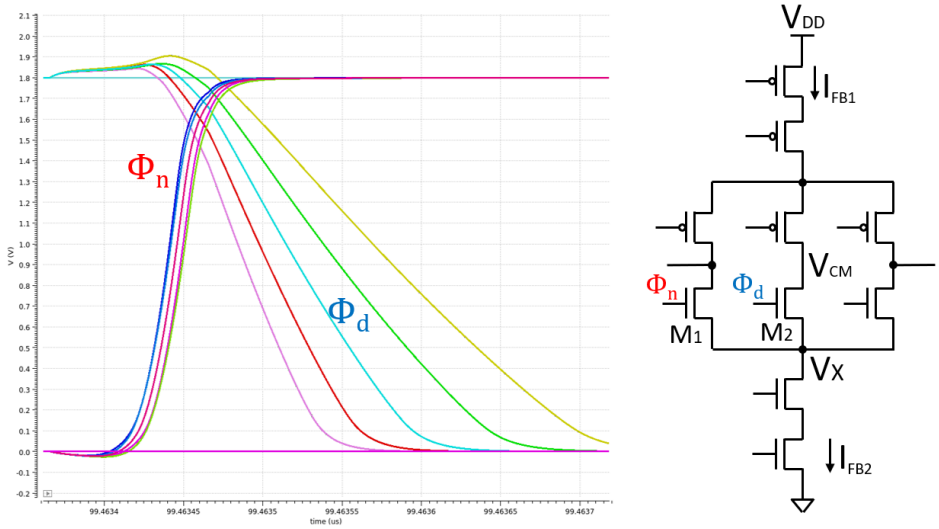

Figure 4.2: I-DAC driving signals over corners and input amplitude variations.

Figure 4.3 and Figure 4.4 show the Monte Carlo simulations of the input current steering DAC for input amplitudes of 0.9 FS and -80 dB FS. It can be noted that the variations between the top and bottom current sources of the I-DAC do not have a significant impact in terms of Signal-to-Quantization-Noise-Distortion-Ratio (SQNDR) at the output of the I-DAC.

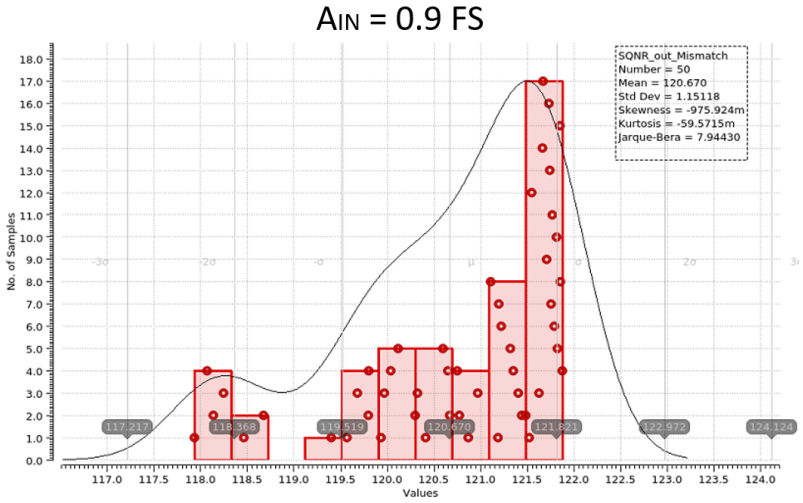

Figure 4.3: Input I-DAC Monte Carlo simulation at 0.9 FS input amplitude.

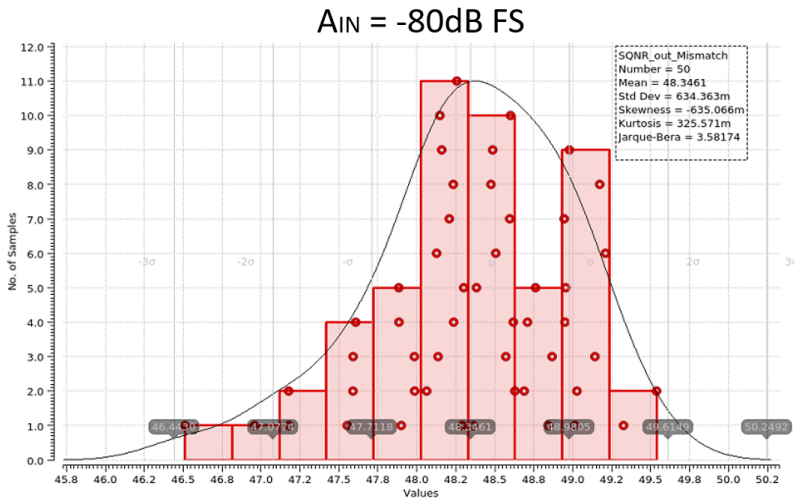

Figure 4.4: Input I-DAC Monte Carlo simulation at -80 dB FS input amplitude.

Figure 4.5 shows the Bode plot, Gain, and Phase, of the loop filter across corners variation. The loop filter results are stable across corners with a minimum phase margin of 58.24° and a minimum unity gain frequency of 239.7 kHz. A maximum unity gain frequency of 301.1 kHz agrees with the stability conditions that impose $F_{UG} = F_{PWM}/\pi = 306\ kHz$ [3].

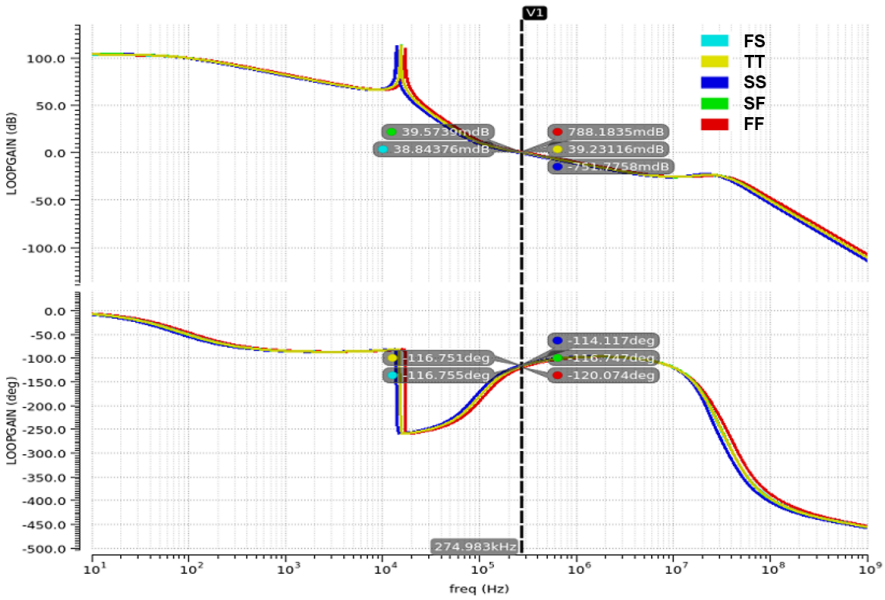

Figure 4.5: Loop filter Bode plot over corners variation.

Figure 4.6 shows a transient simulation showing the triangle waves generated with the circuit shown in Figure 3.15 over corners variation. The triangle wave amplitude nominally to 0.9 FS is controlled by a 2 bits capacitive trimming circuit.

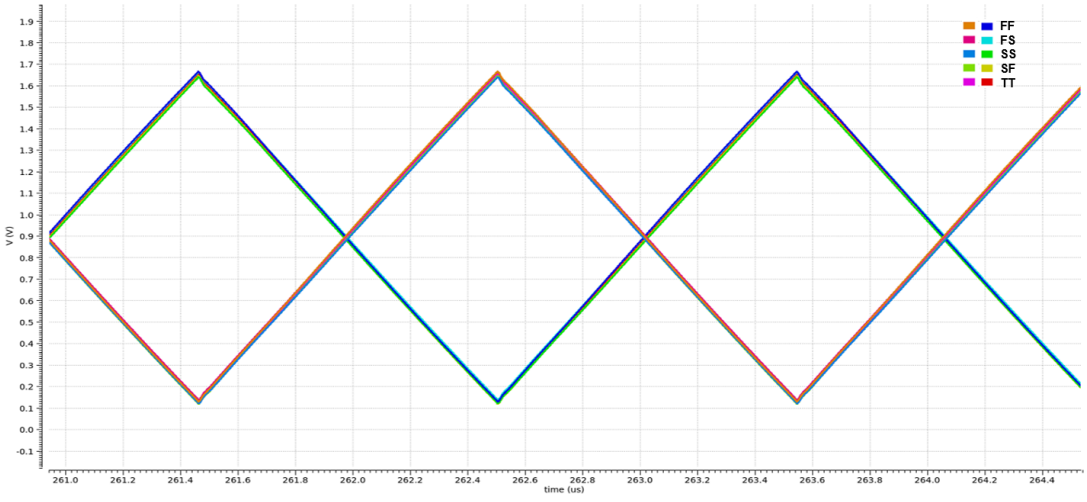

Figure 4.6: Triangle waves transient over corners variation.

Figure 4.7 shows the bootstrapped common-mode output transistor gate driver, as discussed in Section 3.5.1, proposed in the figure for convenience. The simulation shows a transition from a signal state where the $V_{PWM} = 1.8\ V$ to a common-mode state where $V_{PWM} = 0.9\ V$. The voltage at the gate of the common-mode output transistor is bootstrapped to a nominal voltage equal to 2.7 V.

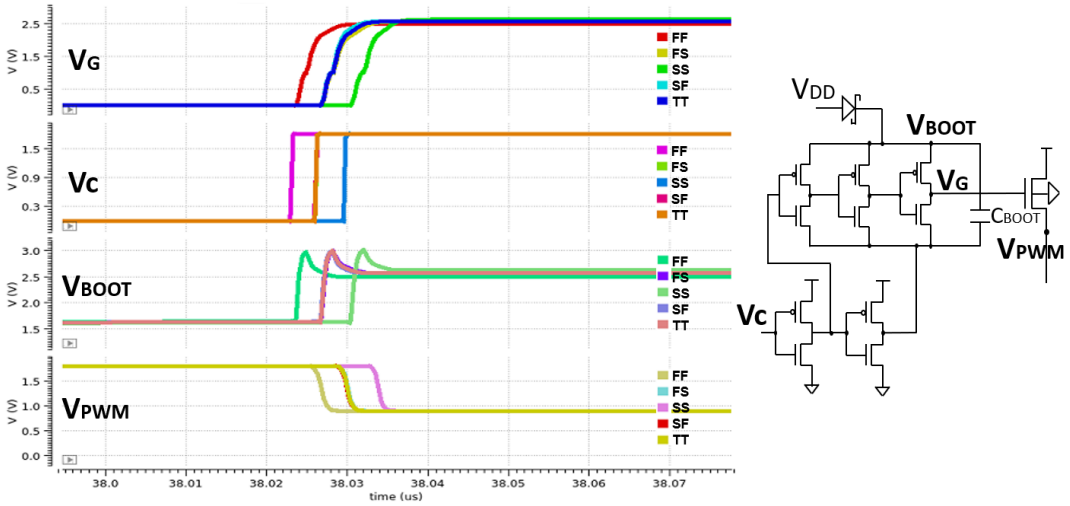

Figure 4.7: Bootstrapped output Common-Mode transistor transient simulation over corners variation.

The power stage was designed to achieve a peak efficiency higher than 90% over corner variations. Table 4.1 shows the simulated peak efficiency over corner variations:

	TT	SF	FS	FF	SS
Peak Efficiency [%]	91.4	91.4	91.4	92.2	90.5

Table 4.1: Simulated efficiency of the proposed class-D amplifier over corners variation.

The idle-state power consumption was simulated by letting the CDA operate with a null digital input. The power supplied by the system was then computed using the expression below:

$$P_{idle} = \frac{1}{T2 - T1} \int_{T1}^{T2} I_{DD}(t) \cdot V_{DD}(t)\, dt \tag{4.1}$$

The breakdown of the various sources of power consumption is shown in Figure 4.8. The relative percentages refer to the power consumption declared in Table 4.2 in the typical corner.

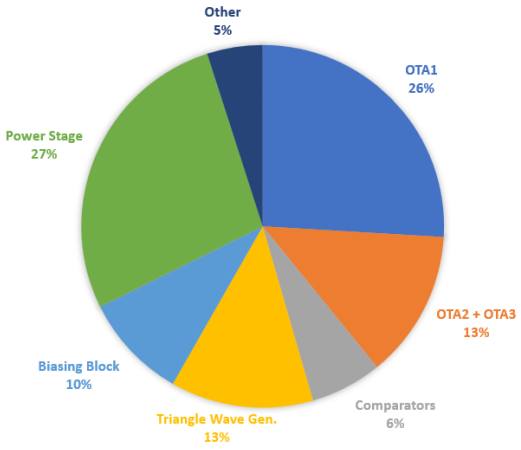

Figure 4.8: Idle power consumption breakdown of the proposed CDA.

Even though introducing an additional output level reduced the switching losses by minimizing the switching activity, the power stage represents the most power-hungry block of the class-D amplifier. As discussed in Section 3.5, this is due to a relatively high amount of shoot-through current needed to maintain a dead time equal to zero.

The first loop filter's two-stages feedforward compensated OTA closely follows the power stage in computing the relative idle power consumption. This is due to its power-hungry class-A output stage, which burns a constant amount of quiescent current.

The voice" Other" in Figure 4.8 includes the contribution of the input current steering DAC. Its low relative percentage demonstrates the positive effect of the implemented dynamic dump state on the idle power consumption of the proposed class-D amplifier.

Figure 4.9 shows the simulated spectrum at the output of the proposed class-D amplifier.

For a maximum stable input amplitude equal to 0.9 FS, the simulated nominal THD+N equals 111.3 dB. The DR was simulated by adding 80 dB to the SNDR of the system when driven by a -80 dB input amplitude; the proposed CDA achieves a nominal DR = 115.6 dB.

The performances of the proposed class-D amplifier in the various corners are summarized in Table 4.2.

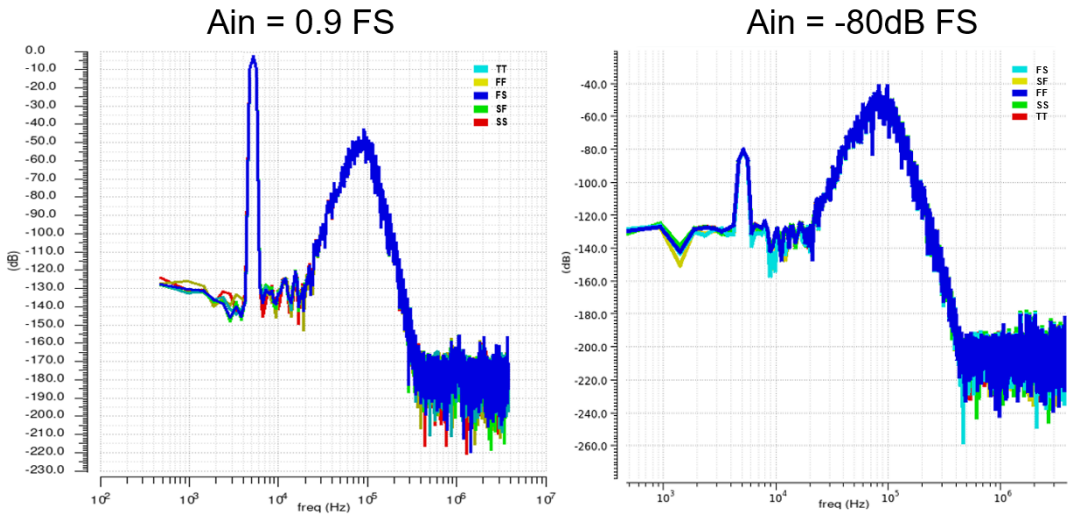

Figure 4.9: Simulated output spectrums for input amplitudes of 0.9 FS and -80 dB FS for the proposed CDA.

	TT	SF	FS	FF	SS
Peak THD+N [dB]	-111.3	-111.2	-111.2	-110.8	-108.7
DR [dB]	115.6	115.2	115.4	116.5	112.6
Idle-State Power Consumption [mW]	2.14	2.15	2.15	2.31	1.99

Table 4.2: Performances of the proposed class-D amplifier.

5 Conclusions and Future Work

A low-power, high dynamic-range, digital-input class-D amplifier has been designed for mobile audio applications. A Delta-Sigma PWM scheme is employed to drive the analog loop filter around the power stage. To keep the noise low for small signals and increase the dynamic range, a 3-level current steering DAC is employed in the digital-to-analog interface. A CM-stabilized 3-level power stage employing only low-voltage transistors was designed to minimize the switching activity and hence the power consumption of the class-D amplifier.

Pre-layout simulations indicate that this design meets the main targeted specifications of $THD + N < -110\ dB$, $DR > 115\ dB$ with a nominal idle power consumption equal to 2.14 mW while driving a 16Ω load.

Table 5.1 shows the proposed design's performances compared with similar class-D amplifiers.

	This Work (Pre-layout)	Matamura ISSCC'21	Chien ISSCC'20	Dooper JSSC'12	Cope ISSCC'18
Process [nm]	180	40	500	140	180
Supply [V]	1.8	1.8	5	5	20
Load [ohms]	16	16	8	4	4
Efficiency [%]	91.8	93	92	90	90
Loop Filter's Order	3rd	5th	2nd	2nd	5th
Peak THD+N [dB]	-111.3	-93.15	-100.91	-76.5	-97.72
DR [dB]	115.6	113	-	103	116
Idle state Power Consumption [mW]	2.14	1.23	2.05	7.6	-
Modulation Scheme	ΔΣ-PWM (Digital In.)	ΔΣ (Digital In.)	PWM (Analog In.)	PWM (Digital In.)	PWM (Digital In.)

Table 5.1: Performance Summary of Class-D amplifiers [17][8][4][5]

5.1 Future Work

Although the targeted performances are achieved with a relatively low idle power consumption, there are multiple potential improvements possible:

- As mentioned in Section 2.3.2, the jitter performance of the main clock degrades the linearity of the CDA. The low-resolution DAC is intrinsically more linear than a multi-bit DAC but shows worse jitter performances due to larger step sizes. A fast, multi-bit current steering DAC could be studied to decrease the sensitivity of the CDA to clock jitter.

- As shown in Figure 4.8, one of idle-state power consumption's main limitations is the loop filter's first OTA. The assisting DAC technique was introduced to decrease its power consumption. However, due to the class A output stage of the OTA, a relatively high biasing current in the output stage is needed to keep the OTA stable. An OTA with a class AB output stage could be designed to decrease the quiescent output current.

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