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Millimeter-Wave On-Wafer TRL Calibration Employing 3-D EM Simulation-Based Characteristic Impedance Extraction

Luca Galatro, *Student Member, IEEE*, and Marco Spirito, *Member, IEEE*

***Abstract*— In this paper, we propose a method based on 3-D electromagnetic simulations, for the characteristic impedance extraction of transmission lines employed in TRL calibration, focusing on lines integrated in silicon technologies. The accuracy achieved with TRL calibrations using the proposed characteristic impedance extraction is benchmarked versus conventional approaches, with an emphasis on aluminum pads structures operating in the (sub) millimeter-wave range. The proposed method proves to be insensitive to common sources of error (i.e., large pad capacitance and inductive pad-to-line transitions), which affect the accuracy of characteristic impedance extraction based on measurements, especially as the testing frequency increases. First, direct on-wafer TRL calibrations are performed on uniform CPWs (i.e., with no pads discontinuities) to demonstrate how the proposed method performs as good as the calibration comparison method and outperforms calibration transfer approaches. Finally, the method is applied to a nonuniform CPW-based calibration kit, demonstrating how the proposed method provides accurate results, improving the calibration quality that can be achieved using the calibration comparison method when inductive pad-to-line transitions are present.**

***Index Terms*— Calibration, characteristic impedance, measurement, millimeter wave, silicon, TRL, vector network analyzer.**

I. Introduction

THE continuous up-scaling of the maximum device operation frequency is pushing the development of millimeter-wave circuits to real-life applications [1], [2]. In order to foster the device improvements and push millimeter-wave applications in the commercial world, the availability of accurate measurement techniques, for low-cost large-volume technology platforms, is becoming a key requirement. Every high-frequency measurement from passive to active device characterization, from noise to large signal parameters extraction, requires the support of accurate on-wafer S-parameter calibrations.

Calibration techniques for on-wafer measurements typically consist of a *probe-level* calibration (first-tier) performed on a low-loss substrate (i.e., alumina or fused silica) [3]–[6]. This probe-level calibration is then transferred to the environment where the DUT is embedded in and often, to increase the measurement accuracy, this calibration is augmented with a second-tier *on-wafer* calibration. This allows moving the reference plane as close as possible to the DUT, by de-embedding the parasitics associated with the contact pads and the device-access vias [7]. The process of transferring the first-tier calibration to another structure assumes that the delta capacitance introduced by changing the substrate under the probes (i.e., boundary conditions) is negligible. As it was shown in [8], this capacitance is dependent on the probe topology and substrate characteristic, creating a coupling that increases with frequencies.

To remove the errors arising from neglecting or improperly removing this delta capacitance, the calibration kit should be implemented in the same environment of the DUT.

Classical probe-level and on-wafer calibration techniques are based on (partially) known devices and lumped models of the DUT fixture (i.e., SOLT/LRM and lumped de-embedding) or employ distributed concepts (TLR and multiline TRL). Due to the objective difficulty, especially at higher frequencies, in manufacturing an accurate and predictable resistor in a commercial silicon technology (multiline)-TRL calibration represents the standard employed technique, as was shown in [9]–[13]. The TRL technique does not require resistors to define the measurement normalization impedance, which is instead set by the characteristic impedance of the lines used during the calibration. Thus, the accurate (frequency dependent) determination of the calibration lines characteristic impedance becomes a key requirement to allow the correct renormalization of TRL-calibrated S-parameter measurements.

When transmission lines are fabricated over well-characterized homogenous materials and both radiation losses and surface waves can be neglected (i.e., lower millimeter-wave frequencies), the line characteristic impedance can be derived by means of quasi-static approaches, typically based on conformal mapping [14]–[16]. However, when the structure geometry and the host substrate become more complex [i.e., silicon integrated grounded CPW (CPWG)], these approaches become less accurate. To overcome these limitations, various techniques have been developed to experimentally determine the characteristic impedance of these lines [17]–[22].

In [17], the characteristic impedance (Z_0) of a transmission line was extracted versus frequency from calibrated

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S-parameter measurements applying (1), where Z_{sys} is the system reference impedance (typically set to 50 Ω)

$$Z_0 = Z_{sys}\sqrt{\frac{(1+S_{11})^2 - S_{21}^2}{(1-S_{11})^2 - S_{21}^2}}. \quad (1)$$

Equation (1) is derived equating the scattering parameters of the measured line to that of a transmission line section, with no input–output reflections. For this reason, (1) is only applicable when measuring uniform lines. Moreover, the equation provides a discontinuity at half wavelength. This approach does not account for the nonideal probe-to-pad transition and the contact-pad capacitance, making the expression in (1) only an estimate of the characteristic impedance of the line.

The method proposed in [18] allows the extraction of the characteristic impedance from the propagation constant measured during the TRL calibration and an estimate of the capacitance per unit length of the line. This capacitance is approximated to the dc-capacitance per unit length, in the assumption of low loss substrates, weak transverse currents in the conductors and constant value versus frequency. These assumptions are often violated at very high frequencies and when employing lossy substrates. In [19], the estimate of the capacitance per unit length is obtained from the dc-resistance per unit length of the line. This approach often leads to large inaccuracies, due to contact repeatability, when considering silicon technologies with aluminum pads. Also in [19], an estimate of the characteristic impedance of the line is computed from the reflection coefficient of a small resistive load, in the assumption that the load is real, constant and equal to its dc resistance, conditions very difficult to reproduce in complex technologies, as the frequency increases. The above-mentioned problems were overcome in the calibration comparison method for Z_0 extraction proposed in [20] and [21]. In [21], the reference impedance of a TRL calibration (i.e., Z_0 of the line) is extracted from the error boxes computed during the calibration and related to a primary (probe-level) calibration, with fixed and known reference impedance. In [22], the method was improved via a lumped model of the probe to line transition, making the calibration comparison also insensitive to large shunt capacitances, typically associated with contact pads. Nevertheless, the calibration comparison method remains limited to noninductive pads-to-line transition [23] and requires the availability of a well-defined calibration substrate at the frequency of interest where the probe-level calibration is performed.

In this paper, we propose a characteristic impedance extraction procedure based on 3-D electromagnetic (EM) simulations. The proposed method is developed to reach comparable accuracy to the calibration comparison method in [22], without requiring the extra calibration substrate, and overcomes its limitation in case of inductive pads-to-line transitions. This paper is structured as follows. In Section II, the challenges associated with the calibration comparison method at millimeter-wave are analyzed, and examples are reported for special cases in which the method in [22] fails to accurately predict the characteristic impedance of transmission lines. In Section III, the realization of a TRL calibration kit developed on a BiCMOS SiGe technology back end of line (BEOL) is described, and in Section IV, the procedure for characteristic impedance extraction based upon 3-D EM simulation is explained. The accuracy of the extraction procedure is validated on the BiCMOS-based TRL kit in Section V, using the calibration comparison method as benchmark. Finally, in Section VI, the proposed method is applied to a TRL calibration kit developed on a different SiGe BiCMOS technology, where inductive pads-to-line transitions are present.

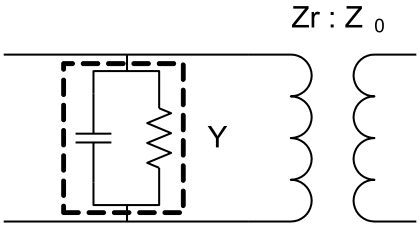

Fig. 1. Equivalent circuit model for the pad-to-line transition as employed in [22].

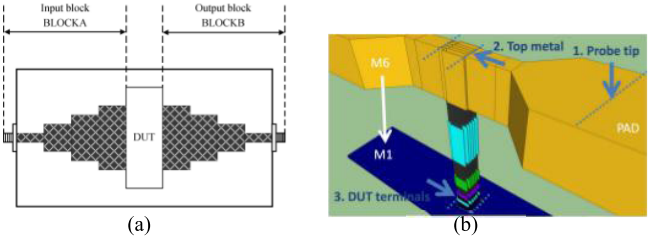

Fig. 2. (a) Test fixture for high power transistor characterization taken from [24]. (b) Zoomed-in view of the vias interconnection for a commercial SiGe technology modeled in a 3-D EM environment, taken from [25].

II. Calibration Comparison Method at Millimeter Wave

The calibration comparison method, in the formulation in [22], accounts for a discontinuity in the transition from contact pads to line, which can be modeled as shunt admittance (Y) with a capacitive susceptance, representing the contact pad, and an impedance transformer, as shown in Fig. 1.

However, the method in [22] loses accuracy when a series inductance or in general a nonlumped transformation is present between the shunt admittance Y and the impedance transformer. These situations can occur when an inductive pad to line transition is considered, as described in [23], or when the TRL kit is embedded in a more complex fixture where impedance tapers [Fig. 2(a)] or complex vias interconnects are employed [Fig. 2(b)].

When considering a commercial integrated technology BEOL (see Fig. 3), the maximum distance between the signal (i.e., top metal line) and the ground (i.e., meshed M1 and M2) line of a microstrip of a CPWG is usually limited to $\sim$10 μm.

This technology restriction translates in the requirement to have narrow linewidths in the fixture embedding the DUT to achieve inductive line sections, i.e., to reduce the large VSWR (partially canceling its input capacitance) of modern ultrascaled technologies [26]. The resulting step change in the width of the coplanar line connecting the DUT can be modeled as a series reactance and can be placed at the plane of the

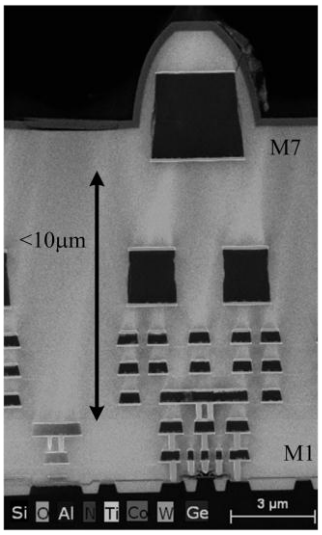

Fig. 3. TEM image of the BEOL of the IHP SG13G2 130 nm SiGe BiCMOS technology.

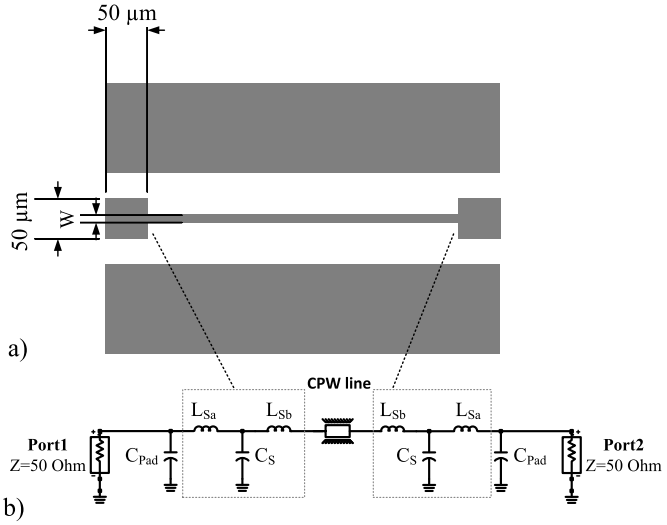

Fig. 4. CPW line used for calibration comparison simulation with $\varepsilon_r = 12.9$, substrate thickness 350 μm and fixed ground distance equal to 150 μm. (a) Top view of the thru, with dimensions. (b) Simulation setup for the thru employing a single shunt capacitance for modeling the pad, and the lumped model introduced in [27] for the pad-to-line transition.

line discontinuity [27]. To propagate the error arising from the presence of a series reactance on the extraction of the characteristic impedance using the method in [22], we applied the calibration comparison method to a set of CPW lines, presenting a varying step in the pad-to-linewidth, using the Keysight ADS simulation environment. The step discontinuity was computed using the model proposed in [27]. The probe pad is considered as a square pad with a 50×50 μm^2 area and is included in the model using a shunt capacitance (simple parallel plate capacitance computation) of 18 fF, as shown in Fig. 4, while the line section is varied from a width of 7.5 μm (W in Fig. 4) to the size of the pad (i.e., no discontinuity). All the lines are included using the frequency-domain analytical model for the coplanar waveguide available in ADS developed by Getsinger and based on conformal mapping techniques.

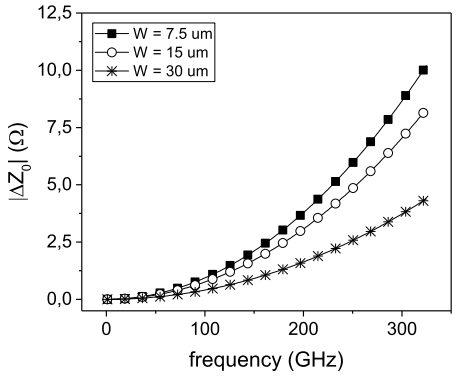

Fig. 5. Difference between the actual characteristic impedance and the one computed applying [22] to the transmission lines modeled in Fig. 4, for different values of linewidth W. The discrepancy increases with increase in the width step between the pad and the line.

All the lines use the same (lossless) substrate model (i.e., *ADS CPWSUB*) employing the values as used in [27], with a substrate thickness of 350 μm and a dielectric constant $\varepsilon_r = 12.9$. The set of lines was simulated using a reference impedance of 50 Ω and the TRL equations applied in order to extract the characteristic impedance of the central line section using the method in [22] (Fig. 4). The results shown in Fig. 5 demonstrate how the computation of the characteristic impedance obtained using the calibration comparison method diverges from the correct characteristic impedance value in the presence of a large step discontinuity. The discrepancy reduces with the reduction of step discontinuity, becoming negligible for uniform lines or lower frequencies (where the inductive contribution is also negligible). Thus, it can be stated that the calibration comparison method represents the reference method only for uniform CPW lines, while proving to be less accurate when applied to nonuniform structures, i.e., when inductive pad-to-line transitions are present. For this reason, the method in [22] will be used as the benchmark method for the method proposed in Section V, where both methods will be applied to a uniform CPW-based calibration kit.

III. On-Wafer Calibration Kit

To compare the accuracy achieved between the characteristic impedance extraction of conventional methods and the proposed one (described in Section IV), we designed and fabricated a TRL calibration kit using the BEOL of the IHP 130 nm SiGe BiCMOS process (see Fig. 3). Uniform CPWG lines have been considered to allow direct comparison with probe-level calibrations (i.e., transferred) and with the calibration comparison method, thus removing the error arising from width discontinuities between lines and pads (see Section II). The fabricated chip microphotograph of the TRL kit is shown in Fig. 6(a)–(c) (i.e., thru, reflect, and line, respectively). The lines are implemented as CPWG, to reduce losses in the (semi) conductive substrate. All the structures employ aluminum pads, i.e., signal pad 30×50 μm^2 and larger ground pads to allow different probe pitches to be used on the same structure (i.e., 75 and 100 μm). The thru line is a 200 μm long uniform coplanar waveguide [Fig. 6(a)]. The calibration kit reflects are realized by two symmetric offset shorts [Fig. 6(b)], with an

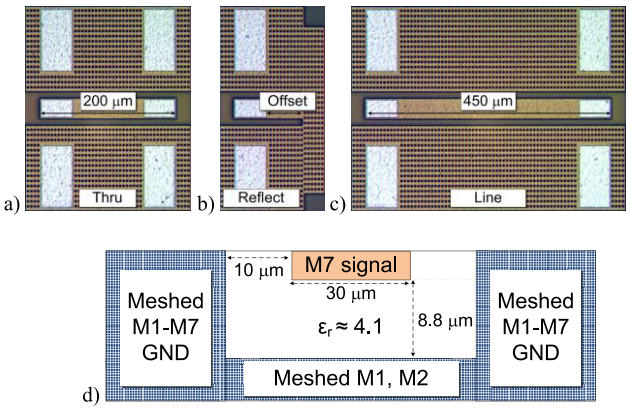

Fig. 6. CPW calibration artifact realized on IHP SiGe 130 nm BiCMOS technology. Microphotograph of (a) thru line, (b) reflect standard, and (c) transmission line employed for the WR05 calibration kit. (d) Cross section sketch of the CPW line.

offset equal to half the thru length. This minimizes the distance between the center of the thru and the location of the short, allowing to fix the sign of the square root solution in the TRL calibration [5] (i.e., +/− open/short) for the entire calibration band. Note that when an electrical length of $\lambda/8$ is present, the sign needs to be changed to enforce phase continuity. Three transmission lines with lengths of 360, 450, and 680 μm are fabricated to allow single line TRL calibration in the WR3, WR5, and WR10 waveguide bands, respectively. Finally a 600 μm long CPWG is used for calibration verification. The first two metal layers of the BEOL (Fig. 3) have been used to realize a meshed ground plane satisfying the metal density rules. The bottom ground plane is electrically connected to the coplanar ground planes using interleaved meshed metal on all layers and employing the maximum via density allowed. The CPW line is 30 μm wide and 3 μm thick with a 10 μm gap [Fig. 6(d)]. The silicon dioxide acting as a dielectric has a relative permittivity of ca. 4.1, almost homogenously among the entire structure, allowing simple simulation geometry.

IV. EM Simulation Setup

The structures were simulated using three different 3-D EM simulators, Keysight EMPro, Ansoft HFSS, and CST Studio Suite, to check for simulation discrepancies. In the model, the meshed ground planes have been simplified considering a continuous metal connection, both vertically and horizontally. This simplification provides good approximation of the electrical response of the structure being the openings in the metal mesh much smaller than the wavelength (maximum aperture is in the order of 2.5 × 2.5 μm^2), and the openings interleaved among different metal levels. The excitation to the CPW lines is provided by means of waveguide (modal) ports. The simulator first solves a 2-D eigenvalue problem to find the waveguide modes of this port and then matches the fields on the port to the propagation mode pattern, and computes the generalized (i.e., mode matched) scattering parameters. In all the simulators, the port dimensions are designed using the rules of thumb described in [28], ensuring ideally no fields at port boundaries, as also depicted in Fig. 7 for two simulator examples. The use of lumped ports was not taken into account

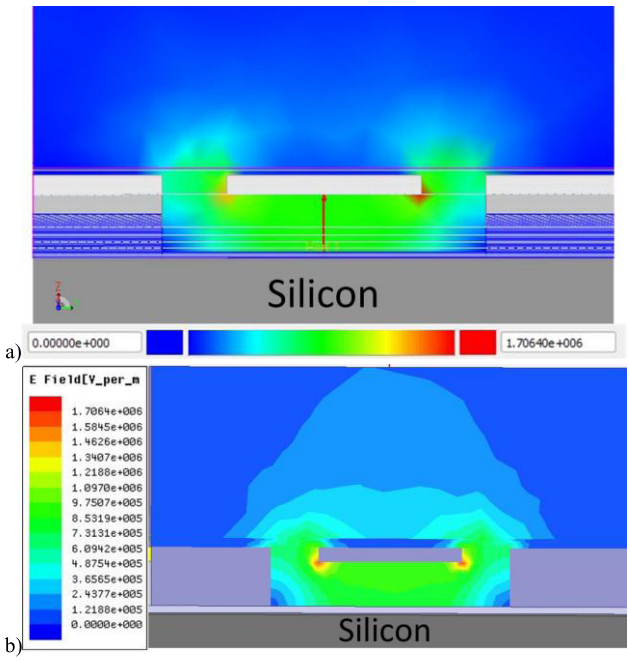

Fig. 7. Field distribution on waveguide ports at 300 GHz when exciting the structures described in Section III for (a) Keysight EMPro and (b) Ansoft HFSS.

in this paper, due to the additional parasitics effect introduced (i.e., bridge topology) that would affect the computation of the characteristic impedance, as it is described in Section V.

Absorbing/radiation boundaries are then imposed at the lateral and top faces of the simulation box. The box is defined horizontally by the dimensions (length/width) of the simulated structure, and vertically by the wavelength ($\lambda/4$ at minimum simulation frequency). The bottom face of the simulation box is defined as a perfect electric conductor, simulating the presence of a metallic chuck underneath the structure, as it is the case during measurements. The absorbing boundaries simulate an unperturbed propagation of the EM waves through this boundary. In this respect, the interference with other structures on the wafer is not taken into account in the simulation. Material parameters and lateral dimension are chosen according to the nominal technology values. The influence of the technology fluctuations on both material properties and geometry on the accuracy of the characteristic impedance computation is discussed in Section V.

V. EM-Based Z_0 Computation

A. Z_0 Extraction Procedure

The scattering parameters calculated during simulation are renormalized to a given system value (i.e., 50 Ω) and used in (1) to compute the line characteristic impedance. The use of waveguide ports during the simulations allows the minimization of the discontinuities between the simulation port and the line. It is important to note that these discontinuities, as shown in [21], contribute to the error in the estimate of Z_0, which is maximum as the line lengths approach half a wavelength. When the half a wavelength condition is reached [$\tan(\beta l) = 0$] within the calibration band, large errors in the Z_0 estimate will

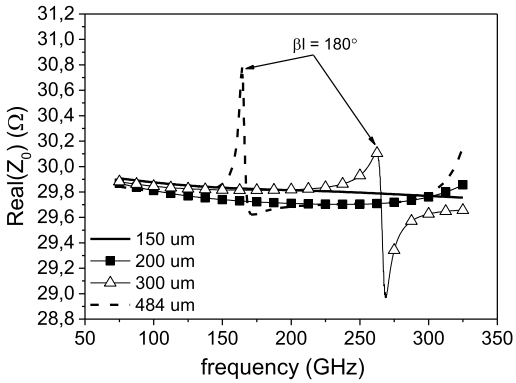

Fig. 8. Comparison of the real part of the characteristic impedance for the considered structures computed using (1) on simulated S-parameters of lines with different lengths,150, 200, 300, and 484 μm versus frequency.

occur. When the half a wavelength condition is kept outside the required frequency band, the differences of Z_0 estimate between lines (i.e., 200 and 150 μm) are smaller than 0.3%.

Similar errors can be seen in the estimate of the imaginary part of Z_0 versus the electrical length of the line. Note that the use of the simulation environment allows the use of line lengths below the minimum advised in experimental characterization (i.e., 150 μm), limited by the probe-to-probe crosstalk, thus allowing an accurate estimate of Z_0 in the entire (sub) millimeter-waveband. A 150 μm line has been used to extract the characteristic impedance in this paper.

To benchmark the proposed EM extraction approach, the characteristic impedance of the line shown in Fig. 6(a) was also extracted, from measured data, with the methods proposed in [17] and [22]. For both experimental extraction procedures, a probe-level (TRL) calibration performed on a fused silica substrate was employed as a first-tier calibration.

In Fig. 9, the characteristic impedance computed with the three methods is compared. As can be seen by the plot, the method in [17], as predicted from [21], is hampered by the discontinuities due to the probe to pad transition.

The impedance extracted using the method in [22] presents some fluctuations, which can be attributed to the inductive nature of the probe to pad transition (i.e., step in transmission linewidth). Moreover, both the mentioned techniques suffer from the errors arising from the calibration transfer from the fused silica substrate as described in [8]. It is interesting to notice from Fig. 9 how simulations performed with different tools produce slightly different values for the characteristic impedance. As a matter of fact, the three computations differ up to a maximum of 1 Ω for the real part and 0.1 Ω for the imaginary part, for the same structure when applying similar settings in terms of meshing and solving methods. This can be considered as an intrinsic uncertainty of the proposed method, since different simulation tools would not converge to exactly equal results. However, as highlighted in Fig. 9, the discrepancy between the simulators is still much smaller than the fluctuations in the characteristic impedance computed with the methods in [17] and [22]. For the rest of this paper, only the simulations obtained with Keysight EMPro will be employed.

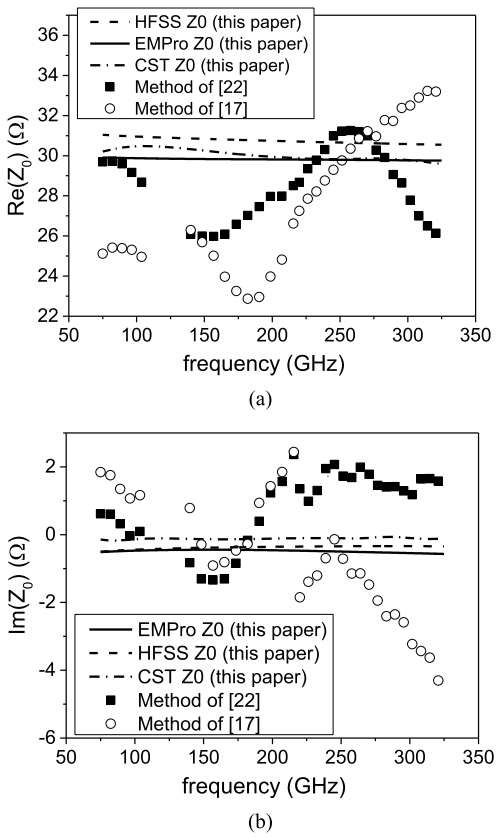

Fig. 9. (a) Real and (b) imaginary parts of characteristic impedance for the line shown in Fig. 6(a), computed by the simulation approach described in Section V (solid lines: EMPro, dashed lines: HFSS, dashed-dotted lines: CST), measured with the method in [17] (empty circles) and measured with the method in [22] (filled squares).

B. Simulation Uncertainties

The accuracy of simulation-based methods (both analytical as well as numerical) relies totally on the accuracy of the model, i.e., completeness of dominant phenomenon and uncertainty/variation on the material parameters. Modern numerical simulation tools are capable of including all the EM effects and parameters associated with transmission line propagation. With respect to the main parameters that can influence the characteristic impedance are the linewidth variations, the interlayer dielectric thickness spread, and the dielectric coefficient uncertainty. In order to investigate the impact of these parameters on the characteristic impedance extraction, simulations have been performed using data provided in the IHP 130 nm SiGe BiCMOS process specifications manual.

Results are shown in Fig. 10, where the variations associated with linewidth have been neglected, being the tolerance in the order of 300 nm (i.e., 1%). The variations on Z_0 are dominated by the dielectric thickness and dielectric constant uncertainty. Using the process variation reported in the manual, the 99% confidence interval results in a range of $\pm$7% with respect to the nominal case (see Fig. 10). The impact of these fluctuations on the calibration error will be discussed in Section VI.

VI. Comparison of Probe Tip Calibrations

In order to validate the method proposed in Section IV, we compared different calibration substrates and strategies applied

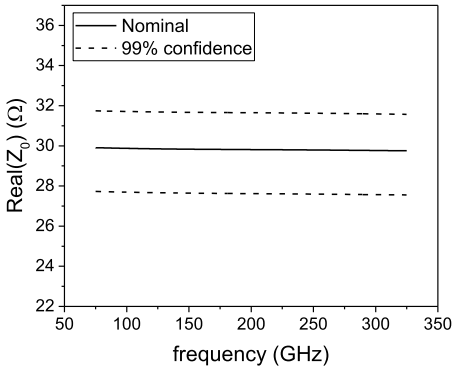

Fig. 10. Characteristic impedance variation associated with technology tolerances for the transmission lines described in Section III, using the same scale of Fig. 9(a).

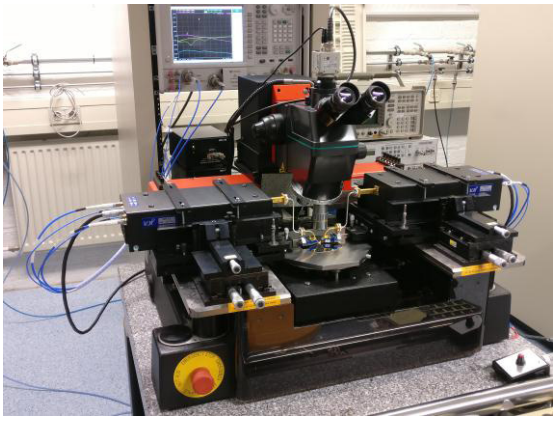

Fig. 11. Measurement setup employed for the comparison of probe tip calibrations in the WR-5 waveguide bandwidth.

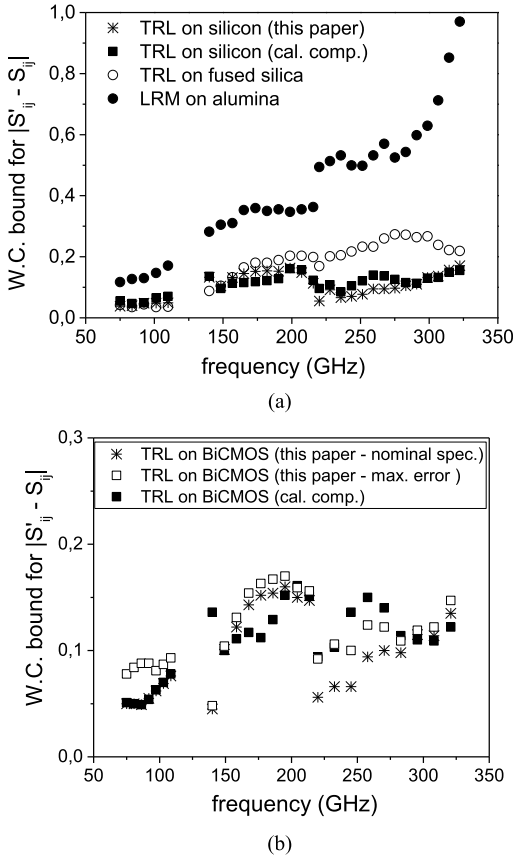

Fig. 12. (a) Comparison of probe-tips corrected measurements of a verification line manufactured on the SiGe BEOL in the frequency range 75–325 GHz for different calibrations. (b) Detail of calibration comparison, with error associated to technology tolerance in the Z_0 extraction (empty squares).

to the measurement of a CPW line. The line is embedded in the technology described in Fig. 3 and the measurements are carried out for three different waveguide bands, i.e., WR-10 (75–110 GHz), WR-5 (140–220 GHz), and WR-3 (220–325 GHz), using simulation data of the reference line for verification.

The measurements have been carried out on a precision semiautomatic probe-station in order to have constant contact force and minimize the probe landing misplacement among the measurements of different structures (see Fig. 11). Three different calibration kits have been employed, an ISS LRM calkit on alumina substrate (i.e., W-band 104–783), a TRL calkit designed on fused silica as described in [29], and the TRL calkit on SiGe BiCMOS BEOL described in Section II. In order to allow a proper comparison, the calibration planes of the on-wafer (i.e., BiCMOS) calibration have been shifted back to the probe-tips using the propagation constant computed by the TRL algorithm. For the BiCMOS calkit, two cases are considered, one in which the characteristic impedance is extracted with the method in [22], where a probe tip calibration on fused silica is considered as reference, and one in which the characteristic impedance is computed *a priori* with the method described in Section V.

In order to compare the different calibrations, the method in [30] has been employed, defining an upper bound (UB) error metric as

$$\mathrm{UB}(f) = \max \left| S'_{ij}(f) - S_{ij}(f) \right| \tag{2}$$

where S' is the reference scattering matrix of the verification line (i.e., 3-D simulated S-parameters), *S(f)* is the frequency-dependent scattering matrix resulting from the investigated calibrations (i.e., LRM on alumina, TRL on fused silica, and TRL on BiCMOS) and $i, j \in [1, 2]$. This metric defines the UB of the deviation of the S-parameters measured by one calibration and the reference S-parameters computed using EM simulations. The measurement data used to compute the error bound of Fig. 11 are based on the same raw data of the verification line, thus removing any measurement variation of the verification artifact from the error propagation mechanisms. On these raw data the respective calibration algorithm (with the previously computed error terms) was applied. In addition, both the methods indicated as TRL on silicon in Fig. 11, use also the same raw measurement in the calibration procedure (i.e., extraction of error terms), thus confining their difference only to the characteristic impedance values versus frequency, computed with the two different methods.

Fig. 12 shows the results of the measurement comparison, where the UB of the error is plotted versus frequency for all the considered calibrations. The LRM calibration on alumina

substrate (filled circles in Fig. 12) performs worse than all the other approaches in the entire frequency band, with a deviation from simulations that increase with frequency. The reasons for this behavior can be associated with the nonidealities in the definition of the "match" standard in the calibration kit, which increase their effect for increasing frequency. Moreover, the onset of spurious modes on "electrically thick" substrates like the alumina ISS ($\varepsilon_r = 9.6$, thickness $= 254$ μm) can affect the accuracy of the calibration, intrinsically based on single mode propagation, as described in [29]. Finally, with the frequency increase toward the (sub) millimeter-wave region, the effect of the probe to substrate coupling in the transfer of calibration among different calkits (i.e., difference in ε_r) can become an important contribution to the calibration error, as described in [8].

TRL on fused silica performed sensibly better than the LRM on alumina (see Fig. 12, empty circles) with the value of the error bound always lower than 0.25 in the entire frequency band. Also in this case, however, the deviation from simulation increases with frequency, as the effect of the delta capacitance associated with the calibration transfer becomes more relevant. The calibration performed on SiGe technology is the one that presents smaller deviation from the reference data, with a UB < 0.17 in the entire frequency band for both characteristic impedance extraction method considered, i.e., the proposed EM-based method (Fig. 12, asterisks) and the calibration comparison method (Fig. 12, filled squares). The two BiCMOS calibrations show good agreement with the reference data and track each other well, demonstrating how even discrepancies in the Z_0 extraction up to 10% (3 Ω), for both real and imaginary parts, result in S-parameter errors smaller than the other sources of error associated with the calibration (e.g., asymmetric probe misplacement, contact resistance fluctuations, and contact force repeatability). For the same reason, errors on simulation extracted associated with process tolerances, as described in Section V-B, have a very small impact on the overall error, as shown in Fig. 12(b), especially at higher frequencies where other sources of error tend to dominate. It is important to mention that repeated measurements over different devices on the BiCMOS calibration kit in the highest frequency band (i.e., WR-3) show a measurement repeatability defined by a maximum standard deviation $\sigma = 0.033$. This value is always below the minimum value of the UB metric shown in Fig. 12, which is in the order of 0.05.

VII. Application to CPWs With Inductive Transitions

In Section V, the proposed method for characteristic impedance extraction based on EM simulations was shown to achieve similar level of accuracy as the calibration comparison method when considering transmission lines with homogenous geometry, i.e., no discontinuity in the line geometry between the landing pad and the intrinsic line. When considering lines with more complex transitions, however, the calibration comparison provides lower accuracy due to the unaccounted series reactance as explained in Section II. In order to demonstrate the improvement provided by the proposed method,

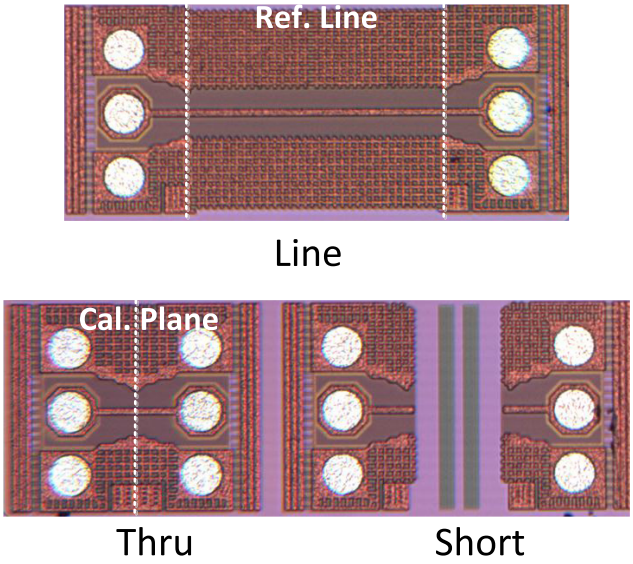

Fig. 13. TRL de-embedding kit manufactured on NXP QubiC4XI 0.25 μm BiCMOS SiGe.

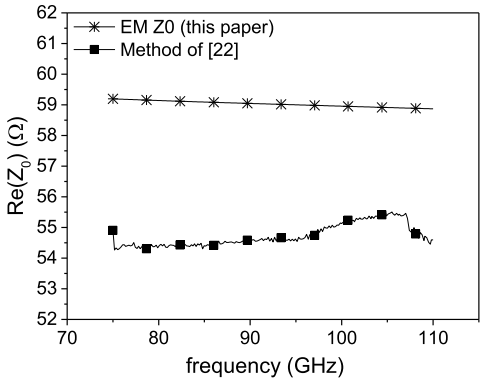

Fig. 14. Real part of the characteristic impedance for the Qubic4XI intrinsic transmission line extracted with the method described in Section III (solid line—asterisks) and the calibration comparison method in [22] (solid line—full squares).

we consider a TRL de-embedding kit manufactured on NXP QubiC4XI 0.25 μm BiCMOS SiGe, employing nonuniform lines. The structures composing this de-embedding kit present large GSG landing pads, with 50 μm diameter. The signal pad is directly connected to a microstrip having a width of 10.5 μm, creating an inductive series transition between the landing pads and the line. The TRL kit features a 162 μm thru, a pair of short standards and a line of additional 662 μm length (see Fig. 13).

This BiCMOS kit has been used to perform a TRL calibration in the frequency range from 75 to 110 GHz, where the employed characteristic impedance has been extracted using EM simulations of the intrinsic transmission line and compared with the Z_0 computed using the calibration comparison method in [22].

Fig. 14 shows the real part of the characteristic impedance as computed with both methods. The characteristic impedance computed with the calibration comparison method shows deviations from simulation (up to 5 Ω for the real part) and a lower value, consistent with the presence of an inductance in series with the pad, as described in [23]. These deviations

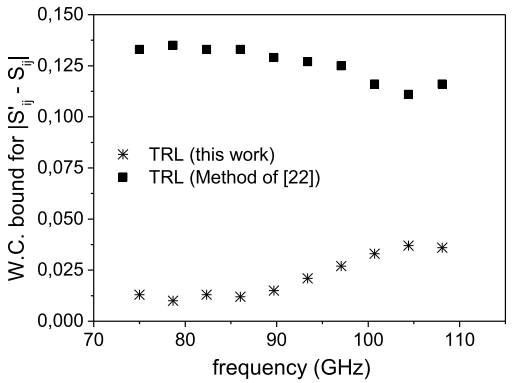

Fig. 15. Comparison of TRL calibrations performed on the calkit shown in Fig. 8 when employing the characteristic impedance extracted with the calibration comparison method of (full squares) and the simulation based method extracted in this paper (asterisks).

directly affect the measurements, as shown in Fig. 15, where the UB of the error as defined in (2) is displayed for both considered methods, using the EM simulated data as the reference values. The results show how the errors in the characteristic impedance extraction, when using the calibration comparison technique, dominate the S-parameter measurements in respect to all other sources of error. This is highlighted by a value of UB up to one order of magnitude higher than the one achieved using the proposed method.

VIII. Conclusion

In this paper, we presented an alternative method for the extraction of the characteristic impedance of transmission lines employed in TRL calibrations. The method is based on an *a priori* computation of the characteristic impedance derived from full wave 3-D EM simulations of the transmission line. We have shown how employing mode matched ports with an adequate length (well below $\lambda/4$) minimizes the errors due to port discontinuities, thus resulting in an accurate estimate of the line characteristic impedance using an equation that only requires the knowledge of the line's S-parameters. The proposed extraction method is immune to pad-to-line discontinuities since it focuses on the intrinsic line properties and is scalable to the entire (sub) millimeter-wave bands and does not require a well characterizes calibration substrate operating in the same frequency band. Comparison of the proposed method with the state-of-the-art calibration approaches was carried out on uniform CPWG lines manufacture in the BEOL of a SiGe BiCMOS technology. Measurement results highlight how the proposed method offers accurate values for the computed characteristic impedance when compared with the calibration comparison method and significantly outperforms probe-level calibration realized on different substrates. Finally, the advantage of the proposed method, i.e., total insensitivity to capacitive or inductive pad-to-line transitions, is demonstrated on a TRL kit with pad-to-linewidth step. Here the proposed method achieves a UB bound more than five times smaller than what is achieved with conventional calibration techniques.

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