# Location-Controlled Large Si Islands by ELA on Glass Substrate

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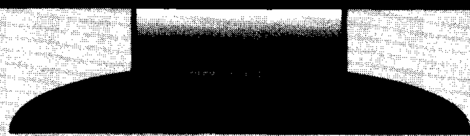
Artyom Burtsev



TR 41175

# Stellingen

behorende bij het proefschrift

## Location-Controlled Large Si Islands By Excimer-Laser Annealing On Glass Substrate

door

Artyom Burtsev

Delft, 20 oktober 2003

1. New types of displays with an active-matrix addressing scheme, such as Organic Light-Emitting Diode (OLED) displays, can benefit from the utilization of c-Si TFTs.
2. The phase-field model can beneficially be applied to simulate the crystal growth of crystallized Si thin films and to predict the resulting size of the c-Si islands (this thesis, chapter IV).
3. ELA NIC Si films can successfully be used with the DBTOP method for the preparation of location-controlled c-Si islands with a uniform crystallographic orientation (this thesis, chapter VI).
4. Due to the inherent limitations of plasma displays (i.e., problems with a full white to dark color ramp, burn-in and burn-out of phosphor), displays on the wall will be based on TFT LCD monitors rather than on plasma monitors.
5. Electronic ink will permit almost any surface to become a display, introducing a new Display On Anything (DOA) technology.
6. If certain power supply companies would use all energy, spent on double billing of their customers and subsequent correction of their mistakes, to improve their technological infrastructure, the reliability of electric networks would rise to inconceivable heights.
7. The rapid increase in popularity of the KGB-invented RU-21 pill among the Western people can lead to unexpected harmful effects. Typical Western consumers tend to forget that this pill is not only an excellent hangover remedy, but also encourages drinking without consequences leading to a stronger alcohol dependence.
8. The Schengen agreement is just as effective to keep people 'outside' as the Iron Curtain was to keep people 'inside'. It makes no difference for the people involved.
9. By developing a strict license and visa policy, countries tend to limit their own development.
10. Everybody knows smoking is lethal. Nevertheless, smokers have a superior developed inhale technique with strong and deep inhales, something that comes in handy during later use of an inhalator or during reanimation.
11. White Russians are the only real Russians.

***These propositions are considered defendable and as such have been approved by the promotor prof. dr. C.I.M. Beenakker.***

1. Nieuwe beeldschermtypen met een actieve-matrixaansturing, zoals de Organische Lichtgevende Diodes (OLED's), kunnen profiteren van het gebruik van c-Si TFTs.
2. Het faseveldmodel kan met goed resultaat worden toegepast om de kristalgroei in gekristalliseerde dunne Si films te simuleren en de resulterende grootte van de c-Si eilanden te voorspellen (hoofdstuk IV van dit proefschrift).
3. ELA NIC Si films kunnen met succes worden gebruikt met de DBTOP methode voor het verkrijgen van plaats-gecontroleerde eilanden van c-Si met een uniforme kristallografische oriëntatie (hoofdstuk VI van dit proefschrift).
4. Wegens de inherente beperkingen van plasmaschermen (d.w.z. de problemen met de overgang van een volledig witte naar een volledig zwarte weergave, inbranden en doorbranden van het fosfor), zullen schermen aan de muur op TFT-LCD monitors worden gebaseerd in plaats van op plasma monitors.
5. Elektronische inkt zal het mogelijk maken om bijna elk oppervlak als monitor te gaan gebruiken, waarmee de Display On Anything (DOA) technologie is geintroduceerd.
6. Als alle "in"spanning die sommige energiebedrijven genereren tijdens het dubbel factureren van hun klanten zou worden gestoken in het verbeteren van hun hoogspanningsnet zou de betrouwbaarheid van dit netwerk tot ongekende hoogte stijgen.
7. De groeiende populariteit van de door de KGB ontwikkelde RU-21 pil onder Westerlingen kan leiden tot onverwachte schadelijke effecten. Typische Westerse consumenten neigen te vergeten dat de pil niet alleen prima een kater kan voorkomen, maar ook het drinken van alcohol bevordert, zodat men sneller verslaafd raakt aan de alcohol.
8. De Schengen overeenkomst is net zo effectief om mensen "buiten" te houden als het Ijzeren Gordijn was om mensen "binnen" te houden. Voor de burger, die ermee te maken heeft, is er geen verschil.
9. Door een streng visum en vergunningen systeem beperken landen hun eigen ontwikkeling.
10. Iedereen weet dat roken dodelijk is. Echter, een roker bezit reeds een goede inhalatietechniek met betrekking tot krachtig en diep inhaleren, iets wat goed van pas komt bij het latere gebruik van een inhalator of tijdens de mond-op-mond beademing.
11. Echte Russen zijn Witrussen.

***Deze stellingen worden verdedigbaar geacht en zijn als zodanig goedgekeurd door de promotor prof. dr. C.I.M. Beenakker.***

TR 4117

# *Location-Controlled Large Si Islands By Excimer-Laser Annealing On Glass Substrate*

Artyom Burtsev

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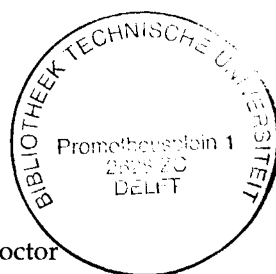

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DELFT


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op gezag van de Rector Magnificus prof. dr. ir. J. T. Fokkema,
voorzitter van het College voor Promoties,
in het openbaar te verdedigen op maandag 20 oktober 2003 om 10.30 uur

door


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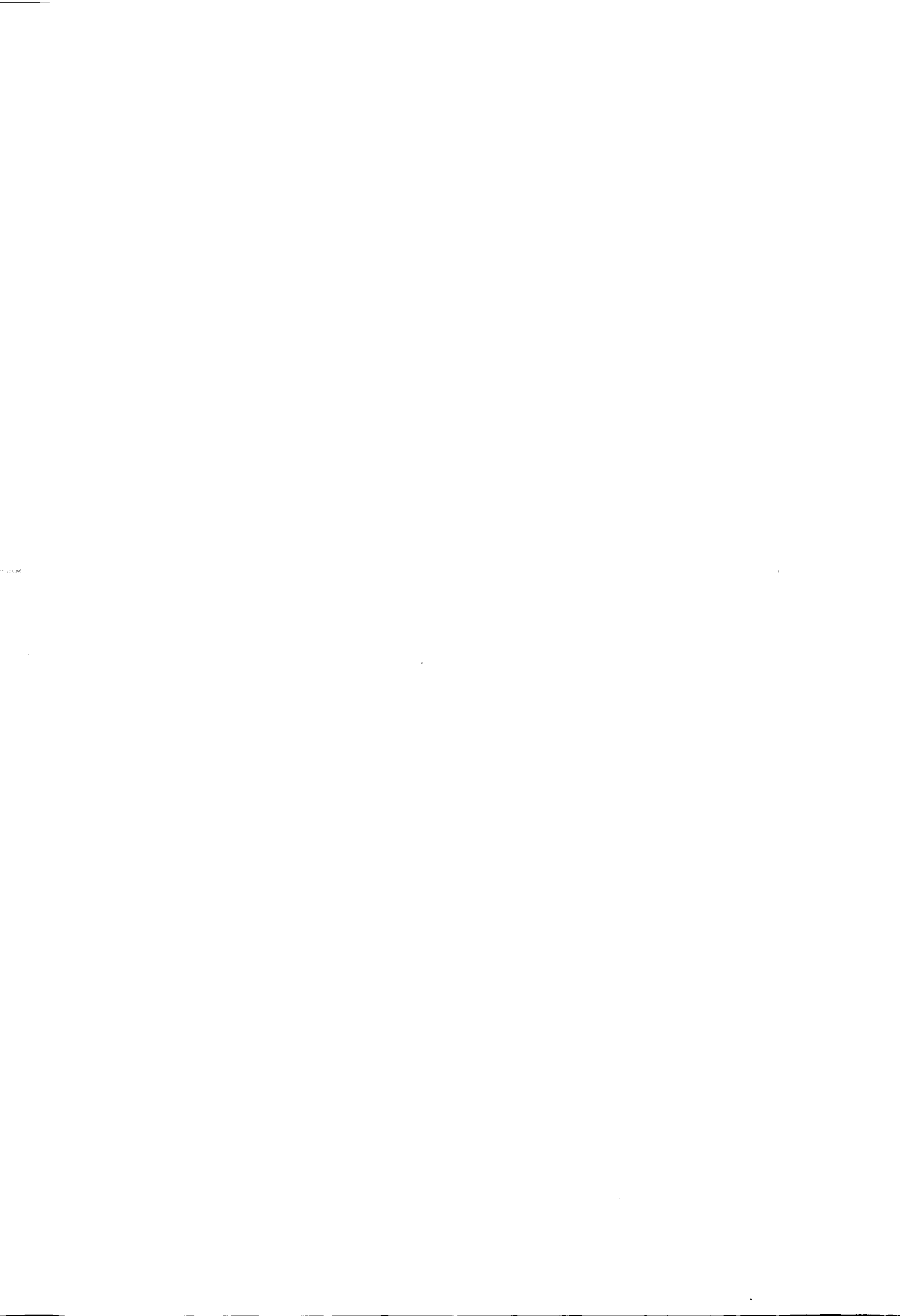
**To my dear parents,
friends, and kleintje**



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# Chapter 1

# Introduction

## 1.1 Preface

Modern science and technology have become increasingly based on the application of thin films. Thin films with an ordered structure are of major concern in such fields as semiconductor electronics, integrated optics and solid-state physics. The necessity to use films with an ordered structure, especially single crystalline films, stems from the fact that physical phenomena and effects can be reproduced best in such films. Also, as a rule, active parts of semiconductor devices and circuits are created in single-crystal regions due to their better performance.

To date, single-crystalline films have been mainly epitaxially grown on a single-crystalline substrate. However, the rapid growth of large-area electronic systems, specifically flat-panel active-matrix thin-film transistor (TFT) displays and two-dimensional imagers [1.1, 1.2] have initiated low-temperature preparation of thin *amorphous Si* (a-Si) films on glass. The potential for TFTs in applications such as smart cards, biometrics and sensors also makes desirable the possibility to prepare thin films on arbitrary substrates, such as glass, plastic and steel. For large-area electronic systems, the driver circuits such as shift registers, multiplexers, and amplifiers generally require higher performance than that available from a-Si. These circuits were provided by crystalline Si and were built externally to the flat panel array, requiring costly packaging to assemble them into the array and inducing potential reliability issues. The use of *poly-Si* TFTs allowed the integration of peripheral circuitry, which significantly reduced the number of interconnect wires and thus the packaging costs [1.3]. Complete integration of drivers, memory and CPU on the glass panel, i.e., system on glass, requires the preparation of *single-crystalline Si* films on a glass

substrate. Additionally, the present two-dimensional ICs are anticipated to reach their maximum degree of minimization in the near future. It is realized that any further increase in packing density and/or functions might depend on three-dimensional integration. To solve the problems mentioned above, techniques for preparing single-crystalline films on arbitrary (including amorphous) substrates are essential.

During the last few years, a variety of techniques have been proposed for the preparation of structured films, including single-crystalline semiconductor films on amorphous substrates. Among these approaches, those based on solid phase crystallization and on recrystallization by energetic beams (*e.g.*, laser, electron, incoherent-light) are highly effective. However, all of them have some shortcomings that limit their application. Seeking for a technological approach that produces low-temperature single c-Si thin films with high electronic quality and stable characteristics is *the* challenge for future thin-film semiconductor electronics.

This thesis is aimed to contribute to these efforts. It presents a new method to fabricate large crystalline-silicon islands on a predetermined location in a thin silicon film on a glass substrate by excimer-laser annealing.

## 1.2 Development of TFT addressed liquid crystal displays

A schematic diagram of TFT-LCD array with controllers, power supply and driver circuits is shown in Fig. 1.1.

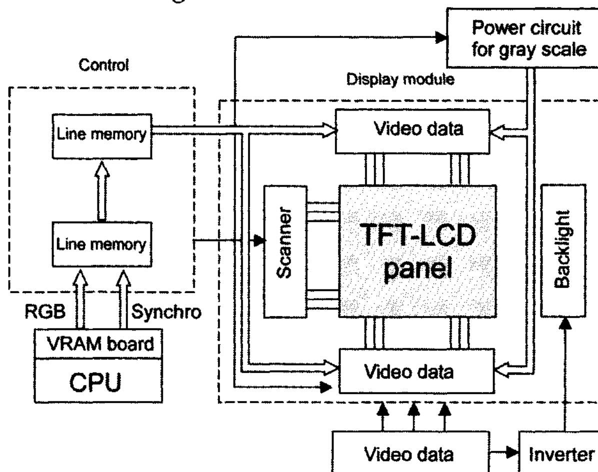


*Fig. 1.1* *A schematic diagram of TFT-LCD array.*

Generally, several trends can be distinguished in the development of recent TFT-LCD. One is the direct-view displays for use in portable computers and TV sets, where LCDs with larger screen sizes and higher pixel content are required [1.4, 1.5]. During the last 10 years, LCD screen size has rapidly increased, and larger ones of over 54 inches have been demonstrated at several exhibitions. The second trend is toward compact LCD modules with high pixel density for use as light valves in projection television sets and viewfinders in video cameras [1.6]. The third trend is fabrication of monolithic integrated drivers, memory and CPU on the glass panel, i.e., the system-on-glass approach.

## 1.3 Amorphous Si TFT

Hydrogenated amorphous silicon (a-Si:H) TFT-LCDs have been widely used for many applications in direct view displays such as LCD desktop monitors, TVs, audio/video displays and various monitors as well as for other large-area applications (i.e., TFT image sensor prototypes). Their wide application is attributed to the low-temperature deposition and fabrication processes, which are compatible with low-cost large-area glass substrates and suitable electronic properties. However, a severe disadvantage of a-Si:H film is its *metastability.* A considerable amount of dangling bonds is created under light soaking [1.7] or prolonged carrier accumulation [1.8]. As a consequence, the density of the defect states changes, even below the equilibrium temperature. Metastability has a great impact on the applicability of a-Si:H films in electronic devices, *e.g.*, it limits the reliability of TFTs. Thermal annealing steps above 150 °C are required to recover the initial state and to avoid further degradation [1.9]. Additionally, prolonged gate-voltage application leads to a voltage shift of the switching characteristics, limiting application of a-Si:H TFTs in electrical circuitry [1.10, 1.11, 1.12]. Nevertheless, the limited stability of a-Si:H is not an issue for the utilization of a-Si:H TFTs as pixel-switching elements. This is due to the relatively small duty cycle of the pulsed gate-voltage application. The low carrier mobility of a-Si:H TFT (~1 $cm^2/V\cdot sec$) implies certain constraints on display resolution and brightness. In order to achieve sufficient on-current, typically >$10^{-6}$ A [1.13], the ratio of the channel width to the channel length must be large, which in turn depends on the design rules of the lithographic process, and decreases the pixel pitch (determining the display resolution) and the fill factor (determining the brightness), leading to an unacceptably low display resolution and brightness. As a result, a low mobility increases the TFT area and the parasitic capacitance between electrodes.

## 1.4 Poly-Si TFT

Higher performance than that which can be achieved by using standard hydrogenated amorphous Si (a-Si:H) technology is required in order to get high-resolution flat-panel displays and imagers, to improve the noise performance of flat-panel imagers, and to integrate peripheral circuits, which include gate line drivers, data line multiplexers, and pixel-level electronics. Poly-Si satisfies many of these requirements due to its higher carrier mobility (approximately 100 $cm^2/V\cdot sec$ versus 1 $cm^2/V\cdot sec$ for a-Si) and the availability of a number of fabrication techniques of poly-Si TFTs at a temperature much lower than the strain point of a glass substrate. For large-area electronic systems, the driver circuits, such as shift registers, multiplexers, and amplifiers, generally require higher performance than is available from a-Si. These circuits were provided by crystalline Si and were built externally to the flat panel array, requiring costly packaging to assemble them into the array and inducing potential reliability issues. The use of poly-Si TFTs allowed the integration of peripheral circuitry, which significantly reduced the number of interconnect wires and thus the packaging costs. The low leakage currents of the poly-Si thin-film transistors (TFTs) in the off state, which are the major concern for pixel switch applications, particularly for imager applications, have been realized via lightly-doped drain structures (LDD) [1.14, 1.15, 1.16].

In general, four approaches are used for the fabrication of poly-Si film: direct deposition by CVD, solid phase crystallization (SPC), pulsed rapid thermal annealing (PRTA) and excimer laser annealing (ELA) [1.17, 1.18, 1.19, 1.20]. The most conventional method to fabricate poly-Si is low-pressure chemical vapor deposition (LPCVD) [1.21]. However, this method has some disadvantages, such as a high deposition temperature of over 600 °C, small grain size < 50 nm, poor crystallinity and high density of grain boundary states. As a result, low-temperature and large-area processes using a cheap glass substrate are impossible. To enhance crystal properties, it is much more useful to use SPC, as it results in a larger grain size than the poly-Si film directly deposited by LPCVD [1.18]. SPC needs annealing at a high temperature of over 600 °C. However, plasma enhanced pressure chemical vapor deposition (PECVD) could also be used to fabricate poly-Si film, using an $SiF_4/SiH_4/H_2/He$ mixture gas at temperature below 450 °C [1.17, 1.22]. However, directly deposited poly-Si films have some problems such as poor crystallinity and a small grain size.

On the other hand, there are liquid phase recrystallization methods such as zone melting regrowth (ZMR) and ELA, which result in a good quality poly-Si film with large grain size and good electrical properties. In the case of ZMR, the temperature of whole substrate increases up to about the melting temperature of a-Si, to nearly 1000 °C, so that a glass substrate cannot be applied. PRTA was suggested as a better process at low temperature < 800 °C [1.19]. Due to the short

pulse duration, PRTA introduces only minor (insignificant) thermal damage to the glass substrate. In contrast, ELA technology can be used to fabricate TFT-LCDs in the low temperature poly-Si films with high grain crystallinity without thermal damage to the glass substrate. By lowering the laser energy density it achieves a sufficient homogeneity of device properties over the large-area substrate, which makes it possible to fabricate reproducibly circuits with controlled properties. Two alternative methods, metal-induced crystallizations (MIC) and metal-induced lateral crystallizations (MILC), have been investigated extensively in the last few years [1.23, 1.24]. However, the drawback of these techniques is a high defect density in Si grains and contamination of Si film with metal impurities.

## 1.4.1 Effect of grain boundary

Polycrystalline material has certain limitations when it comes to transporting electrons due to its microstructure, which is composed of small crystallites, joined by grain boundaries. Generally, two main groups of grain boundaries are distinguished: low- and high-angle boundaries. Low-angle grain boundaries consist of dislocation networks [1.25]. High-angle grain boundaries are misorientations between two adjacent grains. Generally, these high-angle grain boundaries are further classified into random grain boundaries and coincidence grain boundaries. In the case of a coincidence grain boundary, there exists a coincidence site lattice, which is common to both adjacent grains [1.26]. Random grain boundaries lack such a common lattice. The nature of the grain boundary strongly influences the electrical characteristics of the material. Reports in the literature show that coherent first-order twins are electrically inactive [1.27, 1.28, 1.29]. Higher-order twins and faceted twin boundaries, e.g., coherent first-order twins with incoherent segments, are in most cases only weakly electrically active [1.30]. A secondary dislocation network leads to electronic levels in the band gap, initiating electrical activity in terms of minority carrier recombination and potential barriers [1.31]. Random grain boundaries are generally electrically active [1.32].

The conductivity behaviour of the poly-Si films is explained on the basis of the grain boundary trapping model [1.33]. This model assumes the presence of only one level of deep states, located at random grain boundaries. Since atoms in such random grain boundaries are highly disordered, there is a large number of defects due to incomplete atomic bonding. This results in the formation of trapping states, which influence the electrical conduction in the following manner:

1. The free carrier number is reduced, due to immobilization by trap carriers;

2. After trapping the mobile carriers, the traps become electrically charged, creating a potential energy barrier $E_B$, surrounded by a depletion region. This barrier impedes the motion of carriers from one crystallite to another.

The resultant charge distribution and energy band diagram are schematically shown in Fig. 1.2 for p-type poly-Si. According to the grain boundary trapping model, poly-Si film and poly-Si TFT have the following characteristics [1.33, 1.34]:

(a) The current over the potential barrier $E_B$ is governed by thermionic emission over the boundaries, which implies its variation as $exp(-E_B/kT)$ for $E_B > kT$, where $k$ is Boltzmann's constant and $T$ is the temperature.

(b) The mobility increases with the average grain size $d_L$.

(c) The mobility and barrier height are the functions of doping and intrinsic carrier concentration, and hence of the gate voltage.

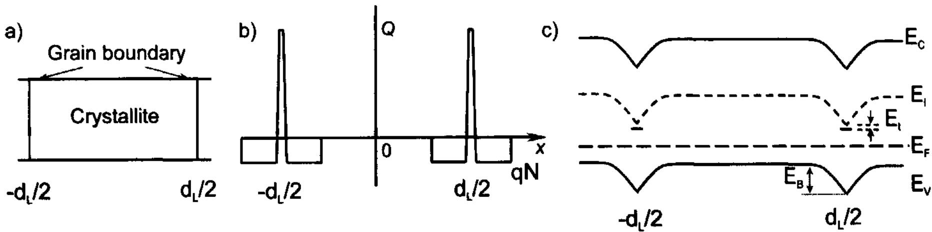


*Fig. 1.2 Effect of grain boundary a) Crystal structure b) Charge distribution c) Energy band structure.*

(d) The source-drain current $I_D$ can be expressed as [1.34]:

$$I_D \approx \left(\frac{\omega C_{ox} q\mu}{l}\right)(V_G - V_T)V_D \times \exp\left(-\frac{qV_B}{kT}\right) \tag{1.1}$$

where $\omega$ and $l$ are the width and the length of the channel region, respectively; $C_{ox}$ is the gate-oxide capacitance, $q$ is the electron charge, $\mu$ is the carrier mobility; $V_G$, $V_D$ and $V_T$ are the gate, the drain and the threshold voltages, respectively; $V_B$ is the height of the potential barrier.

Assuming that the thickness of poly-Si film is proportional to $1/(V_G\text{-}V_T)$ and all traps are filled with a trap state density $Q_t$, the potential barrier at the grain boundary can be written as [1.35]:

$$V_B \sim \frac{Q_t^2}{(V_G - V_T)^2} \tag{1.2}$$

### 1.4.2 Limitations of poly-Si TFT

As follows from the characteristics of the poly-Si film and poly-Si TFT, the carrier conduction in on-state can be increased by:

1) Increase in grain size $d_L$;

2) Lowering of trap density $Q_t$ by defect passivation (e.g., hydrogenation);

3) Increase in the gate voltage $V_G$ (Eq.(1.1), (1.2)).

In general, for poly-Si TFT with few grain boundaries this implies that the carrier mobility should approach that of c-Si TFT. However, even at high doping levels and after hydrogenation treatment, the mobility will be always less than that of single c-Si film. The average grain size of the conventional excimer-laser-produced poly-Si thin films is as small as a few hundred nm, since the melt-regrowth duration is very short (approx. 100 ns). The performance of the resulting device is strongly influenced by the size distribution of the obtained poly-crystals and their crystalline quality, which are controlled by phase transformation mechanisms, occurring during thin Si film irradiation.

Despite the assumption of the grain boundary trapping state model, material defects are located not only at the grain boundaries themselves (i.e., deep states), but also in the intragrain bulk (i.e., tail states), leading to additional scattering at the intragrain defects. Therefore, the efficiency of defect hydrogenation is decreased due to the lower passivation rate of the intragrain material defects. Although the maximum value of the TFT mobility can be reached at the maximum grain size, the uniformity of the device performance is poor due to the non-uniform distribution of large grains. As a consequence, in a poly-Si TFT the average carrier mobility is lower than for a single c-Si TFT [1.36]. On the other hand, a large density of defects at the grain boundary near the drain edge of TFT is the dominant origin of the high off-current due to the thermal generation of carriers at high drain fields [1.36]. Additionally, poly-Si TFTs often suffer from a voltage shift of the switching characteristics (i.e., threshold voltage), limiting their application in electrical circuitry, which requires high duty cycles of the pulsed gate-voltage application [1.11, 1.12].

## 1.5 Aim and outline of this thesis

To realize a complete system on glass, both the field effect mobility and the off-current of the poly-Si TFTs, which are typically five times lower and three decades higher than those of MOS transistors [1.37], respectively, have to be improved. It is obvious that TFT with both high mobility (similar to that of bulk-Si) and low off-current can be obtained if the channel is formed within a single c-Si grain. For excimer-laser re-crystallized a-Si films, this can be realized in two ways:

1. By the *enlarging* the grains to more than the size of the TFT or in the ideal case, the growth of grains that are as large as possible (i.e., islands of several hundred μm in diameter). As will be explained below, the latter approach, realized with the single laser pulse, is not straightforward, due to the inevitable occurrence of homogeneous nucleation in a supercooled Si pool.

2. By the fabrication of *2-Dimensionally aligned* single c-Si islands as large as the TFT active channel region (i.e., few μm in diameter). The important benefits are the elimination of the grain boundary influence and of high defect density planar defects and high uniformity of the resulting TFT devices.

However, the crystallographic orientations of such c-Si island also need to be controlled due to the mobility anisotropy. As was shown experimentally, the electron field-effect mobility $\mu$ (100) is higher than $\mu$ (111) in MOSFETs under a strong electric field [1.38]. Theoretical investigations showed that $\mu$ (100) > $\mu$ (311) > $\mu$ (211) > $\mu$ (111) = $\mu$ (011) due to the effective mass anisotropy [1.39]. Therefore, random crystallographic orientations of the single c-Si islands can lead to the large spread in the electrical characteristics of transistors with different channel Si region orientation [1.38].

Consequently, the topics that are primarily addressed in this work concern mechanisms of grain growth in excimer-laser annealed (ELA) Si film, spatial geometry variation of the sample for location control, process reproducibility in terms of the processing window and seeding techniques to control film texture. Chapter 2 describes transformation mechanisms in conventional excimer-laser a-Si crystallization. In particular, it summarizes the heat transport and melting phenomena during ELA of a-Si, and introduces the vertical and lateral grain growth mechanisms. Consequently, it explains the underlying principles of grain enlargement, and control of the position and crystallographic orientation of grains. To verify these principles, we utilized different structures and laser techniques, such as a single beam method with a multi-layer structure (sample), a dual-beam approach with a non-uniform sample geometry and metal-induced crystallization. The fabrication of these structures, analysis tools and characterization techniques are discussed in Chapter 3. Chapter 4 presents the experimental results of grain enlargement with a single laser beam. It also proposes two different models of vertical and lateral grain growth, based on heat-flow and phase-field approaches. These experimental results are compared with grain-growth simulations. Chapter 5 shows the experimental results obtained with dual-beam irradiation. In particular, it analyses the effect of grain enlargement and the processing energy density window of obtained location-controlled grains. The earlier presented heat-flow model is used to explain experimental results. Chapter 6 presents the metal-induced crystallization of amorphous silicon. The effects of a different Ni film thickness, annealing temperature and laser irradiation on the crystallographic orientation of Si film are investigated. Finally, Chapter 7 gives conclusions and recommendations for further research.

# Chapter 2

# *Underlying theory and concepts*

This chapter describes transformation mechanisms in conventional excimer-laser a-Si crystallization. In particular, it summarizes the heat transport and melting phenomena during excimer-laser annealing of a-Si, and describes the vertical and lateral grain growth mechanisms. It also explains the underlying principles of grain enlargement, control of the position and crystallographic orientation of the grain, as well as the approaches for their realization.

## 2.1 Transformation mechanisms in conventional excimer-laser a-Si crystallization

In pulsed-laser crystallization of silicon thin films, several phase transformation mechanisms have been identified, which are based on the dependence of the resulting microstructure and the temporal phase change on the incident laser energy density [2.2,2.3]. At a sufficiently low energy, the laser irradiation does not modify the a-Si film structure. However, at a certain threshold energy, polycrystalline Si (pc-Si) islands appear at the film surface. Figure 2.1a shows a transmission-electron microscopy (TEM) cross section of the resulting microstructure, where the liquid/solid interface has already propagated halfway through the film. The time-resolved optical reflectivity (TROR) profile, depicted in Fig. 2.2a, shows a small peak around $t$ = 60 ns, attributed to the appearance of liquid Si at the surface. If the energy is increased further, the liquid/solid interface can propagate through the whole film thickness due to the formed thin liquid Si layer near the surface.

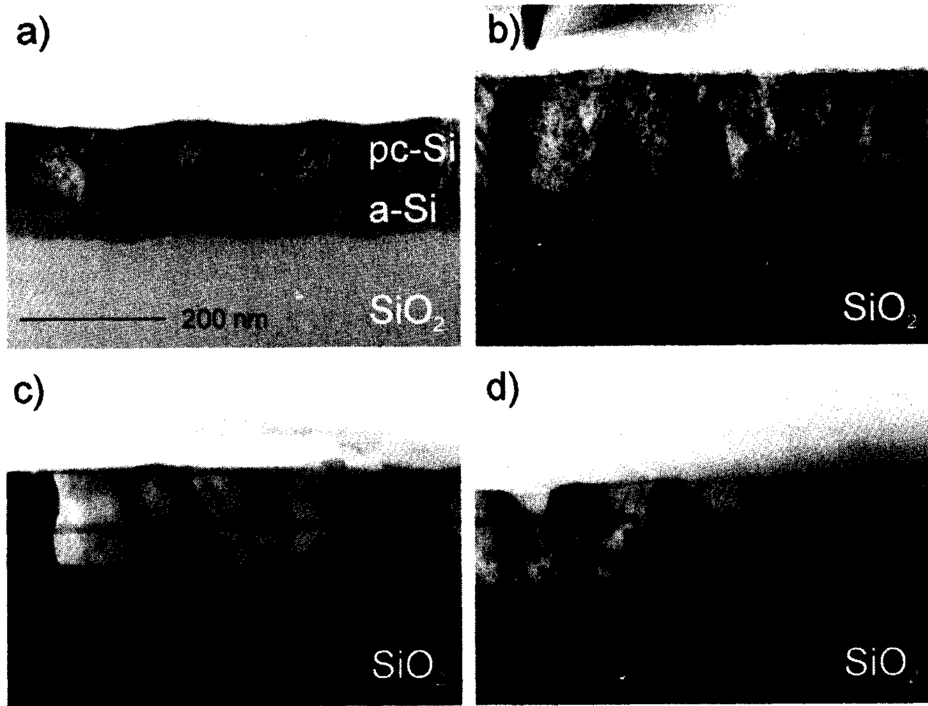


*Fig. 2.1* *TEM cross-section of laser irradiated Si film. Reprinted from* [2.3].

As the liquid begins to solidify during laser irradiation as fine and defective poly-Si, the released latent heat causes the underlying a-Si layer to melt. The newly formed thin liquid layer is severely supercooled compared to the poly-Si layer and therefore re-solidifies as fine-grained poly-Si. As a consequence of latent heat release, this thin liquid layer propagates further through the underlying a-Si, leading to partial melting and re-growth. This is called the explosive crystallization process; it is in fact self-sustaining until the critical quenching of the propagating liquid is reached [2.4].

The TROR profile, depicted in Fig. 2.2b, shows rapid oscillations around $t$ = 50 ns for both the surface and the Si/$SiO_2$ interface. This behaviour is attributed to the above-mentioned explosive crystallization process, i.e., the self-propagating buried liquid layer. Figure 2.1b shows a TEM photo of the resulting microstructure, which consists of small defective grains of 20-50 nm width, increasing in grain size with the laser energy.

A second region has been observed for laser energies inducing the near-complete melt of the a-Si film. In this regime, rather large-grain-sized silicon crystallites are produced through so-called super lateral growth (SLG). The TEM

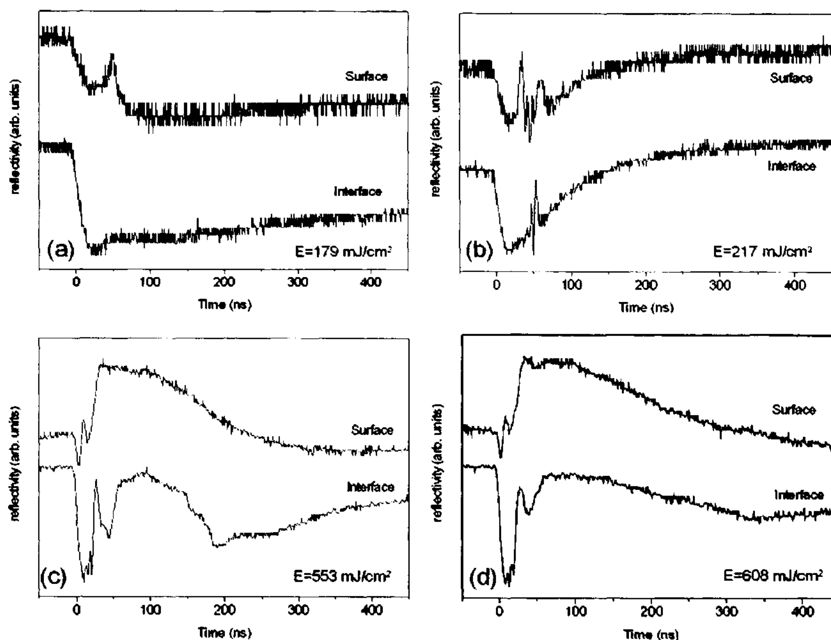


*Fig. 2.2* *Time-resolved optical reflectivity (TROR) profiles of laser-irradiated Si film. Reprinted from* [2.4].

cross section in Fig. 2.1c shows the resulting V-shape tapered grain structure typical for SLG transformation. This phenomenon is based on liquid-phase epitaxial regrowth from discrete unmelted poly-Si clusters in a melt pool. As the second peak in the TROR spectra in Fig. 2.2c indicates, the a-Si film is melted for the second time. However, the resulting melt front is not planar, but zigzag like, propagating faster along defects and grain boundaries towards the interface. In this way the remnant defect-free single clusters, originating from explosive crystallization, act as seeds for subsequent liquid-phase epitaxial regrowth.

The high-energy regime corresponds to energy densities exceeding the threshold for complete melting of the Si film, which can be seen from the TROR spectra in Fig. 2.2d, where both the surface and interface undergo a prolonged melting transition. Because the heat is transferred from the Si melt pool to the substrate, the melt pool becomes severely supercooled, and copious nucleation followed by rapid solidification occurs [2.5]. The final microstructure consists of fine-grained poly-Si, shown in Fig. 2.1d; the influence of the incident laser energy on the grain size was found to be nearly negligible.

## 2.2 Melting and solidification of the excimer-laser melted Si film

Let us consider a semi-infinite substrate that is uniformly irradiated by a single rectangular laser pulse of duration $t_l$, schematically drawn in Fig. 2.3a. Material evaporation shall be ignored. The temporal behaviour of the surface temperature, $T_s = T\ (z = 0)$, is schematically shown in Fig. 2.3b. $T_s$ reaches the equilibrium melting point $T_m$ at time $t_m(0)$. Subsequently, $T_s$ increases much slower or not at all, as the absorbed laser-light energy is spent not only on heating, but also on melting, which requires an enthalpy $\Delta H_m$. After a time $t_m$ the surface has melted to a depth $h_l$. $T_s$ increases further when the melt front matches the heat front. The maximum $T_s$ is reached at $t_l$. For times $t > t_l$, the system cools and resolidifies within a time $t_s$. Generally, the heating and cooling periods are so short that overheating of the solid phase and supercooling of the liquid phase is significant (dotted curves). For grain growth the time $t_s$ during which the layer cools and resolidifies is of particular interest.

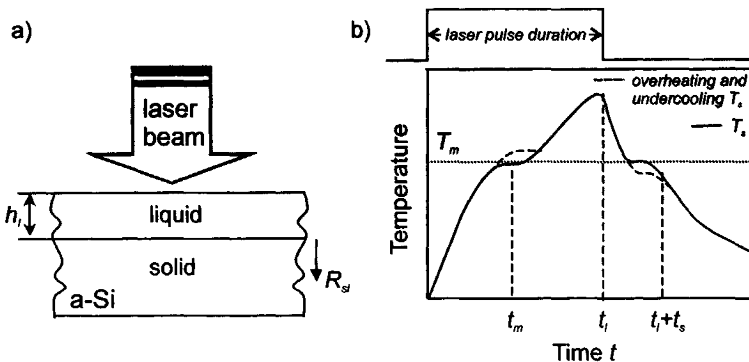


*Fig. 2.3* *a) Excimer-laser-induced surface melting. (b) Temperature profile along the surface.*

### 2.2.1 Driving force for solidification

Solidification is the physical process of the conversion of a liquid melt into a solid phase. From Fig. 2.4 it follows that this conversion is accompanied by the release of the latent heat of fusion $\Delta L_f$ accumulated in the material, i.e., $\Delta H_{ls}$ -$\Delta H_{sl}$ is $\Delta L_f$, since the Gibbs free energy $\Delta G$ is higher in the liquid phase than in the crystal phase. The solid/liquid interface represents the separation between the

material containing latent heat and the material having completely released it. In this way a system will try to reduce the free energy difference $\Delta G$ between the liquid and crystal phases, which can be regarded as the driving force for the melt-crystal transition.

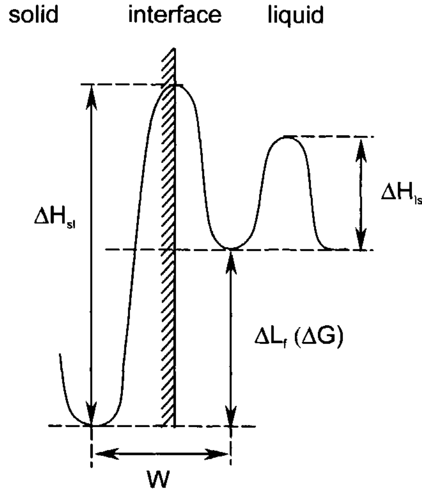


*Fig. 2.4* *Free enthalpy distribution near crystal surface ($\Delta H_{ls}$) and solid/liquid interface ($\Delta H_{sl}$). W is the width of interfacial region.*

The free energy difference $\Delta G$ can be given as [2.6]:

$$\Delta G \approx \frac{\Delta L_f \Delta T}{T_m} \tag{2.1}$$

where $\Delta T$ is the supercooling temperature, usually defined as the temperature difference between the equilibrium temperature of a system $T_e$ and its actual temperature. The latter is lower than the equilibrium temperature when the melt is supercooled. In this case, $\Delta T$ is greater than zero. The term "supercooling" is often used interchangeably with "undercooling" in the literature. As follows from Eq. (2.1) crystal growth is possible as long as there is a suitable deviation from thermodynamic equilibrium with a driving force $\Delta G$. This driving force, $\Delta G$, which is expressed in terms of supercooling, $\Delta T$, is commonly obtained by cooling the mixture to below the equilibrium temperature. Thus, the solidification is a reaction whose rate depends upon the degree of supercooling that drives it.

## 2.2.2 Heat extraction and cooling

The various solidification processes involve heat exchange between the melt and the solid in a more or less controlled manner. Heat extraction changes the energy of the phases (solid and liquid) in two ways:

1. There is a decrease in the enthalpy of the liquid or solid $\Delta H$, due to cooling;
2. There is a decrease in enthalpy, $\Delta H$, due to the transformation from liquid to solid, which is equal to the latent heat of fusion, $\Delta L_f$.

Heat can be extracted from the melt pool by applying a suitable means of cooling to it or solid fraction in order to create an external heat flux $q_{sub}$ towards the underlying substrate. The resultant cooling rate, $dT/dt$, can be deduced from a simple heat balance, under the assumption that the specific heat of the liquid and the solid are the same. Using the latent heat per unit volume, $L_f$, defined to be positive for solidification and also the specific heat per volume, $C$, one can express the heat balance equation as follows [2.7]:

$$q_{sub}\left(\frac{S}{V}\right)=-C\left(\frac{dT}{dt}\right)-\Delta L_f\left(\frac{df_s}{dt}\right) \tag{2.2}$$

so that cooling rate can be presented as:

$$\dot{T}=\frac{dT}{dt}=-q_{sub}\left(\frac{S}{VC}\right)-\left(\frac{df_s}{dt}\right)\left(\frac{\Delta L_f}{C}\right) \tag{2.3}$$

where $f_s = (1- f_l)$ is the volume fraction of solid and $f_l$ is the volume fraction of liquid. The first term on the right-hand side (RHS) of Eq.(2.3) reflects the effect of the external heat flux $q_{sub}$ extracted from the irradiated surface topology (the ratio of laser-irradiated area, $S$, to its volume, $V$). The second term takes into account the continuing evolution of latent heat of fusion during solidification. It can be seen from this equation that, during solidification, heating will occur if the second term on the RHS of Eq.(2.3) becomes greater than the first one. This phenomenon is known as recalescence. For an amorphous material, where solidification occurs over a range of temperatures, the variation of the fraction of solid $f_s$ as a function of time (i.e., solidification rate $R_{sl}$) can be calculated from the relationship:

$$\frac{df_s}{dt}=\left(\frac{dT}{dt}\right)\left(\frac{df_s}{dT}\right) \tag{2.4}$$

since $f_s$ is a function of temperature. Inserting Eq.(2.4) into Eq.(2.3) gives:

$$\dot{T} = \frac{-q_{sub}\left(\frac{S}{VC}\right)}{1+\left(\frac{\Delta L_f}{C}\right)\left(\frac{df_s}{dT}\right)} . \tag{2.5}$$

It is seen that during solidification, the cooling rate decreases, since $df_s/dT$ is negative. As follows from Eq.(2.3) and Eq.(2.5), the cooling rate $dT/dt$ is determined by the thermal flux to the substrate $q_{sub}$ and the heat capacity of the Si material $C$.

## 2.3 Nucleation

Two different steps have to be distinguished in crystallization: the formation of a new crystal, a nucleus, and further growth of the nucleus to a crystal of the required dimensions. The matrix has to be supercooled for nucleation to occur. Two types of nucleation play a role in the generation of new nuclei: homogeneous and heterogeneous nucleation, as shown schematically in Fig. 2.5.

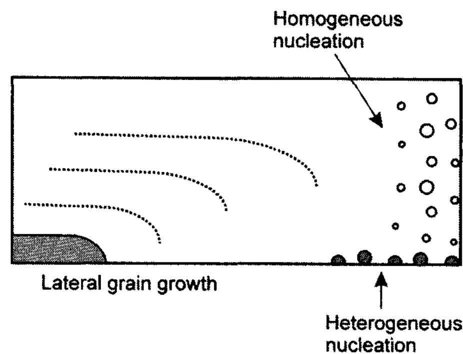


*Fig. 2.5 Nucleation types occurring during crystal growth.*

Homogeneous nucleation starts from sites not predictably recognized in the original volume; or, in an alternative formulation, each point in the volume has the same probability of generating a new seed. In heterogeneous nucleation the sites are either predictable or recognized *a posteriori*; they may be unevenly distributed in the matrix, but the process remains stochastic. The term "site" does not only have the meaning of a particular place where the new phase originates, but also conveys the idea of favouring (catalyzing) the

transformation. The presence of foreign particles, inclusions and internal interfaces in solids can catalyse the process, by reducing the activation barrier.

The critical radius, $r_c$, and the activation energy $\Delta G^*$ for the nucleation of a spherical nucleus in a pure melt are given in Table 2.1 for both nucleation types. Here $\sigma_{sl}$ is the solid/liquid interface energy, $\Delta G_v$ is the Gibbs free energy per unit volume, $\theta$ is the wetting angle between the nucleating solid phase and the substrate, $f(\theta)$ is the shape factor, which is zero if $\theta = 0$ and equal to 1 if $\theta = 180°$.

*Table 2.1 Critical dimensions $r_c$ and activation energy $\Delta G^*$ for the nucleation of a spherical nucleus in a pure melt.*

| *Value* | *Homogeneous nucleation* | *Heterogeneous nucleation* |
|---|---|---|
| $r_c$ | $\frac{2\sigma_{sl}}{\Delta G_v}$ | $\frac{2\sigma_{sl}}{\Delta G_v}$ |
| $\Delta G^*$ | $\frac{16\pi}{3}\frac{\sigma_{sl}^3}{\Delta G_v^2}$ | $\frac{16\pi}{3}\frac{\sigma_{sl}^3}{\Delta G_v^2}f(\theta)$ |

If the size of the cluster is below $r_c$, the cluster tends to disappear since this causes a decrease in free energy. If the size of the cluster equals $r_c$, it will either melt away or grow as illustrated in Fig. 2.6a. As follows from Table 2.1, the activation energy barrier $\Delta G^*$ against heterogeneous nucleation is smaller than that for homogeneous nucleation by a shape factor $f(\theta)$. Due to the lower activation barrier, the probability of heterogeneous nucleation is higher than the the probability of homogeneous nucleation. The effect of supercooling, $\Delta T$, on activation energy $\Delta G^*$ is shown schematically in Fig. 2.6b for both nucleation types. As can be seen, heterogeneous nucleation will occur at much lower supercooling temperatures than homogeneous nucleation. However, despite the frequent occurrence of heterogeneous nucleation in phase-transformation processes due to the presence of interfaces, inclusions or defects in a real system, the pulsed excimer-laser melting of Si film is mainly characterized by the occurrence of homogeneous nucleation [2.8, 2.9]. This is because the molten Si film is subject to ultra-rapid quenching conditions while in contact only with a relatively non-catalytic $SiO_2$ surface, i.e., with a chemically stable and structurally amorphous oxide layer. Only in some cases of excimer-laser dual beam irradiation of Si heterogeneous nucleation was observed before homogeneous nucleation occurred [2.10].

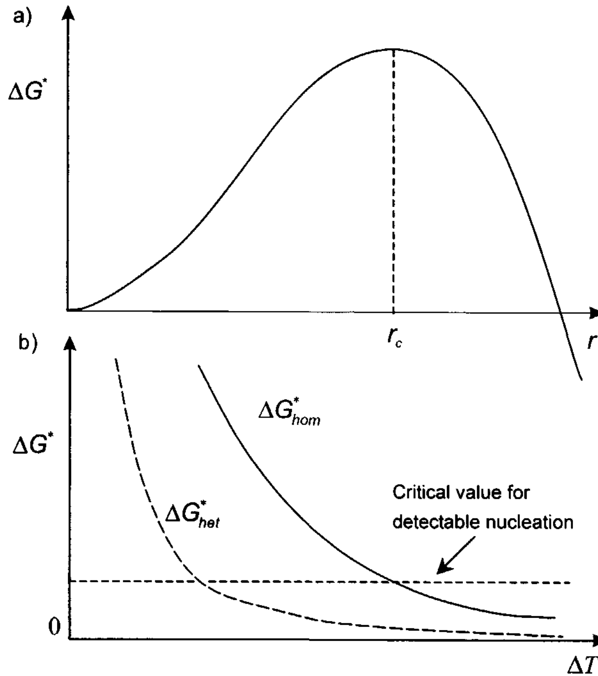


*Fig. 2.6* *(a) Free energy of nucleation cluster as function of its radius (b) Variation of $\Delta G^*$ with supercooling ($\Delta T$) for homogeneous and heterogeneous nucleation.*

## 2.4 Lateral and vertical grain growth

Figure 2.7 shows schematically the influence of the laser energy density on the grain size and growth mechanism [2.2]. As illustrated, the largest grain size occurs in the SLG regime (i.e., mid energy range). In this regime the distance $d$ between remnant c-Si seeds is larger than the maximum lateral overgrowth distance $d_L$, i.e., $d > d_L$. Here the solidification proceeds mainly via the lengthening of grains, i.e., through a *lateral growth mechanism*, as illustrated in Fig. 2.7b. The lateral growth stops due to the onset of homogeneous nucleation, and subsequent thickening of grains takes place. The size of the obtained grains can exceed the Si film thickness many times; the microstructure is equiaxed.

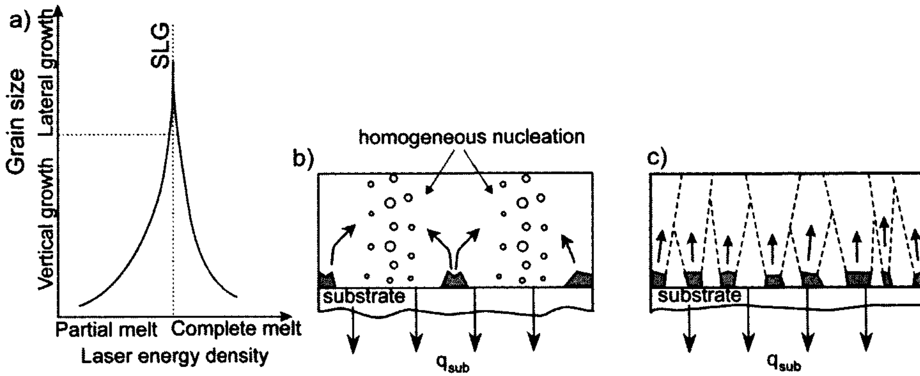


*Fig. 2.7* *Influence of laser energy density on the grain size and growth mechanism. b) Lateral and c) vertical solidification mechanisms.*

In the partial melting regime (i.e., the low energy range in Fig. 2.7a), when $d < d_L$, solidification proceeds mainly via the thickening of grains once the grains occlude with each other. The growth occurs through a *vertical growth mechanism* as illustrated in Fig. 2.7c. Due to the close vicinity of growing grains, released latent heat of solidification keeps the temperature of molten Si above its supercooling value, thus preventing the occurrence of homogeneous nucleation. Finally, the obtained grains have a non-equiaxed columnar microstructure.

In the complete melting regime (i.e., the high energy range in Fig. 2.7a), the growth from homogeneous nucleation in the supercooled melt occurs in every direction. As shown by Fig. 2.7a, the grain growth in the lateral direction occurs only in a very narrow energy range, typically that of 15-20% of the total energy density [2.2]. In the partial melting regime (i.e., ~ 55% of the total energy range) the grain growth is perpendicular to the surface.

In case of crystal growth, one is interested in determining the instantaneous position of the solid/liquid interface as a function of the various process parameter values. This problem belongs to a generic type of problems collectively known as moving boundary problems. The position of the moving boundary can be determined within the framework of the Stefan problem. In case of a-Si, melting and solidification take place over a range of temperatures, but it is still possible to define upper and lower limits to the range as the liquid and solid temperatures. Consider for example vertical growth from a solid Si seed at a velocity $R_{Vsl}$ with a planar interface into a supercooled melt, as illustrated in Fig. 2.8a. The temperature distribution in liquid and solid Si on a $SiO_2$ underlayer is depicted schematically in Fig. 2.8b. It is assumed that the temperature at the solid/liquid interface, $z = h_l(t)$, is continuous and equal to the melting temperature $T_m$:

$$T(z = h_l(t)) = T_l(h_l) = T_s(h_l) = T_m \tag{2.6}$$

where $T_s$ and $T_l$ are the temperatures of solid and liquid fractions.

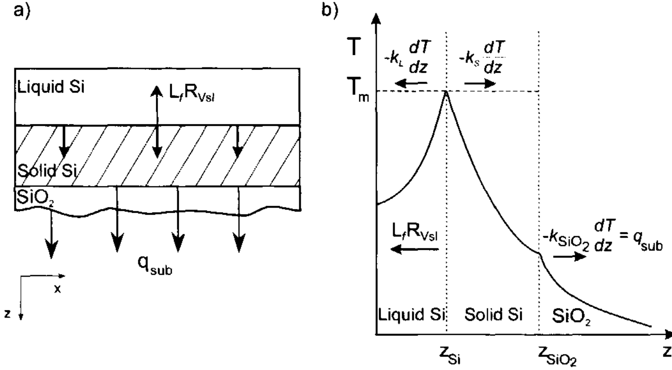


*Fig. 2.8 a) Vertical solidification b) temperature distribution.*

Vertical solidification is controlled by the rate at which the latent heat of solidification is conducted away from the solid/liquid interface. Since the moving boundary is the precise site at which the phase change is taking place, the latent heat of phase transformation $L_f$ must be taken into account in the mathematical formulation. The heat flow away from the interface through the liquid must balance the heat of the solid plus the latent heat generated at the interface:

$$L_f R_{Vsl} = k_L \frac{dT_l}{dz} + k_s \frac{dT_s}{dz} \ . \tag{2.7}$$

Here, $k_L$ and $k_S$ are the thermal conductivities of the Si in the liquid and solid phases, respectively, and z is the solidifying film thickness. The heat flux from molten Si towards its solid fraction can be replaced by heat conduction into the underlying $SiO_2$ layer (i.e., the substrate), since the thermal conductivity $k_{SiO2}$ is almost one order smaller than $k_{Si}$ such as:

$$q_{sub} = -k_{SiO_2} \left. \frac{\partial T(t,z)}{\partial z} \right|_{z=z_{SiO}} \approx -k_{Si} \left. \frac{\partial T(t,z)}{\partial z} \right|_{z=z_{Si}} \tag{2.8}$$

where $z_{SiO}$ and $z_{Si}$ are the positions of the solid $Si/SiO_2$ and the Si liquid-solid interface, respectively. Thus, Eq.(2.7) can be rewritten as:

$$-k_L \frac{dT_L}{dz} = -q_{sub} - L_f R_{Vsl} \ . \tag{2.9}$$

The lateral propagation of the Si liquid-solid interface along the underlying $SiO_2$ film is shown in Fig. 2.9a. Fig. 2.9b and 2.9c illustrate the temperature distribution in liquid Si versus time and film thickness, respectively.

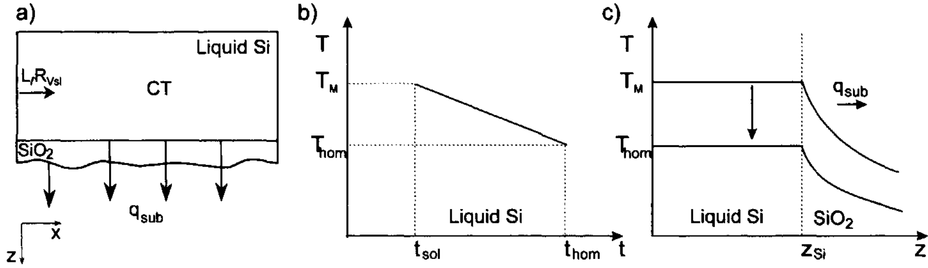


*Fig. 2.9* *a) Lateral solidification and temperature profiles versus b) time and c) depth from the film surface.*

To simplify calculations, the following assumptions are made:

1) The temperature decreases linearly from $T_m$ to $T_{hom}$ over time, Fig. 2.9b.
2) The temperature is constant through the Si thickness, Fig. 2.9c.

As follows from Fig. 2.9b, the time occurrence of solidification and critical supercooling temperatures $T_m$ and $T_{hom}$, can be as:

$$\begin{aligned} T(t) &= T_m \because t = t_{sol} \\ T(t) &= T_{hom} \because t = t_{hom} \\ T(t) &= \Delta T \because t_{sol} < t < t_{hom} \end{aligned} \tag{2.10}$$

where $t_{sol}$ is the onset of solidification. As can be seen, heat removal from the supercooled Si melt into the substrate is determined by the extraction of thermal energy (i.e., $C \times T$) deposited in the liquid Si by means of the following heat conservation equation:

$$\frac{dq_{sub}}{dz_{Si}} = \frac{d}{dz_{Si}}\left(-k_L \frac{dT}{dz_{Si}}\right) = \frac{C_{Si} dT}{dt} . \tag{2.11}$$

Combining Eq.(2.9) and Eq.(2.11) one can derive the equation to describe solidification in the vertical and lateral directions as:

$$\frac{d}{dz_{Si}}\left(-q_{sub} - L_f R_{Vsl}\right) = \frac{C_{Si} dT}{dt} . \tag{2.12}$$

As follows from this equation, the cooling rate, $dT/dt$ is determined by the balance between the thermal flux $q_{sub}$ to the substrate and the generation of latent heat of fusion $L_f$ from liquid fraction, solidifying with velocity $R_{Vsl}$.

The total heat amount conducted from the Si film with thickness $z_{Si}$ during transient solidification can be obtained by integrating Eq. (2.12) from a time $t_{sol}$ of solidification onset to a time $t_{hom}$ of the nucleation onset at which solidification stops:

$$-\int_{q_{sol}}^{q_{hom}} \int_{t_{sol}}^{t_{hom}} dq_{sub} dt - L_f \int_{R_{sol}}^{R_{hom}} \int_{t_{sol}}^{t_{hom}} dR_{Vsl} dt = -C_{si} \int_{T_m}^{T_{hom}} \int_{0}^{z_{Si}} dTdz \quad (2.13)$$

where $q_{sol}$, $q_{hom}$ and $R_{sol}$, $R_{hom}$ are the values of the heat flux and the velocity at solidification and nucleation onsets, respectively. By solving Eq.(2.13), one can determine the time $t_{hom}$ of the homogeneous nucleation onset during the vertical Si growth mechanism as:

$$t_{hom} = \frac{C_{Si}\left(T_m - T_{hom}\right) z_{Si}}{q_{sub} + L_f R_{Vsl}} + t_{sol} \quad . \quad (2.14)$$

The physical significance of Eq.(2.14) is that the nucleation onset $t_{hom}$ during lateral grain growth can be delayed by reduction of thermal flux $q_{sub}$ from the molten Si layer and the vertical solidification velocity $R_{Vsl}$ at a given latent heat of fusion.

The maximum lateral overgrowth distance $d_L$ (i.e., the final grain size) during transient lateral solidification can be determined from:

$$d_L = R_{Lsl} \times \left(t_{hom} - t_{sol}\right) \quad , \quad (2.15)$$

where $R_{Lsl}$ is the lateral solidification velocity. As one can see from Eq.(2.15), the maximum size $d_L$ of laterally solidifying grains can be obtained by increasing the lateral solidification velocity $R_{Lsl}$ and/or by delaying $t_{hom}$.

# 2.5 Enlargement of c-Si single island

## 2.5.1 Theory and requirements

From the above review of solidification of excimer-laser-melted Si film, the fundamental requirements for the enlargement of single c-Si islands become readily apparent.

1) The delay of the homogeneous nucleation onset, occurring at time $t_{hom}$, allows for longer lateral growth during solidification. As can be seen from Eq.(2.14), $t_{hom}$ is determined by the thermal flux $q_{sub}$ to the underlying layer and by the vertical solidification velocity $R_{Vsl}$. From Eq.(2.8) follows that in order to reduce the heat loss, the thermal conductivity of underlying layer should be decreased and/or the temperature gradient $dT/dz$ near the Si/underlayer boundary should be gentle. For example, $q_{sub}$ can be decreased by increasing the thickness $h_{ins}$ of the intermediate thermal insulation layer between the Si film and a heat conductive substrate. As a result, $R_{Vsl}$ decreases and $t_{hom}$ will be delayed.

2) The lateral solidification velocity, $R_{Lsl}$, should be as high as possible. However, the velocity of movement of the solid/liquid interface in the lateral direction influences the morphological stability of the growth front and therefore determines the crystalline quality of the growing island. When the crystal growth is driven at critically high velocities of 15m/s, the growth front becomes morphologically unstable. It can break down completely with the formation of a disordered amorphous solid fraction, resulting in amorphization of the Si film [2.11]. Therefore, the lateral solidification velocity $R_{Lsl}$ should be driven below this critical value in any case.

## 2.5.2 Methods of grain size enlargement

Figure 2.10 shows earlier published results on average grain sizes as a function of vertical solidification velocity [2.12]. One of the first reports that contributed to grain size enlargement is the traditional technique of substrate heating during laser irradiation [2.13]. It reduces the external vertical heat flux $q_{sub}$ from the molten Si pool towards the substrate, reducing $R_{Vsl}$ and produces grain sizes of 200-300 nm. However, in case of glass, the substrate cannot be heated to a temperature higher than 500 °C, which limits the utilization of this method. Another classical approach is the so-called "bridge method" [2.14]. In this technique the substrate is removed and an a-Si film stays on a thin $SiO_2$ membrane, which acts as the ideal thermal insulator. However, this technique has no practical use for industrial applications due to the lack of mechanical strength of the thin membrane, despite the several 10-μm large grains and very high electron field effect mobilities (up to 800 $cm^2/V{\cdot}s$) that were obtained.

Other techniques for elongating the melt-regrowth duration of the Si film on the glass substrate are the dual-beam method [2.15] and the double-pulse method [2.16]. In the dual-beam method, a three-layered structure of Si/insulator/metal on glass is irradiated from both sides. The metal underlayer is heated to the temperature exceeding the melting point of Si, resulting in a small temperature gradient across the insulator. In this way the external heat flux $q_{sub}$ towards the substrate is reduced, resulting in an average grain size of 0.8 μm.

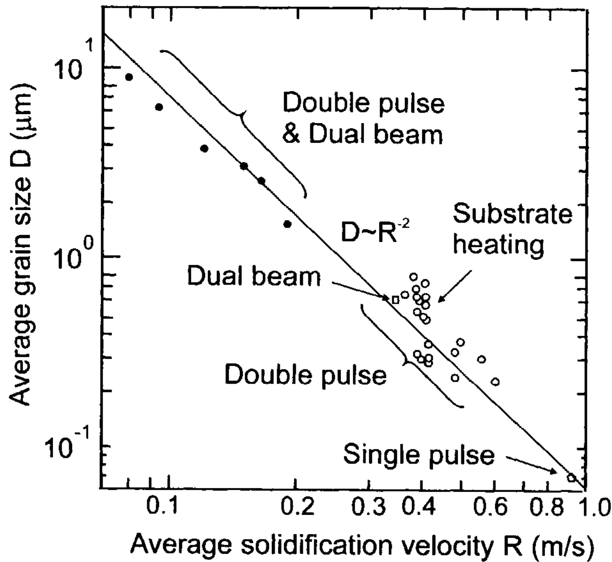


*Fig. 2.10* *Published results on average grain sizes as a function of solidification velocity (before 1995). Reprinted from* [2.12].

In the double-pulse method, two excimer-laser light pulses irradiate the Si surface successively, with a very short time interval, elongating the melt-regrowth duration of Si film, which results in 0.8-µm large grains. However, this technique is limited by difficulty in controlling the characteristic time jitter of the excimer laser, therefore making it difficult to control the time interval between pulses. Recently a feedback process was developed to solve this problem [2.17].

The two techniques are merged in the double-pulse and dual-beam method [2.18]. A single crystalline Si TFT with an electron field effect mobility > 460 $cm^2V{\cdot}s$ and an off-current less than $10^{-13}$A was fabricated in a 10-µm large Si grain [2.19]. The technological limitations are the same as those in the previous case.

Another approach to enlarge the grain size as well as to improve control of the crystallographic orientation is multi-shot irradiation [2.20]. 3 and 4.5-µm large Si grains with an (111) orientation were obtained by 64 and 128 irradiation shots, respectively. The substrate temperature was kept at 400 °C. The extended lateral grain growth and orientation were explained by surface free energy anisotropy, i.e., the (111) texture minimizes the energy of the Si-free surface. The mechanism of this film texture formation will be discussed in Chapter 2.7. Low process throughput and the necessity of substrate heating are the drawbacks of this process.

### 2.5.3 Approach in this study: Concept of c-Si single island enlargement

The method to obtain large Si islands used in this study is schematically illustrated in Fig. 2.11. As can be seen from this cross section, the sample structure consists of three layers, deposited on a transparent glass substrate. The bottom layer is usually a highly conductive metal. An insulating film with low thermal conductivity $k_{sub}$ is used as an intermediate layer (e.g. $SiO_2$). The a-Si layer is deposited on top. Dual-beam laser irradiation is carried out to irradiate both the top a-Si and bottom metal layers simultaneously. Due to the laser energy irradiated at the top a-Si layer, it starts to melt, while the bottom layer is heated up significantly by the backside irradiation. In this way the high external heat flux $q_{sub}$ from the molten Si layer towards the glass substrate is suppressed by a small vertical temperature gradient $dT/dz$ across the underlying insulator:

$$\frac{\partial T}{\partial z} = \frac{T_{ins} - T_{con}}{h_{ins}} \tag{2.16}$$

where $T_{ins}$ is the temperature at the Si/insulator interface, $T_{con}$ is the temperature at the insulator/conductive layer interface and $h_{ins}$ is the insulator thickness. By increasing the thickness $h_{ins}$ and the thickness of a-Si layer on top, one can decrease $R_{Vsl}$ and the cooling rate $dT/dt$ significantly. Consequently, the nucleation onset $t_{hom}$ during lateral grain growth, initiated when the supercooling temperature of the melt pool $\Delta T$ reaches its critical value of homogeneous nucleation $T_{hom}$, is delayed. As a result, the final Si island size $d_L$ increases due to the extended duration of the molten state of the nuclei-free Si pool, as follows from Eq.(2.15) [2.21].

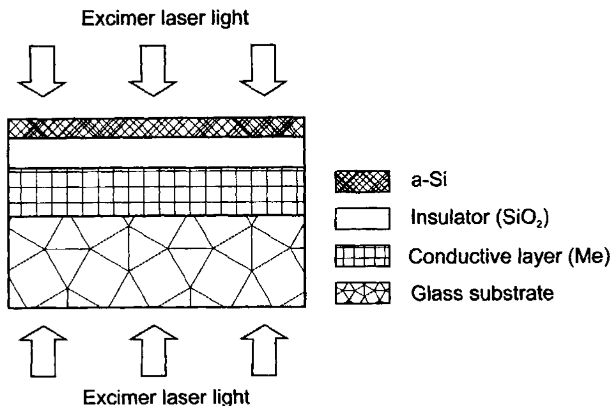


*Fig. 2.11 Dual-beam method for enlargement of single c-Si islands.*

## 2.6 Location control of large c-Si single island

### 2.6.1 Theory and requirements

As was shown in the previous Chapter 2.5, large c-Si islands in the TFT active channel region significantly improve the resulting device performance. However, to ensure that these c-Si islands are located within the TFT channel region, their location should be controlled. This condition will simultaneously affect the device-to-device uniformity of TFT characteristics.

The location of c-Si islands can be controlled by intentional manipulation of *complete and incomplete melting* of the Si film at pre-designated locations. The incomplete melting of the explosively crystallized regions will result in small-grained partial melting or large-grained near-complete melting polycrystalline islands. The complete melting of the remnant cluster regions may lead to copious-nucleation-initiated solidification of the grains. As a result, a fine-grained polycrystalline microstructure will be formed. The spatial manipulations of complete/incomplete melting areas should utilize the following physical phenomena of laser-melted Si film:

1. The Si film microstructure left after explosive crystallization
2. The number (size) of remnant clusters initiating the growth, in contact with the liquid at the start of solidification
3. Lateral and vertical grain growth kinetics in the supercooled Si pool

The explosive crystallization mechanism is important, since it inevitably occurs at the onset of any Si transformation induced by pulsed laser. As was shown in Chapter 2.1, the lateral grain growth occurs from *randomly located* remnant defect-free clusters, originated from explosive crystallization. They act as seeds for subsequent liquid-phase epitaxial regrowth. Therefore, in order to control the starting position of laterally grown grains, one needs to determine the location of such remnant Si clusters in the nuclei-free molten Si pool by spatial manipulations of complete/incomplete melting areas.

These spatial manipulations of complete/incomplete melting can be accomplished via a number of different means, which are reviewed in the next section.

### 2.6.2 Reported methods of 2D location control

The starting position of the grain growth can be controlled by the following approaches:

(1) laser beam modifications (2D);
(2) capping layers (1D);

(3) spatial geometry variation of the sample (2D).

Laser beam modification is utilized in the so-called advanced phase-modulated excimer laser annealing method (APMELA) [2.22]. The steep temperature gradient along the surface is produced by non-uniform laser irradiation, which is controlled by a phase-shift mask. This phase-shift mask usually consists of periodic and circular (or square and so on) step patterns, which induce interference effects and consequent light intensity variation on the sample surface. As a result, the part of the Si film irradiated with the high-intensity laser beam is melted, while that irradiated with the low-intensity beam remains solid and initiates subsequent lateral grain growth at the pre-designed position. The obtained grain size is approximately 3 μm. However, the depth of focus (DOF) in this method is very short, due to the small distance between the phase-shift mask and the sample (typically between 0.2-0.4 mm), in order to avoid oscillating laser intensity distribution [2.23, 2.24]. The latter makes it difficult to have a uniform distance between the phase-shift mask and the sample over a large area, reducing the uniformity of the laser intensity. Difficulties in aligning the mask with the sample also restricts the applicability of this process.

Another variant of laser beam modification is the Sequential Lateral Solidification (SLS) technique, which is also capable of 2D location control [2.25]. In this method a Si film is irradiated with chevron beamlets, formed by projection optics. Epitaxial regrowth by seeding from the remnant solid seed (> 10 μm) is induced via complete melting and micro-translating the sample after each pulse. However, this technique requires very expensive laser-beam projection equipment coupled with an accurate stage translator since the translation distance from pulse to pulse is less than the single pulse lateral overgrowth distance (typically in the order of 0.75 μm), which also limits the throughput of the process.

Capping layers, including antireflective $SiO_2$ layers [2.26,2.27] or reflective metal layers [2.27] on top of an laser irradiated Si film, are used for 1D location control. The principle lies in spatial modulation of the heat losses from the irradiated a-Si film towards the thermally conductive capping layers. In this way lateral growth is triggered when the more heated area (i.e., the capped region, for antireflective coatings or the uncapped region, for reflective coatings) is fully melted. Location control is determined by the position of the less heated region, which remains solid or partially melted for reflective and antireflective layers, respectively. The disadvantages of this method are that only 1D location-control is possible, and that it suffers from impurity contamination in the capped Si film, caused by high-temperature laser irradiation of the capping layers. Moreover, the removal of capping layers is not straightforward.

Spatial geometry variation of the sample (i.e., substrate) is used in the grain-filter method [2.28]. It utilizes geometric selection through a vertical narrow constriction, which is formed by a locally increased thickness of the a-Si film in

the narrow holes etched in the underlying insulating layer. A small unmolten Si region, which remains solid at the bottom of such an hole after laser irradiation, initiates the subsequent grain growth. The primary growth is vertical grain growth; the subsequent growth is lateral. The method's disadvantages are a high planar defect generation rate, and that it is hardly implemented in current TFT production due to the necessity of sub-micron photolithographic resolution, while the current minimum feature size in the LCD industry is approximately 3 µm.

It is worth noticing that all 2D location control techniques based on spatial variation of the sample have the highest accuracy, since the sample topology (i.e., subsequent grain position) is defined via lithographic steps.

### 2.6.3 Approach in this study: DBTOP method

In order to employ the established 2D location-control principles, we utilize spatial geometry variation of the sample. This approach allows us to manipulate the control of *complete* and *incomplete melting* of designated areas of Si film. Preliminary experiments [2.15] in which dual-beam laser irradiation was employed for grain size enlargement of thin Si films produced single-crystal regions that are approximately 1 µm in size, which is not sufficiently large for complete inclusion of an entire TFT device.

The method used to control the position of the large c-Si island in this study is schematically illustrated in Fig. 2.12a. This method is commonly referred to as the dual-beam with thick oxide portion (DBTOP) method and was introduced in 1997 [2.29]. As can be seen from the cross section in Fig. 2.12a, the sample structure is almost the same as that from the dual-beam method for grain size enlargement shown in Fig. 2.11. Not only the conventional dual-beam method was used; we also selectively increased the thickness of the intermediate insulating layer, resulting in a locally thick part (*bump*). The local thickness variation of the underlying insulating layer produces an intentional temperature non-uniformity along the Si/insulator interface. As a result of an increased thermal capacitance of the thicker bump region, the lowest temperature always occurs at the center of the bump, increasing towards the surroundings during and immediately after laser irradiation, schematically shown in Fig. 2.12b.

The crux of the DBTOP method is accurate control of the location of the remnant c-Si cluster, produced by explosive crystallization, in a molten Si pool via this appropriate *3D concave temperature profile*. However, the intentional introduction of a low-temperature area, determining the incomplete melting region is, in itself, a necessary but insufficient condition. This low-temperature area should be small enough so that only *one single c-Si seed* from the cluster remains.

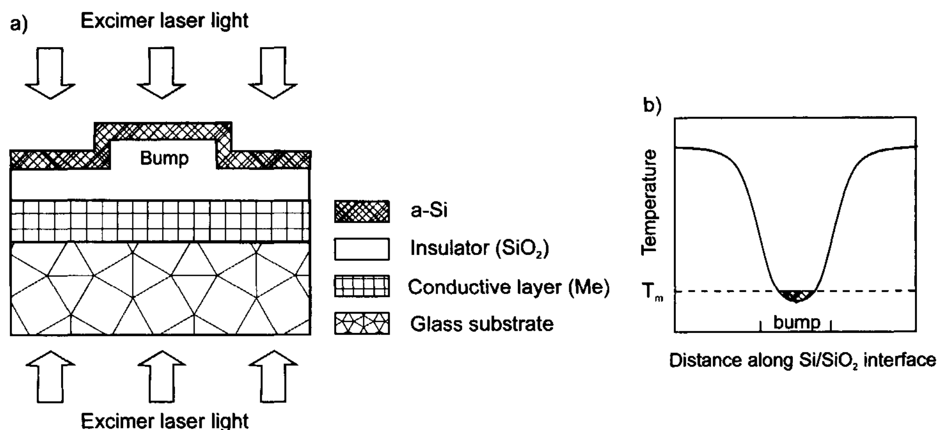


*Fig. 2.12* *a) Schematics of DBTOP method b) Temperature profile along $Si/SiO_2$ interface immediately after laser irradiation.*

# 2.7 Crystallographic orientation control of large location-controlled c-Si single island

## 2.7.1 Theory and requirements

In general, the texture and the orientation of laser irradiated poly-Si film are determined by the nucleation, coalescence and post-coalescence growth and grain boundary motion during these processes. The surface and interface energies, stress in thin film, and anisotropic growth velocities are the key parameters, determining the crystallographic orientation. The addition of metallic impurities to a-Si precursor film lowers the energetic barrier for crystallization and initiates epitaxial growth, which also leads to the required crystallographic orientation.

### 2.7.1.1 Nucleation and Coalescence

In a highly supercooled Si melt, nuclei with high surface and interface energies, $\gamma_s$ and $\gamma_i$, respectively, will shrink while nuclei with low energies will

grow further [2.32]. Such nuclei have an exponentially higher probability of reaching a supercritical radius compared to nuclei with other orientations. Therefore in the resulting grain population the grains with low $\gamma_s$ and $\gamma_i$ will dominate. These grains have high volume to surface and interface energy ratios, i.e., large Si islands with orientations leading to the minimum energies $\gamma_s$ and $\gamma_i$.

As islands coalesce, they can undergo an accelerated coarsening process (i.e., growth of islands at the expense of other islands, which have a higher energy per atom) with material exchange through self-diffusion on the particle surfaces, and through grain boundary motion. Consider the planar view of an SLG structure shown in Fig. 2.13.

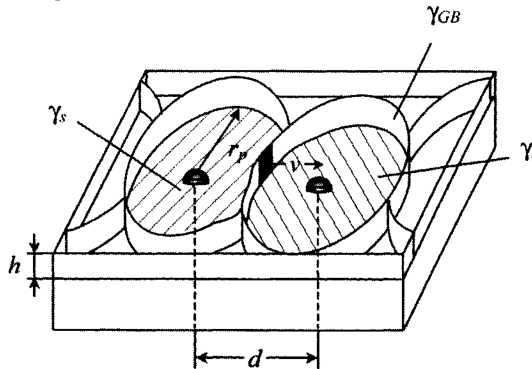


*Fig. 2.13 Schematic view of coalescence during SLG growth.*

Most grain boundaries in such a structure are circular in shape and have a predominant radius of curvature $r_p$ in a film with thickness $h$, expressed as [2.32]:

$$r_p = \frac{h\gamma_{gb}}{\Delta\gamma_s + \Delta\gamma_i} , \tag{2.17}$$

where $\Delta\gamma_s$ and $\Delta\gamma_i$ are the differences in surface and interface energies, respectively, for the grains colliding at the boundary of energy $\gamma_{gb}$ [2.33]. When grain boundaries move, they move so as to minimize the curvature, such that the boundary velocity $v$ will be given by:

$$v = \mu\left(\frac{1}{r_i} + \frac{1}{r_p}\right) \tag{2.18}$$

where $\mu$ is the product of the boundary mobility $M$ and the grain boundary energy $\gamma_{gb}$, and $r_i$ is the predominant in-plane (out-of-plane) radius of the new curvature. The grain growth in thin film results in a decrease in the total grain

boundary area, and therefore, the total grain boundary energy. Surface and interface energy minimization during grain growth in thin films can therefore lead to the development of restricted crystallographic orientations or textures.

### 2.7.1.2 Post-coalescence

Grain selection during lateral and vertical regrowth of laser-irradiated Si film can be attributed to the:

(a) dependence of the surface free energy $\gamma_S$ on crystallographic planes;

(b) crystallographic anisotropy of the solidification velocity.

Figure 2.14 shows two common microstructures of laser-crystallized Si film. In the first case, the grain size $d_L$ is uniform through the thickness $h$ of the film, and is a few times larger than the film thickness (for example, SLG pattern). In the second case, $d_L$ is small at the film substrate interface and increases through the film thickness (i.e., Si regrowth from the partial melt).

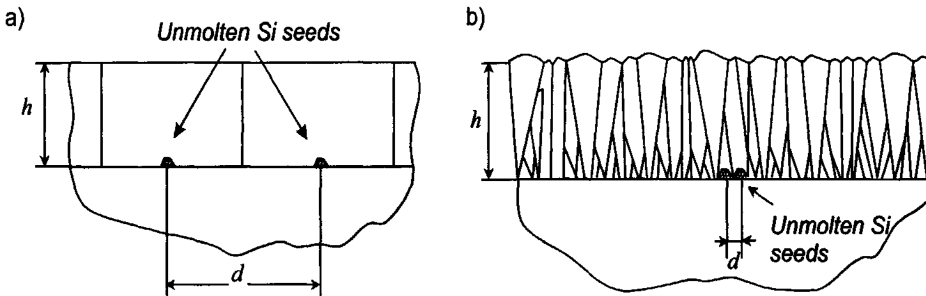


*Fig. 2.14 Schematic cross-sectional view of poly-Si film with (a) SLG-equiaxed and (b) non-equiaxed (regrowth from partial melt) columnar grain structures.*

The equiaxed SLG columnar structures, obtained after single shot irradiation, generally exhibit a random crystallographic orientation, as will be shown in Chapter 6. With multiple shot irradiation, it is likely that the grain texture and orientations are influenced by the difference of the surface free energies $\gamma_S$. In case of the observed {111} texture of SLG after multi-shot irradiation [2.34, 2.35, 2.36], the following explanation applies. For solid phase crystallization (SPC) of Si, it was shown by Haji et al. [2.39] that the occurrence or non-occurrence of a texture depends on the ratio of the mean distance between nuclei $d$ and the film thickness $h$. For $d >> h$ (Fig. 2.14a), a {111} texture is obtained, while for $d << h$ (Fig. 2.14b), no preferred orientation develops. This is explained by the crystallographic anisotropy of the growth rate $v_{Gr}$ perpendicular to the substrate of the low-index planes in silicon, i.e., $v_{Gr}$ {111}< $v_{Gr}$ {110}< $v_{Gr}$ {100} due to the difference of the surface free energies of these planes. According to this model, $d$

>>*h* leads to the formation of a {111} texture because the grains with an orientation which permits a fast growth rate parallel to the substrate (i.e., <111> grains) are extended laterally at the expense of the differently oriented grains (i.e., coarsening). In other words, grains oriented in a fast growth direction solidify rather fast and can overgrow other grains through the occlusion of slow and fast growing grains.

In the case of *d*<<*h*, no preferential orientation appears, because the crystallites have the same chance to grow in any direction. This theory can explain the resulting {111} texture in SLG regime after multi-shot irradiation, which exactly corresponds to the situation *d* >>*h*.

### 2.7.1.3 Metal-induced crystallization

An alternative approach to crystallographic orientation control is the addition of a small amount of metallic impurities to a-Si precursor film - so-called metal-induced crystallization (MIC). Originally this method was used to decrease the thermal budget necessary for the transformation of a-Si to poly-Si by solid phase crystallization (SPC). It was shown that by inserting a thin, discontinuous Pd layer between the substrate and the amorphous-Si precursor, complete crystallization could be obtained within 2 hours at 600 °C [2.46]. Pd induced crystallization was one of the first MIC efforts; recently metals such as Au [2.47], Al [2.48], Sb [2.49], Ag [2.50], and In [2.51], which form eutectics with Si, or metals such as Ti [2.52], and Ni [2.53], which form silicides with Si, were added to crystallize a-Si. Some of these cases were reported to be successful in lowering the crystallization temperature down to 500 °C.

The explanation of crystal orientation control by the MIC process with silicide forming metals is as follows. The MIC process is based on the formation of Me silicide in the early stage of thermal annealing, which lowers the energetic barrier for crystallization. Its phase follows the sequence like $Me_xSi$ - MeSi - $MeSi_x$, leading to the final silicide $MeSi_x$ precipitates formation and their subsequent migration into a-Si, leaving c-Si trails behind [2.62]. The silicide formation proceeds sequentially, not simultaneously. Usually this $MeSi_x$ precipitate can be formed at relatively low temperatures between 300 - 400 °C on a-Si film in the initial stage of thermal annealing

An extension of MIC process was achieved by selective deposition of the same silicide-forming metals, such as Pd [2.55], Ti or Ni [2.56, 2.57, 2.58], on a-Si thin films. It was found that due to the lateral migration of these metals, they induce crystallization of a-Si outside of the metal coverage, enhancing the grain size. This phenomenon has been called metal-induced lateral crystallization (MILC).

### 2.7.2 Methods of crystallographic orientation control

Some researchers already observed a preferential orientation of the grains in laser-crystallized poly-Si films. A microstructure exhibiting (111) crystallographic orientation was obtained by multiple shot excimer laser irradiation (i.e., 64 and 128 shots) of 50 nm thin Si with substrate heating at 400 °C [2.34]. Loreti et al. confirmed a (111) texture for a 80 nm thin Si film on quartz substrate by multiple shot irradiation [2.35]. The substrate temperature was kept at 340 °C. Another paper reports a (111) preferential orientation for thicker films up to 100 nm on quartz crystallized in the SLG regime also by multiple shot excimer laser irradiation [2.36]. This experiment was performed in vacuum at room temperature.

The nickel-induced crystallization (NIC) samples with UV-assisted anneal showed dominant orientations of (110) and (111) [2.54]. The (110) preferentially oriented growth of nickel-induced lateral crystallization (NILC) silicon films has been reported by several groups [2.59, 2.60, 2.61].

### 2.7.3 Approach in this study: NIC method

In order to employ crystallographic orientation control of large location-controlled singe c-Si islands, the NIC method has been utilized in this thesis. It was already discussed in Section 2.7.1.3 that the NIC process is based on the formation of Ni silicide in the early stage of thermal annealing. Its phase follows the sequence $Ni_2Si$ - NiSi - $NiSi_2$, leading to disilicide precipitate formation and their subsequent one-dimensional migration [2.62]. The silicide formation proceeds sequentially, not simultaneously. A $NiSi_2$ precipitate can be formed at a temperature as low as 350 °C on a-Si in the initial stage of thermal annealing and acts as a nucleus of Si. The disilicide precipitates are regular octahedra bound by eight {111} faces, and the lattice mismatch between Si (111) and $NiSi_2$ (111) is only 0.4% [2.63]. As a result, crystalline silicon grows epitaxially on one of eight {111} faces of the nickel disilicide precipitates, forming a needle-like morphology. The needle-like crystallite grows as a result of the diffusion of the Ni atoms in $NiSi_2$ toward the amorphous silicon region, because the free energy of the Ni atom at the interface between $NiSi_2$ and c-Si is higher than that of the Ni atom between the $NiSi_2$ and a-Si [2.63]. As was explained before, the crystallization always occurs along the <111> directions, because the other configurations diminish themselves. Therefore, the crystallites orient themselves along the [110] direction normal to the film surface.

The method to control the crystallographic orientation of the large location-controlled single c-Si islands used in this study is schematically illustrated in Fig. 2.15. As can be seen, the sample structure consists of three layers, deposited

on a 100 mm c-Si (100)-oriented wafer. The bottom layer in contact with a-Si film is usually a non-catalytic, chemically stable and structurally amorphous layer (e.g. $SiO_2$). Layer of the silicide-forming metal (e.g. Ni) is deposited on top of a-Si film.

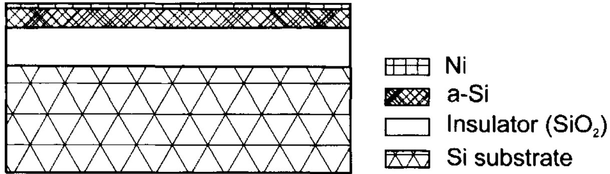


*Fig. 2.15 Schematics of NIC method.*

# Chapter 3

# Technological fabrication aspects

This chapter gives a brief overview of the technological fabrication of the structures used in this study. In particular, it explains in detail the choice of the metal layers for the DBTOP laser processing and their characterization. It also describes the laser set-up of the dual-beam irradiation method realized with only one laser beam.

## 3.1 Experimental structures

Figures 3.1 and 3.2 show the detailed schematics of the sample structures used in this study. The structure used to enlarge the size of Si grains with single laser beam is shown in Fig. 3.1. It consists of two planar layers, i.e., a-Si / $SiO_2$ on a Si substrate.

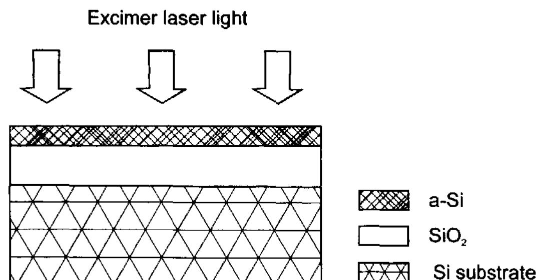


*Fig. 3.1 Structure for grain size enlargement.*

The DBTOP structure consists of tri-layer islands, i.e., a-Si / $SiO_2$ / metal stacks on a glass substrate, as shown in Fig. 3.2a. The underlying patterned

oxide forms an array of bumps for location control of the c-Si islands. The structure in Fig. 3.2b was used to test the applicability of different metal types and also to determine the actual laser energy density.

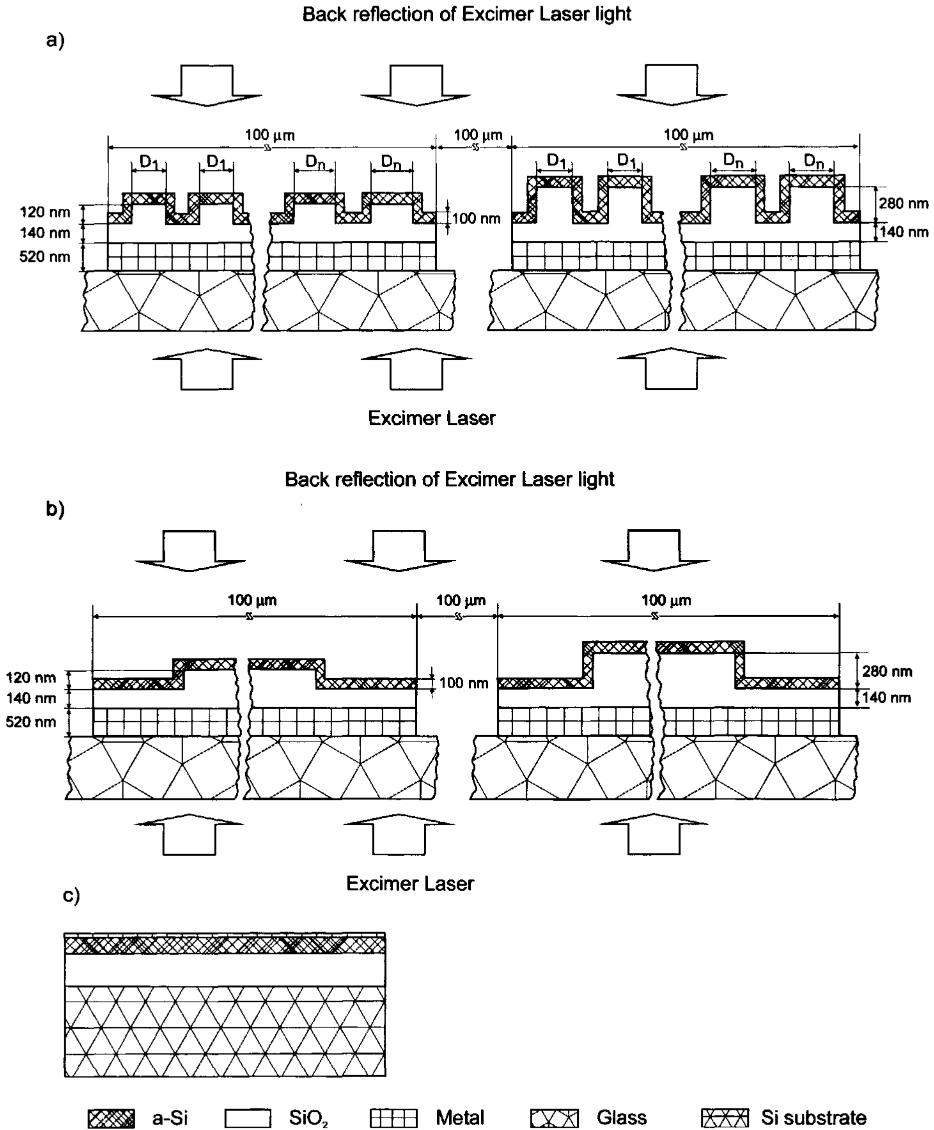


*Fig. 3.2* *a) DBTOP process structure b) DBTOP test structure c) NIC structure.*

The structure used to control the crystallographic orientation of the Si grains by nickel-induced crystallization is schematically illustrated in Fig. 3.2c. It consists of a discontinuous layer of Ni (i.e., Ni islands) deposited onto a-Si / $SiO_2$/Si substrate structure.

## 3.2 Substrate

A c-Si (100)-oriented wafer with a thickness of 525 µm and diameter of 100 mm was used as a substrate material for experiments with the single beam and NIC. A Hoya NA35 alkali-free glass wafer with a thickness of 500 µm and a diameter of 100 mm was used as a substrate material. Its transmittance at 308 nm wave length is 83%, the substrate melting temperature is approximately 730 °C and its temperature coefficient of the linear expansion (TCLE) at RT is $43\times10^{-7}$ K.

## 3.3 Metal layer

The principle of the DBTOP method, described in Chapter 2.6.3, implies the following requirements for the thermo-physical properties of the metal film:

a) high melting temperature $T_m$

b) high propagation velocity of a temperature wave, i.e., thermal diffusivity $a$, expressed as:

$$a = \frac{k}{C} \tag{3.1}$$

where $k$ and $C$ are the heat conductivity and the heat capacity of the material. From a technological point of view, deposited metal films should satisfy the following criteria:

a) good adhesion to the underlying glass substrate at all process temperatures;

b) high thickness uniformity across the wafer;

c) small reflection coefficient;

d) low built-in stresses;

e) TCLE that matches that of the glass substrate. TCLE is defined by:

$$TCLE = \frac{1}{l}\frac{\partial l}{\partial T} \tag{3.2}$$

where *dl/l* is the relative lengthening of the body.

Based on the thermo-physical properties available in the literature [3.1], the following metals were considered for DBTOP application: Cr, Ti, W and Al. The temperature-dependent heat capacity *C*, thermal conductivity *k* and melting temperatures of these metals are shown in Fig. 3.3, their thermal diffusivity and TCLE values are shown in Fig. 3.4 and Fig. 3.5, respectively. As follows from Fig. 3.3, Al has the highest thermal conductivity and diffusivity values, but the lowest melting temperature. This can cause problems during deposition of subsequent layers and during laser crystallization.

Tungsten was also considered a good candidate, despite the slightly lower value of *a*, but it has the highest melting point; one of 3695 K. Cr and Ti have reasonable characteristics, although worse than those of Al and W. Different alloys based on these metals, such as TiW and TiN, should also have thermal properties suitable for DBTOP application. Ni was used to control the crystallographic orientation of the c-Si islands.

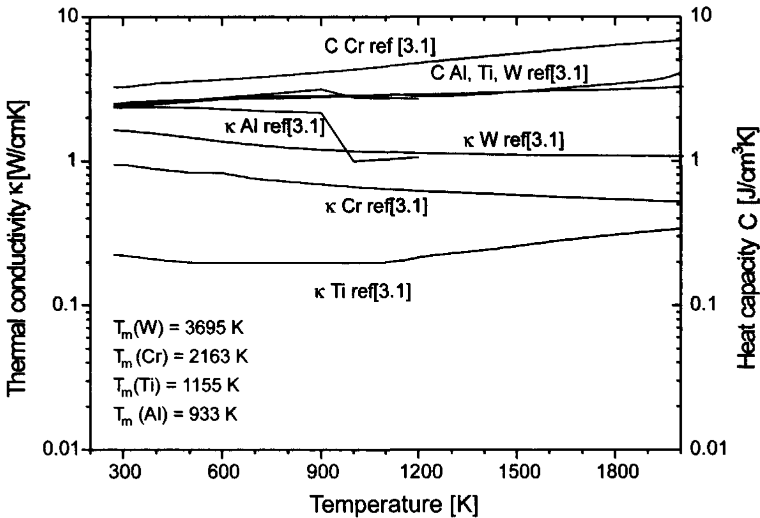


*Fig. 3.3 Temperature-dependent heat capacity, thermal conductivity and melting temperatures of Al, W, Ti and Cr.*

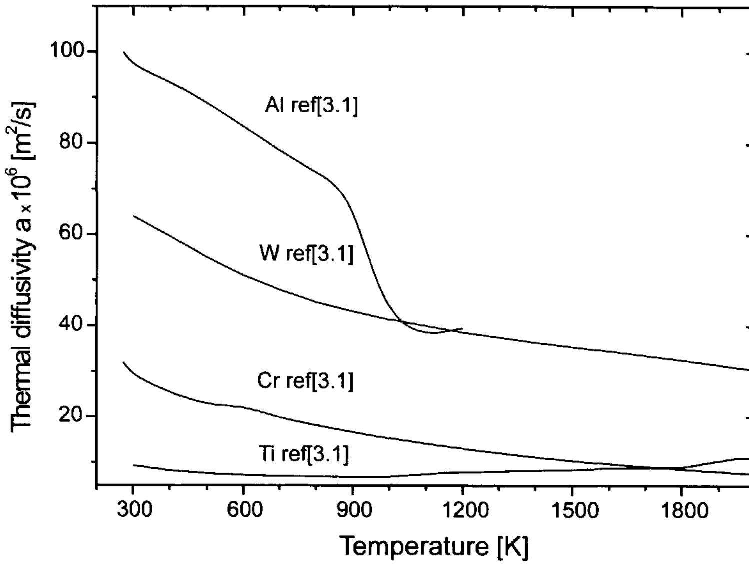


*Fig. 3.4* *Temperature-dependent thermal diffusivity of Al, W, Ti and Cr.*

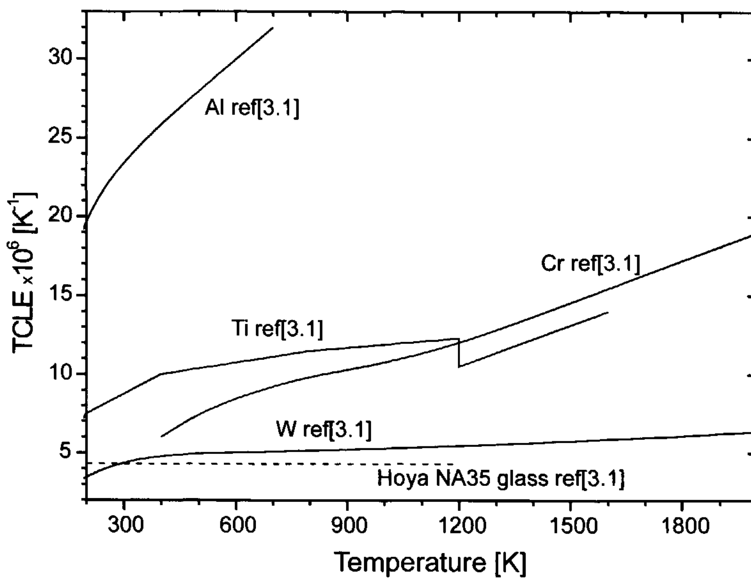


*Fig. 3.5* *Temperature dependence of TCLE for metal films used.*

## 3.3.1 Metal characterization

In order to investigate and optimize the properties of the metal films used in the DBTOP method, several different deposition techniques as evaporation and sputter coating of 520-nm thick metal film were used. The process details can be found in Appendix (Tables 7.1 and 7.2).

### 3.3.1.1 Adhesion at room temperature

The adhesion of sputtered metal layers must be excellent (both when deposited and after subsequent processing). Poor adhesion of the first layer (out of three to be deposited) to the glass substrate represents a potential reliability problem with the DBTOP structure. Very weak adhesion was observed for TiN and TiW alloys, deposited by magnetron and RF sputtering, respectively, which peeled off of the glass substrate after few hours. There are few factors which may influence adhesion, such as cleanness of the substrate, substrate surface roughness and built-in stress. Contamination generally results in reduced adhesion, as does an adsorbed gas layer. However, all substrates were subjected to the same standard cleaning procedure prior to metal deposition, so the contamination level should be the same. The surface roughness of the glass substrate should be the same as well, although substrates were taken from different batches. Probably, the adhesion was also influenced by deposition conditions.

### 3.3.1.2 Stress

The stress may be compressive or tensile. A compressive stress in the film bends the substrate such that it becomes convex. A tensile stress in the film bends the substrate such that it becomes concave. Highly stressed metal films in DBTOP structures are undesirable for several reasons: they are more likely to exhibit poor adhesion and may undergo cracking. The total stress in the film can be written as [3.2]:

$$\sigma = \sigma_{ext} + \sigma_{th} + \sigma_{int} \tag{3.3}$$

where $\sigma_{ext}$ is any external stress on the film, perhaps from another film, $\sigma_{th}$ is thermal stress, and $\sigma_{int}$ is intrinsic stress. Thermal stress results from the difference in the TCLE between the film and the substrate and can be given by [3.2]:

$$\delta_{th} = \left(\alpha_f - \alpha_s\right)\left(T_g - T_{mes}\right) E_f \tag{3.4}$$

where $\alpha_f$ and $\alpha_s$ are the average TCLE for the film and the substrate, respectively; $T_g$ and $T_{mes}$ are the temperatures at film growth (or deposition) and

measurement, respectively; $E_f$ is the Young's modulus of the film. The thermal stress $\sigma_{th}$ can be of either sign. The intrinsic stress depends on the film thickness, deposition rate, deposition temperature, ambient pressure, type of substrate, etc, and has not been characterized clearly so far. The stress measurements were performed with commercial laser wafer-flatness-measuring equipment called Flexus. The measurement procedure is straightforward, because it determines the bending of the substrate after film deposition by measuring the deflection of the wafer center. Stress is then calculated as:

$$\delta = \frac{E_s D}{6rt} \tag{3.5}$$

where $r$ is the measured radius of the curvature of the bent substrate, $E_s$ is the Young's modulus of the substrate, $D$ is the thickness of the substrate and $t$ is the thickness of the film. Any curvature that is inherent to the substrate must be measured before the film is deposited and added to the final measured radius of curvature. All the deposited metal films revealed stress, regardless of the method by which they had been produced. The stress measurements are shown in Fig. 3.6.

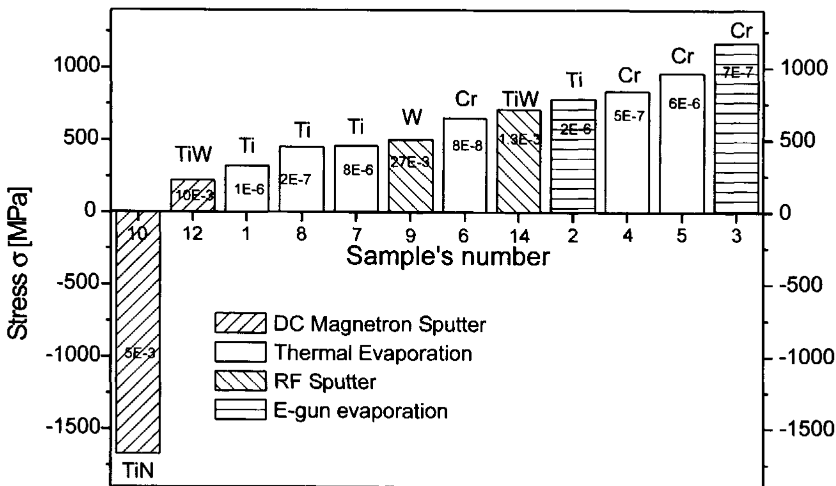


*Fig. 3.6* *Measured values of stress for several metal films deposited by different deposition techniques. Negative stress is tensile stress; positive stress is compressive stress. The process pressure [mBar] is indicated inside the bars.*

As can be seen, only one TiN layer exhibits an extremely high tensile stress of 1674 MPa, while the other films exhibit positive compressive stress, varying from 220 (TiW by magnetron sputtering) to 1170 MPa (Cr by E-gun evaporation). Obviously, bad adhesion of the TiN layer is the result of high stress. Moreover,

the layer peeled off during the standard wet cleaning procedure before oxide deposition.

#### 3.3.1.3 Adhesion at deposition temperature

The highest process temperature in the DBTOP fabrication procedure is the temperature of a-Si layer deposition of 545 °C. Therefore, adhesion of the metal films after 5 hours annealing in $N_2$ ambient at temperature of 545 °C was also tested. Several layers peeled off already during this annealing test, i.e., samples #2, 3 and 5 from Fig. 3.6. This can be explained by to the highest built-in stress in these films (i.e., 962 and 1170 MPa), and also by the higher TCLE of Ti and Cr compared with that of the glass substrate, as illustrated in Fig. 3.5. However, due to the high wafer bending as the result of the relatively high compressive stress, samples #4 and 14 from Fig. 3.6 were not applicable to the pattern transfer through conventional photolithography.

#### 3.3.1.4 Thermal stress

The metal films were consequently used for the fabrication of the DBTOP test structure, shown in Fig. 3.2b. After the structure was fabricated, it was subjected to laser irradiation in order to test if the metal layers deposited on the glass can sustain a certain laser energy $E_{SLG}$ used in DBTOP method. The $E_{SLG}$ is defined as the energy required to convert solid a-Si into a near-complete molten state, i.e., the SLG regime. Table 3.1 lists the $E_{SLG}$ values, the maximum laser energy densities $E_{crack}$ for tested metal films which led to crack appearance, and the reflection coefficients.

*Table 3.1 Maximum laser energy densities for tested metal films and their reflection coefficients.*

| # | Me | $E_{SLG}$ [mJ/cm$^2$] | $E_{crack}$ [mJ/cm$^2$] | Refl. coef. |
|---|---|---|---|---|
| 1 | Ti | 537 | 520 | 0.20 |
| 6 | Cr | 630** | 490** | 0.32 |
| 7 | Ti | 553 | 513 | 0.23 |
| 8 | Ti | 546** | 555** | 0.21 |
| 9 | W | 570 | 578 | 0.27 |
| 11 | Al (mirror) | --- | --- | 0.94 |
| 12 | TiW | 557** | 674** | 0.21 |
| xx | Si (mirror) | --- | --- | 0.6 |

** Oxide thickness was 160 nm. ** Values were obtained by R. Ishihara.*

As follows from Table 3.1, for samples 1, 6 and 7, the cracking and peeling off of the film was observed at laser energy densities significantly lower than that required to achieve the SLG regime, i.e., Si film was still microcrystallized. Samples 8 and 9 gave no enlargement of the Si island size, which indicates that the thermal properties of these Ti and W films were not good enough for the thermal conductor, but were probably rather close to the insulator properties. Sample #12 was found to be suitable for DBTOP fabrication.

## 3.4 Oxide layer

An intermediate $SiO_2$ layer with a thickness varying from 100 nm to 1000 nm was deposited by Low Pressure Chemical Vapor Deposition (LPCVD) at a temperature of 425 °C. Table 3.2 shows the oxide thickness used in single-beam experiments.

*Table 3.2 Thickness variations of intermediate $SiO_2$ films.*

| $SiO_2$ thickness [nm] | 100 | 50 | 200 | 1000 | 1000 | 1000 |
|---|---|---|---|---|---|---|

In case of the DBTOP structure, a part of the $SiO_2$ film was then patterned into an array of circular and square bumps via conventional photolithographic procedures, which included etching of the film in hydrogen fluoride solution. The width of the circular and square bumps varied from 0.8 to 3.5 μm. The bump height and the total oxide thickness are summarized in Table 3.3. The thickness of the thin oxide was fixed at 140 nm. Another part of the $SiO_2$ film was patterned into a step-like profile, where the step height was equal to the bump height (i.e., the test structure in Fig. 3.1c).

*Table 3.3 Bump height and total oxide thickness used in the DBTOP method.*

| $SiO_2$ bump height [nm] | 120 | 180 | 230 | 280 |
|---|---|---|---|---|
| Total $SiO_2$ thickness [nm] | 260 | 320 | 370 | 420 |

In case of the NIC structure, the $SiO_2$ thickness was 1000 nm.

## 3.5 a-Si layer

An a-Si layer was deposited on the planar oxide by LPCVD using $SiH_4$ decomposition at 545 °C. The resulting a-Si layer thickness variations used in the single-beam experiment are summarized in Table 3.4.

*Table 3.4 Thickness variations of a-Si.*

| a-Si thickness [nm] | 100 | 100 | 100 | 50 | 100 | 200 |
|---|---|---|---|---|---|---|

In case of DBTOP and NIC structures the a-Si thickness was 100 nm.

# 3.6 Ni layer

5- and 20-nm thick Ni films were deposited onto the a-Si by RF sputtering. Before the wafers were loaded into the sputter machine, the native oxide on the a-Si film was removed by dipping it into dilute HF (5%). The deposition details are described in the Appendix (Table 7.2). Finally, the heat treatment was carried out at 560 °C in nitrogen ambient in a conventional atmospheric pressure horizontal furnace for different time durations (i.e., 2 - 20 hours).

# 3.7 Laser irradiation

The schematics of the dual-beam irradiation set-up are shown in Fig. 3.7.

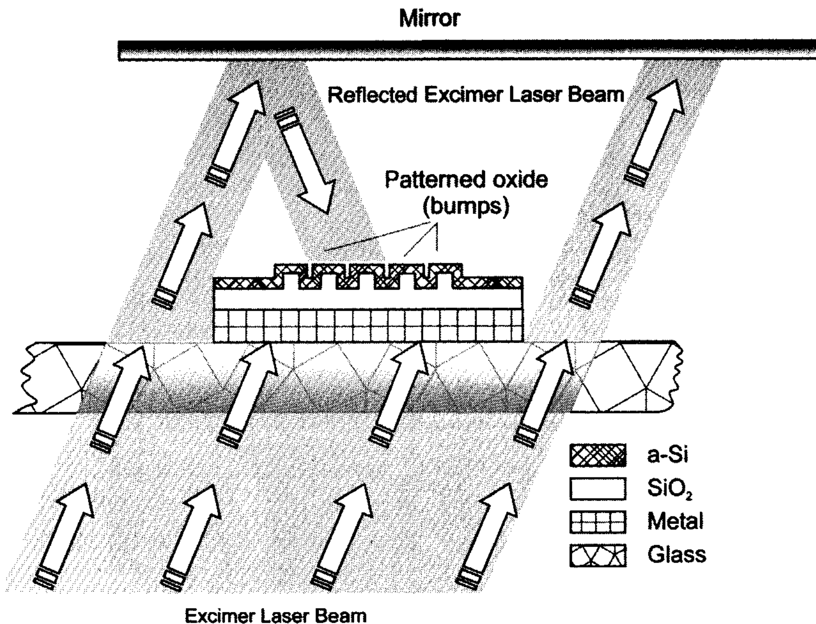


*Fig. 3.7 Schematics of dual-beam irradiation set-up.*

For dual-beam applications, the tri-layer structure was patterned to form an array of individual islands on the glass substrate with a width and length of 100 μm and 8 cm, respectively, as illustrated in Fig. 3.1b. In order to realize the dual-beam irradiation experiment with a conventional single-beam laser system (XMR 7100, 308 nm), the laser beam of the XeCl excimer laser was fired onto the backside of the structure with a single pulse duration of 66 ns. The laser light transmitted through the glass substrate was reflected back from an Al or Si mirror (94 and 60% reflectance, respectively) to the top of the sample. In this way the back side of the sample (i.e. glass substrate and metal layer), which can stand much higher temperatures than the top a-Si layer, was always subjected to a higher laser energy than the a-Si top layer. The homogenizer was used to obtain a uniform spatial profile of the laser beam. The sample was held under high vacuum (~$10^{-7}$Torr).

## 3.8 Characterization techniques

The structure and morphology of the obtained c-Si islands were characterized using scanning electron microscopy (SEM). Before the SEM characterizations, the majority of the samples was defect etched by Schimmel etching and examined via optical microscopy. The c-Si islands were etched at a lower rate than the poly- or amorphous Si fraction. The resulting topography reveals the grain boundaries and planar defects within the grain. Atomic Force Microscopy (AFM) was used to analyze the surface topology of the c-Si islands. The crystal structure and crystal orientation of the Si grains obtained by nickel-induced crystallization were observed using Transmission Electron Microscopy (TEM) and X-ray diffraction (XRD), respectively.

# Chapter 4

# *Simulation of c-Si island growth in excimer-laser-melted Si film*

This chapter introduces two different modelling tools for simulation of crystal growth in pulsed excimer-laser crystallized Si thin films: thermal and phase-field models. The thermal model describes the time- and depth-dependent temperature distribution in thin Si layers during and after laser irradiation, i.e., heating and cooling stages during the vertical growth of a c-Si island. The phase-field model describes the phase-transition kinetics and the thermal distribution of the lateral growth in the Si melt pool from the unmelted residual Si cluster after laser irradiation. Both numerical procedures are validated by comparing their predictions of the solidification behaviour with the experimental results.

## 4.1 Introduction

A detailed analysis of time-dependent solid/liquid interface profiles, nucleation kinetics and resulting temperature field distributions is required in order to investigate the crystal growth process systematically and to realize the ultimate goal: accurate prediction of the average grain size of a laser-recrystallized a-Si film. As was shown in Chapter 2.4, mathematically the growth process is modelled as a moving free boundary problem (FBP), often referred to as the modified Stefan problem (i.e., solidification with release of latent heat, Eq. (2.6), (2.7).

In widely used thermal models, the phase transformations are governed by thermal balance at the equilibrium transition temperature $T_m$ [4.1, 4.2, 4.3,].

These models are capable of simulating the interplay between heat transport in the bulk phases and at the crystal/melt interface. In capillary [4.4] and kinetic [4.5, 4.6, 4.7, 4.8, 4.9] models the temperature fields in each phase satisfy a heat diffusion equation and are coupled at the unknown crystal/melt interface. Coupling is realized through the boundary conditions that account for conservation of energy and relate the interface temperature to the thermodynamic melting point by accounting for the effects of capillarity or interface kinetics. The former implement the presence of excess interfacial free energy, which shifts the local thermodynamic equilibrium; the latter deals with the dynamical rearrangement of atoms or molecules from one phase to the other.

Generally, pure thermal or kinetic models, utilizing only solidification rate gradients, cannot be used to represent an interface morphology in the case of unstable growth fronts, e.g. solidification into supercooled melts. These models do not contain any physical length scale information. This information is provided by the interfacial energies, which therefore cannot be neglected. However, a pure thermal model can be used to simulate the vertical-regrowth solidification mechanism, because it effectively provides:

1. an accurate temperature distribution during and at the end of the laser pulse, which describes the shape of unmelted residual Si clusters;
2. the vertical solidification velocity $R_{Vsl}$ and the cooling rate $dT/dt$ during solidification;
3. the onset of homogeneous nucleation $t_{hom}$, and as a result, the duration of the lateral growth of the c-Si island and its final size $d_L$.

Taking curvature effects into account is in general a non-trivial problem because of the necessity to track and describe the interface for every possible topology and it has not been extended into three dimensions with perhaps one exception [4.10].

## 4.2 Experimental effect of Si film and underlying $SiO_2$ film thicknesses

The sample is a stacked structure of a planar Si film and a planar $SiO_2$ underlayer on the c-Si substrate (heat sink), which is shown in Fig. 3.1 in Chapter 3.1. The thickness of a-Si and $SiO_2$ layers was varied as shown in Table 4.1 in order to investigate their effect on the grain size of a laser-recrystallized a-Si film. The laser energy density was adjusted in such a way that the maximum grain size for each condition was obtained.

Figure 4.1 illustrates the maximum diameter of the c-Si island as a function of the Si film thickness. The underlying oxide thickness was fixed at 1000 nm.

*Table 4.1 Thickness variations of a-Si and underlying $SiO_2$ films.*

| $SiO_2$ thickness [nm] | 100 | 50 | 200 | 1000 | 1000 | 1000 |
|---|---|---|---|---|---|---|
| a-Si thickness [nm] | 100 | 100 | 100 | 50 | 100 | 200 |

As can be seen, the size of Si islands increases almost linearly with the Si film thickness, reaching in average size of 2.3 μm for a 200 nm thick Si film.

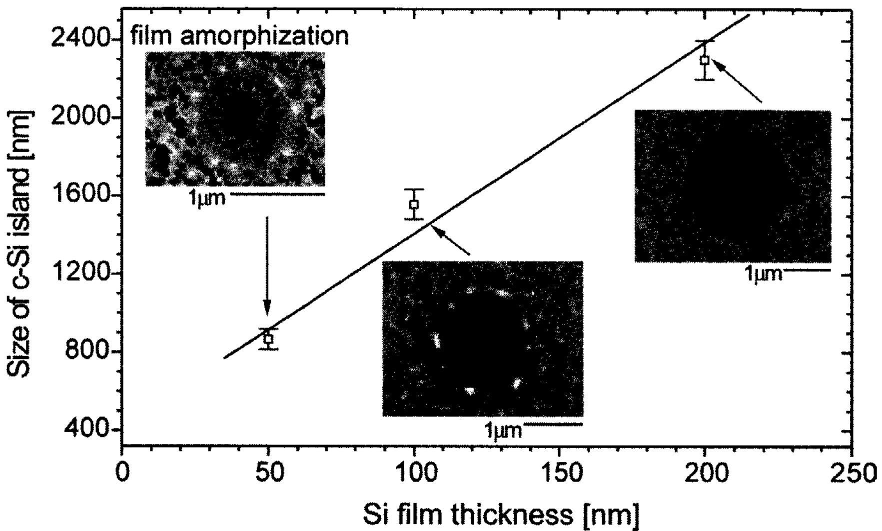


*Fig. 4.1 Maximum size of c-Si islands as a function of Si film thickness. The underlying oxide layer thickness was fixed at 1000 nm.*

Figure 4.2 illustrates the maximum diameter of the c-Si island as a function of the underlying oxide film thickness. The top Si layer thickness was fixed at 100 nm. The size of the Si island increased significantly with the oxide film thickness, reaching an average size of 1.6 μm for 1000-nm thick oxide. As depicted in the SEM images shown in Fig. 4.1 and Fig. 4.2, the final crystallized structure consists of three distinct regions: a large disk-shaped Si island with a diameter varying between 0.5 and 2.2 μm in the center; a small-grained poly-crystal ring around the disk; a fine grain region, surrounding the entire structure. The latter pattern occurs due to the significant supercooling of the Si melt pool in front of the propagating solid/liquid interface. This leads to the homogeneous nucleation of solids in supercooled Si and subsequent limitation of the size of the disk-shaped Si island. A small-grained poly-crystal ring that surrounds the single c-Si island also occurs due to the growth from nucleated solids towards the c-Si island after the homogeneous nucleation [2.10]. However,

the larger size of grains in the poly-crystal ring compared with the peripheral fine grain region is attributed to the release of the latent heat from the growing large c-Si island.

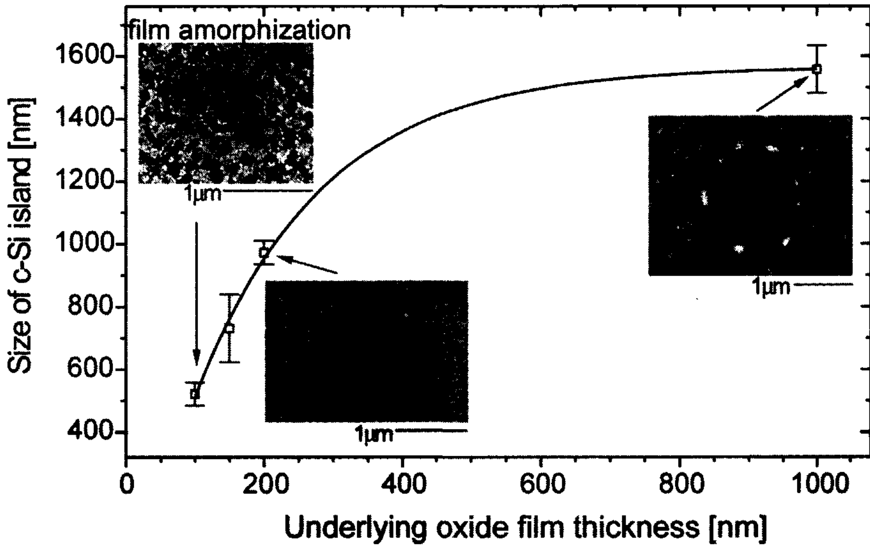


*Fig. 4.2* *Maximum size of c-Si islands as a function of underlying $SiO_2$ film thickness. The top Si layer thickness was fixed at 100 nm.*

Generated thermal energy suppresses the nucleation in the vicinity of the c-Si island as it increases the supercooling temperature in the melt, thus extending the lateral growth distance of the surrounding poly-crystal ring. The increased size of the central c-Si island with a-Si and $SiO_2$ thickness is also attributed to the delay of the homogeneous nucleation onset by suppressing the external vertical heat flux $q_{sub}$.

As can also be seen from the SEM images in Fig. 4.1 and Fig. 4.2, the c-Si islands observed at the thinnest a-Si or at the underlying $SiO_2$ layers have a black ring pattern around the central c-Si disk. This black ring depicts the remnants of the amorphous fraction, removed with Schimmel etching. As was previously reported [4.11], the growth front can break down completely with the formation of a disordered amorphous solid fraction when the crystal growth is driven at a velocity higher than the critical value of 15 m/s.

### 4.2.1 Thermal model

#### 4.2.1.1 Physical model and formulation

Generally, the 2D heat flow through an isotropic medium, which is subjected to laser irradiation and undergoes a first-order phase transition, can be described by the following heat diffusion equation:

$$C(T)\frac{\partial T}{\partial t} = \frac{\partial\left(k(T)\frac{\partial T}{\partial x}\right)}{\partial x} + \frac{\partial\left(k(T)\frac{\partial T}{\partial y}\right)}{\partial y} + S_l(x,y,t) + S_{LH}(x,y,t) \tag{4.1}$$

where $k$ is the heat conductivity, $C$ is the specific heat of the medium, and $x$ and $t$ are the space and time coordinates, respectively. The latent heat released or absorbed in phase changes at the solid/liquid interface is treated as a separate source $S_{LH}$ in addition to the one associated with the laser pulse $S_L$. In this case the thermal model is always nonlinear. Eq. (4.1) implies that the time dependence of the temperature at any point in space is given by the rates of the heat input, $S_{LH}$ and $S_L$, and the heat redistribution, *grad(k×gradT)*. Consequently, a full exploration of the time- and depth-dependent temperature field distribution (i.e., heating and cooling stages) can be obtained from the numerical solution of this equation.

It is known [4.12] that laser heating also depends on the optical absorption coefficient $\xi$ and on the heat diffusion length $l_\tau$ as:

$$l_\tau = \sqrt{2D\tau_p} \tag{4.2}$$

where $D$ is the thermal diffusivity and $\tau_p$ the interaction time between the laser and the irradiated surface, i.e., the pulse length. There are two limit cases depending on ratio between $\xi$ and $l_\tau$:

$$\begin{aligned} &1)\quad l_\tau > \xi^{-1} \\ &2)\quad l_\tau < \xi^{-1} \end{aligned} \tag{4.3}$$

In the first case the laser pulse behaves like a surface source:

$$S_L = (1-R)I_0(y,t) \tag{4.4}$$

where $R$ is the surface reflection coefficient and $I_0$ is the incident laser density. The average surface temperature increase in this case can be approximated as:

$$\Delta T \approx \frac{(1-R)I_0\sqrt{D\tau_p/2}}{k} \tag{4.5}$$

and

$$D = \frac{k}{C}. \tag{4.6}$$

In the second case the laser source is expressed as:

$$S_L = (1-R)I_0(y,t)\xi\exp(-x\xi) \tag{4.7}$$

and $T$ is approximated as:

$$\Delta T \approx \frac{(1-R)I_0\xi\exp(-x\xi)\tau_p}{C}. \tag{4.8}$$

In general, therefore, the surface thermal field induced by pulsed laser irradiation of Si is not only due to heat diffusion, but in some cases it also depends on the penetration depth of laser light itself. With laser pulses of the order of some tens of ns the heat diffusion length in Si is of the order of several hundred nm (i.e.,~750 nm for 66 ns laser pulse at FWHM), while the typical optical absorption depth of a-Si at wavelength of 308 nm (XeCl laser) is approximately 6 nm [4.13]. This means that for ultraviolet-waveband short-duration-pulsed lasers the energy balance near the surface of the medium can be expressed as the surface source term (Eq.(4.4)), since the influence of optical absorption is negligible.

#### 4.2.1.2 Formulation of the mathematical problem

The simulation is confined to the one-dimensional case; this simplifies the analysis and presentation of the simulation, while it does test and demonstrate the capability of the model. A schematical view of the irradiated sample structure used in this study is presented in Fig. 4.3; the physical values are summarized in Fig. 4.4 and Table 4.2. Each layer was initially subdivided into a certain amount of nodes; these nodes were consequently automatically refined in the areas with the highest thermal gradient value (i.e., adaptive mesh refinement).

The boundary and initial conditions are given as:

$$\left.\frac{\partial T}{\partial y}\right|_{y=0} = 0 \qquad \left.\frac{\partial T}{\partial y}\right|_{y=l} = 0 \tag{4.9}$$

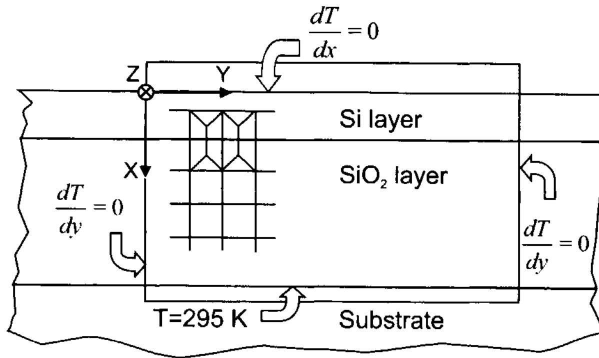


*Fig. 4.3 Schematical view of simulated structure.*

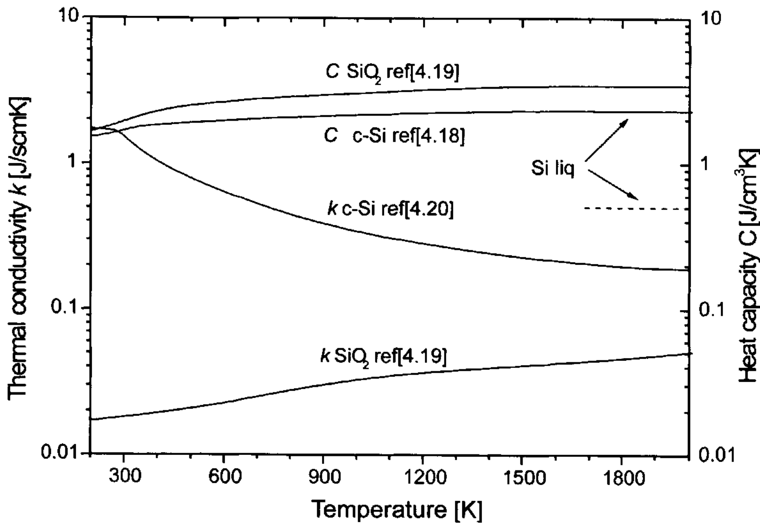


*Fig. 4.4 Thermal properties of Si and $SiO_2$ materials used in the simulation.*

*Table 4.2 Physical values used in the numerical simulation.*

| Properties | c-Si | $SiO_2$ |
|---|---|---|
| Melt temp. $T_m$ [K] | 1683 Ref.[4.16] | 1920 Ref.[4.17] |
| Heat capacity C [J×cm$^{-3}$×K$^{-1}$] | Ref.[4.18] | Ref.[4.19] |
| Heat conductivity $k$ [J×cm$^{-1}$×K$^{-1}$×s$^{-1}$] | Ref.[4.20] | Ref.[4.19] |
| Latent Heat $L$ [J×cm$^{-3}$] | 4130 Ref.[4.16] | --- |

and

$$\left.\frac{\partial T}{\partial x}\right|_{x=0} = 0 \qquad T\big|_{x=SiO_2\,/\,Substrate} = T_s \quad . \tag{4.10}$$

The initial condition is:

$$T\big|_{t=0} = T_s \tag{4.11}$$

where the initial sample temperature $T_S$ = 295 K, i.e., room temperature. Equations (4.9-4.10) account for the fact that the total energy loss at the surface due to radiation and convection to the ambient is equal to zero. This is valid for a nanosecond pulse duration since the energy loss at the surface is negligible with respect to the energy deposited by the laser pulse and diffusing towards the bulk of the sample [4.14], [4.15]. Therefore, the thin Si film surface can be assumed to be adiabatic.

The laser irradiation wavelength is 308 nm. A laser pulse of intensity $I$, which has a rectangular temporal profile, has been considered as follows:

$$I(t) = \begin{cases} I_0, & 0 \le t \le \tau_p, \\ 0, & t > \tau_p, \end{cases} \tag{4.12}$$

where the duration of the laser pulse $\tau_p$ = 66 ns at FWHM. The thin Si film is assumed to be polycrystalline in order to eliminate any ambiguity of physical parameters such as the melting point. It is worth noticing for simplicity that molten Si and solid Si have the same thermophysical values. As has been reported in [4.21], this simplification introduces only small errors.

The instantaneous position of the solid/liquid interface is obtained within the frame of the Stefan problem, Eq. (2.6), (2.7) (Chapter 2.4). It is assumed that the temperature at the solid/liquid interface, $z = h_l(t)$, is continuous and equal to the melting temperature. In this particular case it is 1683 K. Since the moving boundary is the precise site at which the phase change takes place, the latent heat of the phase transformation must be taken into account in the mathematical formulation. It assumed to be released and absorbed within the interval between 1682 K and 1684 K.

In the present analyses, the simulation is simplified and confined to the partial melting regime. In this regime the distance $d$ between the remnant c-Si seeds, left after explosive crystallization, is much less than the distance of lateral overgrowth $d_L$, i.e., $d < d_L$. This situation leads primarily to vertical grain growth, since the lateral distance is limited by the neighbouring grains, as was discussed in Chapter 2.4. Due to the close vicinity of growing grains, released latent heat of solidification keeps the temperature of molten Si above its supercooling value, thus preventing the occurrence of homogeneous nucleation.

The temperature field distribution in Eq. (4.1) was numerically obtained with commercially available MSC software [4.22] coupled with custom user subroutines. This software uses a finite element method [4.23] with an effective heat capacity approach [4.23]. The numerical solution of the model was obtained iteratively by a backward-difference time discretization scheme until the maximum calculated errors in temperature at each step became less than 1.5 K. The entire period of time was taken equal to 2 μs in this study. An adaptive time step starting from $10^{-2}$ ns and a relative error in the iteration procedure of $10^{-6}$ were chosen.

## 4.2.2 Results and discussion

### 4.2.2.1 Effect of Si and underlying $SiO_2$ thickness

Figures 4.5 shows the simulated vertical temperature profiles at the end of the laser pulse for different thicknesses of Si and $SiO_2$ layers. The surface temperature of the Si film varied from 1704 K for 50-nm thick films to 1818 K for 200-nm thick Si films. The calculated thermal gradients in molten Si vary from $480\times10^6$ K/m for 200-nm thick films to $650\times10^6$ K/m for 50-nm thick Si films. The thermal gradients in the underlying oxide vary from $6.5\times10^9$ K/m for 100 nm Si/100 nm $SiO_2$ films to $2.8\times10^9$ K/m for 200 nm Si/1000 nm $SiO_2$ films.

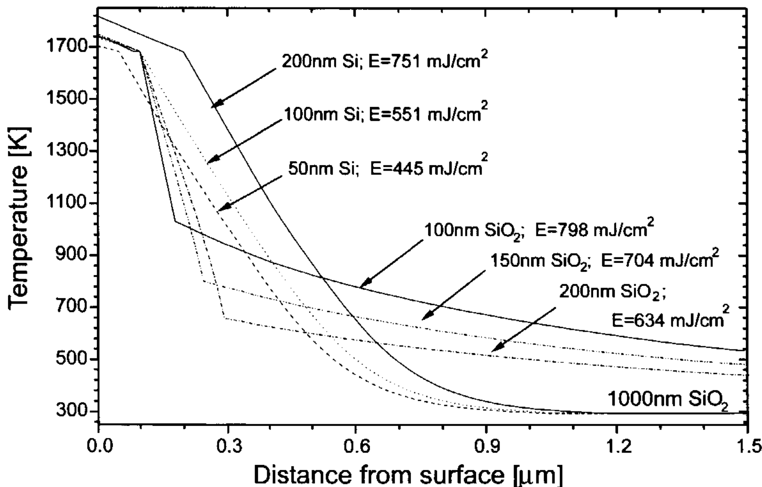


*Fig. 4.5 Simulated vertical temperature profiles after laser pulse for different thicknesses of Si and $SiO_2$ layers.*

Figures 4.6 and 4.7 show the simulated transient temperature profiles at the Si surface and at the $Si/SiO_2$ interface for different thicknesses of Si and $SiO_2$ layers.

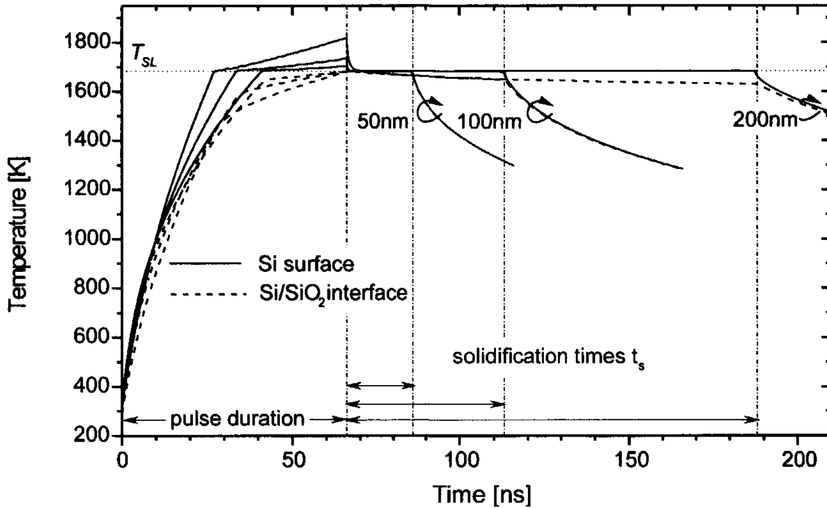


*Fig. 4.6* *Simulated transient temperature profiles at the Si surface and at the $Si/SiO_2$ interface for 50, 100 and 200-nm thick top Si layers. The thickness of the $SiO_2$ underlayer is kept at 1000 nm.*

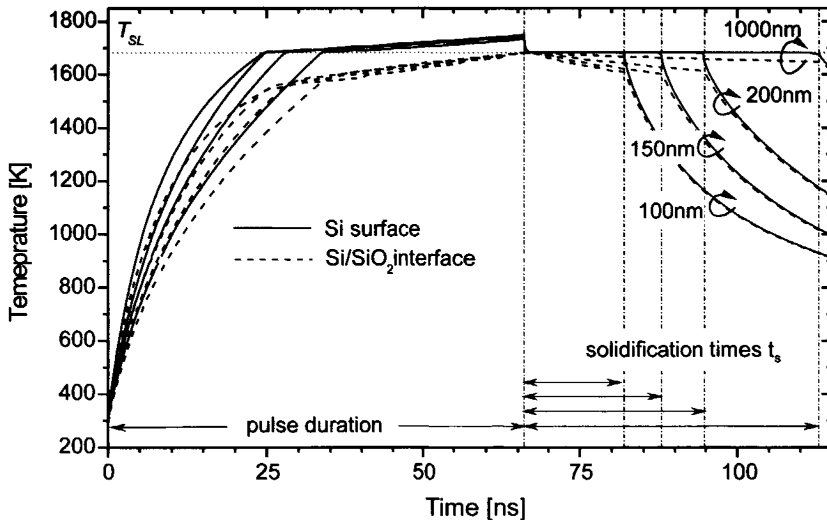


*Fig. 4.7* *Simulated transient temperature profiles at the Si surface and at the $Si/SiO_2$ interface for 100, 150, 200 and 1000 nm thick $SiO_2$ underlayers. The thickness of the top Si layer was kept at 100 nm.*

In all cases the temperature decreased rapidly after the end of a laser pulse, reaching the solid-liquid transition temperature $T_{SL}$, where the latent heat of solidification is released. Solidification times $t_s$ are derived from Fig. 4.6 and Fig. 4.7; the vertical solidification velocity $R_{Vsl}$ is calculated as:

$$R_{Vsl} = \frac{t_s}{h} \quad . \tag{4.13}$$

The times of the homogeneous nucleation onset $t_{hom}$ for a laterally solidifying c-Si island are derived from Eq. (2.14) by using $R_{Vsl}$ values. All the above-mentioned results are summarized in Table 4.3.

*Table 4.3 Solidification times, velocities and nucleation time onsets.*

| $Si/SiO_2$ thickness [nm] | $t_s$ [ns] | $R_{Vsl}$ [m/s] | $t_{hom}$ [ns] |
|---|---|---|---|
| 100/100 | 16 | 6.25 | 3.13 |
| 100/150 | 22.2 | 4.5 | 4.26 |
| 100/200 | 28.5 | 3.5 | 5.83 |
| 100/1000 | 50.0 | 2.0 | 19.4 |
| 50/1000 | 20.0 | 2.5 | 3.69 |
| 200/1000 | 125.0 | 1.6 | 25.7 |

The solidification velocities and nucleation onsets as functions of a-Si and $SiO_2$ layer thicknesses are plotted in Fig. 4.8.

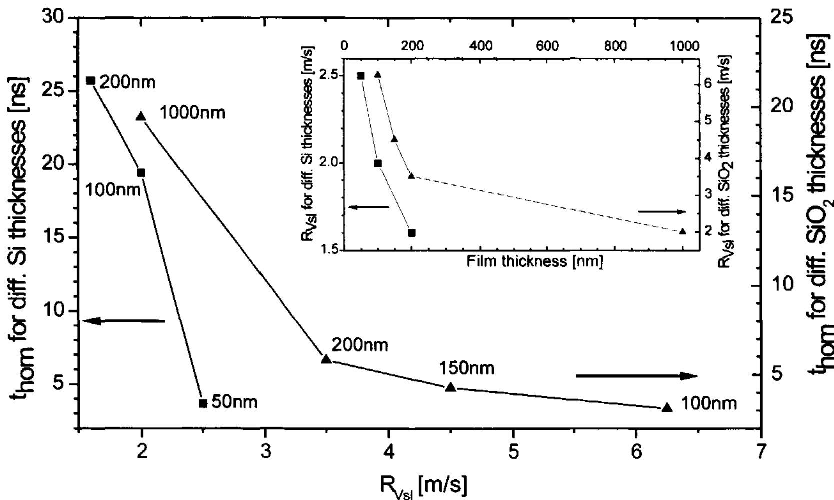


*Fig. 4.8 Nucleation onset and solidification velocity as functions of Si layer thickness (left axis) and $SiO_2$ thickness (right axis).*

One can see that $R_{Vsl}$ decreases with the increase in Si and $SiO_2$ thicknesses. It is caused by the reduced external heat flux $q_{sub}$ from molten Si towards the substrate, as a result of an increased thermal capacitance (i.e., the thickness) of the Si film (Eq. (2.5)), and a reduced vertical temperature gradient (i.e., increased $SiO_2$ thickness) near the Si/underlayer boundary (Eq. (2.16)). The $SiO_2$ underlayer acts as a thermal barrier due to its lower thermal diffusion coefficient than that of solid Si, which slows down the solidification velocity. However, 1000-nm thick $SiO_2$ is already near the limit of "infinite" $SiO_2$ layer thickness, as shown in Fig. 4.5. For such a layer the thermal wave hardly travels through until the end of solidification, due to the thermal diffusion length of approximately 850-900 nm. On the other hand, 100-200-nm thick $SiO_2$ layers are still an intermediate regime and using thinner $SiO_2$ layers will further increase the solidification velocity.

The reduced $R_{Vsl}$ delays the onset of homogeneous nucleation $t_{hom}$ during lateral growth of an c-Si island, as illustrated in Fig. 4.8. As a result, the final c-Si island size $d_L$ increases due to the prolonged duration of the molten state of the nuclei-free Si pool and the fast lateral solidification velocity $R_{Lsl}$ (Eq.(2.15)). This is in a good agreement with the experimental data shown in Fig. 4.1 and Fig. 4.2.

### 4.2.3 Conclusions related to the thermal model

The thermal model has been applied to simulate the growth of c-Si islands in the partial melting regime of an excimer-laser-irradiated Si film. The qualitative agreement with the experimentally observed increase in the size of the c-Si islands with the thickness of a-Si and $SiO_2$ is explained in terms of a reduced heat flux $q_{sub}$ and a vertical solidification velocity $R_{Vsl}$. The reduced $R_{Vsl}$ delays the onset of the homogeneous nucleation event $t_{hom}$, leading to extended growth of the c-Si island in the nuclei-free Si pool and as a result, to a larger c-Si island. Finally, the classical thermal model applied to the nanosecond time scale of the laser pulse duration is capable to explain in a consistent manner the solidification behaviour of Si film in the partial melting regime, even with the simplified model (i.e, without nucleation and supercooling effect).

## 4.3 Phase-field model

This subchapter describes a 2D modelling tool for simulation of the phase-transition kinetics and the thermal distribution of the lateral growth in a Si melt pool from an unmelted residual Si fraction. The solution of the Free Boundary Problem (FBP), which includes curvature supercooling, spontaneous nucleation of solids in a supercooled melt and latent heat recalescence, is obtained by utilizing the *phase-field method*. Solidification behaviour, the supercooling effect in front of the solid/liquid Si interface and the resulting transient temperature profiles are analysed to predict the resulting size of the c-Si islands; these predictions are confirmed by experimental results for model verification. The effects of the a-Si layer thickness and those of the underlying oxide thickness are also discussed.

### 4.3.1 Introduction

The phase-field approach is an alternative method to solve the FBP [4.24, 4.25]. It is rooted in the Ginzburg-Landau theory of phase transitions. In recent years, phase-field models have been introduced to describe the solidification of pure materials [4.26], two-phase binary alloys [4.27], and dendritic growth of these substances [4.28]. The aim of this chapter is to extend the phase-field approach to model pulsed-laser crystallization of a-Si. The advantages of the phase-field model, compared with the classical thermal, capillary and kinetic models are as follows:

1. simple description of the phase transition that appears to embody a rich variety of realistic physical growth phenomena;
2. applicability to model an unstable growth front (i.e., solidification into the supercooled melt) due to the interface of finite thickness. The latter avoids the need to explicitly track the interface and allows a straightforward calculation of any geometrically complex curvature of growing crystal;
3. easy extension to three dimensions;
4. ability to describe the coalescence of two distinct solid regions;
5. applicability to recover sharp- (zero-thickness) interface models of the solidification in the limit of vanishing interface thickness.

In this section, the results from simulations and analyses are presented in order to test the validity of the phase-field model of pulsed-laser crystallization of a-Si. The simulated c-Si island size distribution is compared with the experimentally obtained one. The times of the nucleation onset for different film thicknesses are also compared with those obtained with the thermal model.

## 4.3.2 Phase-field model and formulation

A distinction is made between phases by introducing a phase field which defines the physical state, either liquid or solid, of the system at each spatial position, illustrated in Fig. 4.9. The relevant variable is an order parameter, $\phi$, which changes smoothly from zero in the solid phase to one in the liquid phase across a spatially diffuse interfacial region of finite thickness. The change can be highly localized.

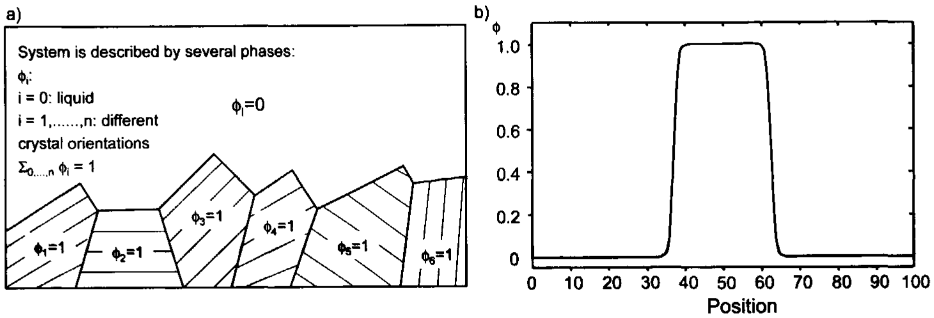


*Fig. 4.9* *a) Physical state definition in phase field by order parameter b) shape of order parameter in solid and liquid phase.*

The phase field formulation is based on the definition of the local entropy, $S$, as [4.29]:

$$S = \int \left( s(\phi, e, c_a) - \frac{\varepsilon^2}{2} |\nabla \phi|^2 \right) dx^3 \tag{4.14}$$

where $s$ is the entropy density, $e$ is the internal energy density, $c_a$ is the alloy concentration (i.e., in case of alloy solidification), epsilon is a gradient correction to the entropy density. The dynamics of the system is described by fluxes of $e$ and $c_a$, while the nucleation and growth of the solid phase are considered as evolution of the phase field.

## 4.3.3 Formulation of the mathematical problem

The evolution of $\phi$ in time and space can be formulated as a set of partial differential equations, which can be solved by standard finite difference methods together with the thermal continuity equation. The equations can be derived in a thermodynamically consistent manner starting from the Gibbs free

energy functional of the present phases. The phase-field equation for the case of solid-liquid transformation of only one Si grain, derived for a double obstacle type of free energy functional, is as follows:

$$\dot{\phi} = \mu_{sl} \left\{ \sigma_{sl} \left[ \left( \nabla^2 \phi \right) + \frac{\pi^2}{\eta^2} \left( \phi - \frac{1}{2} \right) \right] + \frac{\pi}{\eta} \sqrt{\phi(1-\phi)} S_f \left( T_{eq} - T \right) \right\} . \quad (4.15)$$

The part in square brackets on the RHS of Eq. (4.15) accounts for interfacial curvature, and $\sigma_{sl}$ is the solid-liquid interfacial energy. No anisotropy in the interfacial energy is taken into account in this study, but it can be introduced [4.30, 4.32]. The second term is the thermal driving force for phase change, which is proportional to the entropy of melting $S_f$, and the thermal supercooling $T_{eq}$-$T$. $\eta$ is the interface thickness and in our case the only numerical parameter. $\mu$ is the mobility of the interface. The temperature field is obtained from the heat diffusion equation, shown in Eq. (4.1), which is the usual continuity equation and is coupled to the phase field equation by the release of latent heat at time $t$. The physical values used in this calculation are the same as those used in the thermal model, except for the additional parameters summarized in Table 4.4.

*Table 4.4 Physical values used in numerical simulation.*

| Properties | c-Si |
|---|---|
| Entropy of melting $S_f$ [J×cm$^{-3}$×K$^{-1}$] | 2.533 Ref.[4.16] |
| Solid-liquid interfacial energy $\sigma_{sl}$ [J×cm$^{-2}$] | 4.38$^{-5}$ Ref.[4.33] |
| Interface mobility $\mu$ [cm$^4$×J$^{-1}$×s$^{-1}$] | 600 Ref.[4.33] |

The simulation software used in this study was provided by the company Access e.V. [4.31]. The simulation was confined to the two-dimensional case; this simplifies the analysis and presentation of the simulation, while it also tests and demonstrates the capability of the model. The sample structure is the same as that used in the thermal model; the variations of Si film and the oxide underlayer thicknesses used in the simulation are listed in Table 4.1. The model simulates the near-complete melting regime, i.e., regrowth from the residual solid Si nuclei at the Si/$SiO_2$ interface directly after the end of the laser pulse. The solid/liquid interface thickness is 15 nm. The initial boundary conditions are calculated by the thermal model, discussed above, and are shown in Fig. 4.5. These temperature profiles were mapped onto the calculation grid for the phase field simulations.

### 4.3.4 Nucleation model

In the present model, nucleation is treated by a fully deterministic approach with critical supercooling as a single parameter. The dependence of the nucleation rate $dN/dt$ on the supercooling temperature $\Delta T$ is approximated by this simple approach as a step function (illustrated in Fig. 4.10):

$$\frac{dN}{dt} = \begin{cases} 0, & \Delta T < T^*, \\ \frac{1}{\Delta x^3 \Delta t}, & \Delta T > T^*, \end{cases} \tag{4.16}$$

where $\Delta t$ is the time step and $\Delta x$ the grid discretization. According to the latter condition, a nucleus is set immediately if in a grid cell the temperature decreases till the critical nucleation temperature. The nucleation event itself consists of the initiation of a new solid/liquid interface in the grid cell, e.g. the fraction solid is switched from 0 to $10^{-4}$. The minimal distance of two nuclei is assumed to be limited by the propagation length of the thermal wave $L^*$ in one time step $\Delta t$:

$$L^* = \sqrt{\frac{k(T)}{C(T)}\Delta t} \ . \tag{4.17}$$

After the nucleation event is initiated, the grid cell becomes a mixed-phase cell, which is then free to solidify as determined by the interface motion algorithm. Because the interfacial curvature is not defined until the grain size reaches the phase field interface thickness $\eta$, the growth kinetic in this initial stage is calculated without curvature supercooling until the grain size exceeds $\eta$.

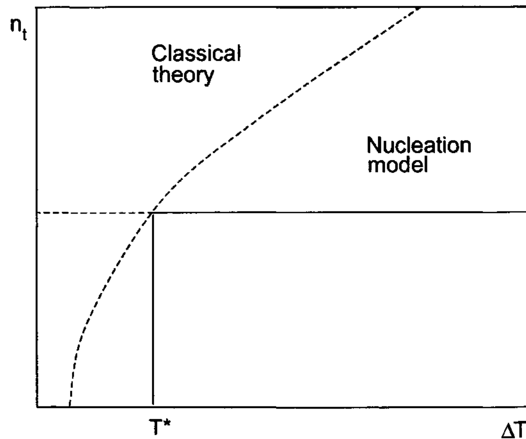


*Fig. 4.10 Deterministic nucleation model used in simulation.*

Since the highest melt supercooling is always reached at the Si(liq)-$SiO_2$ interface because of the heat flow into the substrate, this model will always generate the nuclei near/at the interface. The homogeneous nucleation-initiated solidification mechanism can satisfy this since the consideration simply involves the thermal evolution of the liquid Si in physical contact only with a relatively non-catalytic $SiO_2$ surface, which is a chemically stable and structurally amorphous oxide layer. Therefore, in the present analysis the simulation of the lateral grain growth is restricted only by homogeneous nucleation, neglecting heterogeneous nucleation.

## 4.3.5 Results and discussion

### 4.3.5.1 Overview of solidification dynamics

Figure 4.11 shows the evolution of the crystalline silicon area as a function of time $t$ in the liquid 100-nm-thick Si layer on 200-nm thick underlying oxide.

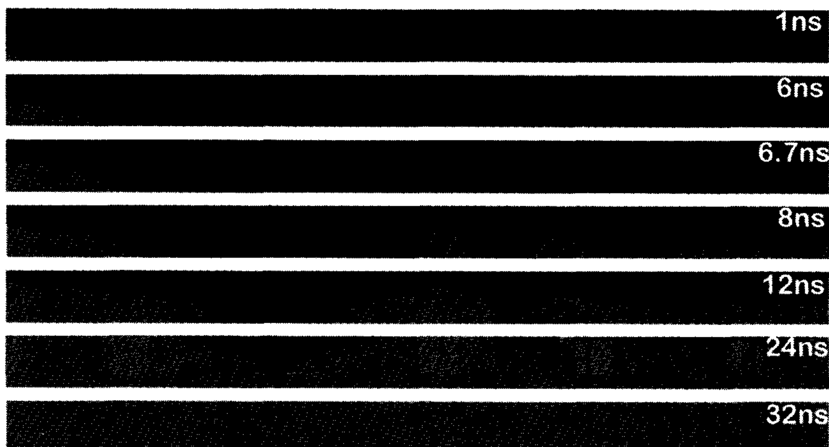


*Fig. 4.11 Shape of Si solid/liquid interface for 100 nm Si / 200 nm $SiO_2$ at different time steps t. The domain size is $1.5\times0.1\mu m$.*

The simulation starts with a small initial nucleus of solid silicon (light grey colour) in the lower left corner of liquid Si (dark grey colour). The black line marks the solid/liquid interface. Heat is extracted through the $SiO_2$ layer at the bottom. As can be directly seen from the parabolic shape of the solid/liquid interface, the solidification rate is larger in the lateral direction parallel to the Si/ $SiO_2$ than normal to the interface. The crystalline layer primarily spreads out

along the interface before it grows in thickness. The inclination of the solid/liquid interface at the tip is determined by the interfacial energy, the growth rate and the wetting angle. In this calculation the wetting angle is equal to 90 degrees.

The position of the solid/liquid boundary along and perpendicular to the Si/$SiO_2$ interface is shown in Fig. 4.12. The lateral solidification velocity $R_{Lsl}$, which is the slope of the tangent of the curve, increases with time, reaching the value of 44 m/s, while that in the vertical direction $R_{Vsl}$ follows a square root behaviour, reaching the value of 9.4 m/s.

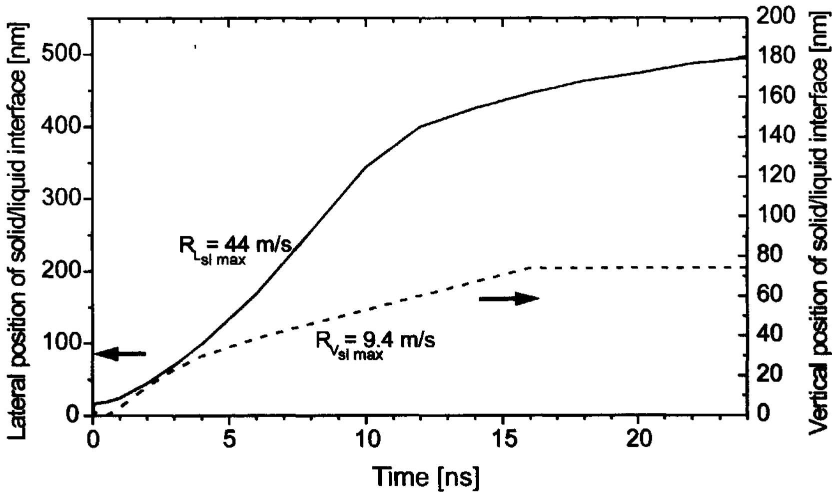


*Fig. 4.12 Solid/liquid interface position perpendicular and parallel to the substrate versus time.*

Figure 4.13 illustrates a detailed two-dimensional temperature profile near the solid/liquid interface in the Si film for various time steps. Thin curves show isothermal temperature profiles for the following temperatures: 1675, 1670, 1665, 1650, 1625, 1600, and 1575K. As follows from this figure, the temperature along the Si/$SiO_2$ interface is always lower than that in the direction of the Si surface due to the thermal diffusion towards the underlying oxide. As a result, the solidification rate is highest at the Si/$SiO_2$ interface. However, the temperature along the horizontal direction always takes the local maximum at the solid/liquid interface, since a large amount of latent heat is released there. As can be seen from the spacing of the isothermal lines, the temperature at the solid/liquid interface is less than that at the top, which means that the supercooling condition is more pronounced at the Si/$SiO_2$ interface. As a result, the stronger supercooling near the Si/$SiO_2$ interface provides a higher growth rate there,

while the less supercooled surface region of the molten Si film results in a slower growth rate there (see also Fig. 4.12).

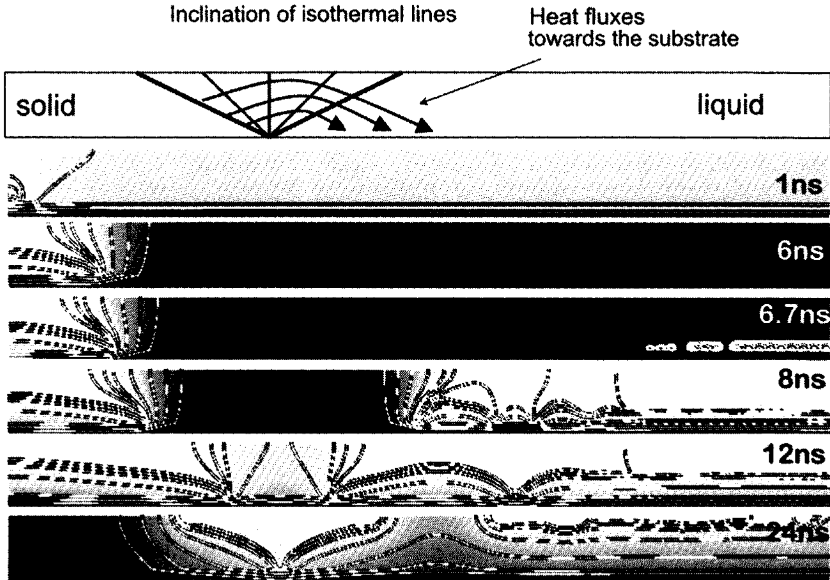


*Fig. 4.13 Si temperature profiles around Si solid/liquid interface at different times t. Thin curves indicate isothermal temperature profiles from left to right, at the following temperatures: 1675, 1670, 1665, 1650, 1625, 1600, and 1575K. The domain size is 1.5×0.1µm.*

The excessive thermal energy generated by latent heat is consequently removed in all directions, which is reflected by the different inclination angles of the isothermal lines to the $Si/SiO_2$ interface:

(a) the lateral energy removal mechanism near the solid/liquid interface is indicated by the isothermal lines normal to the $Si/SiO_2$ interface;

(b) the vertical heat removal mechanism is observed during the first 3 ns for temperature of 1575 K, shown by outward tilted isothermal lines.

The tilted solid/liquid interface is convenient for the fast growth rate, because of the efficient and fast release of the excess latent heat from the solid/ liquid interface tip to the supercooled melt. However, in simulations of Aichmayr et al. [4.6] the solid/liquid interface is sharp at the center of the Si thin film, while Gupta et al. [4.5] reported that the solid/liquid interface is vertical to the Si-underlayer interface. In both cases the interfacial energies were neglected, due to the utilized model types, leading to inaccurate growth rate estimations and elimination of the influence of Si-underlayer interface properties.

Figure 4.14 shows temperature profiles at the $Si/SiO_2$ interface parallel to the substrate for several $t$ values after the end of laser pulse. The solid/liquid interfaces are located at the right edge of the temperature peaks (as shown by arrows), immediately followed by the supercooling region. The solid Si fraction is located at the left edge of the temperature peaks. This particular temperature profile is always found for a complete solidification process of a growing crystal fraction, which may either have started as a set of nuclei or have spontaneously nucleated. Note that $T_m$ is not the equilibrium melting temperature, but reduced by approximately 7 K to 1673 K due to the capillarity effect.

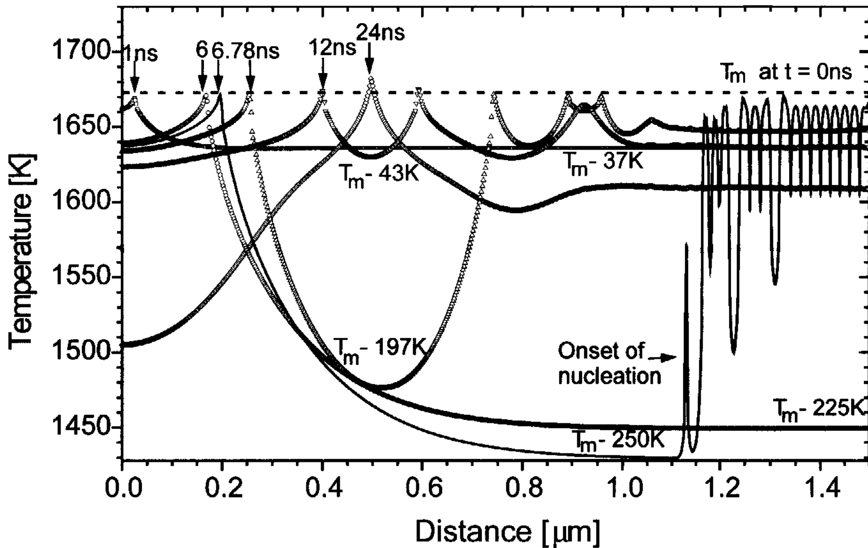


*Fig. 4.14 Temperature profiles at the $Si/SiO_2$ interface at t = 1, 6, 6.7, 8, 12 and 24 ns. Arrows indicate the position of the solid/liquid interface. Note that $T_m$ is not the equilibrium melting temperature, but reduced by approximately 7K to 1673K due to the capillarity effect.*

As can be seen the temperature in the supercooled region gradually drops from the melting point of $T_m$ to $T_m$ - 37 K within the first 1 ns, then it drops to $T_m$ - 125 K over the next 2 ns and gradually it drops further to $T_m$ - 225 K within the next 5 ns. Finally, the melt supercooling reaches the critical supercooling temperature of $T_m$ - 250K within 6.7 ns after the end of laser pulse. At this moment the nucleation event is triggered, which immediately raises the temperature at the peripheral area significantly due to the latent heat recalescence. The first nucleus, which will approach the initially growing grain is born and competitive grain growth starts. At $t$ =8 ns numerous nuclei are generated spontaneously, decreasing the supercooling temperature to $T_m$ - 30 K.

The temperature peaks at the right side of the plot represent the solid/liquid interface for newly formed grains. At $t$ =24 ns the initial grain collides with the neighbouring one at the $Si/SiO_2$ interface. The local temperature rises at the boundary between these grains because of the insignificant diffusion of the excessive thermal energy, generated by latent heat release at the solid/liquid interfaces of these two grains. At $t$ =32 ns the solidification process is completed, resulting in a 1-μm large c-Si island that is in very good agreement with experimental data from Fig. 4.2.

The supercooled Si melt leads to three consequences:

1. The solid/liquid interface inclined to the underlayer is important for enlargement of c-Si island size since it increases the supercooling temperature in the melt by fast heat extraction of the thermal energy released from the latent heat at the solid/liquid interface, i.e., the solidification speed is connected with the supercooling of the melt.
2. The solid/liquid interface can be morphologically unstable. Therefore the interface can break up into a disordered amorphous morphology, which was observed for the thinnest a-Si and underlying $SiO_2$ films (SEM images in Fig. 4.1 and Fig. 4.2).
3. New grains can nucleate due to severe melt supercooling (relative to the equilibrium melting point $T_m$) during lateral growth. The temperature at which nucleation begins depends on the melt-supercooling rate, which is defined by the thermal balance in an a-Si film, i.e., by the relationship between laser energy, heat removal into a substrate, and the rate of releasing the heat of solidification due to a growing grain. As a result, this copious melt nucleation of new fine grains is a limiting stage of lateral growth process, restricting the final c-Si island size.

#### 4.3.5.2 Effect of the Si film thickness

Figure 4.15 shows the simulated radius of the c-Si island as a function of time for various Si film thicknesses. The thickness of underlying oxide was kept at 1μm. As can be seen, the c-Si island size increases with Si film thickness. On the other hand, the thinner the Si film, the fastest the growth rate, which can be estimated from the slope of the respective curve. However, when the crystal growth is driven at a critically high velocity, the growth front can break down completely with the formation of a disordered amorphous solid fraction, which is shown in SEM image in Fig. 4.1 for 50 nm thick Si film. The value of critical velocity was estimated to be 19 m/s by comparing the position of amorphization onset of SEM image in Fig. 4.1 and simulation results. This value lies close to the calculated velocity of 15 m/s as reported in [4.11].

The higher growth rate in 50-nm thick Si film is due to the stronger supercooling near the solid/liquid interface, which is determined by the thermal flow to the underlying oxide.

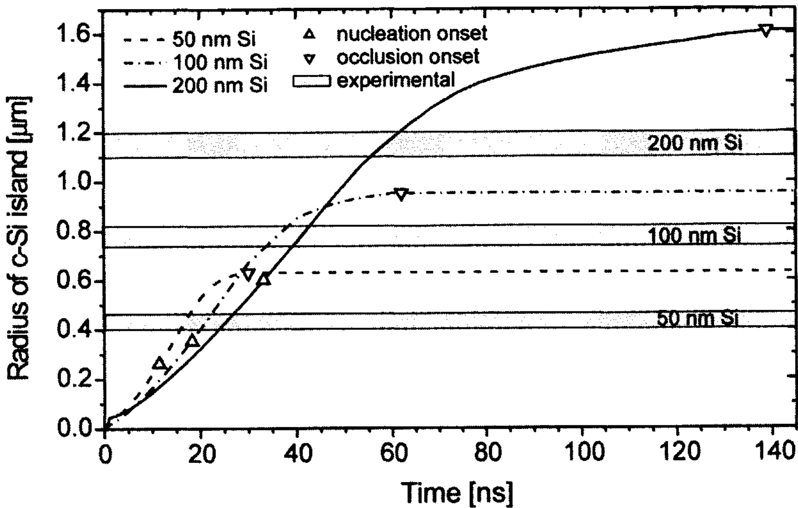


*Fig. 4.15* *Simulated radius of a c-Si island as a function of time for various Si film thicknesses. The thickness of the underlying oxide was kept at 1000 nm.*

One should note that the total thermal energy initially stored in the Si film is proportional to the film thickness as well as to the resulting lateral thermal flow. As a result, the effects of the lateral heat flow on the temperature profile are approximately the same for all Si thicknesses. However, the vertical heat flow to the underlying oxide depends on the Si thickness, resulting in a larger and faster reduction of the temperature for the thinner film. Despite the higher crystal growth rate for the thinner film, the temperature in the supercooled melt drops more quickly, reaching the critical temperature of spontaneous nucleation already at t= 11.4 ns after the end of the laser pulse for a 50-nm Si film, compared to that at t= 33.2 ns for a 200-nm thick Si film. As a consequence, the crystal growth time is reduced, resulting in a smaller grain size. The minimum temperature in the supercooled region for a thick Si film stays longer, resulting in later nucleation event, which extends the crystal growth distance and therefore makes thicker Si films more suitable for fabrication of large c-Si islands and defect-free crystal growth.

#### 4.3.5.3 Effect of the $SiO_2$ film thickness

Figure 4.16 shows the simulated radius of a c-Si island as a function of time for various underlying $SiO_2$ film thicknesses. The thickness of the top Si film was kept at 100 nm. As one can see, the c-Si island size increases with the underlying

$SiO_2$ film thickness. It stems from the fact that the spontaneous nucleation is delayed for a thicker underlying $SiO_2$ film. Despite the decreased solidification velocity, it leads to a longer crystal growth in the nuclei-free Si melt, and subsequently to a larger c-Si island size, which is consistent with our experimental results. The thicker $SiO_2$ layer efficiently suppresses the vertical thermal flow from a molten Si film towards the substrate. In this way the temperature of the molten Si film can remain above the critical temperature of nucleation for a long time, which also results in the high solid/liquid interface temperature, providing the slow crystal growth rate. The influence of the underlying substrate (i.e., a Si wafer or glass wafer) on the cooling rate and the solidification velocity is significant when the intermediate oxide thickness is comparable with the diffusion length of the thermal wave (800-900 nm). 1000 nm thick oxide is already near the limit of infinite $SiO_2$ thickness, and the properties of the underlying substrate do not play any role. As was mentioned before, the breakdown of the growth front can occur at high crystallization velocities, followed by film amorphization. Such behaviour is depicted in the SEM image from Fig. 4.2 for a 100-nm thick $SiO_2$ film. The calculated maximum growth front velocity at the position of the amorphization onset has a value of 19 m/s. Therefore, thicker $SiO_2$ underlayers are desirable for defect-free ultra-large c-Si island growth.

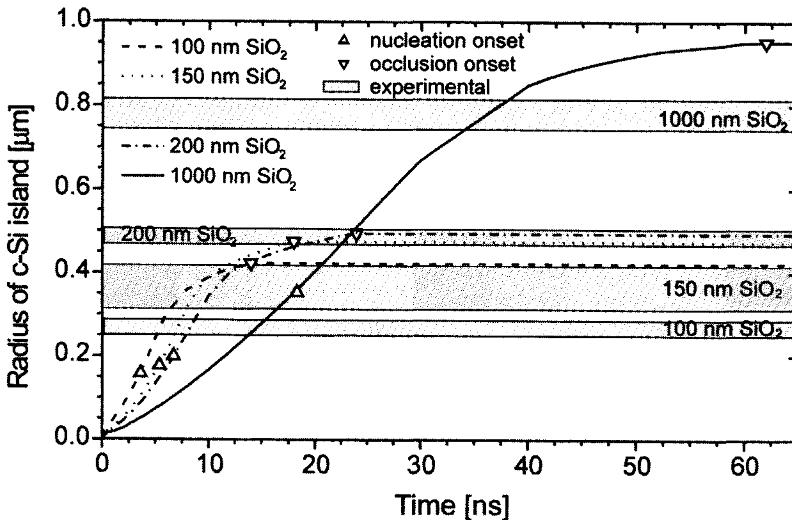


*Fig. 4.16* *Simulated radius of c-Si island as a function of time for various underlying $SiO_2$ film thicknesses. The thickness of top Si film was kept at 100 nm.*

### 4.3.6 Conclusions related to the phase-field model

Here a first attempt at developing a 2D phase-field modelling tool which is able to predict the average grain size of a laser recrystallized a-Si film has been presented. The only free parameter within the applied model is the critical supercooling temperature for nucleation, which was adjusted to 250 K by comparing the simulation for the 100-nm a-Si / 200-nm $SiO_2$ case with experimental observed grain sizes. The maximum lateral and vertical growth velocities in this case differ by nearly four times, i.e., $R_L$ = 44 m/s and $R_V$ = 9.4 m/s. The solid/liquid interface is non-planar: $R_{Vsl}$ decreases in the vertical direction governed by the propagation of the thermal wave into the $SiO_2$ layer; $R_{Lsl}$ accelerates as a consequence of the increasing melt supercooling in front of the interface in the lateral direction. Supercooling temperatures of approximately 250 K at the periphery of the solidifying Si melt were achieved within 6.7 ns. The experimentally obtained sizes of c-Si islands were in a good agreement with the ones predicted by the model for various thicknesses of the Si film and the underlying $SiO_2$ film. The increase in c-Si island size with thicker Si and underlying $SiO_2$ film was explained by the reduced cooling rate in the supercooled Si melt and subsequently delayed spontaneous nucleation. The growth front breakdown (i.e., film amorphization) for thinnest Si and underlying $SiO_2$ films occurred at $R_{Lsl}$ = 19 m/s. Therefore, the thermal properties and thickness of underlying $SiO_2$ layer, as well as the Si layer thickness play an important role in the enlargement of the c-Si island and defect-free crystal growth.

However, for nucleation supercooling of 250 K, the size of c-Si islands was overestimated in most cases by the simulation. This could indicate that the critical supercooling is smaller than 250 K and a better agreement could be achieved by using its lower value. Additionally, the 2D simulations were done with Cartesian coordinates. Due to the spherical symmetry of the grains, cylindrical coordinates should be more appropriate. Especially the size ratio between the main and its next neighbouring grain is different between the simulation and the experiment. This could be a geometrical effect due to the spherical growth.

## 4.4 Thermal model vs. phase-field model

In order to make a meaningful comparison between the 2D phase-field model and the 1D thermal model, it is necessary to note explicitly which output values can be compared in a physically consistent manner. This stems from the

fact that among the parameters that appear in the phase-field model there are several that have no immediate counterpart in a thermal model. In particular the solid-liquid interfacial energy $\sigma_{sl}$ and the interface mobility $\mu$, influencing the solidification mechanism, cannot be related directly to any such parameter in the thermal model. That is why the predictions of solidification velocities and total solidification time derived from the phase-field and the thermal model will generally disagree to some extent.

Therefore, it is interesting to compare only the time of the nucleation onset, since it depends mainly on the supercooling degree of the melt, determined by the external heat flux towards the underlying layer. The corresponding times of the nucleation onsets $t_{hom}$ for different Si and $SiO_2$ thicknesses are illustrated in Fig. 4.17a and Fig. 4.17b, respectively. One can see that the nucleation onsets occur slightly later in the phase-field model than in the thermal model. The reasons that explain the retarded nucleation are as follows. As was mentioned before, the principle of the thermal model lies in coupling of the position of the solid/liquid interface to the equilibrium transition temperature $T_m$ and underlying assumption of temperature uniformity throughout a subvolume. The former means that the selection of the interface morphology cannot be solved properly in the case of unstable growth fronts; the latter means that temperatures are calculated for the subvolume centers, requiring extrapolation and interpolation to estimate temperatures at a specific point in space, which influences the final cooling rate.

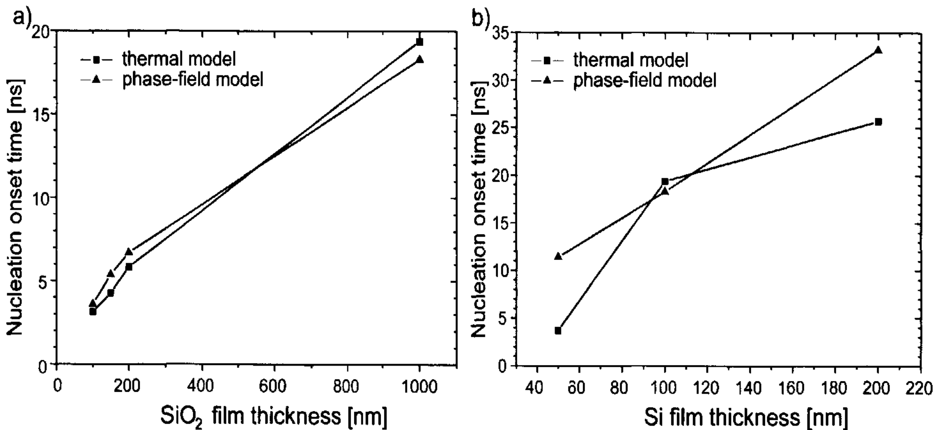


*Fig. 4.17 Comparison between simulated times of nucleation onset, obtained by the thermal model and the phase-field model.*

In case of the phase-field model, the retarded nucleation far away from the initial seed can be also explained as the result of recalescence due to the growth of the c-Si island. As shown in Fig. 4.11 the nucleation starts in the far-away right

side at the bottom of the melt pool in contact with the $SiO_2$ layer. In fact, because the recalescence originates from growing of the c-Si island on the left, an efficient heat conduction decreases the cooling rate of the liquid phase at the far field on the right, around the zone where nucleation should occur; in turn, a resulting lower cooling rate delays the onset of homogeneous nucleation in the 2D phase-field model.

As a concluding remark, the quantitative agreement between the 1D thermal model and the 2D phase-field model can be improved by coupling a simple field theory of the nucleation process with the supercooling effect and the heat flow calculations.

# Chapter 5

# *Enlargement and location control of c-Si islands by the Dual-Beam Method*

This chapter shows the experimental results obtained with dual-beam irradiation. In particular, it analyses the mechanism of Si grain enlargement and the effect of the processing energy density window on the obtained location-controlled grains. The size of the c-Si island and its processing window were influenced by the thickness of an intermediate oxide layer, by its geometry and by the laser energy density. The experimental results are explained on the basis of a 2D heat flow analysis of the solidification mechanism of the Si film.

## 5.1 Results and discussion

### 5.1.1 Experimental effect of underlying $SiO_2$ bump dimension on c-Si island size

As was described in Chapter 3.1, the DBTOP structure consists of tri-layer islands, i.e., a-Si / $SiO_2$ / metal stacks on a glass substrate (shown in Fig. 3.2a). The underlying patterned oxide forms an array of bumps for location control of the c-Si islands. The dimensions of the oxide bumps are summarized in Table 3.3 (Chapter 3.4); the thickness of a-Si and TiW layers were 100 and 520 nm, respectively.

Figure 5.1a illustrates the size (i.e., diameter) of location-controlled c-Si islands as a function of the bump height for bump diameters of 1.6, 2.0, 2.4 and 2.8 μm. In this case an Al mirror was used during dual beam irradiation. Figure 5.1b illustrates the results obtained with a Si mirror. It should be noted that the c-Si islands are always located exactly on top of each $SiO_2$ bump. In both cases their size increased monotonically with the bump height and diameter.

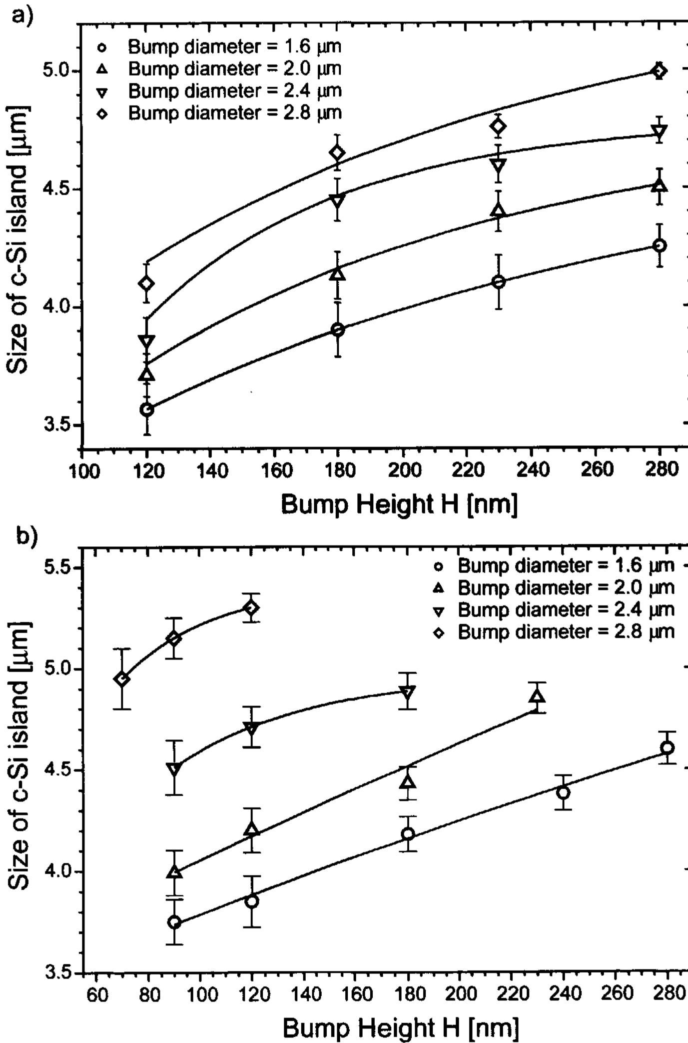


*Fig. 5.1* *Size of location-controlled c-Si islands as a function of the oxide bump dimensions. a) experiment with Al mirror; b) experiment with Si mirror.*

The maximum obtained c-Si islands size was 5.0 and 5.4 µm for the Al and the Si mirrors, respectively. These sizes were obtained with the maximum diameter of the bump, i.e., 2.8 µm and the maximum height of the bump, i.e., 280 and 120 nm for the Al and the Si mirror, respectively. It should be noted that the absence of the large bump height value in the experiment with the Si mirror is due to the cracking of the underlying metal layer at high energy density. Figure 5.2 shows a SEM photograph of the obtained 5.0 and 5.4-µm large c-Si islands, centred on top of the underlying oxide bumps.

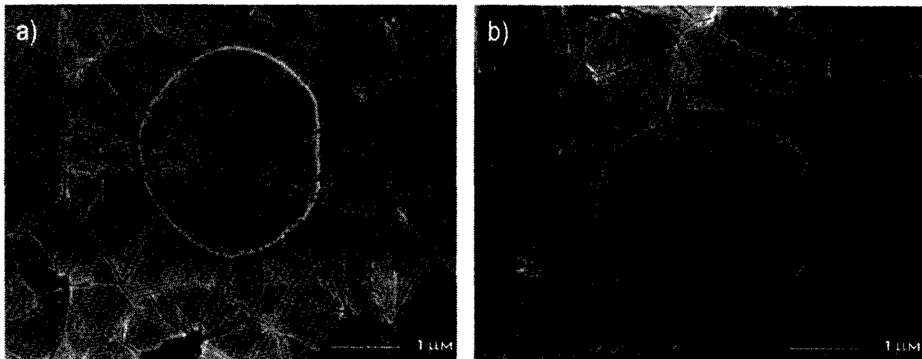


*Fig. 5.2 SEM photographs of largest location-controlled c-Si islands with (a) Al mirror and (b) Si mirror. Underlying oxide bumps are visible as circles.*

## 5.1.2 Numerical simulation and discussion

### 5.1.2.1 Model definition

In order to explain the influence of the bump dimensions on the size of the location-controlled c-Si island we carried out a 2D heat flow analysis. A stacked structure of a 100-nm thick Si layer, a 140-nm thick $SiO_2$ layer (thin oxide), and a 520-nm thick TiW layer on a glass substrate were assumed. The structure schematics, material properties and boundary conditions can be found in Chapter 4.2.1. The diameter of the circular bump varied from 1.6 to 2.8 µm, while the heights of the bump structures were chosen as 120, 230 and 280 nm. The oxide bump dimensions used in the simulations are summarized in Table 5.1.

*Table 5.1 Variations of simulated bump diameter and height.*

| Bump height [nm] | 120 | 230 | 280 |
|---|---|---|---|

For a bump diameter of 2.0 µm.

| Bump diameter [μm] | 1.6 | 2.0 | 2.4 | 2.8 |
|---|---|---|---|---|

For a bump height of 230 nm.

The temperature distributions were numerically obtained with commercially available MSC software [4.22] coupled with custom user subroutines. All the simulations were performed only for an Al mirror.

#### 5.1.2.2 Effect of the $SiO_2$ bump dimensions on the size of the c-Si island

As illustrated in Fig. 5.1 an increase in the bump dimensions results in the enlargement of the c-Si island, both for the Al and the Si mirror. This type of behaviour can be explained by simulated solidification dynamics. Figures 5.3a and 5.3b show the simulated transient temperature profiles at the Si surface and at the $Si/SiO_2$ interface for different bump heights and diameters, respectively. The bump diameter and bump height were kept at 2.0 μm and 230 nm, respectively.

In all cases the temperature dropped rapidly after the end of laser pulse and then reached the solid/liquid transition temperature $T_{SL}$ where the latent heat of solidification is released. Solidification times $t_s$ are shown in Fig. 5.3a and 5.3b. The vertical solidification velocity $R_{Vsl}$ is calculated as:

$$R_{Vsl} = \frac{t_s}{h} \quad . \tag{5.1}$$

The homogeneous nucleation onset times $t_{hom}$ for a laterally solidifying c-Si island are derived from Eq. (2.14) by using $R_{Vsl}$ values. All the above-mentioned results for different bump heights and diameters are summarized in Tables 5.2 and 5.3, respectively.

*Table 5.2 Solidification times, velocities and nucleation time onsets for different bump heights.*

| Bump height [nm] | $t_s$ [ns] | $R_{Vsl}$ [m/s] | $t_{hom}$ [ns] |
|---|---|---|---|
| 130 | 198.5 | 0.5 | 42.7 |
| 230 | 268.2 | 0.37 | 55.8 |
| 280 | 376.6 | 0.26 | 79.4 |

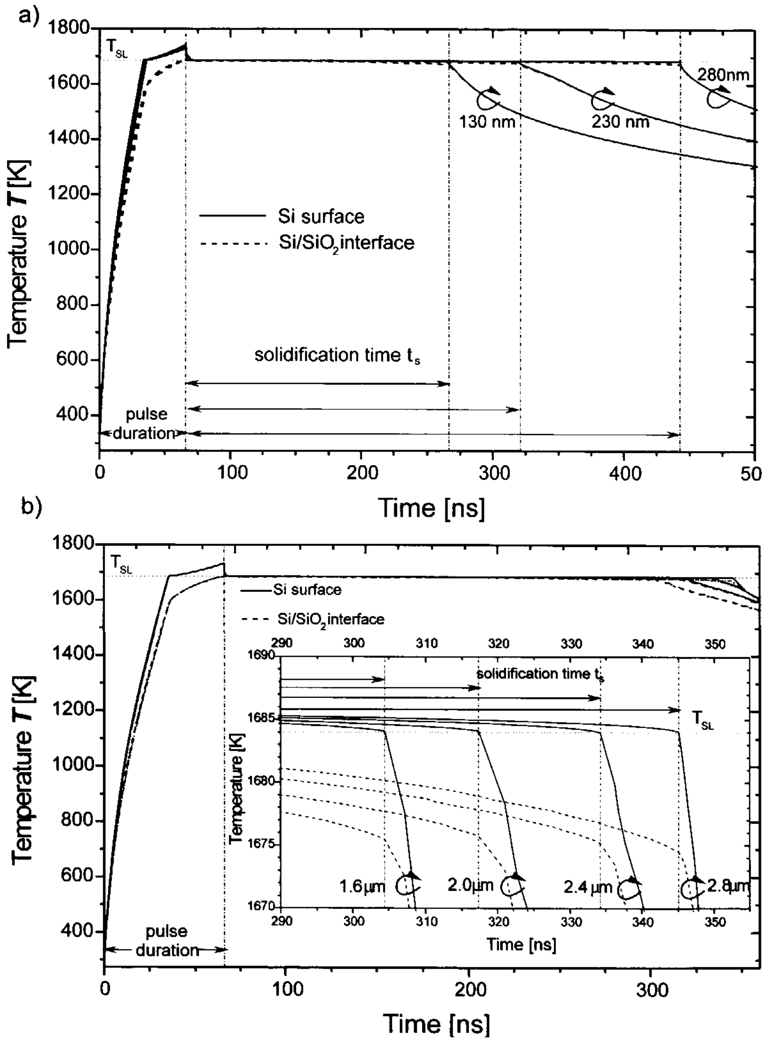


*Fig. 5.3 Simulated transient temperature profiles at the Si surface and at the $Si/SiO_2$ interface for different (a) bump heights and (b) bump diameters. The bump diameter and bump height were kept at 2.0 µm and 230 nm, respectively.*

The solidification velocity $R_{Vsl}$ and nucleation onset $t_{hom}$ as functions of the $SiO_2$ bump height and diameter are plotted in Fig. 5.4a and 5.4b, respectively.

*Table 5.3 Solidification times, velocities and nucleation time onsets for different bump diameters.*

| Bump diameter [μm] | $t_s$ [ns] | $R_{Vsl}$ [m/s] | $t_{hom}$ [ns] |
|---|---|---|---|
| 1.6 | 234.0 | 0.43 | 48.9 |
| 2.0 | 251.3 | 0.4 | 51.3 |
| 2.4 | 265.2 | 0.38 | 53.8 |
| 2.8 | 279.1 | 0.36 | 56.7 |

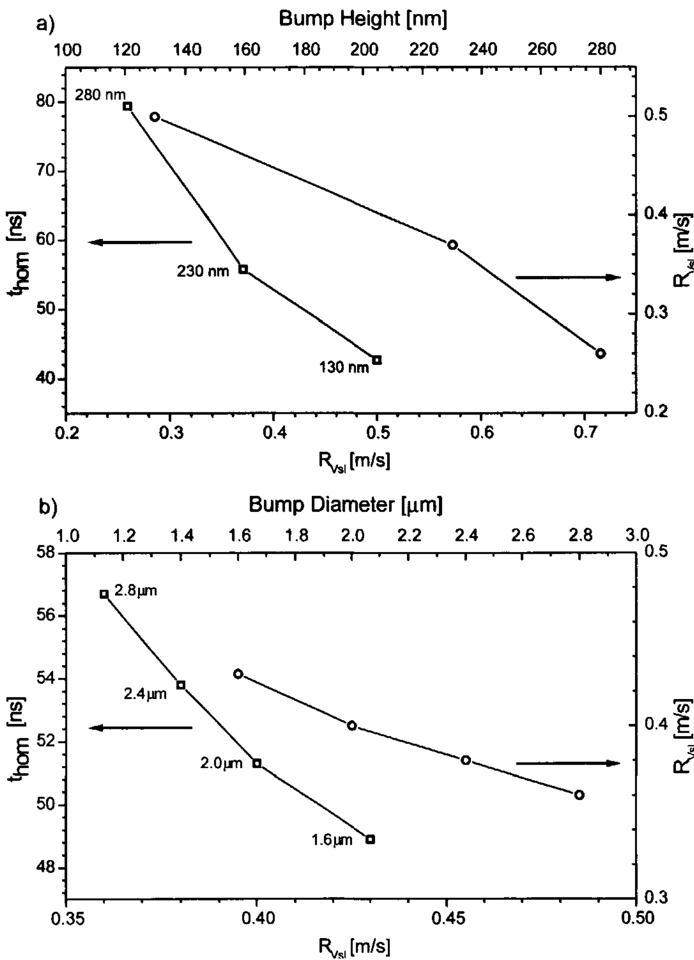


*Fig. 5.4 Nucleation onset (left axis) and solidification velocity (right axis) for different (a) bump heights and (b) bump diameters.*

It can be seen that the homogeneous nucleation onset always increases with the bump dimensions. This behaviour can be explained as follows:

(a) the amount of lateral heat flow in the molten Si film from the periphery into the bump area and the underlying oxide layer increases with the bump dimension. For different bump dimensions Fig. 5.5a and 5.5b show simulated temperature profiles along the $Si/SiO_2$ interface immediately after the laser pulse. Note that the laser energy density was adjusted, so that the temperature at the center of the bumps was constant at $T_m$.

One can see that at 5 μm away from the center of the bump, there is a molten Si film temperature difference between the highest bump and the lowest bump of almost 305 K, and one of 110 K between the bump with the largest and that with the smallest diameter, as shown in Fig.5.5a and 5.5b, respectively. As a result, the difference between temperatures of Si on the bump periphery and that on the bump top also increases significantly, i.e., 271 and 580 K for bumps with different bump heights and 354 and 461 K for bumps with different diameters. It stems from the fact that more energy is required to keep the temperature at $Si/SiO_2$ interface on the top of the bump at $T_m$ with increase in bump heat capacitance (i.e., its dimension). The resulting high temperature gradient between the surrounding thin oxide and the bump causes larger amount of lateral heat flow in molten Si film and underlying $SiO_2$ layer at larger bump. This reduces external heat flux $q_{sub}$ towards the substrate.

b) The increase of the laser energy density with the bump dimensions also leads to higher temperatures of the metal layer, which also reduces $q_{sub}$ from the molten Si layer towards the substrate due to the decreased $dT/dz$ near the Si/$SiO_2$ underlayer boundary.

As a result of the reduced $q_{sub}$, low $R_{Vsl}$ delays the onset of homogeneous nucleation event $t_{hom}$ during lateral growth of c-Si island, as shown in Fig. 5.4. Consequently, the final c-Si island size $d_L$ increases due to the prolonged duration of the molten state of the nuclei-free Si pool and/or the fast lateral solidification velocity $R_{Lsl}$ (Eq.(2.15)). This is consistent with our experimental observations from Fig. 5.1, which showed that the largest c-Si island sizes occur with the largest bump dimensions.

It is worth noticing that the effect of the bump height on the nucleation onset time $t_{hom}$ is more pronounced than that of the bump diameter. The former causes lower vertical temperature gradients $dT/dz$ near the $Si/SiO_2$ underlayer boundary (Eq.(2.16)) and a larger lateral heat flow. The $SiO_2$ underlayer acts as a thermal barrier due to its lower thermal diffusion coefficient compared to the solid Si, which slows down the solidification velocity. However, the maximum bump height (i.e., oxide thickness) is determined by the thermal diffusion length of the thermal wave travelling through it. For the $SiO_2$ layer it is approximately 850-900 nm. For bump heights higher than this value the effect of grain size enlargement will be negligible.

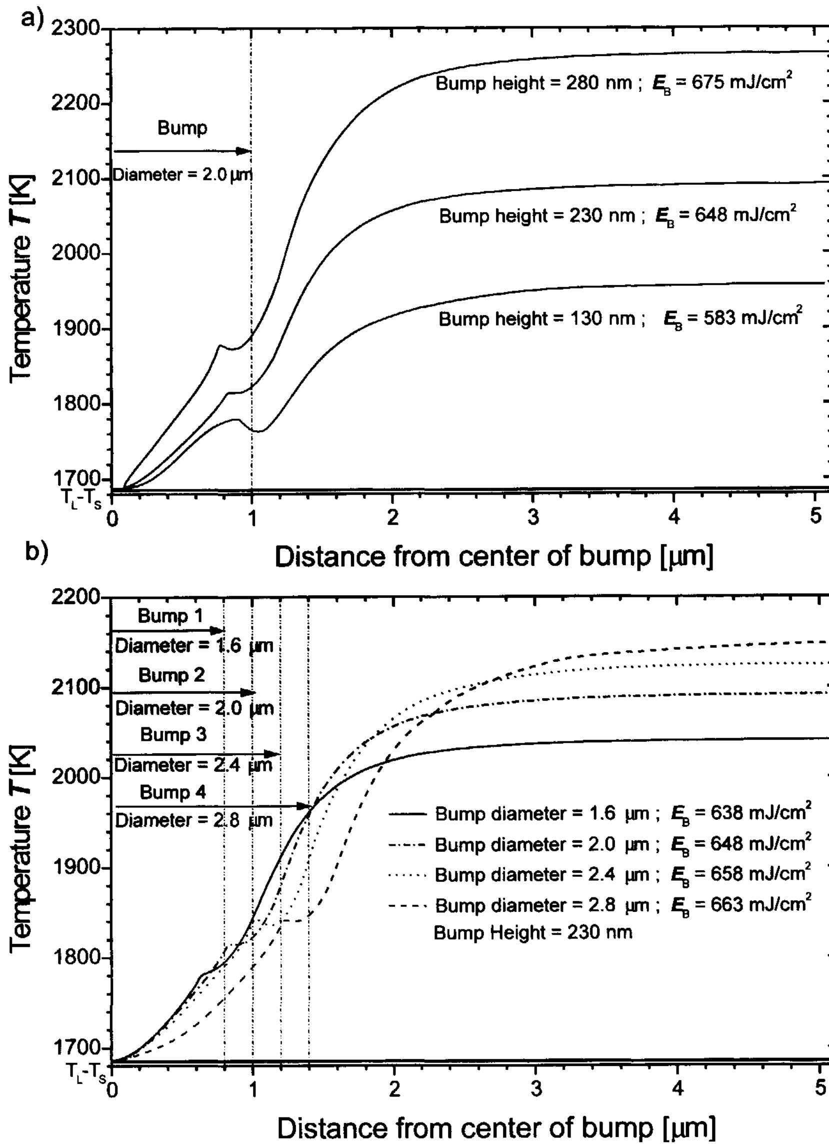


*Fig. 5.5* *Simulated temperature profiles along $Si/SiO_2$ interface immediately after the laser pulse for different (a) bump heights and (b) bump diameters.*

### 5.1.3 Limit of the enlargement of c-Si island size

One of the requirements for c-Si island enlargement is the efficient reduction of the external heat flux $q_{sub}$ from the molten Si layer towards the substrate. Among others, this requirement can be satisfied by increasing the underlying metal layer thickness (i.e., its heat capacitance) and laser energy density $E_B$ (i.e., the temperature of the underlying metal layer). However, as was shown in the fabrication details (Chapter 3.3.1.2), the intrinsic stress $\sigma_{int}$ in the metal film also increases significantly with its thickness, leading to poor adhesion to the underlying substrate. As a result of the increased heat capacitance of the metal layer, the laser energy density should also increase with the thickness of this layer in order to keep the temperature gradient between the metal film and molten Si layer gentle. The increase in the laser energy density strongly increases the temperature of the metal layer near the metal/glass interface, which introduces the undesirable thermal stress $\sigma_{th}$ in it. As was explained in Chapter 3.3.1.2, the thermal stress results because of the mismatch in the temperature coefficients of the linear expansion (TCLE) of the metal film and the substrate (see also Fig. 3.5). This can lead to the formation of cracks in the metal film and its subsequent peeling off from the substrate, which was observed in the DBTOP method with Cr and W layers [5.4,5.6].

Several experiments with different types of metal/metal alloys (i.e., Ti, Cr, W, Al, TiN, TiW) and different deposition conditions were carried out in order to minimize the intrinsic and thermal stresses. A TiW 520-nm thick layer was found to be the optimum metal alloy, which allowed to increase the laser energy up to 650 mJ/cm$^2$ without severe cracks. Therefore, further enlargement of the Si island size with the Si mirror was limited to 5.4 µm, as this was the size obtained at this maximum allowable energy density.

### 5.1.4 Conclusions

We also investigated the effect of the thickness of an intermediate insulator layer as well as the influence of the energy density ratio of the top and bottom laser beams on the size of the location-controlled c-Si islands fabricated by DBTOP method. It was found that an increased volume of the bump in the intermediate oxide layer resulted in enlargement of the grain size. A location-controlled single c-Si island as large as 5.4 µm was positioned on the bump with a height of 120 nm and a diameter of 2.8 µm in the experiment with the Si mirror. A bump height of 280 nm and a bump diameter of 2.8 µm resulted in an 5.0-µm-large location-controlled c-Si island with an Al mirror.

Numerical heat flow analysis of the DBTOP structure confirmed that the increased Si island size could be attributed to the delayed onset of the

homogeneous nucleation event $t_{hom}$ during lateral grain growth. This delay occurs as a result of the decreased heat flux $q_{sub}$ from the molten Si towards the substrate with an increase in the intermediate insulator dimensions. The use of the Si mirror led to the utilization of higher laser energy densities, due to its lower reflectivity, thus leading to the higher temperatures of the underlying metal layer. Therefore, the reduction of the external heat flux and the solidification velocity of molten Si layer were more pronounced than these for an Al mirror. This phenomenon resulted in significantly larger Si islands for the same bump dimensions, i.e. 5.4 vs. 5.0 μm. Further enlargement of the Si island size was limited by the appearance of cracks in the underlying TiW layer and its peeling off due to the thermally induced stress by laser irradiation at a energy density higher than 650 mJ/cm$^2$. Therefore, the choice of the metal and its deposition conditions is crucial to the resulting maximum Si island size.

## 5.2 Processing window of DBTOP

This subchapter describes the processing energy density window of location-controlled c-Si islands fabricated by dual-beam excimer laser irradiation. The influence of the underlying oxide bump dimensions as well as the effect of the energy ratio of the laser beams on the processing window is investigated. The dimensions of the bump were varied in terms of its height and diameter. Different ratios of the top and bottom laser beam energy (i.e., $E_T/E_B$) were obtained by means of Al or Si mirrors, used to split and redirect the laser beam coming from the bottom to the top of the sample. The experimental results were also found to be in very good agreement with those of the 2D thermal simulation.

### 5.2.1 Laser beam non-uniformity

It is worth noticing that the state of the present-day laser technology restricts the applicability of technological processes which require uniform melting of Si films. At present, a typical excimer laser has a pulse-to-pulse variation of approximately ±5% [5.1], whereas the use of a more expensive large-aperture excimer laser [5.2] only offers a slight improvement. A standard beam homogenizer, used to improve the beam spatial uniformity, produces a pulse inhomogeneity of typically ±10%, or slightly less [5.2, 5.3]. The typical pulse spatial laser fluctuation of the homogenized single laser beam is illustrated in Fig. 5.6. It is observed that the laser energy distribution across a spot of 1 × 0.88 cm$^2$ is highly non-uniform, resulting in a colour pattern of recrystallized Si. The

approximate distributions of the laser energy intensities across the planes A-A and B-B are schematically shown above and on the right side of the photo.

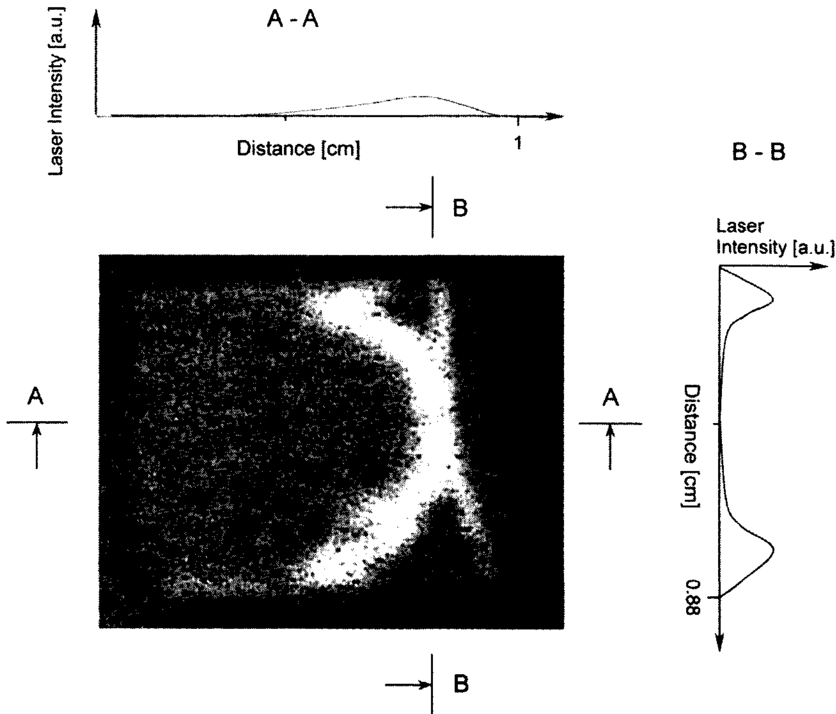


*Fig. 5.6 Optical microscope photo of laser-irradiated a-Si film with the XMR 7100, 308 nm laser system (single beam and homogenizer), showing spatial fluctuation of the laser pulse. The peripheral a-Si film has a dark grey colour, the SLG region is white, the microcrystallized Si film is light grey.*

## 5.2.2 Laser energy constraints of DBTOP

As was mentioned in Chapter 1.4, random location of large c-Si islands across the wafer deteriorates both the yield and uniformity of the resulting TFT devices. The method commonly referred to as the dual-beam with thick oxide portion (DBTOP) [5.4] to control the location of a c-Si island by a non-uniform lateral temperature profile was introduced and described in detail in Chapter 2.6.3. This temperature non-uniformity along the Si/$SiO_2$ interface was realized via an intentional local thickness variation in the underlying oxide layer. The ratio of the top/bottom laser energies was adjusted in such a way that both during and

after the laser pulse the thicker oxide portion always reaches a lower temperature than the surrounding thinner oxide (Fig. 2.12b). The size of an unmelted c-Si portion transformed into a crystal seed by the explosive crystallization of an initial amorphous material was determined by the temperature profile in the Si film immediately after the end of a laser pulse. Therefore, the resulting temperature gradient and concave temperature distribution along the Si/oxide interface near the center of the bump plays a crucial role in the formation of an unmelted c-Si seed with a desirable size. The steepness of the resulting temperature gradient near the center of the bump is responsible for maintaining such a desirable size within a wide range of laser energies.

However, the energy regime of DBTOP, which provides single Si grains of a 3.5 μm diameter, has a reportedly very narrow "processing window" of approximately 1.5% [5.4]. As has been explained before, this narrow window originates from the requirement *to maintain* an unmolten c-Si seed of a critical minimum size, initializing subsequent single grain growth, in a near-completely molten Si [5.4]. Because of the relatively small area of such a c-Si seed (i.e., 100-150 nm) exposed to the laser, homogeneity of the laser beam is very critical to DBTOP processing, implying stringent requirements to the pulse-laser system in terms of pulse-to-pulse variation and pulse spatial non-uniformity.

Despite the mentioned restriction the DBTOP method has potential to extend the conventional processing window of location-controlled Si grain fabrication by using optimized process parameters, even with the currently available laser technique. This can be explained as follows. In order to reduce the sensitivity of the remaining unmelted c-Si seed to the non-uniformity of the irradiated laser energy, the shape of the resulting concave temperature profile along the $Si/SiO_2$ interface at the center of the bump should be altered in such a way as to produce the highest (steepest) temperature gradient as possible. The steepness of the resulting temperature gradient is responsible for maintaining a desirable size of unmelted solid Si fraction, leading to the subsequent formation of a Si grain within a wide range of laser energies. The smallest c-Si seed has the highest probability of single grain initiation. Thus, due to the minimal variation of its size, the probability that a single location-controlled Si grain is formed remains very high even at severe laser energy fluctuations. This temperature gradient is determined by the geometry of the oxide bump as well as by the top/bottom laser energy ratio, which are the topics of interest here.

The aim of this chapter is to investigate the lower and upper boundaries of the processing energy density window of the location-controlled c-Si island fabricated by the DBTOP method. To that end the following structure was used: an a-Si / $SiO_2$ / metal stack with an array of bumps in the oxide. The dependence of the processing energy window of the location-controlled Si island on the dimensions of the thick intermediate oxide portion (i.e., the bump

diameter and the bump height) and the $E_T/E_B$ laser energy ratio in the DBTOP method have been investigated both experimentally and numerically.

### 5.2.3 Determination of actual laser energy density

Figure 5.7a shows the detailed schematics of the sample structure used in the DBTOP experiment. Figure 5.7b shows the resulting test structure, which was used to determine actual energy densities.

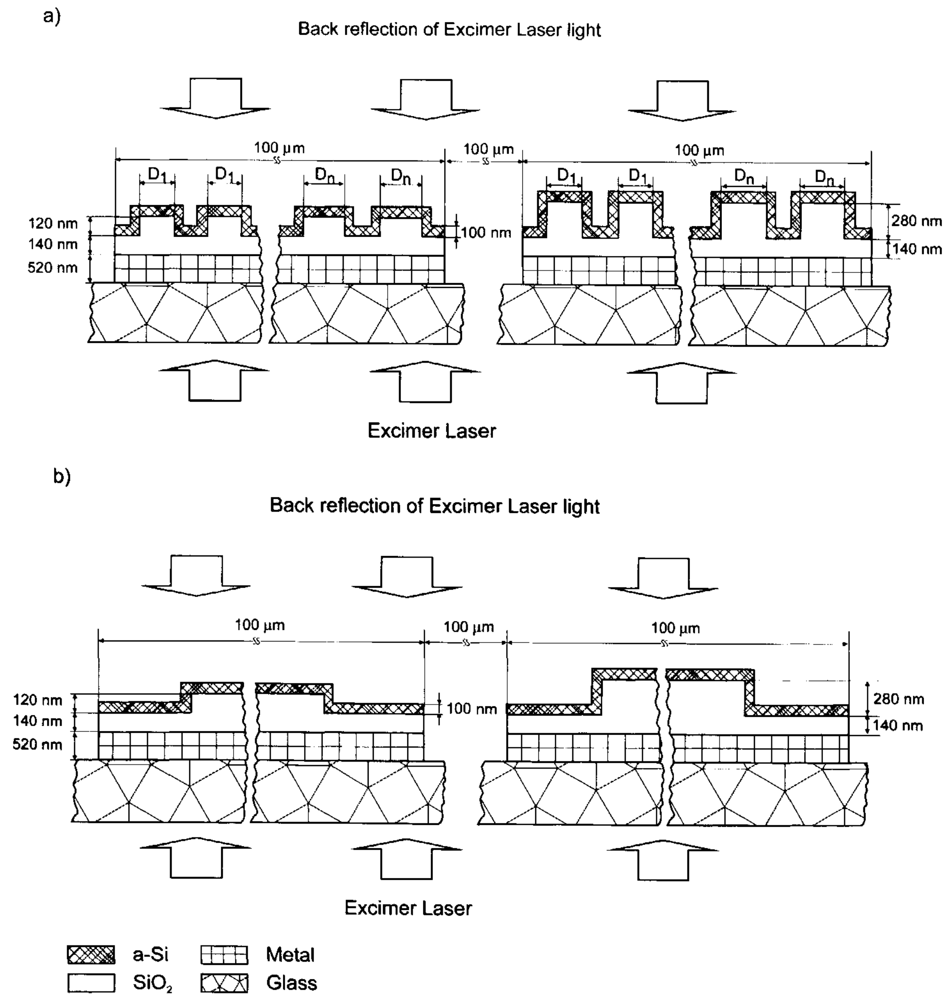


*Fig. 5.7 a)DBTOP tri-layer process and b)DBTOP tri-layer test structures.*

The estimated energy densities of the laser pulse $E_T$ to the top of the sample and $E_B$ to the bottom of the sample can be calculated as follows:

$$E_T = E_B R\,,\;\; E_B = \frac{I_0 T_0 T_{GL}}{XY}\,. \tag{5.2}$$

where $I_0$ is the primary laser energy, $T_0$ the total transmission of the optics, $T_{GL}$ the glass substrate transparency at the laser wavelength, $R$ the mirror reflectivity value, $X$ and $Y$ are the length and the width of the area irradiated on the sample, respectively. The spatial non-uniformity of the laser pulse on the wafer was estimated from the sheet resistance measurements of laser-irradiated n-implanted c-Si and was found to be approximately 10% (XMR 7100). In addition, the shading effect and interference of the laser beam add approximately 10% to the original laser beam non-uniformity. The interference occurs because of the laser light transmission through the glass substrate between patterned multi-layer islands. The shading effect occurs because the structure topology at the surface acts as a mask, shadowing a certain area of the sample from irradiation by the mirror-reflected laser beam. Since the total spatial non-uniformity of the laser pulse on the top of the wafer is approximately 20% and $I_0$ is not measured (in situ) directly, the calculated value of the energy density $E_T$ in Eq. (5.2) could deviate significantly from its actual value, which applies to the location-controlled Si island. Therefore, the actual $E_T$ was always measured on a fabricated planar test structure for every location-controlled Si island on an individual basis, as indicated schematically in Fig. 5.8.

An unique approach was used. Two threshold energies, required to melt a-Si film completely, were measured for different thicknesses of the underlying oxide, i.e., $E_{\mu_thin}$ for the thin layer and $E_{\mu_thick}$ for one of the thick oxides. Apparently, the measured values of the threshold energy densities for different oxide thicknesses can be considered as reference values, suitable to estimate the actual energies at which the location-controlled Si islands on the bumps occur. Knowing these values, energy densities required to produce location-controlled Si islands can be calculated exactly for any place on the structure, assuming the linear distribution of energy density, as follows:

$$E_{LCSG_{min}} = \frac{E_{\mu_thick} - E_{\mu_thin}}{L} X + E_{\mu_thin} \tag{5.3}$$

$$E_{LCSG_{max}} = \frac{E_{\mu_thick} - E_{\mu_thin}}{L} Y + E_{\mu_thin} \tag{5.4}$$

where $E_{LCSGmin}$ and $E_{LCSGmax}$ are the minimum and maximum energy densities, respectively, required to produce a location-controlled single c-Si island, $E_{\mu_thick}$ and $E_{\mu_thin}$ are the known threshold energy densities, required to melt an a-Si film completely on thick and thin oxide, respectively. $X$ and $Y$ are the positions

where complete melting of a-Si film on thick oxide and thin oxide occurred, respectively. $L$ is the distance between these places.

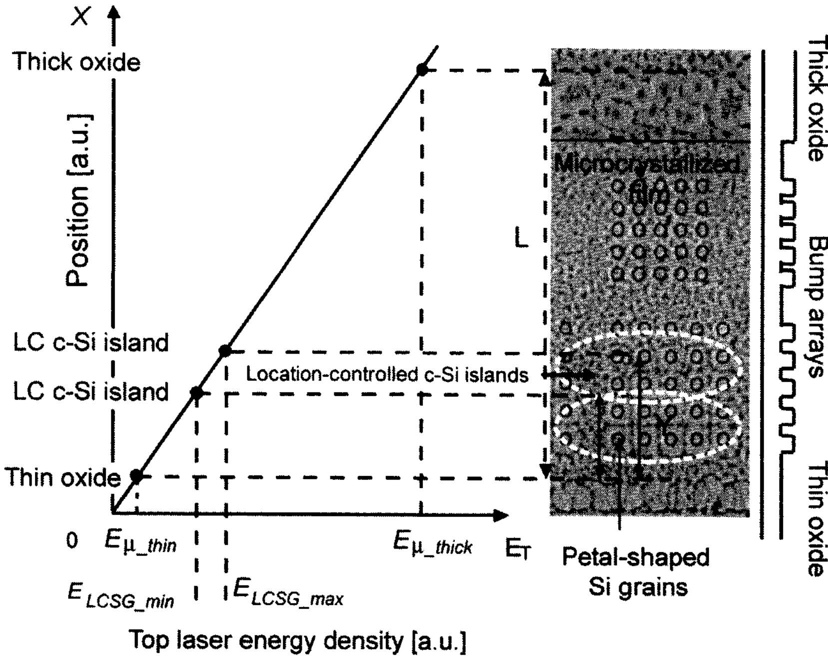


*Fig. 5.8* *Schematic representation of the actual top laser energy density $E_T$ of a location-controlled Si island as a function of its position. Lower bound $E_{LCSGmin}$ and upper bound $E_{LCSGmax}$ represent minimum and maximum energy densities for the LC Si island appearance, respectively. Threshold energies $E_{\mu_thin}$ and $E_{\mu_thick}$ are the energies required to melt a-Si film completely on thin and thick oxide layers, respectively.*

## 5.2.4 Results and discussion

Figure 5.9 illustrates the experimental laser energy densities used to obtain location-controlled single c-Si islands as a function of the bump height for bump diameters of 1.6, 2.0, 2.4 and 2.8 μm. In this case an Al mirror was used during dual beam irradiation. Figure 5.10 illustrates the same data but obtained with a Si mirror. Open squares indicate experimentally observed energy densities required to produce location-controlled Si islands. The purpose of presenting the

data in this format is to visualize the representation of lower and upper bounds of the location-controlled Si island appearance. The shaded areas between these boundaries indicate the energy densities resulting in location-controlled Si islands.

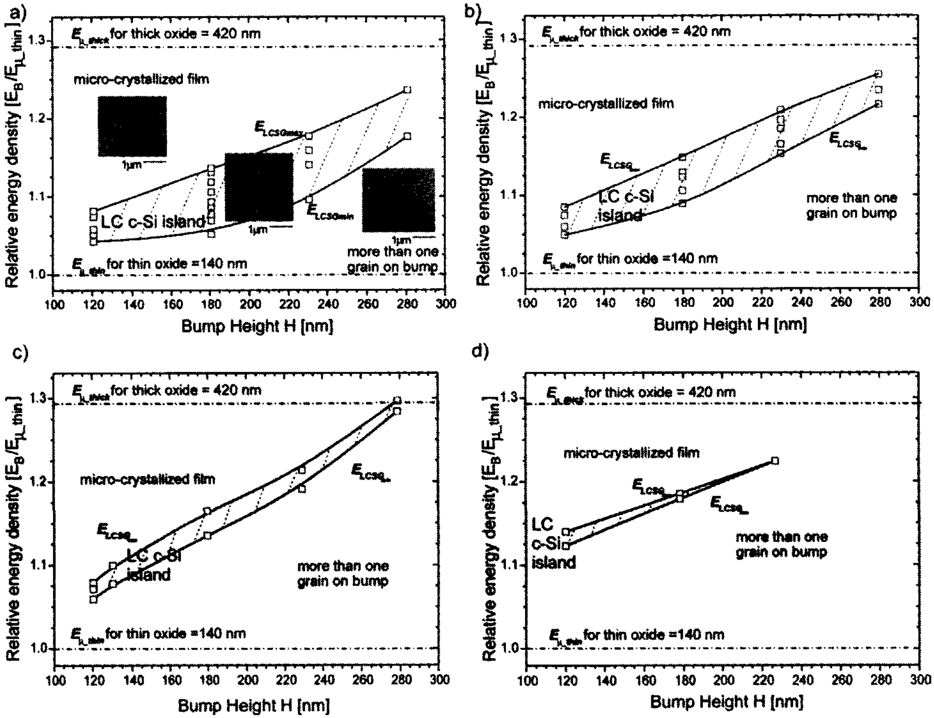


*Fig. 5.9* *Experimentally observed laser energy densities of a location-controlled single c-Si island as a function of the bump height for bump diameters of 1.6 (a), 2.0 (b), 2.4 (c) and 2.8 μm (d). An Al mirror was used during dual beam irradiation. Threshold energies required to melt a-Si film completely on thin and thick oxide layers (measured on a test structure) are shown as dashed-dotted lines for $E_{\mu_thin}$ and $E_{\mu_thick}$, respectively.*

It is worth noticing that in Fig. 5.10 the relative energy density is the ratio between $E_B$ and $E_{\mu_thin}$, obtained with an Al mirror. As shown in Fig. 5.9 and Fig. 5.10, with energy densities above $E_{LCSGmax}$, the entire film becomes micro-crystallized, as spontaneous nucleation immediately takes place after completely melting of a-Si film [5.4]. With energy densities below $E_{LCSGmin}$, more than one grain has grown on and around the oxide bump, because the maximum reached temperature along the $Si/SiO_2$ interface on the top of the bump was not

sufficient to reduce the solid area sufficiently to leave only one single seed. Therefore, numerous small grains had grown in the centre of the bump, with large radially grown grains in their periphery, forming so-called "petal-shaped" Si grains [5.4]. The gradual increase in both $E_{LCSGmax}$ and $E_{LCSGmin}$ with the $H$ value can be explained in terms of an increased heat capacity of the oxide bump. The higher the bump, the more energy is required to form a concave temperature profile along the a-Si /oxide interface over the bump, in such a way that the low-temperature area is then small enough to leave only one single c-Si seed for subsequent location-controlled Si island growth.

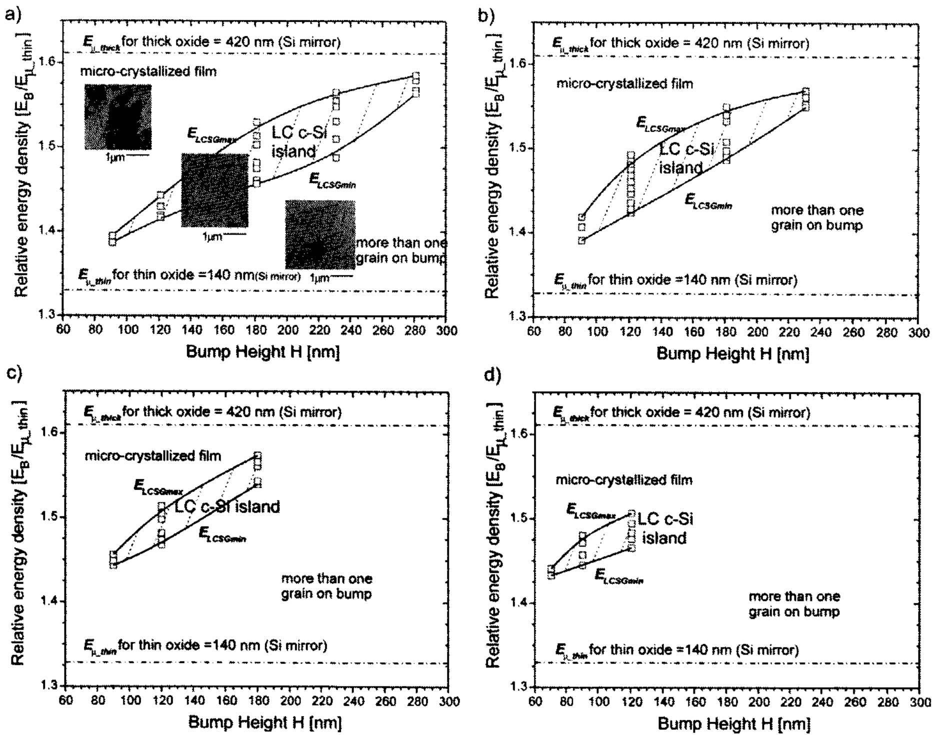


*Fig. 5.10* *Experimentally observed laser energy densities of a location-controlled single c-Si island as a function of the bump height for the bump diameters of 1.6 (a), 2.0 (b), 2.4 (c) and 2.8 µm (d). A Si mirror was used during dual beam irradiation. Threshold energies required to melt a-Si film completely on thin and thick oxide layers (measured on a test structure) are shown as dashed-dotted lines for $E_{\mu_thin}$ and $E_{\mu_thick}$, respectively. The relative energy density was calculated with respect to $E_{\mu_thin}$, obtained with an Al mirror.*

From Fig. 5.9 and Fig. 5.10 one can see that by changing from an Al to a Si mirror, the relative energy densities for $E_{\mu_thin}$ and $E_{\mu_thick}$ could be increased from 1 to 1.33 and from 1.29 to 1.62, respectively. The reason for this is the decreased reflectivity of the Si mirror (60%) compared to that of the Al mirror (94%). In order to melt the top a-Si film completely using DBTOP with the Si mirror, a substantial increase in the bottom laser energy density is required both for thin and thick oxide layers. Note that laser energy densities $E_{LCSGmax}$ and $E_{LCSGmin}$, required to produce a location-controlled c-Si island are also significantly higher than those for DBTOP with an Al mirror.

The experimentally observed energy densities were visualized in the form of a processing energy density window for location-controlled Si island formation. Generally, the processing window is a figure of merit used to describe the optimum range of technological parameters for a certain process. In this case the processing window is the optimum energy density range required to produce location-controlled Si islands by the DBTOP method. The width is thus determined by taking the ratio of the difference between the upper bound energy $E_{LCSGmax}$ and the lower bound energy $E_{LCSGmin}$, over the lower bound energy $E_{LCSGmin}$, expressed in percentage.

Figure 5.11 illustrates the processing windows for a location-controlled single c-Si island as a function of the bump height for bump diameters of 1.6, 2.0, 2.4 and 2.8 μm (i.e., open symbols). Figures 5.11a and 5.11b represent the data obtained with an Al and the Si mirrors, respectively. Typically, the processing window shows a set of convex curves for every bump diameter. Apparently, the maximum of the processing window shifts towards a higher bump height with decreasing bump diameter.

Figure 5.12 shows a SEM photograph of an array of five location-controlled adjacent single c-Si islands, fabricated by the DBTOP method with an Al mirror. The process conditions were as follows: bump width of 1.6 μm, bump height of 180 nm, and the spacing between bumps of 4 μm. Under these conditions a processing window of 6.8% was found, the highest value in Fig. 5.11a.

Figure 5.13 shows a SEM photograph of three location-controlled adjacent single c-Si islands fabricated by the DBTOP method with the Si mirror. The process conditions were as follows: bump width of 2.0 μm, bump height of 120 nm, and the spacing between bumps of 4 μm. This resulted in a processing window of 4.3%.

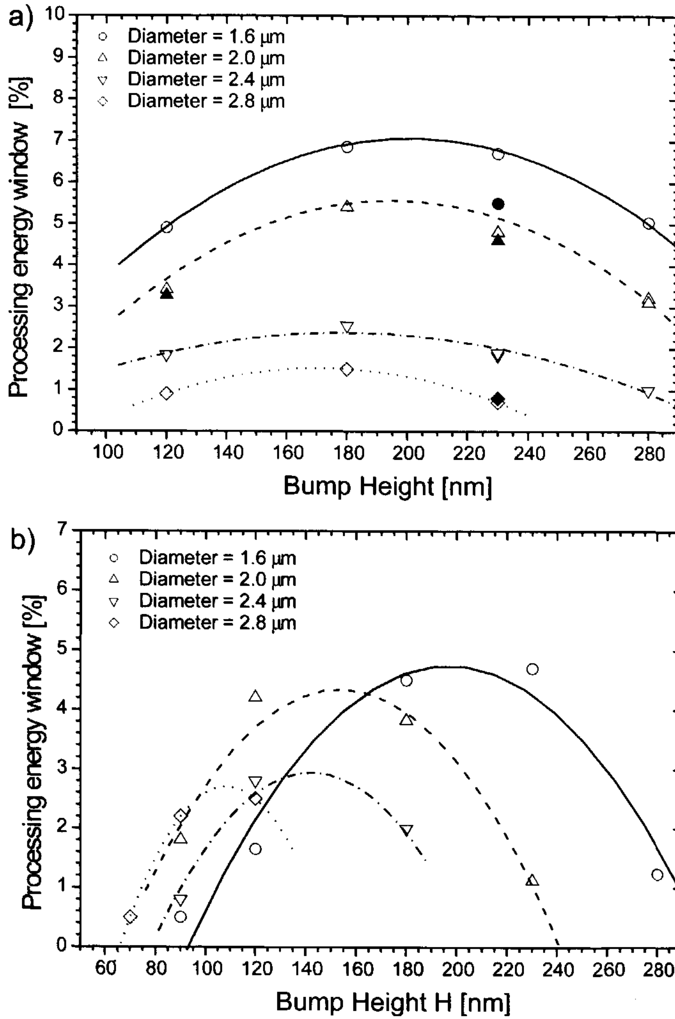


*Fig. 5.11* *Process energy density windows of location-controlled single c-Si islands as a function of the bump height, experimentally obtained using various bump diameters with (a) Al and (b) Si mirrors (open symbols). Numerically calculated energy densities are indicated as solid symbols.*

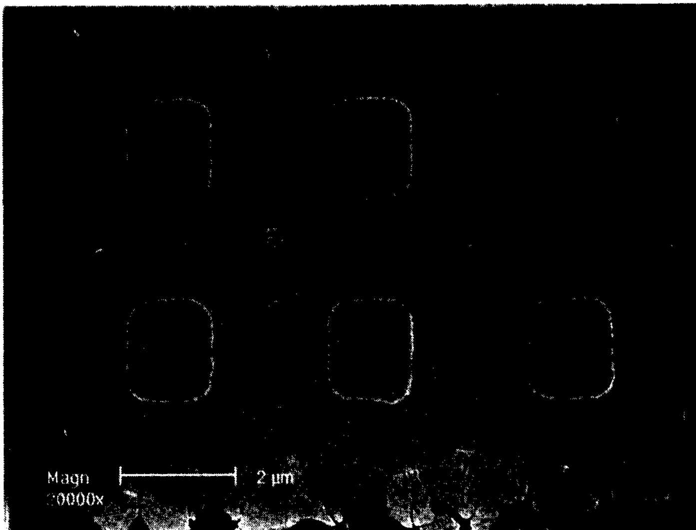


*Fig. 5.12 SEM image of an array of location-controlled adjacent single c-Si islands, obtained within the process energy density window of 6.8% (Al mirror). The bump height is 180 nm, the bump width is 1.6 µm, and bumps are represented as square areas underneath the Si film.*

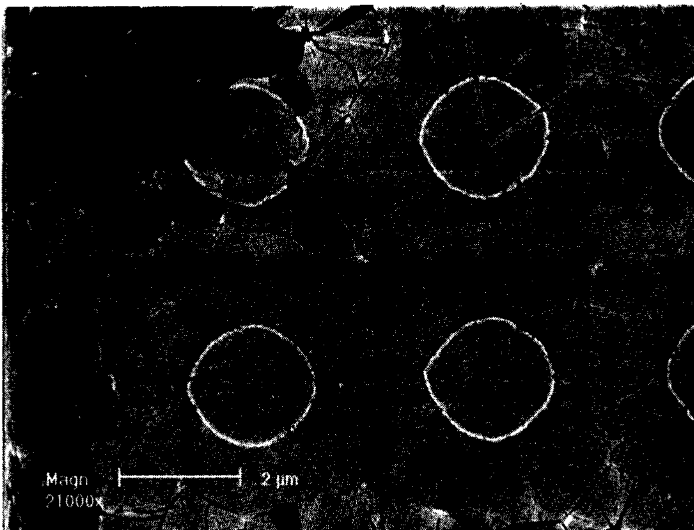


*Fig. 5.13 SEM image of an array of location-controlled adjacent single c-Si islands, obtained within the process energy density window of 4.3% (Si mirror). The bump height is 120 nm, the bump width is 2.0 µm, and bumps are represented as circle areas underneath the Si film.*

Figure 5.14 shows an AFM photograph of five location-controlled adjacent single c-Si islands shown in Fig. 5.12. The underlying square oxide bumps surrounded by grain boundaries (visible as hillocks) are clearly visible. One can also see that substantial mass transport has occurred in the Si film, caused by the lateral solidification, inducing an accumulation of material where the four islands collapse (quadriple junction). The resulting protrusions can be as high as 200 nm. This photograph reveals that grain boundaries of adjacent islands are located exactly between the oxide bumps, which enables the DBTOP method to control the position of the grain boundaries as well as the grain location.

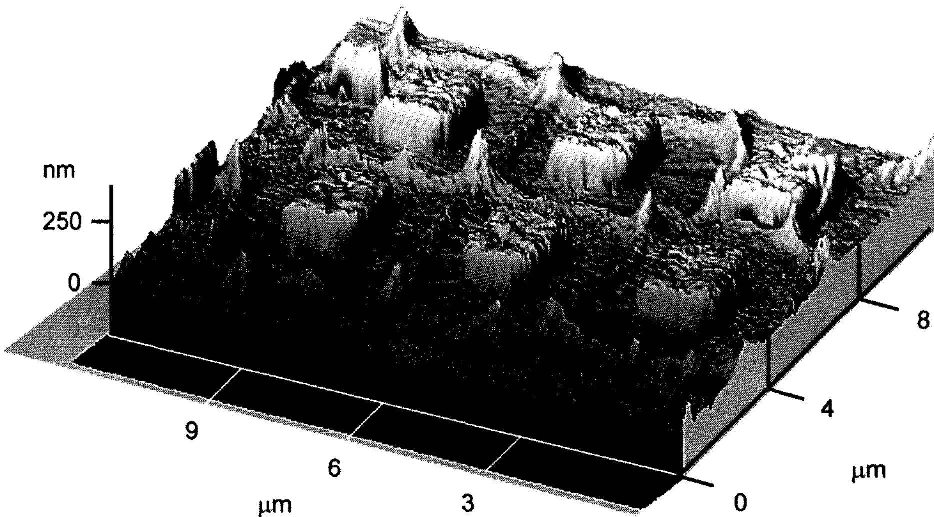


*Fig. 5.14* *AFM photograph of five location-controlled adjacent single c-Si islands on square bumps, shown in Fig. 5.12. Collision of grain boundaries results in hillocks.*

Figure 5.15 shows the surface topology across the centers of the three location-controlled adjacent single c-Si islands from Fig. 5.14. Sidewalls of underlying bumps, covered with Si layer, are slightly tilted (7-15°) from the vertical axis as a result of wet etching of the oxide. Grain boundaries of location-controlled Si islands are shown as small hillocks between bumps.

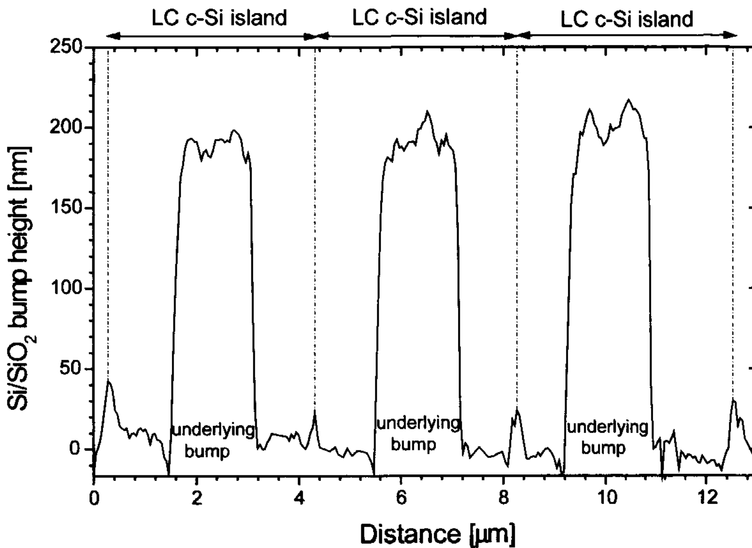


*Fig. 5.15* *Surface topology across the centers of the three location-controlled adjacent single c-Si islands from Fig. 5.14. Sidewalls of underlying bumps, covered with Si layer, are slightly tilted (7-15°) from the vertical axis as a result of wet etching of oxide. Grain boundaries of location-controlled Si islands can be seen as hillocks between bumps.*

## 5.2.5 Numerical simulation and discussion

### 5.2.5.1 Model definition

In order to estimate the energy density range to obtain location-controlled Si islands and to compare this range with experimentally obtained processing window, 2D heat flow analysis was performed. A stacked structure of a 100-nm thick Si layer, a 140-nm thick $SiO_2$ layer (thin oxide), and a 520-nm thick TiW layer on a glass substrate were assumed. Structure schematics, material properties and boundary conditions can be found in Chapter 4.2.1. The diameters of the circular bumps varied from 1.6 to 2.8 µm, while the heights of the bump structures were chosen as 120, 230 and 280 nm. The oxide bump dimensions used in the simulations are summarized in Table 5.1.

The resulted temperature field distributions were numerically obtained with commercially available MSC software [4.22] coupled with custom user

subroutines. The simulated oxide bump topology was built in accordance with AFM scan data and is consistent with the experimental topology observations (i.e., the sidewall angle, bump height and diameter, etc.)

The adaptive meshing technique was used in the areas of high thermal gradient in order to obtain a more accurate solution of the thermal diffusion equation. The top energy density of the laser pulse $E_T$ was estimated according Figure 5.8. All the simulations were performed only for an Al mirror (i.e., reflectivity of 94%).

Figure 5.16 shows the simulated transient temperature profile near the center of the bump after the end of a laser pulse for the bump diameter of 2.0 μm and the bump height of 230 nm. Curved solid and dashed lines indicate the positions of the solid/liquid interface at different laser energies ranging from $1.15 \times E_{\mu_thin}$ to $1.212 \times E_{\mu_thin}$ with 24 steps. The inward and outward curved solid lines represent the position of the solid/liquid interface for the upper bound $E_{LCSGmax}$ and lower bound $E_{LCSGmin}$, respectively. The horizontal dot-dashed lines indicate the phase transition temperature region, where the latent heat is absorbed/released. Vertical dotted lines indicate the size of the unmelted c-Si seed, $c_{min}$ and $c_{max}$.

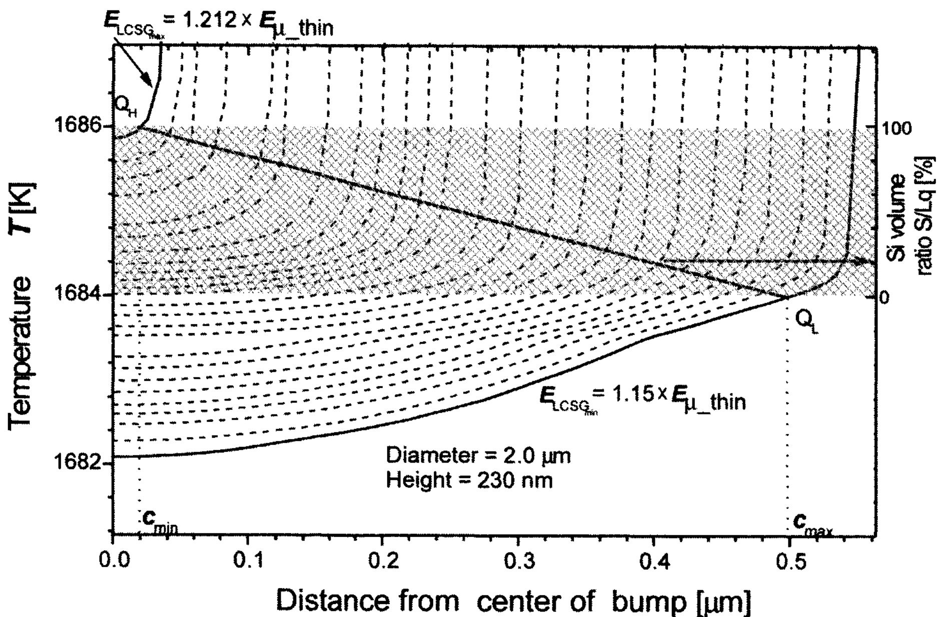


*Fig. 5.16* *The simulated transient temperature profiles along the $Si/SiO_2$ interface near the center of the bump that resulted after a 66 ns laser pulse. The linear dependence of the liquid/solid Si volume ratio vs. the average energy density is shown on the right axis.*

As was shown in Fig. 5.9, and Fig. 5.10, the critical energies for location-controlled single Si island fabrication determine the size of the c-Si seed. In order to determine numerically the upper bound energy $E_{LCSGmax}$ and the lower bound $E_{LCSGmin}$, we chose an unmelted c-Si seed size range from 0.04 to 1 μm. The size of unmolten c-Si seed was determined by the position of the solid/liquid interface in the transition phase between $T_S$ = 1684 K and $T_L$=1686 K. Note that the minimum c-Si solid size of 0.04 μm was determined by mesh resolution of our model (i.e., 20 nm-cell times 2 due to the model symmetry). However, the solid/liquid interface position is difficult to define uniquely since there is an uncertainty about the melting state at $T=T_m$, and criteria for definition of solid and molten fraction in the transition state should be carefully chosen.

In this program, any c-Si seed undergoing the transition phase (between $T_S$ = 1684 K and $T_L$ = 1686 K) should have a finite number of solid Si islands, where the minimum total energy per unit volume for melting, $Q_L$, can be written as:

$$Q_L = C_{Si} T_m \tag{5.5}$$

where $C_{Si}$ is the heat capacity of c-Si. These solid Si islands are surrounded by a molten Si area with a maximum total energy per unit volume $Q_H$, expressed as:

$$Q_H = C_{Si} T_m + L_f \quad at \quad T = T_m \tag{5.6}$$

where $L_f$ is the latent heat of silicon per unit volume. The dependence of the liquid/solid Si volume ratio on the average energy density for a bump diameter of 2.0 μm and a bump height of 230 nm is shown in Fig. 5.16, right axis. The ratio is zero with the minimum total energy of $Q_L$ and approaches 100% linearly at the maximum total energy of $Q_H$ [5.7]. In other words, the transition temperature region has both solid regions and molten regions, which cannot be clearly divided numerically. The upper bound $E_{LCSGmax}$ and the lower bound $E_{LCSGmin}$ of the energy density are defined by the condition that the Si film can accumulate energy of $Q_H$ (for the minimum solid c-Si size) and $Q_L$ (for the maximum solid c-Si size), respectively. The aforementioned numerically calculated energy densities for a bump diameter of 2.0 μm and a bump height of 230 nm are presented in Fig. 5.11a in the form of a processing window as indicated by the solid symbols. As can be seen, the experimentally obtained processing windows are in very good agreement with the numerical simulation.

#### 5.2.5.2 Effect of the $SiO_2$ bump diameter on the processing window of a location-controlled single c-Si island

As follows from Fig. 5.11a, the maximum processing window increases with decreasing bump diameter. This type of behaviour can be explained in terms of simulated temperature profiles along the $Si/SiO_2$ interface immediately after a

laser pulse, as shown in Fig. 5.17. Here, the temperature distributions for bump diameters of 1.6 and 2.8 μm are plotted as solid and dashed curves, respectively, while the bump height was kept at 230 nm. The applied laser energy density was equal to the $E_{LCSGmax}$ for each bump diameter.

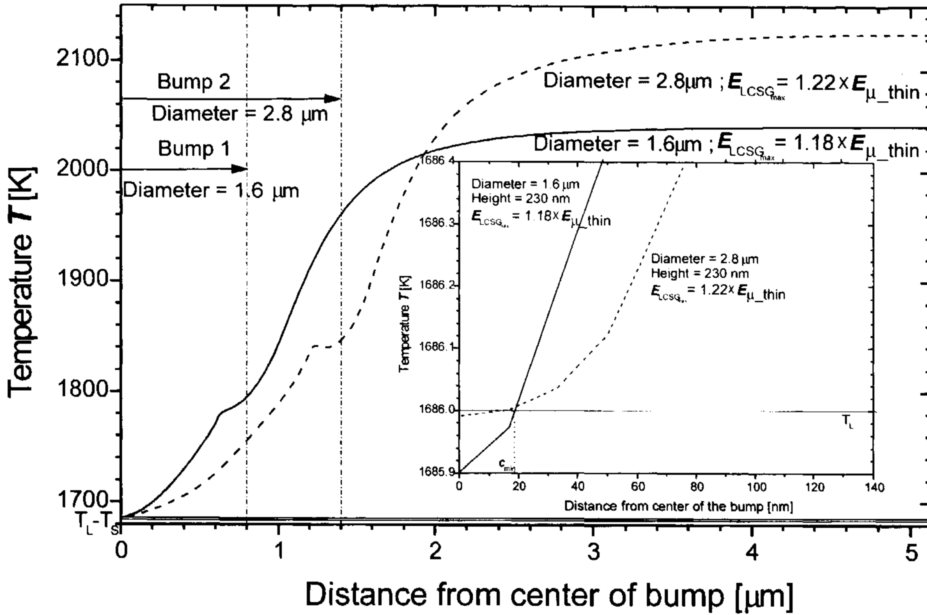


*Fig. 5.17* *Simulated transient temperature profiles along the $Si/SiO_2$ interface near the center of the bump for bump diameters of 1.6 (solid curve) and 2.8 μm (dashed curve) that resulted after a 66 ns laser pulse. The position at $c_{min}$ = 40 nm (due to the model symmetry) is indicated by dotted line.*

From the enlarged view of phase transition area in Fig. 5.17 it follows that for a 1.6-μm bump diameter the slope of the temperature profile is steeper than that for a 2.8-μm bump diameter. The steeper temperature gradient has a better possibility to create unmolten c-Si seeds, with minimal possible size deviations from their critical values at different laser energy densities, than the gradual temperature profile for the bump diameter of 2.8 μm, as was explained in Chapter 5.2.2. The aforementioned explanation is in very good agreement with the experimental data for DBTOP with an Al mirror. As follows from Fig. 5.11a, the bump diameter of 1.6 μm results in the highest obtained processing windows ranging from 4.9 to 6.8%. When the bump diameter increases, the concave temperature profile becomes more gradual on the top of the bump, as indicated in Fig. 5.17 for the bump diameter of 2.8 μm. Therefore, the processing

window is narrow, between 0.9 and 1.5% for this bump diameter, as illustrated in Fig. 5.11a.

This explanation is also valid for the processing window of DBTOP with the Si mirror, illustrated in Fig. 5.11b. One can see that the bump diameter of 1.6 µm also results in the highest obtained processing windows ranging from 1.7 to 4.7%. The increase in the bump diameter leads to the more gradual concave temperature profile along the $Si/SiO_2$ interface on top of the bump. As was shown above, such behaviour of the temperature gradient increases the sensitivity of the unmelted c-Si seed, indicated in Fig. 5.11b for a 2.8-µm bump diameter. Accordingly, the processing window becomes narrow, ranging between 0.5 and 2.5% for this bump diameter.

In the case of our structure the edge of the bump can be approximated as a boundary between the heat diffusion source and the media. The steepest temperature profile is obtained when the distance between the heat sources in the bump becomes equal to twice the heat diffusion length $L$ of molten Si, due to the model symmetry. Thus, this value should be expressed as:

$$2L = 2\sqrt{D_{Si}t} = 2\sqrt{\frac{k_{Si}}{C_{Si}}t} = 1.5\mu m \tag{5.7}$$

**where $D_{Si}$ is the diffusion constant of Si, $C_{Si}$ is the thermal heat capacity of Si, $k_{Si}$ is the thermal heat conductivity of Si, $t$ is the laser pulse duration. Indeed, with average $C_{Si}$ and $k_{Si}$ parameters (taken from Fig. 4.4, Chapter 4.2.1.2), this value is very close to the bump diameter of 1.6 µm, which gives the maximum obtained processing window in our experiment.**

### 5.2.5.3 Effect of the $SiO_2$ bump height on the processing window of a location-controlled single c-Si island

As illustrated in Fig. 5.11, for a fixed bump diameter, the processing window first increases monotonically with increasing bump height, reaches a maximum, and then gradually decreases. The reason for such behaviour stems from the simulated temperature profile along the $Si/SiO_2$ interface after a laser pulse, as shown in Fig. 5.18. Here, the temperature distributions for bump heights of 120 and 280 nm are plotted as dashed and solid curves, respectively, while the bump diameter was kept at 2.0 µm. Applied laser energy densities were equal to the upper bound $E_{LCSGmax}$ and lower bound $E_{LCSGmin}$ for each bump height.

As illustrated in Fig. 5.18, the larger the bump height, the greater the difference between the temperature on top of the bump and that outside the oxide bump (i.e., along Si/thin $SiO_2$ interface). It stems from the fact that the heat capacitance of the underlying bump increases with the oxide thickness,

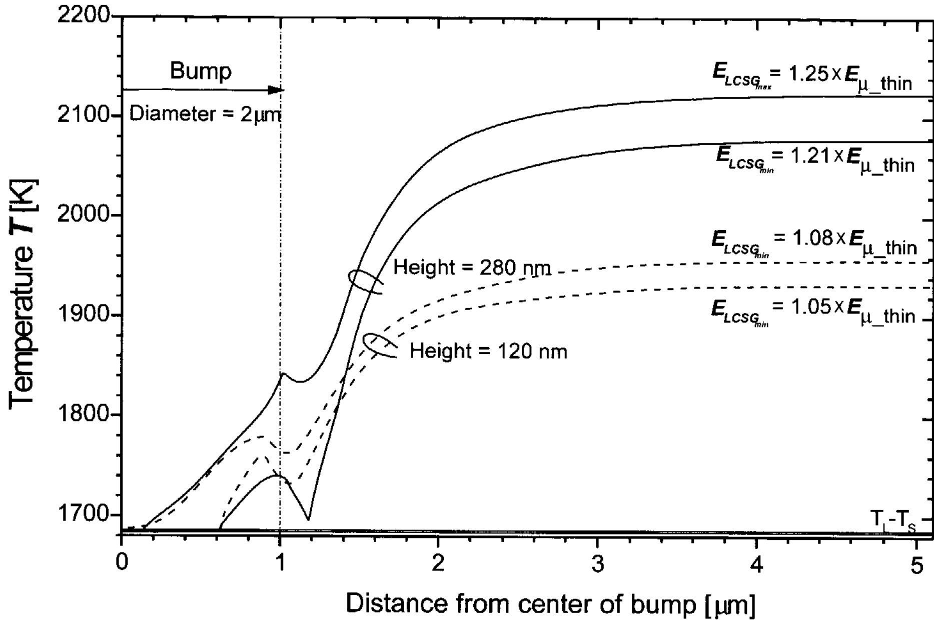


*Fig. 5.18* *Simulated transient temperature profiles along the Si/SiO$_2$ interface near the center of the bump for bump heights of 280 (solid curve) and 120 nm (dashed curve) that resulted after a 66 ns laser pulse. The bump diameter was fixed at 2.0 μm.*

requiring more laser energy to keep the a-Si layer on the center of the bump (i.e, at Si/SiO$_2$ interface) at the same temperature as that on the thinner oxide.

At the upper bound $E_{LCSGmax}$ for the bump height of 280 nm this results in a steeper temperature profile with a sharp low-temperature part than that for the bump height of 120 nm. As was explained before, the steeper temperature profile provides less sensitivity of the unmolten c-Si seed with respect to the laser energy density, thus leading to a wider processing window.

From Fig. 5.18 one can see that concavity of the temperature profile near the center of the bump for the bump height of 280 nm is deteriorated, as the laser energy decreases to the lower bound $E_{LCSGmin}$. As a result, the temperature drops substantially near the oxide bump edge. Due to this local temperature drop, the temperature slope for the bump height of 280 nm decreases, resulting in a higher sensitivity of the unmelted c-Si seed near the lowest laser energy $E_{LCSGmin}$ and therefore, in a smaller processing window. The local temperature drop was caused by the effectively increased Si thickness at the sidewall of the bump, as schematically shown in Figure 5.19.

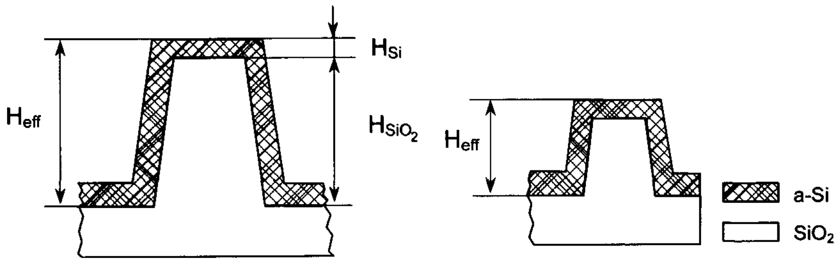


*Fig. 5.19 Increased effective thickness of Si film due to the surface topology.*

The effective thickness $H_{Si_eff}$ of the Si layer can be defined as:

$$H_{Si_eff} = H_{SiO_2} + H_{Si} \tag{5.8}$$

where $H_{SiO2}$ is the bump height and $H_{Si}$ is the actual thickness of the Si film. As follows from Eq. (5.8), the effective thickness $H_{Si_eff}$, which covers the walls of the bump, becomes significantly higher with increasing bump height.

### 5.2.5.4 Effect of Al and Si mirrors on the processing window of a location-controlled single c-Si island

Fig. 5.11 shows that the maximum processing window of DBTOP with an Al mirror is wider than that obtained with the Si mirror. Furthermore, as for the Si mirror the curves are more convex and the local maxima differ more greatly from one another; it is clear that with this mirror the processing windows of DBTOP are more sensitive to bump height and diameter variations than when an Al mirror is used.

These phenomena are attributed to the lower reflectivity of the Si mirror (60%), requiring more laser energy to keep the Si film at the same temperature as with the use of an Al mirror (94%). Figure 5.20 shows simulated temperature distributions obtained with the Si mirror for a bump diameter of 1.6 μm and a bump height of 280 nm after the end of laser pulse and a few nanoseconds later. (It is worth noticing that all simulations before were performed for an Al mirror.) The applied laser energy density was slightly higher than the upper bound $E_{LCSGmax}$ for this bump diameter. One can see that after 1 ns after the end of laser pulse, the temperature in the center of the bump rises sufficiently to melt a part of the remaining c-Si solid seed. At the same time slight heating also occurs in the periphery of the bump center. At 68 ns the temperature keeps rising, both at the center and at the peripheral area, leading to complete melt of the remained c-Si solid seed at 69 ns (i.e., 3 ns after the end of laser pulse).

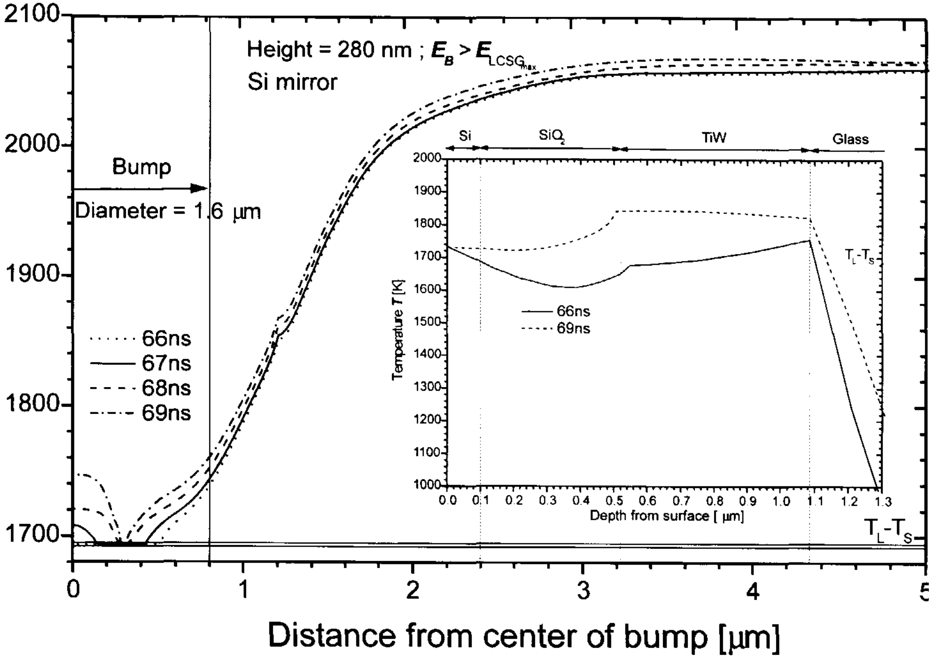


*Fig. 5.20* *Simulated lateral temperature distributions obtained with Si mirror for a bump diameter of 1.6 µm and a bump height of 280 nm after the laser pulse and a few nanoseconds later. Insert of Figure: Simulated vertical temperature profile at different time steps.*

The aforementioned heat flow behaviour can be explained from the vertical heat diffusion mechanism, also shown in Fig. 5.20. It can be seen that the temperature of the underlying TiW and oxide layer at 69 ns is much higher than that at 66 ns. The lower $E_T/E_B$ energy ratio (i.e., low reflectivity of the Si mirror) means that more laser energy is applied on the back side of the wafer, thus meaning that more energy is stored in the bottom TiW layer. In this way heat diffusion initiates from the bottom, i.e., heat diffuses from TiW into the intermediate oxide layer. If the bottom energy increases, this excessive heat accumulated in the thin oxide layer diffuses laterally into the molten Si towards the bump, causing undesirable heating of Si film after the laser pulse.

As a result, the initial concave temperature profile deteriorates. This results in lowering of upper bound $E_{LCSGmax}$, therefore leading to a narrower maximum processing window (4.7%) compared with that of an Al mirror (6.8%).

### 5.2.6 Conclusions

The processing energy density window of the DBTOP method of location-controlled c-Si island fabrication was investigated experimentally and theoretically. The effect of the process parameters, i.e., the oxide bump height, bump diameter and top/bottom laser energy ratio ($E_T/E_B$) was examined. It was shown that by optimizing these process parameters, the processing window of DBTOP can be significantly increased. The widest processing windows of 6.8 and 4.7% were obtained with an Al mirror (i.e, reflectivity of 94%) and the Si mirror (i.e, reflectivity of 60%), respectively, for a bump with a 180-nm height and 1.6-μm diameter. The Si islands obtained within these processing windows were as large as 4.2-4.7 μm for DBTOP with an Al mirror and 4.9-5.0 μm for DBTOP with the Si mirror. The upper energy bound of the location-controlled c-Si island, $E_{LCSGmax}$, is determined by microcrystallization of the entire Si film, while the lower energy bound $E_{LCSGmin}$ is determined by multiple petal-shaped grain appearance.

The experimental results were also found to be in very good quantitative agreement with the numerical simulation based on the resolution of the two-dimensional heat flow equation. This fact proves the overall capability of the thermal model and demonstrates its applicability to simulate laser-initiated processes in Si film.

# Chapter 6

# *Crystallographic orientation control*

This chapter describes nickel-induced crystallization (NIC) of amorphous silicon, which was performed in order to control the crystallographic orientation of the Si film. The crystallization was done by solid-phase crystallization (SPC). SPC combined with excimer-laser anneal (ELA) was applied to NIC Si films in order to reduce the crystalline defect density appearing in SPC Si films. The effect of the Ni film thickness, the annealing temperature and duration, and the laser energy density on NIC Si film microstructure were investigated.

## 6.1 Results and discussion

### 6.1.1 Experimental conditions

Films of Ni with a thickness of 5 or 20 nm were deposited on top of an a-Si layer by RF sputtering. The deposition details are described in the Appendix (Table 7.2). The NIC samples were crystallized at 560 °C for various time durations. In some cases, the samples were subjected to a thermal pre-anneal at 250 °C for 10 minutes before the SPC procedure. The aim of pre-anneal was to initially obtain $Ni_2Si$ silicide, which is the first phase to be formed at temperatures below 500 °C on a-Si [6.1]. NIC samples with different Ni thicknesses were also subjected to ELA with energy densities varying from 336 to 460 mJ/cm$^2$. The experimental conditions of NIC are summarized in Table 6.1.

*Table 6.1 Experimental conditions of NIC Si films.*

| # | Thickness [nm] | Pre-anneal | SPC | LA |
|---|---|---|---|---|
| 1 | 5 | no | 20 hrs at 560 °C | no |
| 2 | 5 | no | 20 hrs at 560 °C | yes |
| 3 | 20 | 10 min at 250 °C | 2 hrs at 560 °C | no |
| 4 | 20 | no | 2 hrs at 560 °C | no |
| 5 | 20 | no | 8 hrs at 560 °C | no |
| 6 | 20 | no | 14 hrs at 560 °C | no |
| 7 | 20 | no | 20 hrs at 560 °C | no |
| 8 | 20 | no | 20 hrs at 560 °C | yes |

### 6.1.2 Effect of the Ni film thickness

Figure 6.1 shows planar and cross-sectional TEM images of NIC Si films for 5- and 20-nm thick Ni layers, respectively. The both samples (i.e., #1 and #7 from Table 6.1) were crystallized at 560 °C during a 20 hour anneal. Annealing at temperatures above 500 °C results in the formation and epitaxial growth of the $NiSi_2$ phase [6.2]. Therefore, Ni should have been transformed into the nickel disilicide. Subsequently, the silicide phase formations depend on the silicon-to-nickel ratio.

Generally, three distinct regions are visible:

1) the darkest contrast area, which is supposed to be the silicide region (i.e., originally covered by Ni);

2) surrounding gray regions of silicide-rich Si;

3) peripheral areas of silicide-poor Si with the brightest contrast.

An annealed NIC Si film has an uniform smooth surface, an equiaxed microstructure free of lattice strain and a nearly random distribution of grain orientations. The grain size at the surface varies between 20 and 40 nm. As illustrated in Fig. 6.1b for a 5-nm thick Ni layer, Ni migrates through the Si film along the crystal defects in the Si grain boundaries. The Ni diffuses approximately three times faster along the Si grain boundary than along other defects in the bulk [6.2], resulting in the bordering of Si grains. It is obvious that the increase in defect density in silicon should lead to an acceleration of nickel diffusion in the silicon lattice.

For the NIC sample with a 20-nm thick Ni film shown in Fig. 6.1c, d, the migration of Ni from the Si surface towards the bulk occurs in a uniform

manner. The V-shaped grains grow towards the film surface. The microstructure is more textured compared to that of the 5-nm thick NIC sample. The grain size is non-uniform and varies at the surface between 50 and 250 nm. Sometimes the evidence of secondary crystallization on the surface or in the bulk and twinning of silicide-poor Si grains was observed.

It is worth noticing that Fig. 6.1b and 6.1d do not show evidence of a well-defined silicide layer nor of any amorphous phase. This may be due to inadequate removal of oxide from the Si surface prior to deposition, or possibly it may be due to oxide incorporation at the onset of Ni deposition. As can be seen, both samples are completely crystallized and exhibit a small grain structure instead of the often reported needle-like crystallites, left in trails of migrating $NiSi_2$ precipitates [6.3, 6.4].

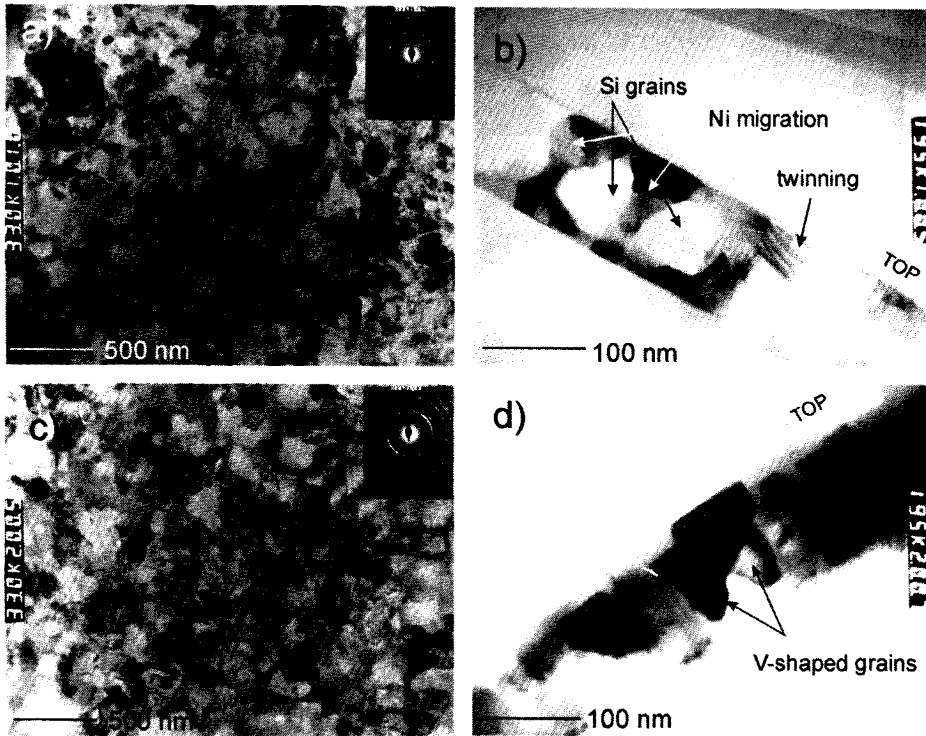


*Fig. 6.1 Bright-field TEM images of NIC Si films with a Ni layer of 5 nm (a, b) and 20 nm (c, d).*

In general, several phase transformation mechanisms of NIC Si films have been reported, which depend on the Ni area density [6.5]. The needle-like crystallites formed by the lateral migration of $NiSi_2$ precipitates are only

observed when the Ni density on a-Si film is very low, i.e., $3.3\times10^{13}$ atoms/cm$^2$. The high density of Ni atoms on a-Si, i.e., ~ $5.7\times10^{14}$ atoms/cm$^2$, leads to a small equiaxed grain microstructure. Experiments in this study were performed in the high-density Ni regime (i.e., ~ $1.6\times10^{15}$ atoms/cm$^2$), where the latter morphology was observed in Fig. 6.1b and 6.1d. Cross-section TEM photos also show that the concentration of Ni is homogeneous throughout the film, and there does not appear to be any excess metal on the film surface. It is possible that crystallization starts at the Si-metal interface, and only when complete crystallization has taken place, the metal diffuses throughout the film.

The crystallinity of the NIC Si films coated with films of various Ni thicknesses was checked by XRD measurements. Figure 6.2 shows the resulted XRD spectrum of the NIC Si films (background is not corrected).

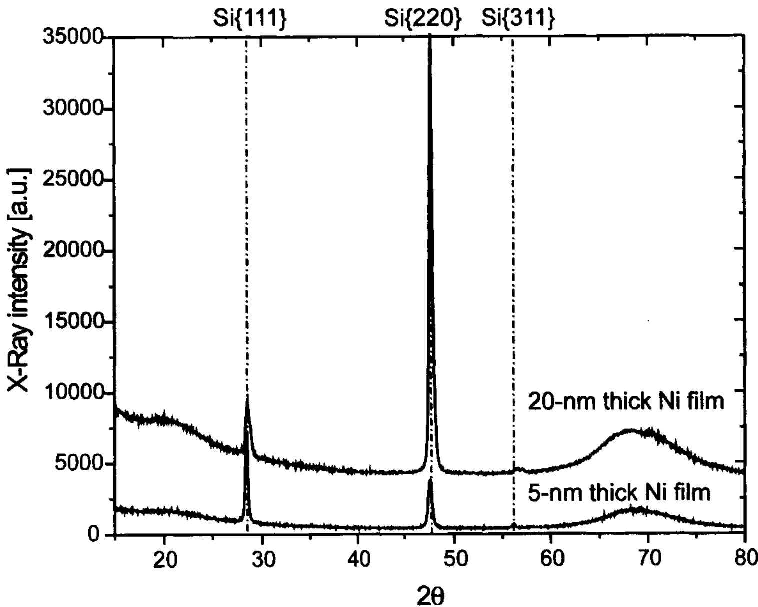


*Fig. 6.2* *XRD spectra of the NIC Si samples measured in symmetric $\theta$ -2$\theta$ geometry. The background was not subtracted from the data.*

It reveals that the NIC Si films have a polycrystalline structure corresponding to {111}, {220} and {311} planes. However, only two significant peaks are always observed, corresponding to {111} and {220} crystal orientations, while the {311} orientation is less observable. As illustrated, the (111) peak is dominant for NIC Si films coated with a 5-nm thick Ni film, while those coated with a 20-nm thick Ni film have a dominant (220) peak.

The preferred crystal orientation of NIC Si films is summarized in Table 6.2, which shows the ratios of the integrated intensity of the {220}- and {111}-Bragg reflections $I_R$ for various Ni thicknesses. $I_R$ was calculated as follows:

$$I_R = \frac{I_{\{220\}}}{I_{\{111\}}} . \tag{6.1}$$

*Table 6.2 The ratio of the integrated intensity $I_R = I\{220\}/I\{111\}$.*

| Parameter | ICDD # 27-1402 | 5-nm thick Ni | 20-nm thick Ni |
|---|---|---|---|
| $I_R$ | 0.55 | 0.75 | 12.45 |

The extra intensity for Si samples, taken from ICDD card number 27-1402, corresponds to a reference intensity value for a Si powder consisting of randomly orientated grains [6.7], i.e., with zero Ni thickness. As shown, the NIC Si sample with a 5-nm thick Ni film exhibits an un-textured structure, i.e., a random crystallographic orientation. In contrast, the NIC Si sample with a 20-nm thick Ni film always shows a {220} preferentially oriented polycrystalline structure. This means that the crystallographic orientation of the SPC NIC Si film strongly depends on the density of $NiSi_2$ precipitates, related to the Ni area density.

### 6.1.3 Effect of temperature anneal duration

In order to investigate the effect of the anneal duration on the crystallographic orientation of NIC Si films, samples were crystallized at 560 °C for times varying from 2 to 20 hours. Figure 6.3 shows the TEM images of NIC Si samples with a 20-nm thick Ni film annealed for 2 (a, b) and 8 (b, c) hours. It is worth noticing that Ni samples with and without a pre-anneal of 10 min at 250 °C (i.e., #3 and #4 from Table 6.1) do not differ significantly with respect to the film texture. The planar view in Fig. 6.3a shows the presence of facetted grains of different sizes, varying from 50 to 300 nm. The surface is relatively smooth, without twinning and visible lattice strain. The cross-sectional view in Fig. 6.3b shows the occurrence of V-shaped and flat grains throughout the Si film thickness. It is worth noticing that at maximum two grains contribute to the layer thickness (i.e., the layer consists of at maximum two grains).

As illustrated in Fig. 6.3c and 6.3d, the NIC Si sample annealed for 8 hours has a textured strained microstructure with relatively large grains (i.e., 200 - 500 nm). Also the diffraction pattern indicates the presence of micrometer-large Si grains. The grain structure is equiaxed and defective. Different types of linear and planar defects (i.e., numerous stacking faults) and twinning are present. No evidence of secondary crystallization was observed on the surface or in the bulk.

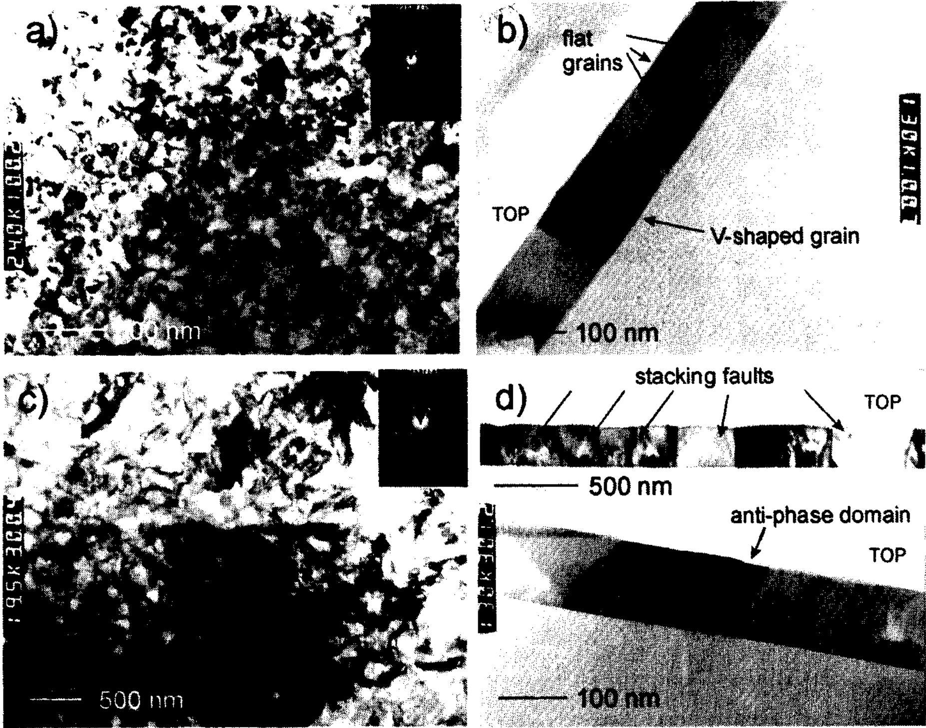


*Fig. 6.3* *a) Bright-field TEM images of NIC Si films with 20-nm thick Ni layer annealed at 560 °C for 2 (a, b) and 8 hours (c, d), respectively.*

Figure 6.4 shows the TEM images of NIC Si samples with a 20-nm thick Ni film annealed for 14 hours (a, b). NIC samples annealed for 20 hours are shown in Fig. 6.1c and 6.1d. As illustrated in Fig. 6.4a and 6.4b, the NIC Si sample annealed for 14 hours has a textured microstructure with grain size of 80 - 150 nm. Grain occlusions during coalescence lead to protrusions on the surface. Significant lattice strain (visible as thin parallel lines in Fig. 6.4a) indicates the presence of residual stress in crystallized poly-Si.

The crystallinity of the NIC Si films was checked by XRD measurements. Figure 6.5a shows the resulted XRD spectrum of the NIC Si films (background is corrected) for different anneal durations. It reveals that NIC Si films have a polycrystalline structure with {111}, {220} and {311} planes. However, a Si {111} crystal orientation is observed only for samples annealed for 20 hours. The other strong peaks correspond to {220} crystal orientations, which are almost always observable. The {311} orientation is not pronounced.

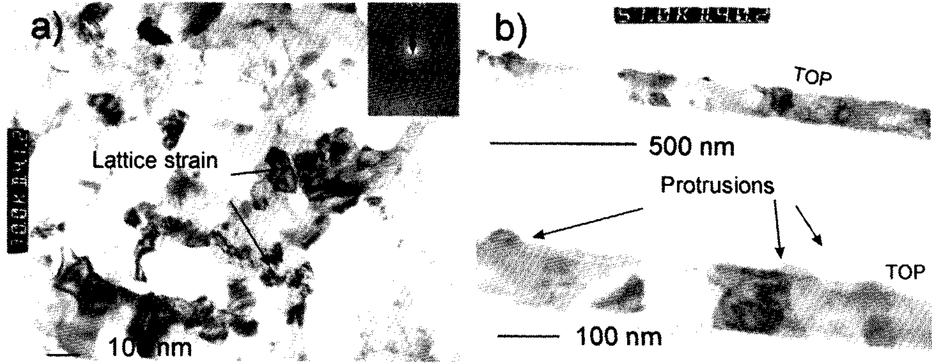


*Fig. 6.4* *a) Bright-field TEM images of NIC Si films with a 20-nm thick Ni layer annealed at 560 °C for 14 hours.*

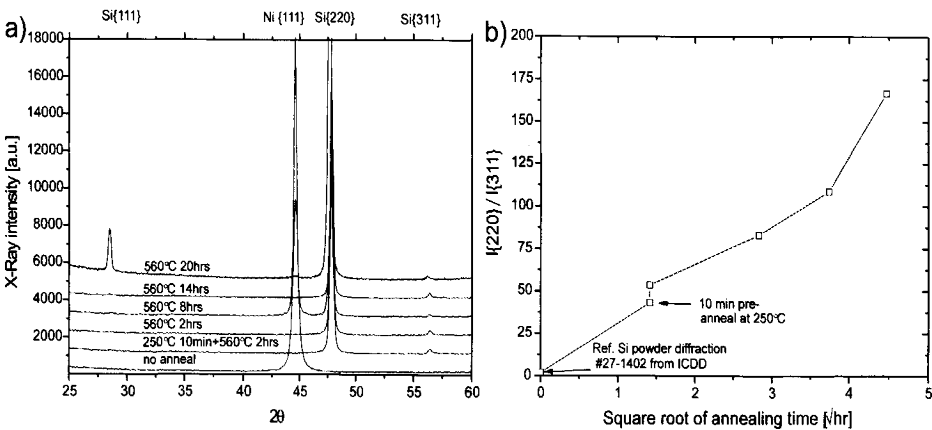


*Fig. 6.5* *a) XRD spectra of the NIC Si samples with a 20-nm thick Ni film annealed for different durations. The background was subtracted from the data. b) The ratio of the integrated intensity of the {220} and {311} Bragg reflections $I_R = I\{220\}/I\{311\}$.*

The preferred crystallographic orientation of a NIC Si sample as a function of the annealing time is illustrated in Fig. 6.5b, which shows the ratios of the integrated intensity of the {220}- and {311}-Bragg reflections $I_R$ for various time durations. $I_R$ was calculated with an equation similar to Eq. (6.1). The extra intensity for Si samples without a Ni layer (i.e., with zero Ni thickness) correspond to a reference intensity value of 0.55 for a Si powder consisting of randomly orientated grains, according to ICDD card number 27-1402 [6.7]. The heat treatment duration is quite important for the crystallographic orientation of

the NIC Si film. It is found that the intensity of {220} reflections is quite high after 2 hours of annealing, but increases dramatically with increasing time duration. The most pronounced preferred [220] orientation appears after a 20 hour anneal.

### 6.1.4 Effect of laser annealing

ELA of the NIC poly-Si film can improve the poly-Si film quality considerably. However, the combination of ELA and NIC has scarcely been reported [6.11]. The purpose of this experiment was to investigate the physical phenomena and the detailed mechanism of the ELA effect on the NIC poly-Si film. Figure 6.6 shows the TEM planar and cross-section photos of NIC Si films irradiated with a low energy density of 460 mJ/cm$^2$.

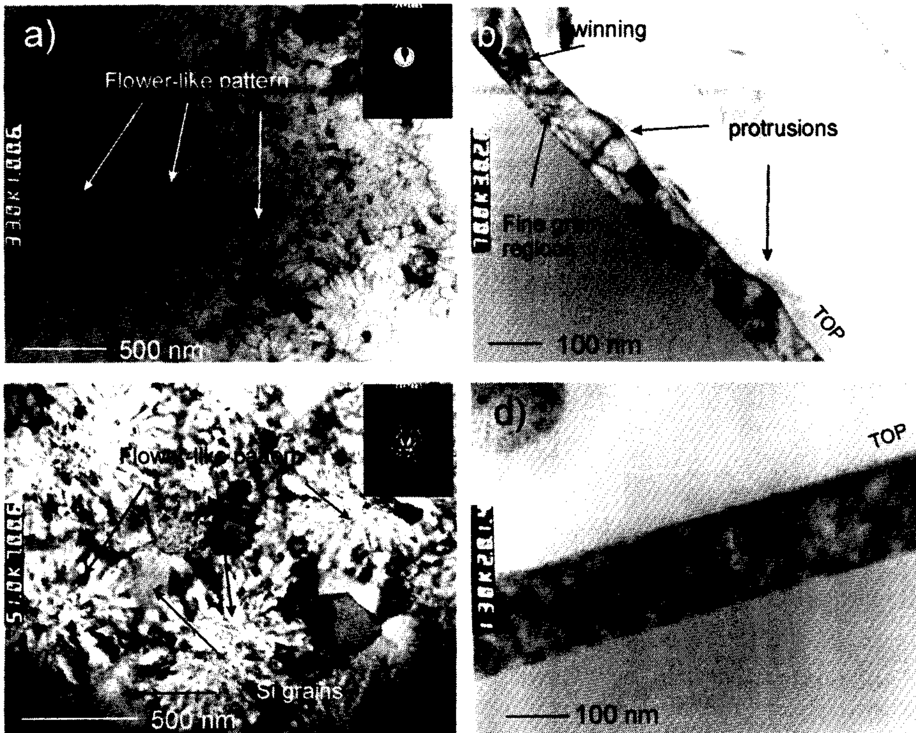


*Fig. 6.6 Bright-field TEM images of NIC Si films for 5 (a, b) and 20-nm (c, d) thick Ni layer irradiated with laser energy of 460 mJ/cm$^2$. $E_{CMsi}$ = 495 mJ/cm$^2$.*

This is only 93% of the energy density $E_{CMSi}$, required to induce complete melting of an a-Si layer without Ni film (i.e., $E_{CMSi}$=495 mJ/cm$^2$). Temperature anneal was carried out at 560 °C during 20 hours.

If the excimer laser energy density is too low to completely melt the silicon film, the grain size should remain the same after the SPC process, which was observed for the NIC Si sample with a 5-nm thick Ni film in Fig. 6.6a, b. However, the laser-annealed structure has a periodical flower-like pattern with numerous petals. As observed in Fig. 6.6a, the microstructure of a typical "flower" consists of a fine crystallite region (i.e., 30-50 nm) in the center, surrounded by small, elongated grains of 20-40 nm width, growing outwards.

When two opposite longitudinal crystalline fronts meet each other, the growth of peripheral elongated grains stops, leaving small crystals in between. The TEM cross section also indicates the presence of surface roughness, i.e., protrusions due to the collision of grain boundaries. The height of these surface protrusions can reach 30-40 nm. Surface roughness is also attributed to the significant lattice strain, visible as thin parallel lines. As illustrated in Fig. 6.6c, a NIC sample with a 20-nm thick Ni film also exhibits a periodical flower-like pattern with numerous petals. However, the microstructure of this flower is much finer than that of the NIC Si with a 5-nm thick Ni film. Additionally, large Si grains of 150-300 nm are located at the periphery of fine elongated grains. The TEM cross section in Fig. 6.6d also indicates evidence of homogeneously distributed small grains (i.e., 10-20 nm) throughout the film thickness and the absence of lattice strain. The flower-like pattern seems to consists of these small grains.

When the laser energy density is raised to 660 mJ/cm$^2$ for NIC samples with a 5 and 20-nm thick Ni layer, respectively, the grain microstructure slightly changes, as shown in Fig. 6.7. The planar view of the NIC Si sample with a 5-nm thick Ni film (Fig. 6.7a) shows a non-textured structure with a periodical flower-like pattern, which was also observed at lower energy densities. However, the peripheral elongated grains at the higher energy are slightly larger (i.e., 80-150 nm). The microstructure is equiaxed with surface roughness at locations of grain occlusions. The surface texture is determined by enlarged peripheral grains. The lattice strain is slightly reduced. As shown in Fig. 6.7c, the NIC sample with a 20-nm thick Ni film has almost the same microstructure as that at a low energy irradiation. Due to the homogeneously distributed small grains (i.e., 10-20 nm) throughout the film thickness, the lattice strain is minimal (Fig. 6.7d).

As illustrated in Fig. 6.6 and 6.7 for NIC samples with a 5-nm thick Ni film, rather than columnar grains or dendrites nucleating at the film surface (the logical place for initial silicide formation) and growing towards the substrate, the microstructure of the film was always equiaxed. The formation of an equiaxed rather than a columnar microstructure may suggest that the presence of Ni throughout the still amorphous film increased the metallic bonding nature of the a-Si. This increases Si atomic mobility via a mechanism similar to that

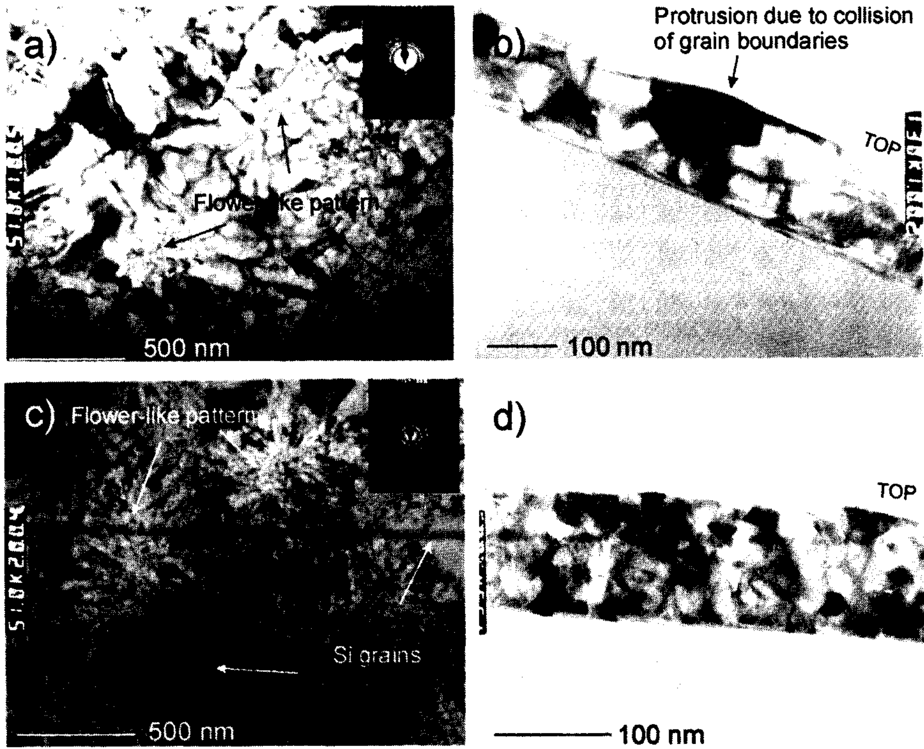


*Fig. 6.7* *Bright-field TEM images of NIC Si films with a Ni layer of 5 nm (a, b) or 20 nm (c, d) irradiated with a laser energy of 660 mJ/cm$^2$. $E_{CMSi}$ = 495 mJ/cm$^2$.*

suggested for other metals [6.4] and thereby induces crystallization homogeneously throughout the film.

However, another explanation applies to the NIC Si samples with the 20-nm thick Ni film, which were always composed of very small poly-Si grains. As follows from Fig. 6.6d and 6.7d, no grain size change was observed over the laser energy range from 460 to 660 mJ/cm$^2$. From the invariance of the poly-Si grain size for these samples it can be inferred that the fine-grain region was formed from the super-cooled molten silicon after complete melting of the NIC poly-Si in the high-energy-density regime. In case of the lowest laser energy of 460 mJ/cm$^2$ used in this experiment, the laser energy was already too much, probably inducing complete melt of Ni film, i.e., small grains homogeneously distributed through film thickness. Considering that 460 mJ/cm$^2$ is only 93% of the energy density required to completely melt the pure poly-Si film, it directly confirms that the Ni content lowers the melting temperature of the poly-Si film. Similar

results with the lower crystallization temperature of a-Si film have also been reported for Ni-incorporated solid-phase crystallization by thermal annealing as MIC or MILC [6.12, 6.13]. As a result, the crystallization temperature depends upon the metal concentration in the Si film. To decrease the crystallization temperature, the thickness of the metal should be increased.

The crystallinity of the laser-crystallized NIC samples was checked by XRD measurements, as illustrated in Fig. 6.8 (background is not corrected). This figure also shows intensities for non-laser-annealed NIC samples (taken from Fig. 6.2). It reveals that Si films have a polycrystalline structure with {111}, {220} and {311} planes. However, only two significant peaks are always observed, corresponding to {111} and {220} crystal orientations, while the {311} orientation is less observable. As can be seen, the (111) peak is dominant for Si films coated with a 5-nm thick Ni film, while those coated with a 20-nm thick Ni film have a dominant (220) peak. The intensity of the {220} peak increases significantly after laser annealing of a Si sample with a 5-nm thick Ni layer, and the {311} peak becomes barely visible. The intensity of the {220} peak slightly decreases after laser annealing of a Si sample with a 20-nm thick Ni layer. However, the {311}-oriented growth disappeared eventually after the laser treatment.

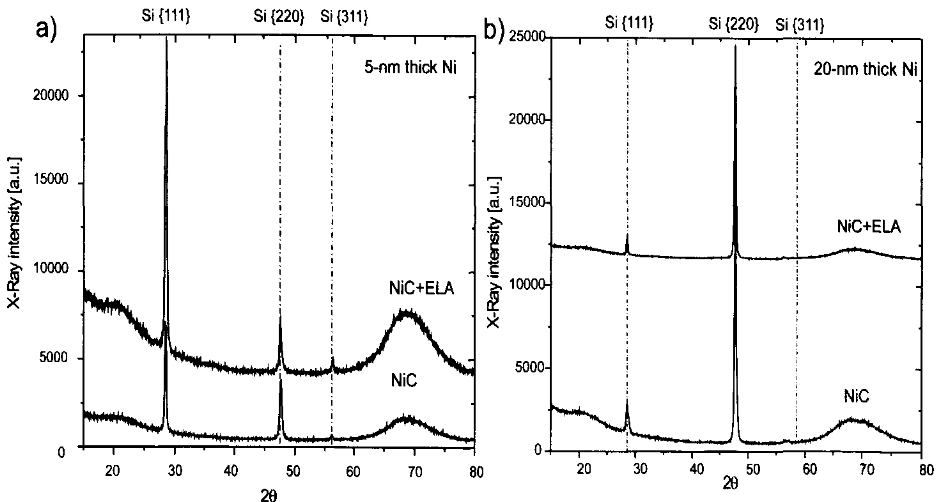


*Fig. 6.8 a) XRD spectra of the NIC Si and laser-annealed NIC Si samples (E= 460 mJ/cm$^2$) with Ni films of (a) 5 and (b) 20 nm. The background was not corrected.*

The preferred crystal orientation is summarized in Table 6.3, which shows the ratios of the integrated intensity of the {220}- and {111}-Bragg reflections $I_R$ for various Ni thicknesses, calculated according to Eq. (6.1).

*Table 6.3 The ratio of the integrated intensity $I_R = I\{220\}/I\{111\}$.*

| Parameter | SLG Si | 5-nm thick Ni | 20-nm thick Ni |
|---|---|---|---|
| $I_R$ | 0.36 | 0.2 | 6.32 |

The extra intensity for Si samples without a Ni layer (i.e., with zero Ni thickness) corresponds to the intensity value of the laser-annealed Si sample (i.e., SLG Si film as NIC+ELA sample). In the NIC Si samples with a 5-nm thick Ni film, the laser treatment seems to result in a more pronounced preferred Si [111] orientation. However, the SPC NIC Si anneal yields randomly distributed polysilicon crystallites, as was shown in Table 6.2.

## 6.2 Conclusions

Nickel-induced crystallization of a-Si with various nickel film thicknesses, annealing durations and laser energies was investigated by SEM, TEM and XRD analysis. The {220}-preferred orientation and random poly-Si crystallites were obtained after thermal annealing of a-Si samples with 20 and 5-nm thick Ni films, respectively. This confirms that the crystallographic orientation of SPC NIC Si film strongly depends on the content of $NiSi_2$ precipitates, related to the Ni concentration. Consequent laser annealing with XeCl laser resulted in {111} and {220} orientations of NIC Si films with 5 and 20-nm thick Ni layers, respectively. However, the reflection of the {220} intensity was slightly reduced compared with the only SPC NIC Si film. The melting temperature of the poly-Si film decreased as the Ni content in it increased, since the threshold energy of melting of a NIC Si sample with a 20-nm thick Ni film was decreased by at least 7% compared with that of pure Si. TEM observations confirm the presence of small grains homogeneously distributed through the Si film thickness, which might indicate complete melting of the NIC Si film with a 20-nm thick Ni layer. NIC Si films with a lower Ni content (i.e., with a 5-nm thick Ni film) had not completely melted at the same energy. However, flower-like grains were found on the surface of both samples.

The annealing time duration was found to have a quite important influence on the resulted crystallographic orientation of the Si films. Extended heat treatment of NIC Si films in the form of a longer anneal tended to produce a pronounced {220}-crystal orientation, as it increased the diffusion length of the Ni in the Si film. 20-nm thick Ni film can effectively induce crystallization of a-Si at a lower temperature. The obtained {220} preferred crystallographic orientation of Si is efficient as it reduces the mobility anisotropy and eliminates spread between electrical characteristics of TFT transistors due to the similar orientation of the channel Si region.

# Chapter 7

# Conclusions and recommendations

## 7.1 Conclusions

To realize a complete system on glass, one should use poly-Si TFTs with a field effect mobility and an off-current that approach those of bulk silicon MOS transistors. Grain boundaries generally have a high defect density (i.e., dangling bonds). Hence, a TFT with both high mobility (similar to that of bulk-Si) and a low off-current can only be obtained if these defects are completely eliminated, i.e., when the channel is formed within a single c-Si grain. This implies that for excimer-laser-recrystallized a-Si films either the grain size should be increased sufficiently and that the position of these grains (or their boundaries) should be precisely controlled. Additionally, for c-Si TFT device uniformity, the crystallographic orientation of such a c-Si island needs to be controlled. The research presented in this thesis investigates the mechanism of grain growth in excimer-laser-annealed (ELA) Si film by simulation, the fabrication process of 2-dimensionally aligned single c-Si islands, its processing window and the technique to control the film texture. Below we present the main conclusions and give recommendations for further study:

• The dual-beam with thick oxide portion (DBTOP) method is an excellent fabrication process for large c-Si islands, which allows independent spatial control of the temperature in the a-Si (i.e., concave thermal profile) and suppression of the heat flux towards the glass substrate. The former provides the location control of c-Si islands, while the latter significantly increases their size. However, the spatial variations in the laser intensity of the present typical excimer laser are a practical limitation to DBTOP application. If the beam spatial homogeneity of lasers can be improved such that their typical pulse inhomogeneity is less than ±6.8%, the process may be widely adopted for its

high-yield formation of c-Si islands on a glass substrate. An alternative approach to improving the pulse uniformity is the utilization of two lasers; then an external mirror is not required, so that additional laser beam reflection is eliminated as well as other side effects such as the shading effect and interference of the laser beam.

• The increased volume of the thick oxide portion (bump) in the intermediate insulation layer of the DBTOP method leads to an enlargement of the c-Si island up to 5.0 μm due to the reduced heat removal into the substrate. The maximum c-Si island size can be further increased up to 5.4 μm by utilizing a low-reflective material as a mirror (i.e., a Si mirror (60%) instead of an Al mirror (94%). However, it appears that stress in the underlying heat-conductive (metal) layer is an important factor limiting further enlargement of the c-Si islands.

• The processing window of the DBTOP method can be considerably improved from 1.5 to 4.7% by optimization of the geometry of the intermediate insulation layer. The bump dimensions determine the temperature gradient of the concave thermal profile in the a-Si layer, where the low-temperature area determines the size of the remnant unmolten c-Si seed. The maximum processing window can be further increased to 6.8% by utilizing a high-reflective material as a mirror, such as Al.

• The wider processing window of the DBTOP is counterbalanced by a smaller c-Si island size. However, it is preferable to use an Al mirror instead of a Si one, since the resulting c-Si size of 4.2 μm exceeds the minimum feature size of TFT anyway (i.e., > 3 μm).

• Simulation of crystal growth in pulsed excimer-laser-crystallized thin Si films by the phase-field model shows that the solid/liquid Si interface is non-planar (i.e., it has a parabolic shape) and is tilted with respect to the Si-underlayer interface. This is because the growth velocity is higher in the lateral direction than in the vertical one. The calculated maximum vertical and lateral growth velocities generally differ by a factor of nearly four.

• Enlargement of grains by reduction of the solidification velocity was successfully related to the elongation of lateral crystallization. Higher lateral growth rates led to larger Si islands. However, from a comparison between the experiments and calculations, it was found that at high solidification velocities of 19 m/s, the growth front became morphologically unstable, followed by film amorphization. Therefore, the lateral solidification velocity should be kept below this critical value at all times.

• A high Ni content (i.e., 20-nm thick film) leads to a {220}-preferred orientation of NIC Si film, while a low Ni content (i.e., 5-nm thick film) results in randomly oriented poly-Si grains. This could be related to the amount of $NiSi_2$ precipitates, migrating into a-Si and leaving {110}-oriented c-Si trails behind. Subsequent laser annealing resulted in almost solely {111} or {220} orientation of NIC Si films with 5 or 20-nm thick Ni layers, respectively.

• The melting temperature of the poly-Si film decreases as the Ni content in it increases. As a result the threshold energy for melting of a NIC Si sample with a 20-nm thick Ni film decreases by 7% at least compared to that of pure a-Si.

• The furnace anneal duration of NIC Si films is a quite important parameter determining the eventual crystallographic orientation of Si films. Extended heat treatment of NIC Si films with 20-nm thick Ni layer for 20 hours tended to result in a Si film with a crystal orientation of almost solely {220}.

## 7.2 Recommendations

• A simple thermal model applied to the nanosecond time scale of the laser pulse duration, extensively used in this research, was capable to explain in a consistent manner the solidification behaviour of Si film in the partial melting regime. However, the quantitative agreement between the thermal and 2D phase-field model can be improved by the coupling between a simple field theory of the nucleation process together with the supercooling effect and the heat flow calculations.

• It appeared that for the DBTOP method the mechanical stress in the underlying heat conductive (metal) layer is an important limiting factor for further enlargement of the c-Si islands. However, taking into account the strong dependence of built-in stress in metal on the sputtering techniques and process pressure, the deposition conditions could be optimized further.

• The ELA NIC films may be successfully implemented into the DBTOP method for the preparation of location-controlled c-Si islands with a uniform crystallographic orientation.

# Appendix

Metal deposition conditions:

*Table 7.1 Process conditions of evaporated Ti and Cr films.*

| # | *Me* | *Deposition Method* | $P_{base}$ [mbar] | $P_{evap}$ [mbar] |
|---|---|---|---|---|
| 1 | Ti | Therm. evaporation | 2.5E-7 | <1E-6 |
| 2 | Ti | E-gun evaporation | 2.0E-6 | <2E-6 |
| 3 | Cr | E-gun evaporation | 7.0E-7 | <7E-7 |
| 4 | Cr | Therm. evaporation | 3.0E-7 | <5E-7 |
| 5 | Cr | Therm. evaporation | 5.0E-7 | <6E-6 |
| 6 | Cr | Therm. evaporation | 2.5E-7 | <8E-8 |
| 7 | Ti | Therm. evaporation | 2.0E-7 | 8E-6 |
| 8 | Ti | Therm. evaporation | 3.5E-6 | <2E-7 |

*Table 7.2 Process conditions of sputtercoated W, TiN, TiW, Al and Ni films.*

| # | *Me* | *Depos. Method* | $P_{base}$ [mbar] | $P_{sput}$ [mbar] | $PWR_F$ [Watt] |
|---|---|---|---|---|---|
| 9 | W | RF | 2.0E-5 | 27E-3 | 450 |
| 10 | TiN | Magnetron | 5E-9 | 5E-3 | 12000 |
| 11 | Al | Magnetron | 5E-9 | 4.7E-3 | 15000 |
| 12 | TiW[20/80] | Magnetron | 2.6E-7 | 10.1E-3 | 470-500 |
| 13 | TiW[50/50] | Magnetron | 2.5E-7 | 10.1E-3 | 470-500 |
| 14 | TiW[20/80] | RF | 3.3E-7 | 1.3E-3 | 500 |
| 15 | Ti(20nm)+ TiW[20/80] | RF | 5.3E-7 | 1.0E-2 | 500 |
| 16 | Ni | RF | 9.3E-7 | 9E-3 | 500 |

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# Summary

Finding an industrially viable technological approach that produces low-temperature single c-Si thin films with high electronic quality and stable characteristics is a main challenge for future thin-film semiconductor electronics. During the last few years, a variety of techniques have been proposed for the preparation of structured films, including single-crystalline semiconductor films on amorphous substrates. However, all the recent approaches, based on solid phase crystallization of a-Si film and on its recrystallization by energetic beams (e.g., laser, electron, incoherent-light) have some shortcomings that limit their application.

This thesis deals with a new method to fabricate large crystalline-silicon islands on a predetermined location in a thin silicon film on a glass substrate by excimer-laser annealing. The topics that are primarily addressed in this work concern grain growth mechanisms in excimer-laser annealed (ELA) Si film, varying the spatial geometry of the sample for location control, process reproducibility in terms of the processing window, and seeding techniques to control the film texture.

Chapter 1 gives a general introduction about the development of TFT addressed liquid crystal displays, in particular about limitations of a-Si and poly-Si TFTs, caused by grain boundaries.

Chapter 2 describes transformation mechanisms in conventional excimer-laser a-Si crystallization. In particular, it summarizes the heat transport and melting phenomena during ELA of a-Si, and introduces the vertical and lateral grain growth mechanisms. It also explains the underlying principles of Si grain enlargement, location control and crystallographic orientation of grains.

Different structures and laser techniques, such as a single beam method with a multi-layer structure, a dual-beam approach with a non-uniform sample geometry (DBTOP) and metal-induced crystallization were utilized in this research. The fabrication of these structures, the analysis tools and characterization techniques are discussed in Chapter 3.

Chapter 4 presents the experimental results of grain enlargement with a single laser beam. It also introduces two different modelling tools for simulating crystal growth in pulsed excimer-laser-crystallized Si thin films: thermal and phase-field models. The thermal model describes the time- and depth-dependent temperature distribution in thin Si layers during and after laser irradiation, i.e., heating and cooling stages during the vertical growth of a c-Si island. The phase-field model describes the phase-transition kinetics and the thermal distribution of the lateral growth in the Si melt pool from the unmelted residual Si cluster after laser irradiation. Both numerical procedures are validated by comparing their predictions of the solidification behaviour with the

experimental results. It was found that the solid/liquid Si interface is non-planar and tilted with respect to the Si-underlayer interface due to its higher lateral growth velocity; it is four times higher than the vertical growth velocity. Enlargement of grains by reduction of the solidification velocity was successfully related to the elongation of lateral crystallization. However, from a comparison between the experiments and calculations, it was found that at high solidification velocities of 19 m/s, the growth front becomes morphologically unstable, followed by film amorphization.

Chapter 5 shows the experimental results obtained by dual-beam irradiation. In particular, it analyses the effects of grain enlargement and the processing energy density window of obtained location-controlled grains. Control of the position of the Si island is realized by spatial geometry variation of the sample in order to produce an intentional temperature non-uniformity along the Si/insulator interface and to induce a complete/incomplete melting regime. The size of the c-Si island and its processing window were influenced by the thickness of an intermediate oxide layer, by its geometry and by the laser energy density. It was found that the increased volume of the thick oxide portion (bump) in the intermediate insulation layer of the DBTOP method led to an enlargement of the c-Si island up to 5.0 μm due to the reduced heat removal into the substrate. The maximum c-Si island size could be further increased up to 5.4 μm by utilizing a low-reflective material as a mirror (i.e., a Si mirror (60%) instead of an Al mirror (94%). However, it appears that stress in the underlying heat-conductive (metal) layer is an important factor limiting further enlargement of the c-Si islands.

The influence of the underlying oxide bump dimensions as well as the effect of the energy ratio of the laser beams on the processing window are also investigated in Chapter 5. It was concluded that the processing window of the DBTOP method could be considerably improved from 1.5 to 4.7% by optimization of the geometry of the intermediate insulation layer. The experimental results were also found to be in very good agreement with those of the 2D thermal simulation. The bump dimensions determine the temperature gradient of the concave thermal profile in the a-Si layer, where the low-temperature area determines the size of the remnant unmolten c-Si seed. The maximum processing window can be further increased to 6.8% by utilizing a high-reflective material as a mirror, such as Al. The wider processing window of the DBTOP is counterbalanced by a smaller c-Si island size of 4.2 μm, which still exceeds the minimum feature size of a TFT of 3 μm.

Chapter 6 presents nickel-induced crystallization (NIC) of amorphous silicon. The crystallization was performed by solid-phase crystallization, which was consequently combined with excimer-laser anneal of Si films in order to reduce the crystalline defect density. The effects of a different Ni film thickness, annealing temperature and duration, and the effect of laser irradiation on the crystallographic orientation of Si film were investigated. It was found that the Ni

content and the isothermal anneal duration of NIC Si films is a quite important parameter determining the eventual crystallographic orientation of Si films. A high Ni content (i.e., 20-nm thick Ni film) leads to a {220}-preferred orientation of NIC Si film, while a low Ni content (i.e., 5-nm thick Ni film) results in randomly oriented poly-Si grains. Subsequent laser annealing resulted in an almost solely {111} or {220} orientation of NIC Si films with 5 or 20-nm thick Ni layers, respectively. Extended heat treatment of NIC Si films with 20-nm thick Ni layer tended to result in an almost solely {220}-crystal orientation of the Si film. The obtained NIC Si films may be successfully implemented into the DBTOP method for the preparation of location-controlled c-Si islands with a uniform crystallographic orientation.

Finally, Chapter 7 gives conclusions and recommendations for further research.

# *Samenvatting*

De voornaamste uitdaging voor toekomstige elektronica gebaseerd op dunne lagen van halfgeleiders is een technologische methode te vinden waarmee bij lage temperaturen dunne lagen van silicium eenkristallen gemaakt kunnen worden en die uit industrieel oogpunt levensvatbaar is. Gedurende de laatste jaren zijn verschillende technieken voorgesteld, waarmee gestructureerde lagen gemaakt kunnen worden, waaronder lagen van halfgeleidende eenkristallen op amorfe substraten. Echter, al deze recentelijk voorgestelde methoden, gebaseerd op kristallisatie in de vaste fase (*solid phase crystallization*) van een laag van amorf silicium (a-Si) en de rekristallisatie daarvan met energetische bundels (zoals een laserbundel, elektronenbundel of een bundel van incoherent licht), hebben enkele tekortkomingen die de toepasbaarheid daarvan limiteren.

In dit proefschrift wordt een nieuwe methode besproken waarmee met behulp van een warmtebehandeling met een excimer-laser (*excimer-laser annealing*, ELA) eilandjes van kristallijn silicium (c-Si) gemaakt kunnen worden op een van te voren bepaalde positie in een dunne film van Si op een glazen substraat. De onderwerpen die voornamelijk in dit werk aan bod komen behelsen de groeimechanismen van korrels in een film van Si na ELA, waarbij de ruimtelijke geometrie van het monster om controle van de positie te verkrijgen, de reproduceerbaarheid van het proces in termen van een procesbereik en de kiemtechnieken, waarmee de filmstructuur gecontroleerd kan worden, gevarieerd worden.

In hoofdstuk 1 wordt een algemene inleiding gegeven over de ontwikkeling van schermen gebaseerd op vloeibare kristallen, die geaddresseerd worden door dunne-film transistoren (*thin-film transistors*, TFTs). In het bijzonder worden de beperkingen belicht van TFTs van a-Si en polykristallijn Si, die worden veroorzaakt door korrelgrenzen, de zogenaamde *grain boundaries*.

In hoofdstuk 2 worden de overgangsmechanismen beschreven in de conventionele kristallisatie van a-Si met behulp van een excimer-laser. Meer in het bijzonder worden het warmtetransport en de smeltfenomenen gedurende de ELA van a-Si summier besproken en worden de verticale en horizontale groeimechanismen van korrels geintroduceerd. Verder worden de principes uitgelegd die ten grondslag liggen aan de vergroting van de Si korrels, de controle over de positie en de kristalorientatie van de korrels.

Verschillende structuren en lasertechnieken werden gebruikt in dit onderzoek, zoals een methode met een enkele bundel met een multilaags structuur, een methode met een dubbele bundel met een niet-uniforme geometrie (DBTOP) en metaal geinduceerde kristallisatie. De fabricage van deze structuren, de analysemethoden en de karakteriseringstechnieken worden uitgelegd in hoofdstuk 3.

Experimentele resultaten van korrelvergroting met behulp van een enkele laserbundel worden gepresenteerd in hoofdstuk 4. In dit hoofstuk worden ook twee verschillende modelleringsmethoden geintroduceerd waarmee de groei kan worden gesimuleerd van kristallen in dunne films van Si die met behulp van een gepulste excimer-laser gekristalliseerd zijn, te weten thermische en faseveld modellen. Het thermische model beschrijft de tijds- en diepteafhankelijke temperatuursverdeling in dunne lagen van Si voor en na laserbestraling, met andere woorden de opwarm- en afkoelstadia gedurende de verticale groei van een eilandje van c-Si. Het faseveld model beschrijft de kinetiek van de faseovergangen en de thermische verdeling van de laterale groei in het gesmolten gedeelte van het ongesmolten Si residu cluster na laserbestraling. Beide numerieke procedures worden gevalideerd door de voorspellingen van het stollingsgedrag te vergelijken met experimentele resultaten. Er werd gevonden dat de overgang tussen de vaste stof en vloeistof niet planair is en schuin staat ten opzichte van de onderliggende Si overgang als gevolg van de grotere laterale groeisnelheid; deze is een factor vier groter dan de verticale groeisnelheid. Vergroting van de korrels door reductie van de stollingssnelheid werd succesvol gerelateerd aan de verlenging van de laterale kristallisatie. Echter, uit een vergelijking tussen experimentele resultaten en berekeningen werd gevonden dat bij een hoge stollingssnelheid van 19 m/s het groeifront morfologisch instabiel is, waarna de film amorf wordt.

In hoofdstuk 5 worden experimentele resultaten getoond die verkregen zijn door bestraling met een dubbele bundel. In het bijzonder worden de effecten geanalyseerd van korrelvergroting en het energiedichtheidbereik van verkregen korrels waarvan de positie vooraf bepaald is. Controle van de positie van een eiland van Si wordt gerealiseerd door ruimtelijke geometrievariatie van het monster om zodoende met opzet een temperatuurverdeling te verkrijgen die niet uniform langs de overgang tussen het silicium en de isolator is. Ook wordt op deze manier een compleet/incompleet smeltregime verkregen. De grootte van het eilandje van c-Si en het bijbehorende procesbereik worden beinvloed door de dikte van een tussenliggende oxidelaag, de geometrie van het eilandje en de energiedichtheid van de laser. Er werd gevonden dat met de DBTOP methode het grotere volume van het dikke oxidegedeelte (hobbel) in de tussenliggende isolerende laag leidde tot een vergroting van het eilandje van c-Si tot een grootte van 5.0 µm als gevolg van een gereduceerd warmtelek in het substraat. De maximale grootte van het eilandje van c-Si kon verder worden vergroot tot 5.4 µm door een 'spiegel' te gebruiken van materiaal met een lage reflectiviteit (m.a.w. een Si spiegel (60%) in plaats van een Al spiegel (94%)). Echter, het bleek dat de spanning in de onderliggende warmtegeleidende (metaal) laag een belangrijke beperkende factor is voor verdere vergroting van de eilandjes van c-Si.

De invloed van de dimensies van de onderliggende oxidehobbel alsmede het effect van de energieverhouding van de laserbundels op het procesbereik zijn

ook onderzocht in hoofdstuk 5. Er werd geconcludeerd dat het procesbereik van de DBTOP methode aanmerkelijk verbeterd zou kunnen worden van 1.5 tot 4.7% door optimalisatie van de geometrie van de tussenliggende isolerende laag. Er werd eveneens gevonden dat de experimentele resultaten zeer goed overeenstemmen met de resultaten van 2D thermische simulaties. De afmetingen van de hobbel bepalen de temperatuurgradient van het concaaf thermisch profiel in de a-Si laag, waar het deel met lage temperatuur de grootte bepaalt van de overgebleven, niet gesmolten kiem van c-Si. Het maximale procesbereik kan verder vergroot worden tot 6.8% door gebruik te maken van materiaal met een hoge reflectiviteit als spiegel, zoals Al. Het bredere procesbereik van DBTOP gaat ten koste van de grootte van het eilandje van c-Si dat nu 4.2 μm is. Dit is nog steeds groter dan de minimale grootte van de patronen in een TFT van 3 μm.

In hoofdstuk 6 wordt kristallisatie van a-Si geinduceerd door nikkel (*nickel-induced crystallization*, NIC) behandeld. De kristallisatie werd uitgevoerd door middel van vaste-fase kristallisatie, dat consequent werd gecombineerd met ELA van Si films om hiermee de dichtheid van kristallijne defecten de verkleinen. Het effect van een andere dikte van de Ni laag, de temperatuur en duur van de warmtebehandeling en van de laserbestraling op de kristallografische orientatie van de Si film werd onderzocht. Er werd gevonden dat de Ni inhoud en de duur van de isothermische warmtebehandeling van NIC Si films redelijk belangrijke parameters zijn in de bepaling van een eventuele kristallografische orientatie van de Si films. Een grote Ni inhoud (m.a.w. een Ni film met een dikte van 20 nm) leidt tot een NIC Si film met een voorkeursorientatie {220}, terwijl een lage Ni inhoud (m.a.w. een Ni film met een dikte van 5 nm) resulteert in willekeurig georienteerde poly-Si korrels. Daaropvolgende ELA leidde vrijwel alleen tot {111} of {220} orientatie in de NIC Si films met Ni lagen van respektievelijk 5 of 20 nm. Verdere warmtebehandeling van de NIC Si films met een Ni laag van 20 nm leek vrijwel uitsluitend te resulteren in {220} kristalorientatie van de Si film. De verkregen NIC Si films kunnen mogelijk geimplementeerd worden in de DBTOP methode voor de vervaardiging van eilandjes van c-Si met een uniforme kristalorientatie en waarvan de positie gecontroleerd kan worden.

In hoofdstuk 7 tenslotte, worden conclusies en aanbevelingen gegeven voor verder onderzoek.

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Профессор кислых щей, ваш Артемушка.

# *List of publications*

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# *About the Author*

Artyom Burtsev was born on 28 November 1973 in Minsk, Belarus. He received the M.Sc. degree in Electrical Engineering (speciality: Microelectronics and Semiconductor Components) from the Belarussian State University of Informatics and Radioelectronics in 1996. The topic of his graduation work was anisotropic U-shaped $SF_6$-based plasma silicon trench etching. This project was partially performed at the Delft Institute of Microelectronics and Submicron Technology (DIMES) of Delft University of Technology during his eight-month practical training in 1994 - 1995. During his stay at DIMES he was responsible for the development of trench isolation processes for high-density integrated circuit applications.

In 1997 he continued his research in DIMES, where he worked towards his Ph.D. degree in the field of excimer-laser crystallization of thin a-Si films. The author is currently working at the same laboratory on shallow junction formation by laser annealing as a postdoc.

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