A 28W -108.9dB/-102.2dB THD/THD+N Hybrid ΔΣ-PWM Class-D Audio Amplifier with 91% Peak Efficiency and Reduced EMI Emission

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23.4 A 28W -108.9dB/-102.2dB THD/THD+N Hybrid ΔΣ-PWM Class-D Audio Amplifier with 91% Peak Efficiency and Reduced EMI Emission

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Class-D amplifiers are often used in high-power audio applications due to their high power efficiency. They typically employ pulse-width modulation (PWM) at a fixed carrier frequency, which may cause electromagnetic interference (EMI). Setting this frequency (f_{PWM}) below the AM band (535 to 1605kHz) helps mitigate this, but its harmonics still contain substantial energy and must be filtered out by bulky LC filters with low cut-off frequencies (f_C = 20 to 40kHz), significantly increasing system cost and size. Stability considerations also constrain the amplifier's unity-gain frequency to be < f_{PWM}/π [1], compromising the audio-band loop gain required to suppress output-stage nonlinearity. Setting f_{PWM} above the AM band helps increase f_C and allows a higher loop gain [2]. However, this results in narrower pulses at higher power levels (higher modulation index), which cannot be faithfully produced by the output stage, thus exacerbating its non-linearity. Delta-sigma modulation (ΔΣM) has fixed pulse widths and does not suffer from these narrow-pulse artefacts. However, the out-of-band noise of 1bit modulators then requires larger LC filters. Moreover, high-order loop filters must be used to achieve sufficient SQNR, which then require additional techniques to maintain stability as the modulation range approaches 100% [3].

In this work, a 3rd-order 17-level hybrid ΔΣ-PWM Class-D amplifier is proposed. Its hybrid modulation scheme allows a high f_{PWM} to be combined with fixed pulse widths, while the use of multilevel quantization significantly reduces its out-of-band noise and increases its stable modulation range. As a result, the proposed Class-D amplifier meets the CISPR-25 average EMI mask (150kHz to 30MHz) for automotive applications with 12dB margin, while using a relaxed LC filter (f_C = 100kHz). Overall, it achieves state-of-the-art performance compared to prior art shown in the Figure 23.4.6, with -102.2dB peak THD+N, -108.9dB peak THD and 109dB dynamic range (A-weighted), while obtaining a peak efficiency of 91% at its maximum output power of 28W (@10% THD).

Figure 23.4.1 shows the system diagram of the proposed fully differential Class-D amplifier. It consists of a 3rd-order loop filter, a 17-level flash quantizer, a PWM generator, a high-voltage (HV) power stage and a resistive feedback network that defines a closed-loop gain of 8. The key block of the system is the PWM generator, which converts the output of the multi-level quantizer into the two-level signals needed to drive the output stage. As shown in Fig. 23.4.2, the various voltage levels output by the quantizer are mapped to a set of time-quantized PWM waveforms with the same average value [5].

While this mapping results in less quantization noise than a 1bit modulator, it also results in a strong tone at the sampling frequency f_S. Alternate PWM pulses are flipped in the time domain (from the end to the beginning of the period) to avoid a transition and smoothly follow on from the preceding pulse shape, beneficially reducing switching losses by half and doubling the minimum pulse width applied to the output stage. As pulse-flipping also shifts the main tone from f_S to $f_S/2$, setting f_S = 4MHz positions the main tone at 2MHz, avoiding the AM band with sufficient margin. In this work, a normalized time-quantization step of 0.1FS is used, resulting in 21 bipolar voltage and time steps distributed between (and including) ±1FS. Since narrow pulses will degrade linearity, the levels corresponding to ±{0.8, 0.9} FS are not used, reducing the number of discrete steps to 17. This results in a minimum pulse width of 75ns, comfortably wider than the minimum pulse width (~16ns) that the output stage can actually produce. The PWM generator is realized by on-chip digital logic. It uses an 80MHz ($20\times f_S$) master clock to serialize the 16bit thermometer code of the flash quantizer (or its flipped version), after appropriately adding 0/1 padding bits corresponding to the unused levels.

As shown in Fig. 23.4.3, high loop gain is achieved by using a 3rd-order loop filter with optimized NTF zeros. Input feedforward paths eliminate the signal content in the outputs of the first two integrators, relaxing the linearity requirements on the associated OTAs. The coefficients were optimized to achieve an SQNR of 123dB and avoid excessive noise in the AM band. To ensure robustness against process variation, which may introduce some 30% spread in its coefficients, the loop-filter capacitors are 2bit trimmable. For high GBW, the integrators are built around two-stage feedforward OTAs which together draw 1.8mA from a 1.8V supply. This combination of multilevel quantization together with a high f_S results in a loop gain of >76dB (26dB higher than [6]) in the audio band irrespective of process spread, thus ensuring high linearity.

The fully differential H-bridge output stage is shown in Fig. 23.4.1. It consists of four identical N-LDMOS devices (M_H and M_L) with an R_{ON} of ~100mΩ, which results in >90% peak power efficiency. Schottky diodes (D_S) and off-chip bootstrap capacitors (C_{BS}) are used to derive the boosted supply voltages (~14V with respect to V_{SW}) of the M_H gate drivers. As the maximum V_{GS} of M_H and M_L is 5V, on-chip voltage regulators are used to create local 5V supplies relative to the sources of M_H and M_L, and power the respective gate drivers [7]. Level shifters transmit the control signals from the low-voltage digital domain (D_{VDD} = 1.8V) to the HV domains. AD modulation is used to drive the two halves of the H-bridge, as the resulting outputs are then 180 degrees phase apart, producing significantly lower common-mode (CM) EMI than BD modulation [6]. In general, CM EMI is more problematic as it cannot be suppressed by using differential cabling.

The prototype IC, shown in Fig. 23.4.7, was fabricated in a 0.18μm BCD process and occupies an active area of 4.8mm². An external LC filter (L=2.2μH, C=1.15μF) is used to suppress out-of-band noise.

Figure 23.4.4 shows the in-band audio performance of the proposed Class-D amplifier with a 14.4V supply (P_{VDD}) and a 4Ω load. When idling, it draws 17mA from P_{VDD}, which is dominated by the switching loss of the HV output stage. At 1W output power, a THD+N of -94.0dB and -94.2dB is achieved, at input frequencies of 1kHz and 6kHz, respectively. With respect to the state-of-the-art [4], this is an improvement of 6.1dB for a 4Ω load. For the same output power and input frequencies, the CDA achieves a THD of -103.6dB and -109.1dB, respectively. The proposed Class-D amplifier can deliver 28W peak power at 10% THD and has an efficiency of 91%. Over its full power range, it achieves a peak THD+N of -102.2dB and -100.5dB, for input frequencies of 1kHz and 6kHz, respectively. Similarly, it achieves a peak THD of -108.9dB and -110.1dB, for input frequencies of 1kHz and 6kHz, respectively. For comparison, a 1bit quantizer was also implemented (Fig. 23.4.1). In this case, the THD+N performance starts to deteriorate at significantly lower power levels (~8W), indicating the onset of modulator overload; while the 17-level Class-D amplifier maintains <-80dB THD+N up to ~20W. This is comparable with [4], but is achieved with significantly lower supply voltage.

Figure 23.4.5 shows the measured CISPR-25 average radiated emission in the frequency range of 150kHz to 30MHz. Compared to the use of a 1bit quantizer, the 17-level technique results in an extra ~10 dB margin in the AM band. The reduced out-of-band energy is converted into tones above the AM band.

Figure 23.4.6 summarizes the performance of the Class-D amplifier and compares it with other state-of-the-art designs with similar supplies (12V to 25V) and loads (4Ω to 8Ω). It achieves the highest THD (1W O/P power) and peak THD+N, as well as the highest power efficiency. Thanks to the ΔΣM-PWM modulation technique, the Class-D amplifier is able to achieve high THD(+N) levels even at high output power levels, while satisfying the CISPR-25 average EMI mask using a relaxed LC filter with a 100kHz cut-off frequency.

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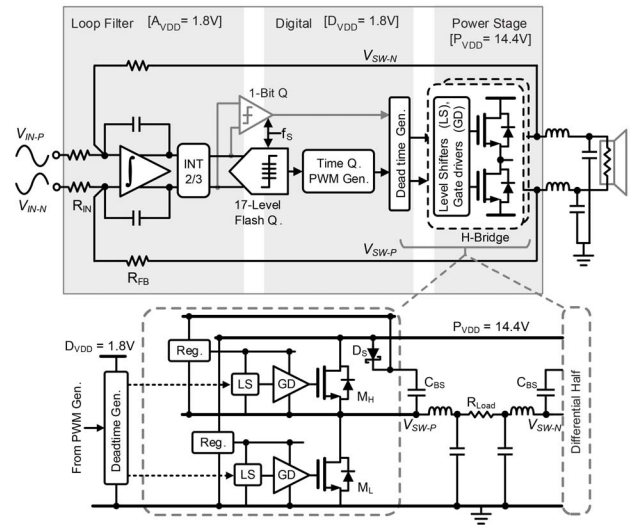

Figure 23.4.1: Simplified block diagram of the fully differential CDA (Top) and simplified half-circuit schematic of the output power stage (Bottom).

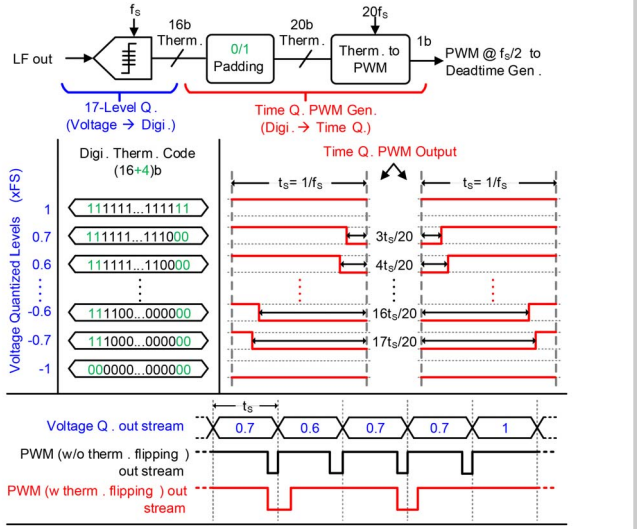

Figure 23.4.2: The 17-level voltage-to-time-domain quantizer PWM conversion (Top) and typical time-domain output streams (Bottom).

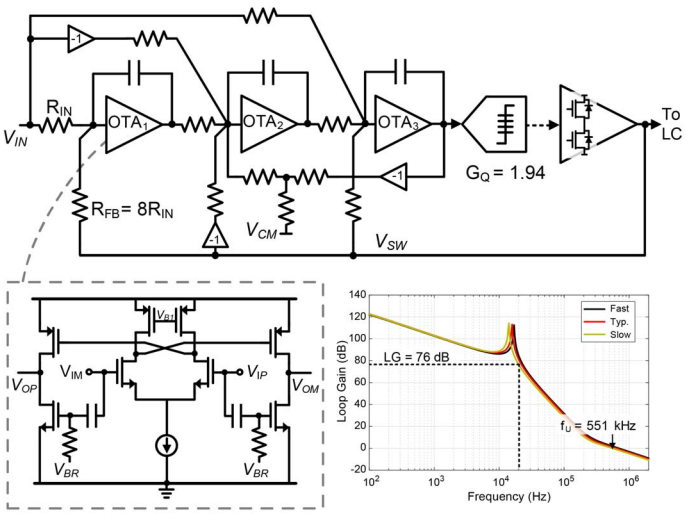

Figure 23.4.3: Simplified single-ended schematic of the loop filter (Top) and loop-gain plot after trimming (Bottom).

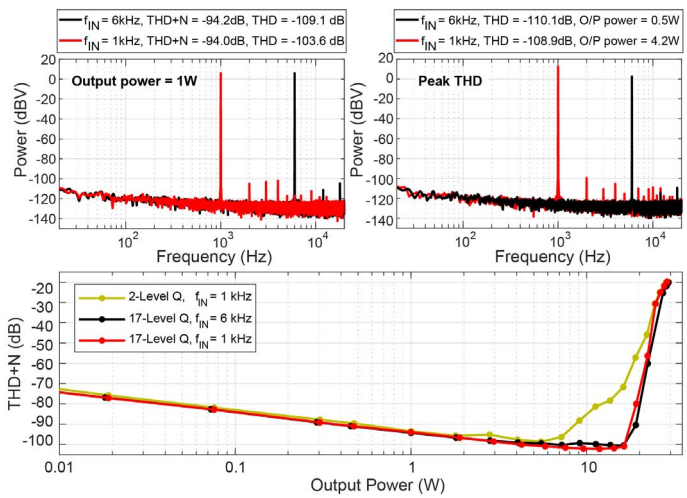

Figure 23.4.4: Measured performance of the CDA for P_{VDD} = 14.4V and a 4Ω load: FFTs at 1W output power (Top- Left); FFTs at peak THD performance (Top-Right); THD+N across output power (Bottom).

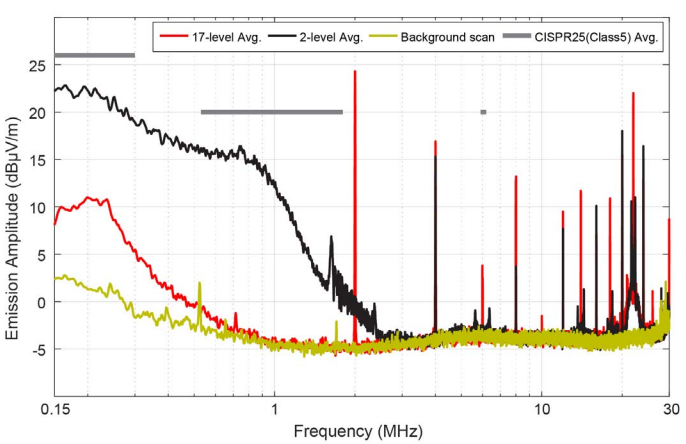

Figure 23.4.5: Radiated emission of the fully functioning CDA across frequency.

Parameter	[2]	[3]		[4]		[6]	This work
Modulation Scheme	PWM (Digital In.)	ΔΣ (Analog In.)		PWM (Digital In.)		PWM (Digital In.)	**ΔΣ-PWM (Analog In.)**
Supply	14.4V	12V	20V		20V	25V	**14.4V**
Load	4Ω	6Ω	4Ω	8Ω	4Ω	4Ω	**4Ω**
THD+N (f_{IN}=1kHz, P_O=1W)	0.02% -74.0dB	0.0032%* -90dB	0.0065%* -83.7dB	0.0029% -90.7dB	0.004%* -87.9dB	0.004% -87.9dB	**0.002% -94.0dB**
THD (f_{IN}=1kHz, P_O=1W)	-	0.0012% -98.4dB	-	-	-	-	**0.00066% -103.6dB**
Peak THD+N (f_{IN}= 1kHz)	0.015%* -76.5dB	0.0032%* -90.0dB	0.0065%* -83.7dB	0.0013% -97.7dB	0.0021%* -93.6dB	0.0037%* -88.6dB	**0.00078% -102.2dB**
$P_{O\text{-}MAX}$ (10% THD)	27W	10W	40W	20W	20W	80W	**28W**
DR (A wt.)	-	106dB	-	115.5dB	-	115dB	**109dB**
O/P Noise (A wt.)	42uVrms	50uVrms	-		20uVrms	34uVrms	**31uVrms**
Efficiency	86%		88%		90%	>90%	**91%**
SW Freq	2.1MHz		< 0.7MHz		0.4MHz	0.5MHz	**2.0MHz**
Comp. Count [L, C] / Values	2L, 2C 3.3μH, 1uF		2L, 2C 15μH, 1uF		2L, 2C -	4L, 2C -	**2L, 2C 2.2μH, 1.1uF**
LC filter cutoff	88kHz		41kHz		-	40kHz*	**100kHz**
Process	-		600n BCD		180n BCD	140n BCD	**180n BCD**

* Values taken from plots

Figure 23.4.6: Performance summary and comparison with state-of-the-art CDAs.

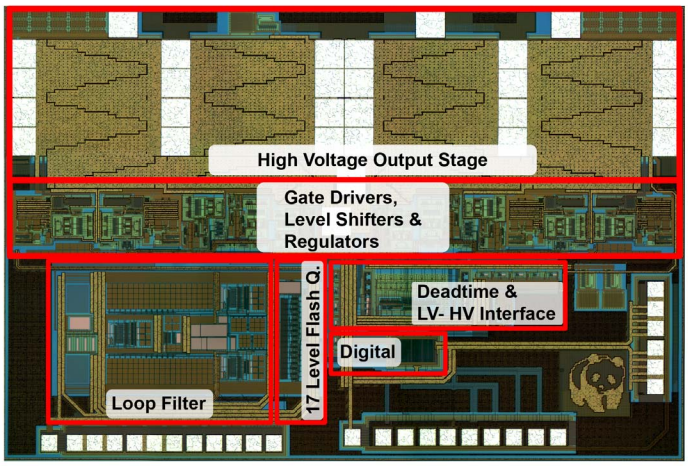

Figure 23.4.7: Die micrograph of the Hybrid ΔΣ -PWM Class-D Audio Amplifier.

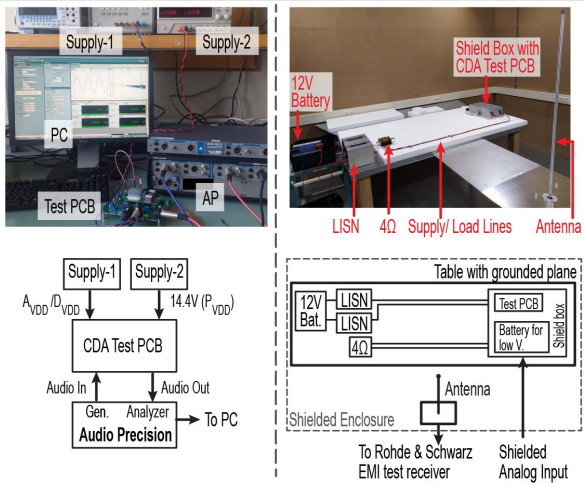

Figure 23.4.S1: Measurement setups: Left- Setup to characterize the audio performance using an Audio Precision (with AES17 filter enabled) test equipment; Right- Setup to measure radiated EMI (150kHz to 30MHz) using the guidelines and dimensions set by the CISPR25- Class5 standard.

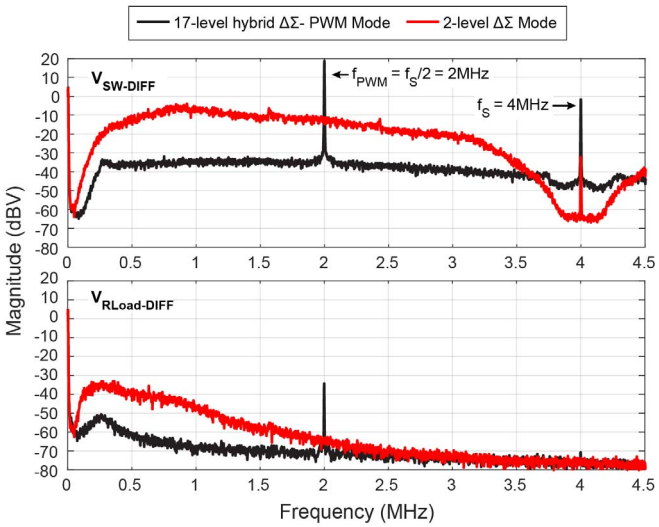

Figure 23.4.S2: Measured out-of-band voltage spectrum of the Class-D Audio Amplifier: before LC filter (Top: $V_{SW-DIFF}$) and after LC filter (Bottom: $V_{RLoad-DIFF}$).

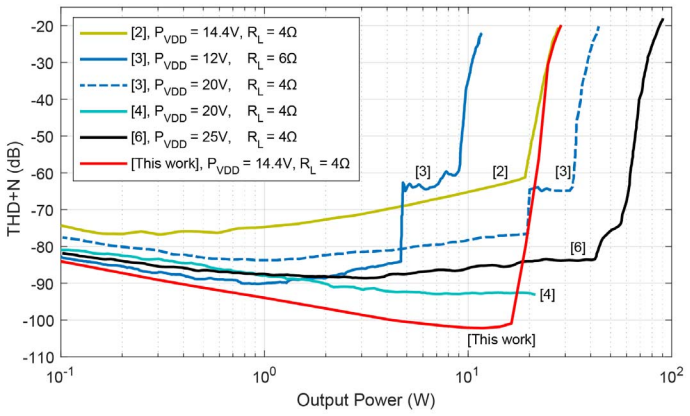

Figure 23.4.S3: Comparison of THD+N across output power (f_{IN} = 1kHz) with state-of-the-art CDAs.

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