

MSc thesis in Electrical Engineering

An Ultrasound Receiver ASIC with Slow-time Feedback for Transcranial Doppler Imaging

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Abstract

Transcranial Doppler ultrasound imaging is a crucial tool for both clinical and research applications. Despite its significance, its utility is constrained by the dynamic range limitations of the receiver system. Traditional methods, relying on high-dynamic-range front-end amplifiers and high-resolution ADCs, are often inefficient. These methods expend unnecessary effort on the clutter component of the input signal, which, although non-targeted, dominates the signal swing.

This research addresses this challenge by introducing a feedback path near the transducer end. This integration effectively mitigates the clutter component, thus relaxing the dynamic range requirements of the receiver chain. To ensure stability and precision, the system uses a closed-loop configuration with a slow-time integrator, ensuring consistent tracking of the feedback path.

The thesis provides an in-depth architectural exploration. A Matlab model is developed to assess the impact of circuit non-linearities. An analytical model is also introduced to understand the stability of the slow-time feedback system. Validated through simulations, this model serves as a robust framework for system bandwidth design.

Using the TSMC 180nm technology, a prototype system is implemented. Specifically, the LNA adopts a capacitively-coupled current amplifier design, enhanced with resistive broadbanding for the OTA cell. This design ensures efficient loop gain control. The feedback path incorporates a 10-bit resistive DAC, followed by a capacitively-coupled current amplifier acting as a buffer. A boxcar integrator is also integrated, converting the current into a sampled voltage. Simulation results underscore the system's efficiency, with a power consumption of 20.72mW and a dynamic range of 89.57dB.

Keywords: Transcranial Doppler Ultrasound; Clutter Filtering; Dynamic Range Relaxation; Delta Modulator

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Tianyi Liu
The Hague

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1. Introduction

1.1. Application - Transcranial Doppler Ultrasound

Increasing impact of neurological disorders on health and life expectancy is gaining global recognition as a critical public health concern. This issue is expected to worsen in the coming decades. In 2016, neurological disorders became the leading cause of years lost due to poor health and the second leading cause of global mortality [1]. This severity is particularly evident in the Netherlands, as depicted in Figure 1.1, where conditions like Alzheimer's disease and strokes have become the primary causes of death [2]. Additionally, more than a quarter of healthcare spending in the Netherlands is dedicated to addressing brain disorders [3]. This underscores the urgent need to closely monitor, diagnose, and understand these brain-related afflictions.

Among the array of current diagnostic tools for brain disorders, transcranial Doppler ultrasound (TCD) stands out as a promising option. TCD is a noninvasive ultrasonic technique that measures blood flow velocity and direction in the major intracranial arteries. Compared to other noninvasive diagnostics techniques, e.g magnetic resonance imaging (MRI) or computerized tomography (CT), it offers the advantages of 1) lower cost 2) ability to be performed in neurosurgery 3) higher temporal resolution [4]. Since the last century, TCD has found widespread clinical use for localized flow measurement in major cerebral arteries, proving crucial for early stroke diagnosis and microemboli detection [5][6]. Moreover, it has great research potential. Recent advancements in ultrasound-based imaging techniques have enabled visualization of microvascular cerebral blood volume, allowing direct observation of the link between neuronal activity and behavior, significantly advancing brain function understanding [7][8][9].

An example of transcranial doppler ultrasound is illustrated in Figure 1.2. The transducer receives an electrical stimulus and responds by generating an acoustic wave. This wave passes through the acoustic window, reflects off blood cells, and is captured as reflected acoustic signals. Through processing in the electrical domain, blood flow velocity and direction can be determined.

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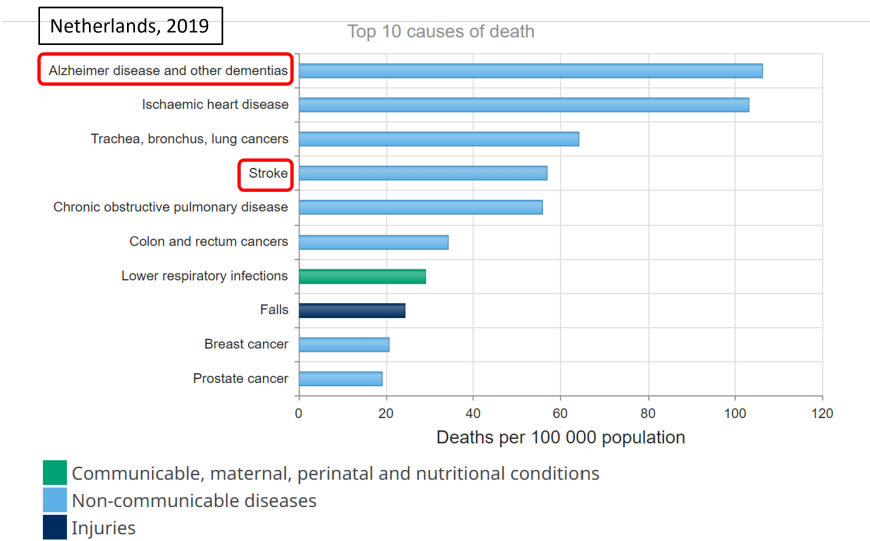


Figure 1.1.: Percentage of total depth variation against year for top 10 causes of deaths: Netherlands, year 2019. [2]

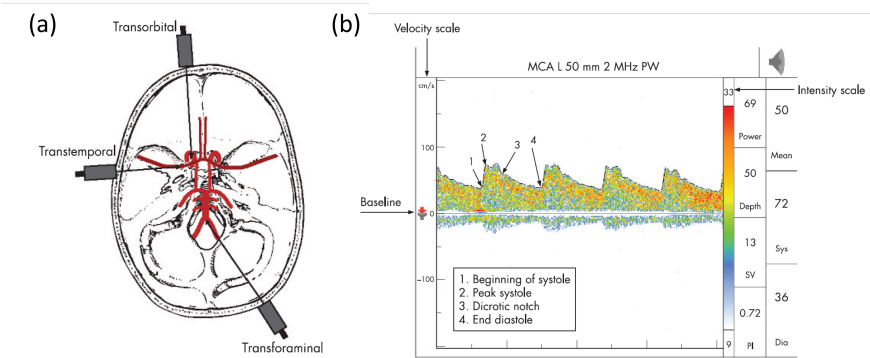


Figure 1.2.: An example of TCD: main brain artery blood flow imaging. (a) The acoustic window used in transcranial Doppler examination. (b) A typical transcranial Doppler spectra with velocity and intensity scale on the left and right axis, respectively. [5]

1.1.1. Challenges - Sensitivity Problem

One of the primary challenges in TCD is sensitivity. Sensitivity is defined as the ability to visualize faintly echogenic objects and is indicative of the minimum detectable echogenicity [10].

In the context of TCD, the signal comprises two main components. The first component is the reflection signal from blood cells, which is valuable yet weak. The second component originates from the skull and static tissues, including blood vessel walls. Often referred to as 'clutter', this component doesn't contribute to the final output but is typically more pronounced than blood reflections [11]. Given a fixed dynamic range of a receiver system, substantial portion is consumed by the static reflection, making it difficult to distinguish blood reflections from background noise.

Past approaches to address this challenge primarily focused on manipulating these two signal strengths:

- One approach involves reducing the strength of the clutter signal. The transducer central frequency is usually carefully chosen to minimize the attenuation and dephasing of skull [12]. Traditional TCD are usually performed through the region where the skull is at its thinnest. Therefore the attenuation and scattering is also lowest, Commonly used window are shown in Figure 1.2(a). In specific cases involving animal research or patients with skull injuries, skull thinning or removal is also possible [7]. However, these measures limit where TCD can be used and what TCD can detect.
- An alternative approach is achieved by injecting contrast agents into the blood-stream. Utilizing nonlinear imaging of injected microbubbles, higher-sensitivity imaging has been demonstrated. Nonetheless, maintaining a consistent concentration of microbubbles within the blood pool proves challenging [4].

Therefore, for broader utilization of transcranial Doppler ultrasound, enhancing the sensitivity of the receiver system itself holds significant importance.

1.2. Doppler Imaging Basics

1.2.1. Fundamental Principle of Doppler Imaging

Before diving into the Doppler probe system design, it is valuable to introduce some fundamental principles of Doppler ultrasound.

Doppler ultrasound is based on the principle of the Doppler effect, which is the perceived change in frequency if there is a relative velocity between the sound source

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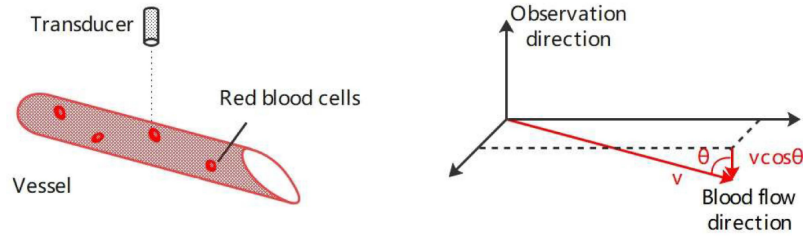


Figure 1.3.: Schematic of doppler effect applied in blood flow detection

and the observer. When the observer is moving away from the sound source, the received wave will have a negative frequency shift, and vice versa.

In Doppler ultrasound, the probe is usually fixed, and the blood cells are flowing, as shown in Figure 1.3. With the blood cells' velocity v , the sound speed c , the angle between ultrasound beam propagation direction and blood flow direction is θ and the transducer center frequency is f_s , the frequency shift of the reflected wave f_d follows the equation [13]:

$$f_d = \frac{2|v|\cos\theta}{c} f_s \quad (1.1)$$

Therefore, the blood velocity can be derived when the frequency shift is read out.

1.2.2. Doppler Categories: Continuous-wave & Pulsed-wave Doppler

Doppler frequency extraction methods vary across different Doppler systems. Doppler measurements encompass two types: continuous-wave (CW) and pulsed-wave (PW) measurements. A diagram is shown in Fig 1.4 to compare the differences.

CW Doppler measurement has the longest history in the field [14]. There are two transducers, or two sub-apertures of one transducer array in the system. One is continuously emitting the sound wave while the other is collecting the echos. Reflections from static components produce a tone at emitted frequency, while moving components generate the Doppler signal tone at an offset frequency. The receiver end processing can be done by down-converting the received signal and applying a high-pass filter. The drawback of CW Doppler is that it suffers from range ambiguity due to the absence of depth information.

To overcome the drawback of CW Doppler, PW Doppler is devised, where a pulsed wave with several cycles is emitted and being processed [15]. The depth of the scatterers can be read out with time delay and sound propagation speed known. However, time-domain waveform narrowing leads to spectrum broadening, causing overlap

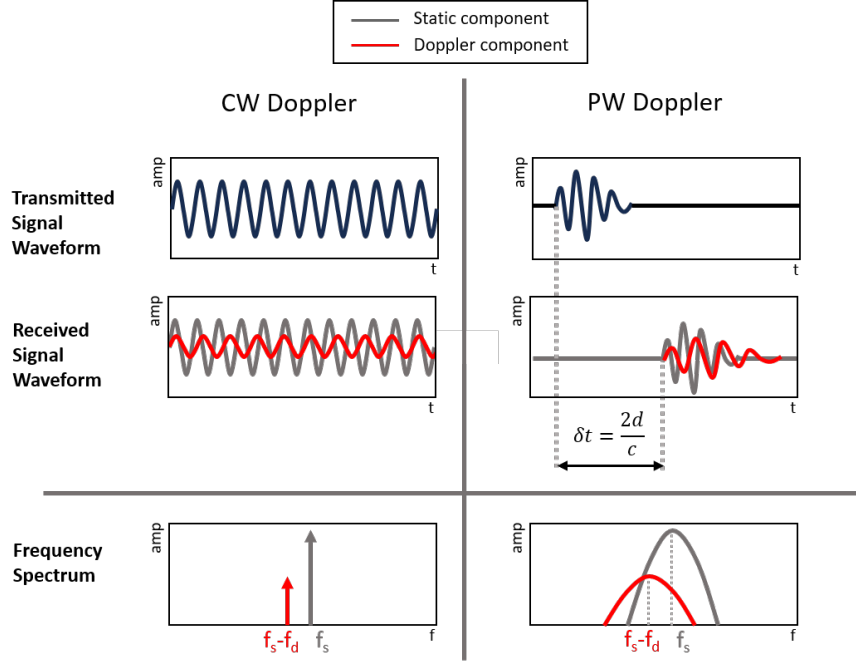


Figure 1.4.: Comparison of CW Doppler and PW Doppler.

between two signal spectra. This brings difficulty in the post-processing process. As the static component is usually much stronger than the Doppler component, the distortion of the static component could easily lead to error when estimating the Doppler shift by calculating the center frequency.[13].

1.2.3. Clutter Filtering in Pulsed-wave Doppler

As discussed in the last section, it is necessary to filter out the static component before calculating the Doppler shift. This process is called clutter filtering.

To overcome the difficulty of filtering the overlapped spectrum, clutter filtering normally utilizes multi-cycle processing. It records the reflected signal from multiple transmit/receive (T/R) cycles and performs filtering in the digital domain [13].

An example is given in Fig 1.5 to introduce this multi-cycle processing idea. Received signals from one blood cells that is flowing away from transducer are shown in the figure. The x-axis signifies time elapsed after pulse transmission in a T/R cycle, while the y-axis represents the T/R cycle count. To distinguish, this thesis designates time within a T/R cycle as the **fast time**, while the scale across T/R cycles is termed the **slow time**.

The slow-time processing utilizes the fact that the moving objects not only introduce a frequency shift in one T/R cycle, but also a time delay of the echoed signal. As-

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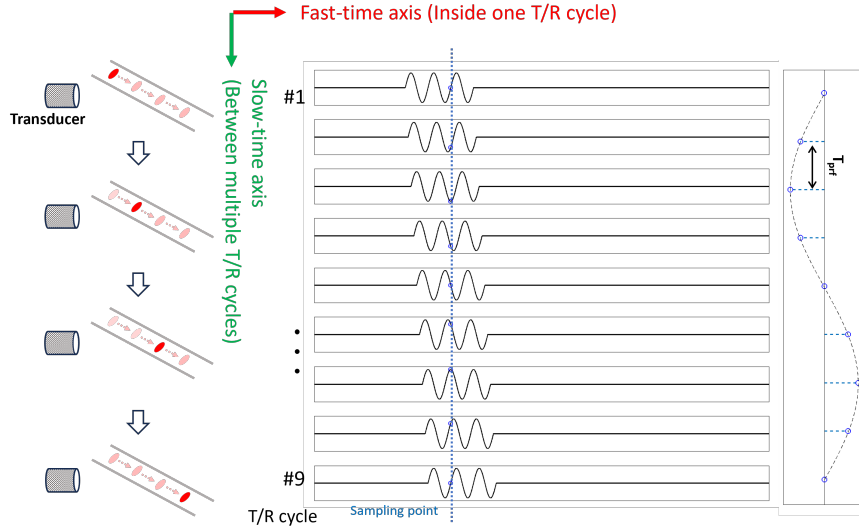


Figure 1.5.: Illustration of slow-time processing in PW Doppler

sume the pulse repetition frequency is f_{prf} . The time delay of one moving object's reflection signal between two consecutive T/R cycles is:

$$\delta t = \frac{2v \cos \theta}{c f_{prf}} \quad (1.2)$$

The time delay can be translated into a phase shift of: (Assuming $f_d \ll f_s$, so $f_s - f_d \approx f_s$)

$$\delta \phi = 2\pi \frac{2v \cos \theta}{c f_{prf}} f_s \quad (1.3)$$

Therefore, in the slow-time a sinusoidal sequence can be obtained with frequency of

$$f_{out} = \frac{\delta \phi}{2\pi} f_{prf} = \frac{2|v| \cos \theta}{c} f_s \quad (1.4)$$

which is exactly the Doppler shift frequency, referred to equation 1.1. A more rigorous derivation can be found in [13].

For static reflection, in contrast, its signal doesn't vary between successive T/R cycles; it is always a fixed value in slow-time domain. Therefore, in the slow-time spectrum, the static signal tone is at DC while the Doppler tone is at the Doppler shift frequency. Clutter filtering is thus possible in the slow-time domain.

One thing worth mentioning is that the clutter signal is not always from truly static scatters. Often either the tissue in the body is moving due to cardiac activity or

respiration, or the transducer itself is moving due to human motion [16]. But these frequencies are usually much lower than Doppler shift frequency. An quantitative example can be given to illustrate that: for ultrasound transducer center frequency at 1MHz and a blood cell velocity of about 0.5m/s, the Doppler frequency shift will be 677Hz. In comparison, both the respiration frequency or cardiac cycle are below the frequency of 10Hz. Therefore, the assumption that the static signal and the Doppler signal can be separated in the slow-time spectrum still holds true.

1.3. Previous Work: Pulsed-wave Doppler Hardware Design

One type of pulsed-wave Doppler system diagram is shown in Figure 1.6(a). The signal is amplified by the first-stage low-noise amplifier (LNA) to match the mixer's input scale. It's then multiplied with the emitted signal and subsequently low-pass filtered to eliminate the up-converted component. It is further sampled by analog-to-digital converter (ADC) at a fixed time point of each T/R cycle with the sampling frequency of f_{prf} . This sampled sequence is sent to a back-end DSP for processing. Processing begins with high-pass filtering to eliminate the clutter signal, followed by a frequency estimator for Doppler frequency read-out. The benefit of the demodulation-based system is to relax the sampling speed and conversion speed of ADC. The disadvantage is that mixer with high dynamic range requirement is hard to design. Also it only generates one sample point at one T/R channel, which greatly limits its usage and compatibility. For example, to read the information from the two blood vessels of different depth, two separate channels are needed. This system design with demodulation in the analog domain more serves as a compromised design considering the technology limitation of ADC speed. It is more frequently seen in designs from last century [17] [15] [18].

Nowadays, the pulsed-wave Doppler systems more rely on direct sampling of RF data. The system diagram is shown in Figure 1.6(b). The LNA is usually designed with a varying gain to compensate for the different attenuation of acoustic wave propagation from different depths. This function is called time gain compensation (TGC). The ADC is cascaded after the LNA with the sampling rate at a multiple of ultrasound center frequency. The sampled fast-time data is then reshaped in the back-end digital domain to perform the slow-time clutter filtering. The benefit of this design is that it facilitates more versatile back-end processing and it is compatible with B-mode imaging. It is commonly adopted in many commercial Doppler ultrasound system [19][20].

The biggest challenge for both systems discussed above is the stringent requirement of system dynamic range. As described in section 1.1.1, the received signal consists of a weak blood Doppler component on top of a large low-frequency clutter component. The system dynamic range is defined by the clutter component. Only when the system DR is design to be very large, it can achieve a medium blood signal SNR

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after the clutter filtering. In the application of TCD, the receiver system usually targets at dynamic range of more than 80dB [21][22].

This brings mainly two difficulties:

- For front-end design, it required more power consumption and design complexity. Suppression of receiver blocks noise to the desired dynamic range usually paid the price of increased power. It also limits the topology choice of blocks.
- For back-end processing, it also poses a higher requirement on the memory size and digital processing speed. The dynamic range of 80dB usually translates to the ADC resolution of more than 14bits. For example, ADC with 16bits at 10MHz sampling rate also generates the output data streaming of 20MB/s. And the situation is even worsen for a transducer matrix.

1.3.1. Clutter Cancellation Circuit

The dynamic range problem comes from the fact that the static clutter component defines the signal maximum scale until the slow-time clutter filter at the very back-end. Clutter component cancellation at the analog front-end is proposed to solve this problem [23]. As shown in Figure 1.6(c), A DAC is inserted at the ADC input to provide a copy of the static clutter component. Thus only the weak and dynamic Doppler component enters the ADC, which reduces the dynamic requirement of the ADC and shrinks the output data stream size. The DAC should be carefully designed with low noise for not making the noise contribution of feedback path dominant. However, this approach doesn't alleviate the challenges related to the LNA design, which typically consumes a significant amount of power within the receiver chain. As a result, the effect of the dynamic range relaxation is somewhat constrained. Moreover, it adopts an open-loop calibration scheme to ensure that the feedback path tracks the static part. This scheme requires periodic calibration cycles, which limit its applicability in various scenarios.

1.4. Proposal

In this study, a novel system structure is introduced to address the prevailing challenge of dynamic range limitations. The system-level representation is depicted in Figure 1.7. This design encompasses two enhancements, each representing a exploration into the concept of executing clutter cancellation at the receiver's front end.

- The first is to perform the clutter cancellation at the transducer end. Compared with previous clutter cancellation design, by now setting the cancellation point at the input of the whole receiver chain, the dynamic range of both LNA and

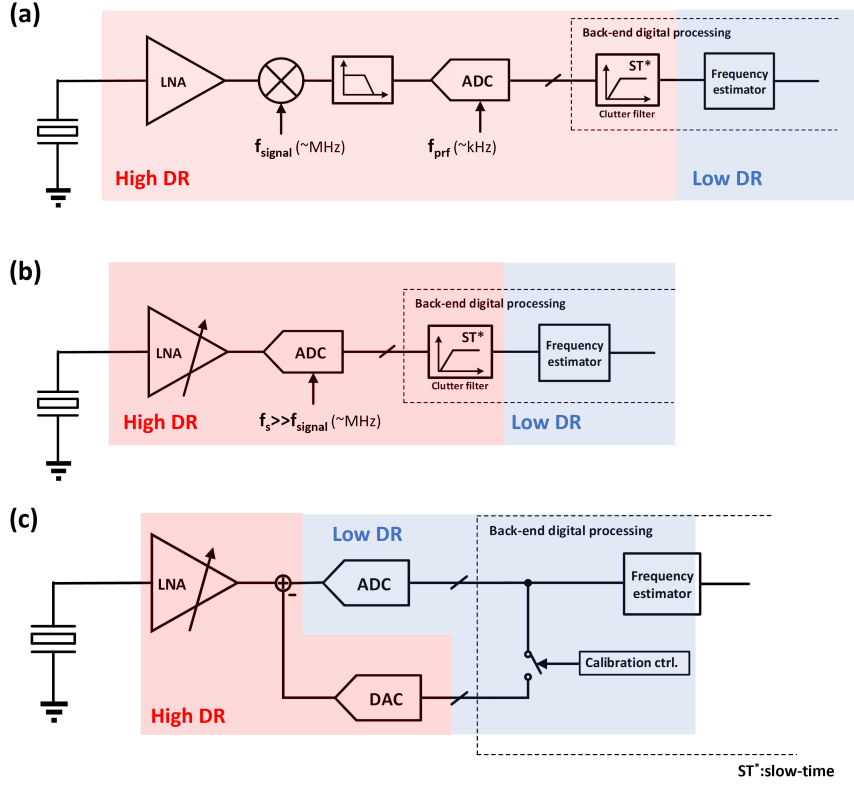


Figure 1.6.: Block diagram of previous PW Doppler ultrasound receivers: (a) down-mixing based system[17] [15] [18]. (b) RF-sampling based system [19][20]. (c) RF-sampling based system with clutter cancellation at the ADC input[23].

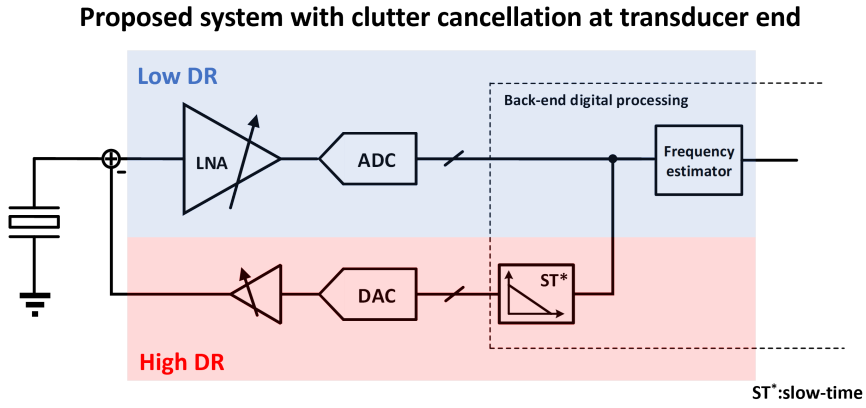


Figure 1.7.: Block diagram of proposed PW Doppler ultrasound receiver RF-sampling based system with clutter cancellation at transducer end

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ADC is relaxed. Therefore, it brings the benefit of further power reduction and complexity reduction of circuit design. At the same time, it still keeps the benefit of data stream reduction at the output of front-end.

- The second innovation is enabling of closed-loop clutter cancellation by introducing a slow-time loop filter. The slow-time integrator performs the averaging of signals from previous cycles, ensuring the feedback path to track the clutter components while not influencing the Doppler component. This point will be further discussed in Chapter 2. This is done in real-time during the measurement without the need for open-loop calibration. Therefore, it expands the horizons of its practical applicability.

The concept of implementing cancellation at the ultrasound receiver front-end holds multifaceted potential. While this work primarily serves as a prototype focused on the application of transcranial imaging, the system and block-level considerations can be applied to alternative application domains. One example lies in mitigating the challenge of leakage from the transmitting channel to the receiving channel inside the ultrasound system, where the static component from the cross-talk should be removed when isolation design is bad.

1.5. Thesis Outline

The structure of this thesis is organized as follows:

In **Chapter 2**, the architecture-level design of the system is elucidated using a top-down approach. The signal-flow level behavior of the system is introduced at the beginning, followed by an exploration of the circuit-level design. This chapter also presents simulation results, evaluations of circuit non-idealities, and introduces a stability model to analyze the slow-time feedback system.

Chapter 3 delves deeper into each block of the system. Rationale behind topology choices are presented, grounded on derived specifications. A transistor-level implementation, along with sizing details, is also included.

In **Chapter 4**, simulation results drawn from the transistor-level system implementation are provided. Analyses of SNR and the overall power consumption of the system are provided. Furthermore, a comparative study with state-of-the-art designs is highlighted.

Chapter 5 provides a summary of the thesis, pointing out the remaining tasks for completing the prototype and suggesting potential enhancements to the design.

2. Architecture Design

2.1. Specs Derivation

The first step is to establish system specifications to align with the target applications. The considerations related to these specifications are discussed below.

- **Transducer:** For this design, a single-element transducer with a center frequency of 1 MHz is chosen. While matrix implementation provides opportunities for advanced 2-D imaging with broader application prospects, the single-element transducer was selected to simplify the design and demonstrate its feasibility. The choice of the transducer frequency is primarily influenced by acoustic domain requirements and the specific application. A higher transducer frequency results in increased propagation attenuation through both tissue and the skull. However, it offers advantages such as higher back-scattering coefficients of blood cells and improved spatial resolution in 2-D imaging [24]. In the context of Transcranial Doppler (TCD), the attenuation through the skull plays a pivotal role, leading to the selection of a relatively low-frequency transducer operating at 1 MHz. A fractional bandwidth of 100% is assumed, translating to a bandwidth of interest ranging from 0.5 to 1.5 MHz.
- **Doppler Signal-to-noise Ratio:** The Doppler signal-to-noise ratio (SNR) is defined as the ratio between the blood reflection signal and the system background noise. It's important to note that this ratio does not account for clutter. This design aims for a Doppler SNR of 30 dB.
- **Distortion:** The tolerance for distortion in Doppler ultrasound applications is an intriguing aspect. Previous ASIC designs have primarily focused on B-Mode imaging, where distortion requirements are generally less stringent compared to noise. The impact of receiver system linearity on the final image and clinical diagnosis of Doppler ultrasound is not extensively discussed in the existing literature. In this design, a conservative goal is set to keep distortion much smaller than the noise level. A Total Harmonic Distortion (THD) target of -40 dB is set, specifically for the Doppler signal. It's important to emphasize that the linearity requirement for the feedback paths is even more stringent. This ensures that the distortion component of the clutter segment remains minimal, allowing the slow-time filter to effectively filter it out without compromising the output quality.

2. Architecture Design

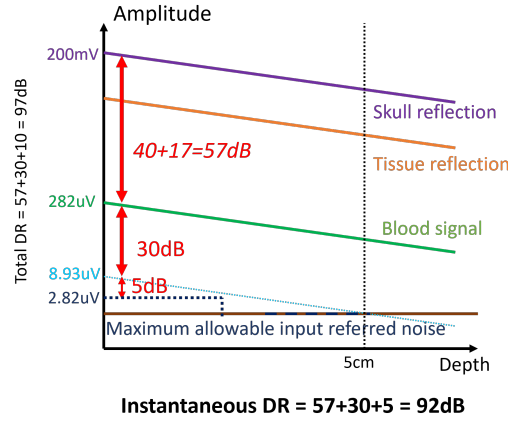


Figure 2.1.: Dynamic range requirement with time-gain compensation included

- **Dynamic Range:** In comparison to the Doppler SNR, the system's dynamic range is significantly larger as it is primarily defined by the substantial clutter component, often dominated by skull reflections. Based on measured data from previous Transcranial Doppler (TCD) studies involving the human skull, the ratio between static clutter and the Doppler signal is set at 57 dB[25]. Additionally, time-gain compensation should be taken into account. To maintain simplicity, a two-step time-gain compensation approach is adopted. The round-trip loss of a 1 MHz transducer at a target imaging depth of 5 cm is estimated to be 10 dB, based on an estimated attenuation of $1\text{dB}/\text{MHz}/\text{cm}$ [26]. This results in an instantaneous dynamic range of 92 dB and a total dynamic range of 97 dB. An illustrative graph is presented in 2.1. Note that the numbers shown in the y-axis are all voltage level referred to the output of the transducer, i.e. input of the whole system.
- **Area:** There is no strict upper limit on the area since this design utilizes a single-element transducer. However, considering the potential application scenario involving a matrix transducer, it would be advantageous if the ASIC area aligns with the pitch size of a matrix transducer. The pitch size should not exceed half of the wavelength, which can be calculated as follows

$$pitch < \frac{\lambda}{2} = \frac{v}{2f} = \frac{1500\text{m/s}}{2 * 1\text{MHz}} = 750\mu\text{m} \quad (2.1)$$

Therefore, the ASIC area should be smaller than $750 \times 750 \mu\text{m}^2$.

- **Technology:** Given the selection of a low-frequency transducer ($f_{center} = 1\text{MHz}$) and the benefit of leveraging existing designs from this group, the TSMC 180nm BCD process was chosen for this design.

The goal of this design is to meet these specifications while minimizing power consumption. A summary of the design specifications is provided in 2.1.

Trasducer frequency	1MHz
Bandwidth of interest	0.5-1.5MHz
Doppler SNR	30dB
THD	-40dB
Dynamic Range	97dB
Area	$0.5625mm^2$
Power	As low as possible
Technology	TSMC 180nm

Table 2.1.: Design Specs

2.2. Signal-flow Level Design

The general goal of architecture design at the signal-flow level is to ensure that the feedback signal effectively tracks the clutter component while preserving the integrity of the useful Doppler signal. This goal is accomplished through the implementation of a slow-time delta modulator. This section discusses the design considerations pertaining to this topology.

2.2.1. Slow-time Delta Modulator

Delta modulation is widely used in RF system design to reduce the dynamic range of transmitted signal [27]. It incorporates an integrator within the feedback path, quantizing only the difference between two samples in consecutive cycles, while preventing the DC or low-frequency component from entering the quantizer.

In this work, a similar idea is adopted by using an integrator to enable the feedback path to track the clutter component at DC or low frequencies while allowing the high-frequency Doppler signal to enter the receiver chain. The key distinction from a traditional delta modulator lies in the implementation of the loop filter in the slow-time domain. Instead of accumulating consecutive sampling points, this filter accumulates values from fixed time points across different T/R cycles.

The general signal-flow block diagram of this slow-time integrator is depicted in Figure 2.2. Within the bandwidth of interest, the blocks in the receiver path and feedback path can be simplified with gains denoted as A_{rx} and A_{fb} . The summation node is implemented at the input of the LNA to perform the clutter cancellation. Subsequently, the remaining signal is sampled by the ADC and sent to the digital block, where it is processed by the slow-time loop filter with a transfer function denoted as $L(z')$. It's worth noting that z' is employed to represent the slow-time domain, signifying sequences with intervals of T_{prf} . This loop filter is a slow-time first-order integrator with a gain index of α . The output of the loop filter is then fed back through a DAC to complete the clutter cancellation process.

2. Architecture Design

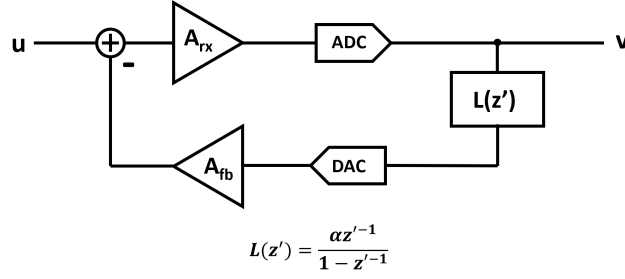


Figure 2.2.: Simplified system signal-flow diagram

An example waveform is presented in Figure 2.3 to facilitate the understanding of this architecture. In this example, a static signal, meaning it remains constant across each T/R cycle, is introduced into the system. This sequence is quantized by the ADC and accumulated within the loop filter over several T/R cycles. In a well-designed system, the residue gradually diminishes until it becomes smaller than one least significant bit (LSB) of the DAC.

A more detailed analysis of this clutter cancellation characteristic is provided below. The Signal Transfer Function (STF) from input u to output node v can be derived as follows:

$$STF_{|u \rightarrow v} = A_{rx} \frac{1 - z'^{-1}}{1 - (1 - \alpha A_{rx} A_{fb}) z'^{-1}} \quad (2.2)$$

The Bode diagram of this system is depicted in Figure 2.4 and it typically exhibits characteristics of a high-pass filter. As discussed in 1.2.3, this design choice enables effective clutter filtering, allowing the removal of clutter signals. The plateau region of the Bode plot forms a pass-band signal, which can be conveniently controlled by adjusting the digital coefficient α .

An important question to consider is whether first-order suppression is sufficient to filter out the clutter component. The answer is actually application dependent. In this work, the clutter component is assumed to be associated with skull reflections, which are predominantly at DC, with variations introduced primarily by slow changes in the measurement setting, such as low-frequency movements (below 0.1 Hz). Consequently, a first-order loop filter is deemed adequate. Another rationale for not opting for a higher-order loop filter relates to stability considerations, as will be elaborated upon in Section 2.4.4.

2.2.2. Output Reconstruction Design

One issue with the delta modulator is that at the output node, it contains not only the signal from Doppler reflection but also quantization noise from the feedback

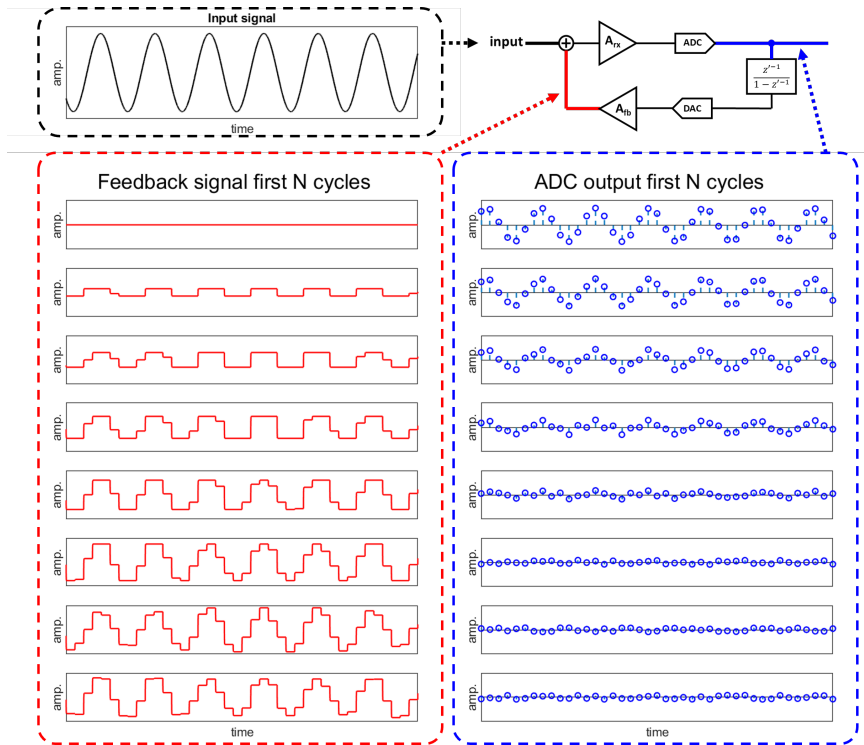


Figure 2.3.: Illustration of a slow-time delta modulator with a static input

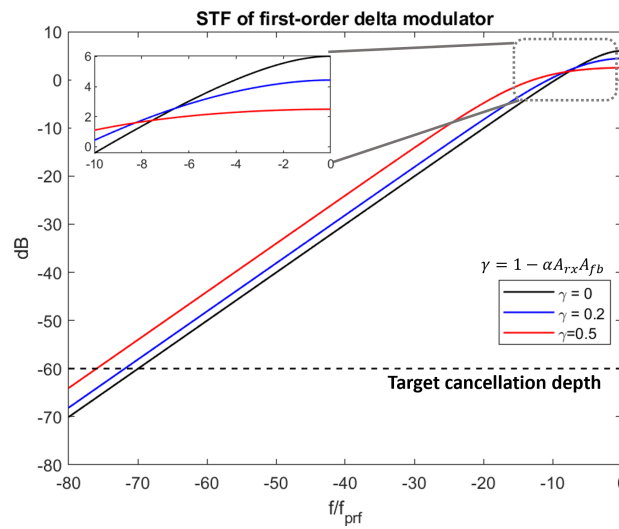


Figure 2.4.: STF of first-order delta modulator

2. Architecture Design

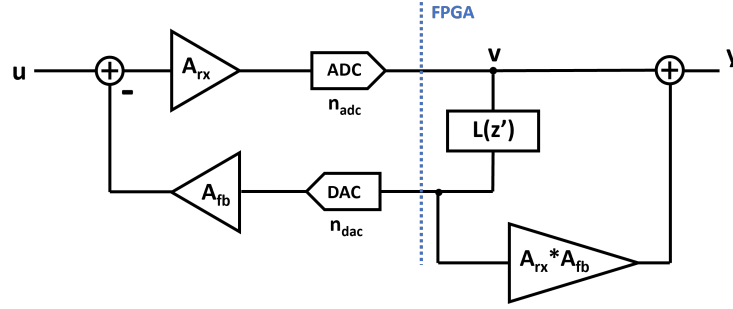


Figure 2.5.: Output reconstruction of the slow-time delta modulator

path. Therefore, an additional step of output reconstruction is required to restore the original signal

A possible approach is illustrated in Figure 2.5, and it can be understood as follows: In each T/R cycle, the loop filter produces a coarse quantization result of the input sequence in the feedback path. Subsequently, after passing through the feedback node, the residue undergoes further amplification and quantization. By combining the coarse result from the DAC input and the fine result from the ADC output, with a loop gain of $A_{rx}A_{fb}$, the original signal can be reconstructed.

It's important to note that through the output reconstruction process, the signal at node y follows:

$$STF_{|u \rightarrow y} = A_{rx} \quad (2.3)$$

Detailed derivation of this output reconstruction can be found in Appendix A. At the final output node, the complete spectrum is obtained with a gain of A_{rx} , enabling diversified back-end signal processing. Simultaneously, the slow-time high-pass characteristic is provided only at node v to ensure that the clutter component does not enter the receiver path.

The previous discussion was based on the assumption that the bandwidth of all analog blocks is sufficiently large and that the delay is negligible. However, this is not the case in real-world designs. The effect of reconstruction is significantly compromised when considering limited bandwidth. The fine part experiences delay due to contributions from every analog block in the loop, while the coarse part from the DAC is processed in the digital domain without delay. This issue can be mitigated by employing an equalizer in the reconstructed path, a topic which will be further explored in Section 2.4.3.

2.2.3. DAC & ADC Resolution

The resolution of both the ADC and DAC depends on the system's dynamic range requirements.

The signal from the feedback path can be considered as a copy of the clutter component with quantization noise introduced by the DAC. To prevent this quantization noise from dominating the dynamic range of the receiver path, its amplitude should be designed to be smaller than that of the Doppler signal. Consequently, it is calculated at the feedback node as follows, the term Amp is used to represent the amplitude of signal and noise:

$$Amp_{fb,noise} < Amp_{doppler,in} \quad (2.4)$$

$$A_{fb} \frac{Amp_{max,dac}}{2^{n_{DAC}}} < \frac{Amp_{max,in}}{10^{57dB/20}} \quad (2.5)$$

Where A_{fb} is scaled for matching the maximum DAC signal with input signal, it follows that,

$$A_{fb} Amp_{max,DAC} = Amp_{max,in} \quad (2.6)$$

Thus,

$$n_{DAC} \geq 10 \quad (2.7)$$

The ADC resolution is linked to quantization noise. Since this architecture is already advantageous in reducing quantization noise, thermal noise presents a greater challenge. Therefore, to ensure that the quantization noise is at least 10 dB smaller than the thermal noise:

$$SQNR > DR + 10dB \quad (2.8)$$

$$(6.02n_{adc} + 1.76) + A_{rx} > 102dB \quad (2.9)$$

As A_{rx} depends on the difference between the clutter part and Doppler signal, it has the value of 57dB. Thus,

$$n_{adc} \geq 8 \quad (2.10)$$

In this design, both the ADC and DAC are set with a resolution of 10 bits. It's worth noting that the ADC resolution is slightly higher than the requirement, which stems from considerations related to the design complexity and the reuse of the existing ADC design within this group, but it's important to acknowledge that a lower resolution ADC is certainly feasible and could offer advantages.

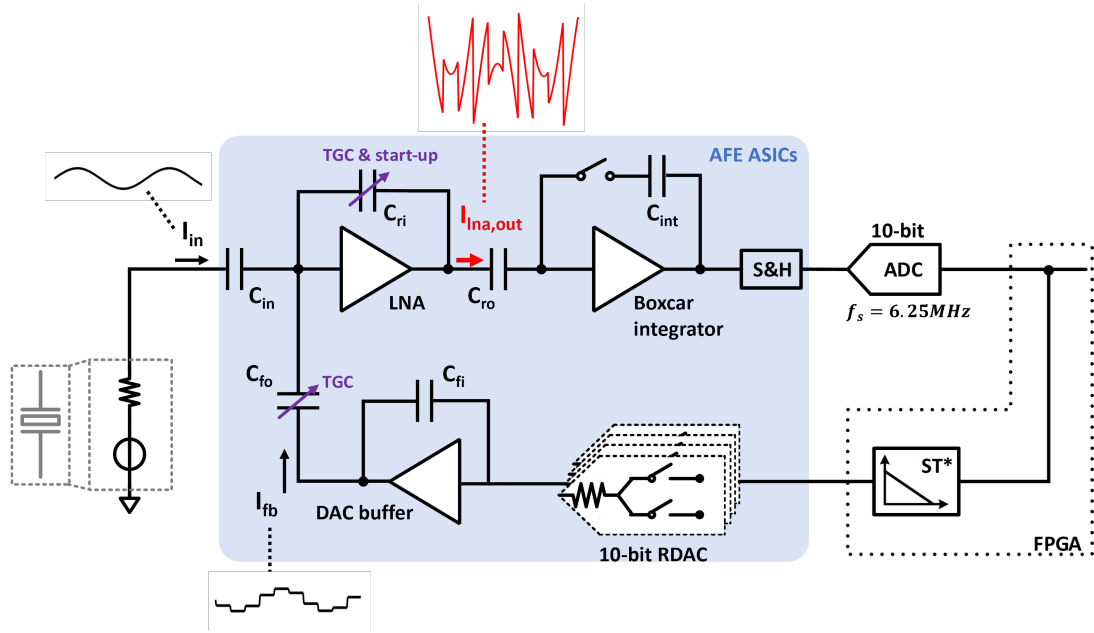


Figure 2.6.: System diagram with circuit block implementation

2.3. Circuit Level Design

The system implementation with circuit blocks is presented in Figure 2.6.

The system is designed to operate in the current domain. This facilitates the cancellation node design based on a closed-loop OTA integrator as LNA, with its virtual ground of LNA to absorb all the current and summed it at the capacitor.

Typically, commercial single-element transducers deliver an output via a BNC connector that has a 50Ω impedance. To intercept this signal, a capacitor, denoted as C_{in} , acts as a high-impedance load. This setup captures the voltage, converts it to current, and directs it to the LNA's virtual ground. A notable advantage is the inherent noiselessness of the capacitor, allowing flexibility in its value selection without noise constraints. Nevertheless, the capacitor yields a differentiated version of the input, which can be rectified during back-end digital processing.

The feedback path comprises a 10-bit RDAC and a buffer with a current gain of $A_{fb} = C_{f0}/C_{fi}$. Compared with a feedback path solely using a DAC, incorporating a buffer yields multiple advantages. Firstly, it introduces the TGC function without the need for excessive DAC resolution and noise design. As the cancellation node is now near the transducer node, the feedback path also needs to provide the TGC. Implementing TGC at the buffer end is straightforward: one can switch the output capacitor C_{f0} , ensuring the feedback signal and noise scales proportion-

ately. Second, the buffer offers a gain that allows the DAC's maximum output adjust flexibly to scale with noise specifications.

After the cancellation at the transducer side, the remaining current is then directed into the receiver path. The receiver path also functions as a current amplifier with its gain defined by $A_{ina} = C_{ro}/C_{ri}$. Subsequently, the output current is routed into a Boxcar integrator and an ADC with a sampling circuit. The loop filter and output reconstruction are implemented in an FPGA.

The capacitor values of the LNA feedback capacitor C_{ri} and the feedback path coupling capacitor C_{fo} are set to be variable for the purposes of TGC and startup. Startup is necessary because the slow-time integrator requires several T/R cycles to capture the clutter signal fully. Consequently, during the initial T/R cycles, a portion of the clutter signal enters the receiver path. As the gain of the receiver path is determined by the Doppler signal, it is gradually increased during startup to prevent saturation when the clutter component is not entirely removed.

2.3.1. Cancellation Node Design with OTA-C Topology

The LNA can be viewed as a closed-loop OTA-C integrator, which integrates the input current to generate an output voltage. This voltage is then differentiated by the output capacitor to produce a current output for the subsequent Boxcar integrator. Compared to other integrator designs like open-loop gm-C integrators [28] [29], this approach offers the advantages of low distortion and a well-defined common-mode voltage.

The drawback of this OTA-C topology is its difficulty in achieving high bandwidth. When targeting the same unity gain bandwidth, the closed-loop bandwidth is typically lower due to the increased gain required to stabilize the loop. This bandwidth limitation is more pronounced in this design, as the receiver path needs to provide a closed-loop gain of approximately 60 dB to amplify the weak Doppler signal.

The impact of bandwidth on the output is illustrated in Figure 2.7. Concerns about limited bandwidth primarily stem from three aspects. Firstly, excess loop delay can potentially lead to instability, which will be discussed in Section 2.4.4. Secondly, there's SNR degradation, as the feedback path includes a step-like DAC current, causing high-frequency quantization error that affects output reconstruction. A solution involving an equalizer is described in Section 2.4.3. Thirdly, parasitic transmission can occur, with the step-wise function resulting in spikes near the transducer. These glitches typically consist of high-frequency components beyond the transducer's bandwidth, which are suppressed by the transducer's filter characteristics. Initial simulation-based evaluation indicates that parasitic transmission is negligible (at least -10 dB lower than the input-referred noise) in this design.

2. Architecture Design

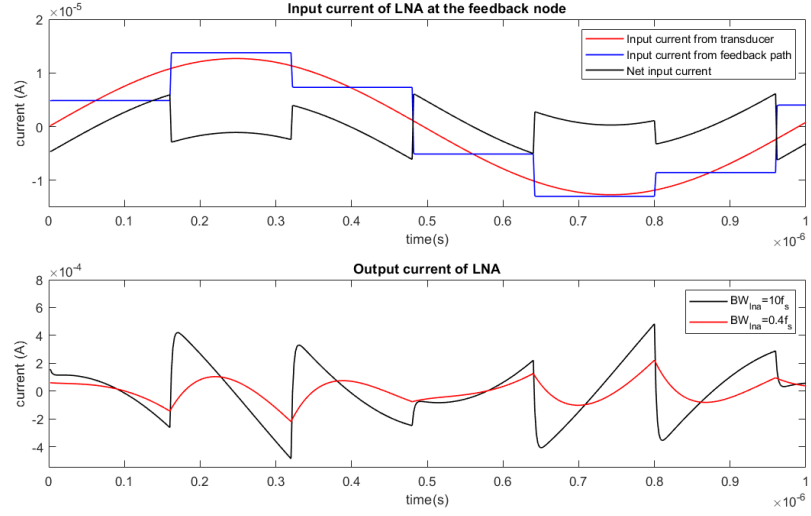


Figure 2.7.: Input & output waveform of LNA for different bandwidth (BW)

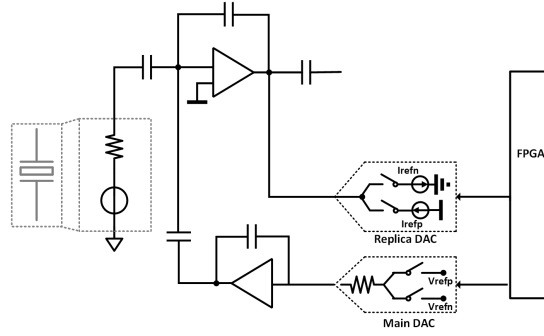


Figure 2.8.: Illustration of cancellation node design with replica DAC

An appealing solution to address the bandwidth limitation problem is explored in this design, as depicted in Figure 2.8. The concept is to utilize a replica path to compensate for the OTA's inability to handle high-frequency input. This missing high-frequency component can be directly injected at the output using a replica DAC. A similar idea is proposed in [30] with the aim of reducing virtual ground swing. This configuration results in an all-pass signal transfer function, where the high-frequency components do not appear at the virtual ground, and it significantly reduces delay.

However, the problem with this solution is that, for complete bandwidth enhancement, a replica of the input signal is also required to be fed into the output path. Designing such a system within this architecture is challenging because the replica path should also perform a differentiation operation, similar to the role of C_{in} in converting the input voltage to current. However, achieving this without excessively

loading the OTA seems impractical in this design. When the replica path consists solely of feedback components, it can lead to a significantly larger voltage swing at the virtual ground of the OTA. In this scenario, the summation node is not at the input of the OTA but rather at the output.

Therefore, it appears that we must work within the constraints of this limited bandwidth LNA and carefully design the circuit blocks to ensure stability and preserve the output SNR.

2.3.2. Boxcar Integrator

After the cancellation node at the LNA, the output current is directed into the Boxcar integrator to convert the current into a voltage signal that is ready to be sampled. The diagram and waveform of the Boxcar integrator are presented in Figure 2.9. Within each sampling window, the input current undergoes integration, and at the end of the sampling window, the output voltage is extracted as the sampled voltage output.

One notable advantage of this Boxcar integrator is its inherent anti-aliasing characteristic. By employing windowed integration, as depicted in Figure 2.9(b), its transfer function is equivalent to a sinc filter cascaded with a traditional sampler [31]. This sinc filter typically functions as a first-order low-pass filter with notches occurring at integer multiples of f_s .

The presence of this anti-aliased filter is crucial for mitigating the effects of sampling clock leakage in the Boxcar sampler, which can introduce tones at multiple frequencies of f_s . Additionally, the low-pass characteristic plays a role for suppressing noise from the LNA, which will be discussed in Section 3.1

2.4. System-level Simulation Results

In this section, system-level simulation results are discussed. The simulations were mostly done using Matlab. This section also discusses how circuit non-idealities influence the system.

2.4.1. Clutter SNR & Doppler SNR

For system benchmarking, a two-tone test is employed, wherein the input comprises two tones. One is the clutter signal, assumed to be a sinusoidal wave with a frequency of $f_{\text{clutter}} = 1$ MHz. The other is the Doppler signal, which is attenuated by 57 dB compared to the clutter signal and has a frequency of $f_{\text{doppler}} = 0.8$ MHz. It's worth noting that the Doppler shift is exaggerated to ensure clear separation of

2. Architecture Design

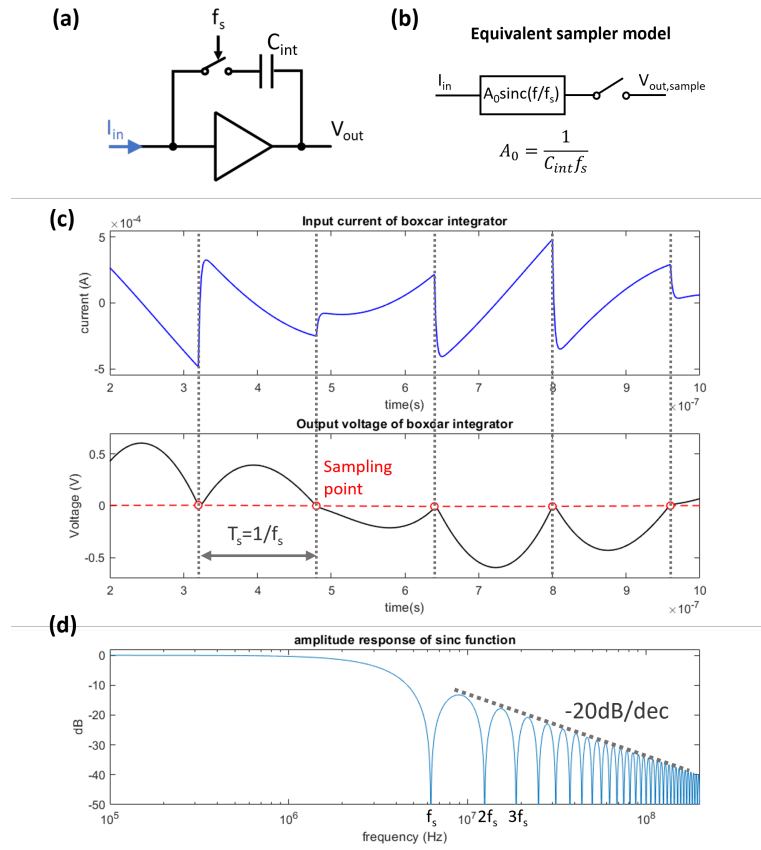


Figure 2.9.: Boxcar Integrator: (a) block diagram (b) analysis model (c) waveform (d) spectrum of sinc filter

2.4. System-level Simulation Results

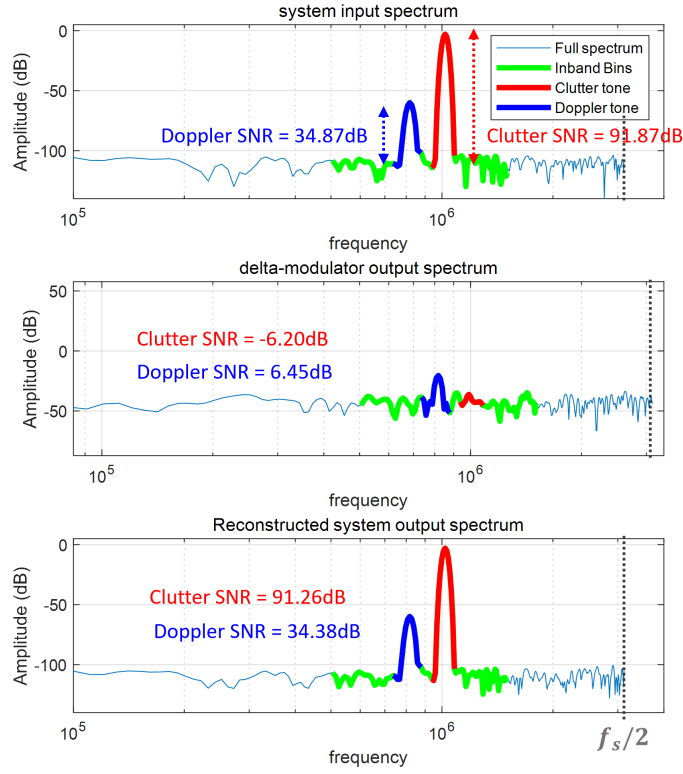


Figure 2.10.: Spectrum of system from a two-tone test

the two tones in the spectrum. To create a Doppler signal that varies in the slow-time domain, the phase of the Doppler signal varies across different T/R cycles. Noise is added at the input to represent the input-equivalent noise of all the blocks in the system.

The fast-time spectrum is plotted in Figure 2.10. The clutter SNR is defined as the ratio between the clutter signal and the noise background. This defines the system dynamic range, while the Doppler SNR serves as a metric for evaluating the output signal quality and is defined as the ratio between the Doppler signal and the noise background.

Note that at the output of the slow-time modulator (i.e., at the ADC output), the clutter tone is completely canceled, transforming into quantization noise from the DAC contribution. Furthermore, the Doppler SNR remains above 0 dB, indicating that the dynamic range of the receiver path is primarily influenced by the Doppler signal, aligning with the design target. In the reconstructed system output spectrum, the original input spectrum is largely restored, with a slight degradation stemming from the quantization noise of the ADC.

2. Architecture Design

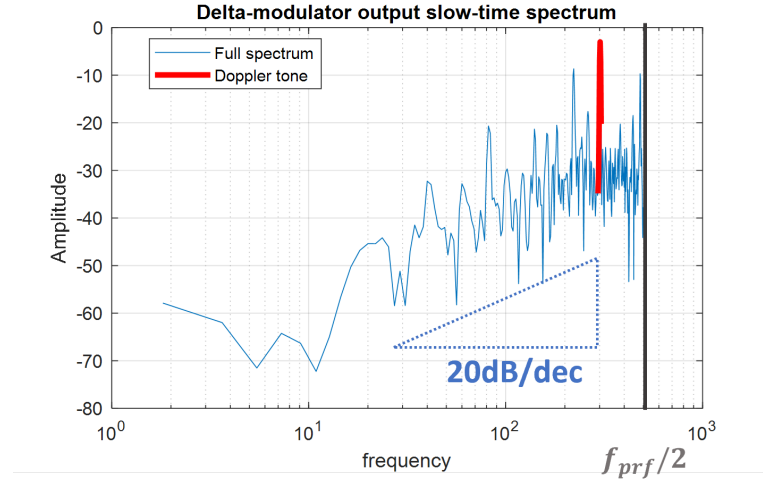


Figure 2.11.: Slow-time spectrum of delta modulator output

The slow-time spectrum is plotted in Figure 2.11. The first-order high-pass characteristic is clearly evident in the spectrum.

2.4.2. DAC Mismatch

Previous simulations were based on ideal blocks. Therefore, the non-idealities of these blocks should be carefully examined. First, let's discuss the influence of DAC mismatch. DAC mismatch introduces an error term at the feedback node, which can degrade the SNR. The simulation results shown in Figure 2.12 help assess how much DAC mismatch or non-linearity can be tolerated

In this simulation, the DAC implementation is assumed to have a hybrid structure with 7-bit binary R-2R MSB and 3-bit unary LSB. All unit resistors are assumed to have the same standard deviation σ . Differential Non-Linearity (DNL) and Integral Non-Linearity (INL) are also extracted in the figure.

It's quite interesting to note that the Doppler SNR shows greater tolerance for DAC mismatch compared to the clutter SNR. One possible explanation is that mismatch of DAC causes the distortion in the feedback path. The feedback component mainly consists of the clutter component and DAC noise. The harmonics of the clutter part remain static and can be filtered out by slow-time filtering, thus not significantly degrading the Doppler SNR. Therefore, it's only when the mismatch is large enough that harmonics of quantization noise result in drops in the Doppler SNR.

From the simulation results, it is evident that the DAC imposes matching requirements of DNL ideally being smaller than 0.25 LSB. In the simulated hybrid structure it translates to mismatch standard variation σ of unit resistor smaller than 0.4%, which is quite feasible.

2.4. System-level Simulation Results

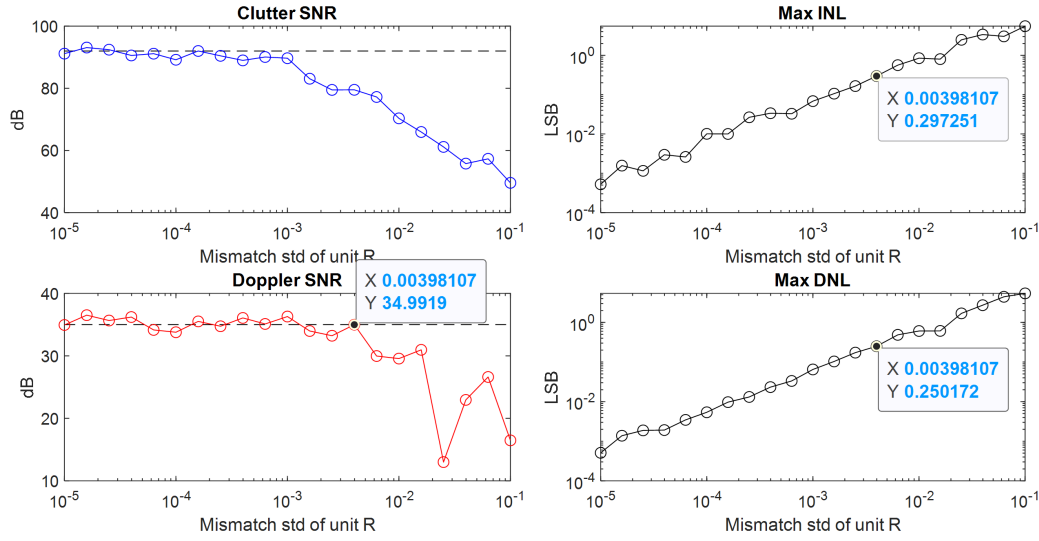


Figure 2.12.: Influence of DAC mismatch on SNR and linearity

2.4.3. Limited Bandwidth

Another non-linearity that can degrade SNR is limited bandwidth, which introduces delay to the signal as it propagates along the loop, consequently causing SNR degradation in the final reconstruction step.

As discussed in Section 2.3.1, typically, among all the blocks in the loop, the LNA is the point that limits the bandwidth. Therefore, a model with a dominant pole determined by the LNA is discussed here. The feedback path is also modeled to have a pole, which is at a much higher frequency of $10f_s$ compared to the LNA bandwidth. As shown in Figure 2.13, the SNR can be degraded by a few or tens of dB when the LNA bandwidth is comparable to the sampling frequency.

To mitigate this issue, an equalizer is inserted to compensate for the delay in the reconstruction process. This requires an additional calibration cycle for training the equalizer, as illustrated in Figure 2.14. As shown in Figure 2.13, this allows the LNA bandwidth to be as low as $0.3f_s$. Therefore, the cost of a calibration cycle appears to be worthwhile.

2.4.4. Stability Criteria for Slow-time Delta Modulator

Stability is a crucial consideration for all feedback systems. However, in the case of systems with slow-time feedback, stability issues have not been thoroughly discussed before. In this section, we delve into the stability problem specific to a slow-

2. Architecture Design

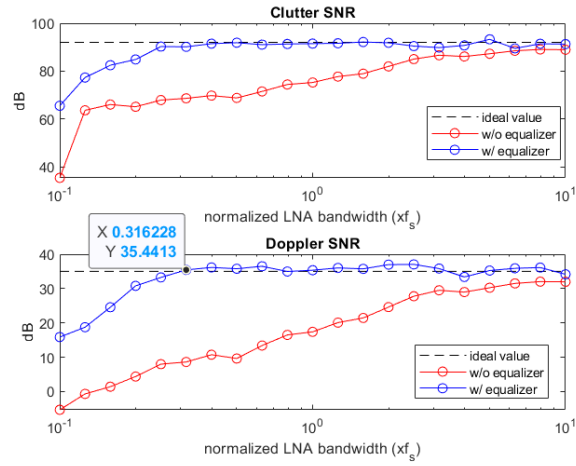


Figure 2.13.: Evaluation of equalizer effect with comparison

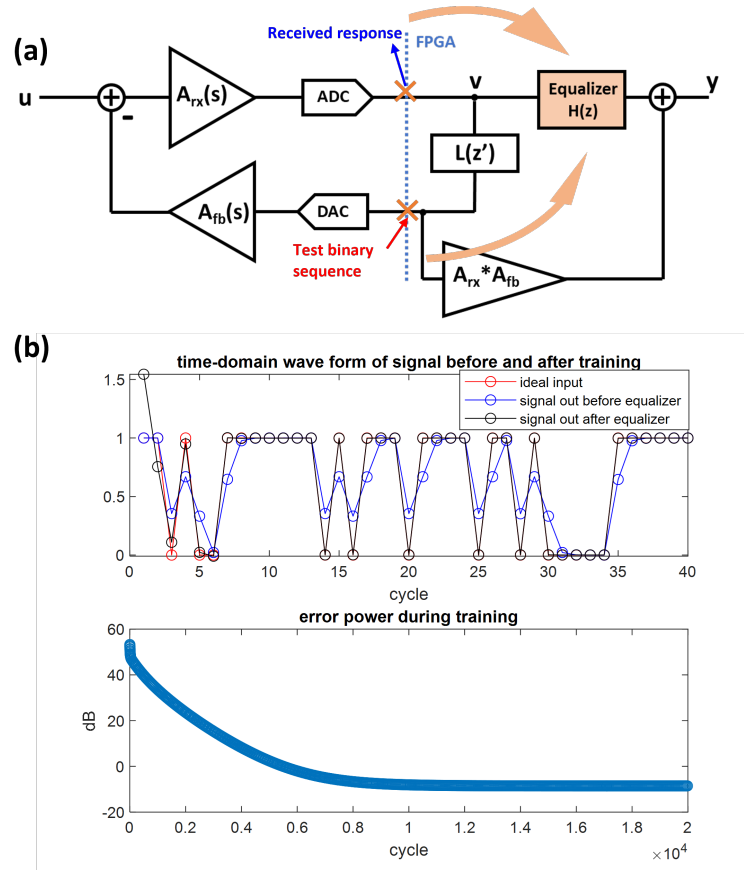


Figure 2.14.: (a) Block diagram and illustration of the calibration cycle (b) Training process of the equalizer

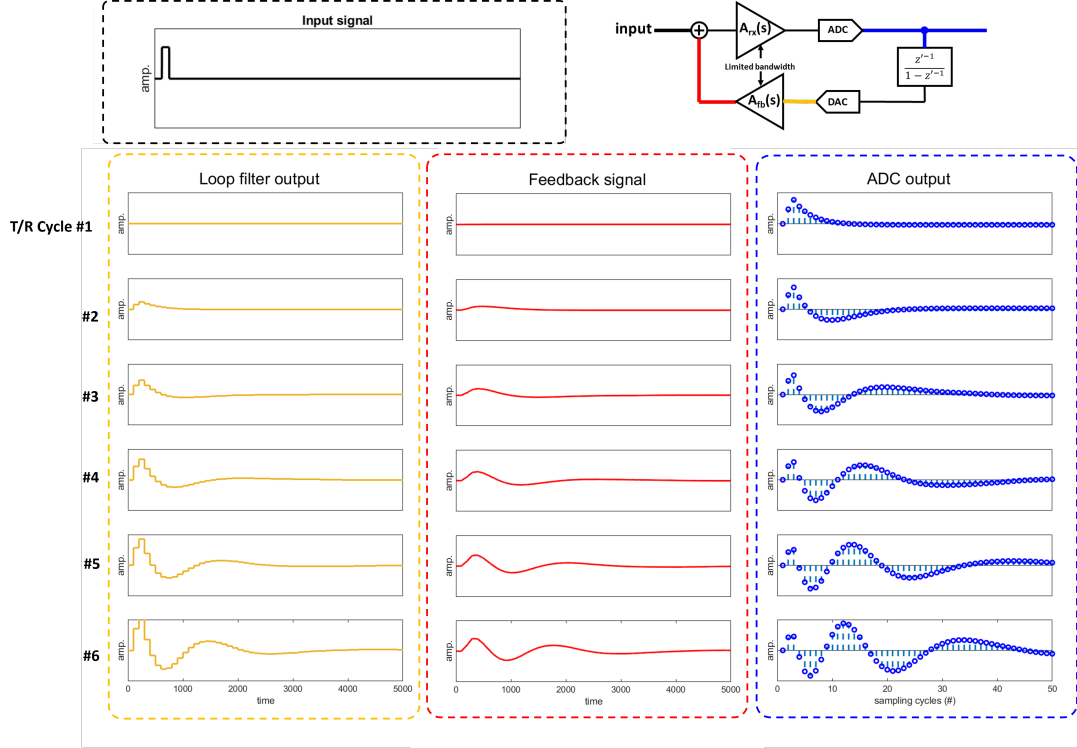


Figure 2.15.: Illustration of instability in a slow-time delta modulator

time feedback system and derive stability criteria for the design presented in this work.

Similar to traditional fast-time delta-sigma modulators, the risk of instability is also related to the loop bandwidth, specifically, the excess loop delay.

An illustration of the potential instability of a slow-time feedback system is presented in Fig 2.15. Here, the impulse response of the system is focused. An impulse function is injected into the system as the input for every T/R cycle. The limited bandwidth of the amplifiers results in a delay as the signal propagates within the loop. The lower the bandwidth, the greater the time shift between the feedback signal and the input signal intended for cancellation. When this error becomes too large, it enters the loop filter, gets amplified with each T/R cycle, and eventually leads to system oscillations

A comprehensive representation of this oscillation behavior is depicted in Fig 2.16. The signal at the ADC input is visualized in a 3D plot, where the x-axis corresponds to fast-time sampling cycles, the y-axis to slow-time T/R cycles, and the z-axis to signal amplitude. It is interesting to note that this oscillation is more pronounced along the slow-time axis.

2. Architecture Design

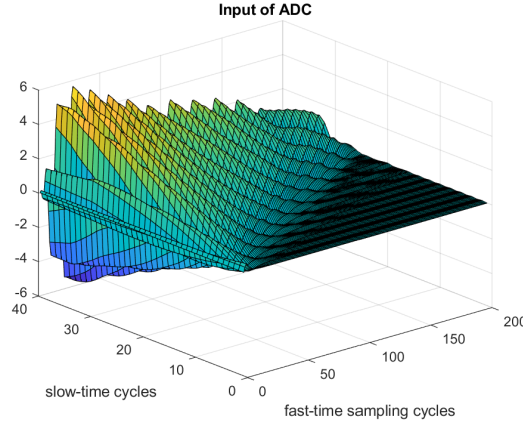


Figure 2.16.: 3-D plot of instability in a slow-time delta modulator

This phenomenon can be analyzed using the models below. The system diagram, including considerations for fast-time bandwidth, is presented in Figure 2.17(a). Here, $H_{rx}(s)$ and $H_{fb}(s)$ are employed to describe the transfer functions of all the components in the receiver path and feedback path, including the sampling and zero-order hold operations.

For a first-order slow-time integrator as the loop filter, where $L(z') = \frac{\alpha z'^{-1}}{1 - z'^{-1}}$. Assume that there is no input fed in, but for the initial state there is a sequence at the system output $v(s, z')$ and the loop filter output $f(s, z')$, where s stands for fast-time domain. It follows the relationship:

$$f(s, z') = z'^{-1} f(s, z') + \alpha z'^{-1} v(s, z') \quad (2.11)$$

$$v(s, z') = H_{fb}(s) H_{rx}(s) f(s, z') \quad (2.12)$$

Thus,

$$v(s, z') = z'^{-1} (1 - \alpha H_{fb}(s) H_{rx}(s)) v(s, z') \quad (2.13)$$

This implies that for an output sequence, as it propagates in each slow-time cycle, its spectrum can be calculated by multiplying it with the loop transfer function $(1 + \alpha H_{fb}(s) H_{rx}(s))$. Therefore, this slow-time system can be expanded into a fast-time sequence that propagates through a chain of loop transfer functions given the initial state $u(s)$, as depicted in Figure 2.17(b).

Therefore, the stability depends on whether this loop transfer function leads to infinity.

$$\lim_{n \rightarrow \infty} |(1 - \alpha H_{fb}(s) H_{rx}(s))^n| < 1 \quad (2.14)$$

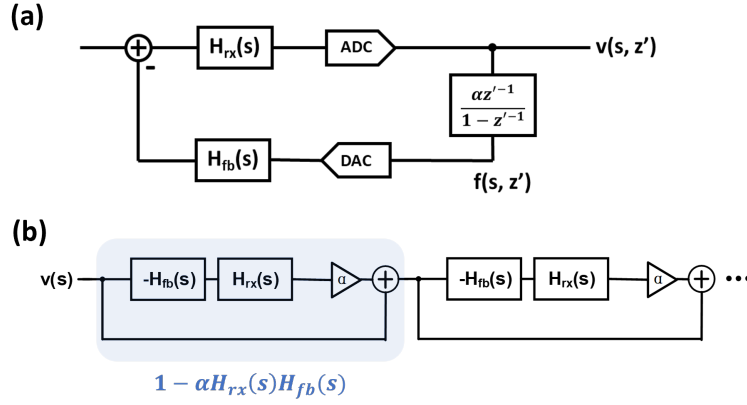


Figure 2.17.: Analysis model of slow-time stability

The stability criteria can be established as follows:

$$|1 - \alpha H_{fb}(s) H_{rx}(s)| < 1 \quad (2.15)$$

For this current-mode slow-time delta modulator with a Boxcar integrator, the transfer function model is presented in Figure 2.18(a). Similar to the previous section, it is assumed that the dominant pole lies in the LNA. The DAC buffer also contributes a pole but at a higher frequency. The sinc function in the feedback path arises from the Zero-order hold (ZOH) operation of the DAC, while the sinc filter in the receiver path results from the boxcar integrator. As depicted in 2.18(b), the bode plot of stability function $1 - \alpha H_{fb}(s) H_{rx}(s)$ is derived step by step.

Validation of this stability criteria is provided in 2.19. Here, the bandwidth of the LNA and DAC path is intentionally reduced to study the stability margin. The simulation results align well with the analysis model.

By confirming that the analysis framework is correct in predicting stability, valuable design insights can be gained from this model. In addition to increasing the bandwidth of the blocks, other methods to improve stability include reducing the sampling frequency and decreasing the digital gain index α . Decreasing the sampling frequency involves a trade-off between stability and the dynamic range of the receiver path. As shown in 2.9(b), the maximum output swing at the boxcar integrator is limited by the maximum integrated value, and a larger sampling period (i.e., integration window) results in a larger swing. On the other hand, the second method of reducing α is achieved at the cost of reduced filter depth for the delta modulator, as when α approaches zero, the corner frequency also moves to DC. In this work, stability is ensured by choosing a low f_s (6.25MHz) and carefully designing the blocks to meet the bandwidth requirements.

2. Architecture Design

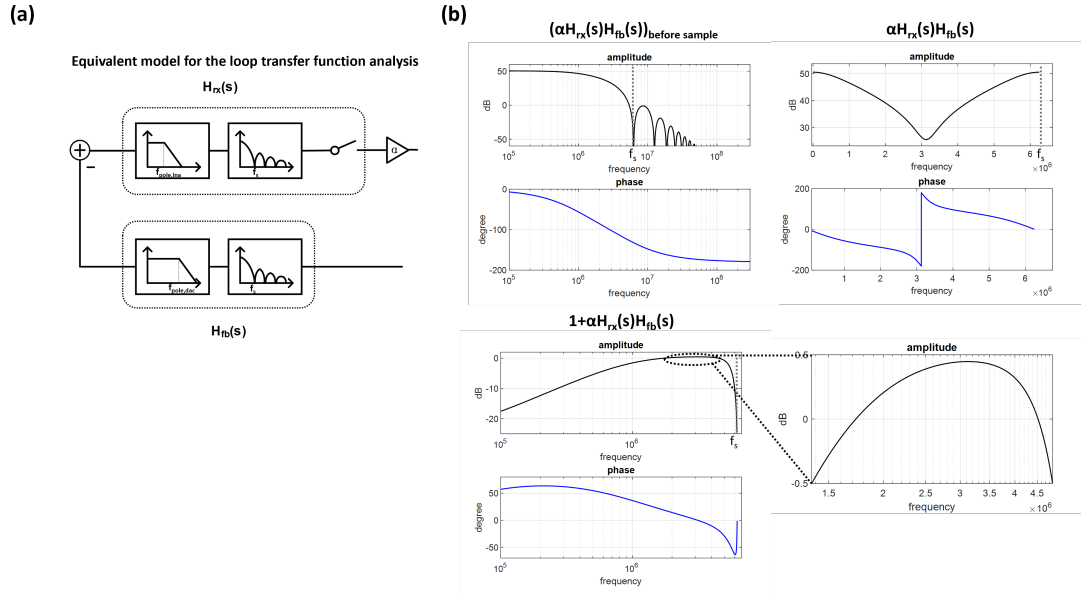
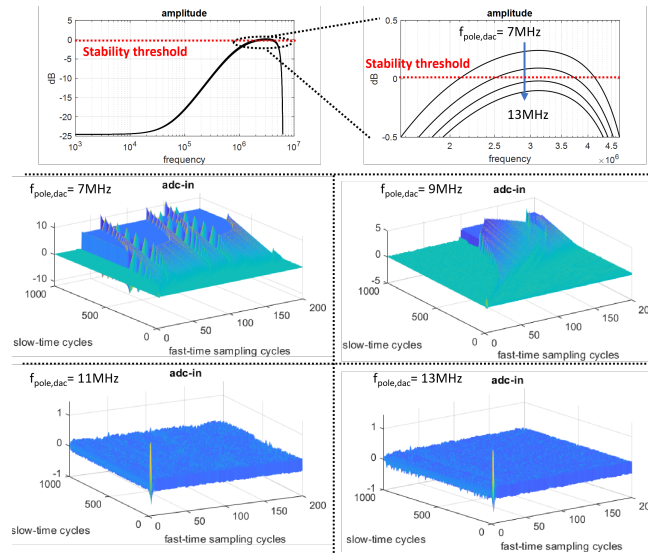


Figure 2.18.: (a) System transfer function modeling (b) Bode plot of the system stability function



2.5. Conclusion

In summary, in this chapter, the design specifications have been derived based on the application scenario and practical considerations. Based on these specifications, design considerations at both the signal-flow level and circuit-implementation level have been discussed. Finally, Matlab-level simulation results have been provided, with circuit non-idealities also considered.

The important take-away messages for guiding the block designs are summarized below.

- For the correct reconstruction consideration, the linearity of feedback path should be carefully design. The design target is set based on simulation with DAC $DNL < 0.2$ and DAC buffer $THD < -80dB@V_{pp} = 1.2$.
- For minimizing excess loop delay and also for stability consideration, the loop bandwidth limitation point is set at the LNA, while other blocks' bandwidths should be designed for as far away from the sampling frequency as possible. The design target is also set based on simulation, with LNA $BW \geq 2MHz$ and for DAC and DAC buffer the bandwidth should satisfied $BW > 2f_s$.

3. Block-level Circuit Design

In this chapter, the design and reasoning behind the circuit block choices and numerical values are discussed.

The circuit block diagram of the whole system is replotted here in Figure 3.1 to offer a comprehensive overview. A input capacitor is inserted for converting the transducer voltage into input current. The feedback path consists of current-domain resistive DAC that provides the clutter signal for cancellation, along with a buffer following to match its scale with the input current. A continuously running integrator driving a capacitor load acts as a current amplifier at the front end of receive path to set the noise floor. The difference between input current and feedback current is amplified and sent into the Boxcar integrator. Then the Boxcar integrator average the input current in a fixed window and then provides a voltage output to the later-stage sample-and-hold circuit. All the blocks in this system share the same supply of 1.8V.

The input capacitor is chosen as $C_{in} = 20pF$. This selection strikes a balance: it offers low impedance for current sinking when compared to the I/O parasitic capacitors in parallel, yet it also ensures relatively high impedance against the 50Ω output impedance of the single-element transducer. It's important to emphasize that this choice is a preliminary estimation. For precise on-chip applications, this value should be carefully re-evaluated based on the specific transducer selection and I/O characteristics. Using this value as a reference, other capacitor values can be determined in relation to the desired output swing.

The subsequent sections of this chapter delve into the specifics of each individual block.

3.1. LNA

The LNA plays a pivotal role in this design, primarily due to its substantial power consumption and its role as the bandwidth-limiting component in the entire system loop.

From C_{in} value chosen, the feedback capacitor C_{ri} is chosen to meet the output swing of 0.9V. It has the nominal value of $500fF$ and switch to $281fF$ when TGC implied. Then C_{ro} is chosen for minimizing the input-referred current noise. Considering

3. Block-level Circuit Design

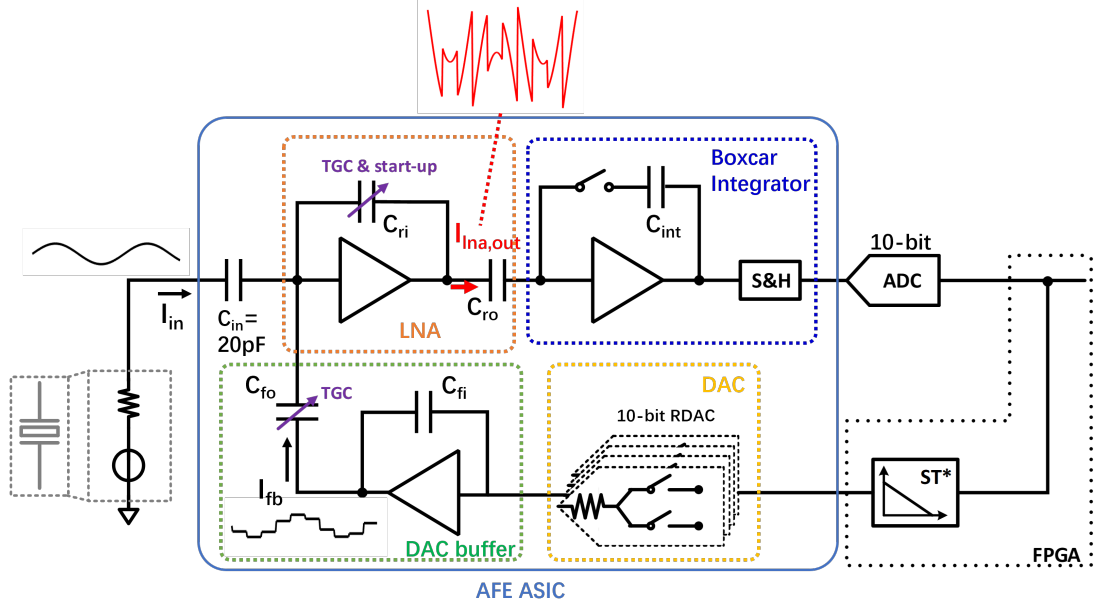


Figure 3.1.: System circuit block diagram

the biggest closed-loop gain scenario, where $C_{ri} = 281fF$ and $C_{ro} = 40pF$. This translates to a feedback factor of

$$\beta = \frac{C_{ri}}{C_{in} + C_{fo} + C_{ri}} = -39.55dB \quad (3.1)$$

To meet our target loop gain of $A\beta$ greater than 10dB at the signal bandwidth of interest, which is essential for non-linearity suppression and gain accuracy, we require a minimum open-loop gain of 50dB.

This high open-loop gain requirement eliminates the possibility of a single-stage implementation, as it would necessitate a unity gain frequency exceeding the 300MHz range, especially when considering a 20dB/decade roll-off. Achieving such a high frequency in 180nm technology is challenging.

When considering a two-stage design, careful attention must be paid to pole placement to avoid stability issues. In this design, the pole placement becomes more complex when taking the startup phase into account. During this phase, the feedback capacitor may start with a value of 4pF when the clutter cancellation is incomplete. This translates into a feedback coefficient 10 times smaller than the previous discussion. Optimizing the pole for the highest feedback coefficient will result in insufficient phase margin at start-up phase, while optimizing for the lowest one will result in inadequate loop gain when TGC is applied.

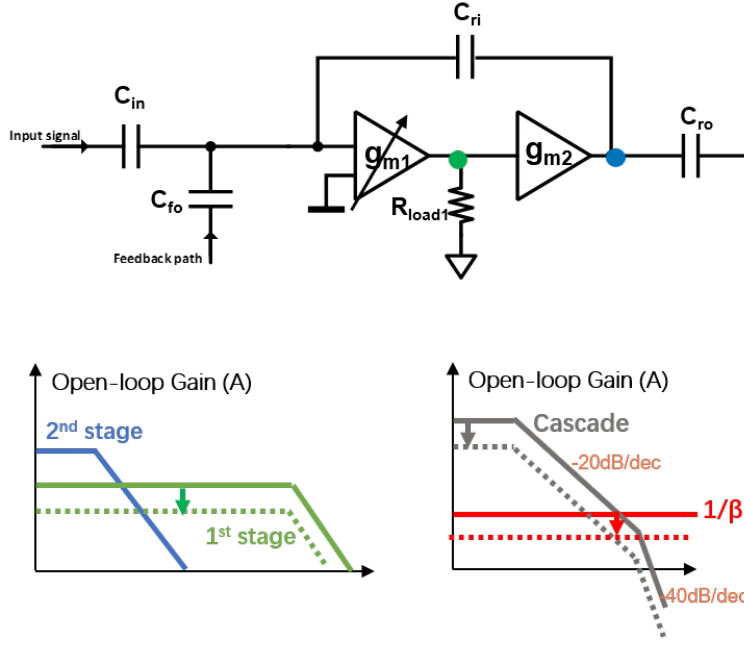


Figure 3.2.: Illustration of two-stage amplifier LNA topology design with a resistive loading 1st stage

Sharing a similar design challenge of a varying feedback coefficient, this design adopts a two-stage topology inspired by the front-end amplifier design in [32]. The topology is shown in Figure 3.2. Unlike most two-stage amplifiers, this design positions its main pole as the output pole, while the inter-stage pole serves as the second pole. This configuration is suitable for our system design, as the loading for this amplifier is clearly defined. In the first stage, a resistor is employed for loading, which results in the creation of a high-frequency pole at the inter-stage node. This pole is formed due to the presence of the loading resistor and parasitic capacitors. Importantly, this pole can be effectively isolated from the low-frequency output pole to ensure system stability. One notable advantage of this design is its ability to maintain required loop gain and phase margin by adjusting the transconductance (g_m) of the first stage in response to variations in the feedback coefficient.

Another significant design challenge within this topology pertains to noise considerations. It is hard to obtain low noise and efficient loop gain at the same time. It can be illustrated with the analysis below. The output current with a input current I_{in} can be derived as:

$$I_{out} = \frac{c_{ro}}{C_{ri}} \frac{1 - s/\omega_{zero}}{1 + s/\omega_{BW}} \quad (3.2)$$

$$\omega_{BW} = \frac{g_m}{2\pi[C_i + (C_{ro} + C_{rop})(1 + \frac{C_i}{C_{ri}})]} \quad (3.3)$$

3. Block-level Circuit Design

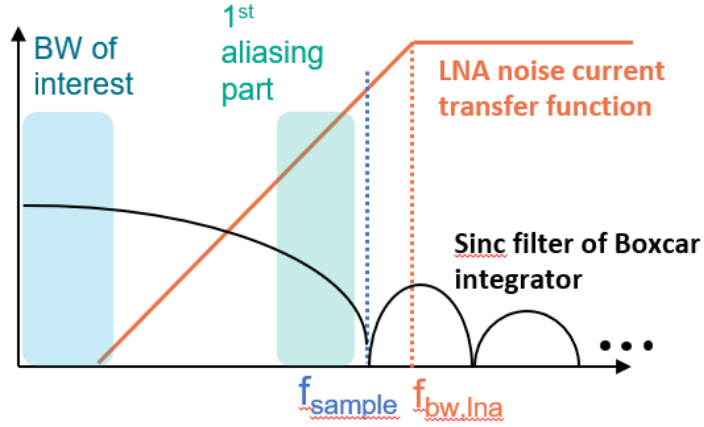


Figure 3.3.: Illustration of LNA noise contribution

g_m is used to describe the equivalent transconductance of this two-stage amplifier. With the LNA noise modeled as a current source injecting noise current I_n at LNA output, it has the output noise current of:

$$I_{out,n} = \frac{c_{ro}}{(C_{ri}/C_i) + C_{rop} + C_{ro}} \frac{s}{1 + s/\omega_{BW}} I_n \quad (3.4)$$

The full derivation is available in the Appendix B. At the LNA output, the noise current transfer function features a pole same with the LNA's bandwidth, as represented by the orange curve in Figure 3.3. To understand the noise's influence on the system output, the Boxcar integrator's transfer function is also considered. The high-pass LNA output current noise is subsequently filtered by the Boxcar integrator's sinc function before sampling. The primary contribution of LNA noise to the system output emerges from the out-of-band portion aliased back into the signal bandwidth post-sampling. An increase in LNA bandwidth leads to more noise being aliased into the desired signal band.

Therefore, considering the LNA bandwidth be fixed by the loop gain requirement, another filtering stage is needed to suppress noise.

To achieve this, a resistor is placed in cascade with the output capacitor to introduce a low-pass characteristic for the output current, with the corner frequency at approximately 3MHz. This resistor is designed to be trim-able, allowing for further optimization between bandwidth and noise performance. Consequently, the finalized LNA diagram, along with device sizing, is presented in Figure 3.4.

The transistor-level implementation of the two-stage amplifier is illustrated in Figure 3.5. The design of the first stage and the Common-Mode Feedback (CMFB)

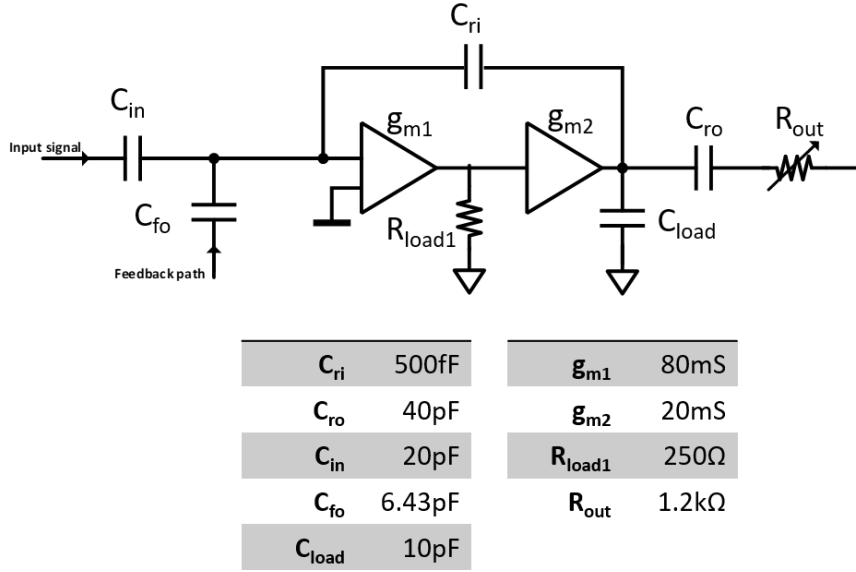


Figure 3.4.: Schematic of the LNA and device sizing

circuit is inspired by the amplifier presented in [32]. The first stage is a fully differential current-reuse stage with cascode transistors. The incorporation of the cascode structure serves to reduce parasitic capacitance between the input and the inter-stage output. For the loading stage, transistors with diode connections are chosen for implementation. This choice ensures a matching conductance between the two branches, resulting in a well-defined first-stage gain expressed as $g_{m,1}/g_{m,load}$. The second stage is also a current-reuse amplifier which performs differential-to-single-end conversion, which will be also discussed in the DAC buffer design.

A biasing control, which consists of switched current sources, is designed to control the biasing current of the first stage. At the start-up phase, when the feedback coefficient is large, the biasing current is reduced to maintain stability. During TGC, the biasing current is increased to maintain loop gain and reduce input-referred noise.

The simulated results of the LNA are presented in Figure 3.6. As discussed earlier, the control for the first stage functions effectively, ensuring sufficient loop gain within the desired signal bandwidth and maintaining stability. However, the noise suppression at the maximum gain is constrained. This is caused by two primary factors. The first is the swing requirement of the first stage, which limits the overdrive voltage of each transistor, subsequently preventing further increases in biasing current. The second factor is the contribution of the $1/f$ noise, which remains constant and doesn't scale with the current consumed. Both challenges can be mitigated by more meticulous sizing of the transistors, suggesting potential areas for future improvement.

3. Block-level Circuit Design

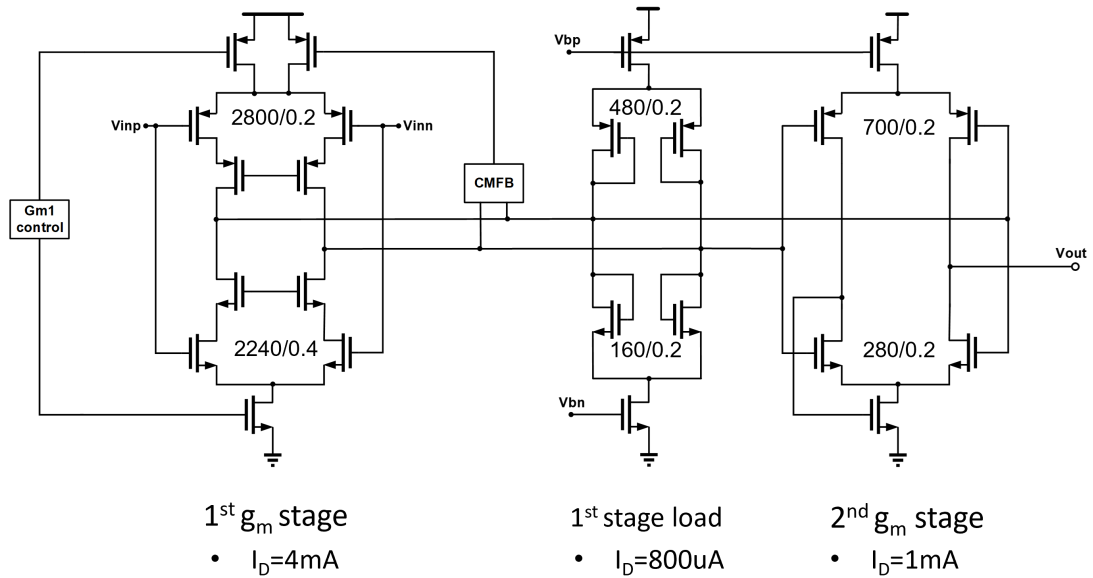


Figure 3.5.: Transistor-level implementaion of the LNA

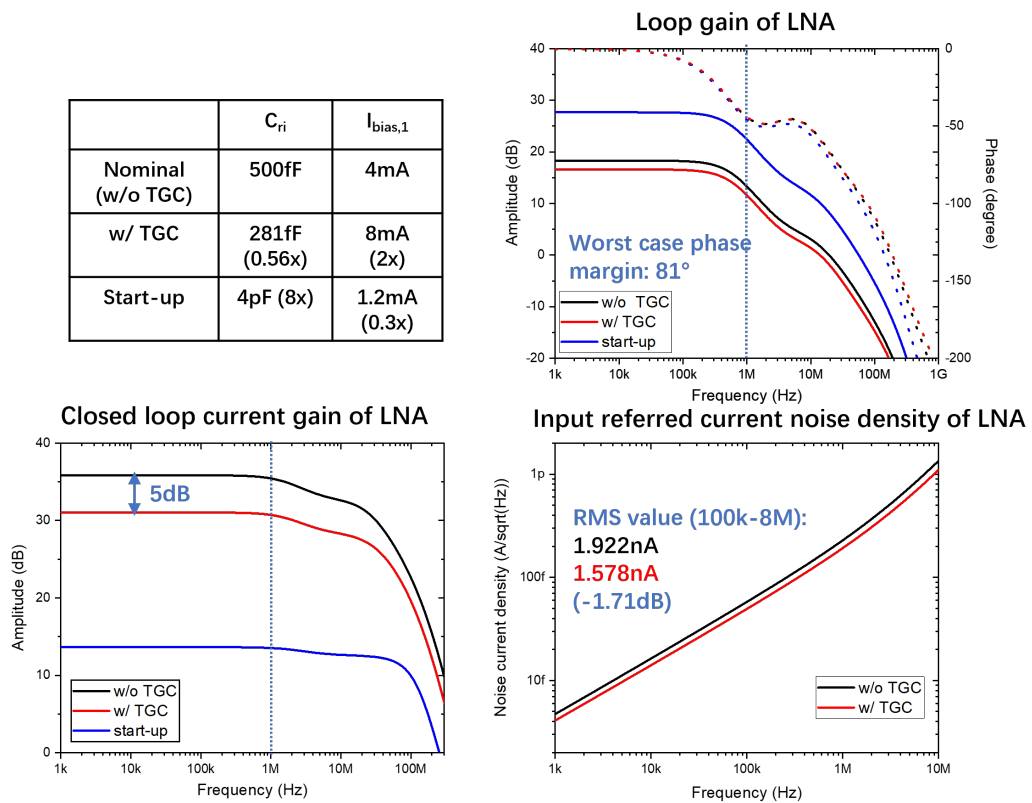


Figure 3.6.: Simulation results of LNA

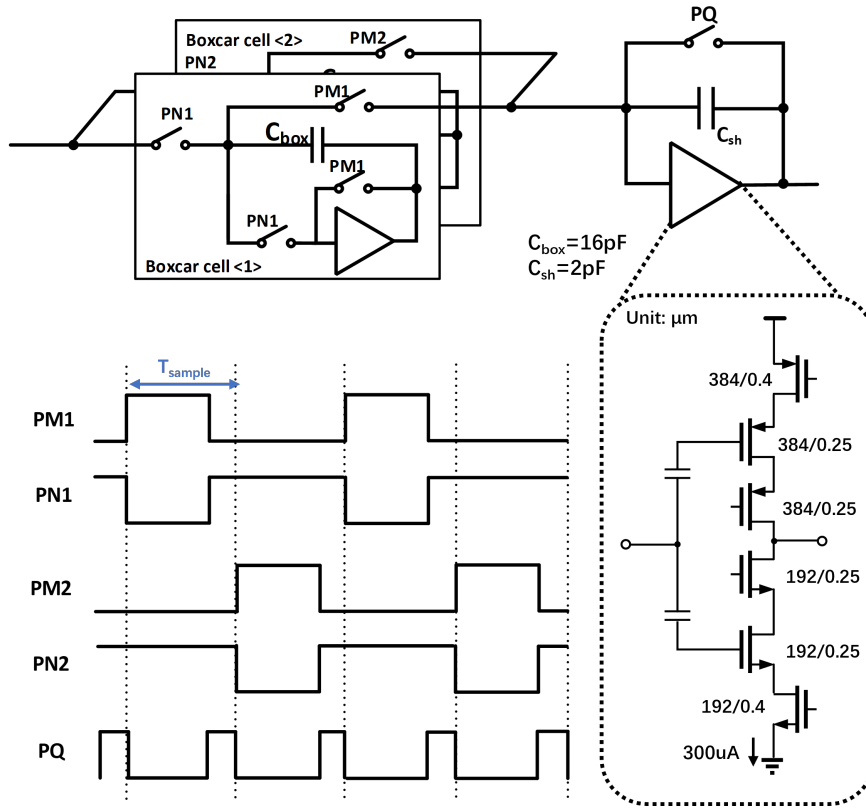


Figure 3.7.: Schematic and timing diagram of Boxcar integrator

3.2. Boxcar Integrator

With the cancellation node positioned at the input of the LNA, subsequent blocks within the receiving path have significantly reduced noise and swing requirements. In this design, the boxcar integrator closely follows the design outlined in [33]. A comprehensive schematic and timing diagram can be found in Figure 3.7.

The boxcar integrator primarily operates in two stages. The first consists of ping-pong operated Boxcar cells that alternately perform windowed integration. The second stage functions as a capacitively-coupled amplifier, amplifying the final voltage of the Boxcar cells at the conclusion of each integration window. The capacitor ratio between C_{box} and C_{sh} defines the gain. This gain is essential because, at the output of the Boxcar cell, the maximum swing is typically much greater than the final sampled value, as illustrated in Figure 2.9.

The operation of the boxcar integrator can be divided into two phases. During the first phase, controlled by PN , the C_{box} connects to the input current for integration. In the subsequent phase, managed by PM , C_{box} connects to the second stage. As

3. Block-level Circuit Design

both of its plates now connect to the virtual ground voltage, the final charge stored on C_{box} transfers to C_{sh} . These phases are ping-pong operated between the two Boxcar cells: while one integrates the currents, the other manages charge extraction. The reset phase is governed by PQ . Notably, the output of the second amplifier already offers a sampled voltage, facilitating further processing by the subsequent ADC and reducing the strictness of sampling clock alignment requirements.

The three OTAs in the block cells are identical and its schematic as shown in the inset of Figure 3.7. Based on the design in [33], the OTA is an inverter-based, single-ended input to single-ended output amplifier, equipped with a local feedback loop (not shown in the figure) to stabilize its DC operating point. Each consumes a current of $300\mu A$ and provides a g_m of approximately $12mS$.

3.3. DAC

The DAC operates in the current domain. The most crucial specifications focus on noise, as the overarching aim of this design is to incorporate a feedback path for dynamic range relaxation without introducing a significant additional noise burden. Furthermore, linearity and bandwidth must be meticulously designed to avoid degrading the overall SNR and inducing stability issues.

Several options are available for DAC implementation. The Resistive DAC (RDAC) and Current Steering DAC (CS-DAC) are two popular choices [34]. Both can obtain low-noise performance by allocating more power. When power doubles, the signal also doubles, whereas the noise increases only by the square root of this increment. An advantage of RDAC is that, for the same current consumption, it yields lower thermal noise [27]. However, RDAC's disadvantages include a reduced output resistance, determined by its total resistance, which can load the subsequent amplifier and diminish loop gain. Moreover, its speed is restricted by the RC constant of the switching node. Given the buffer following for drive capability and the targeted 1MHz signal bandwidth, the RDAC seems a more favorable choice due to its guaranteed lower noise. Another DAC type often utilized in continuous-time delta-sigma modulators is the Switched Capacitor DAC, which boasts enhanced jitter immunity [35]. Nevertheless, it produces a spike-like current demanding a high bandwidth from the LNA, making it unsuitable for this design. Consequently, the RDAC is the chosen approach for this design.

The linearity performance of the RDAC is tied to its code representation. A full unary structure offers excellent matching but necessitates thousands of unit resistors, leading to area and routing challenges. Additionally, the unary structure yields a unit resistor in the $M\Omega$ range, challenging to implement given process constraints. In contrast, a binary structure facilitates routing and conserves space, especially in configurations like the R-2R topology that demands fewer unit resistors. However, it falls short in terms of matching. To strike a balance between linearity and area

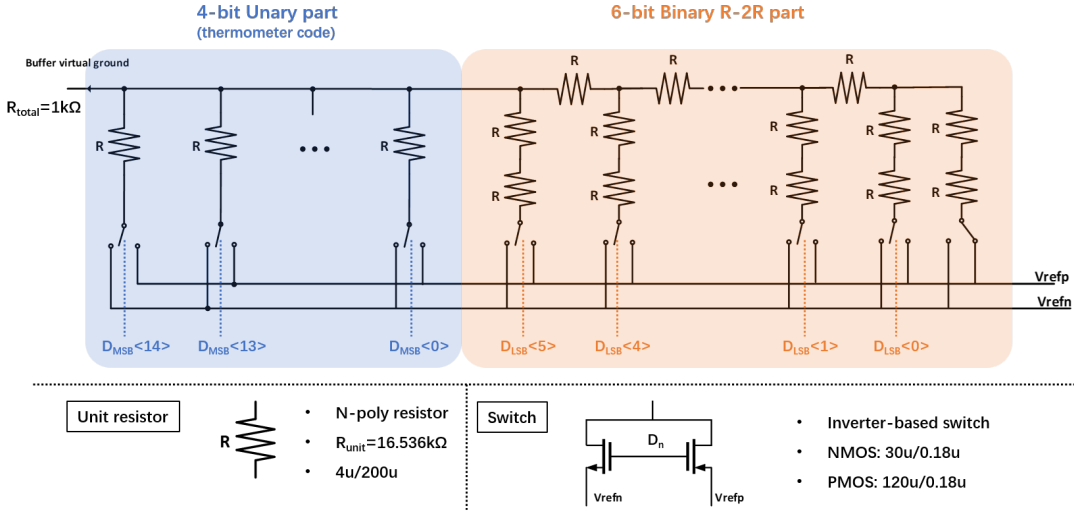


Figure 3.8.: Schematic of 10-bit hybrid RDAC

considerations, a hybrid structure combining a 4-bit unary MSB with a 6-bit binary LSB is selected for this design.

Consequently, a 10-bit hybrid RDAC is selected for this design. The schematic of the DAC block, along with component sizing, is presented in Figure 3.8. While the 4-bit binary to thermometer decoder is not depicted in the figure, it is implemented using standard logic cells. The decoder contributes negligible power consumption and delay in comparison to the resistor ladder.

The unit resistor value is determined based on the noise requirement, and its area is sized to account for mismatch. With R_{total} of $1k\Omega$, which translates to maximum output current of $0.9mA$ and LSB current of $1.75\mu A$. The switch is designed to have an on-resistance significantly lower than the unit resistor, aiming to reduce non-linearity and enhance speed.

Linearity was assessed using Monte Carlo simulations. The design meets the specified criteria, with the maximum DNL being less than $0.28LSB$ across different corners corners at a 3σ tolerance. Furthermore, the system's speed was tested for a bandwidth of $80MHz$, revealing that the phase delay is negligible.

3.4. DAC Buffer

The primary role of the DAC buffer is to reconcile the mA -scale DAC current with the $10\mu A$ -scale input current while also delivering TGC at its output. It must provide a substantial output swing to manage the integrated voltage resulting from the full-scale clutter current originating from the feedback DAC. Additionally, the noise from

3. Block-level Circuit Design

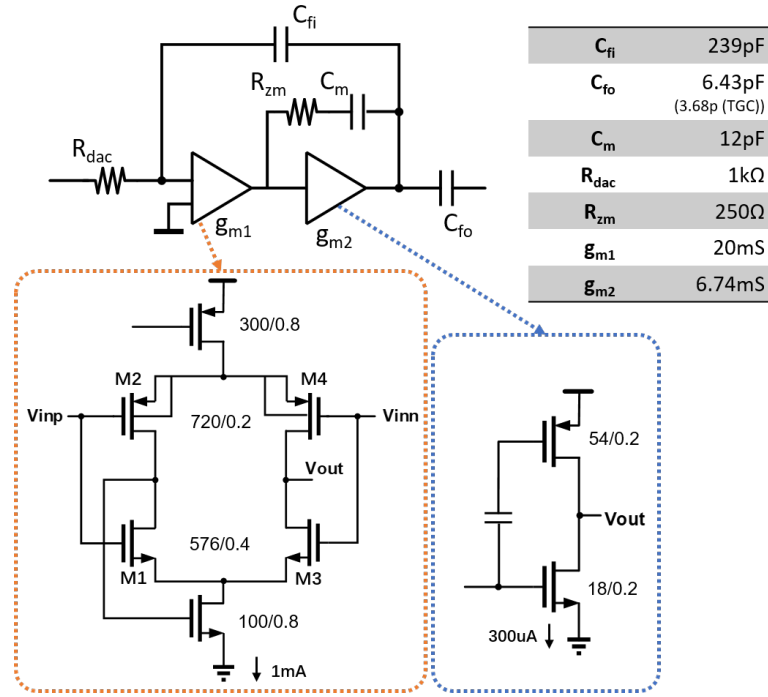


Figure 3.9.: Schematic of the DAC buffer: a two-stage amplifier with Miller compensation

this buffer should be meticulously controlled to ensure it doesn't contribute more noise than the DAC itself.

Consequently, a two-stage amplifier has been implemented, as depicted in Figure 3.9.

The first stage is optimized for noise performance. It utilizes a topology similar to the front amplifier design as described in [36]. A current-reuse configuration is chosen to double the g_m . Moreover, input pairs are biased close to sub-threshold region for achieving high g_m efficiency. The positive input branch output is fed into the tail transistor, forming a local feedback loop. This local feedback loop forces the source of M1,M2 to track the variation of V_{inp} and then converts to output current at the output node through M3,M4. This enables the implementation of a current-reuse topology for a differential input and singled-ended output amplifier. Note that the input NMOS pairs are not using minimum length for the purpose of $1/f$ noise reduction.

The second stage is a simple push-pull stage optimized for output swing. Each transistor is biased with an overdrive voltage of 100mV, thus allowing an output swing of 1.6V. The DC biasing circuit isn't depicted in this figure, but the bias current is approximately 6 times the dynamic output current, which is scaled for the distort-

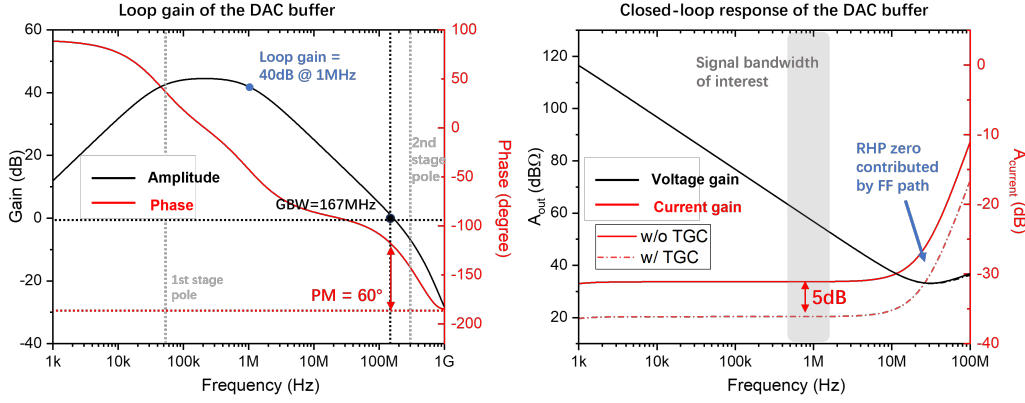


Figure 3.10.: Simulated loop gain and closed-loop response of the DAC buffer

tion requirement and also for solving the feed-forward right-half-plane (RHP) zero, which will be discussed later. A Miller cap C_M is used for the stability compensation and a resistor R_{zm} is introduced to cancel the right-half-plane (RHP) zero introduced by the Miller cap.

The simulated loop gain and the current signal transfer function are presented in Figure 3.10. The Miller compensation effectively ensures a phase margin of 60 degrees. Furthermore, it's evident that even though the Miller capacitor shifts the first pole to the kHz range, the loop gain remains adequate in the signal bandwidth of interest, guaranteeing gain accuracy and linearity.

A notable point of discussion is the presence of an RHP zero in the closed-loop transfer function. This arises from the large feedback capacitor utilized in the amplifier, which establishes also a strong feed-forward path. This results in a high-pass characteristic in the current transfer function as shown in Figure 3.10. While this doesn't adversely affect noise performance—given that the subsequent LNA and boxcar integrator provide low-pass filtering and bandwidth limitation. However, system stability must be carefully monitored due to the associated phase delay, as outlined in Section 2.4.4. To address this, the second-stage g_m is adjusted to push this RHP zero further from the sampling frequency.

3.5. Reference Source & Biasing

All the amplifiers in this design share the same current reference for biasing. The current reference circuit is shown in Fig 3.11(a). It is a cascode constant g_m circuit that is designed to deliver unit current of $10\mu A$. It is simulated under different corners and Monte-Carlo simulation for a current variation smaller than $\pm 20\%$.

3. Block-level Circuit Design

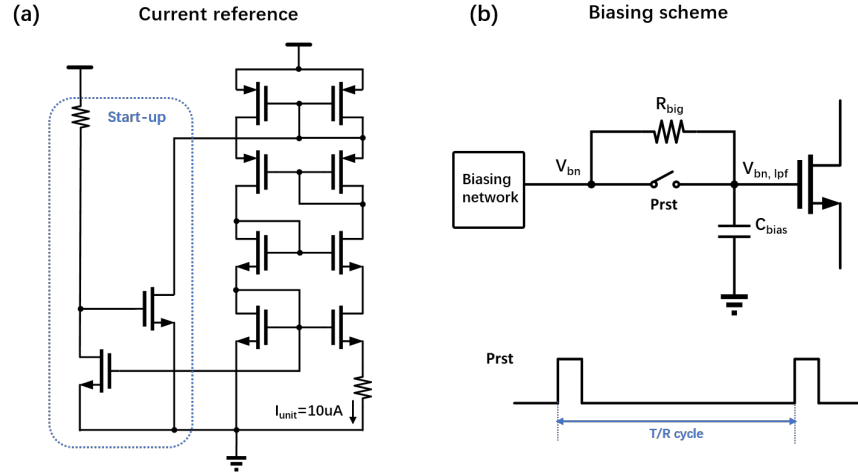


Figure 3.11.: (a)Schematic of current reference (b)Illustration of the biasing scheme

Given the system's reliance on closed-loop amplifiers, such a variation is deemed acceptable. This unit current is then routed to each amplifier via a biasing network composed of ratio-metric current mirrors.

The adopted biasing methodology is depicted in Figure 3.11(b). Typically, an RC pair is employed to minimize noise intrusion from the biasing network. Nevertheless, setting a sufficiently low low-pass corner requires a significantly large resistor or capacitor. This leads to extended system start-up times. Similar to the design in [37][38], this work adopts a biasing network with $G\Omega$ resistors which consists of turn-off transistors and an auxiliary switch. It utilizes the periodic operating nature of the ultrasound system. The switch is turned on at the reset phase of every T/R cycle for quickly establishing the biasing voltage, and turned off during operation for bias noise blocking.

4. Simulation Results

Following the design of the architecture and blocks, the system was implemented using Cadence Virtuoso and was then validated. The ADC and the slow-time loop filter were simulated using their Verilog-A models, ensuring comprehensive mixed-signal system simulation. The specifications for the ADC are based on [36]. It is worth noting that, for this work, the ADC was not implemented at the ASIC level due to the limitations of the thesis scope. However, for a complete system, an on-chip ADC is clearly preferred. Using a single-ended output with an off-chip ADC can pose challenges due to potential reference reliability issues. Moreover, the current system design is already conducive to integrating an ADC, given its sampled output and the presence of a front-end anti-aliasing filter.

4.1. Waveform & Spectrum

The system testbench is configured to mirror the Matlab benchmark described in Chapter 2. The input signal comprises two components. The first is a static signal with an amplitude of $200mV$ at $1MHz$, which remains consistent throughout each T/R cycle. The second component is a Doppler signal at $1.2MHz$. Though this signal is $57dB$ weaker than the static signal, it demonstrates a consistent phase shift between each T/R cycle. Figure 4.1 depicts the wave-forms representing the outputs from various blocks of the system. The purpose of this simulation is to demonstrate the system's behavior in clutter cancellation, with transient noise excluded for the sake of simulation speed.

The start-up phase is depicted on the left side. This phase shows that the feedback path incrementally captures the static clutter, leading to a swing reduction at the outputs of both the LNA and the boxcar integrator. It's important to note that the gain is tempered during this phase to prevent system saturation; thus, its absolute value is only indicative. After the first 20 cycles, which constitute the designed start-up phase, the system reaches its convergence state. The zoomed-in waveforms for this state are displayed on the right. At this juncture, the feedback branch effectively isolates the clutter component without compromising the Doppler signal. The outputs from the LNA and boxcar integrator primarily consist of the faint Doppler signal and the static quantization noise derived from the cancelled clutter segment. This is further elucidated by the spectrum shown in 4.2. As depicted in the last spectrum, the clutter tone vanishes, and the noise floor rises.

4. Simulation Results

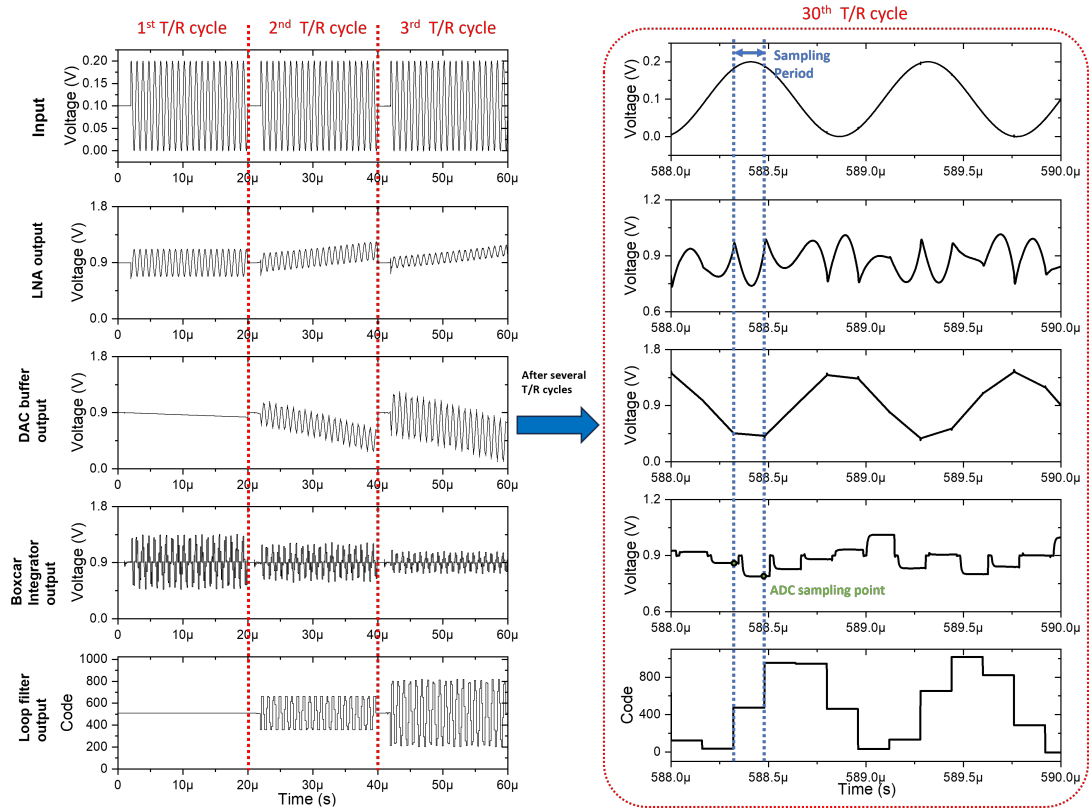


Figure 4.1.: Simulated waveform of the system

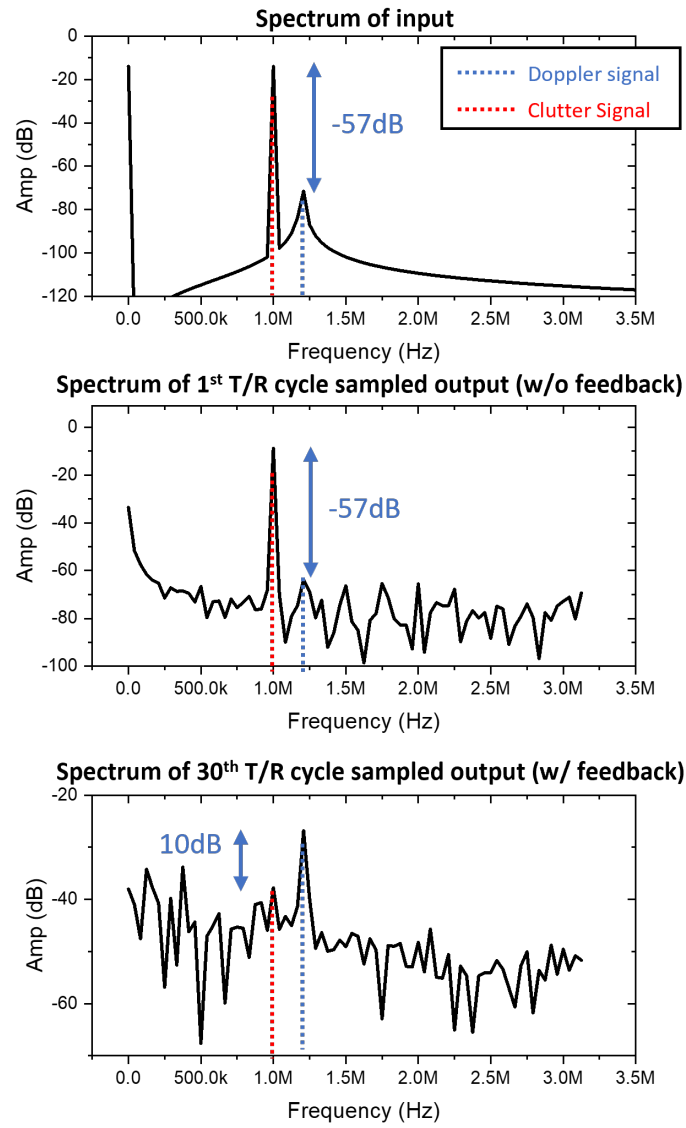


Figure 4.2.: Simulated spectrum of the system demonstrating the clutter cancellation

4. Simulation Results

Another noteworthy observation from the waveform needs to be addressed. As illustrated in 4.1, prominent voltage drifts can be observed at the initial outputs of both the LNA and the DAC buffer. These drifts can be traced back to the DC current input, which arises from the offset in all the blocks within the loop. Given that every block in the current simulation operates in a single-ended fashion, a mismatch in the common-mode level is inevitable, leading to the offset. For instance, the RDAC's output is channeled into the virtual ground of the buffer, and this deviates by 1mV from the global common-mode voltage due to the amplifier's limited gain. This causes a common-mode voltage mismatch between the ADC and the DAC. When the gain is at its lowest, this DC current stays beneath the ADC's LSB, thus not activating the feedback. However, once the gain returns to its designated value, this drifting ceases. This is, in fact, a significant concern that merits attention in subsequent works. If the T/R cycle duration is extended, this DC drift could saturate integrator blocks like the LNA and the DAC buffer, considerably delaying the convergence time. Transitioning to a differential mode offers a potential remedy, which will be elaborated upon in Section 5.2.2.

Due to limitations in simulation time, the output reconstruction filter with an equalizer has not been included at this juncture, considering its training process is significantly time-consuming. A detailed demonstration of this aspect will be deferred to future work. Instead, for the purpose of simulation and validation, the system employs a specific approach. After the start-up phase, the system operates for an additional 10 cycles in an open loop, ensuring that the input to the feedback path remains consistent. Following this, clutter residue is removed by subtracting the signal from its averaged counterpart. This method represents a basic form of slow-time filtering, where the primary objective is to eliminate the slow-time DC component. As a result, what's left is predominantly the Doppler signal intertwined with the system's thermal noise. The relevant spectrum is depicted in Figure 4.3. This simulation is to demonstrate the system noise behavior with transient noise included.

The simulation was conducted under standard settings (TT corner) at room temperature, using the highest input amplitude. The resulting Doppler SNR is 32.59dB. Given that the maximum input is defined by the clutter part, which is 56.98dB higher than the Doppler tone, the system's dynamic range (DR) can be calculated as $DR = 32.59 + 56.98 = 89.57dB$.

4.2. Power

The power distribution of the system is presented in Figure 4.4. As noted earlier, while the ADC is not realized at the transistor level in this research, its specifications, such as resolution and input range, are based on the successive-approximation (SAR) ADC design detailed in [36]. The power consumption value is also sourced from this reference. It's crucial to recognize that this could be an overestimation. The

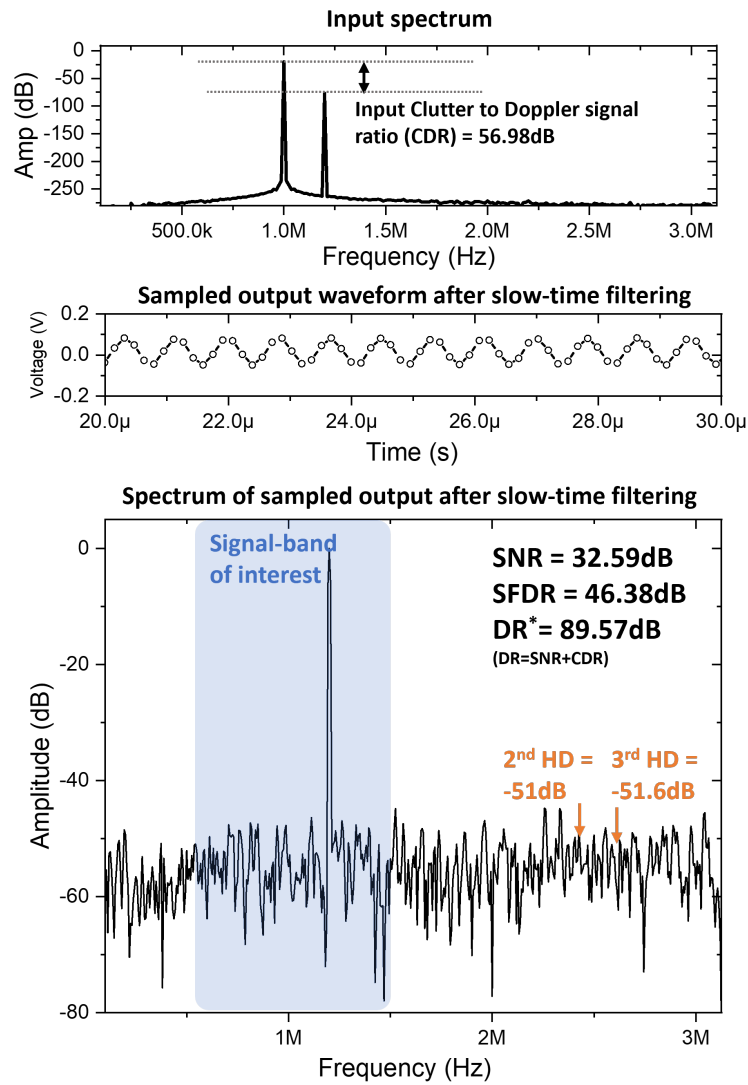


Figure 4.3.: Simulated spectrum of the system demonstrating the noise behavior

4. Simulation Results

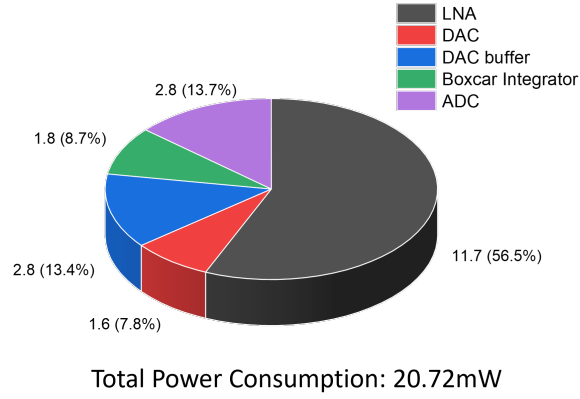


Figure 4.4.: Power breakdown of the system

reason being, the sampling frequency for the current system has been reduced from 60MHz to 6.25MHz, and a decrease in sampling frequency typically corresponds to a decrease in power consumption for SAR ADCs.

Power is typically expended in a trade-off with noise. As the figure illustrates, the LNA dominates the system's power consumption. This is understandable since the LNA is the primary determinant of noise for the entire system. The feedback path accounts for less than a quarter of the total power usage, which aligns with the design's aim to incorporate a cancellation path without a significant increase in power overhead. Interestingly, even though the DAC defines the noise from the feedback path, its power consumption is still lower than that of the DAC buffer. The decision not to further refine the power-noise balance was made because reducing the DAC resistor further would necessitate a larger feedback capacitor for the buffer. Such a change would increase the capacitor size, approaching the nF range, resulting in an undesired increase in area. The power consumption of both the boxcar integrator and ADC are also significantly smaller compared to the LNA, aligning with the goal of a simplified ADC design.

However, it's essential to note that its power consumption exceeds the initial expectations set during the architecture design phase, which was estimated to be about 10mW. This estimate began by determining the transconductance (g_m) each block required to achieve its bandwidth or noise requirement. From there, the bias current was derived, assuming a conservative biasing point of $g_m/I_d = 15$. The discrepancy arises primarily for two reasons. First, ideal model analysis considered only thermal noise, but in the actual design $1/f$ noise remains considerable within the

1MHz. Additional power was allocated to suppress the thermal noise to fit the original overall noise budget. The second reason relates to the prior calculations being based on a single-ended-input amplifier, where only one branch consumed power and contributed to noise. In this design, both the LNA and DAC buffer adopt a differential-input-single-ended-output topology due to design complexities. This choice doubled the power consumption since two branches are necessary to achieve the same g_m . This observation suggests a potential improvement in increasing LNA power efficiency by redesigning the block using a single-ended amplifier.

4.3. Comparison with State-of-the-art Designs

A comparison table has been crafted to highlight the potential of the proposed solution. Since no previous AFE ASICs have been specifically designed for Doppler ultrasound applications, the papers chosen for comparison are grounded on traditional Doppler system topologies. These generally incorporate a high-resolution ADC ($> 14\text{bits}$) that samples directly and performs slow-time filtering in the digital domain.

However, many ADC-focused publications design their ADCs to cater to an input signal swing that considerably surpasses the maximum output voltage of the transducer. Consequently, there's a demand for a low-noise, low-distortion amplifier to drive the ADC. Regrettably, the details of this driver amplifier are frequently glossed over in most ADC publications.

For a fair comparison, for those papers that don't specify but evidently need a driver, an additional figure-of-merit (FOM) is introduced. This FOM draws on the specifications from cutting-edge, off-the-shelf amplifiers. To accommodate a $V_{pp} = 200\text{mV}$ signal input without undermining the SNR performance of the ADCs, the selected driver amplifier boasts an input-referred noise density of $1.25\text{nV}/\sqrt{\text{Hz}}$ and a bias current of 10mA as detailed in [39]. The power consumption for each design is subsequently calculated by multiplying its bias current with the employed reference voltage. It's worth noting that for the FOM calculation of this work, instantaneous dynamic range (DR) is utilized.

4. Simulation Results

References	This work	Li[40] ISSCC'23	Elshater[41] ISSCC'19	Ho[42] ISSCC'15
Technology (nm)	180	180	180	55
Supply (V)	1.8	3.3	3.3	1.8
Bandwidth (MHz)	1	6	1	2.2
DR(dB)	89.6 ¹	94.1	95	92
ENOB(bits)	14.6	15.3	15.5	15.0
Power(mW) (w/ driver)	20.72	30.41(63.41)	1.61(34.61)	4.5(22.5)
FOM*(dB) ²	166.4	177	182.9	177.3
FOM w/ driver (dB)	166.4	173.9	169.6	171.9
Output bits per sample	10	22	18	N/A

¹ TGC not included

² $Fom = DR + 10\log(BW / Power)$

Table 4.1.: Comparison table of system with state-of-the-art design

The system demonstrates a FOM that is competitive with state-of-the-art designs. Additionally, it offers other advantages such as a reduced output data flow and simpler design complexity.

5. Conclusion

5.1. Thesis Contribution

In this study, an analog front-end ASIC system designed for transcranial Doppler ultrasound systems is presented. By leveraging feedback to eliminate the clutter portion at the transducer output, the entire receiver chain—comprising the LNA and subsequent ADC—benefits from a relaxed dynamic range. Additionally, a slow-time integrator is incorporated to close the loop, ensuring the feedback path tracks the static clutter without compromising the Doppler signal.

At the architectural level, we delve into the design considerations of system parameters, specifically discussing ADC & DAC resolutions and sampling frequency. The system's susceptibility to circuit non-linearities, such as DAC mismatch and excess loop delay, is also scrutinized. An adaptive equalizer-based output reconstruction filter is proposed to counteract the reconstruction errors stemming from the excess loop delay. Ultimately, a model is formulated, providing insights into the stability of a dual time-scale feedback system. This serves as a foundation for forthcoming endeavors and similar system designs.

On the circuit implementation front, the primary AFE blocks are crafted in alignment with specifications derived from the architectural design phase. We meticulously assessed and actualized each block's topology. Specifically, the DAC was realized as a hybrid RDAC, the LNA took the form of a two-stage amplifier with resistive broadbanding with efficient loop gain control provided, and the DAC buffer was designed as a two-stage Miller compensated amplifier. System simulations affirmed the successful operation of the loop. The analog front-end system achieved an dynamic range of 89.57dB and consumed a power of 20.72mW.

5.2. Future Work

5.2.1. Remaining Prototype Implementation

First of all, it has to be admitted that the current system simulation results are more of intermediate results. The whole architecture design with reconstruction and equalizer results are not tested at the transistor level yet. In the current system

5. Conclusion

simulation, the spectrum is obtained by opening the loop and performing readout, which is not practical for a real application. For fulfilling a real closed-loop readout, a reconstruction filter should be implemented and tested based on the frequency response of the real circuits. Then, the influence of the feedback branch non-linearity can be examined and evaluated.

Second, as discussed in Chapter 4, an on-chip ADC still needs to be incorporated in this design with also a single-end-to-differential buffer required. Several other auxiliary blocks also need to be implemented, including the timing blocks for the Boxcar integrator.

Thirdly, a more comprehensive evaluation of the system results is needed. The influence of process-voltage-temperature (PVT) variation on system performances has not been examined yet.

Final steps towards an experimental prototype include layout design, chip fabrication and measurement.

5.2.2. Potential Improvements

From the architectural design perspective, several alternatives can be explored as improvements to enhance system reliability and facilitate the process of simulation and demonstration.

- The design consideration of going single-ended or differential needs to be examined. For this design, all the blocks are single-ended based on the consideration that the transducer is usually single-ended, with the other node typically connected to the ground foil. However, for a single-element transducer-based system, this assumption might not hold true as the ground foil doesn't need to be shared. Going fully differential provide many benefits including better system PSRR, improved swing at DAC buffer output, easier i/o design with ADC, and importantly, immunity from DAC buffer amplifier offset. Even if using a single-ended transducer is necessary when considering matrix implementation, partially going differential still helps. For example, making DAC buffer differential-to-single-ended and the DAC fully differential.
- The other point concerns the design consideration of either going with current-domain processing at the output of the LNA. For this design, it adopts a boxcar integrator that processes the output current of the LNA. This brings the benefit of intrinsic anti-aliasing filter. However, the output noise current has a high-pass characteristic which results in an extra stage of filtering needed, which seems no improvement in noise perspective. Current-domain operation means there is no control for the DC or low-frequency voltage at the LNA output, the LNA output is an integrator to the input current and is easily saturated when there is a small DC current from feedback path and the T/R cycle is sufficiently

long. An alternative way might be using a resistive-feedback transimpedance amplifier (TIA) as LNA and go for voltage mode processing for the following blocks.

A. STF and NTF Derivation of Slow-time Delta Modulator

In this appendix, the signal transfer function (STF) and noise transfer function (NTF) of the slow-time delta modulator is discussed. Furthermore, the situation when output reconstruction is taken into account is also elaborated.

The block diagram of the proposed slow-time delta modulator and its equivalent model are shown in Figure A.1. The influence of the ADC can be modeled as a unity-gain block with a quantization noise e_{adc} added upon. The quantized signal then enters the loop filter $L(z')$ which is implemented in FPGA. It is assumed to operate with values encoded as 64-bit length floating-point number. Thus when its output enters the DAC, it also experience a quantization error e_{dac} . Note that even if this is called e_{adc} , this error is actually from the rounding operation inside the FPGA instead of the DAC block itself.

Thus, the STF and NTF can be derived as follows. This derivation is based on linear system assumption that each signal source can be separated.

Derivation of STF from node u to node v:

$$\begin{aligned} v &= A_{rx}(u - A_{fb}L(z')v) \\ v &= \frac{A_{rx}}{1 + A_{fb}A_{rx}L(z')}u \end{aligned} \quad (A.1)$$

Derivation of NTF from ADC to node v:

$$\begin{aligned} v &= e_{adc} - A_{rx}A_{fb}L(z')v \\ v &= \frac{1}{1 + A_{fb}A_{rx}L(z')}e_{adc} \end{aligned} \quad (A.2)$$

Derivation of NTF from DAC to node v:

$$\begin{aligned} v &= -A_{rx}A_{fb}(e_{dac} + L(z')v) \\ v &= -\frac{A_{rx}A_{fb}}{1 + A_{fb}A_{rx}L(z')}e_{dac} \end{aligned} \quad (A.3)$$

Note that A_{rx} is used to amplified the Doppler signal after the clutter part is cancelled. A_{fb} is used to matched the DAC signal with the input signal. If we assume

A. STF and NTF Derivation of Slow-time Delta Modulator

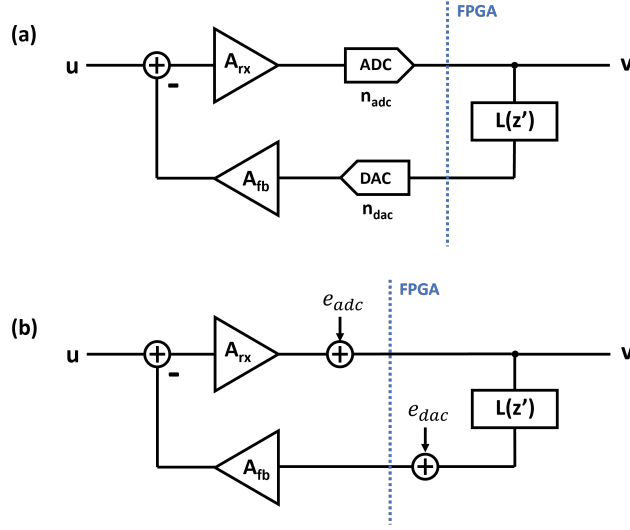


Figure A.1.: (a)Block diagram and (b)equivalent model of slow-time delta modulator

that in all blocks the maximum signal amplitude is normalized to 1. Then $A_{fb} = 0dB$ and $A_{rx} = 57dB$ according to the specs. Thus, we can see that in the receiver path, the quantization noise is mainly from the DAC. And the NTF of DAC quantization noise is same as STF.

The DAC quantization noise will be eliminated with the output reconstruction. The block diagram of the whole system with output reconstruction is shown in Fig A.2.

Derivation of STF from node u to node y:

$$\begin{aligned} y &= (1 + A_{rx}A_{fb}L(z'))v \\ y &= A_{rx}u \end{aligned} \tag{A.4}$$

Derivation of NTF from ADC to node y:

$$\begin{aligned} y &= (1 + A_{rx}A_{fb}L(z'))v \\ y &= e_{adc} \end{aligned} \tag{A.5}$$

Derivation of NTF from DAC to node y:

$$\begin{aligned} y &= (1 + A_{rx}A_{fb}L(z'))v + A_{rx}A_{fb}e_{dac} \\ y &= -A_{rx}A_{fb}e_{dac} + A_{rx}A_{fb}e_{dac} \\ y &= 0 \end{aligned} \tag{A.6}$$

Thus, by output reconstruction, only the quantization noise of ADC is shown at the system output.

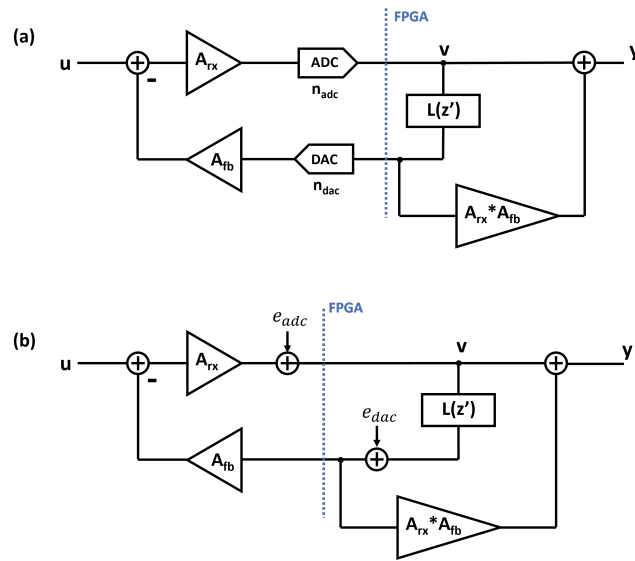


Figure A.2.: (a)Block diagram and (b)equivalent model of slow-time delta modulator with reconstructed output

B. LNA Analysis

In this appendix, the current gain of LNA and also the noise gain are analysed. The amplifier is based on a capacitively-coupled amplifier with a output capacitor to offer a current output. The schematic is shown in Figure B.1. As discussed in Chapter 3, the inter-stage pole is at a very high frequency away from signal bandwidth of interest. Therefore, the two-stage amplifier can be modelled using a single-stage OTA with equivalent transconductance $g_m = g_{m1}R_{load1}g_{m2}$.

For the first-order calculation, the output resistance of the OTA is neglected, and the small-signal model is plotted in Figure B.2.

For the input transfer function with input current I_{in} , the output is calculated as shown below.

$$g_m V_x + sC_{ri}(V_o - V_x) + s(C_{rop} + C_{ro})V_o = 0 \quad (B.1)$$

$$sC_{ri}(V_o - V_x) + I_{in} - sC_i V_x = 0 \quad (B.2)$$

Combine two equation together, the output current can be derived as:

$$\frac{V_o}{I_{in}} = \frac{sC_{ri} - g_m}{sC_{ri}[g_m + sC_i + s(1 + \frac{C_i}{C_{ri}})(C_{ro} + C_{rop})]} \quad (B.3)$$

$$\frac{I_o}{I_{in}} = \frac{sC_{ro}V_o}{I_{in}} = \frac{C_{ro}}{C_{ri}} \frac{sC_{ri} - g_m}{[g_m + sC_i + s(1 + \frac{C_i}{C_{ri}})(C_{ro} + C_{rop})]} \quad (B.4)$$

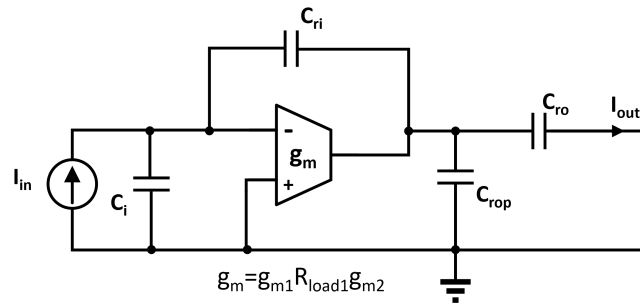


Figure B.1.: Schematic of LNA

B. LNA Analysis

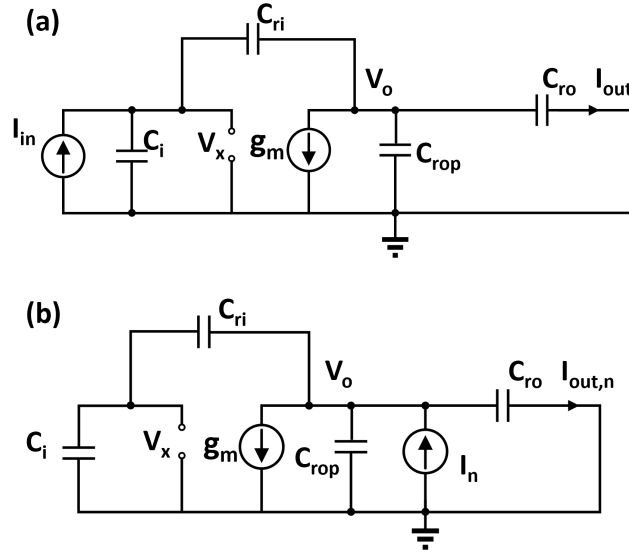


Figure B.2.: Small-signal model of LNA: (a) with current input (b) with noise current injected at output

The output current transfer function has one RHP zero and one pole. The zero is at

$$f_{zero} = \frac{g_m}{2\pi C_{ri}} \quad (B.5)$$

And the pole is at

$$f_{pole} = \frac{g_m}{2\pi(C_i + (1 + \frac{C_i}{C_{ri}})(C_{ro} + C_{rop}))} \quad (B.6)$$

which determines the bandwidth of LNA. In this design, it has $C_i \gg C_{ri}$, thus the equation can be simplified to

$$f_{pole} = \frac{C_{ri}}{C_i} \frac{g_m}{2\pi(C_{ro} + C_{rop})} \quad (B.7)$$

Similarly, the output current noise can be calculated.

$$g_m V_x + sC_{ri}(V_o - V_x) - I_n + s(C_{rop} + C_{ro})V_o = 0 \quad (B.8)$$

$$sC_{ri}(V_o - V_x) - sC_i V_x = 0 \quad (B.9)$$

Combining these two together and solving, gives

$$\frac{V_o}{I_n} = \frac{1}{g_m \frac{C_{ri}}{C_i + C_{ri}} + s(C_{ri} / C_i + C_{ro} + C_{rop})} \quad (B.10)$$

$$\frac{I_{o,n}}{I_n} = \frac{C_{ro}}{C_{ri} // C_i + C_{ro} + C_{rop}} \frac{1}{g_m \frac{C_{ri}}{s(C_i C_{ri} + (C_i + C_{ri})(C_{ro} + C_{rop}))} + 1} \quad (\text{B.11})$$

The noise transfer function has a pole at:

$$f_{pole} = \frac{g_m}{2\pi(C_i + (1 + \frac{C_i}{C_{ri}})(C_{ro} + C_{rop}))} \quad (\text{B.12})$$

which is exactly same as input transfer function. In this design, as $C_i, C_o \gg C_{ri}$, the output noise can be simplified to.

$$\frac{I_{o,n}}{I_n} = \frac{C_{ro}}{C_{ro} + C_{rop}} \frac{1}{g_m \frac{C_{ri}}{sC_i(C_{ro} + C_{rop}))} + 1} \quad (\text{B.13})$$

Therefore, it can be concluded that the noise transfer function having a high-pass characteristic with high-frequency gain approximates 1 when neglect output parasitic capacitors. This meets the understanding of a closed-loop amplifier that only in-band noise is suppressed and when the frequency is too high to be out of bandwidth the amplifier is not functioning, resulting in the output current noise being directly fed to the next stage.

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Colophon

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